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PAPER Special Section on Analog Circuit Techniques and Related Topics

Active Shield Circuit for Digital Noise Suppression in Mixed-Signal Integrated Circuits

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SUMMARY An active shield circuit which effectively reduces the substrate noise on the entire area inside the guard ring regardless of the noise source position is proposed. Simulation result shows that the proposed circuit can reduce the noise level to −85 dB while a conventional guard ring gives −52 dB.

key words: *digital noise, substrate coupling, active noise cancellation, active shield circuit, mixed-signal integrated circuits*

1. Introduction

Digital substrate noise has been known as a big issue in mixed-signal integrated circuits since it will deteriorate the performance of analog circuits [1]–[3].

A guard ring is commonly used to protect the analog circuits in mixed-signal integrated circuits from the effect of digital noise. However, this method will only reduce the noise on the surface of the substrate and has small effect on the noise coupled through the deep portion of the substrate.

Active noise reduction techniques have been proposed to handle the noise coupled through the deep portion of a substrate [4]–[12]. These circuits are implemented either off-chip or using external components [4]–[6], [12]. Circuits in [6], [12] use an AC coupling technique which needs capacitances as large as 10 μF to isolate the bias level of the circuits from substrate level. A proper DC biasing enables the implementation of a fully on-chip active guard band circuit as is introduced in [7]–[11]. However, as will be explained in section 2.2, the circuit layouts in [4], [7], [8] (refer to Fig. 2) are only effective for a particular area not the entire area inside the guard ring. In other words, a proper substrate noise suppression performance will only be obtained on a narrow area inside the guard ring. The circuit layouts proposed in [9]–[11] (refer to Fig. 3) suppress the digital noise for the entire area inside the guard ring. However as is discussed in section 2.2, it is not correctly practicable for a large chip area since the delay of the transmission line became significant.

This paper proposes a system layout which enables the noise reduction on the entire inside the guard ring and reducing the issue of transmission delay. Section 2 describes the substrate model and the conventional active shield circuit. The proposed active shield circuit will be discussed in section 3 covering the circuit layout and implementation. It will be followed by simulation results in section 4 and conclusions in section 5.

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2. Substrate Model and Conventional Circuits

2.1 Substrate Model

Since a substrate can be assumed as a resistance network [1], here a 2-dimensions substrate model as is shown in Fig. 1 is used to evaluate the performance of the active shield circuit. Here 5 substrate contacts and a guard ring are placed in the order shown in Fig. 1. Each substrate contact and the edges of the guard ring are represented by a node. Node SENSE is the input node of the active shield circuit and nodes CANCEL1, CANCEL2, and CANCEL 3 are the output nodes of the conventional circuits [7], [9], and the proposed active shield circuit respectively. Furthermore the horizontal resistance depends on the distance between two nodes and therefore the longer the distance the larger the resistance is. On the other hand, the vertical resistance depends on the size of the node and therefore a substrate contact with a wider area will have a smaller vertical resistance.

2.2 Conventional Circuits

The first type of the conventional circuit is introduced in [4], [7], [8]. The basic circuit is shown in Fig. 2. In order to simplify the calculation, unused nodes are eliminated. Here the noise source is given by a current source i_n. Calculating the transfer function from i_n to v_d and solving $v_d/i_n = 0$ will give

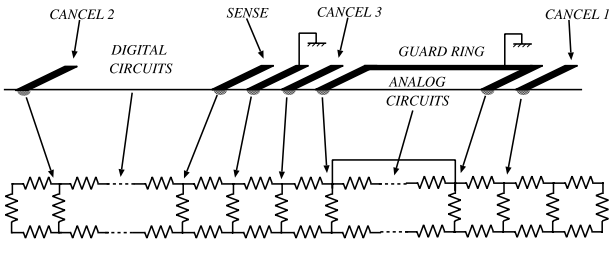

Fig. 1 Substrate model.

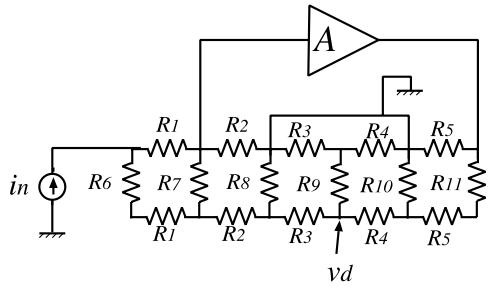

Fig. 2 Conventional circuit [4], [7], [8].

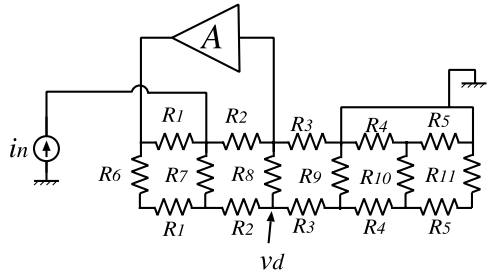

Fig. 3 Conventional circuit [9]–[11].

$$A = -\frac{(R_2 + R_A)R_B}{R_2 R_C} \tag{1}$$

where A is the amplifier's gain and

$$R_A = \frac{R_1 R_7}{2R_1 + R_6 + R_7} \tag{2}$$

$$R_B = \frac{(R_5 + R_{11})(R_4 + R_{10}) + R_4 R_{10}}{R_{10}} \tag{3}$$

$$R_C = \frac{(R_D + R_2)(R_3 + R_8) + R_3 R_8}{R_8} \tag{4}$$

$$R_D = \frac{(R_1 + R_6)R_7}{2R_1 + R_6 + R_7}. \tag{5}$$

Equation (1) shows that the optimum gain of the amplifier depends on the values of R_3 and R_4 which are determined by the position of the observation point inside the guard ring. This means that the value given by Eq.(1) only valid for fixed values of R_3 and R_4 which is a particular area inside the guard ring. Therefore, the noise reduction will be only obtained on a relatively narrow area inside the guard ring. This is the major drawback of the conventional circuits in [4], [7], [8].

An active shield circuit layouts which has a good noise suppression effect on the entire area inside the guard ring is proposed in [9]–[11]. The circuit layout is shown in Fig. 3. The gain of the amplifier required to make the transfer function from i_n to v_d becomes zero is given by

$$A = -\frac{(R_3 + R_A)R_B}{R_3 R_C} \tag{6}$$

where

$$R_A = \frac{R_2 R_8}{R_2 + R_8 + R_D} \tag{7}$$

$$R_B = \frac{(R_1 + R_6)(R_2 + R_7) + R_2 R_7}{R_7} \tag{8}$$

$$R_C = \frac{R_8 R_D}{R_2 + R_8 + R_D} \tag{9}$$

$$R_D = \frac{(R_1 + R_6)(R_2 + R_7) + R_2 R_7}{R_1 + R_6}. \tag{10}$$

Equation (6) shows that the optimum gain value is independent of the values of R_4 and R_5 which means the noise suppression effect is not affected by the position of the observation point inside the guard ring. In other words, a proper noise suppression performance can be obtained for the entire area inside the guard ring. The difference of the noise suppression performance of these conventional circuits is based on the way of how the noise is suppressed. The conventional circuit layouts in [4], [7] suppress the noise after it reached the analog circuits inside the guard ring. Therefore it only suppress the noise in a particular area inside the guard ring. On the other hand, the circuit layouts in [9]–[11] suppress the noise before it reaches the analog circuits inside the guard ring and therefore the noise suppression performance is obtained on the entire area inside the guard ring.

Unfortunately the conventional circuit in Fig. 3 has a shortcoming. Commonly the digital part in a mixed-signal integrated circuit usually has a much larger area than the analog part. In case of the layout in Fig. 3, the sense node should be placed between the guard ring and the digital part while the output node should be placed at the opposite edge of the digital part. It means that the cancellation signal should be transmitted across the digital part which in most cases would be a long transmission line and produce a significant delay. This will reduce the performance of the active shield circuit.

3. Proposed Circuit

3.1 Circuit Layout

Based on the study of the conventional circuit layouts, in order to obtain a proper noise suppression for the entire area inside the guard ring, the method which suppresses the noise before it reaches analog part is chosen. Furthermore, in order to reduce the delay of the transmission line, the output of the active shield circuit should be placed near its input. The proposed layout is shown in Fig. 4.

In this case, the optimum gain will be given by

$$A = -\frac{(R_2 + R_A)R_{11}}{R_2 R_B} \tag{11}$$

where

$$R_A = \frac{(R_1 + R_8)R_9}{2R_1 + R_8 + R_9} \tag{12}$$

$$R_B = \frac{(R_C + R_2)(R_3 + R_{10}) + R_3 R_{10}}{R_{10}} \tag{13}$$

$$R_C = \frac{R_1 R_9}{2R_1 + R_8 + R_9}. \tag{14}$$

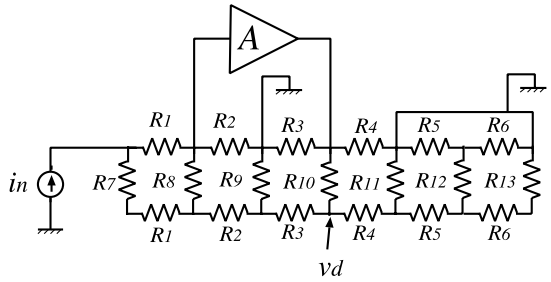

Fig. 4 Proposed circuit.

Table 1 Gain sensitivity to substrate resistances.

Name	Value[Ω]	S_R^A	Name	Value[Ω]	S_R^A
R_1	100	−0.095	R_8	50	0.175
R_2	50	0.924	R_9	50	0.36
R_3	50	−0.64	R_{10}	50	1
R_7	100	0.124			

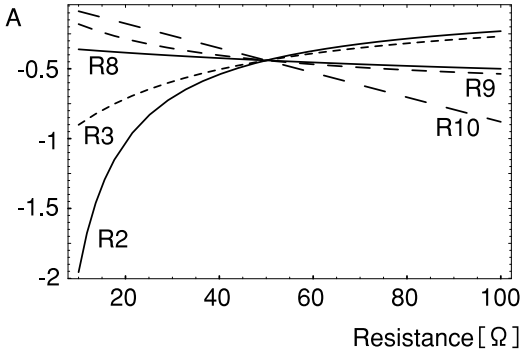

Fig. 5 Gain sensitivity to resistances.

Since the optimum gain is determined by the substrate resistances, it will be very useful to examine the sensitivity of the optimum gain value to the variation of substrate resistances which is given by

$$S_{R_i}^A = \frac{\partial A}{\partial R_i}\frac{R_i}{A}. \tag{15}$$

The sensitivities for typical resistances are shown in Table 1. It shows that the optimum gain value has a high sensitivity to the values of R_2, R_3, R_9, and R_{10}. However, since the resistances are fixed for a given layout, this can be ignored. The values of R_1 and R_7 will vary with various noise source positions and injection area. Fortunately, since the gain sensitivities to these resistances are low, the variation of noise source position and injection area will not have great effects on the active shield circuit performance. The optimum gain value for various resistances is shown in Fig. 5. Using the initial resistance in Table 1, for a given resistance range from 10 to 100 Ω, the optimum gain value never exceeds −1. On the other hand, it reaches −2 for $R_2 = 10\,\Omega$. Note that since the horizontal and the vertical resistances depend on the distance between two nodes and the size of the substrate contact respectively, a careful layout which also means carefully selecting the resistances will guarantee that the optimum gain value will always be smaller than −1. Therefore an attenuator will be required instead of an amplifier. This will gives an advantage for improving the active shield circuit's bandwidth.

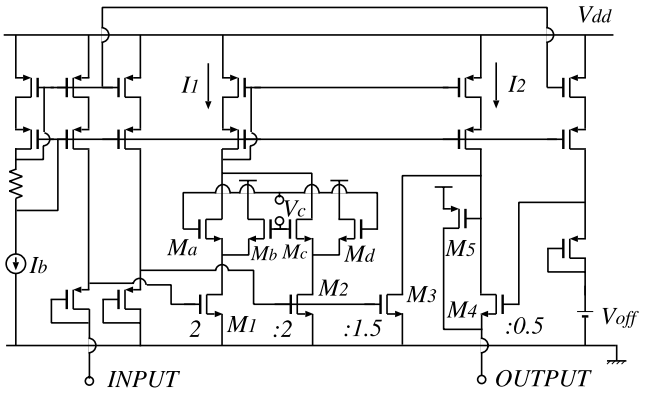

Fig. 6 Proposed circuit.

3.2 Circuit Implementation

An alternative implementation of the amplifier for an active shield circuit is shown in Fig. 6. This circuit is derived from the circuit proposed in [10]. Transistor M_1 works as a V-I converter which converts the input voltage to current. This current then will be inverted by the current mirror and converted to output voltage by M_4. Transistors M_a to M_d construct a current switch to control the gain of the amplifier while keeping the bias current constant. Assume that V_C and the input voltage are zero (the input node is grounded) and therefore the gate to source voltages of M_1 to M_3 are equal ($V_{GS1} = V_{GS2} = V_{GS3} = V_0$). Here their drain currents will be given by

$$I_{DS1} = I_{DS2} = 2K(V_0 - V_{TN})^2 \tag{16}$$

$$I_{DS3} = 1.5K(V_0 - V_{TN})^2. \tag{17}$$

Assuming an ideal current mirror,

$$I_1 = I_2 = \frac{1}{2}I_{DS1} + \frac{1}{2}I_{DS2} \tag{18}$$

$$= 2K(V_0 - V_{TN})^2, \tag{19}$$

therefore the drain current of M_4 is

$$I_{DS4} = I_2 - I_{DS3} \tag{20}$$

$$= 2K(V_0 - V_{TN})^2 - 1.5K(V_0 - V_{TN})^2 \tag{21}$$

$$= 0.5K(V_0 - V_{TN})^2. \tag{22}$$

The gate to source voltage of M_4 then will be given by

$$V_{GS4} = \sqrt{\frac{I_{DS4}}{0.5K}} + V_{TN} \tag{23}$$

$$= V_0. \tag{24}$$

Thus the bias voltage of the output node is

$$V_{OUT} = V_{off} + V_0 - V_{GS4} \tag{25}$$

$$= V_{off}. \quad (26)$$

A DC offset at the output node is needed to enable the proposed active shield circuit directly drives the substrate [7]. In order to produce this offset voltage, a constant bias current is injected into the substrate. Transistor M_5 will supply this bias current while forming a feedback loop to fix the drain voltage of M_4.

4. Simulation Results

4.1 Simulated Substrate Model

Resistive networks with 11 nodes are used to represent the area of the digital part and analog part inside the guard ring as is shown in Fig. 7. The noise source is injected at nodes $\mathbf{d}_1 \sim \mathbf{d}_{11}$ while the noise level inside the guard ring will be observed at nodes $\mathbf{a}_1 \sim \mathbf{a}_{11}$. The unlabeled horizontal resistance and vertical resistance are 50 Ω and 100 Ω respectively. Other resistances are shown in Table 2.

4.2 Proposed Circuit Characteristic

The proposed circuit is simulated using HSpice circuit simulator with 0.35 μm CMOS process parameters. The supply voltage is 3 V and the output offset voltage V_{off} is set to 50 mV. Figure 8 shows the gain characteristic of the proposed circuit versus the control voltage V_C. Here the gain varies from −46 dB to 9 dB when V_C is changed from −0.5 V to 0.5 V.

4.3 Active Shield Circuit

Figure 9 shows the frequency characteristic of the conventional guard ring and the proposed active shield circuit. A current noise source is injected into node $\mathbf{d}_6$ and the noise level inside the guard ring is observed at node $\mathbf{a}_6$. Since the guard ring is connected to the ideal ground, the frequency characteristic is flat. The conventional guard ring suppresses the noise level to −52 dB. The proposed active shield circuit gives the minimum noise level of −85 dB for $V_C = -0.31$ V. Assuming 10 mV fluctuation in V_C shows that the proposed active shield circuit still gives a noise level 18 dB lower than the conventional guard ring.

Figure 10 shows the noise level at each node inside the guard ring. It shows that the conventional circuit [7] reduces the noise only for a relatively narrow area. On the other hand, the conventional circuit [9] and the proposed circuit effectively reduce the noise level on the entire area inside the guard ring. It seems that the conventional circuit [9] might have a better performance than the proposed circuit. However, with the given substrate model the conventional circuit [9] needs an amplifier with a gain of 72 dB. Since

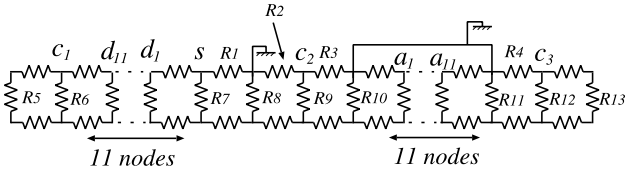

Fig. 7 Simulated substrate model.

Table 2 Resistances for substrate model.

Name	Ω	Name	Ω	Name	Ω
R_1	50	R_6	50	R_{10}	50
R_2	50	R_7	80	R_{11}	30
R_3	50	R_8	50	R_{12}	50
R_4	50	R_9	50	R_{13}	80
R_5	50				

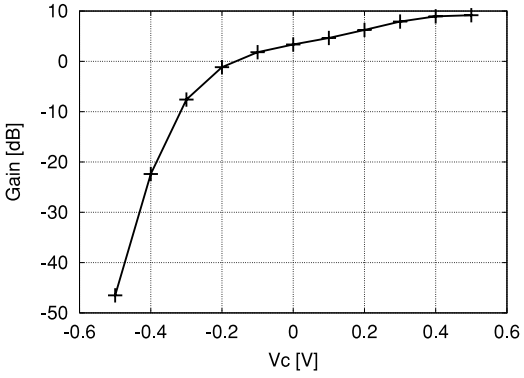

Fig. 8 Gain versus control voltage.

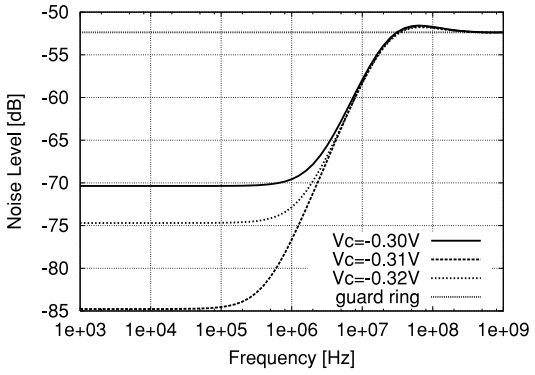

Fig. 9 Frequency characteristic of the proposed active shield circuit.

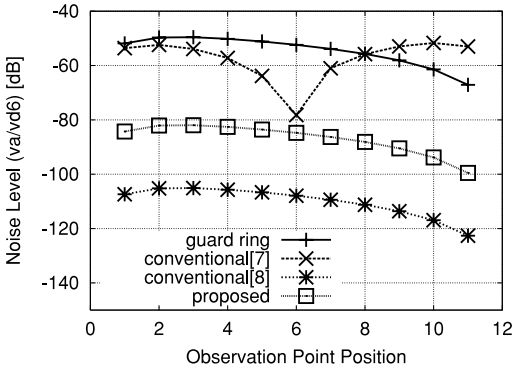

Fig. 10 Noise level observed at each node inside the guard ring.

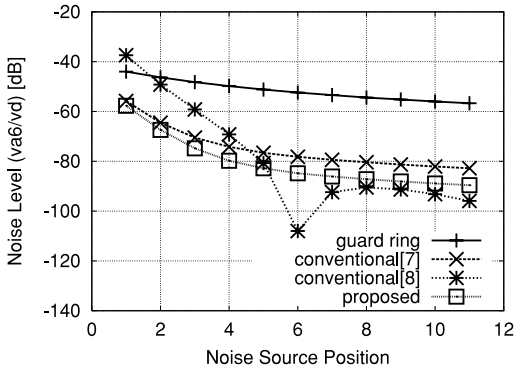

Fig. 11 Noise level observed at node $\mathbf{a}_6$ with various noise source position (optimized for noise injected at node $\mathbf{d}_6$).

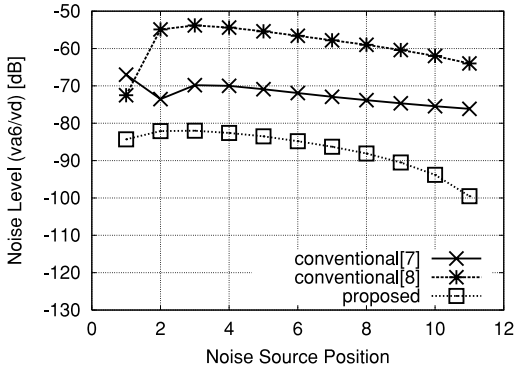

Fig. 12 Noise level observed at node $\mathbf{a}_6$ with various noise source position (optimized for noise injected at node $\mathbf{d}_1$).

the implementation is impractical, it is simulated using ideal components. Practically, noise source positions in a mixed-signal integrated circuit are arbitrary and it is necessary to inspect the performance of the proposed active shield circuit considering this property of noise source position. The simulation result is shown in Fig. 11. It shows that the noise levels inside the guard ring when using the passive guard ring, conventional circuit [7] and the proposed circuit decrease with the increase of the distance from the noise source to the guard ring. The conventional circuit [9] gives the lowest noise level for the optimized noise source position but noise from different position is not properly reduced. The difference between the lowest and the highest noise level for the conventional circuit [9] is about 70 dB while the proposed circuit only has a difference of about 30 dB.

Since the noise level inside the guard ring is reduced proportionally with the increase in the noise source distance to the guard ring, it will be more effective to optimize the gain of the active shield circuit with a noise source injected at node $\mathbf{d}_1$. Figure 12 shows the simulation result of the noise level inside the guard ring for various noise source positions when the gain of the active shield circuit is optimized for a noise source at node $\mathbf{d}_1$. Similar to the characteristic in Fig. 11, the conventional circuit [9] has lowest noise level for the noise in the optimized position ($\mathbf{d}_1$). Although reduced, the difference between the noise level for the optimized noise source position and the worst noise level is 20 dB. On the other hand, the difference between the noise level for the optimized noise source position and the worst noise level of the proposed circuit is only 3 dB. As a conclusion, in order to obtain the optimum noise suppression performance for arbitrary noise source positions, the gain of the active shield circuit should be optimized to suppress the noise from the nearest source to guard ring.

In the previous simulations, it is assumed that there is only one noise source while there are actually multiple noise sources. Fortunately, since superposition principle is adaptable, multiple noise sources can be represented as a single equivalent noise source. Therefore the above simulation results is also well applied with multiple noise sources.

5. Conclusions

A new layout of an active shield circuit is proposed. The proposed layout is able to suppress the noise inside the entire area of the guard ring regardless of the position of noise sources. Simulation results show that the proposed circuit gives a noise level of −85 dB while the guard ring suppresses the noise to −52 dB. The deterioration of the noise suppression performance due to the fluctuation in the gain control voltage of the amplifier can be reduced by reducing the voltage-to-gain conversion parameter value.

The layout of the proposed active shield circuit should be chosen carefully in order to keep the optimum gain of the amplifier as low as possible and thus gives possibility for speed improvement.

Acknowledgments

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