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LETTER *Special Issue on Devices and Circuits for Next Generation Multi-Media Communication Systems*

Wide Tuning Range Voltage-Controlled Ring Oscillator

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SUMMARY A voltage-controlled ring oscillator with an RC delay as an additional delay to vary the oscillation frequency is proposed. The use of MOS resistors provides a wide range tuning ability from 40 Hz to 366 MHz. The proposed circuit also enables implementation of a low frequency voltage-controlled ring oscillator with relatively smaller devices than the conventional one.

key words: *ring oscillator, voltage-controlled oscillator, RC delay*

1. Introduction

Voltage-controlled oscillators (VCOs) have been known to play an important role on communications and signal processing [1]–[7]. One of the well known VCOs is based on a ring oscillator (current starved ring oscillator) [2].

A current starved ring oscillator varies its bias current to control the oscillation frequency. However, extremely decreasing or increasing bias current will not give effective tuning range improvement. Another implementation such as a current mode logic ring oscillator [3] is also introduced, but still the tuning range is limited.

This letter proposes a simple design of a ring oscillator which uses additional delay to obtain a wider tuning range. Section 2 will describe the conventional current starved ring oscillator. The proposed ring oscillator will be introduced in Sect. 3, followed by simulation and measurement results in Sect. 4. At last, the conclusions will be given in Sect. 5.

2. Current Starved VCO

A conventional current starved ring oscillator circuit is shown in Fig. 1. Here N is the number of the stages and has to be an odd number. Assuming that the control current I_{ctrl} is constant and well matched to each other,

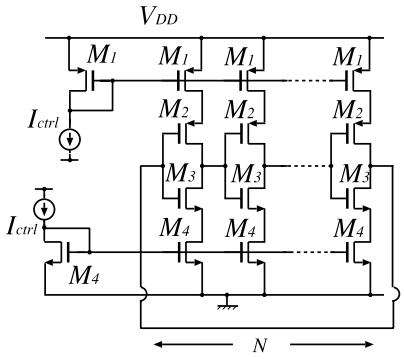

Fig. 1 Current starved ring oscillator.

the oscillation frequency for an N-stage ring oscillator f_{osc} will be approximately

$$f_{osc} = \frac{I_{ctrl}}{2NC_GV_{osc}}, \tag{1}$$

where C_G is the parasitic capacitance at the input of each stage and V_{osc} is the oscillation amplitude which is typically the supply voltage.

Since C_G and V_{osc} are assumed to be constant, the oscillation frequency changes with the change in control current. Thus, decreasing or increasing control current will decrease or increase the oscillation frequency. Theoretically, the tuning range will be reasonably wide enough. Unfortunately that is not true at all. When the control current is decreased to a very small value, it is practically difficult to keep the matching between current sources at the upper part and lower part, which will make the rise time of the pulse wave different from its fall time. If the lower current limit is fixed to allow reasonable matching between current sources, then the conventional circuit will need additional load capacitance for lower oscillation frequencies. On the other hand, increasing the control current will reduce the voltage headroom of the MOS current source which will result in the saturation of the f-v characteristic at high frequencies.

3. Proposed Circuit

First, recall that the delay of a simple RC ladder will be given as

$$\tau = RC, \tag{2}$$

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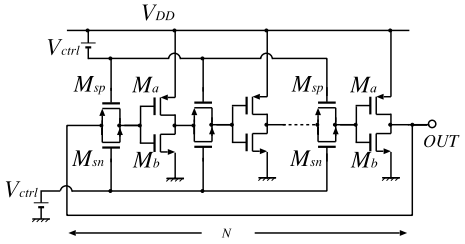

Fig. 2 Proposed ring oscillator.

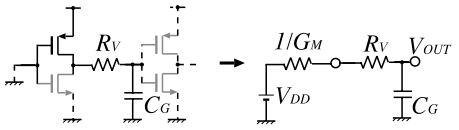

Fig. 3 Proposed ring oscillator.

which means varying the value of resistance and/or capacitance will vary the delay. The proposed circuit shown in Fig. 2 applies this characteristic to control its oscillation frequency. A voltage-controlled resistor implemented by CMOS resistors is added at the input of each inverter stage. Using Fig. 3, the oscillation frequency of the proposed circuit is approximately

$$f_{osc} = \frac{G_M}{2NC_G(1 + G_M R_V)}, \tag{3}$$

where R_V is the resistance of CMOS resistors and G_M is the transconductance of the inverter. For a relatively small R_V, the oscillation frequency of the proposed circuit will be approximately the same to the oscillation frequency of a simple ring oscillator or

$$f_{osc} \approx \frac{G_M}{2NC_G}. \tag{4}$$

When R_V reaches a considerably large value, the oscillation frequency will be approximately

$$f_{osc} = \frac{1}{2NR_V C_G}, \tag{5}$$

which is simply determined by the RC delay. Since the resistance of MOS resistors could achieve a quite large value, the proposed circuit does not need any additional capacitances to obtain low oscillation frequencies.

4. Simulation and Measurement Results

The simulations on 3-stage ring oscillator of the conventional current starved and proposed ring oscillators are done using HSpice with level 28, 0.6 μm CMOS process parameters. The sizes of MOS transistors are shown in Table 1. The supply voltages are 3 V for both circuits.

Figures 4 and 5 show the transient characteristics of the conventional and proposed circuits with different oscillation frequencies. Here the proposed circuit has a faster voltage transition than the conventional circuit

Table 1 Transistors' W/L ratio.

MOS	W/L(μm/μm)
M_1,M_{sp}	3/0.6
M_2,M_a	9/0.6
M_3,M_b	4.5/1.2
M_4,M_{sn}	1.5/1.2

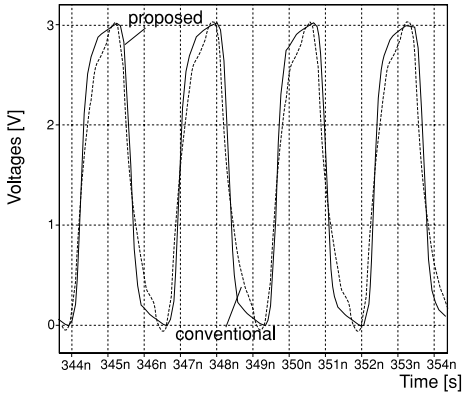

Fig. 4 Transient characteristic (f_{osc}=370 MHz).

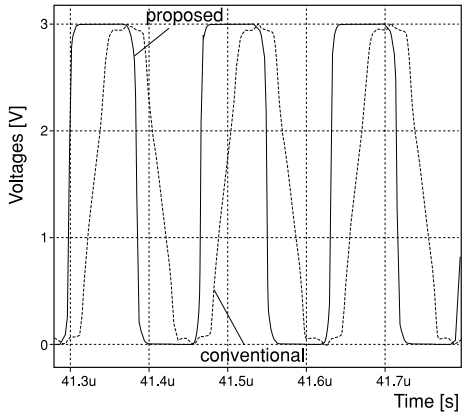

Fig. 5 Transient characteristic (f_{osc}=6 MHz).

for low oscillation frequencies. In case of $f_{osc} = 6$ MHz, the rise/fall time (10–90% of voltage swing) for the conventional and the proposed circuits are 32.1 ns and 4.3 ns respectively. Here the rise/fall time of the proposed circuit is roughly 1/8 of the conventional circuit.

Simulation result of the f-v characteristic of the conventional and the proposed voltage-controlled ring oscillators are shown in Fig. 6. The control voltage V_{ctrl} of the conventional circuit is the gate to source voltage of the NMOS transistor's current source M_4. The conventional circuit cannot oscillate for control voltage less than 0.6 V. Therefore the proposed circuit has a wider tuning range. It also shows that a low frequency oscillator using small size devices can be implemented by the proposed circuit.

Figure 7 shows the average power dissipations P_{avg} of the conventional and the proposed circuits which is given by

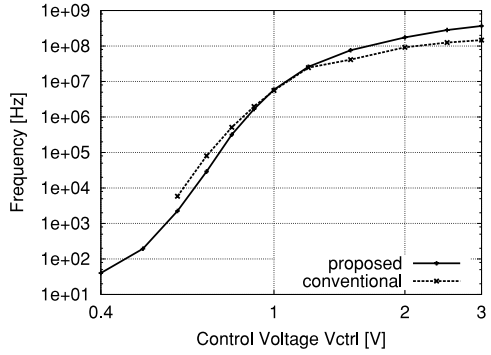

Fig. 6 F-V characteristics.

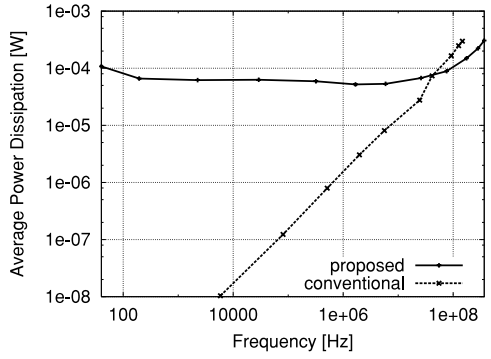

Fig. 7 Power dissipation.

$$P_{avg} = \frac{\int_0^T I(t) \times V_{DD} dt}{T}, \tag{6}$$

where,

$I(t)$: the time function of total current dissipation

T: the period of oscillation.

Here the average power consumption of the conventional circuit is decreased in proportion to the oscillation frequency. However, the average power consumption of the proposed circuit does not change much with the variation in its oscillation frequencies. Figure 5 shows that the proposed circuit has a fast time transition even if its oscillation frequency is decreased. This means that the proposed circuit drives a large current during the transition. In the other words, the proposed circuit dissipates more currents to maintain the transition time short. As a result, the average power dissipation of the proposed circuit is not decreased for low oscillation frequencies.

The proposed circuit is fabricated on $0.6\,\mu$m CMOS process without any additional output buffer. Figures 8 and 9 show the measurement results of the proposed ring oscillator for f_{osc}=415 [kHz] and f_{osc}=7 [MHz] respectively. Since the proposed circuit was made without output buffer to drive large capacitance load, the capacitance of the measurement probe limits the measurable frequency. Higher frequency is observed in measurements although the oscillation amplitude is decreased.

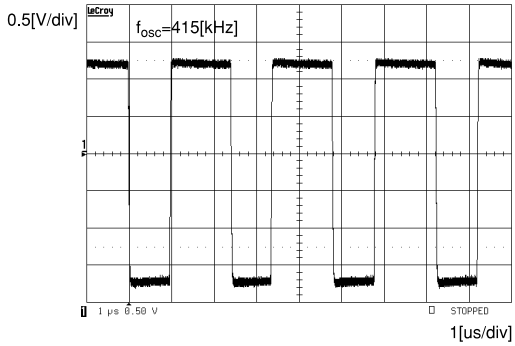

Fig. 8 Measurement result of low oscillation frequency.

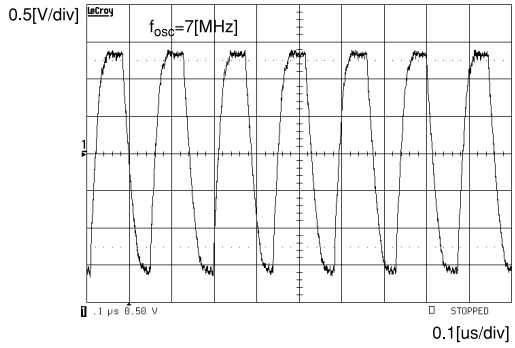

Fig. 9 Measurement result of high oscillation frequency.

5. Conclusions

A voltage-controlled ring oscillator with an additional RC delay is proposed. Simulation results show that a VCO with wide tuning range can be implemented using the proposed design. The proposed VCO achieves a tuning range from 40 Hz to 366 MHz for control voltage between 0.4 V to 3 V. The upper frequency limit is depend on the size of the CMOS inverter. The proposed VCO also has a faster voltage transient than the conventional one for low oscillation frequencies. The proposed VCO can produce low oscillation frequencies without any additional capacitances and thus enables implementation of a low frequency VCO with relatively small devices.

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