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# Control of Flat Band Voltage by Partial Incorporation of La<sub>2</sub>O<sub>3</sub> or Sc<sub>2</sub>O<sub>3</sub> into HfO<sub>2</sub> in Metal/HfO<sub>2</sub>/SiO<sub>2</sub>/Si MOS Capacitors

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## Abstract

High-k/SiO<sub>2</sub> interfacial properties are most critical factors determining the high-k gate MOSFET characteristics. We fabricated MOS capacitors of metal/HfO<sub>2</sub>/SiO<sub>2</sub>/Si structures in which were contained in the HfO<sub>2</sub> layer. Flat-band voltage ( $V_{FB}$ ) shifts were measured by changing composition in metal/HfO<sub>2</sub>/(HfO<sub>2</sub>)<sub>1-x</sub>(La<sub>2</sub>O<sub>3</sub>)<sub>x</sub>/SiO<sub>2</sub>/Si and metal/HfO<sub>2</sub>/(HfO<sub>2</sub>)<sub>1-x</sub>(Sc<sub>2</sub>O<sub>3</sub>)<sub>x</sub>/SiO<sub>2</sub>/Si structures. It was found that  $V_{FB}$  shift arises mainly from high-k/SiO<sub>2</sub> interface rather than metal/high-k interface.  $V_{FB}$  could be effectively controlled by incorporating La<sub>2</sub>O<sub>3</sub> or Sc<sub>2</sub>O<sub>3</sub> near the high-k/SiO<sub>2</sub> interface.

## Introduction

Combination of metal and high-k dielectrics is necessary in order to achieve smaller EOT for eliminating the poly-Si gate depletion effect without excess leakage current. HfO<sub>2</sub> based materials have been the promising candidates for next generation gate dielectric thanks to its high temperature endurance and relatively high permittivity. One of the issues of HfO<sub>2</sub> based oxides is the difficulty in reducing the threshold voltage ( $V_{th}$ ) as relatively high  $V_{th}$  were obtained with HfO<sub>2</sub> based oxides whatever the electrode material is. On the other hand, it has been reported that La<sub>2</sub>O<sub>3</sub> and Sc<sub>2</sub>O<sub>3</sub> produce negative shift in  $V_{FB}$  with respect to HfO<sub>2</sub> reference<sup>[1]</sup>. However, the detailed mechanism is not clarified yet. In this paper, first we extract the effective work function ( $EFW$ ) of tungsten gate metal on high-k dielectrics, and then investigated the effect of La<sub>2</sub>O<sub>3</sub> or Sc<sub>2</sub>O<sub>3</sub> incorporation into a HfO<sub>2</sub> layer in a metal/HfO<sub>2</sub>/SiO<sub>2</sub>/Si MOS capacitor.

## Experimental

Si(100) substrates with 200 nm-thick field SiO<sub>2</sub> in which diode holes were opened (1-10 ohm-cm) were cleaned in a mixed solution of H<sub>2</sub>SO<sub>4</sub> and H<sub>2</sub>O<sub>2</sub>, followed by dipping in diluted HF. The substrates were then thermally oxidized to grow 3.5-nm-thick SiO<sub>2</sub> film. High-k dielectrics were deposited on these substrates by e-beam evaporation with O<sub>2</sub> partial pressure of 1x10<sup>-4</sup> Pa. Tungsten (W) gate electrode was *in-situ* deposited by RF sputtering. The W film was lithographically patterned and etched by reactive ion etching (RIE) using SF<sub>6</sub> chemistry to form gate electrodes for MOS capacitors. Annealing in forming gas (3 %-H<sub>2</sub>+97 %-N<sub>2</sub>) was performed at 420 °C for 30 min. Finally, aluminum (Al) was thermally evaporated on backside of the wafers for bottom electrode. Capacitance-voltage ( $C-V$ ) characteristics of the fabricated MOS capacitors were measured at 100 kHz using Agilent 4284A precision LCR meter, from which  $V_{FB}$  and EOT were calculated using NCSU CVC program.

The dielectrics studied here are  $\text{La}_2\text{O}_3$ ,  $\text{HfO}_2$  and  $\text{Sc}_2\text{O}_3$ . To evaluate the main reason of  $V_{FB}$  shift, laminated dielectric stacks of  $\text{HfO}_2/\text{La}_2\text{O}_3$  were fabricated. Moreover, mixed dielectrics of  $\text{HfO}_2\text{-La}_2\text{O}_3$  and  $\text{HfO}_2\text{-Sc}_2\text{O}_3$  with  $\text{HfO}_2$  atop were also fabricated by co-evaporation of the two oxides.

## Results and Discussions

### Effective Work Function (EWF) Extraction

A schematic model of the charge locations in a metal/ $\text{SiO}_2$ /Si structure and metal/high-k/ $\text{SiO}_2$ /Si structure are illustrated in Fig.1. As the thickness of the dielectric layer is small, the bulk charges of each oxide can be neglected. Indeed, the results shown in Fig. 2 revealed a linear relationship between  $V_{FB}$  and the EOT, thus, it is reasonable to assume low charge concentration inside the  $\text{SiO}_2$  and the high-k layer. Under the assumption, the effective work function (EWF) of metal on a  $\text{SiO}_2$  can be derived from the relation of  $V_{FB}$  and EOT using the following equation,

$$V_{FB} = -\left(\frac{Q_{\text{SiO}_2/\text{Si}}}{\epsilon_0 \epsilon_{ox}}\right) \cdot EOT + \frac{\phi_{ms}}{q} + q\Delta_{\text{SiO}_2/\text{Metal}}, \quad (1)$$

where  $Q_{\text{SiO}_2/\text{Si}}$  is the fixed charge at the  $\text{SiO}_2$ /Si interface,  $\phi_{ms}$  is the work function difference of gate metal and semiconductor and  $\Delta_{\text{SiO}_2/\text{Metal}}$  is the dipole at metal/oxide interface. The EWF of gate metal, defined as  $\frac{\phi_{ms}}{q} + q\Delta_{\text{SiO}_2/\text{Metal}}$ , can be extracted by the y-intercept from the  $V_{FB}$ -EOT slope. When interfacial  $\text{SiO}_2$  layer (IL) is inserted between high-k dielectric and Si substrate, the Eq.(1) can be modified using total EOT as shown in eq.(2),

$$V_{FB} = -\left(\frac{Q_{\text{high-k/IL}} + Q_{\text{SiO}_2/\text{Si}}}{\epsilon_0 \epsilon_{ox}}\right) \cdot EOT + \frac{Q_{\text{SiO}_2/\text{high-k}}}{\epsilon_0 \epsilon_{ox}} \cdot EOT_{\text{IL}} + \frac{\phi_{ms}}{q} + q\Delta_{\text{Metal/high-k}}. \quad (2)$$

Here,  $Q_{\text{high-k/IL}}$ ,  $\Delta_{\text{high-k/Metal}}$  and  $EOT_{\text{IL}}$  are the fixed charge at high-k/IL interface, the dipole at high-k/metal interface and the EOT of IL, respectively. Eventually, the EWF of metal on high-k/ $\text{SiO}_2$  stack can be expressed as follows,

$$EWF_{(\text{high-k})} = EWF_{(\text{SiO}_2)} + (q\Delta_{\text{high-k/Metal}} - q\Delta_{\text{SiO}_2/\text{Metal}}). \quad (3)$$

Figure 2 shows the typical  $C$ - $V$  curves of  $\text{La}_2\text{O}_3/\text{IL}$ ,  $\text{HfO}_2/\text{IL}$  and  $\text{Sc}_2\text{O}_3/\text{IL}$  capacitors. The difference between  $V_{FB}(\text{HfO}_2/\text{IL})$  and  $V_{FB}(\text{La}_2\text{O}_3/\text{IL})$  is about 0.48 V, whereas difference between  $V_{FB}(\text{HfO}_2/\text{SiO}_2)$  and  $V_{FB}(\text{Sc}_2\text{O}_3/\text{SiO}_2)$  is 0.15 V. Figure 3 shows the result of  $V_{FB}$  of  $\text{La}_2\text{O}_3/\text{IL}$ ,  $\text{HfO}_2/\text{IL}$  and  $\text{Sc}_2\text{O}_3/\text{IL}$  capacitors with different high-k thicknesses. Capacitors with  $\text{SiO}_2$  with different thickness are also shown to derive  $Q_{\text{SiO}_2/\text{Si}}$ . Using the equations (1)-(3), EWF of W on  $\text{SiO}_2$ ,  $\text{HfO}_2$ ,  $\text{La}_2\text{O}_3$  and  $\text{Sc}_2\text{O}_3$  can be calculated and summarized in Table.1. The smallest EWF of 4.46 eV was obtained with  $\text{La}_2\text{O}_3$ , whereas relatively large value was obtained with  $\text{HfO}_2$ . These results suggest high

$V_{th}$  in nMOSFET when  $HfO_2$  is used as gate dielectrics. In the next subsection, the origin of  $V_{FB}$  is examined in detail.

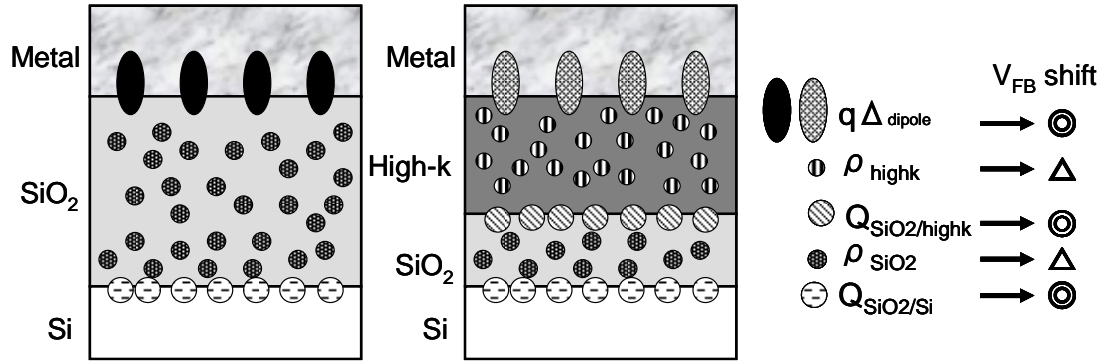


Fig.1 Schematic model of the charge locations used in the extraction of fixed charge.

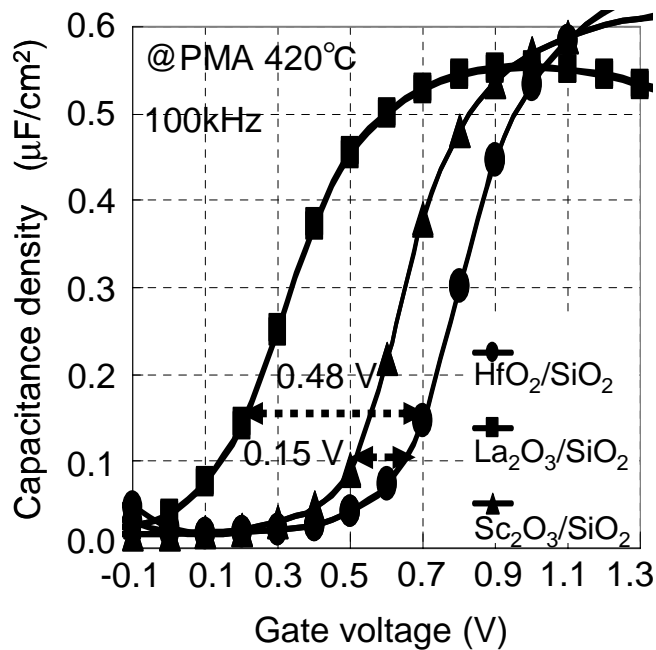


Fig.2 C-V characteristics of MOS capacitors with single layered high-k dielectric ( $HfO_2$ ,  $La_2O_3$ ,  $Sc_2O_3$ )

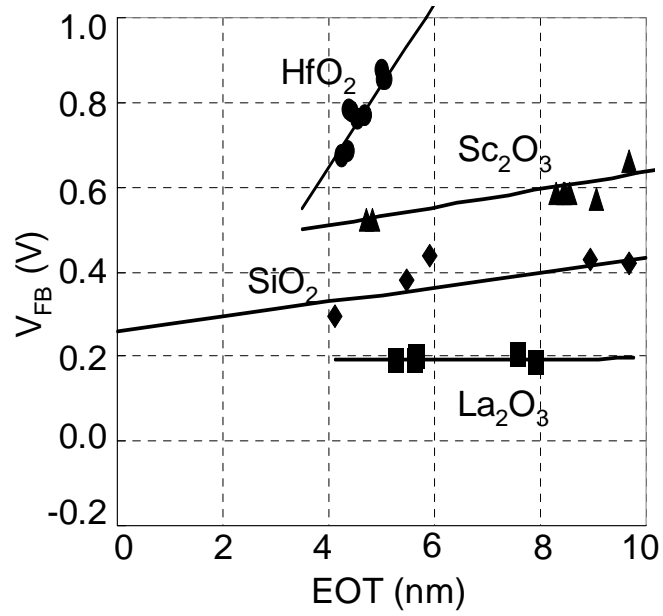


Fig.3  $V_{FB}$ -EOT plot obtained from the analysis of C-V curves.

Table 1. Effective work function of W gate electrode on various gate dielectric (SiO<sub>2</sub>, La<sub>2</sub>O<sub>3</sub>, HfO<sub>2</sub>, La<sub>2</sub>O<sub>3</sub>)

Gate Oxide	SiO <sub>2</sub>	La <sub>2</sub> O <sub>3</sub>	HfO <sub>2</sub>	Sc <sub>2</sub> O <sub>3</sub>
EFW (eV)	4.59	4.46	4.80	4.75

### C-V Characteristics of HfO<sub>2</sub>/La<sub>2</sub>O<sub>3</sub> Stack Structure

In order to investigate the  $V_{FB}$  shift on stacked dielectrics, double layer stacked films were fabricated, as shown in Fig. 4. Capacitors with single layer of HfO<sub>2</sub> or La<sub>2</sub>O<sub>3</sub> are also fabricated as references. The total thickness of the high-k film was designed to have 5 nm. Figure 5 shows the C-V characteristics of W/HfO<sub>2</sub>/La<sub>2</sub>O<sub>3</sub>/IL stacked MOS capacitors. The C-V curves of the stacked capacitors showed negative  $V_{FB}$ , which are close to that of the single La<sub>2</sub>O<sub>3</sub> layer reference. From these results, it is clear that the  $V_{FB}$  shift is determined by the high-k material in contact to SiO<sub>2</sub> IL. It is known that positive charges or dipole at the interface could attribute to negative shift in  $V_{FB}$ , however, either or both effects on these results are not clarified yet. Nonetheless, it is expected that by changing the composition of high-k at the high-k/IL interface might allow precise  $V_{FB}$  control.

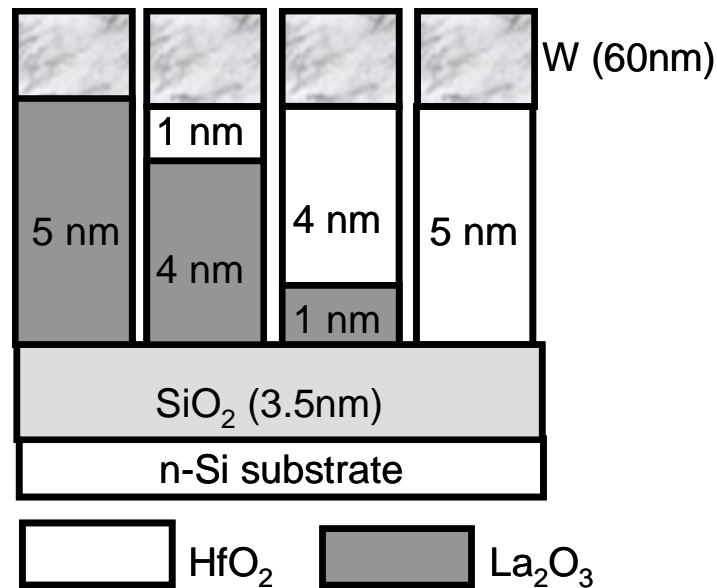


Fig.4 Schematic illustration of fabricated MOS capacitors with stack of HfO<sub>2</sub> and La<sub>2</sub>O<sub>3</sub>. Capacitors with single HfO<sub>2</sub> or La<sub>2</sub>O<sub>3</sub> layer are fabricated as references.

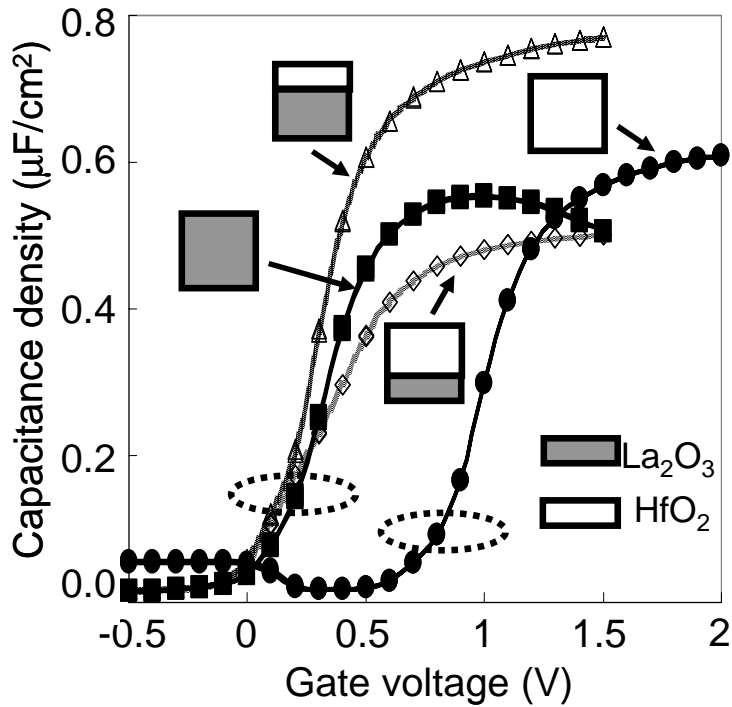


Fig.5 C-V curves for W/HfO<sub>2</sub>/La<sub>2</sub>O<sub>3</sub>/SiO<sub>2</sub> stacked MOS capacitors.

#### $V_{FB}$ Shift Dependence on La<sub>2</sub>O<sub>3</sub> Incorporation at High-k/SiO<sub>2</sub> Interface

In this subsection, the  $V_{FB}$  shift depending on the amount of La<sub>2</sub>O<sub>3</sub> at the high-k/SiO<sub>2</sub> interface is investigated. From the result that even 1 nm of La<sub>2</sub>O<sub>3</sub> at high-k/SiO<sub>2</sub> interface can negatively shift the  $V_{FB}$ , the amount of the incorporated La<sub>2</sub>O<sub>3</sub> to realize controllability of  $V_{FB}$  should be less than 1 nm. To obtain precise controllability of amount of La<sub>2</sub>O<sub>3</sub> during the deposition process, we employed co-evaporation of HfO<sub>2</sub> and La<sub>2</sub>O<sub>3</sub> with different concentration, those are 20, 50 and 80 %. The thickness of the mixed high-k layers was set to 1 nm. HfO<sub>2</sub> with 5 nm thickness was capped on the mixed high-k. The schematic illustrations of the fabricated capacitors are shown in Fig. 6. The C-V characteristics of the mixed high-k stack capacitors together with those of the references with La<sub>2</sub>O<sub>3</sub> and HfO<sub>2</sub> capacitors are shown in Fig. 7. With the La<sub>2</sub>O<sub>3</sub> concentration of 80%, the  $V_{FB}$  of C-V curves showed almost identical value for the La<sub>2</sub>O<sub>3</sub> reference, where that of 20 % showed in between of those of HfO<sub>2</sub> and La<sub>2</sub>O<sub>3</sub> references. With 50 % of La<sub>2</sub>O<sub>3</sub> incorporation, the  $V_{FB}$  was slightly positive to the La<sub>2</sub>O<sub>3</sub> reference. Also from these results, it is noted that the  $EWf$  of the gate metal is mainly dominated by the high-k/IL interface, not at the Metal/high-k interface. By plotting the  $V_{FB}$  on La<sub>2</sub>O<sub>3</sub> concentration, as is shown in Fig. 8, we obtain a monotonic relation between concentration and  $V_{FB}$ . It can be concluded that  $V_{FB}$  can be effectively controlled by changing the concentration of the mixed high-k at the high-k/IL interface.

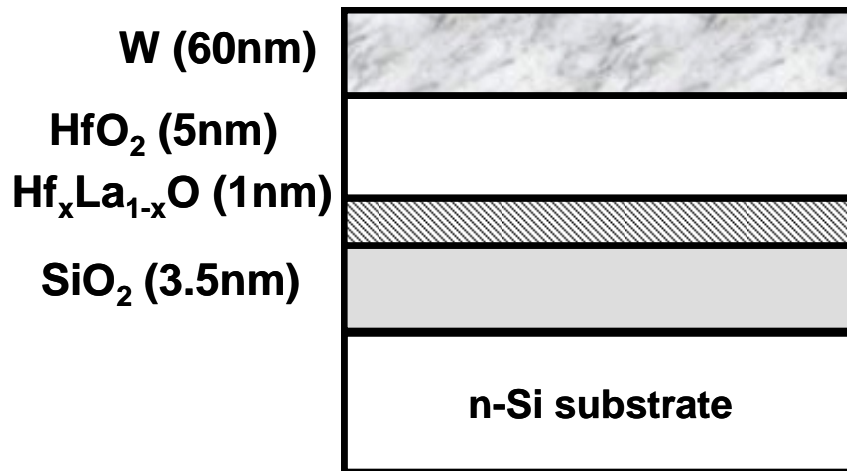


Fig.6 Schematic illustration of fabricated MOS capacitor incorporating La<sub>2</sub>O<sub>3</sub> into HfO<sub>2</sub>/SiO<sub>2</sub> interface

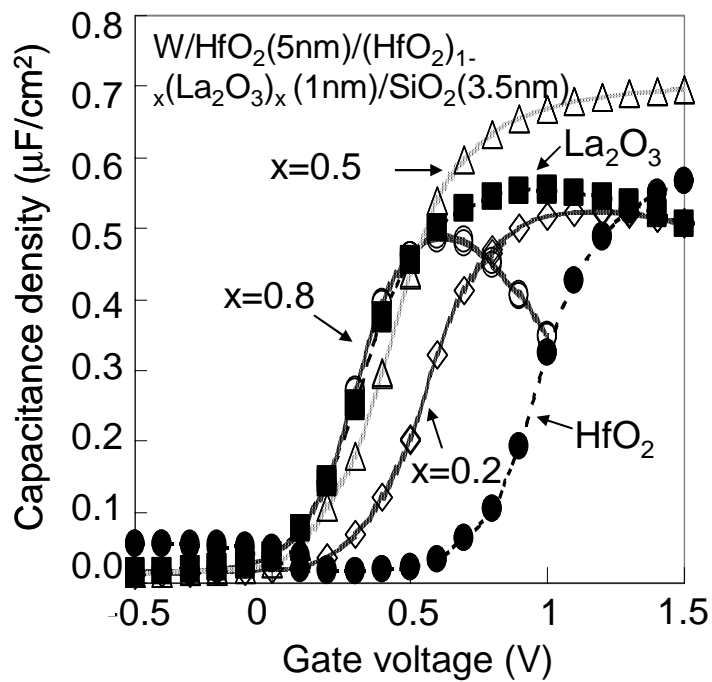


Fig.7 C-V curves of W/HfO<sub>2</sub>/(HfO<sub>2</sub>)<sub>1-x</sub>(La<sub>2</sub>O<sub>3</sub>)<sub>x</sub>/SiO<sub>2</sub> structure

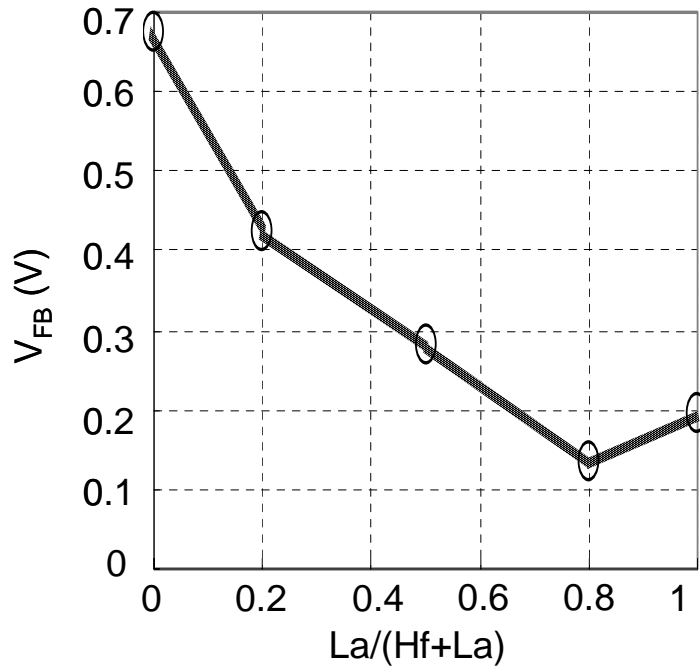


Fig.8  $V_{FB}$  shift depending on concentration of incorporation La at  $\text{HfO}_2/\text{SiO}_2$

#### $V_{FB}$ Controlled by $\text{Sc}_2\text{O}_3$ Incorporation into $\text{HfO}_2$

The same experiments were carried out using  $\text{Sc}_2\text{O}_3$  and  $\text{HfO}_2$ . In this case, the thickness of  $\text{Sc}_2\text{O}_3$ - $\text{HfO}_2$  mixed high-k and  $\text{HfO}_2$  capping layer were set to 5 nm and 0.5 nm, respectively. The structure is depicted in Fig. 9. The concentrations of  $\text{Sc}_2\text{O}_3$  were set to 33, 50 and 67%. Figure 10 shows the  $C$ - $V$  curves of the  $\text{Sc}_2\text{O}_3$  incorporated  $\text{HfO}_2$  capacitors. Also  $\text{Sc}_2\text{O}_3$  and  $\text{HfO}_2$  references are shown. Negative shifts of  $V_{FB}$  with increase in the concentration of  $\text{Sc}_2\text{O}_3$  were obtained. The relation between the concentration and  $V_{FB}$  is shown in Fig. 11. From this figure, the  $V_{FB}$  control range of 0.15 V was achieved using  $\text{Sc}_2\text{O}_3$  incorporation into  $\text{HfO}_2$ . This value is smaller than that of  $\text{La}_2\text{O}_3$ , which can be expected from  $\text{Sc}_2\text{O}_3$  single layer capacitor. Therefore,  $\text{Sc}_2\text{O}_3$  and  $\text{La}_2\text{O}_3$  incorporation technique is useful as fine and coarse tuning of  $V_{FB}$ , respectively.

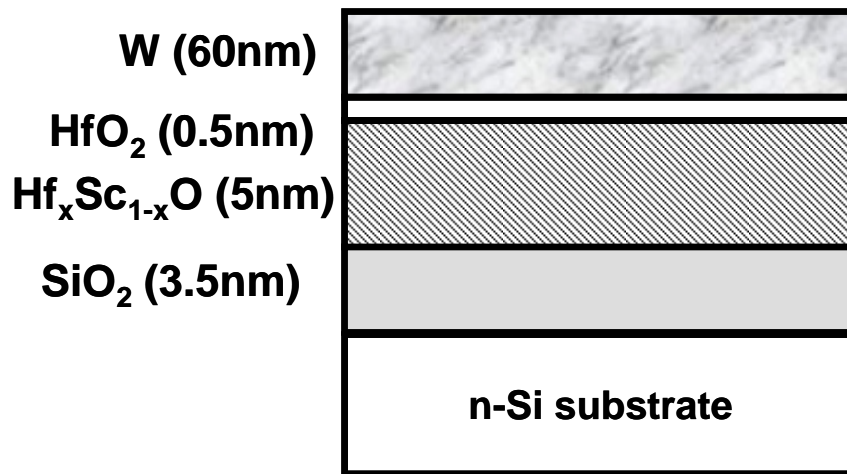


Fig.9 Schematic illustration of fabricated MOS capacitors incorporating Sc<sub>2</sub>O<sub>3</sub> into HfO<sub>2</sub>/SiO<sub>2</sub> interface

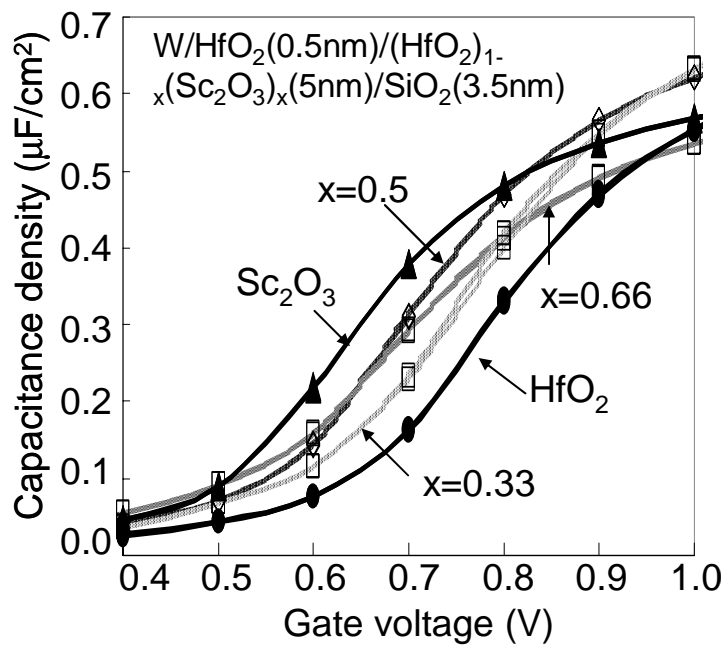


Fig.10 C-V curves of W/HfO<sub>2</sub>/(HfO<sub>2</sub>)<sub>1-x</sub>(Sc<sub>2</sub>O<sub>3</sub>)<sub>x</sub>/SiO<sub>2</sub> structures.

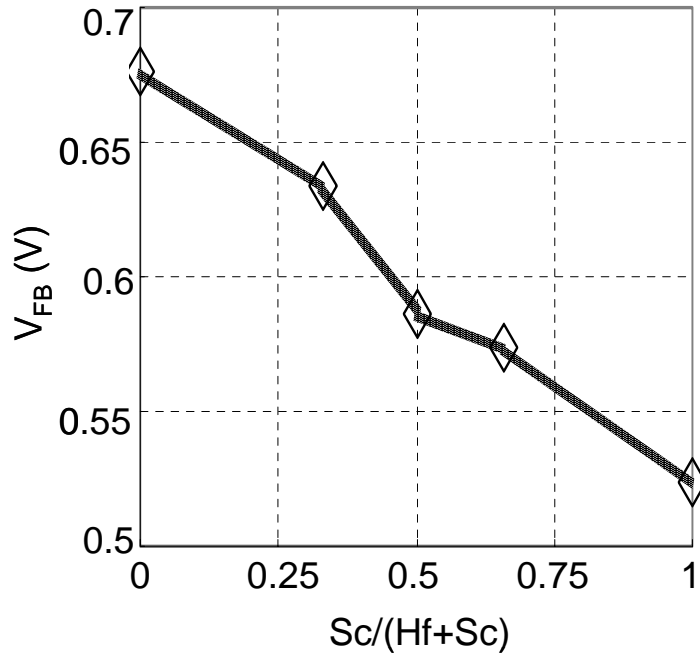


Fig.11  $V_{FB}$  shift depending on incorporation of Sc at  $\text{HfO}_2/\text{SiO}_2$  interface

### Conclusions

The  $V_{FB}$  shift was found to be dominated by the high-k/ $\text{SiO}_2$  interface property. The most considerable causation is an existence of the dipole at the high-k/ $\text{SiO}_2$  interface. We observed the  $V_{FB}$  shift for the MOS capacitors using  $(\text{HfO}_2)_{1-x}(\text{La}_2\text{O}_3)_x/\text{SiO}_2$  or  $(\text{HfO}_2)_{1-x}(\text{Sc}_2\text{O}_3)_x/\text{SiO}_2$  as gate dielectrics. The  $V_{FB}$  is dependent on concentration of  $\text{La}_2\text{O}_3$  or  $\text{Sc}_2\text{O}_3$ , and the large concentration results in large negative  $V_{FB}$  shift up to the  $V_{FB}$  obtained for the capacitors using  $\text{La}_2\text{O}_3/\text{SiO}_2$  or  $\text{Sc}_2\text{O}_3/\text{SiO}_2$ . Coarse and fine tuning of  $V_{FB}$  for  $\text{HfO}_2$  gate dielectrics were successfully observed by  $\text{La}_2\text{O}_3$  and  $\text{Sc}_2\text{O}_3$  incorporation, respectively.  $V_{FB}$  of MOS capacitors using high-k dielectrics could be controlled by the incorporation of  $\text{La}_2\text{O}_3$  or  $\text{Sc}_2\text{O}_3$  at the  $\text{HfO}_2/\text{SiO}_2$  interface.

## **Acknowledgments**

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## **References**

- [1] Y. Yamamoto, et al., Ext. Abst. of SSDM p.212, (2006)
- [2] Vidya S. Kaushik et al., IEEE Transaction on Electron Devices Vol 53, No10, (2006)
- [3] M. Kadoshima, et al., Symposium on VLSI Technology Digest of Technical Papers, p.226, (2006)
- [4] Rashmi Jha et al., IEEE Electron Device Letters, Vol 25, No6, June (2004)
- [5] "NCSU CVC Analysis, Version 5.0", (North Carolina State University, 2000).