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PAPER Special Section on Analog Circuit Techniques and Related Topics

Reduction of Bootstrapped Switch Area Consumption Using Pre-Charge Phase

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SUMMARY This paper discusses the input range limitation problem in a track-and-hold circuit and the compensation method using a bootstrapped switch. A bootstrapped switch with an additional control circuit is proposed to compensate charge loss in conventional bootstrapped switch circuit. Simulation results using 0.18-μm CMOS process parameters show that the proposed circuit reduces the bootstrap capacitance down to 25% for the conventional circuit.

key words: *track-and-hold circuit, bootstrapped switch*

1. Introduction

Along with the development in mixed-signal integrated system technologies, track-and-hold (TH) circuit becomes a key element since it is the gateway from the world of continuous-time to discrete-time signal processing.

A simple TH circuit is realized by a MOSFET and a capacitor as is shown in Fig. 1 where V_{IN}, V_{CLK} and V_{OUT} are the input signal (continuous-time), the switch clock and the output signal (discrete-time) respectively. Here the n-channel MOSFET is driven by V_{CLK} and operates in non-saturated region as a switch.

When the switch is turned-on, the output of TH circuit will track its input. This phase is called track phase. As the TH circuit is switched-off, it will store the charge in capacitor C until the next track phase. Therefore, the output of the circuit is held to the value of the input signal when the switch is turned-off. This phase is called hold phase.

There are some commonly known problems in the design of a TH circuit. They are

- power supply limitation
- bandwidth limitation
- charge injection
- clock feed through.

Assume that $V_{CLK} \leq V_{PS}$ (V_{PS}: power supply voltage), then the maximum input voltage V_{IN_MAX} is given by

$$V_{IN\_MAX} = V_{PS} - V_T \tag{1}$$

where V_T is the threshold voltage of a MOSFET. This means the maximum input voltage is limited by power supply and MOSFET's threshold voltages. Input voltage of a TH circuit should not exceed the value given in Eq. (1) or the MOSFET will fall into weak inversion region during track phase. Furthermore, the use of low-V_T devices is commonly not preferable since it will increase leakage current. In deep sub-micron processes, where the device's breakdown voltage is getting lower, this will be a significant problem.

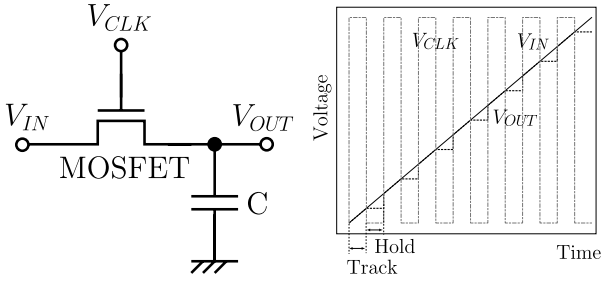

Fig. 1 Simple TH circuit (n-channel MOSFET).

Although most of TH circuit analysis are large-signal analysis, in order to get a rough estimation on the maximum input frequency of the switch, a small-signal analysis is more convenient. Since a MOSFET switch in Fig. 1 operates in non-saturated region, its drain current, I_{SW} will be given as [1]

$$I_{SW} = 2K\left(V_{GS} - V_T - \frac{V_{DS}}{2}\right)V_{DS} \tag{2}$$

$$I_{SW} = 2K\left(V_{CLK} - V_{OUT} - V_T - \frac{V_{IN} - V_{OUT}}{2}\right) \times (V_{IN} - V_{OUT}) \tag{3}$$

with an assumption that $V_{IN} > V_{OUT}$. Here K is the transconductance parameter of a MOSFET. The partial differential of Eq. (2) will be given by

$$\frac{\partial I_{SW}}{\partial V_{DS}} = 2K(V_{GS} - V_T - V_{DS}), \tag{4}$$

$$R_{ON} = \frac{\partial V_{DS}}{\partial I_{SW}} = \frac{1}{2K(V_{GS} - V_T - V_{DS})}. \tag{5}$$

If $V_{DS} \ll V_{GS} - V_T$ then

$$R_{ON} \approx \frac{1}{2K(V_{GS} - V_T)}. \tag{6}$$

Here R_{ON} is called "on-resistance" of the MOSFET switch. This means the small signal equivalent circuit of TH circuit

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is a "low-pass filter" made of R_{ON} and C. The cutoff frequency of the "filter," f_c is

$$f_c = \frac{1}{2\pi C R_{ON}} \approx \frac{2K(V_{GS} - V_T)}{2\pi C}. \quad (7)$$

As a result, the bandwidth of TH circuit is limited by the value of "on-resistance" and load capacitance. With a given load capacitance, bandwidth improvement is achieved by increasing MOSFET's channel width with the cost of larger power consumption and area.

Charge injection and clock feed through cause fluctuations of the voltage held by the load capacitance during the hold phase. Ideally the relation between output voltage V_{OUT} and input voltage V_{IN} is

$$V_{OUT} = V_{IN}, \quad (8)$$

however with charge injection, it will be

$$V_{OUT} = V_{IN} - \frac{C_{OX}WL}{2C}(V_{CLK} - V_{IN} - V_T), \quad (9)$$

where C_{OX}, W, and L are the channel capacitance per unit area, the channel width and length of the switch respectively. On the other hand, the output voltage V_{OUT} with clock feed through will be given by

$$V_{OUT} = V_{IN} - \frac{C_{OVL}W}{C + C_{OVL}W}V_{CLK}, \quad (10)$$

where C_{OVL} is the overlap capacitance per unit length. Since an overlap capacitance is much more smaller than the channel capacitance, the effect of clock feed through is less significant compared to the one of charge injection.

This paper proposes a TH circuit based on a bootstrapped switch. A conventional compensation of input range limitation of a TH circuit using a bootstrapped switch will be explained in Sect. 2. Improvement of a bootstrapped switch using a simple additional control circuit will be explained in Sect. 3.

2. Bootstrapped Switch

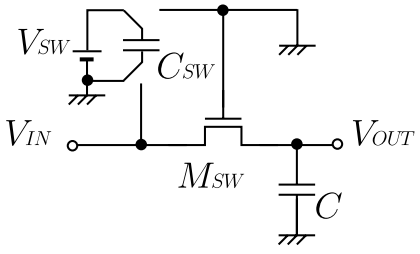
Deep sub-micron processes provide higher operating frequency with the cost of lower device breakdown voltage. As a result the power supply voltage of TH circuit becomes lower and thus reduces its input range (see Eq. (1)). A conventional bootstrapped switch [2]–[6], [8] as is shown in Fig. 2 has been proposed to expand the input range of TH circuit with low supply voltage. A bootstrap capacitor C_{SW} is added to provide the switching voltage.

During the hold phase, C_{SW} is charged by a voltage source V_{SW}. In the track phase, C_{SW} is connected between the input of TH circuit and the MOSFET's gate to turn the switch on. Assume that $V_{OUT} = V_{IN}$, the gate-to-source voltage of the MOSFET will be equal to V_{SW} regardless of the value of V_{IN}. This means as long as $V_{SW} > V_T$ then the TH circuit will work properly. Of course it still has a limitation. The allowed input voltage range of the bootstrapped switch is

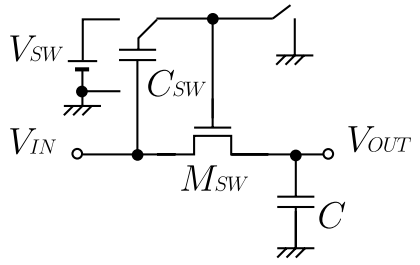
$$V_{IN} \le V_{BD} - V_{SW} \quad (11)$$

where V_{BD} is the breakdown voltage of the MOSFET. Here the input range is independent of supply voltage although it is limited by the device's breakdown voltage.

As the bootstrapped switch moves from hold phase to track phase, the MOSFET switch will create its channel.



(a) Hold phase



(b) Track phase

Fig. 2 Basic operation of bootstrapped switch.

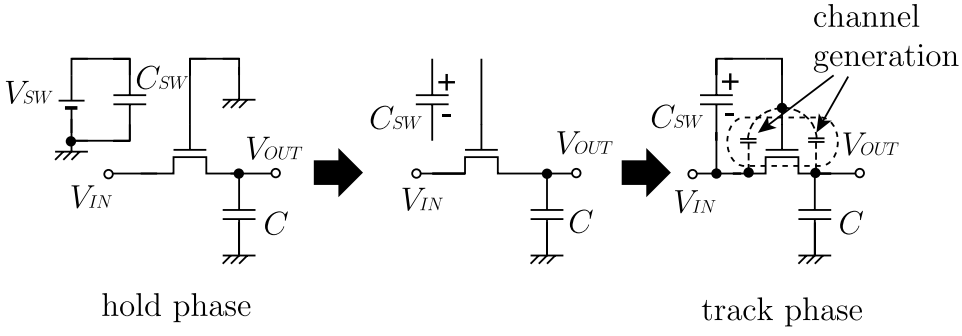


Fig. 3 The effect of channel generation in MOSFET switch.

The generation of channel needs accumulation of charges where negative charges will be drawn from a power supply (ground). However since the gate is only connected to C_{SW}, the positive charges required to pull-up the gate potential (to turn the MOSFET on) will be drawn from C_{SW} (see Fig. 3). As a result there will be a "charge leakage" from C_{SW} and thus reduce the voltage between its terminals. Assume that the voltages between C_{SW}'s terminals at the beginning and at the end of track phase are V_{SW} and V_{SWconv}, the relation between them will be given by

$$V_{SWconv} = \frac{C_{SW}}{C_{SW} + C_{OX}WL}(V_{SW} + V_{IN}) \tag{12}$$

Equation (12) shows that in order to keep the switching voltage V_{SWconv} as large as possible, larger bootstrap capacitance is required. Since load capacitor C is determined by circuit blocks following TH circuit (for example comparators array in A/D converter), a large scale circuit should use a larger switch otherwise the bandwidth of TH circuit will be reduced. Larger MOSFET switch needs larger bootstrap capacitor.

3. Proposed Circuit

Figure 4 shows the basic operation of the proposed bootstrapped switch. Using the charge preservation law, the switching voltage at the end of track phase for the proposed switch V_{SWprop} will be given by

$$V_{SWprop} = \frac{C_{OX}WL}{C_{SW} + C_{OX}WL}V_{DD} + \frac{C_{SW}}{C_{SW} + C_{OX}WL}(V_{SW} + V_{IN}). \tag{13}$$

From Eqs. (12) and (13), it is clear that the first term of Eq. (13) is the additional term from the pre-charge phase. Therefore the proposed switch will have a larger switching voltage than the conventional one when the bootstrap capacitance C_{SW} is equal.

The ratio of bootstrap capacitance of the conventional and proposed switch can be calculated with the assumption that the switching voltage of both circuits are equal. Therefore,

$$\frac{C_{SWconv}(V_{SW} + V_{IN})}{C_{SWconv} + C_{OX}WL} = \frac{C_{OX}WLV_{DD}}{C_{SWprop} + C_{OX}WL} + \frac{C_{SWprop}(V_{SW} + V_{IN})}{C_{SWprop} + C_{OX}WL}, \tag{14}$$

and as a result,

$$C_{SWprop} = \frac{V_{IN} + V_{SW} - V_{DD}}{V_{SW} + V_{IN}}C_{SWconv} - \frac{V_{DD}}{V_{SW} + V_{IN}}C_{OX}WL. \tag{15}$$

In case $V_{SW} = V_{DD}$, then

$$C_{SWprop} = \frac{V_{IN}}{V_{DD} + V_{IN}}C_{SWconv} - \frac{V_{DD}}{V_{DD} + V_{IN}}C_{OX}WL. \tag{16}$$

Since V_{IN} will always be smaller than V_{DD}, Eq. (16) shows that the bootstrap capacitance of the proposed switch will always be smaller than the conventional one. The ratio of bootstrap capacitance then will be given by

$$\frac{C_{SWprop}}{C_{SWconv}} = 1 - \frac{1 + c}{1 + v}, \tag{17}$$

where

$$c = \frac{C_{OX}WL}{C_{SWconv}} \tag{18}$$

$$v = \frac{V_{IN}}{V_{DD}}. \tag{19}$$

Figure 5 plots the ratio of bootstrap capacitance in the proposed circuit to the one of conventional circuit as is given in Eq. (17). It shows that even for a rail-to-rail input ($v = 1$), the proposed circuit has a smaller bootstrap capacitor.

The maximum input voltage can be estimated using Eqs. (7) and (12) for the conventional circuit and (13) for the proposed circuit. As a result, the maximum input voltage V_{INmax} for the conventional circuit is

$$V_{INmax} = \frac{C_{SW}}{C_{OX}WL}V_{SW} - \frac{C_{SW} + C_{OX}WL}{C_{OX}WL}\left(\frac{\omega_C C}{2K} + V_T\right) \tag{20}$$

while the maximum input voltage for the proposed circuit

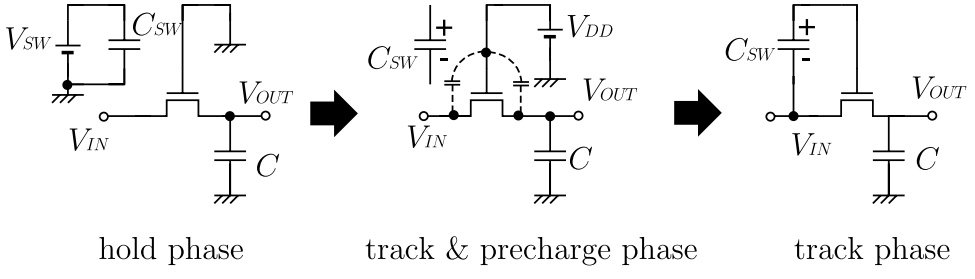


Fig. 4 Bootstrapped switch with track & pre-charge phase.

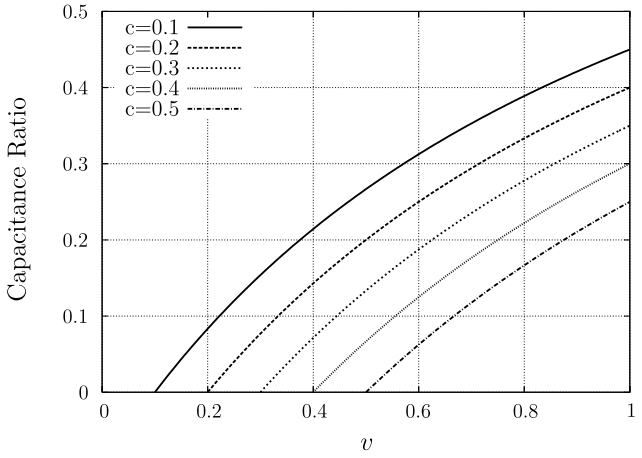


Fig. 5 Bootstrap capacitance ratio.

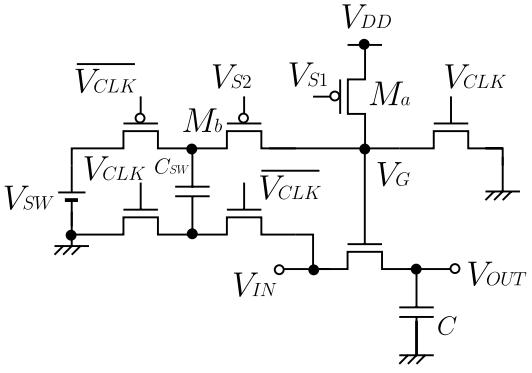


Fig. 6 Implementation of the proposed bootstrapped switch.

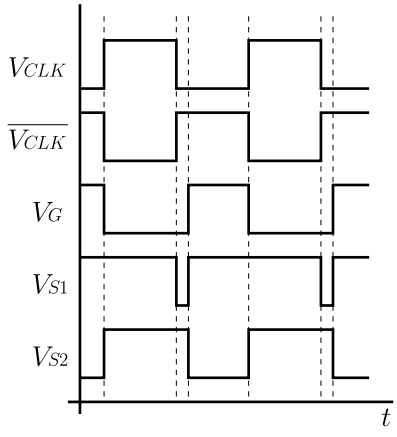


Fig. 7 Switching scheme for the proposed TH circuit.

will be given by

$$V_{INmax} = V_{DD} + \frac{C_{SW}}{C_{OX}WL}V_{SW} - \frac{C_{SW} + C_{OX}WL}{C_{OX}WL}\left(\frac{\omega_C C}{2K} + V_T\right). \quad (21)$$

Equations (20) and (21) show that for a given switch size, bootstrap capacitance and maximum input frequency, the proposed bootstrapped switch has a larger input voltage than the conventional one.

Table 1 Logical table for control circuit.

V_{CLK}	V_G	V_{S1}
1	1	1
1	0	1
0	1	1
0	0	0

$\overline{V_{CLK}}$	V_G	V_{S2}
1	1	0
1	0	1
0	1	1
0	0	1

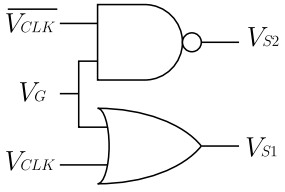


Fig. 8 Control circuit for the proposed bootstrapped switch.

The implementation of the proposed bootstrapped switch is shown in Fig. 6. The circuit topology is almost the same to the conventional one except for the addition of one MOSFET (M_a) to pre-charge the main switch and a logic circuit to create control signals V_{S1} and V_{S2}.

At hold phase, V_{CLK}, V_{S1} and V_{S2} are at high level. Next, V_{CLK} and V_{S1} turn to low-level and thus V_G moves toward V_{DD}. As soon as V_G reaches V_{DD}, V_{S1} is switched to high-level and disconnecting MOSFET's gate from V_{DD}. V_{S2} is then turned to low-level to connect bootstrap capacitor to the gate of MOSFET switch and the TH circuit completely moves to track phase. Finally, V_{S2} and V_{CLK} are turned to high-level and the TH circuit goes back to hold phase. The switching scheme is illustrated in Fig. 7. The logical relations between $V_{CLK}, \overline{V_{CLK}}, V_G, V_{S1}$ and V_{S2} are listed in Table 1. Here a control circuit for the proposed circuit can be realized using one NAND and OR gates as is shown in Fig. 8.

4. Simulation Result

The proposed circuit is simulated using Spectre circuit simulator with 0.18-μm CMOS process parameters. The power supply voltage and bootstrap voltage V_{SW} are 1 V. The size of the main switch and the value of load capacitance are 30 μm/0.24 μm and 5 pF respectively. The basic conventional bootstrapped switch in Fig. 2 is used for performance comparison. A non-overlapping clock with a frequency of 100MHz is used to drive both the conventional and proposed bootstrapped switches. A 500 $\mathrm{mV_{pp}}$ sinusoidal wave at 25MHz is added to both conventional and proposed circuits as an input signal. The input common mode is set to 350mV assuming that a buffer is preceding the TH circuit. Figure 9 shows the simulation result when both conventional and proposed TH circuits use a bootstrap capacitor with the same value (200 fF). For the given input signal, the conventional TH circuit failed to track the input signal correctly when the level exceeds the common mode voltage. As a

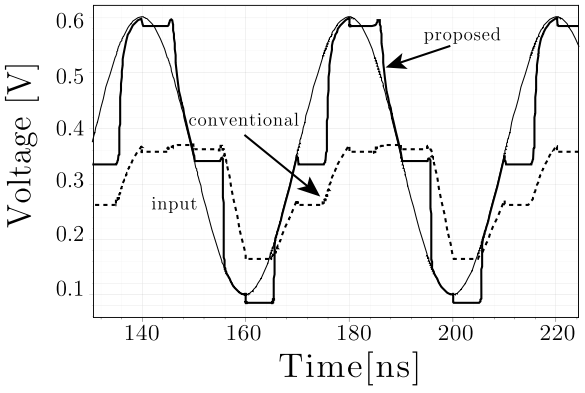


Fig. 9 Simulation result with C_{SW} = 200 fF for both conventional (Fig. 2) and proposed TH circuits (Fig. 6).

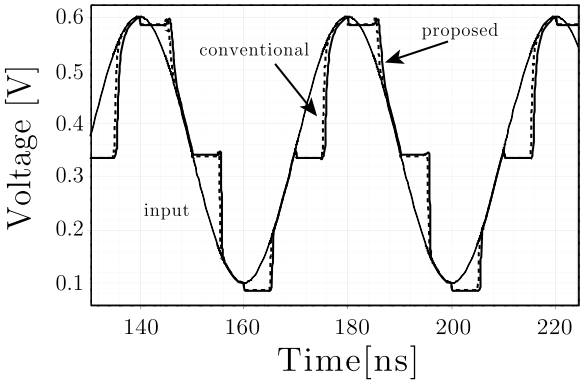


Fig. 10 Simulation result with C_{SW} = 800 fF for conventional circuit (Fig. 2) and C_{SW} = 200 fF for proposed circuit (Fig. 6).

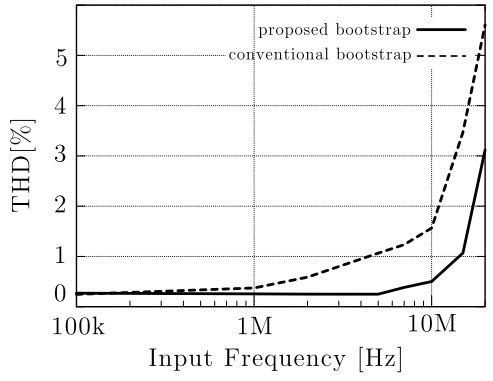


Fig. 11 Total harmonic distortion of conventional (Fig. 2) and proposed bootstrapped switches (Fig. 6) with f_s = 100 MHz, V_{IN} = 500 mV_{pp}.

result, the output signal for high-level input is greatly distorted. On the other hand, the proposed circuit is capable of tracking the input signal without suffering too much signal degradation using the same bootstrap capacitance. In both cases, there is a level shifting in output voltage when the TH circuit moves to hold phase. This is mainly caused by charge injection [7].

Figure 10 shows the simulation result when C_{SW} = 800 fF is used in the conventional circuit. The proposed circuit uses 200 fF as the bootstrap capacitor. This means that the proposed TH circuit uses only 25% of capacitance used in the conventional circuit to achieve the same output. Although the proposed circuit needs additional control circuit, the area of the capacitor is still dominant and therefore the total area of the proposed circuit, which uses a smaller capacitor, is smaller than the conventional one. Finally, Fig. 11 shows the THD simulation result. The proposed circuit achieves THD of −52 dB@5 MHz and −46 dB@10 MHz while the THD for input frequencies up to 15 MHz is below 1%.

5. Discussions

5.1 Timing Overhead

As is explained in Sect. 3, the proposed bootstrapped switch has an additional timing scheme to control the pre-charge phase. At a glance, it seems that the proposed circuit will need a large timing overhead and therefore will degrade its maximum operation frequency. This section will discuss about this timing overhead.

A simple conventional bootstrapped switch will have a similar topology to the proposed one (Fig. 6) except that there will be no pre-charge MOS switch (M_a) and M_b will be driven by V_{CLK} instead of V_{S2}. This means the main switch in the conventional circuit will be turned on immediately when V_{CLK} turns to logical "0" (in fact there will be a transition time of the gate to reach sufficient voltage to turn the switch on). On the other hand, the main switch of the proposed circuit will be turned on a little bit later because there will be a delay mainly caused by control circuit.

Assume that the main switch in Fig. 6 is in the off state. In order to turn on the main switch, V_{S1} of the control circuit (Fig. 8) should be changed from logical "1" to "0." Here the time required by OR gate to fall to "0" state (define it as $\tau_{OR-fall}$) will be the additional delay before the gate voltage of the main switch starts to increase. Another factor which has a possibility to add time delay is the "gate slewing" time (define it as τ_g). Since both the conventional and proposed circuits will suffer from this "gate slewing" delay, then the net delay will be given by the difference between them ($\tau_{g-prop} - \tau_{g-conv}$). Because the main switch in both the conventional and the proposed circuits are turned off at the same timing, the difference of duration where the switch is in the ON state will be given by $\Delta\tau_{on}$

$$\Delta\tau_{on} = \tau_{OR-fall} + \tau_{g-prop} - \tau_{g-conv}. \quad (22)$$

As a result, the main switch of the conventional circuit will be turned on $\Delta\tau_{on}$ longer than the proposed one. From simulation results for the given simulation setup in Sect. 4, $\Delta\tau_{on}$ = 370ps ($\tau_{or-fall} = 270ps$). This value equal to 3.7% of the clock period. From the above results, the fall time of OR gate is the main contributor of the timing overhead. This timing overhead will slightly reduce the maximum operating frequency of the proposed circuit. However a careful design of the control circuits will minimize it.

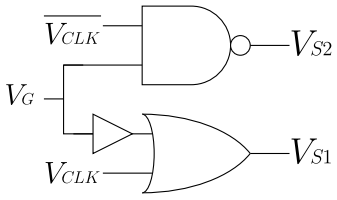


Fig. 12 Optional control circuit.

5.2 Timing Optimization

The control circuit in Fig. 8 is chosen for its simplicity. It is written in Sec.3 that as soon as V_G reaches V_{DD}, V_{S1} is switched to high level. However, in fact V_G is not exactly compared to V_{DD} in order to turn V_{S1} to high-level. As is shown in Fig. 8, V_G is one of the OR gate inputs while V_{S1} is the output of the gate. Therefore, V_{S1} will start to turn to high-level when V_G exceeds the threshold voltage of the OR gate. As a result, before V_G reaches V_{DD}, V_{S1} turns off M_a and M_b is turned on. This means the pre-charge phase does not give optimum performance.

An alternative solution to optimize the performance is by adding a fixed delay before inputting V_G to the OR gate as is shown in Fig. 12. This delay will enable V_G to reach higher voltage than the OR gate's threshold voltage without changing the output. However, as a consequence excessive delay will make the settling time of V_G become longer. The additional delay will not reduce the "ON state" duration of main switch because the output of OR gate only changes from "1" to "0" when V_{CLK} turns from "1" to "0" (Sect. 5.1).

6. Conclusions

A bootstrapped TH circuit with additional track and pre-charge phase is proposed. The proposed technique reduces the charge leak in bootstrap capacitor and thus enables the use of smaller capacitance without reducing the level of output signal. Simulation result using 0.18-μm CMOS process parameters shows that the proposed circuit reduces the bootstrap capacitance down to 25% for the conventional circuit. Although the proposed circuit needs an additional control circuit, the total area is still smaller than the conventional one. Furthermore, the THD of -52 dB@5 MHz is close to the result reported in [3].

Acknowledgment

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