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Substrate Noise Reduction Techniques in Mixed-Signal Integrated Circuits

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Contents

Chapter 1

Introduction

1.1 Backgrounds and Objective

Demands on high performance mixed-signal integrated circuits are increasing because of the advancing of multimedia technologies. Modern process technology enables integration of a large mixed-signal system on a relatively small chip area. In the case of high performance mixed-signal integrated circuits, both speed and precision have been the main demands. In order to meet these requirements, integration of sensitive analog circuits together with high-speed clocked digital circuits is the only solution.

Periodical behavior of digital circuits produces what so called digital noise[1]-[19]. This noise appears as the fluctuation of substrate level and has been observed in integrated circuits containing of digital circuits[20]-[26]. Thus, it is also called as substrate noise. The periodical operation of digital circuits will charge and discharge parasitic capacitances. These parasitic capacitances then will couple the switching signal to the substrate. Since a substrate can be assumed as a pure resistive network[27],[73] for frequencies up to few gigahertz, then it will spread over the noise to the entire chip [27],[28].

Many designers use physical approaches to improve the immunity to digital substrate noise on a mixed-signal circuit [53]-[58]. A passive guard ring has been commonly used to reduce the substrate fluctuation [59]. However, it only suppresses the noise coupled through a substrate's surface and has quite small effect on noise transfered through the deep portion of a substrate. Other methods such as active decoupling[60], utilization of low noise digital circuits[62, 63] are also introduced.

Active noise cancellation techniques have been introduced to suppress the noise coupled through deep portion of a substrate[66]-[72]. The circuit

proposed in [66] is an off-chip circuit. Circuits based on AC coupling are proposed in [67]-[70],[72]. The circuits in [67]-[69] are on-chip although external components are still needed. The circuits in [70] and [72] use small coupling capacitances and thus incapable of reducing low-frequency noise. The circuit in [71] uses a digitally driven well to reduce the substrate noise.

The implementation of a fully on-chip active guard band circuit is the main objective of this research because the use of additional external elements will degrade the cost performance.

1.2 Organization of The Dissertation

First, physical characteristic, the modeling of a substrate, and the basic knowledge on digital noise suppression techniques will be explained in Chapter 2. Layouts of a guard ring and diffusion bands for circuit evaluation are also discussed in this chapter. Chapter 3 will introduce the conventional active shield circuit followed by its main drawback. The proposed integration method which enables the integration of an active shield circuit on a chip will also be described in this chapter. A fully integrated active shield circuit is proposed and its performance is confirmed by simulations and experimental chip measurements. Chapter 4 will describe a design methodology of an active shield circuit based on the evaluation of the average noise transfer function. The validity of the proposed design method is confirmed by simulation. Chapter 5 will discuss different layouts for active shield circuit. It will show the major shortcoming of the conventional layout and offer alternatives to solve the problem. Chapter 6 will describe the utilization of an automatic gain control scheme to improve the performance of the proposed active shield circuit. Finally this dissertation will be concluded in Chapter 7.

Chapter 2

Basic Knowledge

This chapter will describe the physical (electrical) properties of a substrate and how a model of substrate is derived from a layout of a guard ring and diffusion bands. The basic knowledge of noise suppression techniques will be introduced at the end of this chapter.

2.1 Substrate Modeling

2.1.1 Physical Characteristic

First, it is important to investigate the physical characteristic of a substrate in order to understand its electrical properties. This characteristic can be derived from the Maxwell's equation

$$\mathbf{J} = \text{curl } \mathbf{H} - \epsilon\frac{\partial \mathbf{E}}{\partial t} = \nabla \times \mathbf{H} - \epsilon\frac{\partial \mathbf{E}}{\partial t} \tag{2.1}$$

where $\mathbf{J}$, $\mathbf{H}$, $\mathbf{E}$, and ϵ are the current density, magnetic field, electric field, and dielectric constant respectively. Taking the divergence from both sides will give

$$\nabla\mathbf{J} = \nabla \times (\nabla\mathbf{H}) - \epsilon\frac{\partial \nabla\mathbf{E}}{\partial t}. \tag{2.2}$$

Since $\nabla\mathbf{H}$ is zero and $\mathbf{J} = \sigma\mathbf{E}$, then Eq.(2.2) will become

$$\nabla\mathbf{J} + \epsilon\frac{\partial \nabla\mathbf{E}}{\partial t} = 0 \tag{2.3}$$

$$\sigma\nabla\mathbf{E} + \epsilon\frac{\partial \nabla\mathbf{E}}{\partial t} = 0 \tag{2.4}$$

where σ is conductivity. Now assume that a substrate can be expressed by a group of cubes as is shown in Fig.2.1, that the potential of two nearby cubes

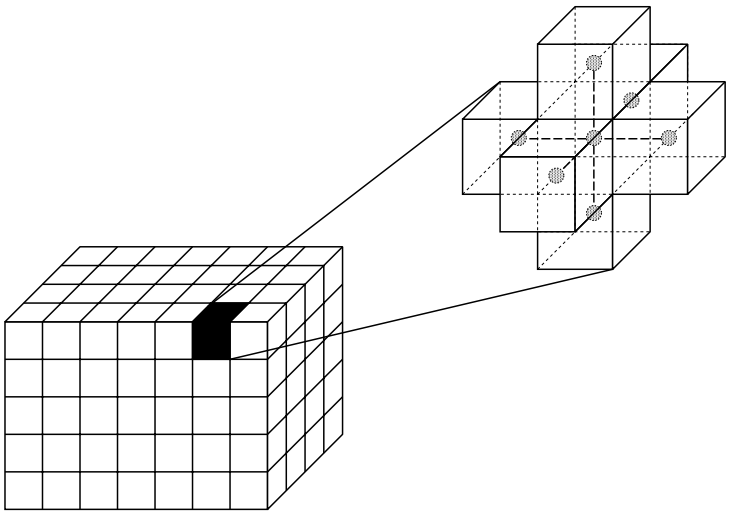

Figure 2.1: Discontinue representation of a substrate.

i and j are V_i and V_j respectively, and that the total charge in each cube lies on its center. If the distance between their centers of charge is l_{ij} then the electric field E_{ij} which is perpendicular to the border plane of both cubes can be defined as

$$E_{ij} = \frac{V_i - V_j}{l_{ij}}. \tag{2.5}$$

If the impurity concentration in each cube is uniform, substituting Eq.(2.5) into (2.4) and applying Gauss' Law will result in

$$\sum_{ij} \left(\sigma \frac{V_i - V_j}{l_{ij}} + \frac{1}{l_{ij}} \frac{\partial \rho}{\partial t} \right) = 0 \tag{2.6}$$

$$\sum_{ij} \left(R_{ij}^{-1}(V_i - V_j) + C_{ij} \frac{\partial (V_i - V_j)}{\partial t} \right) = 0 \tag{2.7}$$

where

$$R_{ij} = \frac{l_{ij}}{\sigma} \tag{2.8}$$

$$C_{ij} = \frac{\rho}{(V_i - V_j) l_{ij}}. \tag{2.9}$$

Equations (2.8) and (2.9) denote the parasitic resistance and capacitance between the center of cubes i and j. This means that the substrate can be

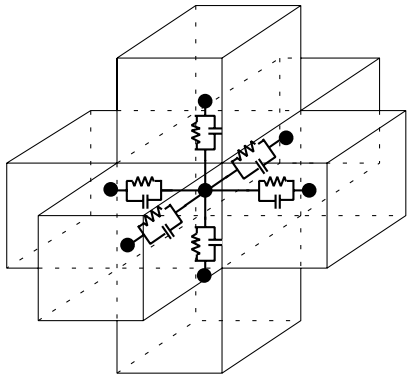

Figure 2.2: Representation of a substrate as a parasitic resistors and capacitors mesh.

represented by a mesh of parasitic resistors and capacitors as is shown in Fig.2.2.

The typical parasitic capacitance of silicon is 10fF for 100μm mesh size [73]. The time constant for 50Ωcm substrate is 10ps regardless of mesh size. This means that the substrate can be assumed as a pure resistive network at frequencies up to few gigahertz [27]. Here a substrate model using only resistors is used for the rest of this dissertation.

2.1.2 Guard Ring Layout and Modeling

In order to evaluate the circuit performance, a model of band layout will be discussed in this section. In the modeling procedure, some assumptions are made as followed :

1. The result from section 2.1.1 is used. Therefore the substrate is expressed by a resistors mesh.

2. The noise source is represented by a current source and only comes from one direction.

3. The substrate resistive network is represented by horizontal and vertical resistors. The values of the horizontal ones are determined by the distance between two nodes. Thus two-node pairs with the same distance between nodes are assumed to have the same resistances. The vertical ones are proportional to the area of the guard ring or the diffusion bands.

The layout of the guard ring and diffusion bands is shown in Fig.2.3. Five diffusion bands (A to E) are used in the evaluation of active shield circuits as noise sense nodes and cancellation signal injection nodes.

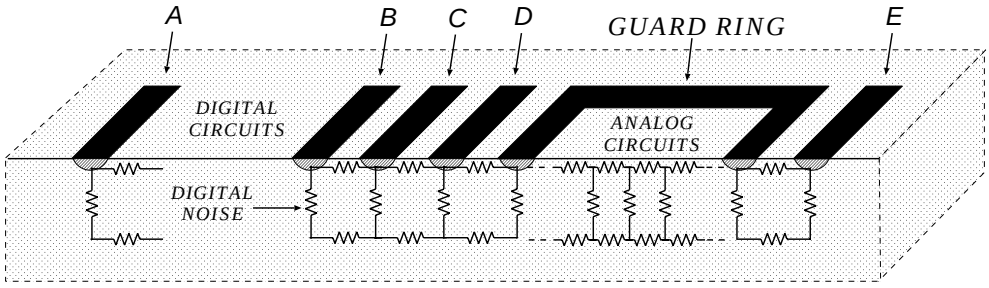

Figure 2.3: Layout of the guard ring and diffusion bands.

Since the circuits in this dissertation will be evaluated using a circuit simulator, it is necessary to implement the substrate layout shown in Fig.2.3 to a mesh resistive network. It is preferable to implement the substrate model as a 3-dimensional resistive network with a detailed mesh since it will give a more accurate result. However this will make the number of nodes increases and thus will also increase the simulation time. Some methods of simulating the substrate noise has been introduced[73]-[75]. This dissertation will use a rough substrate model to reduce simulation time and to make the calculation easier. Although the accuracy is decreased, the tendency is well preserved and it will be enough to examine the properties of various noise suppression techniques. The circuit model of the substrate is shown in Fig.2.4. The

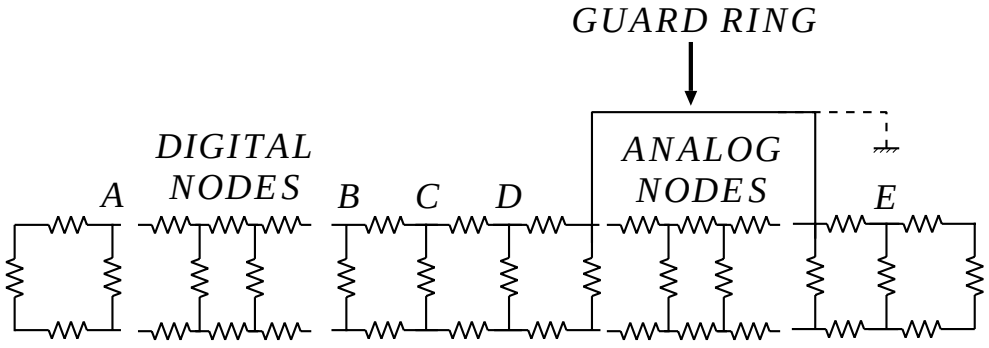

Figure 2.4: Circuit implementation of the guard ring and bands.

diffusion bands are represented by nodes **A** to **E** while the guard ring is

represented by connecting two nodes at each side of analog nodes. A few number of nodes are used to represent the digital and analog nodes where the noise will be injected and observed respectively. Furthermore the resistors at the bottom of the model represent the noise transfer path at the deep portion of a substrate. The model shown in Fig.2.4 is the complete model to evaluate the performance of noise reduction techniques in this dissertation. Since each technique uses different layout and does not use all of the nodes, the unused nodes will be omitted to simplify the calculation.

2.2 Noise Suppression Techniques

This section will introduce two types of noise suppression techniques. They are the passive guard ring and active noise cancellation techniques. Section 2.2.1 will explain the commonly used passive guard ring. Section 2.2.2 will describe the fundamental of active noise cancellation technique.

2.2.1 Passive Guard Ring

A passive guard ring is a commonly used technique to reduce the digital substrate noise. It is implemented simply by surrounding the analog circuits with a guard ring which is connected to an analog ground as is shown in Fig.2.5. The transfer function from the noise source i_n to the noise amplitude v_a at the observation point **a** will be given by

$$\frac{v_a}{i_n} = \frac{R_1 R_2 R_3 R_5 (R_3 + R_7)}{\alpha + \beta + \gamma} \tag{2.10}$$

where

$$\alpha = R_5(R_2 + R_3)(2R_2R_3 + R_2R_6 + R_3R_6) \tag{2.11}$$

$$\beta = R_5 R_7\{R_2(R_2 + 2R_3) + R_6(R_2 + R_3)\} \tag{2.12}$$

$$\begin{aligned}\gamma = {} & R_1\{R_2^2(2R_3 + R_6 + R_7) + R_3(R_5R_6 + (R_3 + R_7)(R_5 + R_6)) \\ & + R_2(2R_3^2 + R_5R_6 + (R_5 + R_6)R_7 + 2R_3(R_5 + R_6 + R_7))\}\end{aligned} \tag{2.13}$$

If there is no noise path into the deep portion of the substrate (by removing $R_4 \sim R_7$), then Eq.(2.10) will become zero which means that the noise will be totally removed by the passive guard ring. In other words, the passive guard ring will effectively reduce the noise transfered through the surface of a substrate. However, the fact is that there is a noise path into the deep portion of a substrate and therefore the digital noise is still observed inside the guard ring. This also proves that the passive guard ring cannot reduce the digital noise coupled through the deep portion of a substrate.

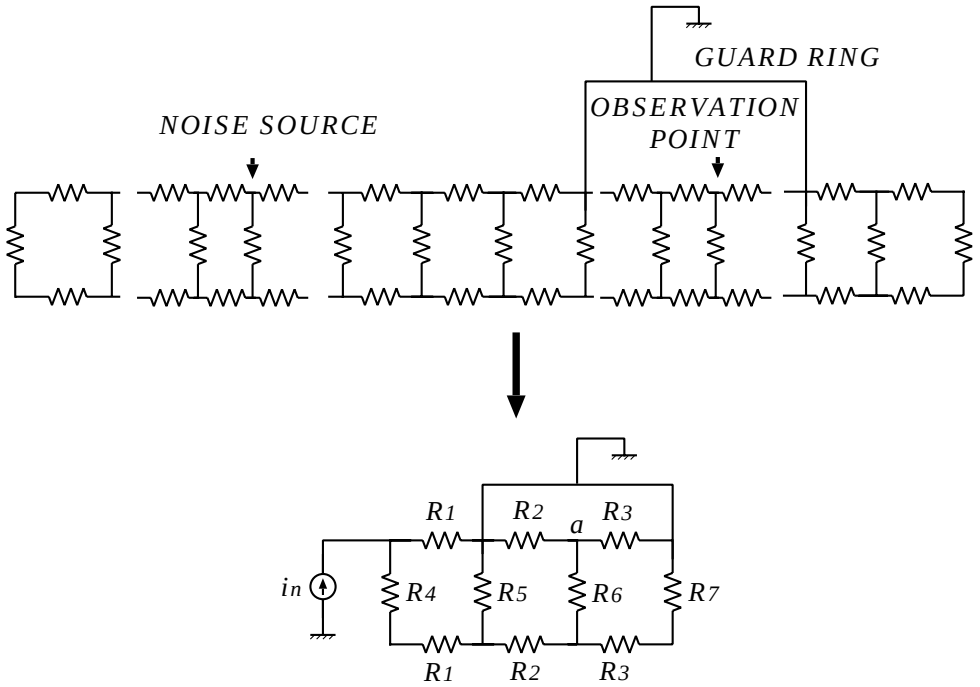

Figure 2.5: Simplified model of a passive guard ring.

2.2.2 Active Noise Cancellation

Section 2.2.1 explains that a passive guard ring cannot totally remove the digital noise because there is a noise path into the deep portion of a substrate. The only way to furthermore reduce the noise is by reducing the noise which is coupled through the deep portion of a substrate.

There are two approaches to reduce the noise coupled through the deep portion of a substrate. The first method is by using a physical approach. For examples, the use of SOI(Semiconductor On Insulator), process which has a low-impedance back-plane connected to ground or a triple-well process is known to have a good isolation of digital substrate noise. However these methods commonly need a special process and thus increase fabrication cost. The second approach is using a noise cancellation method by injecting a cancellation signal into the substrate. This method reduces the noise using the electrical properties and thus does not require special process. Indeed this method is highly recommended to be used on a standard double-well CMOS process which is relatively cheaper. The circuit used for this active noise cancellation then will be called active shield circuit.

Digital substrate noise is the fluctuation in a substrate and therefore its

bias level will be the same to the bias level of the substrate. For a p-type semiconductor substrate it will be equal to the lowest power supply while in an n-type semiconductor substrate it is the highest power supply. For this reason, the earlier active shield circuits are not integrated on the same chip and use a lower (or higher) power supply to drive the substrate of the mixed-signal integrated circuits.

Researchers make an effort to integrate the active shield circuits with approaches from both digital and analog circuits. This dissertation will discuss the approach from analog side in detail and therefore it will not be explained here. A brief explanation on the digital approach of active shield circuit will be given here. Figure 2.6 shows an implementation of active shield circuit using digital circuit.

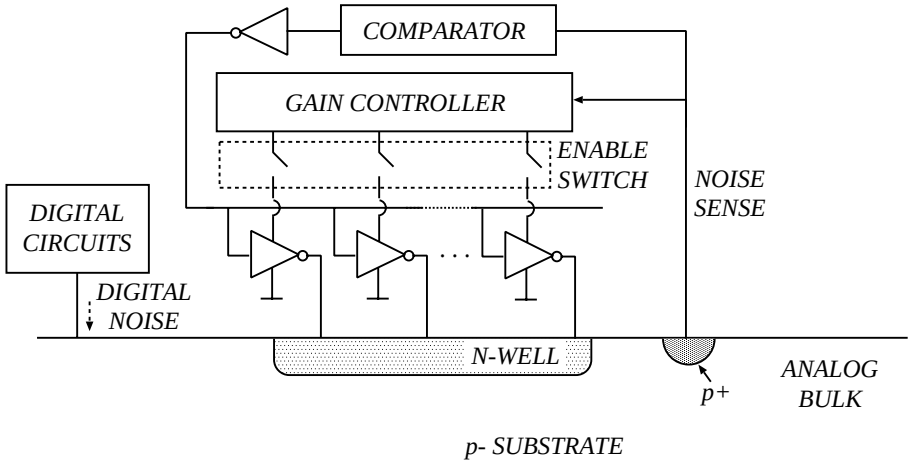

Figure 2.6: Digital implementation of an active shield circuit.

Since substrate noise is caused by the injection of charges into the substrate due to the periodical behavior of digital circuits, it is possible to create the cancellation signal using the same principle. First the substrate noise will be detected from a contact on the substrate between the digital area and analog area. This noise then will be used as the input of the inverters array after passed through a buffered comparator. The inverters then drive the n-well and produce the charge injection to reduce the noise amplitude. The detected noise amplitude will also be used as the input of a gain controller which then will determine how many inverters should be turned on.

Chapter 3

Fully Integrated Active Shield Circuit

This chapter will introduce the implementation of active shield circuits. The reason why the conventional active shield circuits cannot be fully integrated into a chip will also be described. Since external elements will increase the manufacturing cost, it will be preferable if the active shield circuit is fully integrated. The integration method will be explained and then followed by the implementation of the proposed active shield circuit.

3.1 Conventional Active Shield Circuit

3.1.1 Circuit Principal

The conventional active noise cancellation is based on a signal cancellation using its opposite signal as is shown in Fig.3.1. Here the transfer function from v_n to the potential v_a at node **a** will be given by

$$\frac{v_a}{v_n} = \frac{R_2 - R_1}{R_1 + R_2}. \tag{3.1}$$

With an assumption that the resistances are symmetrical($R_1 = R_2$), then Eq.(3.1) will become zero. The conventional active shield circuit uses the assumptions that the substrate resistances are symmetrical and the noise is injected exactly at the sense node. Furthermore it does not consider the analog area inside the guard ring as is shown in Fig.3.2.

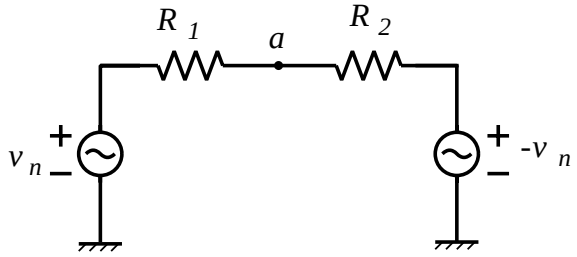

Figure 3.1: Basic of active noise cancellation technique.

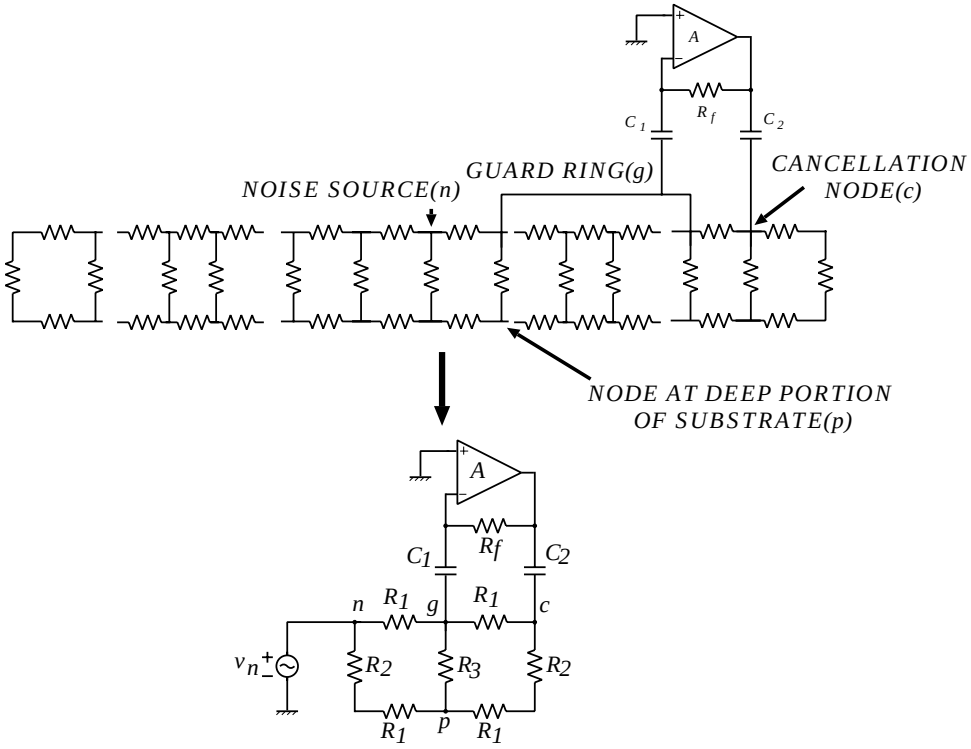

Figure 3.2: Conventional active shield circuit.

At a relatively high frequency, the transfer functions from v_n to the potential v_g at node **g** and to the potential v_p at node **p** will given by

$$\frac{v_g}{v_n} \approx \frac{1}{A} \tag{3.2}$$

$$\frac{v_p}{v_n} \approx \frac{R_a}{R_f} \tag{3.3}$$

where A is the open loop gain of the operational amplifier and R_a is

$$R_a = \frac{R_1^2 R_2}{(2R_1 + R_2)(2R_1 + 3R_2)} \tag{3.4}$$

respectively. Equations (3.2) and (3.3) show that the noise suppressions at nodes **g** and **p** are determined by the operational amplifier's open loop gain A and feedback resistance R_f respectively. Noise suppression at node **g** can be improved using a high-gain operational amplifier while noise suppression at node **p** is improved by increasing feedback resistance.

3.1.2 Drawbacks in Conventional Active Shield Circuit

There are some drawbacks in the conventional active shield circuit as is given below.

1. It uses an operational amplifier and needs a high gain to improve the noise suppression performance. This means that it is difficult to improve the speed of the circuit.

2. It needs a large feedback resistance R_f in order to achieve a proper suppression for the noise coupled through the deep portion of a substrate.

3. It uses capacitors C_1 and C_2 to separate the common mode level of the operational amplifier from the substrate bias. In order to guarantee that low frequency noise is not attenuated by the coupling capacitors, large capacitances are required (in fact it requires capacitances in the order of micro Farads).

The needs of large coupling capacitances and a feedback resistance make the conventional circuit not practically suitable for a fully on-chip implementation.

3.2 Inverter-Based Active Shield Circuit

3.2.1 DC Offset Technique

In order to integrate the overall circuit into the chip, AC coupling method using large capacitances should not be used. Therefore the active shield circuit should directly drive the substrate. Consider the block diagram in Fig.3.3. Assume that the circuit has a gain of -1 and the output bias level is zero. The output voltage v_o then will be given by

$$v_o = \begin{cases} V_{DD} & v_n < -V_{DD} \\ -v_n & -V_{DD} \leq v_n \leq 0. \\ 0 & v_n > 0 \end{cases} \tag{3.5}$$

Note that the circuit output cannot excess the power supply range($0 \sim V_{DD}$). Therefore when $v_n > 0$ the output voltage will always become zero and the circuit cannot work properly. It means that although the circuit can directly drive the substrate, it will not work properly as long as the output bias level is equal to the substrate bias level. In order to make the circuit work properly,

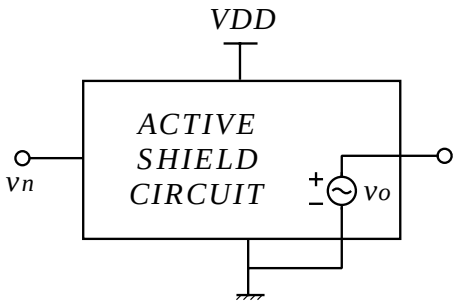

Figure 3.3: Active shield circuit without DC offset.

a DC offset is added to the output of the circuit as is shown in Fig.3.4. In this case, the output voltage of the circuit will be given by

$$v_o = \begin{cases} V_{DD} & v_n < -V_{DD} + V_{off} \\ -v_n & -V_{DD} + V_{off} \leq v_n \leq V_{off}. \\ 0 & v_n > V_{off} \end{cases} \tag{3.6}$$

It shows that the noise source v_n may have a maximum positive value of V_{off} and the circuit is still able to work properly. As a result, the use of DC offset technique will enable the integration of an overall active shield circuit into the chip.

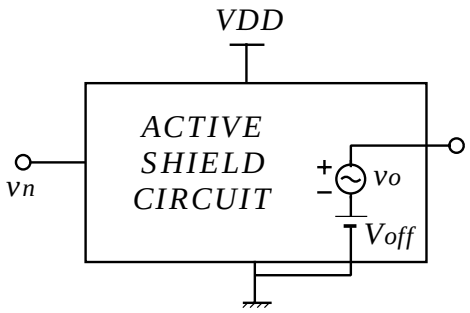

Figure 3.4: Active shield circuit with DC offset.

3.2.2 Circuit Implementation

This section will introduce the implementation of the active shield circuit based on an inverter. The DC offset technique is applied to make the entire proposed circuit able to be integrated on the chip.

Large Signal Analysis

Recall the conventional circuit in Fig.3.2. Under an ideal condition it can be redrawn as an inverting amplifier as is shown in Fig.3.5. It can be easily found that the transfer functions from v_n to the potentials v_g and v_p at nodes **g** and **p** will become zero. The implementation of the inverter-based active

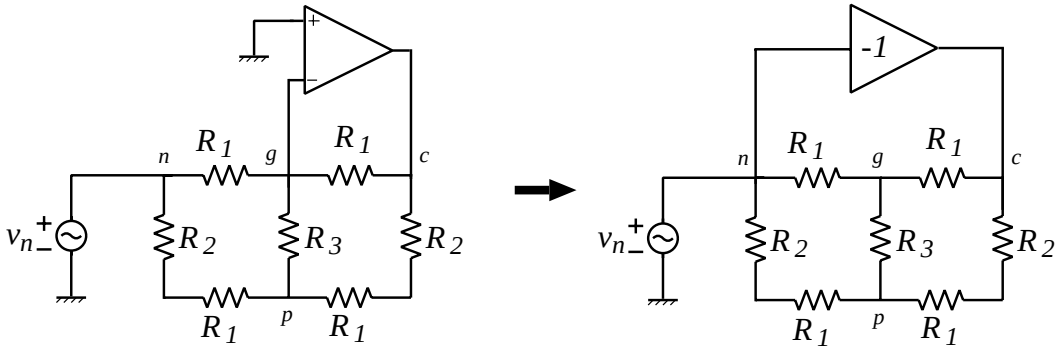

Figure 3.5: Inverter based active shield circuit.

shield circuit is shown in Fig.3.6. As is shown in Fig.3.6, the active shield circuit is realized using 4 current mirrors as the main part. Assume that when a noise source V_N is detected at node **n**, the drain currents of M_2 and M_6

are equal to I_2, and I_1 flows through M_1 and M_5. Assuming ideal matching between transistors will make the drain currents of M_3 and M_7 to be equal to I_1. In the same way, drain currents of M_4 and M_8 will be equal to I_2. These will result in $V_{GS1} = V_{GS3}$ and $V_{GS2} = V_{GS4}$. The relations between gate to

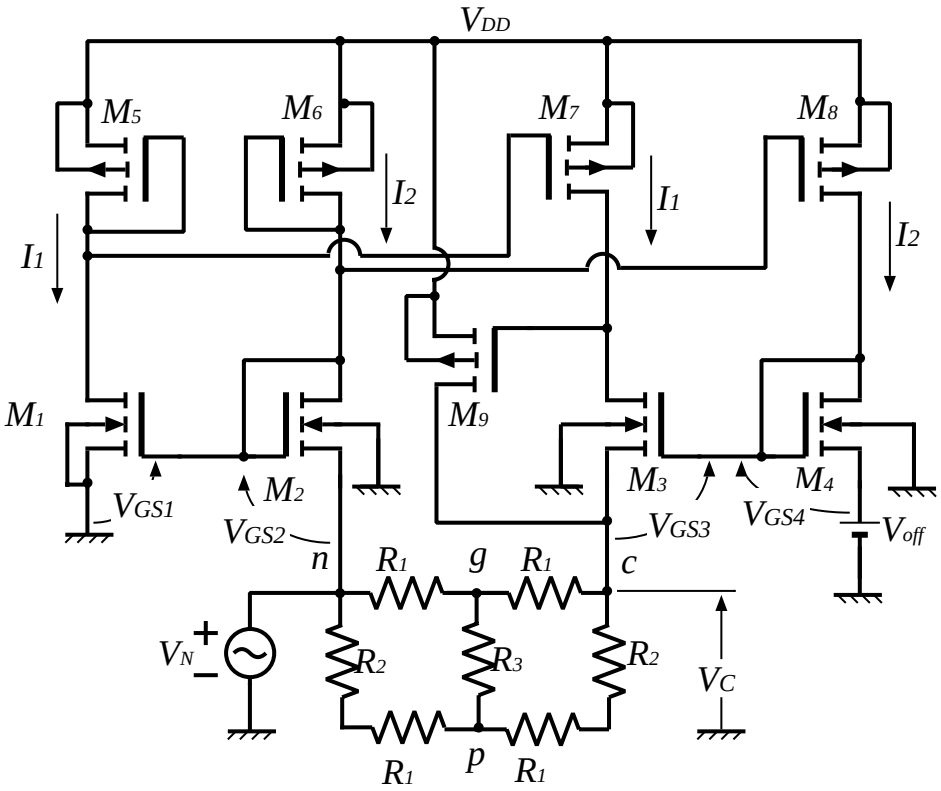

Figure 3.6: Inverter based active shield circuit with DC offset.

source voltages of NMOS transistors are

$$V_{GS1} = V_{GS2} + V_N \tag{3.7}$$

$$V_C + V_{GS3} = V_{off} + V_{GS4}. \tag{3.8}$$

Since $V_{GS1} = V_{GS3}$ and $V_{GS2} = V_{GS4}$, substituting Eq.(3.7) into Eq.(3.8) gives

$$V_C = V_{off} - V_N \tag{3.9}$$

$$V_G = V_P = \frac{V_{off}}{2}. \tag{3.10}$$

Since V_{off} is a constant voltage source, Eq.(3.9) shows that the proposed circuit works as an inverter because it produces $-V_N$ at the cancellation

band (node **c**) as an output. From Eq.(3.10) it is clear that the potential levels of nodes **g** and **p** will be constant.

Assume that V_N moves from 0 to a positive voltage. When it reaches $V_{off}/2$, then $V_C = V_{off}/2$ which is the same level with V_G and V_P. Here nodes **n**, **g**, **p** and **c** are at the same potential level, and no current flows through substrate resistances. This means no current flows in M_3, M_7, M_9 and the circuit is not working anymore for any input level bigger than $V_{off}/2$. On the other hand, when V_N moves to a negative voltage, such a limitation does not exist. Thus the input voltage range is limited by $V_{off}/2$.

Simulation Results

This section will show simulation results of the circuit in Fig.3.6 using HSpice and 1.2μm standard CMOS process parameters. Transistor sizes and the other parameter values are shown in Tables 3.1, 3.2, and 3.3.

Table 3.1: Transistors' W/L

MOS	**W(μm)**	**L(μm)**
M1..M8	6	1.2
M9	60	1.2

Table 3.2: Voltage sources

Name	Value[V]
V_{DD}	5
V_{off}	50m

Table 3.3: Substrate resistors

Name	Value[Ω]
R_1	100
R_2	50
R_3	20

The frequency characteristic of the active shield circuit is shown in Fig.3.7. Here the low-frequency noise suppression level of 22dB is obtained. Transient characteristic simulation is performed using a sine wave as an input signal. The results are shown in Figs.3.8 and 3.9. Fig.3.8 shows transient characteristic with 1MHz input frequency. Here the voltage fluctuation of node **p** is relatively small. This respects the small-signal simulation result where a noise suppression level of 22dB is obtained for input frequency up to 1MHz. On the other hand, voltage fluctuation of node **p** is observed from Fig.3.9 because there is no noise suppression effect at 100MHz. The total current dissipation is 874μA.

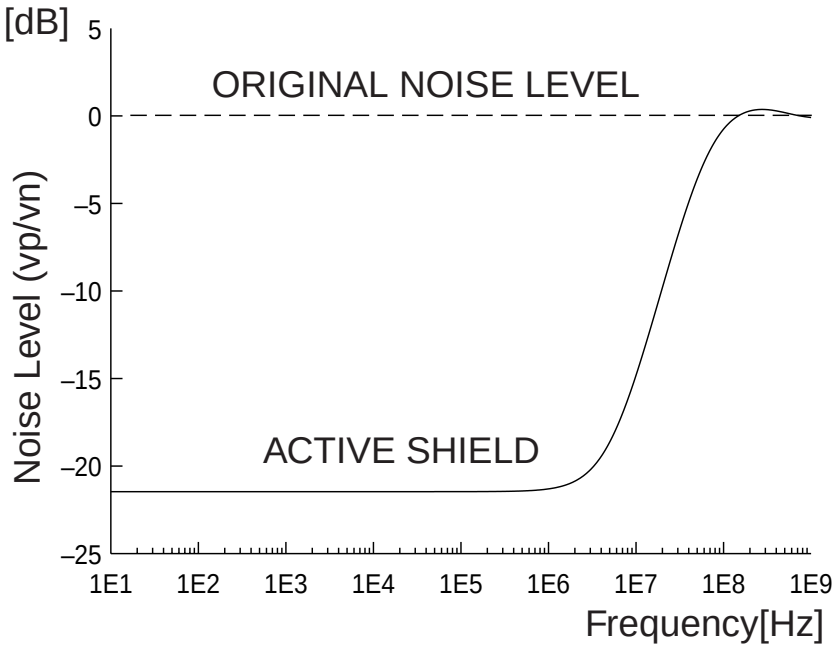

Figure 3.7: Simulated noise suppression level at node **p**.

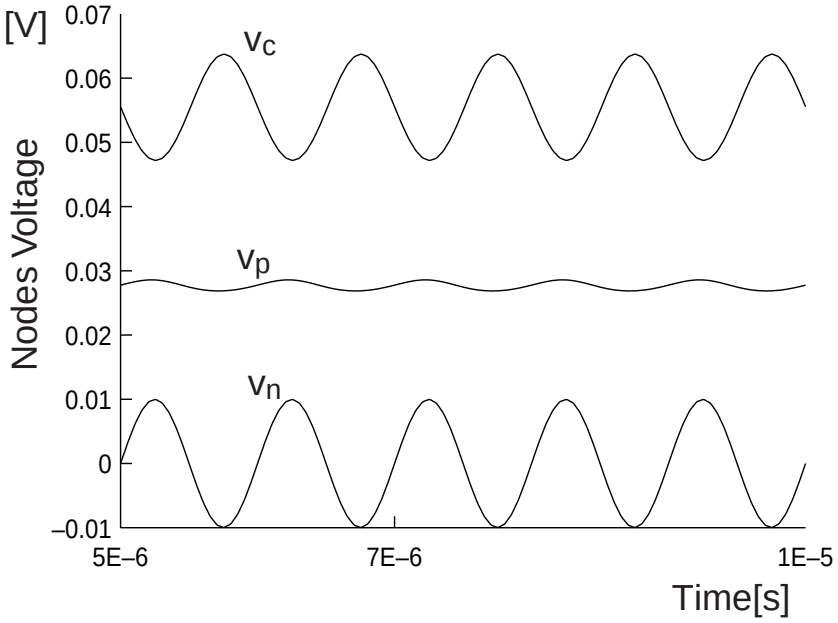

Figure 3.8: Simulated transient characteristic (Input signal : $20mV_{p\text{-}p}$ at 1MHz).

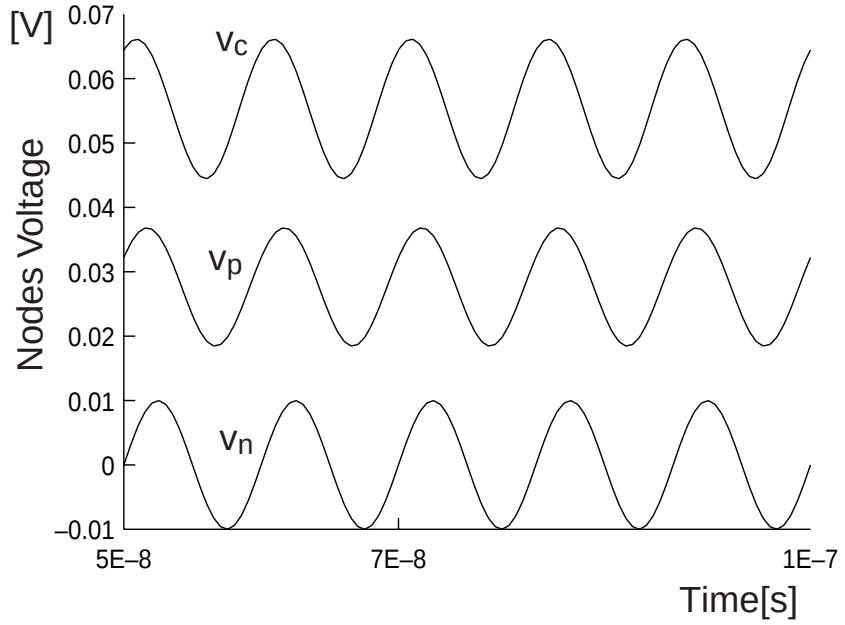

Figure 3.9: Simulated transient characteristic (Input signal : $20\text{mV}_{\text{p-p}}$ at 100MHz).

Power Supply Rejection Ratio and Effect of Unideal Offset Voltage Source

Note that M_2 and M_6 in Fig.3.6 are diode-connected MOS transistors between the power supply and the sense node. The bias current of the circuit then will be determined by the supply voltage V_{DD} and transconductances of M_2 and M_6. This makes disadvantages of the active shield circuit in Fig.3.6.

First, any fluctuation in the supply voltage causes fluctuation in bias current and will greatly affect the circuit performance. Second, note that I_2 changes with the fluctuation in input signal. Since it flows into the reference voltage V_{off}, any internal resistance existence will cause the reference voltage fluctuation. This will reduce the circuit performance as is shown in Fig.3.10.

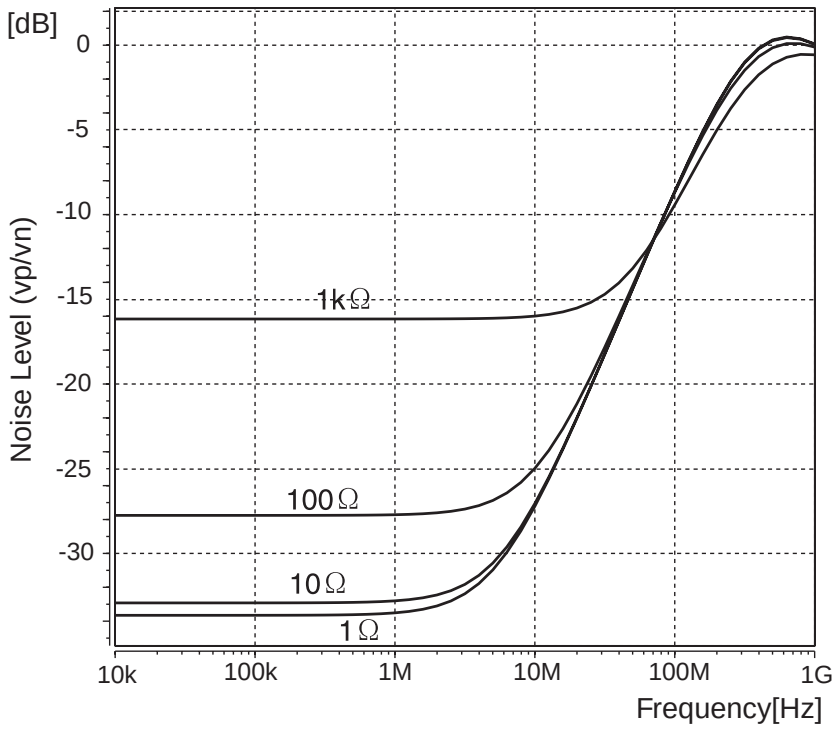

Figure 3.10: Effect of unideal reference voltage with various internal resistances

Circuit improvement

In the previous section, it is found that the active shield circuit in Fig.3.6 has poor characteristics versus a power supply and the internal resistance of a reference voltage. In this section, an active shield circuit with an improved Power Supply Rejection Ratio(PSRR) characteristic will be introduced.

Since the pair of the diode-connected M_2 and M_6 is the main cause of a poor PSRR characteristic in the active shield circuit in Fig.3.6, removing one of them is expected to improve the PSRR. Here, M_6 and its pair M_8 are replaced by constant current sources as is shown in Fig.3.11.

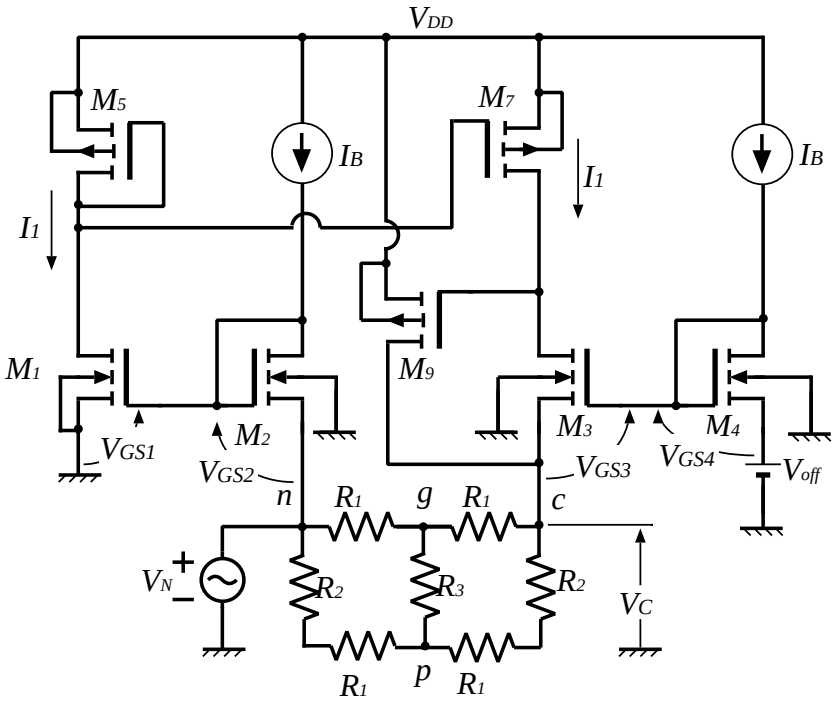

Figure 3.11: Active shield circuit with improved PSRR.

Except for the current sources, the rest of the circuit is the same as the circuit in Fig.3.6. This implies that the proposed circuit in Fig.3.11 still works as an inverter. Furthermore, bias currents of the proposed circuit are determined by I_B only. This results in a power-supply independent biasing and therefore improving PSRR. In addition, since the current flows into voltage reference is constant, the internal resistance of the voltage source will not have any effect on the noise suppression performance of the active shield circuit. This will make the design of the circuit become easier.

The simulation result of the gain of the inverter when V_{DD} is varied $\pm 10\%$ is shown in Fig.3.12. Here the conventional and proposed circuits are the ones shown in Figs.3.6 and 3.11 respectively. Note that the gain of the circuit in Fig.3.6 is greatly affected by the fluctuation of power supply. On the other hand, the inverter gain of the circuit in Fig.3.11 is relatively constant even if the power supply is varying.

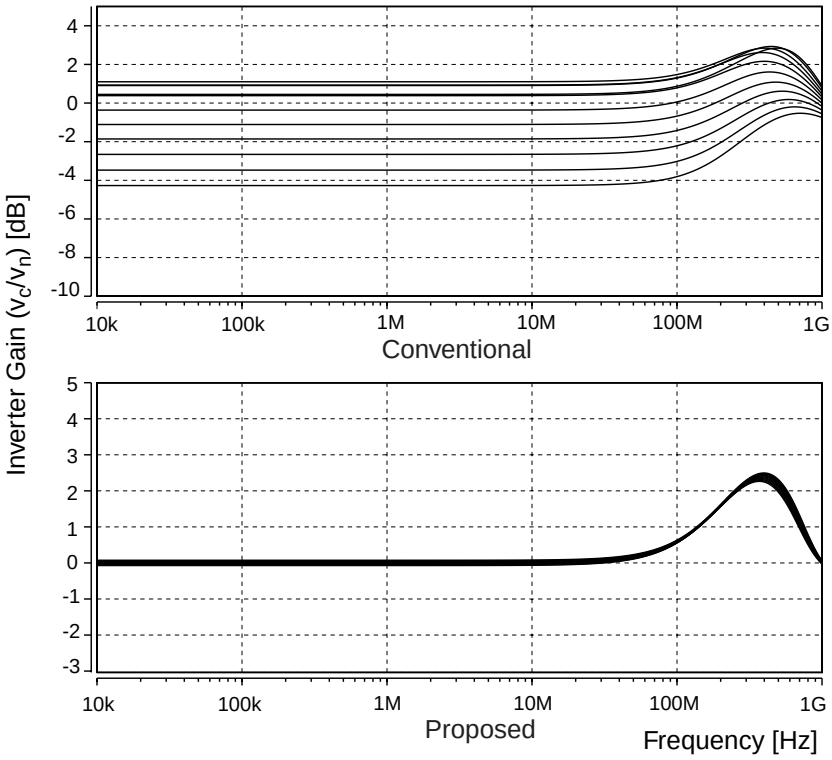

Figure 3.12: The inverter gain when V_{DD} varies $\pm 10\%$.

3.2.3 Design Optimization

The design optimization of the active shield circuit with consideration on device mismatch and frequency characteristic will be discussed in this section. The simplified active shield circuit shown in Fig.3.13 will be used. Here MOS transistor M_1 works as a V-I converter. The drain current of M_1 then will be copied by the current mirror M_3-M_4 such that the drain current of M_2 is equal to that of M_1. Finally M_2 will convert its drain current to output voltage. Since this circuit directly drives the substrate and creates a DC offset, it needs an extra bias current. This current will be supplied by M_5 while it will also fixed the drain voltages of M_2 and M_4.

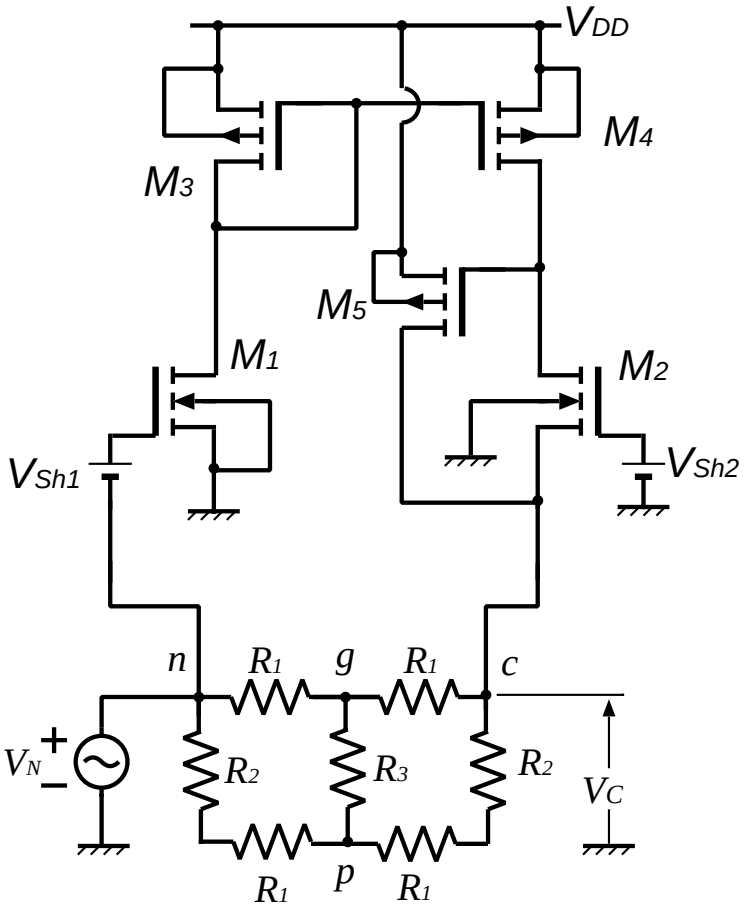

Figure 3.13: Simplified inverter-based active shield circuit with DC offset.

Here the operation of the circuit will be analyzed in order to make sure that the circuit still have the same performance to the circuit in Fig.3.11.

Under the assumption that all MOS transistors operate at the saturation region, the drain current of M_1 will be given by

$$\begin{aligned} I_{D1} &= K_1(V_{GS1} - V_{THN})^2 && (3.11)\\ &= K_1(V_N + V_{Sh1} - V_{THN})^2 && (3.12)\end{aligned}$$

where $K_n(n = 1, 2, 3, ..)$ is the MOS transistor's transconductance parameter and given by

$$K_n = \frac{\mu C_{OX}}{2}\frac{W_n}{L_n}. \quad (3.13)$$

Under an additional assumption that M_3 and M_4 make an ideal current mirror, then the drain current of M_2 is

$$I_{D2} = K_2(V_{GS2} - V_{THN})^2 = I_{D1}. \quad (3.14)$$

Solving Eqs.(3.12) and (3.14) for V_{GS2} will give

$$V_{GS2} = \sqrt{\frac{K_1}{K_2}}(V_N + V_{Sh1}) - \left(\sqrt{\frac{K_1}{K_2}} - 1\right) V_{THN}. \quad (3.15)$$

Finally, the output voltage V_C is

$$\begin{aligned} V_C &= V_{Sh2} - V_{GS2} && (3.16)\\ &= V_{Sh2} - \sqrt{\frac{K_1}{K_2}}(V_N + V_{Sh1}) - \left(\sqrt{\frac{K_1}{K_2}} - 1\right) V_{THN} && (3.17)\\ &= \left(V_{Sh2} - \sqrt{\frac{K_1}{K_2}}V_{Sh1}\right) + \left(\sqrt{\frac{K_1}{K_2}} - 1\right) V_{THN} - \sqrt{\frac{K_1}{K_2}}V_N. && (3.18)\end{aligned}$$

If it is assumed that the transconductance parameters of M_1 and M_2 are equal, then

$$V_C = V_{off} - V_N \quad (3.19)$$

where $V_{off} = V_{Sh2} - V_{Sh1}$. Here the output of the circuit contains a DC offset V_{off} and the inverted noise $-V_N$. Thus the circuit works as an inverter.

The small-signal equivalent circuit in Fig.3.14 is used to calculate the transfer function of the active shield circuit in Fig.3.13. The substrate resistance is replaced by an equivalent resistor R_{sub} in order to simplify the evaluation. Here the transfer function from v_n to v_c is given by

$$\frac{v_c}{v_n} \approx \frac{g_{m3}(r_{ds2} + r_{ds4}) + g_{m1}g_{m4}(1 - g_{m5}r_{ds2})r_{ds4}R_{sub}}{g_{m3}(r_{ds2} + r_{ds4}) + g_{m2}g_{m3}(1 + g_{m5}r_{ds4})r_{ds2}R_{sub}}. \quad (3.20)$$

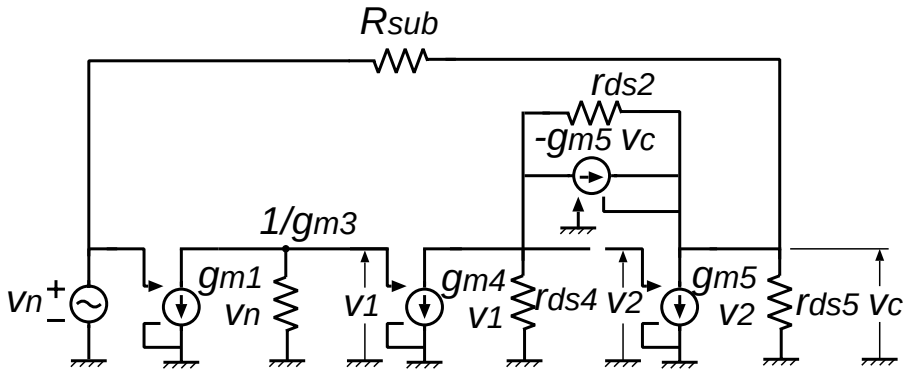

Figure 3.14: Small-signal equivalent circuit

If $g_m r_{ds} \gg 1$, then the transfer function from v_n to v_c will be approximately

$$\frac{v_c}{v_n} \approx -\frac{g_{m1}g_{m4}}{g_{m2}g_{m3}}. \tag{3.21}$$

If the matching between transistors is ideal, then the transfer function from v_n to v_c is

$$\frac{v_c}{v_n} = -1. \tag{3.22}$$

Effects of Mismatch Between Devices

Figure 3.13 shows that M_1 and M_2 play a role of a V-I and an I-V converter respectively, while M_3 and M_4 compose a current mirror. This means that any mismatch between M_1 and M_2 or M_3 and M_4 will degrade the circuit performance. From Eq.(3.21) it is clear that the transfer function is determined by the transconductances of $M_1 \sim M_4$. Therefore mismatches in these transistors will greatly affect the circuit performance.

The mismatch between MOS transistors is mainly caused by the mismatch in their threshold voltage V_{TH} and transconductance parameter K. If the mismatch of V_{TH} is ΔV_{TH} and mismatch of K is ΔK, then the mismatches are known to be given by [77]

$$\Delta V_{TH} = \frac{A_{VT}t_{OX}}{\sqrt{LW}} \tag{3.23}$$

$$\frac{\Delta K}{K} = \frac{A_K}{\sqrt{LW}} \tag{3.24}$$

where L and W are the channel length and channel width of a MOS transistor. For 0.6μm process, typical values of $A_{VT}t_{OX}$ and A_K are 14μm·mV and 10$\sim$20nm respectively.

First, consider the effect of mismatch between M_1 and M_2. From Eq.(3.18), V_C becomes

$$V_C = V_{Sh2} - \sqrt{\frac{K_1}{K_2}}V_{Sh1} + \sqrt{\frac{K_1}{K_2}}V_{TH1} - V_{TH2} - \sqrt{\frac{K_1}{K_2}}V_N. \tag{3.25}$$

Since the terms without V_N will be a DC offset voltage, then the ratio between the change in output voltage and input voltage T_1 is given by

$$T_1 = \frac{\partial V_C}{\partial V_N} = -\sqrt{\frac{K_1}{K_2}}. \tag{3.26}$$

Thus, the output voltage error due to mismatch between M_1 and M_2 can be calculated as

$$\frac{\Delta T_1}{T_1} = \left|\frac{-\sqrt{K_1/K_2} + \sqrt{K_1/K_1}}{\sqrt{K_1/K_1}}\right| \tag{3.27}$$

$$= \left|\frac{K_1 - K_2}{K_2 + \sqrt{K_1K_2}}\right| = \frac{\Delta K}{K}\frac{1}{1+\sqrt{1+\Delta K/K}} \tag{3.28}$$

where $\Delta K = |K_1 - K_2|$. Since $\Delta K/K \ll 1$, then output voltage error due to mismatch between M_1 and M_2 will be given by

$$\frac{\Delta T_1}{T_1} \approx \frac{\Delta K}{2K}. \tag{3.29}$$

Now assume that M_1 and M_2 are perfectly matched and there is mismatch between M_3 and M_4 so that the currents flow through M_1 and M_2 are different. The output current error in a current mirror is given by

$$\frac{\Delta I}{I} = \sqrt{4\left(\frac{\Delta V_{TH}}{V_{GS} - V_{TH}}\right)^2 + \left(\frac{\Delta K}{K}\right)^2}. \tag{3.30}$$

If $K_1 = K_2 = K_N$ and $V_{TH1} = V_{TH2} = V_{THN}$ then the drain currents of M_1 and M_2 will be given by

$$I = K_N(V_{Sh1} + V_S - V_{THN})^2 \tag{3.31}$$

$$I + \Delta I = K_N(V_{Sh2} - V_C - V_{THN})^2. \tag{3.32}$$

Defining $\Delta I/I = \alpha$ and substituting Eq.(3.31) into (3.32) will result in

$$V_C = V_{Sh2} - \sqrt{1+\alpha}V_{Sh1} - (1 - \sqrt{1+\alpha})V_{TN} - \sqrt{1+\alpha}V_N. \tag{3.33}$$

Since only the last term contains the input signal, the ratio of V_C and V_N, T_2 is given by

$$T_2 = \frac{\partial V_C}{\partial V_N} = -\sqrt{1+\alpha}. \tag{3.34}$$

Therefore, the output voltage error due to mismatch in M_3 and M_4 is

$$\frac{\Delta T_2}{T_2} = |1-\sqrt{1+\alpha}| \tag{3.35}$$

$$= \left| \frac{\Delta I}{I} \frac{1}{1+\sqrt{1+\Delta I/I}} \right|. \tag{3.36}$$

If $\Delta I/I \ll 1$ then $\Delta T_2/T_2$ is approximately

$$\frac{\Delta T_2}{T_2} \approx \frac{\Delta I}{2I}. \tag{3.37}$$

Thus the total output voltage error ratio $\Delta T/T$ due to the device mismatch is

$$\frac{\Delta T}{T} = \sqrt{\left(\frac{\Delta T_1}{T_1}\right)^2 + \left(\frac{\Delta T_2}{T_2}\right)^2} \tag{3.38}$$

$$= \frac{1}{2}\sqrt{4\left(\frac{\Delta V_{TH}}{V_{GS}-V_{TH}}\right)^2 + 2\left(\frac{\Delta K}{K}\right)^2}. \tag{3.39}$$

Substituting Eqs.(3.23) and (3.24) into (3.39) will give the total output voltage error as

$$\frac{\Delta T}{T} = \frac{1}{2\sqrt{LW}}\sqrt{4\left(\frac{A_{VT}t_{OX}}{V_{GS}-V_{TH}}\right)^2 + 2A_K^2} \tag{3.40}$$

$$= \frac{10^{-8}}{2\sqrt{LW}}\sqrt{\frac{7.8}{V_{Eff}^2}+8} \tag{3.41}$$

where $V_{Eff} = V_{GS} - V_{TH}$ is the overdrive voltage of M_3.

Frequency Characteristic

A simplified model of the proposed circuit is shown in Fig.3.15. Here the substrate resistances are represented by an equivalent resistance R_{sub} in order to simplify the calculation. $T'(s)$ and Z_O denote the transfer function of the proposed circuit without load impedance (substrate resistance R_{sub}) and

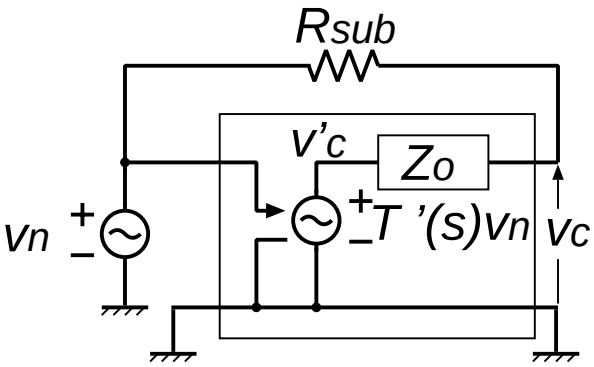

Figure 3.15: Circuit model to calculate the frequency characteristic

output impedance of the proposed circuit respectively. Only gate-source capacitances are considered in the calculation of the frequency characteristic. Small-signal equivalent circuits to find $T'(s)$ and Z_O are shown in Figs.3.16 and 3.17. From Fig.3.16, $T'(s) = v_c'/v_n$ is given by

$$T'(s) = \frac{-g_{m1}g_{m4}(g_{m5}r_{d2} - 1)Z_1Z_2Z_3}{r_{d2} + Z_2 + (1 + g_{m2}r_{d2})(1 + g_{m5}Z_2)Z_3} \tag{3.42}$$

where

$$Z_1 = \frac{1}{g_{m3} + s(C_{gs3} + C_{gs4})} \tag{3.43}$$

$$Z_2 = \frac{r_{d4}}{1 + sC_{gs5}r_{d4}} \tag{3.44}$$

$$Z_3 = \frac{r_{d5}}{1 + sC_{gs5}r_{d2}}. \tag{3.45}$$

If $g_{m2}r_{d2}, g_{m5}r_{d2} \gg 1$ then $T'(s)$ is approximately

$$T'(s) \approx \frac{-g_{m1}g_{m4}g_{m5}r_{d2}Z_1Z_2Z_3}{r_{d2} + Z_2 + g_{m2}r_{d2}(1 + g_{m5}Z_2)Z_3}. \tag{3.46}$$

Substituting Eqs.(3.43),(3.44),(3.45) into (3.46) and assuming $g_{m2} = g_{m1}, g_{m4} = g_{m3}, C_{gs2} = C_{gs1}, C_{gs4} = C_{gs3}$ will result in

$$T'(s) \approx \frac{-g_{m1}g_{m3}g_{m5}}{g_{m3} + s2C_{gs3}} \times \frac{1}{C_{gs1}C_{gs5}s^2 + g_{m1}C_{gs5}s + g_{m1}g_{m5}}. \tag{3.47}$$

The assumption that $g_{m2}r_{d2}, g_{m5}r_{d2} \gg 1$ will also make the output impedance

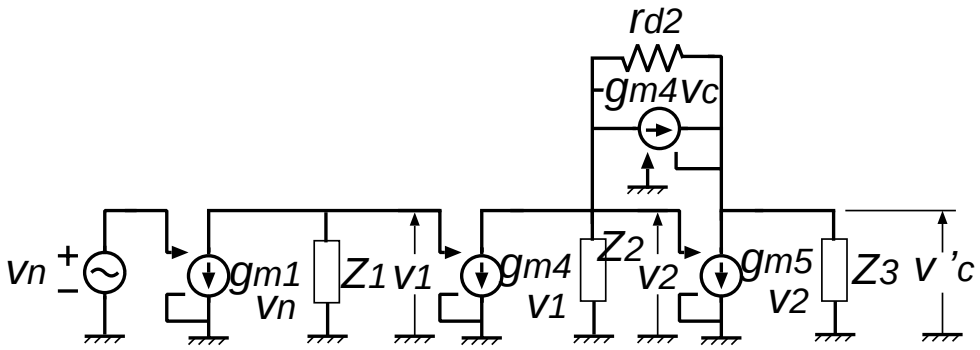

Figure 3.16: Small-signal equivalent circuit to calculate $T'(s)$

Z_O calculated from Fig.3.17 to be

$$Z_O = \frac{v_o}{i_o} = \frac{(r_{d2}+Z_2)Z_3}{r_{d2}+Z_2+(1+g_{m2}r_{d2})(1+g_{m5}Z_2)Z_3} \tag{3.48}$$

$$\approx \frac{(r_{d2}+Z_2)Z_3}{r_{d2}+Z_2+g_{m2}r_{d2}(1+g_{m5}Z_2)Z_3}. \tag{3.49}$$

Substituting Eqs.(3.43),(3.44), and (3.45) into (3.49) will give

$$Z_O \approx \frac{(1+sC_{gs5}r_{d3})r_{d1}+r_{d3}}{r_{d1}r_{d3}(C_{gs1}C_{gs5}s^2+g_{m1}C_{gs5}s+g_{m1}g_{m5})}. \tag{3.50}$$

If $\omega C_{gs5}r_{d1}, \omega C_{gs5}r_{d3} \gg 1$, then Z_O will be given by

$$Z_O \approx \frac{sC_{gs5}}{C_{gs1}C_{gs5}s^2+g_{m1}C_{gs5}s+g_{m1}g_{m5}}. \tag{3.51}$$

From Fig.3.15, the final transfer function $T(s) = v_c/v_n$ is

$$T(s) = \frac{Z_O+R_{sub}T'(s)}{Z_O+R_{sub}} \tag{3.52}$$

$$= \frac{1}{g_{m3}+2C_{gs3}s} \times \frac{2C_{gs3}C_{gs5}s^2+g_{m3}C_{gs5}s-g_{m1}g_{m3}g_{m5}R_{sub}}{R_{Sb}\{C_{gs1}C_{gs5}s^2+(\frac{1}{R_{sub}}+g_{m1})C_{gs5}s+g_{m1}g_{m5}\}}. \tag{3.53}$$

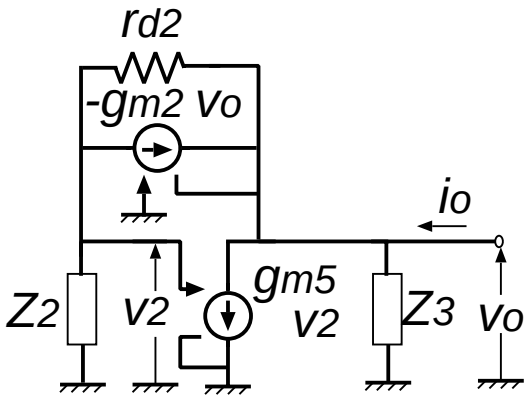

Figure 3.17: Small-signal equivalent circuit to calculate Z_O

Optimization Function

Note that the inverse of Eq.(3.41) seems like a gain of an amplifier. Therefore the evaluation function F can be defined as the product of the *gain* and the *bandwidth*. Thus function F is defined as

$$F = \left|\frac{T}{\Delta T}\right| \omega_p \tag{3.54}$$

$$= \frac{\omega_p}{|\Delta T|} \tag{3.55}$$

where $|T| = 1$ for an ideal inverter and ω_p is the dominant pole of the active shield circuit. In Eq.(3.53) there are three poles and two zeroes. However, the zeroes do not have much influence to the circuit bandwidth. Therefore only the poles are considered here. The poles obtained from Eq.(3.53) are

$$\omega_{p1} = -\frac{g_{m3}}{2C_{gs3}}, \tag{3.56}$$

$$\omega_{p2,3} = -\frac{g_{m1}R_{sub}+1}{2R_{sub}C_{gs1}} \pm \frac{1}{2}\sqrt{\left(\frac{g_{m1}R_{sub}+1}{R_{sub}C_{gs1}}\right)^2 - \frac{4g_{m1}g_{m5}}{C_{gs1}C_{gs5}}}. \tag{3.57}$$

Assume that the bias currents of $M_1 \sim M_4$ are I_1 and bias current of M_5 is I_2. Using $g_m = 2\sqrt{KI}(K = \mu C_{OX}W/2L)$, $C_{gs} = \frac{2}{3}C_{OX}LW$ and $L_i = L(i=1\sim 5)$ will

give

$$\omega_{p1} = -\frac{3}{2}\sqrt{\frac{\mu_p I_1}{2C_{OX}W_3L}}, \tag{3.58}$$

$$\omega_{p2,3} = -\frac{3\sqrt{\frac{2\mu_n C_{OX}W_1}{L}I_1}R_{sub}+1}{2R_{sub}2C_{OX}W_1L} \pm\frac{1}{2}\left(\left(\frac{3\sqrt{\frac{2\mu_n C_{OX}W_1}{L}I_1}R_{sub}+1}{2R_{sub}2C_{OX}W_1L}\right)^2 - \frac{9}{2C_{OX}L}\sqrt{\frac{\mu_n\mu_p I_1 I_2}{W_1W_5}}\right)^{1/2}. \tag{3.59}$$

Note that the first pole is only determined by the parameters of M_3. Furthermore, the change in parameters of M_3 do not affect the other two poles. The typical threshold voltage for 0.6μm process shown in Table 3.4 and the bias settings shown in Table 3.5 are used in the evaluation.

Table 3.4: Device parameters

Name	**Value**
C_{OX}	2.1×10^{-3}F/m^2
μ_n	0.024m^2/V.s
μ_p	0.007m^2/V.s
V_{THN}	0.7V
V_{THP}	0.9V

Table 3.5: Bias settings

Name	**Value**
V_{Eff}	0.5 V
V_{off}	0.05 V

Furthermore, the other parameters are given by

$$\frac{W_3}{W_1} = -\frac{\mu_n}{\mu_p}\left(\frac{V_{GS1}-V_{THN}}{V_{Eff}}\right)^2 \tag{3.60}$$

$$W_5 = \frac{2LI_2}{\mu_p C_{OX}V_{Eff}^2} \tag{3.61}$$

$$I_1 = \frac{\mu_p C_{OX}W_3}{2L}V_{Eff}^2 \tag{3.62}$$

$$I_2 = \frac{V_{off}}{R_{sub}} - I_1. \tag{3.63}$$

As a result, ω_{p1} can be expressed as

$$\omega_{p1} = -\frac{3}{4}\frac{\mu_p V_{Eff}}{L^2} \tag{3.64}$$

which will be constant for a given V_{Eff} and device length L. For the values given above and $L = 0.6\mu$m, $\omega_{p1} = 7.3\times10^9$rad/s. From Eq.(3.60), $V_{GS1} = 1$V will result in $W_3 \approx 1.2W_1$. Next, assume that the equivalent substrate resistance $R_{sub} = 50\Omega$

(actually it depends on the layout) and from Eq.(3.59) the last two poles will be given by

$$\begin{aligned}\omega_{p2,3} &= \frac{1}{L^2W}\{-7.1(L+7.5\times10^{-4}W) \\ &\pm \sqrt{\{7.1(L+7.5\times10^{-4}W)\}^2-2.2\times10^{-4}W^2}\}\end{aligned} \tag{3.65}$$

where $W = W_1$. Now all poles are expressed by device parameters L and W. For $L = 0.6\mu$m, the position of each pole versus W is shown in Fig.3.18. This figure shows that only the consideration of ω_{p2} is necessary since it is the lowest pole.

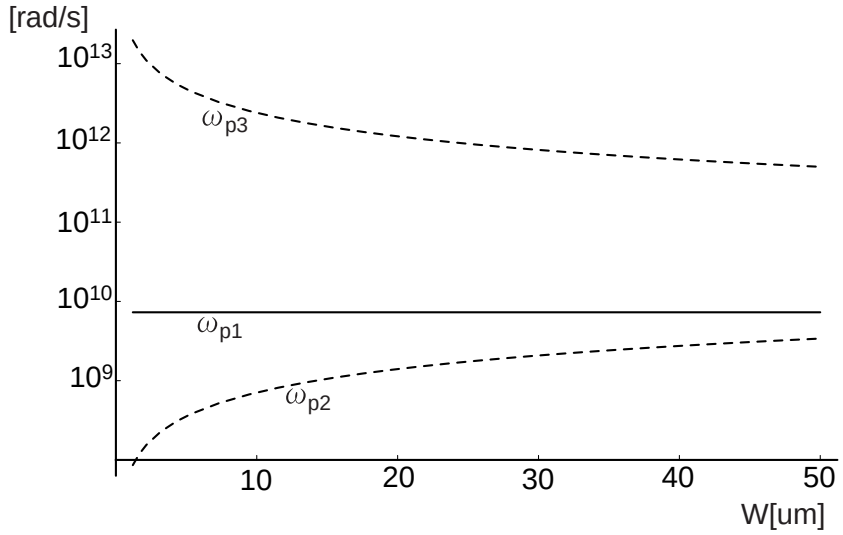

Figure 3.18: Pole position versus W.

From Eqs.(3.41) and (3.65) an evaluation function F is obtained. The plot of this evaluation function is shown in Fig.3.19. It shows that the evaluation function gives better results for bigger W (channel width) values. However, from Eqs.(3.61)$\sim$(3.63), the channel width of M_5, W_5 will be given by

$$W_5 = \frac{2L}{\mu_p C_{OX} V_{Eff}^2}\frac{V_{off}}{R_{sub}} - W_3 \tag{3.66}$$

$$= \frac{2L}{\mu_p C_{OX} V_{Eff}^2}\frac{V_{off}}{R_{sub}} - 1.2W \tag{3.67}$$

and thus increasing W will reduce W_5. As a result, a zero or negative values of W_5 will be obtained from the equation for a quite big W although it is not realistic. The possible value of W will be given by

$$W < 2.27\times10^4\frac{L}{R_{sub}}. \tag{3.68}$$

Furthermore, the equivalent substrate resistance R_{sub} also affects the optimization result. From Eq.(3.63), I_2 becomes smaller when R_{sub} increases and therefore W_5 will decrease.

Figure 3.20 shows the noise level at node **g** with various W when $R_{sub} = 50\Omega$. Here a greater value of W gives a better noise suppression performance. This result is predictable from the analysis result shown in Fig.3.19. The result of the optimization says that a greater channel width W will give a better performance. However it should be noted that there is a limitation on the size of the channel width. In addition, since increasing W will also increase the bias current then the power consumption should also be considered.

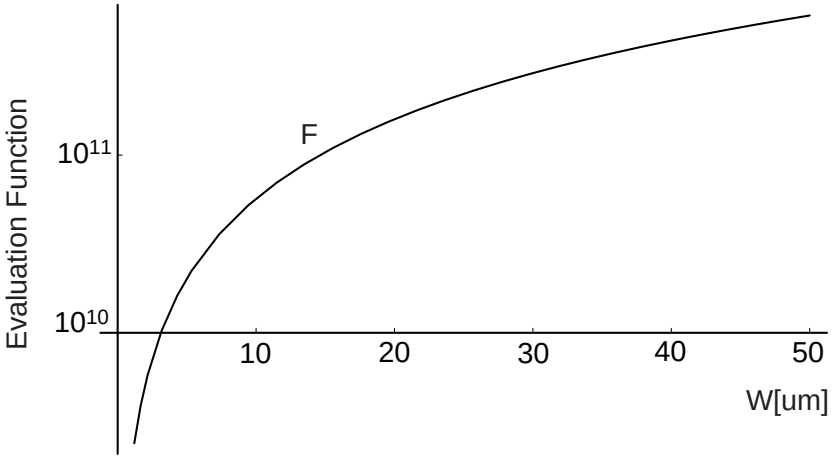

Figure 3.19: Evaluation function versus W.

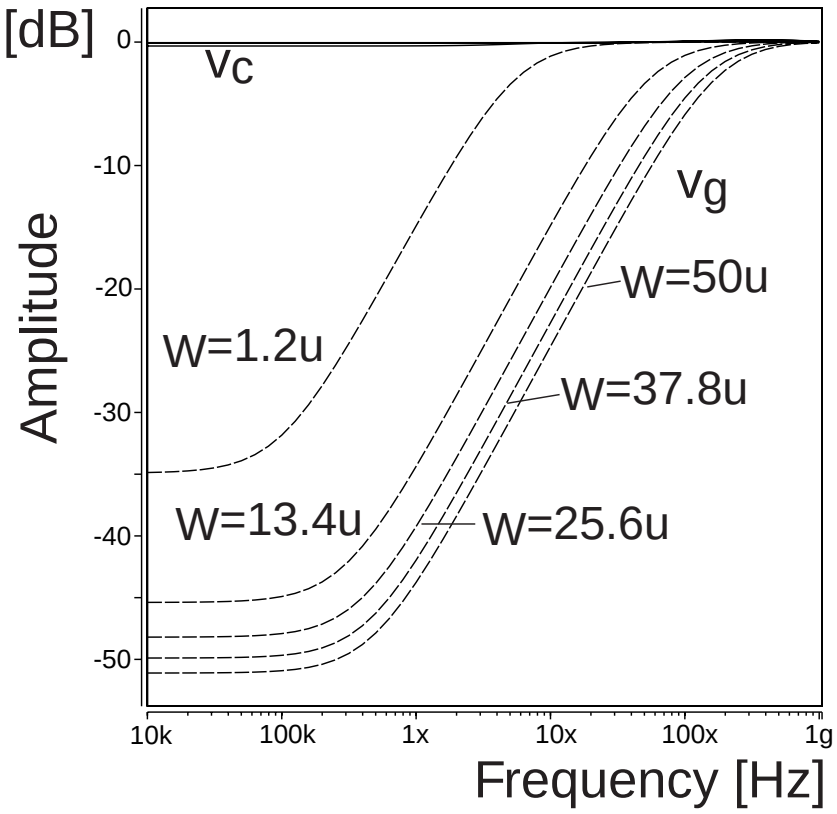

Figure 3.20: Frequency characteristic with various W ($R_{sub} = 50\Omega$)

3.3 Simulation Results

The circuit shown in Fig.3.13 is simulated using a circuit simulator HSpice and level 2 device parameters for 0.6μm CMOS process. MOS transistors aspect ratios, voltage sources, and the other parameters values are shown in Tables 3.6, 3.7, and 3.8.

Table 3.6: MOS transistors aspect ratio

Transistors	**W/L**
$M_{1,2}$	15μm/ 0.6μm
$M_{3,4}$	30μm/ 0.6μm
M_5	200μm/0.6μm

Table 3.7: Voltage sources

Name	Value
V_{DD}	3 V
V_{Sh1}	0.8 V
V_{off}	50 mV

Table 3.8: Substrate resistors

Name	Value[Ω]
R_1	100
R_2	50
R_3	30

The simulation will be performed to confirm the basic operation of the improved active shield circuit. Therefore low level MOS device parameters are used instead of more complicated ones. The large-signal, small-signal and transient characteristic of the active shield circuit will be simulated and the results then will be compared to the measurement results in section 3.4.

3.3.1 DC Characteristics

The DC characteristics is simulated by varying the input voltage V_N from -30mV to 30mV. The result is shown in Fig.3.21. Since the offset voltage is set to 50mV,

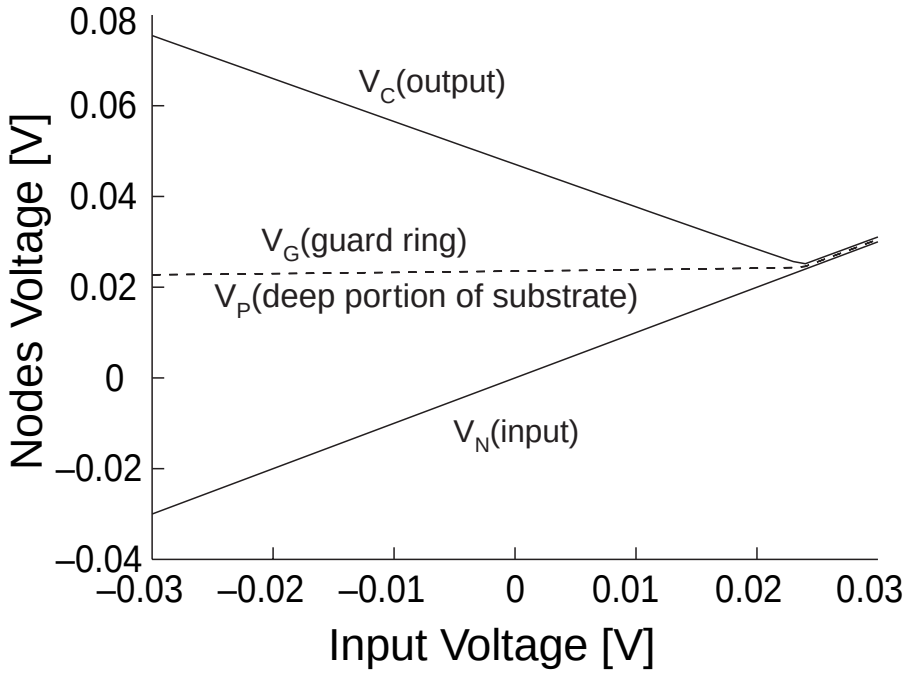

Figure 3.21: DC characteristics simulation results.

according to section 3.2 the circuit is expected to work for input signal from -25mV to 25mV. Figure 3.21 shows that when V_N increases the output node voltage decreases. This holds for V_N up to approximately 24mV. V_G and V_P are almost constant between this input range. When V_N increases further, V_C, V_G, and V_P also increase. This means the circuit cannot handle the input signal anymore.

This simulation result confirms the large signal analysis in section 3.2.2. It also shows that the proposed DC offset technique enables the implementation of a fully integrated active shield circuit.

3.3.2 Frequency Characteristics

The frequency characteristic is simulated by adding a small signal to node **n**. The result is shown in Fig.3.22. The amplitude of v_p/v_n shows the noise amplitude at node **p** compared to the original noise while v_c/v_n shows the gain of the active shield circuit. Here a noise suppression level of about 30dB is obtained at frequencies up to 1MHz. Figure 3.22 shows that although the gain of the active shield circuit is not greatly changed at frequencies up to 10MHz, the noise level starts to increase when the frequency goes higher than 1MHz. This is due to the delay of the cancellation signal. Note that the phase of the output signal of the active shield circuit starts to decrease from 180° at frequencies higher than 1MHz. This delay makes the noise remain although the cancellation signal has the same amplitude to the noise.

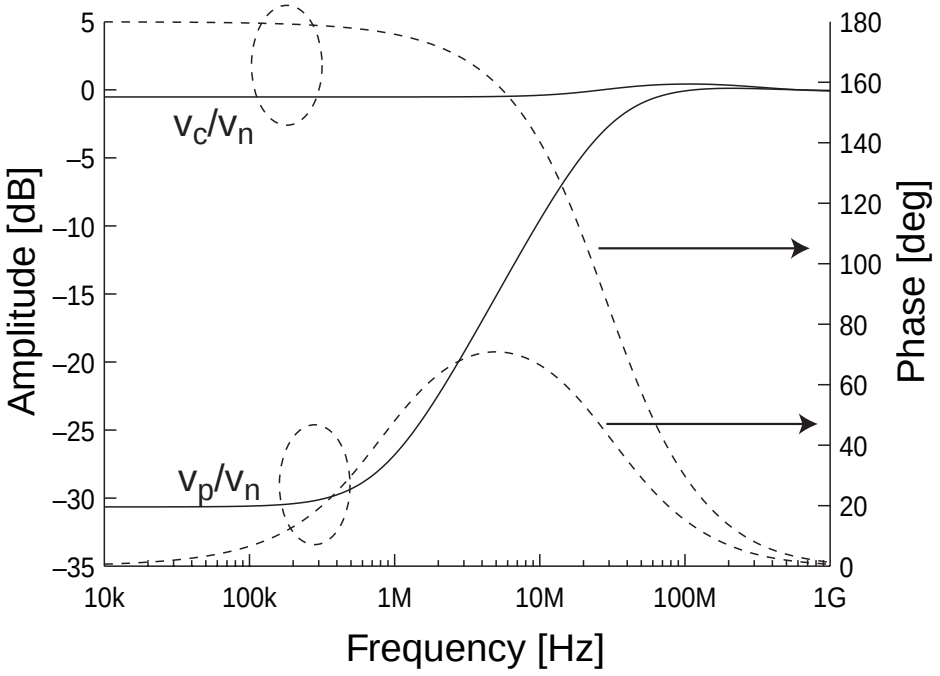

Figure 3.22: Frequency characteristics simulation results.

3.3.3 Transient Characteristics

The transient characteristics are simulated using sine waves with various frequencies and amplitudes. First, a 20mV$_{p\text{-}p}$ and 100kHz sine wave is added to node **n**. The result is shown in Fig.3.23. Here an inverted sine wave relative to the input appears at node **c** and the potential of node **p** only varies in small amounts.

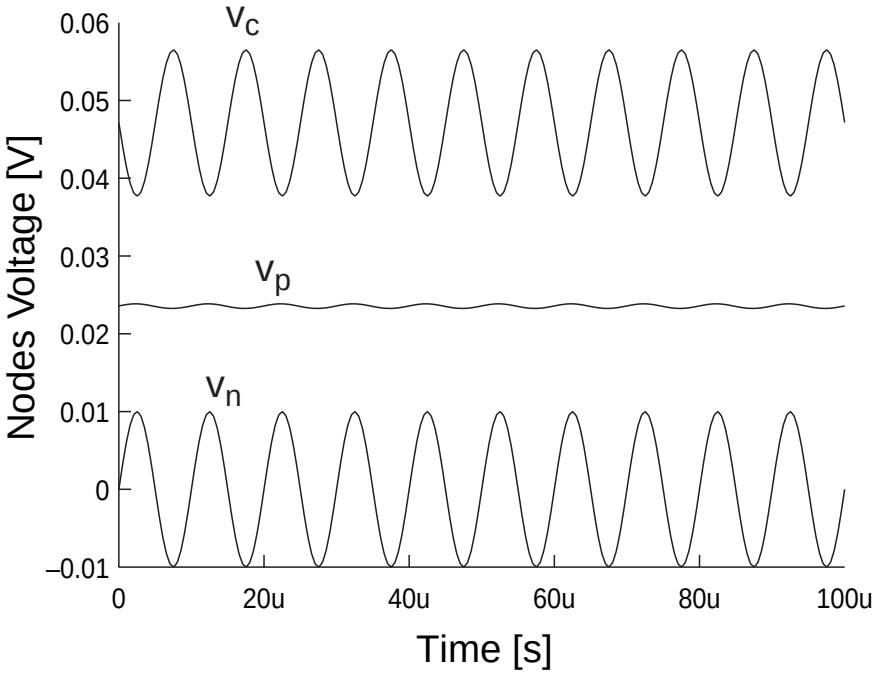

Figure 3.23: Transient characteristics simulation results (20mV$_{p\text{-}p}$@100kHz).

Next, a 20mV$_{p\text{-}p}$ and 10MHz sine wave is added to node **n**. The result is shown in Fig.3.24. Here a delay can be seen at the output signal v_c. Therefore, the cancellation effect is reduced and the noise signal remains large at node **p**. This can also be confirmed from the frequency characteristic simulation result in Fig.3.22. A noise suppression level of about 30dB is obtained at frequencies up to 1MHz. However, the effect is weakened as the frequency increases. The noise suppression level at 10MHz is only about 10dB.

In order to find the transient characteristic for a large amplitude input signal, a 60mV$_{p\text{-}p}$ and 100kHz sine wave is added to node **n**. The result is shown in Fig.3.25. In this case, since the input signal excesses the allowable range, there are parts of the input signal that the circuit cannot handle. As a result, input signal still appears at node **p**.

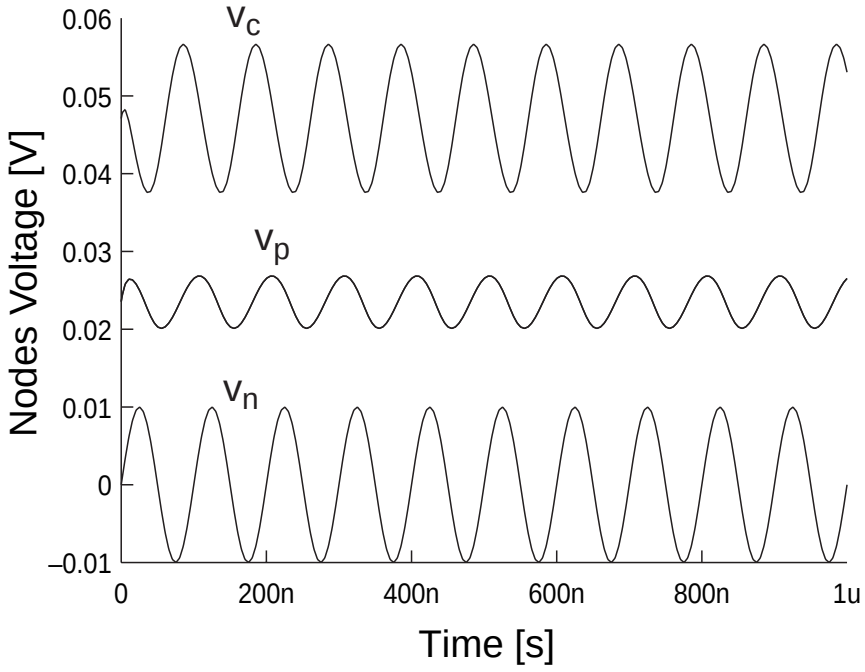

Figure 3.24: Transient characteristics simulation results ($20mV_{p\text{-}p}$@10MHz).

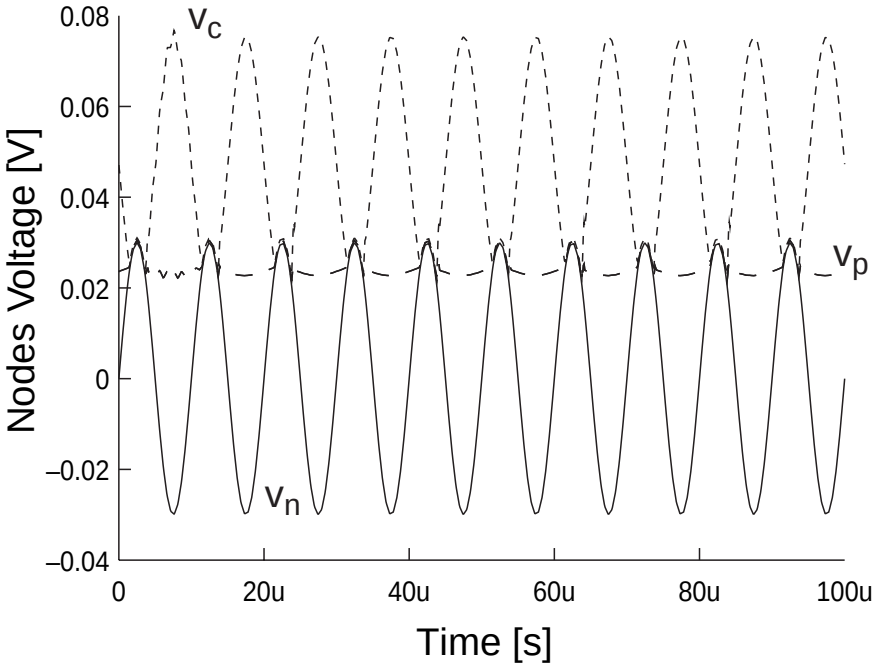

Figure 3.25: Transient characteristics simulation results ($60mV_{p\text{-}p}$@100kHz).

3.4 Measurement Results

This section will show the measurement results to confirm the basic operation of the active shield circuit and the validity of the proposed implementation method using the DC offset technique. The experimental chip is fabricated on 1.2μm standard CMOS process with p-type substrate. Figure 3.26 shows the layout of a guard ring, diffusion bands and measurement pins on the chip. The applied power supply is 5V and the offset voltage V_{off} is set to 50mV.

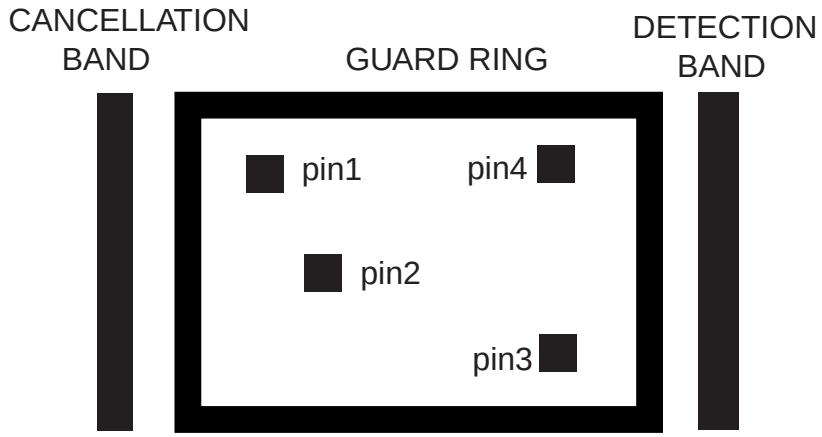

Figure 3.26: Layout of guard ring, bands, and measurement pins.

3.4.1 DC Characteristics

Figure 3.27 shows the characteristic of the circuit for DC operation. The output voltage decreases when the input voltage increases. On the other hand, the guard ring voltage only varies in a small amount even if the input voltage reaches 30mV. Guard ring voltage starts to increase faster when the input voltage goes over 30mV. Figure 3.28 shows measurement results of voltages from four measurement pins inside the guard ring.

Figure 3.27 gives an abstract about how the active shield circuit works for large signal inputs. Since the reference voltage is 50mV, the initial voltage levels of the output node and the guard ring should be 50mV and 25mV (theoretical values). The measurement result shows that the initial voltage levels of the output node and the guard ring are approximately 50mV and 23mV. Since the substrate resistances are biased by the drain currents of M_3 and M_9, the bias point of the output node will be strongly determined by the amount of current which M_3 and M_9 can supply. Therefore it could be smaller than the offset voltage V_{off} when the current supply is insufficient. The other factor which determines this bias point is the variation of substrate resistances. Since the actual substrate resistances are not exactly symmetrical, the bias point of the guard ring may vary between a few millivolts from the theoretical value.

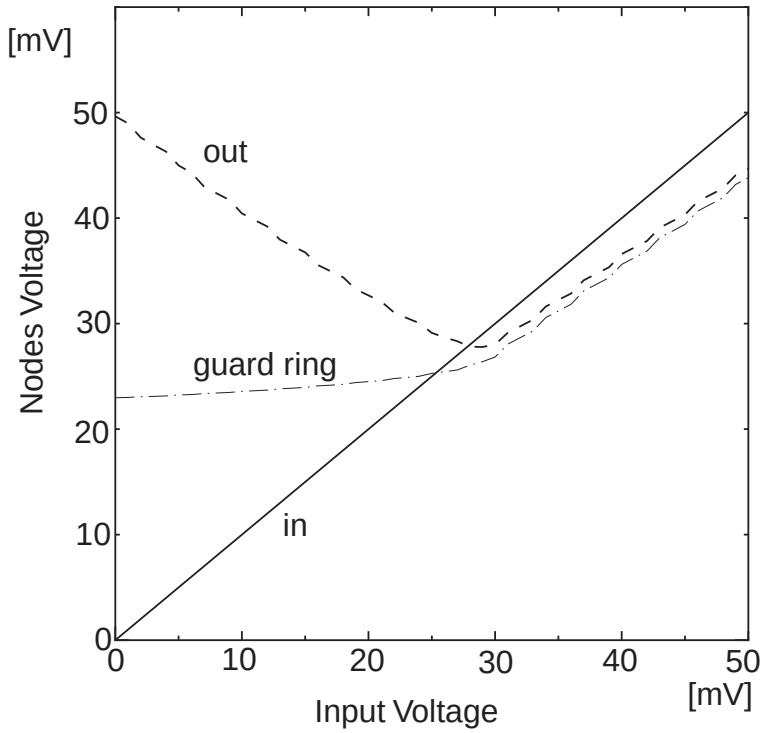

Figure 3.27: Measured DC operation of proposed circuit.

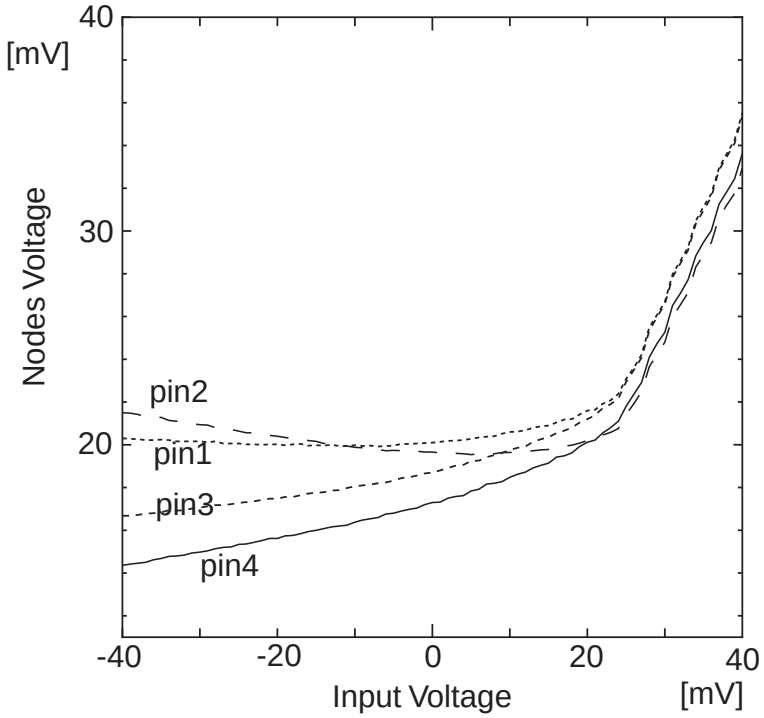

Figure 3.28: Measured voltage of measurement pins.

3.4.2 Frequency Characteristics

Next, frequency characteristics are measured. The result is shown in Fig.3.29. The reference means the signal amplitude measured at the measurement point when the active guard band circuit is not activated. The actual reference amplitude is not at 0dB, however it is set to 0dB in order to make a comparison between simulation and measurement results.

The solid lines show the amplitudes in decibel while the dashed lines show the phases. It can be observed that the measured and simulated frequency characteristics are quite similar. Figure 3.29 shows that the actual circuit has a lower cutoff frequency while the noise suppression level is better than the simulation result. This difference may be caused by the precision of the device parameter used in the simulation.

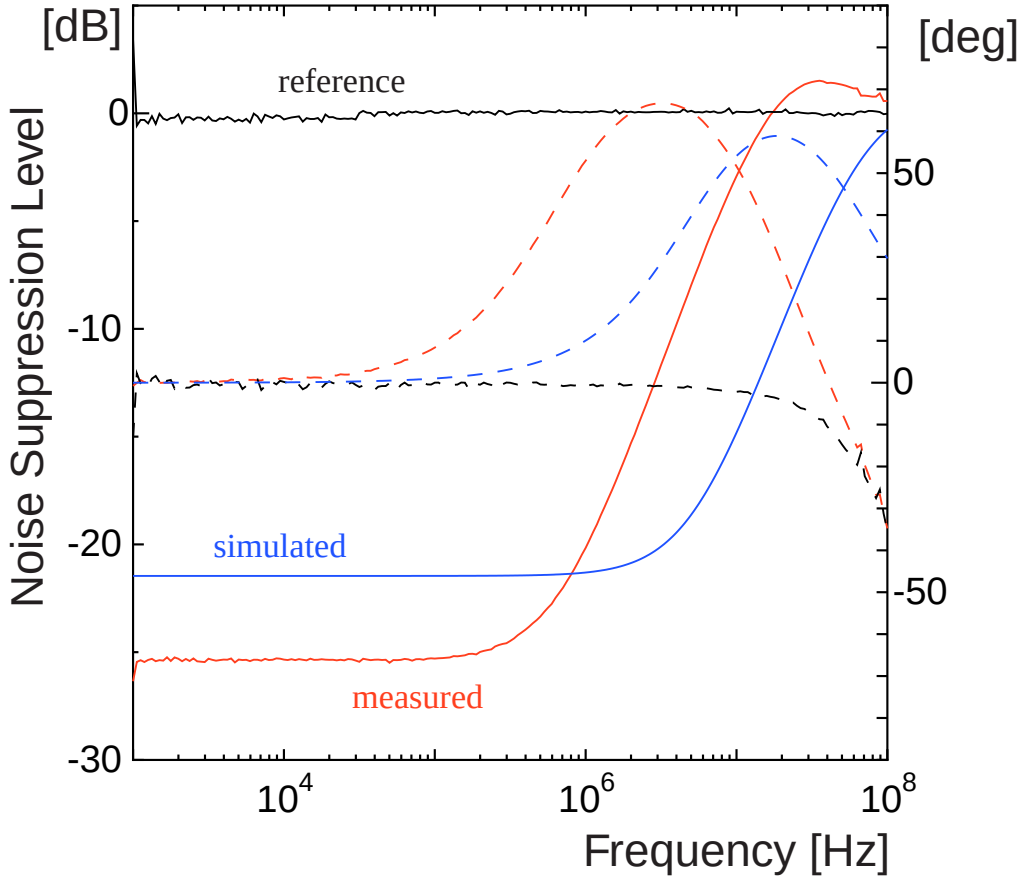

Figure 3.29: Frequency characteristics measurement results.

3.4.3 Transient Characteristics

A few transient characteristics are measured by using a $10mV_{p\text{-}p}$ and 10kHz sine wave as an input signal. The offset voltage V_{off} is 30mV in this case. Figure 3.30 shows the transient characteristic measurement result at the output node (cancellation band). Here, an inverted sine wave relative to the input can be observed at the output node. Figure 3.31 shows the transient characteristic measurement result at a measurement pin inside the guard ring using the same input signal. Note that the voltage fluctuation at the measurement point is relatively small.

Figure 3.32 shows the transient characteristic measurement result of the same pin with an input signal amplitude of $17.5mV_{p-p}$. Since the input signal amplitude is bigger than the allowed maximum input range, the voltage fluctuation at the measurement pin should increase. The increase in voltage fluctuation at the measurement pin can be observed in Fig.3.32.

At last, a $20mV_{p\text{-}p}$ sine wave at 10MHz is applied to the sense band. The offset voltage V_{off} is set to 50mV for this case. The measurement result is shown in Fig.3.33. Here the residual signal observed at the measurement pin is still large. The frequency characteristic measurement result in Fig.3.29 will explain this result.

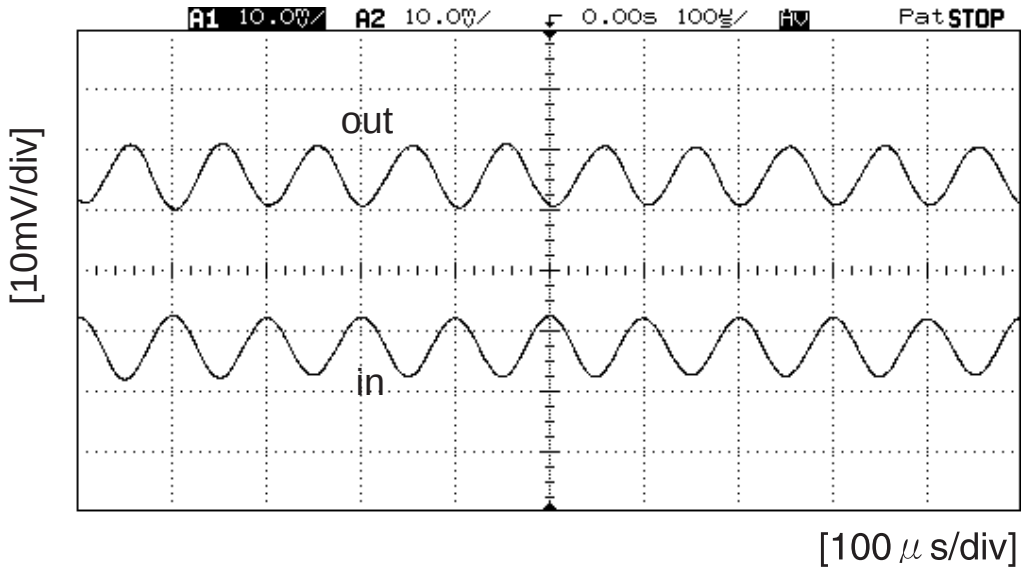

Figure 3.30: Measured transient characteristic at output node a($10mV_{p\text{-}p}$ @ 10kHz).

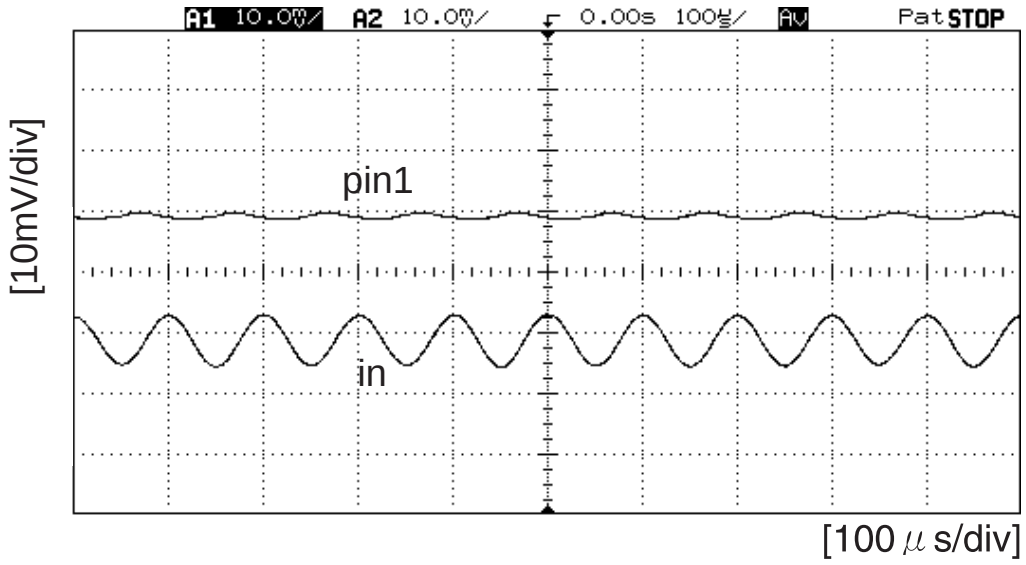

Figure 3.31: Measured transient characteristic at pin1 ($10mV_{p\text{-}p}$ @ 10kHz).

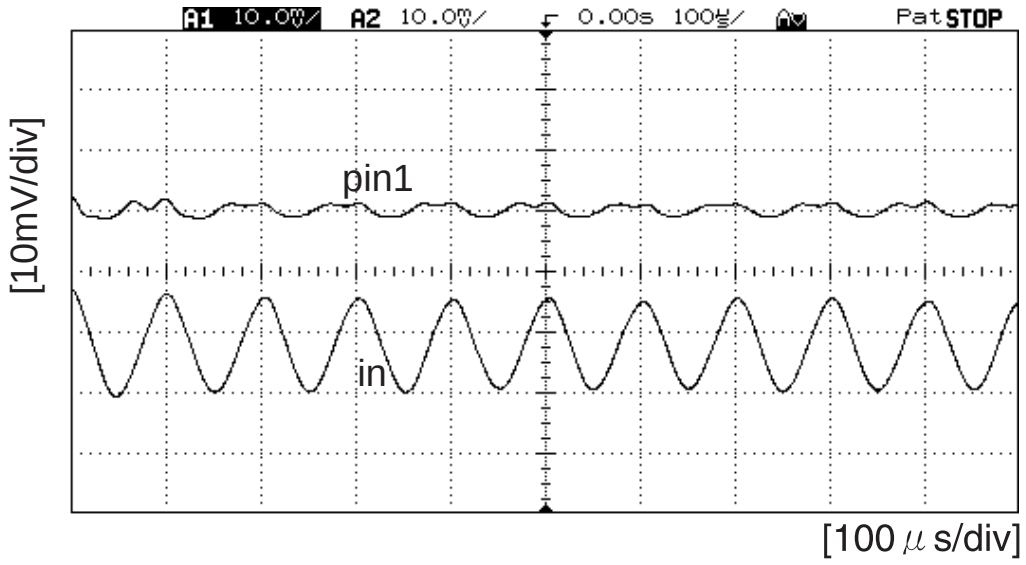

Figure 3.32: Measured transient characteristic at pin1 ($17.5mV_{p\text{-}p}$ @ 10kHz).

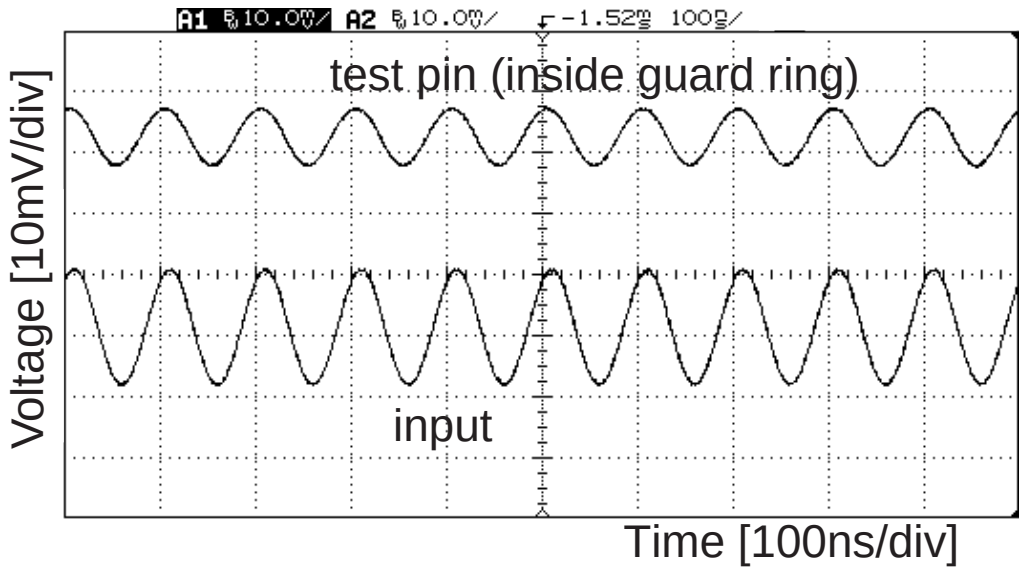

Figure 3.33: Measured transient characteristic at pin1 ($20mV_{p\text{-}p}$ @ 10MHz).

3.5 Discussions

3.5.1 Comparison Between Feedback and Feedforward Techniques

It has been introduced that there are two approaches of implementing active shield circuit. They are the feedback and the feedforward approaches. In this section, the comparison between both techniques will be discussed in order to examine the proper structure for an active shield circuit. First, consider a simple feedback structure used in the conventional active shield circuit as is shown in Fig.3.34.

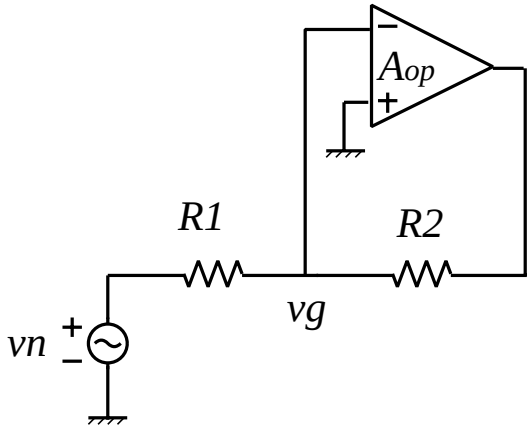

Figure 3.34: A simple feedback structure.

Assume that the gain of the operational amplifier A_{op} is given by

$$A_{op} = \frac{A_{op0}}{1 + s/\omega_{op}} \tag{3.69}$$

where A_{op0} and ω_{op} are the DC gain and the cutoff frequency of the operational amplifier respectively. Here the transfer function from v_n to v_g will be given as

$$\frac{v_g}{v_n} = \frac{1}{1 + (1 + A_{op})\frac{R_1}{R_2}} \tag{3.70}$$

$$= \frac{1 + s/\omega_{op}}{(1 + \frac{R_1}{R_2} + A_{op0}) + (1 + \frac{R_1}{R_2})s/\omega_{op}}. \tag{3.71}$$

The frequency characteristic estimation of Eq.(3.71) is shown in Fig.3.35. Here the cutoff frequency of the operational amplifier will determine the effective noise suppression bandwidth. For a given specification of noise level NL and noise

suppression bandwidth ω_N, the requirement on the operational amplifier will be given by

$$A_{op0} = \frac{1}{NL} - \left(1 + \frac{R_1}{R_2}\right) \tag{3.72}$$

$$\omega_{op} = \omega_N. \tag{3.73}$$

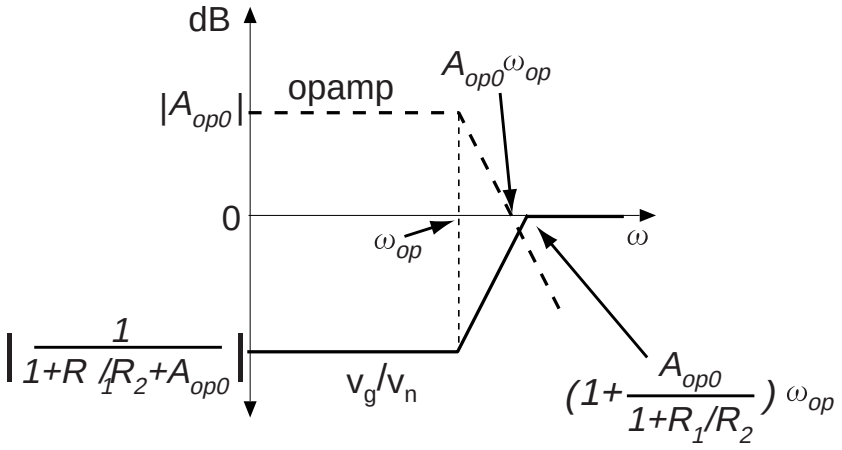

Figure 3.35: Estimated frequency characteristic of a feedback structure.

Commonly, the DC gain and the cutoff frequency of an operational amplifier are affected by manufacturing tolerance. Let the maximum manufacturing tolerance is given by $\alpha(0 \leq \alpha \leq 1)$ and thus the DC gain A_{op0} and the cutoff frequency ω_{op} of the operational amplifier in the worst case will be given by $A_{op0}(1-\alpha)$ and $\omega_{op}(1-\alpha)$ respectively. As a result, Eqs.(3.72) and (3.73) can be rewritten as

$$A_{op0} = \frac{1}{NL(1-\alpha)} - \left(1 + \frac{R_1}{R_2}\right)\frac{1}{1-\alpha} \tag{3.74}$$

$$\omega_{op} = \frac{\omega_N}{1-\alpha}. \tag{3.75}$$

Next, consider the simple feedforward structure shown in Fig.3.36. If the gain of the inverter A_{inv} is given by

$$A_{inv} = \frac{A_{inv0}}{1 + s/\omega_{inv}}, \tag{3.76}$$

then the transfer function from v_n to v_g will be obtained as

$$\frac{v_g}{v_n} = \frac{R_2 - A_{inv}R_1}{R_1 + R_2} \tag{3.77}$$

$$= \frac{R_2 - A_{inv0}R_1 + R_2 s/\omega_{inv}}{(R_1 + R_2)(1 + s/\omega_{inv})}. \tag{3.78}$$

$$= \frac{\frac{R_2}{R_1} - A_{inv0} + \frac{R_2}{R_1} s/\omega_{inv}}{(1 + \frac{R_2}{R_1})(1 + s/\omega_{inv})} \tag{3.79}$$

$$= \frac{A_{opt} - A_{inv0} + A_{opt} s/\omega_{inv}}{(1 + A_{opt})(1 + s/\omega_{inv})} \tag{3.80}$$

$$= \frac{\delta + A_{opt} s/\omega_{inv}}{(1 + A_{opt})(1 + s/\omega_{inv})} \tag{3.81}$$

where $A_{opt} = R_2/R_1$ is the optimum gain value to make $v_g = 0$ and δ is the gain error of the inverter respectively. The estimated frequency response of the

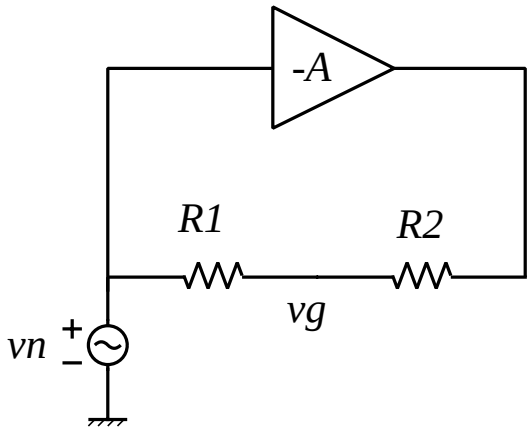

Figure 3.36: A simple feedforward structure.

feedforward structure is shown in Fig.3.37. Here the noise suppression bandwidth not only determined by the cutoff frequency of the inverter ω_{inv}, but also by the ratio of inverter gain error δ to the optimum gain value A_{opt}. Recall the term of noise level NL and noise suppression bandwidth ω_N, and the requirement on the inverter will be given by

$$\delta = NL(1 + A_{opt}) \tag{3.82}$$

$$\omega_{inv} = \frac{A_{opt}}{\delta}\omega_N. \tag{3.83}$$

If the inverter is implemented by the circuit in Fig.3.11, then the gain accuracy will be determined by the mismatch between devices. On the other hand, the

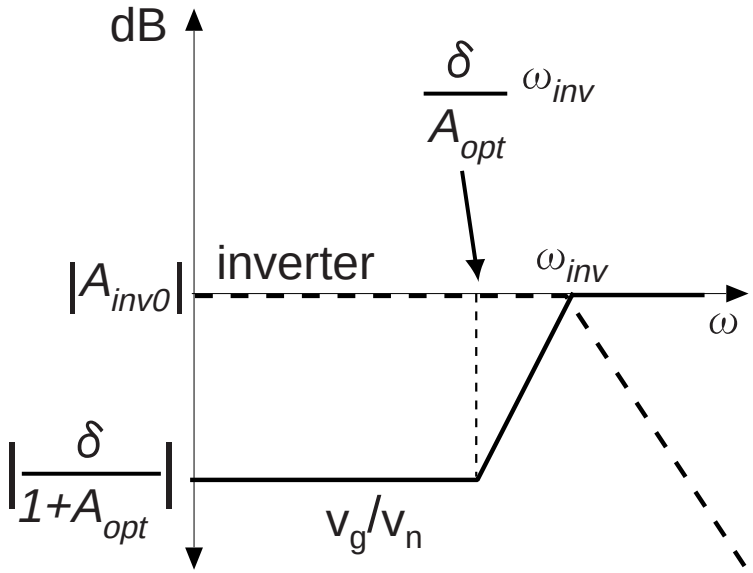

Figure 3.37: Estimated frequency characteristic of a feedforward structure.

frequency characteristic depends on the manufacturing tolerance. Again assume that the manufacturing tolerance is given by α, thus the inverter's cutoff frequency at the worst case is given by $\omega_{inv}(1-\alpha)$. As a result, Eq.(3.83) will become

$$\omega_{inv} = \frac{1}{1-\alpha}\frac{A_{opt}}{\delta}\omega_N. \tag{3.84}$$

In addition, the inverter's gain error will be equal to the total device mismatch. For example, consider the specification in Tab.3.5.1 and assume that $R_1 = R_2$. From Eqs.(3.74), (3.75), (3.82) and (3.84), the operational amplifier's DC gain

Table 3.9: System specification example.

Parameter	**Value**
Noise level	0.1(-20dB)
Noise bandwidth	100MHz
Manufacturing tolerance	±20%
(total)	(40%)

A_{op0} and cutoff frequency ω_{op} , the inverter's gain error δ and cutoff frequency

ω_{inv} are

$$A_{op0} = 13.34\ (\approx 22.5\text{dB}) \tag{3.85}$$
$$\omega_{op} = 167\text{MHz} \tag{3.86}$$
$$\delta = 20\% \tag{3.87}$$
$$\omega_{inv} = 834\text{MHz}. \tag{3.88}$$

In the case of feedback structure, an operational amplifier with a gain-bandwidth product of about 2.2GHz is required to fulfill the specification. On the other hand, an inverter with cutoff frequency of 834MHz and mismatch tolerance of 20% is sufficient to achieve the same performance. These results show that the speed requirement of the feedforward structure is easier than the feedback one. The required noise suppression performance then will determine the allowable mismatch or the gain error of the inverter. In other words, the device mismatch will limit the noise suppression level. In the contrary, the noise level on the feedback structure is determined by the gain of the operational amplifier. The higher the gain the smaller the noise level will be. However the feedback structure suffers from speed requirement that will limit the noise suppression bandwidth.

3.5.2 Circuit Placement

Since the active shield circuit is also placed on the same chip, it is important to investigate the effect of substrate noise on the performance of the circuit. Again consider the active shield circuit in Fig.3.13. If the circuit is implemented on a double-well p-type substrate, then the digital noise will appear on the bulk of the NMOS transistors as is shown in Fig.3.38. Here the output voltage V_{OUT} will be given by

$$V_{OUT} = V_{Sh1} - V_{Sh2} - V_{IN} + V_{TH1} - V_{TH2}. \tag{3.89}$$

where $V_{THi}(i = 1,2)$ is the threshold voltage of the NMOS transistors. The threshold voltage V_{TH} of a MOS transistor with consideration of the body effect can be written as

$$V_{TH} = V_{TH0} + \gamma(\sqrt{V_{SB} + |2\phi_F|} - \sqrt{|2\phi_F|}) \tag{3.90}$$

where V_{SB}, V_{TH0}, ϕ_F are the source-to-substrate voltage, the threshold voltage when $V_{SB} = 0$, the electrostatic potential of p-type substrate respectively, and γ is given by

$$\gamma = \frac{\sqrt{2qN_A\epsilon_{si}}}{C_{OX}}. \tag{3.91}$$

Here N_A, ϵ_{si}, and C_{OX} are the substrate doping, the dielectric constant of silicon and the channel capacitance per unit area respectively. As a result, if the substrate

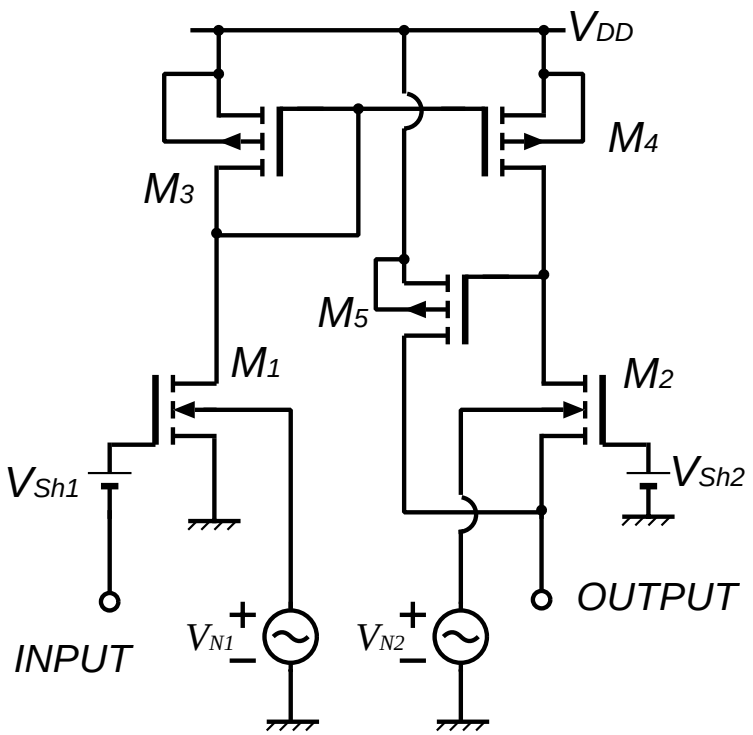

Figure 3.38: Considering the effect of substrate noise.

noise V_{N1} and V_{N2} are correlative, the last two terms in Eq.(3.89) will be

$$V_{TH1} - V_{TH2} = \gamma(\sqrt{V_{N1} + |2\phi_F|} - \sqrt{V_{N2} + |2\phi_F|}) \quad (3.92)$$

$$= \gamma\left(\frac{V_{N1} - V_{N2}}{\sqrt{V_{N1} + |2\phi_F|} + \sqrt{V_{N2} + |2\phi_F|}}\right). \quad (3.93)$$

Here, when $V_{N1} = V_{N2}$, the substrate noise will not appear at the output of the active shield circuit. As a result, the active shield circuit can be placed outside the guard ring without suffering from the bulk fluctuation caused by the digital substrate noise.

3.6 Conclusions

The necessity to use external elements is the main drawback in earlier active shield circuits. The use of DC offset technique is proposed to enable the implementation of the overall active shield circuit on a chip without any external elements. Simulation results show the validity of the proposed circuit and noise suppression of 30dB is achieved.

The measurement results of the active shield circuit show that the DC offset technique is applicable and the circuit is successfully implemented on the chip without any external components. It also can be confirmed that the proposed circuit characteristics are consistent with the simulation results. Measurement results show that the active shield circuit gives noise suppression performance of 25B while the simulation results only give 20dB. In addition, the measured frequency characteristic is worse than the simulated one. These results will occur when the bias current in the active shield circuit is reduced. Thus the precision of the model parameters used in the simulation can be considered as the cause.

The implementation of an active shield circuit using feedback and feedforward structures are examined too. As a result, a feedback structure can provide a high noise suppression performance while it will be a hard task to improve the speed of the active shield circuit. On the other hand, the feedforward structure promises an easier speed improvement while the noise suppression performance will depend on the matching between devices. Furthermore, the proposed active shield circuit uses a circuit structure which is less sensitive to the substrate noise and thus it does not need any particular protection to keep the noise suppression performance. As a result, it can be placed outside the guard ring.

Chapter 4

Design Methodology Using Average Noise Evaluation

Figure 4.1 shows the inverter-based active shield circuit introduced in section 3.2. This circuit assumes that the digital noise is injected exactly at the sense node and the area inside the guard ring is zero. The gain of the amplifier is set to -1 and since the resistances are symmetrical, the transfer function from v_n to v_p becomes zero. Unfortunately, in the actual mixed-signal integrated circuits the area of analog circuits inside the guard ring is not zero and digital noise appears at arbitrary positions instead of the sense node. When these considerations are taken into account, it is hard to say that the gain of -1 is a reasonable value.

When the area inside the guard ring is expanded to a nonzero value, it will be found that the active shield circuit will only give a proper noise suppression performance on a relatively narrow area. The fact that the noise source position is arbitrary makes the assumption of the symmetrical layout improper.

4.1 Evaluation Method

Figure 4.2 shows the active shield circuit to be optimized. The guard ring is connected to the ground and the amplifier gain is given by A instead of a fixed value of -1. The noise source is represented by a current noise source. Since the purpose of the active shield circuit is to make the transfer function from i_n to v_p becomes zero, then solving $v_p/i_n = 0$ for gain A will give

$$A = -\frac{(R_3 + R_a)R_b}{R_3 R_c} \tag{4.1}$$

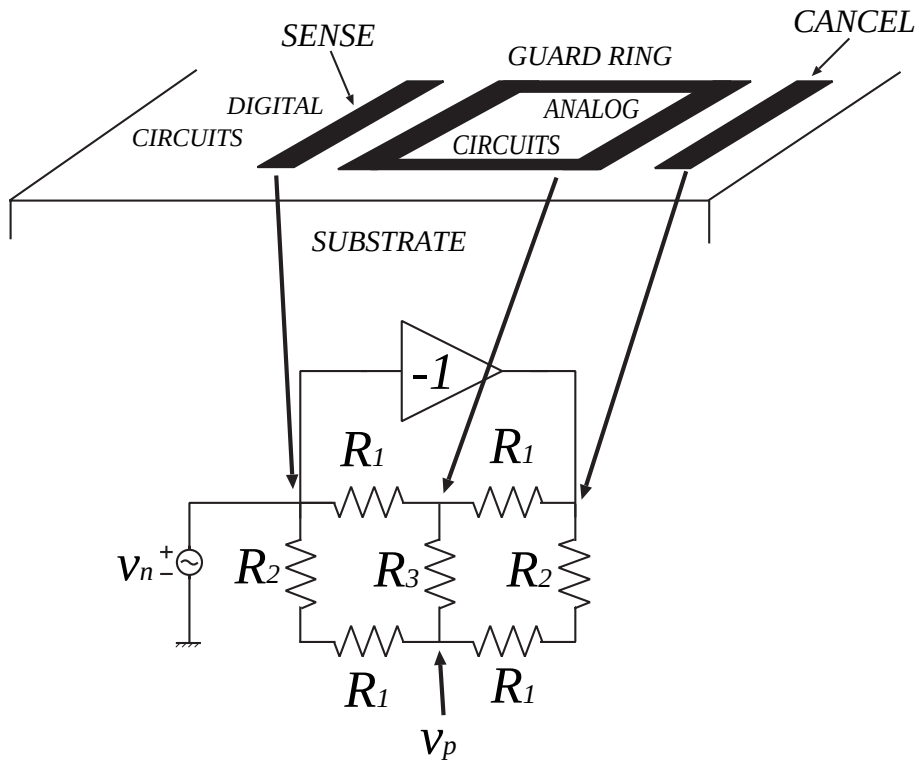

Figure 4.1: Inverter based active shield circuit.

where

$$R_a = \frac{R_2 R_9}{R_2 + R_8 + R_d} \tag{4.2}$$

$$R_b = \frac{(R_6 + R_{13})(R_5 + R_{12}) + R_5 R_{12}}{R_{12}} \tag{4.3}$$

$$R_c = \frac{(R_e + R_3)(R_4 + R_{10}) + R_4 R_{10}}{R_{10}} \tag{4.4}$$

$$R_d = R_2 + \frac{R_8(2R_1 + R_7)}{2R_1 + R_7 + R_8} \tag{4.5}$$

$$R_e = \frac{R_9 R_d}{R_2 + R_9 + R_d}. \tag{4.6}$$

Equation 4.1 shows that the optimum gain A depends on the values of R_4 and R_5 which are determined by the position of the observation point inside the guard ring. In other words, when A is fixed for a given values of R_4 and R_5, a sufficient noise suppression performance will only be obtained in a narrow area around the position represented by those resistances.

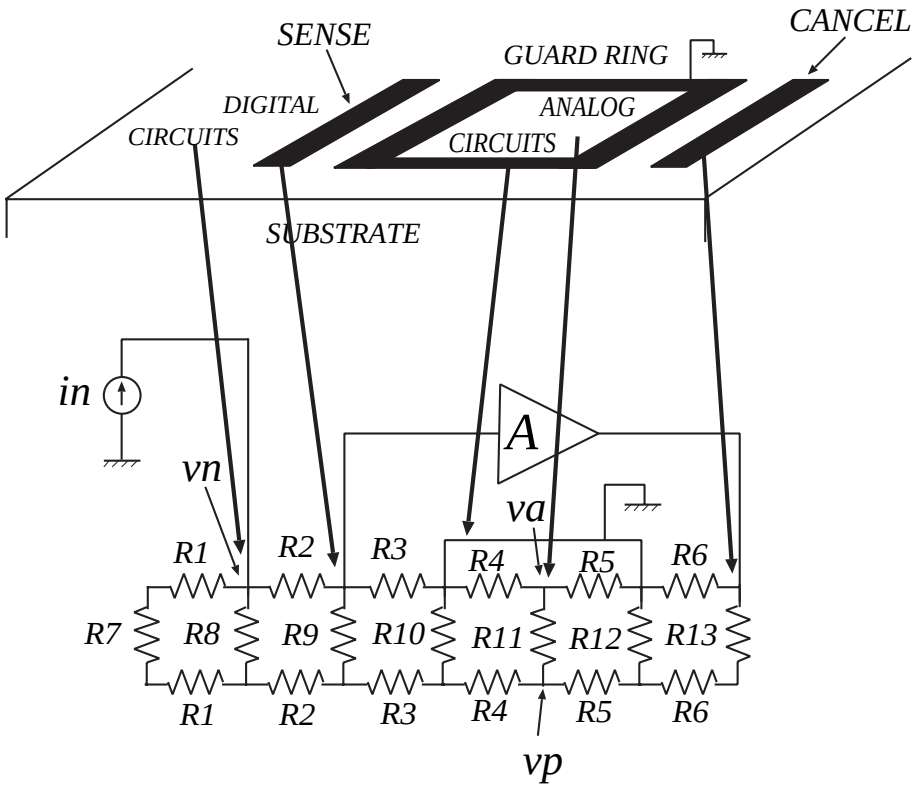

Figure 4.2: Active shield circuit for optimization.

In order to represent the positions of the noise source and the observation point inside the guard ring, the resistances R_1, R_2, R_4, and R_5 are rewritten as

$$R_1 = (1-a)R_{digital} \tag{4.7}$$
$$R_2 = aR_{digital} \tag{4.8}$$
$$R_4 = bR_{analog} \tag{4.9}$$
$$R_5 = (1-b)R_{analog} \tag{4.10}$$

where

$$R_{digital} = R_1 + R_2 \tag{4.11}$$
$$R_{analog} = R_4 + R_5 \tag{4.12}$$

and $0 < a, b < 1$. Using the typical resistances given in Table 4.1, the transfer functions from v_n to v_a for various gain values are shown in Figs.4.3 and 4.4. Figure 4.3 shows the transfer function characteristic versus the noise source position for a fixed observation point. Here when the arbitrary noise source position is taken into account, the noise transfer function differs from one to another noise source.

Figure 4.3 also shows that different gain values will also give different noise transfer characteristics.

Table 4.1: Typical resistances.

Name	**Value**[Ω]	**Name**	**Value**[Ω]
$R_{digital}$	400	R_8	100
R_{analog}	200	R_9	30
R_3	50	R_{10}	10
R_7	100	R_{11}	100

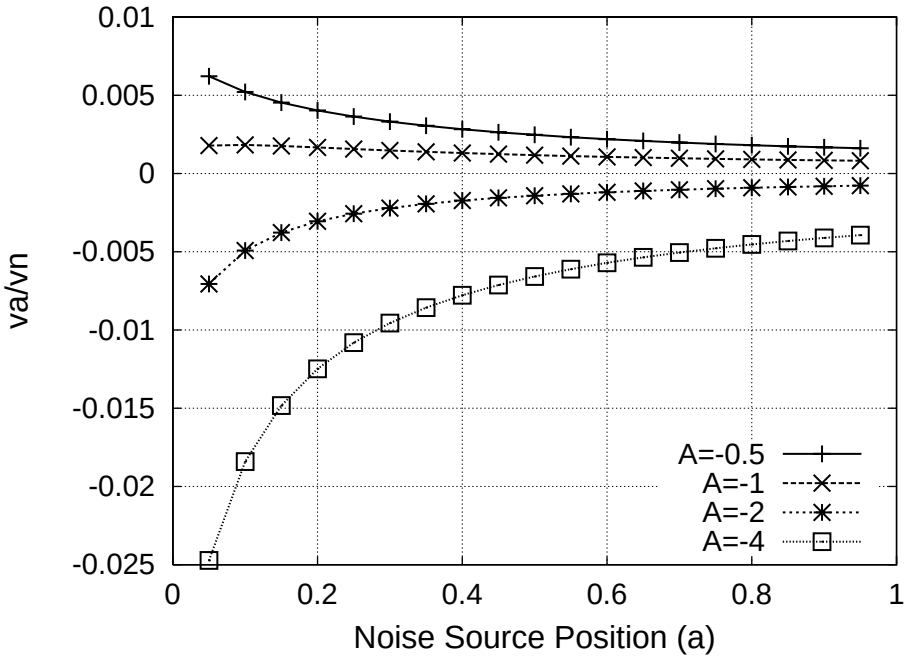

Figure 4.3: Transfer function from v_n to v_a for $b = 0.5$.

Figure 4.4 shows the noise transfer function for various observation points (the noise source is fixed at $a = 0.5$). Here when the area inside the guard ring is taken into account, it can be found that the noise transfer functions are different for all points in the area across the guard ring. For a given gain value, the zero noise transfer function will only be obtained at one b value and therefore a sufficient noise suppression performance can only be obtained in a relatively narrow area. Note that when A becomes more negative, the observation point position with the zero noise transfer function will move to a smaller b value. As a result, there is a value of

the gain A_{max} where the position of the point with the zero noise transfer function lies on the guard ring area. The essential point is that for $0 < |A| < |A_{max}|$, there always be a point (which is the value of b) where the noise transfer function becomes zero. Furthermore the zero noise transfer point drifts with the variation of the gain value. It seems that any gain value is reasonable because an area with zero noise transfer function can always be obtained although the position is different. However as is shown in Fig.4.4, when the gain varies, the noise transfer function is decreased for a particular area while another area has an increased noise transfer function. Therefore in order to optimize the performance of the active shield circuit, an evaluation method considering the overall noise transfer function characteristic in the whole analog area is required.

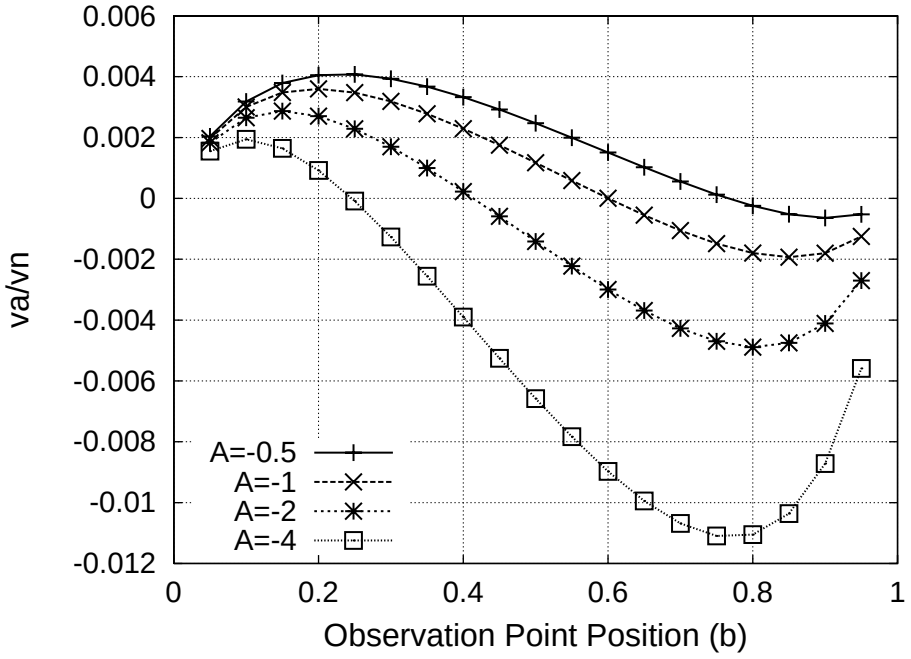

Figure 4.4: Transfer function from v_n to v_a for $a = 0.5$.

Recall Eq.(4.1) which shows that the optimum gain value depends on the resistances and therefore it will be very useful to examine the sensitivity of the gain to the resistances. Here the sensitivity of the gain to the resistances is defined by

$$S_{R_i}^{A} = \frac{\partial A}{A}\frac{R_i}{\partial R_i}, (i = 1..13). \tag{4.13}$$

The results are shown in Fig.4.5. Note that the gain has a large sensitivity to the variation of the values of R_3, R_6, R_{10}, R_{12}, and R_{13}. The sensitivities to the other resistances are small and can be ignored. As is shown in Fig.4.2, R_3 and R_6, R_{10}

and R_{12} create two pairs of resistances that will have the same value when the layout is symmetrical. Assuming $R_6 = R_3 = R_x$ will make the sensitivity of the gain to R_x as the sum of the sensitivities of the gain to R_3 and R_6. Thus for a relatively large R_x the gain sensitivity will become lower. Next, assuming that $R_{12} = R_{10} = R_y$ will make the sensitivity of the gain to R_y becomes negligible as is shown in Fig.4.6. Now it is clear that only R_{13} and $R_3(= R_x)$ are left for the consideration. Fortunately, R_{13} will be fixed for a given layout and therefore will have less contribution to the noise suppression performance.

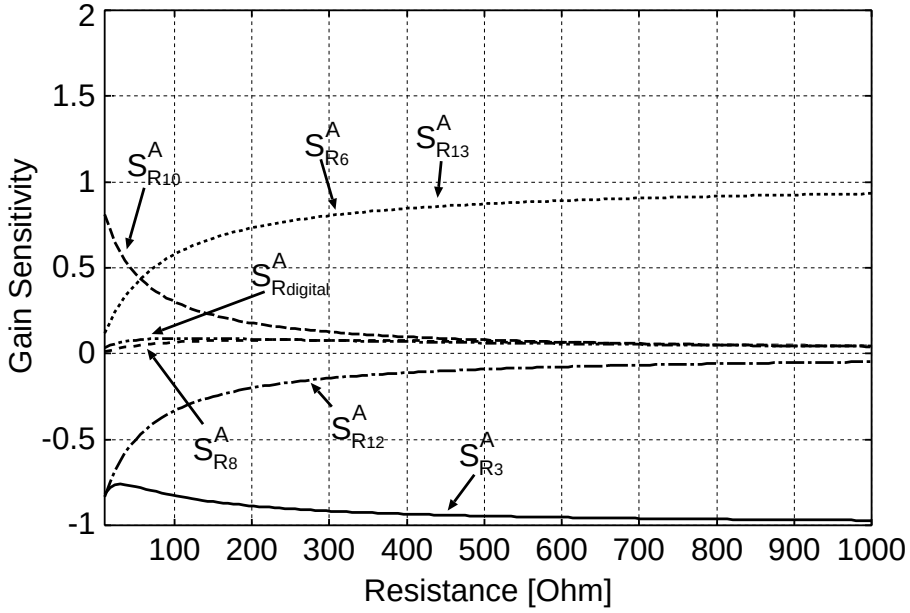

Figure 4.5: Gain sensitivity to resistances ($a = b = 0.5$).

The gain insensitivity to the values of R_{analog} and $R_{digital}$ is an advantage since it means that the optimum value of the gain will not be affected by the size of analog and digital area. When the noise source position (a value) varies in the active shield circuit in Fig.4.2, the noise amplitude at the sense node and the part of the noise coupled through the deep portion of the substrate will also vary. Therefore the sensitivity of the gain to the variation of the noise source position will be small. On the other hand, since the value of the optimum gain highly depends on the observation point position (b value), the gain will have a high sensitivity to the variation of the noise source position. These characteristics can be observed in Fig.4.7. Note that when $A = 0$ (thus there is only the conventional guard ring), the noise transfer function from a noise source to any point inside the guard ring will always be positive. Next, when $A < 0$, then the noise transfer function will move to negative values as the gain becomes more negative. Since the point of interest is the amplitude of the noise, the absolute value of the noise transfer function then

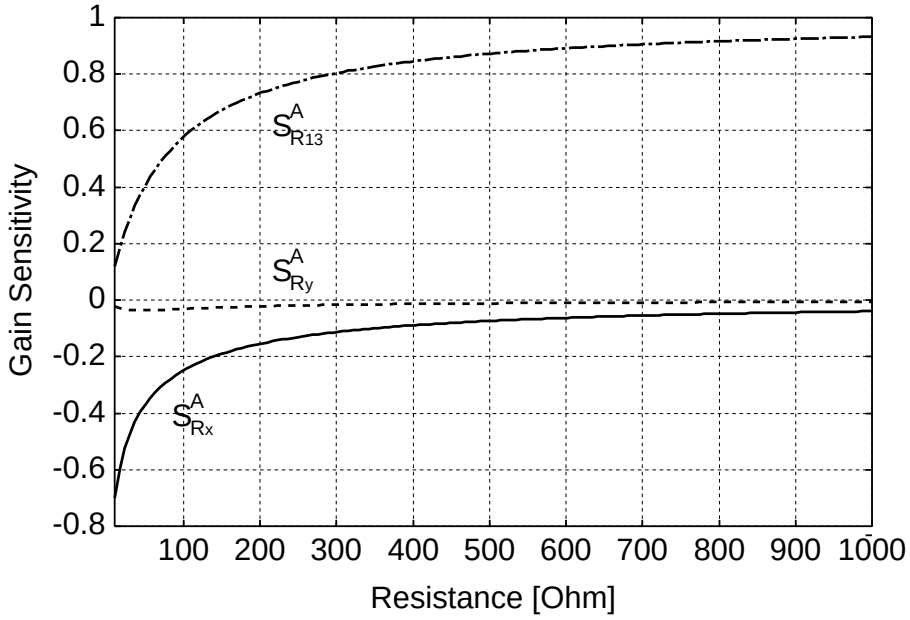

Figure 4.6: Gain sensitivity to resistances ($a = b = 0.5, R_3 = R_6 = R_x, R_{10} = R_{12} = R_y$).

will be considered. Remember that in the range of $0 < |A| < |A_{max}|$ there always be a zero noise transfer function at an observation point inside the guard ring. When A becomes more negative than A_{max}, a noise transfer function to every point inside the guard ring becomes negative (remember that the cancellation signal itself is a "noise") or in other words the amplitudes are larger than zero. As a result, the sum of the absolute value of the noise transfer functions will always have a minimum value at a gain value between 0 and A_{max}. Based on the property that the sum of the noise transfer functions for a specific noise source will always have a minimum value, an evaluation term by averaging the noise transfer function which is called Average Noise Transfer Function($ANTF$) is introduced. In case of the active shield circuit as is shown in Fig.4.2, the $ANTF$ will be given by

$$ANTF = \frac{1}{N}\left(\underbrace{\left|\frac{v_{a1}}{v_n}\right| + \left|\frac{v_{a2}}{v_n}\right| + \cdots + \left|\frac{v_{aN}}{v_n}\right|}_{N}\right) \tag{4.14}$$

$$= \frac{1}{N}\sum_{i=1}^{N}\left|\frac{v_{ai}}{v_n}\right| \tag{4.15}$$

where v_n is the noise amplitude at the noise injection point, v_{ai} is the noise amplitude observed inside the guard ring, and N is the number of observation points.

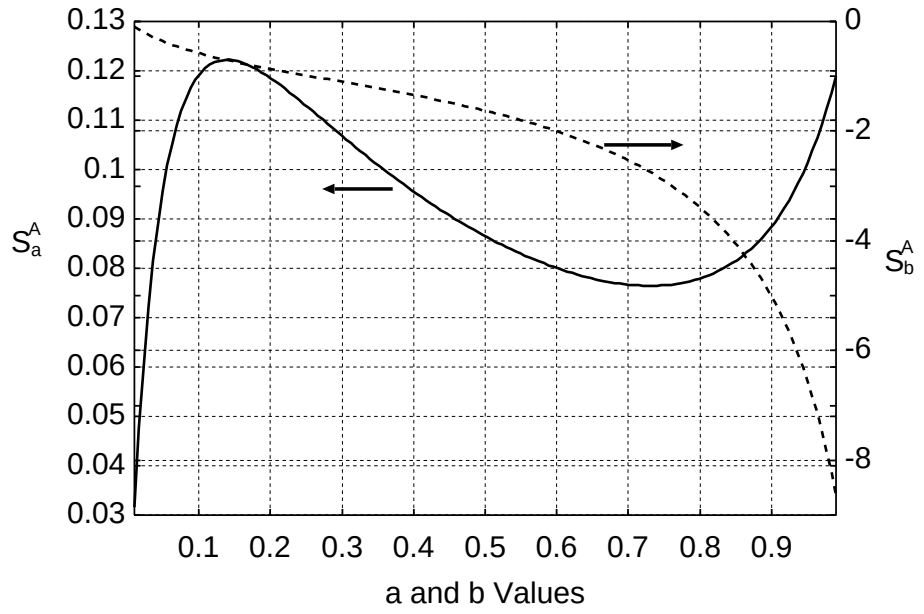

Figure 4.7: Gain sensitivity to noise source and observation point positions.

Under assumptions that $R_{12} = R_{10}, R_{13} = R_9, R_6 = R_3$ and using the typical resistances shown in Table 4.1, the $ANTF$ values with different gain values and noise source positions are shown in Fig.4.8.

Figure 4.8 shows that there is a gain value where $ANTF$ from a noise source at a given position becomes minimum. However this value depends on the substrate resistances. For example, Fig.4.9 shows the sum of $ANTF$s for $a = 0.1, 0.3, 0.6, 0.9$ with different R_3 values. The larger the value of R_3 is, the minimum value of the total $ANTF$ becomes smaller. When $R_3 \geq 100\Omega$, the total $ANTF$ for every gain value becomes smaller. Note that when R_3 becomes larger, the equivalent resistance between the noise source and the observation point becomes larger and this means an increase in the distance between these two points. The farther the noise source is, the noise amplitude observed inside the guard ring will be smaller and it explains the result in Fig.4.9. However, since this result is based on the calculation of a 2-dimensions resistive network, it does not reflect the area of the sense and the cancellation bands. In fact, a smaller diffusion area will give a larger value of R_3 without increasing the distance between noise source and guard ring. Since it is too complicated to perform a numerical evaluation of this property, it will only be shown by simulation results in section 4.2.

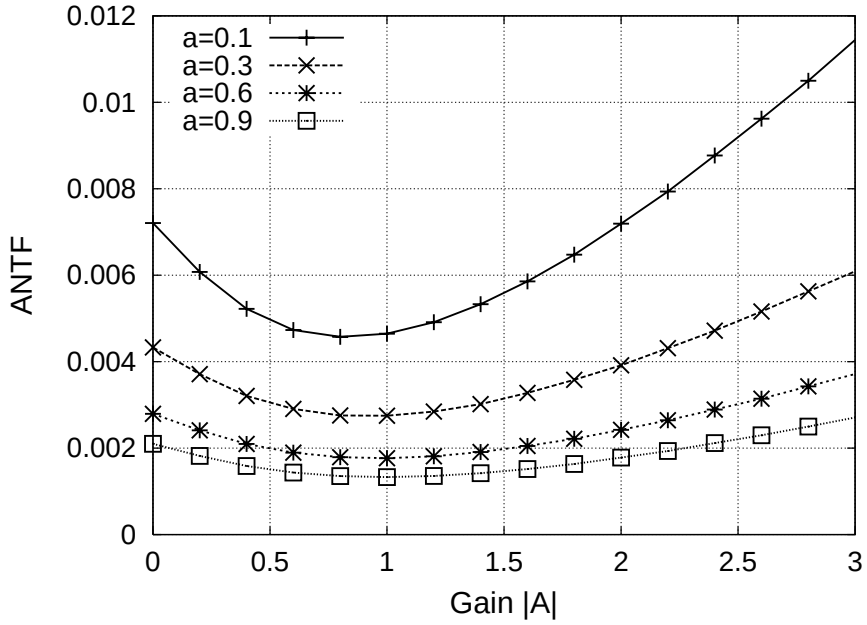

Figure 4.8: $ANTF$ versus gain ($R_3 = 50\Omega$).

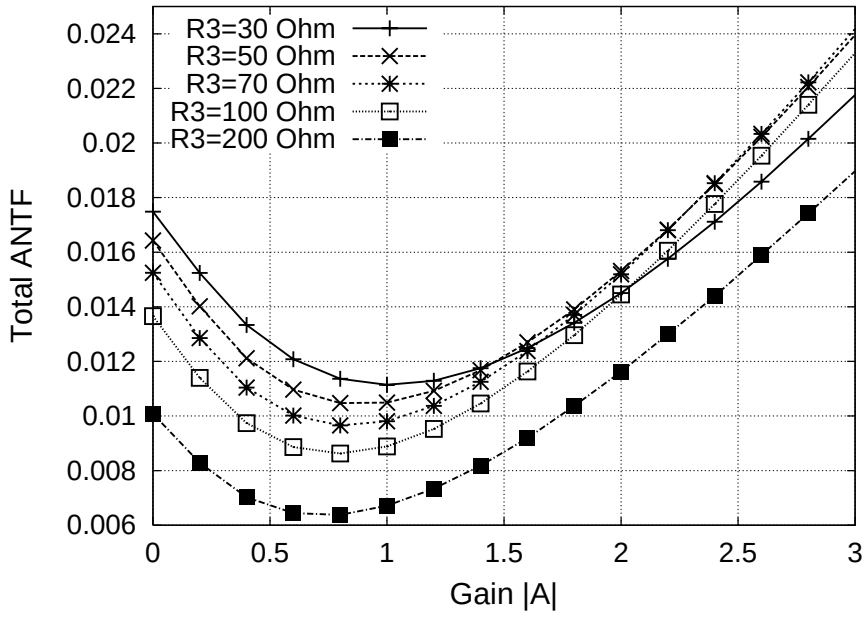

Figure 4.9: Total $ANTF$ versus gain.

Figure 4.10 shows the value of the gain A at which the minimum total $ANTF$ is obtained. Note that when $R_3 > 30\Omega$ the optimum gain value becomes $|A_{opt}| < 1$. The result in Fig.4.10 agrees with the fact that the optimum gain value has a large sensitivity to R_3 when the resistance is small and the sensitivity is smaller when R_3 increases(Fig.4.6). As is explained above, since a large R_3 means wasting chip area then medium R_3 values are more preferred. Figure 4.10 shows that for $R_3 > 80\Omega$ the gain fluctuation becomes smaller. Therefore choosing the optimum gain when $R_3 = 80\Omega$ will be reasonable since larger R_3 will not greatly change the optimum gain value. In this case the optimum gain value will be –0.8.

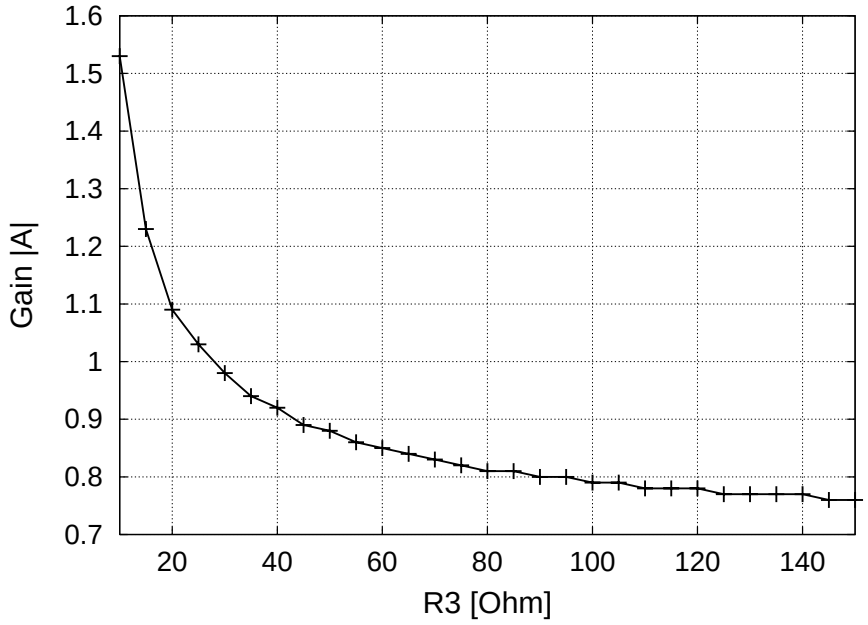

Figure 4.10: Optimum gain for various R_3 values.

Figure 4.11 shows the $ANTF$ of the conventional guard ring and the active shield circuit for various noise source positions (a values). Here the active shield circuit gives a lower $ANTF$ than the conventional guard ring. A maximum $ANTF$ improvement of about 40% is achieved using the active shield circuit.

4.2 Simulation Results

4.2.1 Simulated Substrate Model

A 3-dimensional resistive network as is shown in Fig.4.12 is used to evaluate the performance of the active shield circuit more accurately. The top view of the

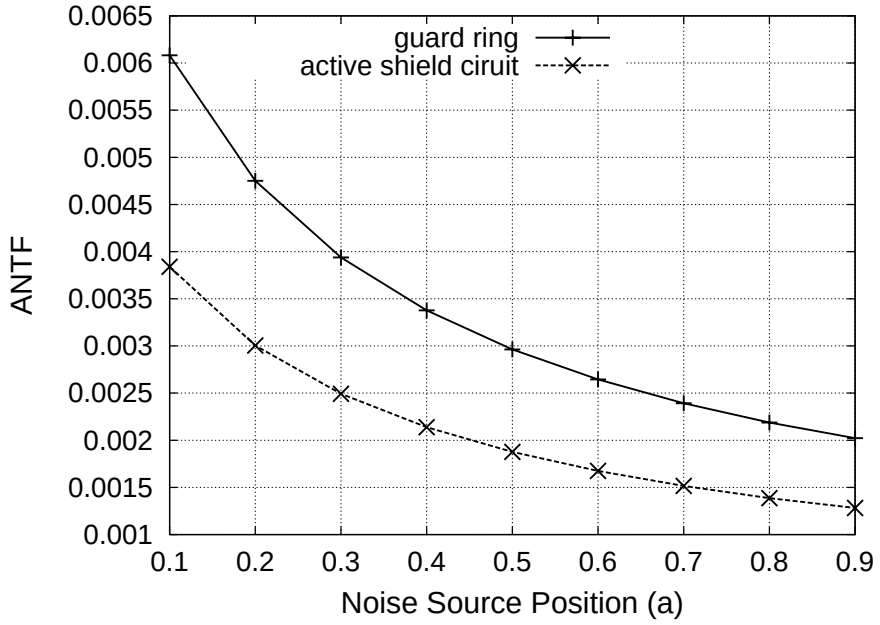

Figure 4.11: Optimum gain for various noise source positions.

substrate model with detailed resistances is shown in Fig.4.13. Nodes **n** and **p** are the nodes where the noise is injected and observed respectively. Nodes $\mathbf{s}_1$-$\mathbf{s}_2$-$\mathbf{s}_3$ and $\mathbf{c}_1$-$\mathbf{c}_2$-$\mathbf{c}_3$ are connected together with small resistances R_c's and represent the sense and cancellation bands respectively. Resistances are shown in Table 4.2. Here R_{vert} is the resistance of the vertical resistor in the 3-dimensional model (Fig.4.13). The guard ring, sense and cancel bands are represented by connecting 0.1mΩ resistances. Furthermore, a and c will represent the position of the noise source while b and d represent the position of the observation point inside the guard ring ($0 < a, b, c, d < 1$).

Table 4.2: Resistances for substrate model

Name	Ω	**Name**	Ω
R_{ah}	2k	R_{dh}	4k
R_{av}	2k	R_{dv}	2k
R_c	0.1m	R_u	100
R_s	400	R_{vert}	100

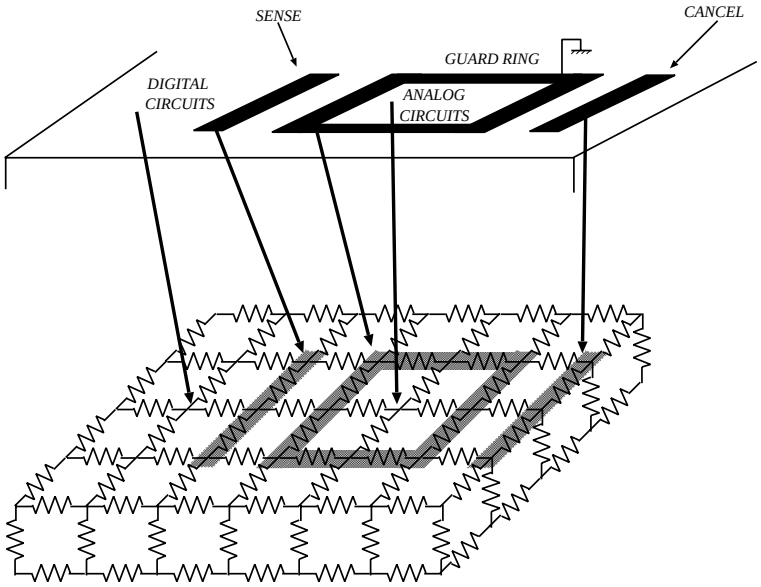

Figure 4.12: Simulated substrate model.

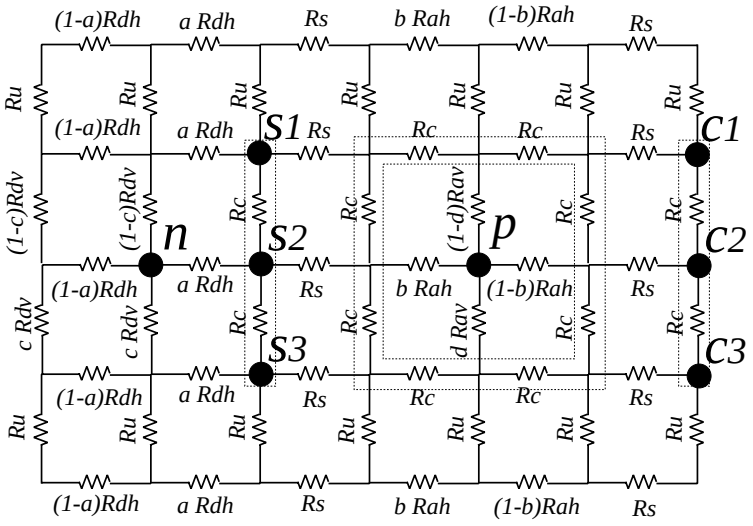

Figure 4.13: Substrate model top view.

4.2.2 Average Noise Transfer Function

Figure 4.14 shows the $ANTF$ versus gain values for various noise source positions. Here the minimum $ANTF$ values are obtained at around $A = -0.8$ regardless of the noise source position. Noise sources at a considerable distance will only contribute small $ANTF$s and become less significant as is shown in Fig.4.15. It also shows that the $ANTF$ obtained with the active shield circuit is about half of the one when using the conventional guard ring. However, the proposed circuit ($A = -0.8$) only has a lower $ANTF$ around 5% of the conventional circuit ($A = -1$).

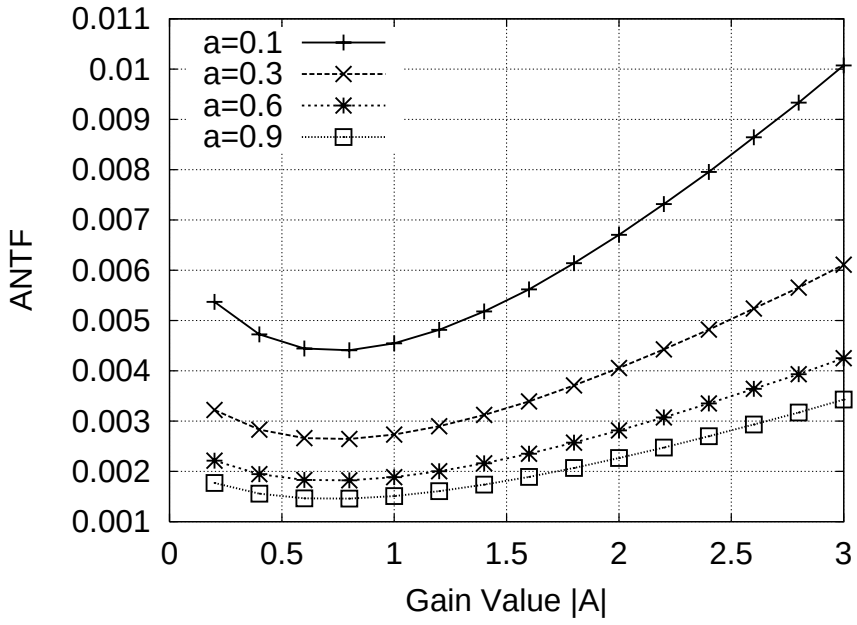

Figure 4.14: Simulated $ANTF$ for various gain values.

As is shown in Fig.4.10, the optimum gain becomes smaller with the increasing in R_3 value which will give the advantage for speed improvement. It is written in section 4.1 that increasing the distance between noise source and the guard ring will increase R_3. However this is not preferred since it will increase the area consumption of the active shield circuit. Another way to increase R_3 is reduction in the area of the sense and cancellation bands. This property can be implemented by removing the small resistances R_c's which connecting nodes $\mathbf{s}_1$-$\mathbf{s}_2$-$\mathbf{s}_3$ and $\mathbf{c}_1$-$\mathbf{c}_2$-$\mathbf{c}_3$ thus the input and the output of the active shield circuit are only connected to nodes $\mathbf{s}_2$ and $\mathbf{c}_2$ respectively. The variations of the area of the sense and cancellation bands are reflected by changing the resistances R_s's connecting nodes $\mathbf{s}_2$ and $\mathbf{c}_2$ to the guard ring.

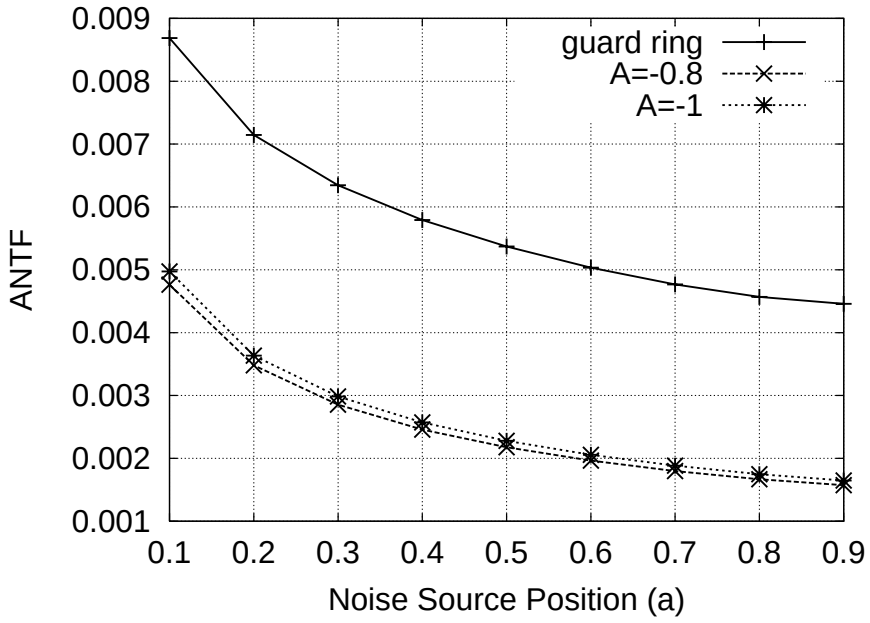

Figure 4.15: Simulated $ANTF$ for various noise source positions.

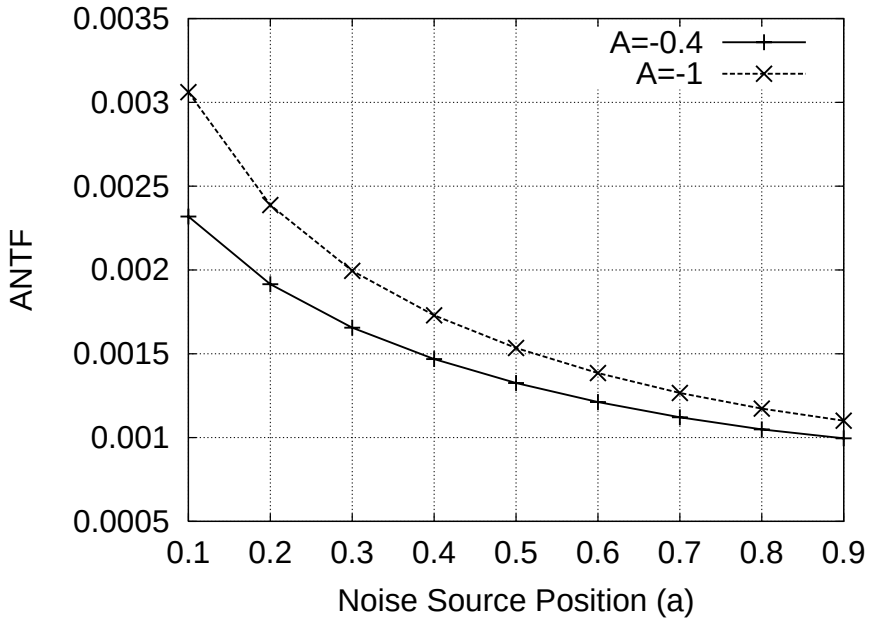

Figure 4.16: Average noise transfer function for smaller sense and injection diffusion areas.

As an example, the resistances R_s's connecting nodes $\mathbf{s}_2$ and $\mathbf{c}_2$ to the guard ring are increased ten times larger. In addition, the optimum gain for this case is found to be -0.4. Figure 4.16 shows the average noise level for the conventional circuit ($A = -1$) and the proposed circuit ($A = -0.4$). It shows that the proposed circuit gives the best improvement of about 28% for $a = 0.1$ and an improvement of 10% is achieved at $a = 0.9$.

4.3 Conclusions

A design methodology of active shield circuit based on average noise evaluation is proposed. An investigation on the sensitivity of the gain to the resistances shows that only R_3 which should be considered in the design methodology to find the optimum gain value. As is shown in Fig.4.10, choosing $R_3 > 50\Omega$ will give a gain value which is less sensitive to the variation of R_3.

A further design with consideration on the area of the sense and cancellation bands shows that the optimized gain is found to be -0.4. The active shield circuit designed with the proposed optimization method gives a maximum improvement of about 28% compared to the conventional circuit. In addition an $ANTF$ improvement of about 10% is achieved for noise sources at a far distance from the guard ring.

Chapter 5

Layout Consideration

This chapter will discuss the optimum layout of the active shield circuit. First the drawback of the conventional layout will be shown and then followed by the explanation of the cause. For speed improvement of an active shield circuit, some of the layouts that require an operational amplifier will not be discussed. Active shield layouts proposed in this chapter will only need an active shield circuit with a small gain.

5.1 Conventional Active Shield Layout

The previous chapters introduce the active shield circuit which senses the noise at a node between digital circuits and guard ring, and injects the cancellation signal into a node on the other side of the guard ring. Consider the active shield circuit in Fig.4.2. Equations (4.1) $\sim$ (4.6) show that the optimum gain value A depends on the values of R_4 and R_5. Since these resistances represent the position of the noise observation point inside the guard ring, this also means that for a fixed A, a proper noise suppression will only be obtained at a relatively narrow area. This can be explained briefly using Fig.5.1.

Figure 5.1 shows that the conventional active shield layout reduces the noise after it reaches the analog bulk. This means that the noise will be effectively reduced only when the amplitude of the cancellation signal is equal to the amplitude of the noise and its phase perfectly differs 180° from the noise phase. Since both the noise and the cancellation signal are attenuated across the substrate, the area where the noise is canceled out will be very narrow. Furthermore, since the cancellation signal itself is a *noise* this layout will add a noise at the other side of the guard ring. Define the effective noise suppression as the ratio of noise amplitude inside the guard ring between passive guard ring and active shield circuit.

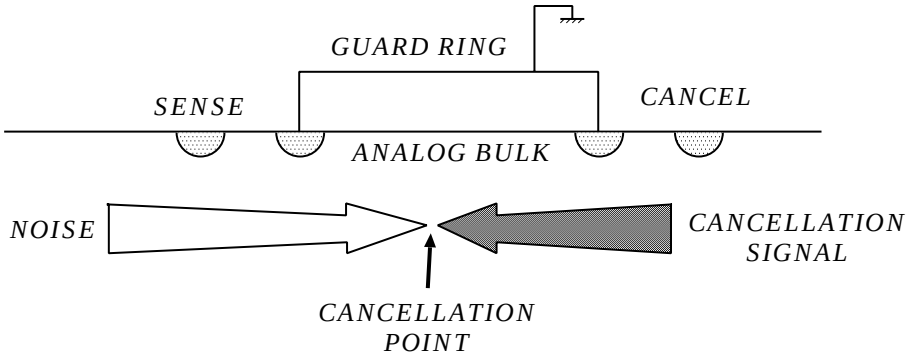

Figure 5.1: Conventional active shield layout.

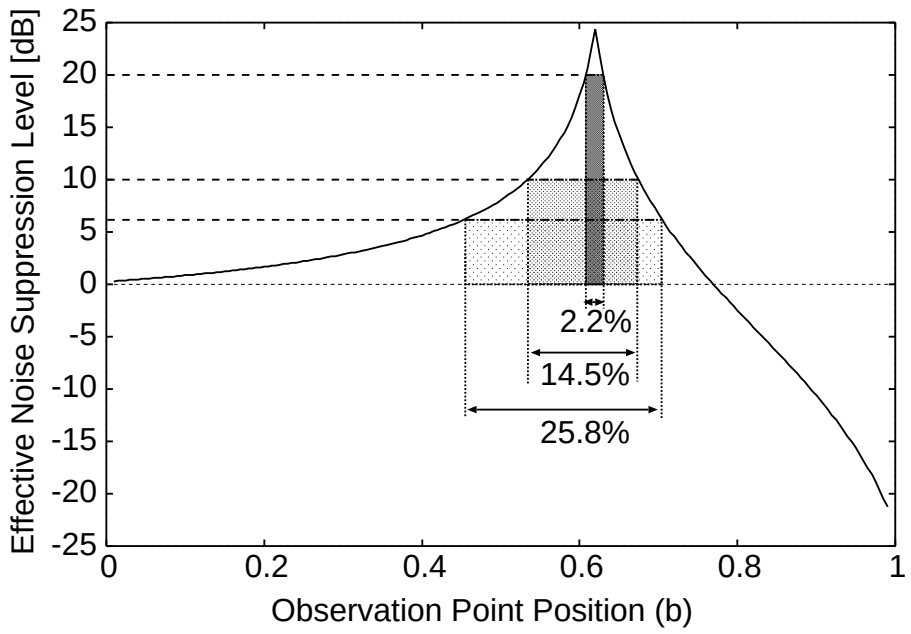

Figure 5.2: Effective noise suppression of the conventional layout.

The effective noise suppression when $A = -0.8$ and $R_3 = 80\Omega$ is shown in Fig.5.2. This figure shows that the active shield circuit reduces the noise to half of the noise level for about 26% of the entire area inside the guard ring when a conventional passive guard ring is used. Furthermore it will reduce the noise level to one tenth for 2.2% of the area inside the guard ring.

5.2 Proposed Active Shield Layout

Section 5.1 describes that the conventional active shield layout will be only effective for a narrow area since the noise is reduced after it reaches the analog area. Therefore, the key of the solution is how to reduce the noise before it reaches analog area. This section will show two alternatives to improve the effective noise suppression area of the active shield circuit.

5.2.1 Basic Idea

The first solution is canceling out the noise at the digital area instead of analog area by injecting the cancellation signal into a node on the other side across the digital area as is shown in Fig.5.3. Here the gain of the amplifier A required to

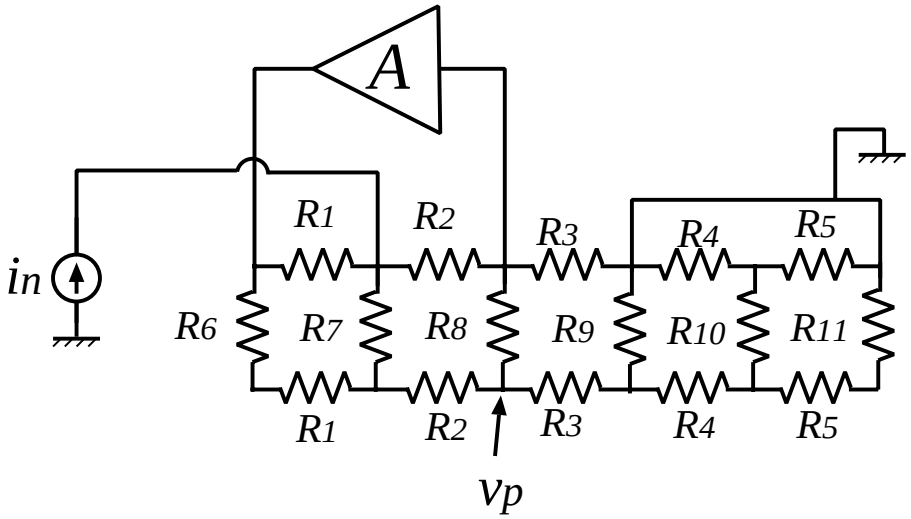

Figure 5.3: Active shield layout with cancellation node in digital area.

make the transfer function from i_n to v_p becomes zero is given by

$$A = -\frac{(R_3 + R_A)R_B}{R_3 R_C} \tag{5.1}$$

where

$$R_A = \frac{R_2 R_8}{R_2 + R_8 + R_D} \tag{5.2}$$

$$R_B = \frac{(R_1 + R_6)(R_2 + R_7) + R_2 R_7}{R_7} \tag{5.3}$$

$$R_C = \frac{R_8 R_D}{R_2 + R_8 + R_D} \tag{5.4}$$

$$R_D = \frac{(R_1 + R_6)(R_2 + R_7) + R_2 R_7}{R_1 + R_6}. \tag{5.5}$$

Equation (5.1) shows that the optimum gain value is independent of the values of R_4 and R_5 which means the noise suppression performance is not affected by the position of the observation point inside the guard ring. In other words, a proper noise suppression performance can be obtained for the entire area inside the guard ring.

Unfortunately the proposed circuit layout in Fig.5.3 has a shortcoming. Commonly the digital part in a mixed-signal integrated circuit usually has a much larger area than the analog part. In case of the layout in Fig.5.3, the sense node should be placed between the guard ring and the digital part while the output node should be placed at the opposite edge of the digital part. It means that the cancellation signal should be transmitted across the digital part which in most cases would be a long transmission line and thus produce a significant delay. This will reduce the performance of the active shield circuit.

Based on the study of the conventional circuit layouts, in order to obtain a proper noise suppression for the entire area inside the guard ring, the method which suppresses the noise before it reaches analog part is chosen. Furthermore, in order to reduce the delay of the transmission line, the output of the active shield circuit should be placed near its input. The proposed layout is shown in Fig.5.4. In this case, the optimum gain will be given by

$$A = -\frac{(R_2 + R_A)R_{10}}{R_2 R_B} \tag{5.6}$$

where

$$R_A = \frac{R_1 R_8}{2R_1 + R_7 + R_8} \tag{5.7}$$

$$R_B = \frac{(R_2 + R_C)(R_3 + R_9) + R_3 R_9}{R_9} \tag{5.8}$$

$$R_C = \frac{(R_1 + R_7)R_8}{2R_1 + R_7 + R_8}. \tag{5.9}$$

Since the optimum gain is determined by the substrate resistances, it will be very useful to examine the sensitivity of the optimum gain value to the variation of substrate resistances. The sensitivities for typical resistances are shown in Table

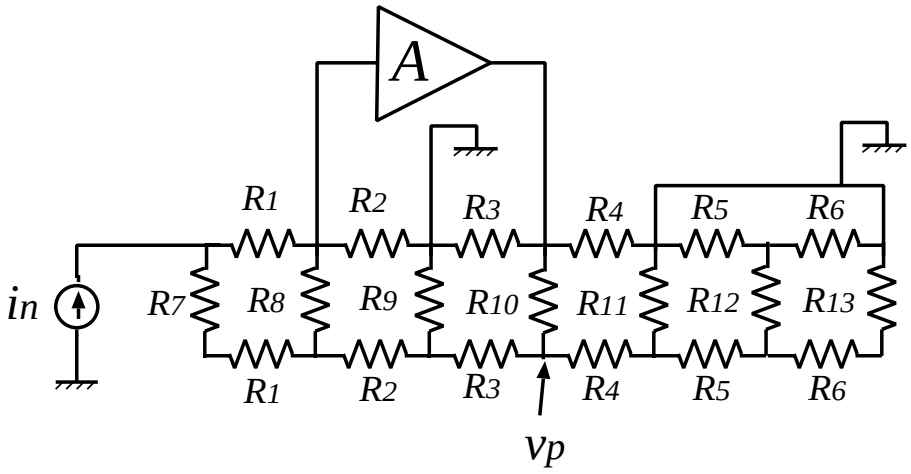

Figure 5.4: Active shield layout for optimum performance.

5.1. It shows that the optimum gain value has a high sensitivity to the values of R_2, R_3, R_9, and R_{10}. However, since they are fixed for a given layout, the sensitivities to these resistances can be ignored. The values of R_1 and R_7 will vary with various noise source positions and injection area. Fortunately, since the gain sensitivities to these resistances are low, the variation of noise source position and injection area will not have great effects on the active shield circuit performance. The optimum gain value for various resistances is shown in Fig.5.5. Using the initial resistance in Table 5.1, for a given resistance range from 10 to 100Ω, the optimum gain value never exceeds –1. On the other hand, it reaches –2 for $R_2 = 10\Omega$. Note that since the horizontal and the vertical resistances depend on the distance between two nodes and the size of the substrate contact respectively, a careful layout which also means carefully selecting the resistances will guarantee that the optimum gain value will always be smaller than –1. Therefore an attenuator will be required instead of an amplifier. This will give an advantage for improving the active shield circuit's bandwidth.

Table 5.1: Gain sensitivity to substrate resistances.

Name	**Value**[Ω]	S_R^A	**Name**	**Value**[Ω]	S_R^A
R_1	100	-0.095	R_8	50	0.175
R_2	50	0.924	R_9	50	0.36
R_3	50	-0.64	R_{10}	50	1
R_7	100	0.124			

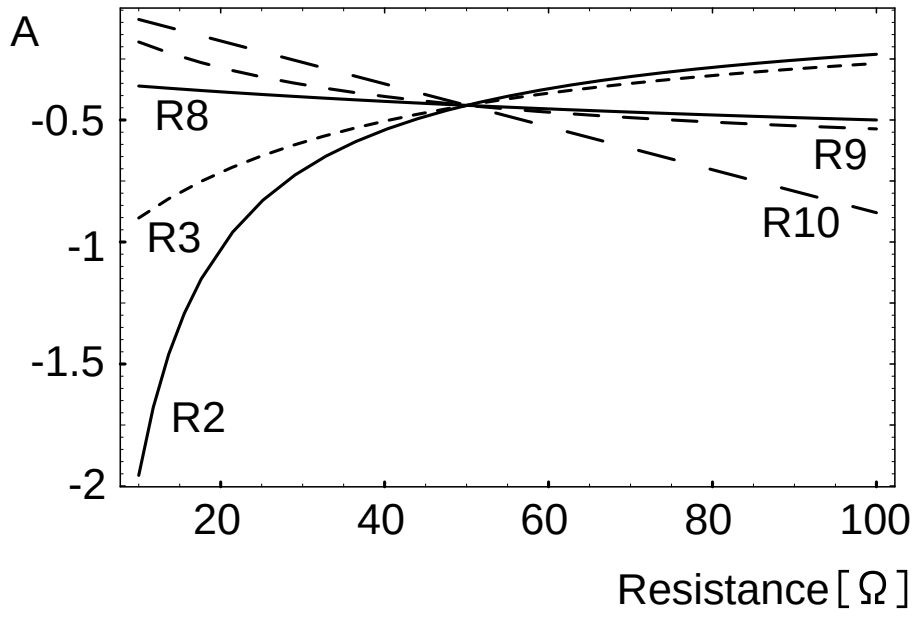

Figure 5.5: Optimum gain for various substrate resistances.

5.2.2 Circuit Implementation

An alternative implementation of the amplifier for an active shield circuit is shown in Fig.5.6. This circuit is derived from the circuit in Fig.3.13. Transistor M_1 works as a V-I converter which converts the input voltage to current. This current then will be inverted by the current mirror and converted to the output voltage by M_4. The MOS transistors M_a to M_d construct a current switch to control the gain of the amplifier while keeping the bias current constant. Assume that V_C and the input voltage are zero (the input node is grounded) and therefore the gate to source voltages of M_1, M_2 and M_3 are equal ($V_{GS1} = V_{GS2} = V_{GS3} = V_0$). Here their drain currents will be given by

$$I_{DS1} = I_{DS2} = 2K(V_0 - V_{TN})^2 \tag{5.10}$$

$$I_{DS3} = 1.5K(V_0 - V_{TN})^2. \tag{5.11}$$

Under the assumption of an ideal current mirror, I_1 and I_2 become

$$I_1 = I_2 = \frac{1}{2}I_{DS1} + \frac{1}{2}I_{DS2} \tag{5.12}$$

$$= 2K(V_0 - V_{TN})^2, \tag{5.13}$$

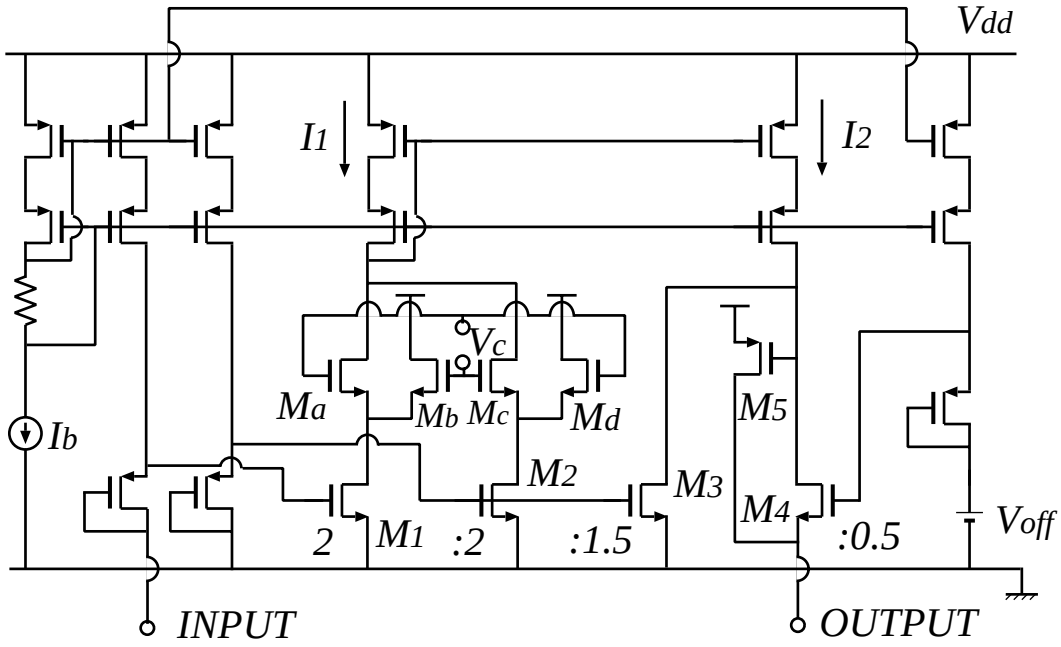

Figure 5.6: Proposed circuit.

therefore the drain current of M_4 is

$$\begin{aligned} I_{DS4} &= I_2 - I_{DS3} && (5.14)\\ &= 2K(V_0 - V_{TN})^2 - 1.5K(V_0 - V_{TN})^2 && (5.15)\\ &= 0.5K(V_0 - V_{TN})^2. && (5.16) \end{aligned}$$

The gate to source voltage of M_4 then will be given by

$$\begin{aligned} V_{GS4} &= \sqrt{\frac{I_{DS4}}{0.5K}} + V_{TN} && (5.17)\\ &= V_0. && (5.18) \end{aligned}$$

Thus the bias voltage of the output node is

$$\begin{aligned} V_{OUT} &= V_{off} + V_0 - V_{GS4} && (5.19)\\ &= V_{off}. && (5.20) \end{aligned}$$

In order to produce this offset voltage, a constant bias current is injected into the substrate. The transistor M_5 will supply this bias current while forming a feedback loop to fix the drain voltage of M_4.

5.2.3 Poles and Zeros Estimation

In this section, the poles and zeroes of the circuit in Fig.5.6 will be estimated as a consideration to improve the frequency performance of the active shield circuit. Note that the frequency characteristic of noise suppression performance is determined by the dominant pole of the active shield circuit. Since the gain of the active shield circuit needs to be tuned to achieve a proper noise suppression, it is preferable that the dominant pole of the circuit is not affected by the variation of the gain. Therefore it is necessary to find which circuit parameters determine the dominant pole. First, consider the input stage shown in Fig.5.7. Here the transfer

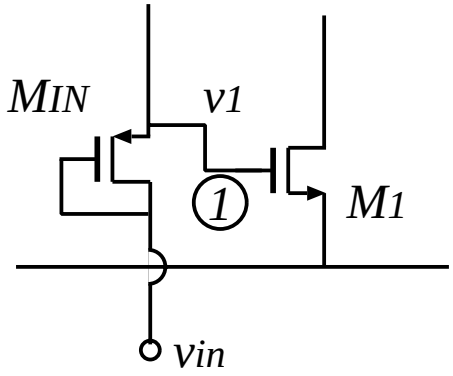

Figure 5.7: Input stage of the active shield circuit.

function from v_{in} to v_1 will be given by

$$\frac{v_1}{v_{in}} \approx \frac{g_{m\_in} + sC_{gs\_in}}{g_{m\_in} + s(C_{gs\_in} + C_{gs1})}. \tag{5.21}$$

Here g_m and C_{gs} are the transconductance and the parasitic capacitance between gate and source of a MOS transistor respectively. The first pole and zero will be given by

$$\omega_{p1} \approx \frac{g_{m\_in}}{C_{gs\_in}} \tag{5.22}$$

$$\omega_{z1} \approx \frac{g_{m\_in}}{C_{gs\_in} + C_{gs1}}. \tag{5.23}$$

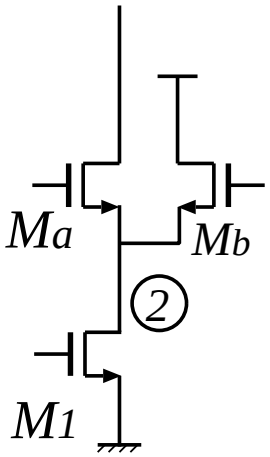

Figure 5.8: Gain control stage.

Next, the second pole can be obtained from the the drain node of M_1 as is shown in Fig.5.8. Here it will be given by

$$\omega_{p2} \approx \frac{g_{ma} + g_{mb}}{C_{gsa} + C_{gsb}}. \tag{5.24}$$

The third pole will be the pole of a current mirror and is commonly given by

$$\omega_{p3} \approx \frac{g_{mcm}}{C_{gscm}}. \tag{5.25}$$

The fourth and fifth poles can be estimated from the output stage in Fig.5.9. They will be given by

$$\omega_{p4} \approx \frac{g_{m4} g_{m5} R_{sub}}{(1 + g_{m4} R_{sub}) C_{gs5}}, \tag{5.26}$$

$$\omega_{p5} \approx \frac{g_{m4} g_{m5} r_{ds3} r_{ds4}}{(r_{ds3} + r_{ds4}) C_{gs4}} \tag{5.27}$$

respectively. When $g_{m4} R_{sub} \ll 1$ is assumed, the fourth pole given by Eq.(5.26) will be the dominant pole of the active shield circuit. In order to keep the speed of the circuit, it is necessary to make the transconductances g_{m4} and g_{m5} constant. This can be achieved by applying a constant bias current to M_4 and M_5. Assume that M_2, M_c, and M_d are removed from Fig.5.6. When the gain is changed by varying V_C, the bias currents flow through M_4 and M_5 will also be changed. The cutoff frequency of the circuit will become lower when the gain is decreased. In order to avoid this problem, M_2, M_c, and M_d are added. These transistors provide an additional bias current which will increase when the gain is decreased. Thus the bias current of M_4 will always be constant.

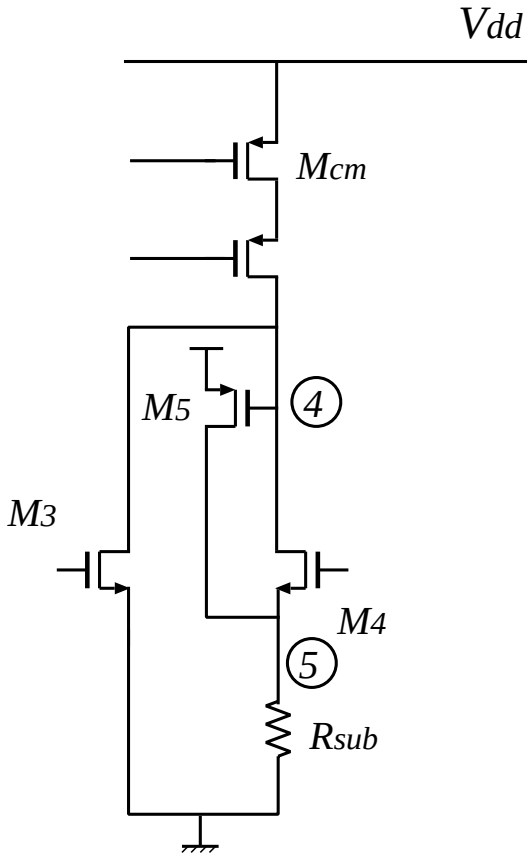

Figure 5.9: Output stage of the active shield circuit.

5.2.4 Simulation Results

Simulated Substrate Model

Resistive networks with 11 nodes are used to represent the area of the digital part and analog part inside the guard ring as is shown in Fig.5.10. The noise source is injected at nodes $\mathbf{d}_1 \sim \mathbf{d}_{11}$ while the noise level inside the guard ring will be observed at nodes $\mathbf{a}_1 \sim \mathbf{a}_{11}$. The unlabeled horizontal resistances and vertical resistances are 50Ω and 100Ω respectively. The other resistances are shown in Table 5.2.

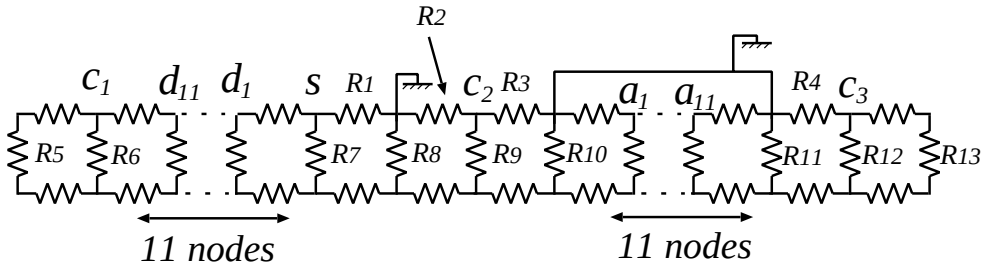

Figure 5.10: Simulated substrate model.

Table 5.2: Resistances for substrate model

Name	Ω	Name	Ω	Name	Ω
R_1	50	R_6	50	R_{10}	50
R_2	50	R_7	80	R_{11}	30
R_3	50	R_8	50	R_{12}	50
R_4	50	R_9	50	R_{13}	80
R_5	50				

Proposed Circuit Characteristic

The proposed circuit is simulated using HSpice circuit simulator with 0.35μm CMOS process parameters. The supply voltage is 3V and the output offset voltage V_{off} is set to 50mV. Figure 5.11 shows the gain characteristic of the proposed circuit versus the gain control voltage V_C. Here the gain varies from -46dB to 9dB when V_C is changed from -0.5V to 0.5V. Figure 5.12 shows the frequency characteristic of the variable gain amplifier. Note that the cutoff frequency of the variable gain amplifier does not change even when the gain is varied. This result is

confirmed by the analysis of the dominant pole in section 5.2.3. It is proved here that the speed of the variable gain amplifier will not decrease as long as the bias currents of M_4 and M_5 are kept constant.

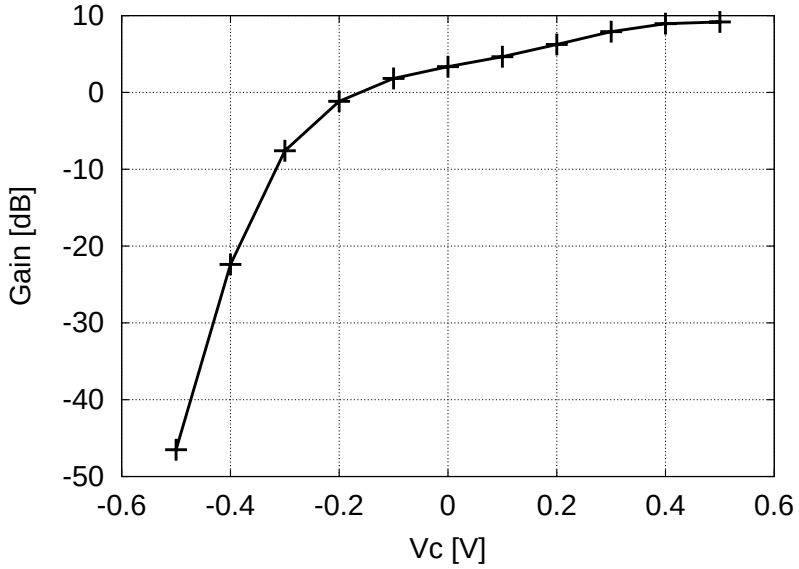

Figure 5.11: Gain versus control voltage.

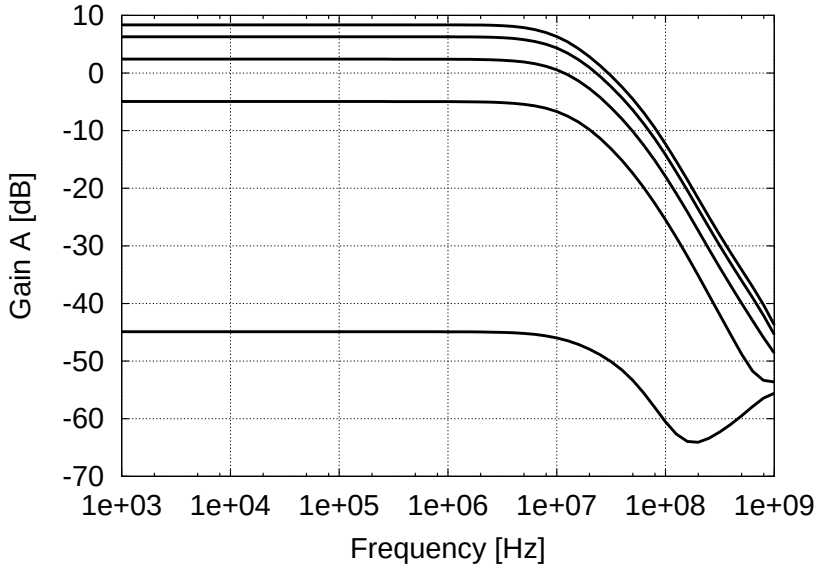

Figure 5.12: Frequency characteristic of variable gain amplifier.

Active Shield Circuit

Figure 5.13 shows the frequency characteristic of the conventional passive guard ring and the proposed active shield circuit. A current noise source is injected into node $\mathbf{d}_6$ and the noise level inside the guard ring is observed at node $\mathbf{a}_6$. Since the guard ring is connected to the ideal ground, the frequency characteristic is flat. The conventional passive guard ring suppresses the noise level to -52dB. On the other hand, the active shield circuit gives a minimum noise level of -85dB for $V_C = -0.31V$. Under an assumption that V_C varies in a range of $\pm$10mV, the active shield circuit still gives a noise level 18dB lower than the conventional passive guard ring.

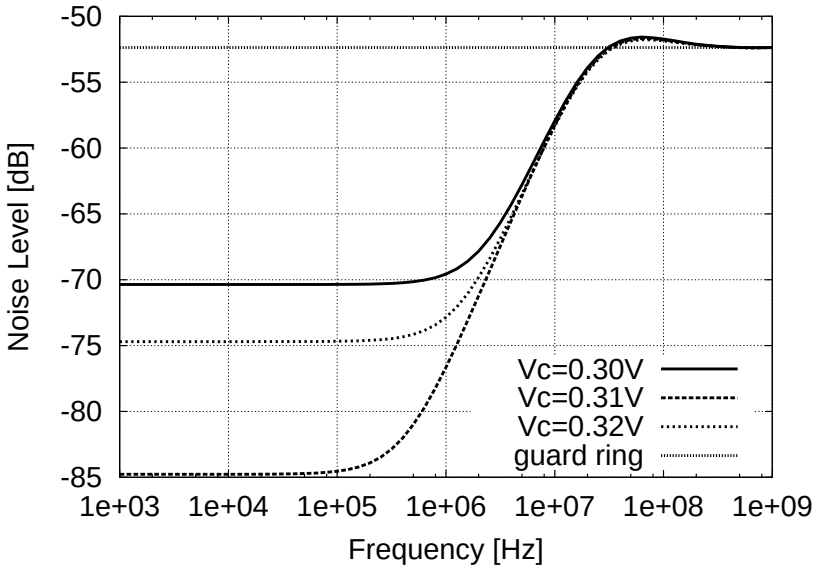

Figure 5.13: Frequency characteristic of the proposed active shield circuit.

Figure 5.14 shows the noise level at each node inside the guard ring. It shows that the conventional layout reduces the noise only for a relatively narrow area. On the other hand, the proposed layout effectively reduces the noise level on the entire area inside the guard ring. It seems that the proposed layout shown in Fig.5.3 might have a better performance than the proposed layout in Fig.5.4. However, with the given substrate model the proposed layout in Fig.5.3 needs an amplifier with a gain of 72dB. Since the implementation is impractical, it is simulated using ideal components. Practically, noise source positions in a mixed-signal integrated circuit are arbitrary and it is necessary to inspect the performance of the proposed active shield circuit considering this property of a noise source position. The simulation result is shown in Fig.5.15. It shows that the noise levels inside the guard ring when using the passive guard ring, the conventional layout and the

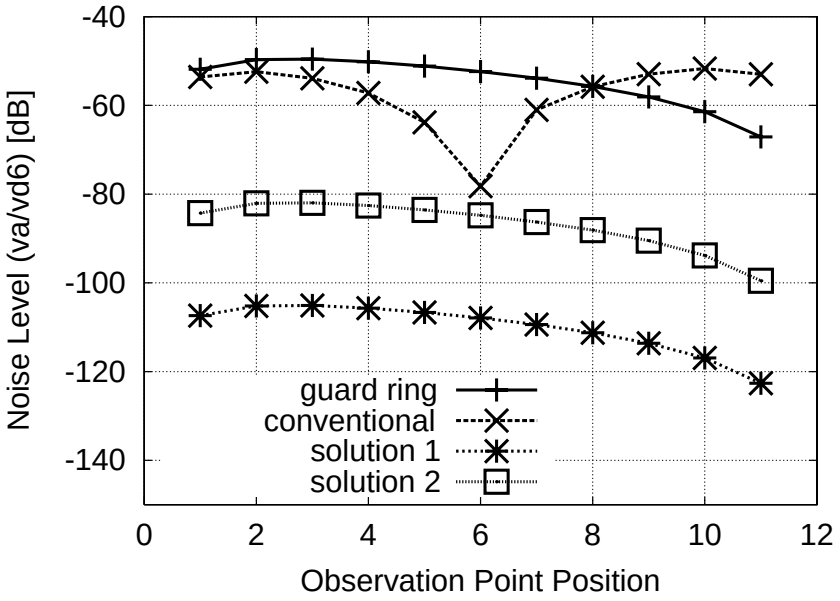

Figure 5.14: Noise level observed at each node inside the guard ring.

proposed layouts decrease with the increase of the distance from the noise source to the guard ring. The proposed layout in Fig.5.3 gives the lowest noise level for the optimized noise source position but noise from different position is not properly reduced. The difference between the lowest and the highest noise level for the layout in Fig.5.3 is about 70dB while the layout if Fig.5.4 only has a difference of about 30dB.

Since the noise level inside the guard ring is reduced proportionally with the increase in the noise source distance to the guard ring, it will be more effective to optimize the gain of the active shield circuit with a noise source injected at node $\mathbf{d}_1$. Figure 5.16 shows the simulation result of the noise level inside the guard ring for various noise source positions when the gain of the active shield circuit is optimized for a noise source at node $\mathbf{d}_1$. Similar to the characteristic in Fig.5.15, the layout in Fig.5.3 has lowest noise level for the noise in the optimized position ($\mathbf{d}_1$). Although reduced, the difference between the noise level for the optimized noise source position and the worst noise level is 20dB. On the other hand, the difference between the noise level for the optimized noise source position and the worst noise level of the layout in Fig.5.4 is only 3dB. As a conclusion, in order to obtain the optimum noise suppression performance for arbitrary noise source positions, the gain of the active shield circuit should be optimized to suppress the noise from the nearest source to the guard ring.

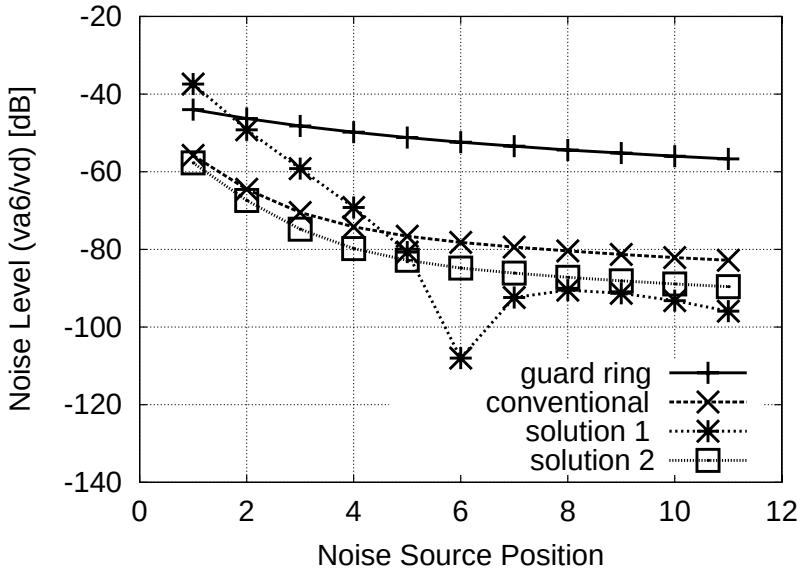

Figure 5.15: Noise level observed at node $\mathbf{a}_6$with various noise source position (optimized for noise injected at node $\mathbf{d}_6$).

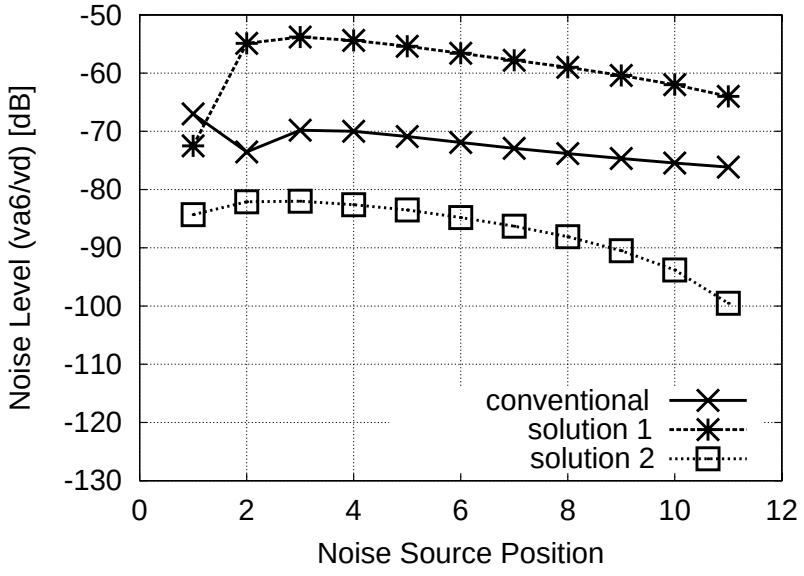

Figure 5.16: Noise level observed at node $\mathbf{a}_6$ with various noise source position (optimized for noise injected at node $\mathbf{d}_1$).

In the previous simulations, it is assumed that there is only one noise source while there are actually multiple noise sources. Fortunately, since superposition principle is adaptable, multiple noise sources can be represented as a single equivalent noise source. Therefore the above simulation results is also well applied with multiple noise sources.

5.3 Consideration on Bulk Potential Gradient

As is explained in section 3.2.1, the DC offset technique is applied in order to enable the full integration of the overall active shield circuit on the chip. This method will apply a DC voltage to the substrate and therefore it may cause a substrate potential gradient on the analog area. Since the bulk potential gradient is a serious issue when device matching is critical, it should be fairly examined. The potential gradient is simulated using the substrate model in Fig.5.10. A DC bias offset of 50mV is applied at node $\mathbf{c}_2$ and the potentials at nodes $\mathbf{a}_i (i = 1 \sim 11)$ are observed. The simulation result is shown in Fig.5.17. Here the maximum bulk

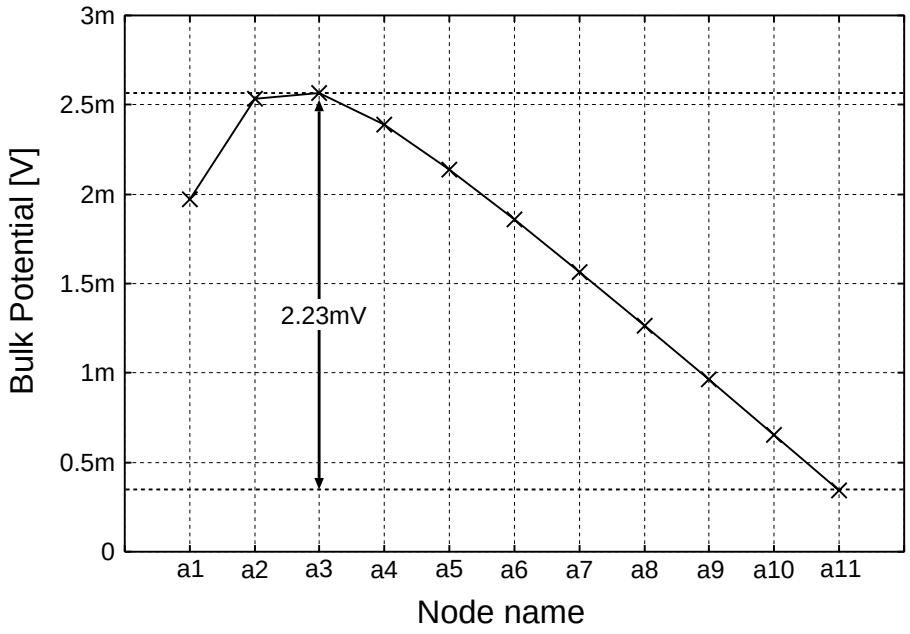

Figure 5.17: Bulk potential gradient on the area inside the guard ring.

potential difference is found to be as small as 2.23mV. Since devices which need good matching should be placed nearby, the bulk potential difference will be less

than 2.23mV. As a result, the DC bias offset applied on the substrate will not greatly affect the matching between devices.

5.4 Conclusions

It is revealed that the conventional active shield layout only has an effective noise suppression performance on a narrow area inside the guard ring because the noise is canceled after it reaches analog bulk. A new layout of an active shield circuit based on the noise cancellation before the noise itself reaches analog bulk is proposed. The proposed layout is able to suppress the noise at the entire area inside the guard ring. Simulation results show that the proposed layout gives a noise level of -85dB while the passive guard ring suppresses the noise to -52dB. The deterioration of the noise suppression performance due to the fluctuation in the gain control voltage of the amplifier can be reduced by reducing the voltage-to-gain conversion parameter value.

A brief estimation on the dominant pole of the proposed active shield circuit is performed. The dominant pole position is kept constant by applying a bias that does not depend on the gain of the circuit. The layout of the proposed active shield circuit should be chosen carefully in order to keep the optimum gain of the amplifier as low as possible and thus gives a possibility for speed improvement.

The effect of applying a DC bias offset onto the substrate is also investigated. A simulation result shows that the maximum bulk potential difference is 2.23mV when an offset of 50mV is applied. Since devices need to have a good matching are commonly placed nearby, the bulk potential difference then will be less than 2.23mV and therefore the DC bias offset will not cause a significant effect on the matching between devices.

Chapter 6

Automatic Gain Controlling

6.1 Drawback in Proposed Layout

This section will describe the drawback of the proposed active shield layout. Consider the proposed active shield layout shown in Fig.5.4 and redraw it to a simplified circuit block as is shown in Fig.6.1. This simplified circuit block will be used to

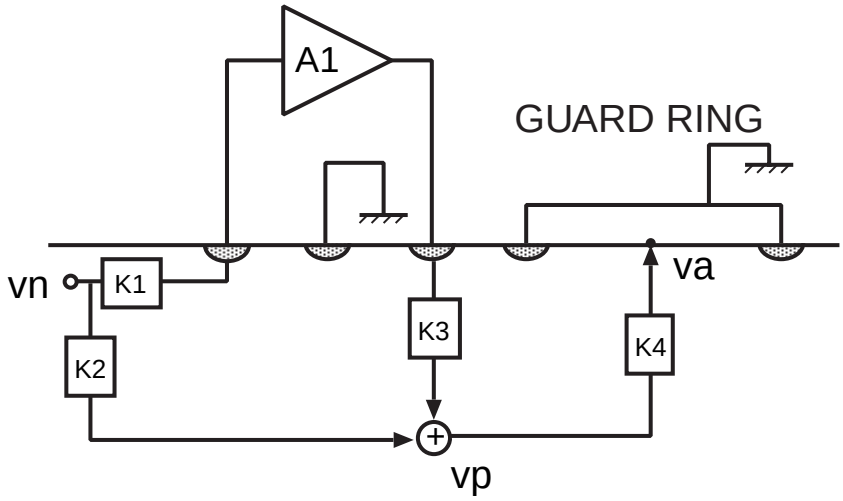

Figure 6.1: Simplified circuit block of active shield layout in Fig.5.4.

analyze the transfer function of the proposed active shield layout in Fig.5.4. Here v_n, v_p, v_a and K_i's$(i = 1 \sim 4)$ are the noise source, the noise at the deep portion of the substrate, the noise at an observation point inside the guard ring and the transfer parameters which are determined by the substrate resistances respectively.

The transfer function from v_n to v_p then will be given by

$$\frac{v_p}{v_n} = K_1 K_3 A_1 + K_2. \tag{6.1}$$

The noise transfered to the analog portion will become zero when $v_p = 0$, that will result in the optimum gain value A_1 of

$$A_1 = -\frac{K_2}{K_1 K_3}. \tag{6.2}$$

The above result shows that as long as the gain of the amplifier A_1 is set to the value given by Eq.(6.2), the transfer function from v_n to v_p will always become zero. It is clearly stated that the optimum gain of the active shield circuit is determined by substrate resistances. In order to set the gain of the active shield circuit to a proper value, it is necessary to know the substrate resistances in advance. The practical problem is that the values of substrate resistances and thus the values of K_i's are unknown until the chip is fabricated because they highly depend on physical characteristics of the substrate. Since the physical characteristics of the substrate are affected by the fabrication process itself, process variation also has a significant effect on the performance of the active shield circuit. As a result when the gain of the active shield circuit differs from the optimum value given by Eq.(6.2), then the absolute value of the noise transfer function from v_n to v_p will become larger as is shown in Fig.6.2.

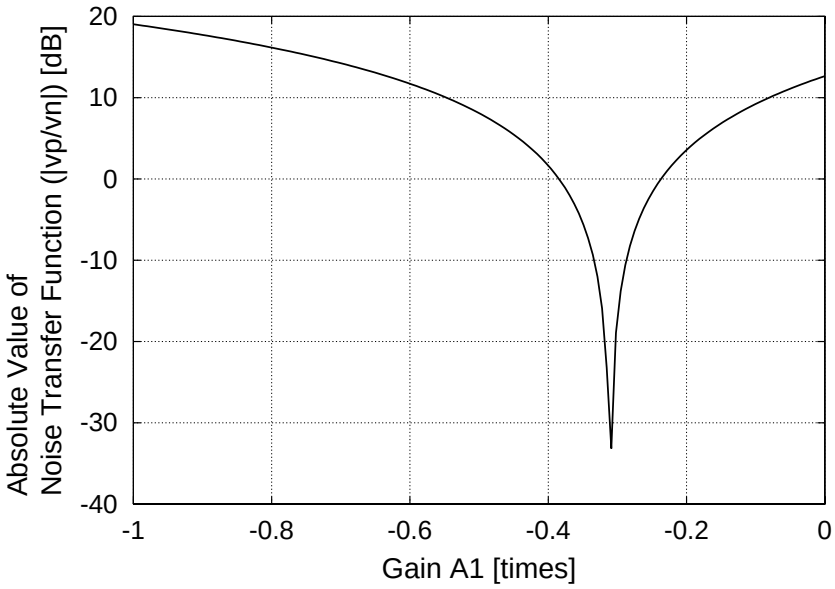

Figure 6.2: Noise transfer function versus the gain of the active shield circuit.

6.2 Automatic Gain Control Principle and Implementation

Since the process variation will vary the substrate resistances and thus change the optimum gain value which is required to make the transfer function from v_n to v_p become zero, the utilization of an automatic gain control technique will compensate this problem.

Assume that the gain control is given by the circuit block G as is shown in Fig.6.3. Next, rewrite the gain A_1 as

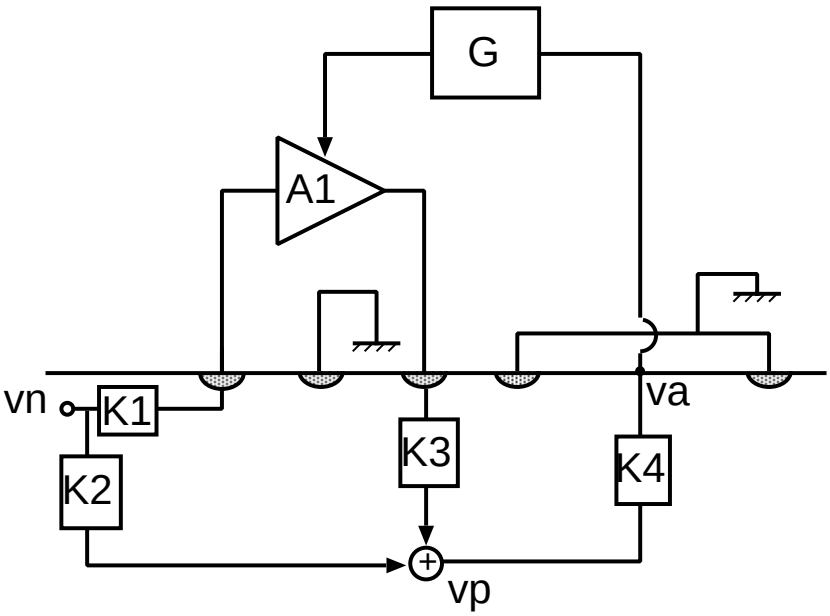

Figure 6.3: Circuit block for automatic gain scheme.

$$A_1 = A_0 - Gv_a \tag{6.3}$$
$$= A_0 - GK_4v_p, \tag{6.4}$$

where A_0 is an initial gain of VGA and G is a gain control parameter. Substituting Eq.(6.4) into (6.1) and solving it for v_p will give

$$v_p = \frac{(A_0K_1K_3 + K_2)v_n}{1 + GK_1K_3K_4v_n}. \tag{6.5}$$

It can be derived from Eq.(6.5) that $v_p = 0$ when A_0 set to the optimum gain value given in Eq.(6.2). However it is assumed that the initial value of the amplifier cannot be set to the optimum value because of process variation. Fortunately,

increasing the value of G will make v_p approaches zero. This shows that G will need a high-gain circuit block such as an operational amplifier. Refers to Fig.6.3, the input of the circuit block G is the residual noise v_a detected at one node inside the guard ring while its output is the gain control voltage of the VGA A_1. Since a DC bias is more preferred as the gain control voltage of the VGA, the circuit block G will also need an integrator. In order to prevent the integrator output from converging to zero value, a wave rectifier preceding the integrator is needed. As a result, the circuit block G will be given by the circuit in Fig.6.4.

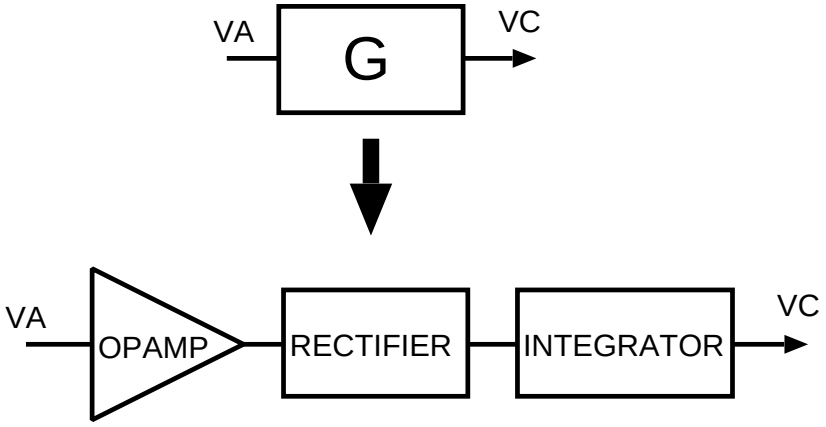

Figure 6.4: Implementation of circuit block G.

In order to calculate the integrator output, assume that the noise waveform, operational amplifier gain and the integrator transfer function are given by $V_N \sin(\omega t)$, A_v, and $1/(1+sCR)$ respectively. Here the integrator input $v_{int}(t)$ will be given by

$$v_{int}(t) = A_v |V_N \sin(\omega t)| \tag{6.6}$$

$$= \begin{cases} -A_v V_N \sin(\omega t) & (-\frac{T}{2} \le t < 0) \\ A_v V_N \sin(\omega t) & (0 \le t < \frac{T}{2}) \end{cases} \tag{6.7}$$

where $T = 2\pi/\omega$. Here the Fourier series of $v_{int}(t)$ will be given by

$$v_{int}(t) = \frac{a_0}{2} + \sum_{n=1}^{\infty} a_n \cos(n\omega t) + \sum_{n=1}^{\infty} b_n \sin(n\omega t) \tag{6.8}$$

where

$$a_0 = \frac{4}{\pi} A_v V_N \tag{6.9}$$

$$a_n = \frac{2A_v V_N}{T} \left\{ \frac{1-(-1)^{n+1}}{(n+1)\omega} - \frac{1-(-1)^{n-1}}{(n-1)\omega} \right\} \tag{6.10}$$

$$b_n = 0. \tag{6.11}$$

Note that when n is an odd number, $a_n = 0$ and for an even number $n = 2m$, a_n is

$$a_n = a_{2m} = \frac{4A_vV_N}{\pi}\frac{1}{1-4m^2}. \tag{6.12}$$

Substituting Eqs.(6.9) and (6.12) into (6.8) will give the output voltage of the integrator $v_{int}(t)$ as

$$v_{int}(t) = \frac{2A_vV_N}{\pi}\left(1 + 2\sum_{m=1}^{\infty}\frac{\cos(2m\omega t)}{1-4m^2}\right). \tag{6.13}$$

The Laplace transform of Eq.(6.13) will be given by

$$V_{INT}(s) = \frac{2A_vV_N}{\pi} \times \left(\frac{1}{s} + 2\sum_{m=1}^{\infty}\frac{1}{(1-4m^2)}\frac{s}{(4m^2\omega^2+s^2)}\right). \tag{6.14}$$

The integrator output $V_C(s)$ then can be found as

$$V_C(s) = V_{INT}(s)\frac{1}{1+sCR}. \tag{6.15}$$

Substituting Eq.(6.14) into (6.15) will give

$$\begin{aligned} V_C(s) &= \frac{2A_vV_N}{\pi}\left(\frac{1}{s}\frac{1}{(1+sCR)}\right. \\ &\quad \left. +2\sum_{m=1}^{\infty}\frac{1}{(1-4m^2)}\frac{2}{(4m^2\omega^2+s^2)}\frac{1}{(1+sCR)}\right) \end{aligned} \tag{6.16}$$

because a lossy integrator, or a 1st-order RC circuit is assumed as an integrator in Fig.6.4. This can be rewritten into

$$\begin{aligned} V_C(s) &= \frac{2A_vV_N}{\pi}\left(\frac{1}{s} - \frac{CR}{(1+sCR)}\right. \\ &\quad \left. +\sum_{m=1}^{\infty}\frac{4\left[\frac{s}{(4m^2\omega^2+s^2)} + 2m\omega CR\frac{2m\omega}{(4m^2\omega^2+s^2)} - \frac{1}{2}\frac{CR}{(1+sCR)}\right]}{(1-4m^2)(1+4m^2\omega^2C^2R^2)}\right). \end{aligned} \tag{6.17}$$

Finally, the output of the integrator can be found as the inverse Laplace transform of Eq.(6.17) as

$$\begin{aligned} v_c(t) &= \frac{2A_vV_N}{\pi}\left(1 - e^{-\frac{t}{RC}}\right. \\ &\quad \left. +\sum_{m=1}^{\infty}\frac{4\left[\cos(2m\omega t) + 2m\omega CR\sin(2m\omega t) - \frac{1}{2}e^{-\frac{t}{RC}}\right]}{(1-4m^2)(1+4m^2\omega^2C^2R^2)}\right) \end{aligned} \tag{6.18}$$

Assuming that $\omega \gg 1/(CR)$ will make the second term of Eq.(6.18) approaches zero and $v_c(t)$ becomes

$$v_c(t) \approx \frac{2A_vV_N}{\pi}(1 - e^{-\frac{t}{CR}}) \tag{6.19}$$

which is in fact the step response of the circuit in Fig.6.4. Equation (6.19) shows that the settling time of the gain control circuit can be roughly estimated by calculating its step input response. Now rewrite Eq.(6.5) as

$$v_p(t) = \frac{(A_0K_1K_3 + K_2)v_n(t)}{1 + K_1K_3K_4Gv_n(t)} \tag{6.20}$$

$$= \frac{(A_0K_1K_3 + K_2)v_n(t)}{1 + K_1K_3K_4v_c(t)}. \tag{6.21}$$

Substituting Eq.(6.19) into (6.21) will give

$$v_p(t) \approx \frac{(A_0K_1K_3 + K_2)}{1 + K_1K_3K_4\frac{2A_vV_N}{\pi}(1 - e^{-\frac{t}{CR}})}v_n(t). \tag{6.22}$$

For $t \gg 1/(CR)$, $e^{-\frac{t}{CR}} \approx 0$ and therefore the noise level at the deep portion of the substrate $v_p(t)$ is

$$v_p(t) \approx \frac{(A_0K_1K_3 + K_2)}{1 + K_1K_3K_4\frac{2A_vV_N}{\pi}}v_n(t). \tag{6.23}$$

When A_v is large enough, then Eq.(6.23) will approximately equal to zero. This result gives a proof that the active shield circuit with automatic gain scheme can effectively reduce the noise regardless of process variation.

Furthermore, investigating the transient characteristic of the gain of the VGA A_1 will give an additional explanation to the mechanism of the gain control feedback loop. Substituting Eq.(6.5) into (6.4) will give the gain of VGA as

$$A_1 = \frac{A_0 - K_2K_4Gv_n(t)}{1 + K_1K_3K_4Gv_n(t)} \tag{6.24}$$

which can be rewritten as

$$A_1(t) = \frac{A_0 - K_2K_4v_c(t)}{1 + K_1K_3K_4v_c(t)} \tag{6.25}$$

$$= \frac{A_0 - K_2K_4\frac{2A_vV_N}{\pi}(1 - e^{-\frac{t}{CR}})}{1 + K_1K_3K_4\frac{2A_vV_N}{\pi}(1 - e^{-\frac{t}{CR}})}. \tag{6.26}$$

Here when $t = 0$ then $A_1(0) = A_0$ which is the initial gain of the VGA. For $t \gg 1/(CR)$ and assume that $K_1K_3K_4\frac{2A_vV_N}{\pi} \gg 1$, then $A_1(t)$ becomes

$$A_1(t) \approx \frac{A_0}{K_1K_3K_4\frac{2A_vV_N}{\pi}} - \frac{K_2}{K_1K_3}. \tag{6.27}$$

Note that the second term of Eq.(6.27) is equal to the optimum gain value given in Eq.(6.2).

6.3 Simulation Results

HSpice simulation using a circuit model as is shown in Fig.6.5 is used to confirm the performance of the proposed system. The substrate model is given by the resistive network shown in Fig.5.10. The circuit parameters are given in Table 6.1.

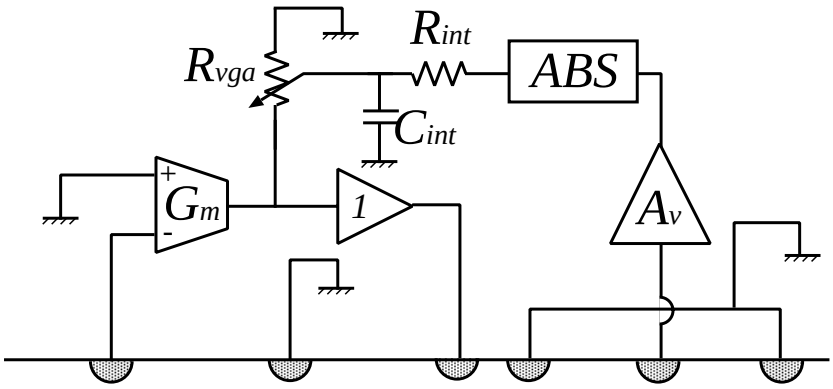

Figure 6.5: Simulated model of the proposed circuit.

Here the cutoff frequency of the integrator f_{int} and the gain of the operational

Table 6.1: Circuit parameters

Name	**Value**	
G_m	100	μS
VGA gain	-1∼0	
f_{int}	1	Hz
A_{v0}	112	dB
f_{op}	100	Hz
K_g	-2	V^{-1}

amplifier A_v are given by

$$f_{int} = \frac{1}{2\pi R_{int} C_{int}}, \tag{6.28}$$

$$A_v = \frac{A_{v0}}{1 + s/(2\pi f_{op})}, \tag{6.29}$$

and K_g is the voltage-to-gain conversion parameter of the VGA. The initial gain of the VGA is set to zero.

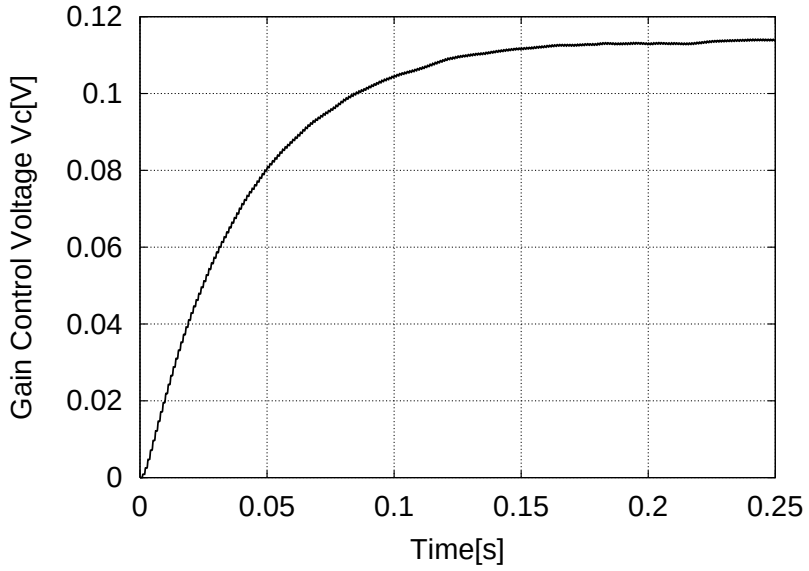

Figure 6.6: Transient characteristic of the gain control voltage V_C (sine wave $200\mu A_{p\text{-}p}$@1kHz).

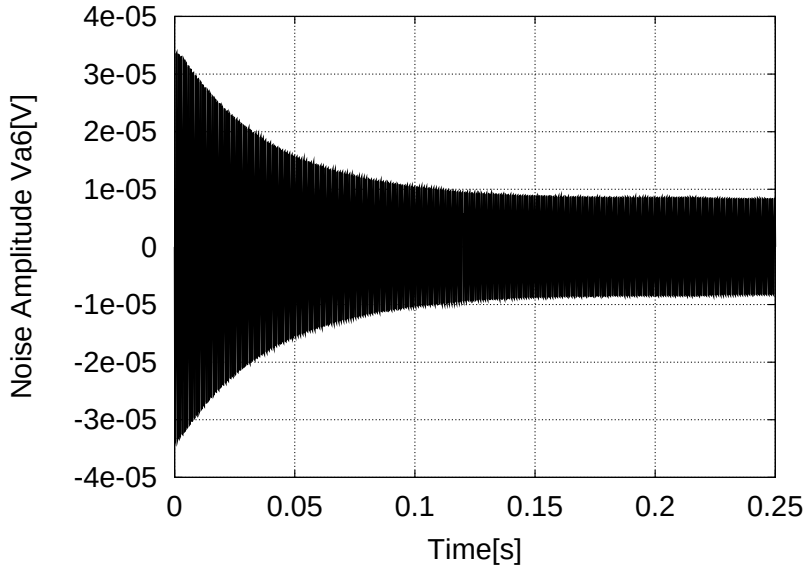

Figure 6.7: Noise level inside the guard ring observed at V_{a6} (sine wave $200\mu A_{p\text{-}p}$@1kHz).

The noise source is represented by a current source of a sine wave with an amplitude of $200\mu A_{p-p}$ at 1kHz which is injected at node $\mathbf{d}_6$. The gain control voltage V_C and the noise amplitude at node $\mathbf{a}_6$ are observed. The results are shown in Figs.6.6 and 6.7 respectively. After the system is settled, the noise amplitude is 17μV while the noise amplitude without active shield circuit is 83μV. This means a noise reduction ratio of 14dB is achieved when the active shield circuit is used.

In an actual mixed-signal ICs there are multiple noise sources with different amplitudes. Figure 6.8 shows the circuit model to simulate this case. Here i_{n1}, i_{n2}, and i_{n3} are given by 1kHz sine waves with amplitudes of 200μA, 300μA, and 400μA respectively. The result is shown in Fig.6.9. It shows that the control voltage V_C keep tracking the change of noise source position and amplitude. As a result, the noise amplitude V_{a6} is kept small although it increases slightly at the transition period of the VGA gain.

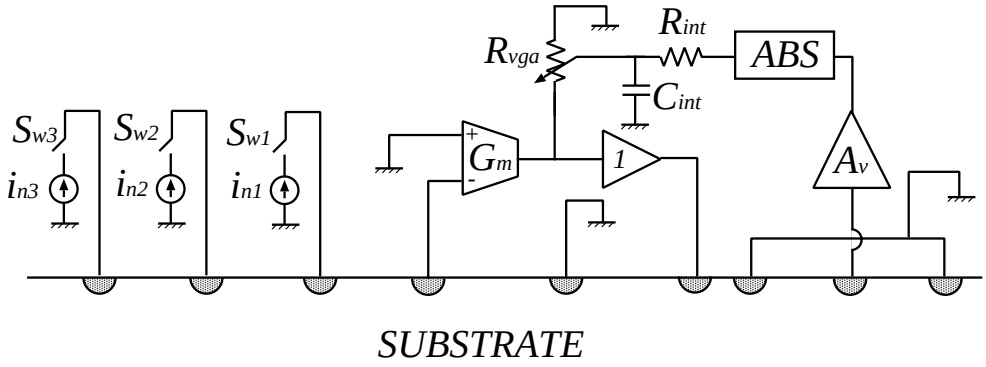

Figure 6.8: Active shield circuit model with multiple noise sources.

Table 6.1 shows that the cutoff frequency of the integrator is set to 1Hz. Although it may depend on the implementation of the integrator, a large capacitance might be required and thus consumes chip's area. Let the ratio between the cutoff frequency of the integrator f_{int} and the frequency of the noise f_n be m. The transient characteristics of the automatically controlled active shield circuit for different m values are shown in Fig.6.10. Here m is varied from 10 to 10000 and the noise frequency is 1MHz. It shows that the active shield circuit converges even if the cutoff frequency of the integrator is only one tenth of the noise frequency. Equation (6.18) shows that the gain control voltage of the active shield circuit V_C contains the noise component whose amplitude is inversely proportional to the value of m. Thus the fluctuation of V_C will increase for smaller m values. As a result the gain of the active shield circuit will vary and the noise suppression performance is degraded. However Fig.6.10 shows that the noise level does not increase much for small m. The reason is that the voltage-to-gain conversion pa-

rameter of the active shield circuit is small and thus the fluctuation of the gain control voltage will not cause a great variation of the gain.

6.4 Conclusions

The noise suppression performance of the proposed active shield layout in Fig.5.4 is found to have a high dependency on the gain of the active shield circuit. An automatic gain control scheme is applied in order to obtain an optimum gain which will give a proper noise suppression performance without a priori knowledge of substrate resistances. The proposed active shield circuit with automatic gain control gives an improvement on the noise suppression performance of 14dB compared to the guard ring.

The behavior of the proposed system under the condition of multiple noise sources is also simulated. The proposed circuit shows capability to track change in noise source position and amplitude as well. A consideration on the relation between the integrator cutoff frequency and the noise frequency is also examined in order to ease the design requirement of the proposed system. As a result the cutoff frequency of the integrator can be set as high as one tenth of the noise frequency without causing any significant degradation in the noise suppression performance.

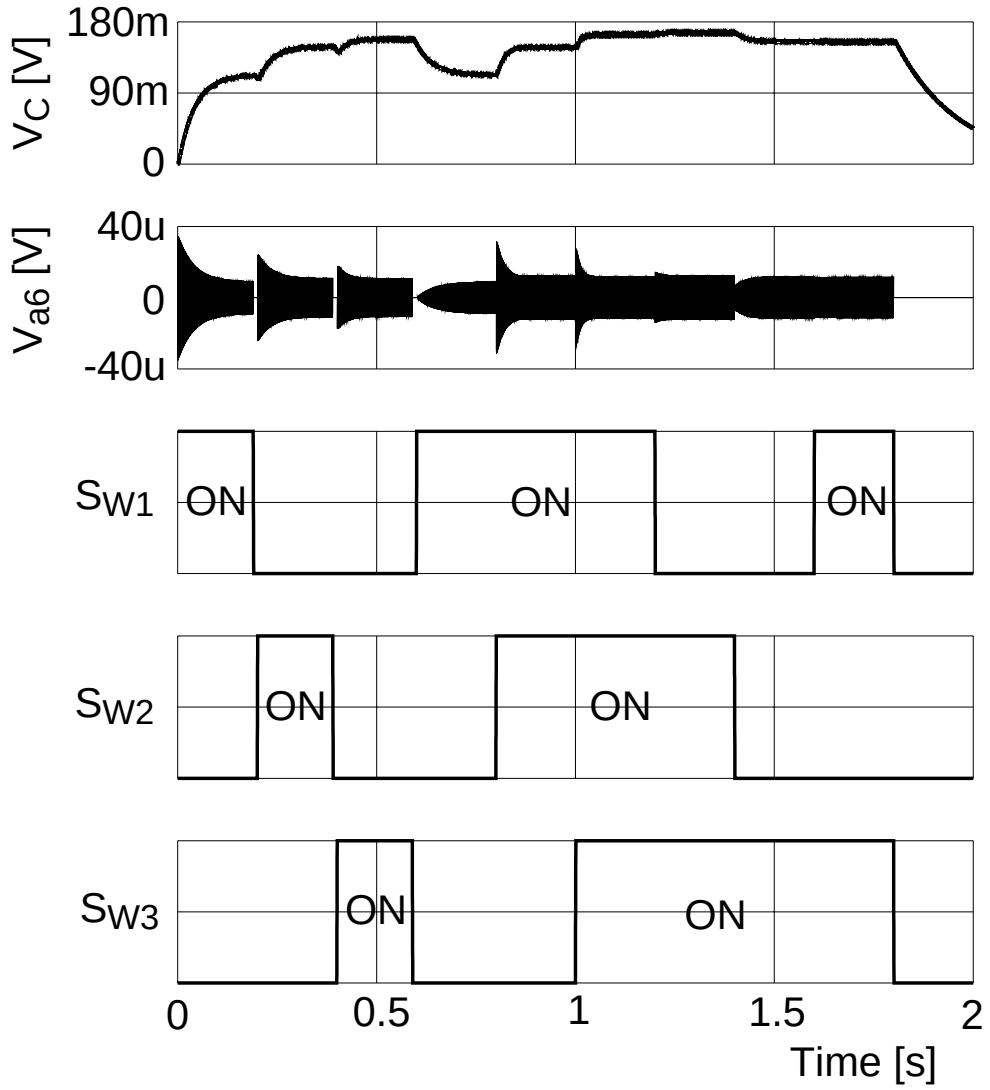

Figure 6.9: Active shield circuit model with multiple noise sources.

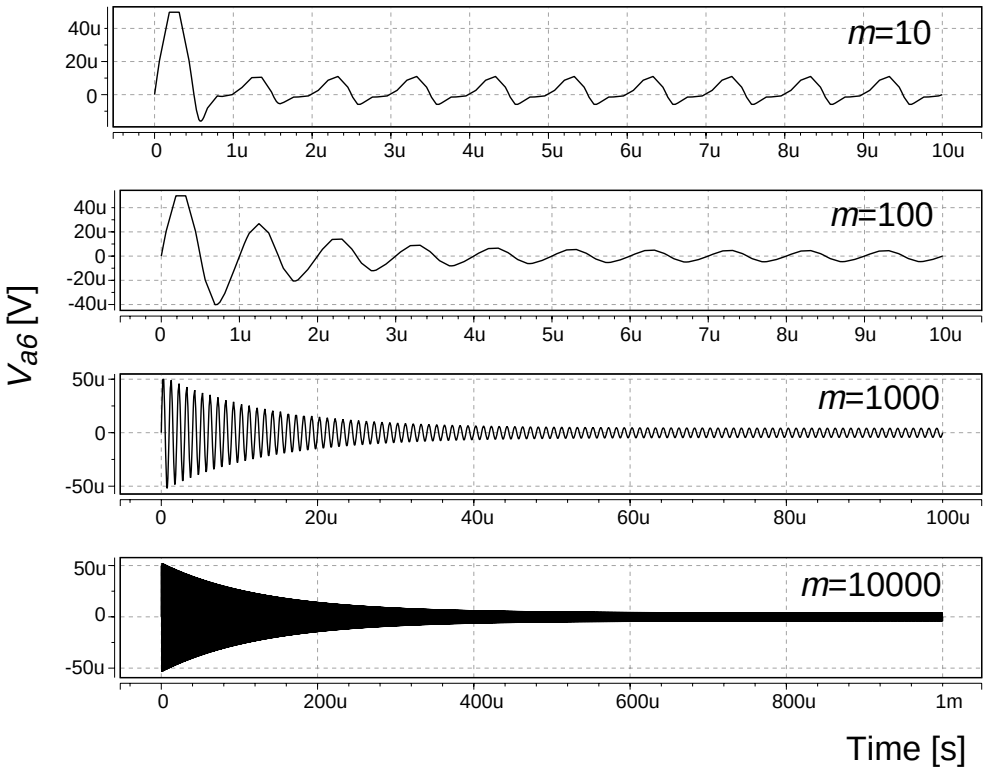

Figure 6.10: Transient characteristics of the active shield circuit for different integrator's cutoff frequencies.

Chapter 7

General Conclusions

Various substrate noise suppression techniques are discussed. A commonly used passive guard ring effectively reduces the noise transfered through the surface of a substrate. However it cannot reduce the noise coupled through the deep portion of a substrate. Noise suppression using active shield circuit is proposed as a solution to reduce the noise coupled through the deep portion of the substrate on a standard double-well CMOS process.

The earlier active shield circuits are either implemented off-chip or need external components. This is not preferable that the substrate noise is once brought out of the chip because it may affect other devices. The integration of the active shield circuit is enabled by the use of the proposed DC offset technique. The validity of the proposed technique is confirmed by both simulations and measurements. Measurement results show that the active shield circuit gives a noise suppression performance of about 25dB or in other words the noise is reduced to approximately 5% of its original amplitude.

The simulation using substrate model which considers the area of digital and analog circuits shows that the active shield circuit implemented using an inverter with a gain of -1 is no longer valid. A design methodology for the active shield circuit by evaluating the average noise transfer function is proposed. The simulation results show that the active shield circuit with optimized gain gives a lower average noise transfer function than the one with gain of -1. The improvement is found to be as large as 28% for noise sources near the guard ring to 10% for noise sources far from the guard ring. The noise suppression improvement for noise sources far from the guard ring is smaller, however it will not be a great matter since the farther the noise source is the noise amplitude when it reached analog bulk will become smaller.

The conventional layout of the active shield circuit is found to be effective only for a narrow area inside the guard ring. A new layout based on the principle of noise cancellation before it reaches analog bulk is proposed. Analysis results show that the proposed layout is capable of reducing the noise on the entire area inside the guard ring. A brief estimation on the dominant pole of the proposed

active shield circuit is performed. The dominant pole position is kept constant by applying a bias that does not depend on the gain of the circuit. The proposed active shield layout provides a noise suppression improvement of more than 30dB compared to a passive guard ring. The layout of the proposed active shield circuit should be chosen carefully in order to keep the optimum gain of the amplifier as low as possible and thus gives a possibility for speed improvement.

The noise suppression performance of the proposed active shield layout highly depends on the gain of the active shield circuit. An automatic gain control scheme is proposed in order to tune the gain of the active shield circuit and to obtain a proper noise suppression regardless of substrate resistances. Simulation results show that the proposed system gives a noise suppression performance of 14dB or more compared to that of passive guard ring. The behavior of the proposed system under the condition of multiple noise sources is also simulated. The proposed circuit shows capability to track change in noise source position and amplitude as well. A consideration on the relation between the integrator cutoff frequency and the noise frequency is also examined in order to ease the design requirement of the proposed system. As a result the cutoff frequency of the integrator can be set as high as one tenth of the noise frequency without causing any significant degradation in the noise suppression performance.

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Publications Related to This Dissertation

Papers

1. S. Takagi, R.A. Nicodimus, K. Wada and N. Fujii, "Fully on-chip active guard band circuit for digital noise cancellation," IEICE Trans. Fundamentals, Vol.E85-A, No. 2, pp.373-380, Feb 2002.

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