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PAPER

Design of Wave Digital Filters with Simplified Structures

Eiji WATANABE† *and* Akinori NISHIHARA†, *Members*

SUMMARY In the design of digital filters, it is desirable to achieve lower sensitivity. Wave digital filters (WDF's) are considered one solution to this problem, and two design approaches have been proposed. However, WDF's have complicated structures compared with conventional ones. This will make it difficult to implement WDF's. The aim of this paper is to reduce the difficulty owing to the complexity of the network structures. Two kinds of simplification techniques are presented. One is to reduce the number of adders. For this purpose, new series and parallel sections and a new port matching scheme are proposed. The other is to construct WDF's using identical 3-port adaptors except the one to match the port resistance. Examples of WDF's with proposed structures are provided and the effectiveness of the proposed techniques is also shown.

1. Introduction

In the design of digital filters, it is desirable to achieve lower sensitivity, because lower sensitivity filters can realize the same performance with shorter word length, and can realize better performance with the same word length.

One solution to this problem is to simulate the wave flow of analog distributed filters. The resultant so-called wave digital filters (WDF's) are known to inherit the low sensitivity property of the reference filters. So far two design methods have been proposed. The original technique introduced by Fettweis[1] uses "adaptors", which are connected with the delay units corresponding to inductors and capacitors. The early WDF's can only simulate cascaded unit element filters and the distributed filters which have unit elements between stub elements, in order to avoid delay free loops. After that, they proposed the new adaptors with reflection free ports[2].

The alternative approach was proposed by Constantinides[3] and Swamy and Thyagarajan[4]. Later, it was generalized by Erfani and Peikari[5], using the concept of the generalized delay unit (GDU).

In spite of many favorable features, WDF's have complicated structures compared with conventional ones such as cascade realizations. This will increase the program steps in the implementation on digital signal processors (DSP's), and will restrict the realizable order of WDF's.

The aim of this paper is to propose a design method to reduce the restriction due to the complexity of the network structure. The simplification of network structures is considered, involving the reduction of the number of adders and the synthesis using identical 3-port adaptors. At first, new digital series and parallel sections are proposed,

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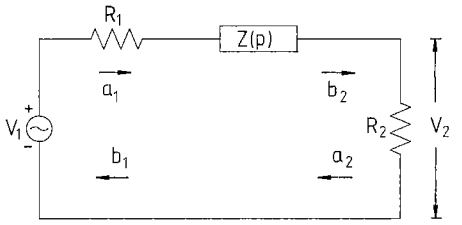


Fig. 1 Analog series section.

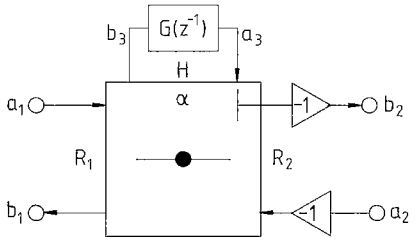


Fig. 2 Digital series section.

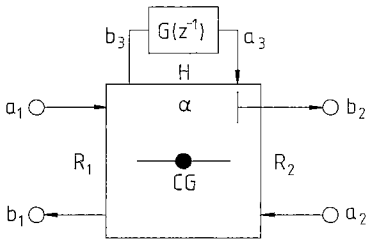


Fig. 3 Series section represented by series CG-adaptor.

which contain fewer adders than the conventional ones. Each section consists of an adaptor and a GDU. In the series section, a new series adaptor, named "series CG-adaptor", is introduced instead of Fettweis' one. Since the new sections consist of adaptors and GDU's, they are the general forms between the two methods mentioned above. This generalization also gives the physical interpretation of GDU's which were introduced arithmetically. The new Erfani and Peikari's sections[7], which do not use the concept of GDU, have the same structures as two of the new sections proposed in this paper. But the sections proposed here seem to be more flexible, because GDU's can simulate general LC one-port structures. The choice of the port matching scheme also affects the number of adders. The effective scheme is shown.

After the first simplification, equivalent transformations of adaptors are introduced to form a series section using a

parallel adaptor in place of a series CG-adaptor and vice versa. Further, equivalent transformations of multiplier movement are presented. These two transformations enable one to design a WDF using identical 3-port adaptors.

Design procedure and examples are presented, and the effectiveness of the proposed techniques are shown in Section 7.

2. New Series and Parallel Sections

The scattering matrix of a series section in the z-domain is given by

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \frac{1}{1-\alpha G(z^{-1})} \begin{bmatrix} 1-\alpha & \alpha\{1-G(z^{-1})\} \\ 1-G(z^{-1}) & (1-\alpha)G(z^{-1}) \end{bmatrix} \cdot \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} \tag{1}$$

where $G(z^{-1})$ is the GDU and defined as follows[5]:

$$H = Z(p)\,|_{p=1} \tag{2}$$

$$Z(z^{-1}) = H\frac{N(z^{-1})}{D(z^{-1})} \tag{3}$$

$$G(z^{-1}) = \frac{N(z^{-1}) - D(z^{-1})}{N(z^{-1}) + D(z^{-1})} . \tag{4}$$

The continuous domain counterpart of this section is shown in Fig. 1. The correspondence of variable "z" with Richards' variable "p" is given by bilinear transformation. The relation between port resistances R_1 and R_2 is given by

$$R_2 = R_1 + H . \tag{5}$$

In this case, the multiplier coefficient is given by

$$\alpha = \frac{R_1}{R_2} . \tag{6}$$

The scattering matrix (1) can be realized as a combination of a Fettweis' 3-port series adaptor and a GDU shown in Fig. 2[6]. Two inverters and one adaptor in Fig. 2 are combined into one adaptor named "series CG-adaptor" as shown in Fig. 3 and its internal circuit is shown in Fig. 4. Figs. 1 and 3 show that the new series section simulates the wave quantity of the analog series section with the common ground. Therefore, it is convenient for the simulation of LC ladder filters.

In the same way as the series section, the scattering matrix of a parallel section in the z-domain is given by

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \frac{1}{1+\alpha G(z^{-1})} \begin{bmatrix} \alpha - 1 & 1+G(z^{-1}) \\ \alpha\{1+G(z^{-1})\} & (1-\alpha)G(z^{-1}) \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} \tag{7}$$

and can be realized as a combination of a 3-port parallel adaptor and a GDU as shown in Fig. 5. The internal circuit of the parallel adaptor is given in Fig. 6. The relation of port

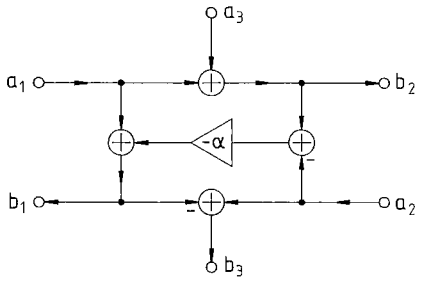


Fig. 4 Internal circuit of series CG-adaptor.

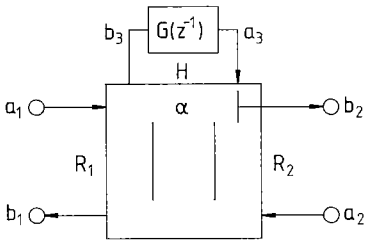


Fig. 5 Parallel section.

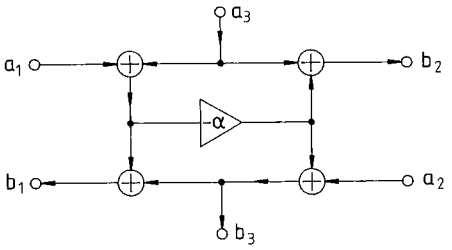


Fig. 6 Internal circuit of parallel adaptor.

Table 1 Example of GDU's.

Z(P)	G(z⁻¹)
C H = 1/C	Z⁻¹ G(z⁻¹) = z⁻¹
L H = L	Z⁻¹ -1 G(z⁻¹) = -z⁻¹
L C H = (1 + LC)/C β = (1 - LC)/(1 + LC)	Z⁻¹ Z⁻¹ β G(z⁻¹) = z⁻¹ (β + z⁻¹)/(1 + βz⁻¹)
C L H = L/(1 + LC) β = (1 - LC)/(1 + LC)	Z⁻¹ -1 Z⁻¹ β G(z⁻¹) = -z⁻¹ (β + z⁻¹)/(1 + βz⁻¹)

resistances is given by

$$\frac{1}{R_2}=\frac{1}{R_1}+\frac{1}{H} \tag{8}$$

and the multiplier coefficient is given by

$$\alpha=\frac{R_2}{R_1} \tag{9}$$

Table 1 shows the circuit realization of the GDU's corresponding to some reactance 1-port networks.

Here, the new sections proposed above are compared with the conventional circuits. Both the series CG-adaptor and the parallel adaptor contain four adders, while Erfani and Peikari's section excluding a GDU needs five adders. Thus, the new sections contain fewer adders than Erfani and Peikari's ones. In the digital simulation of resonant circuits, a second order GDU has two adders as shown in Table 1, while Fettweis' realization uses one 3-port adaptor and two delay units. This means that the new sections can construct WDF's with fewer adders than Fettweis' configurations. New Erfani and Peikari's sections[7] consist of an adaptor and a delay unit, and new circuit configurations are similar to Fettweis' ones. Therefore, the new sections proposed in this paper require smaller numbers of adders than the conventional sections and enable one to design WDF's with fewer adders.

Both sections mentioned here have no delay free path in S_{22}. The other types of the sections which have no delay free path in S_{11} and have delay free paths in both S_{11} and S_{22} can also be realized in a similar manner.

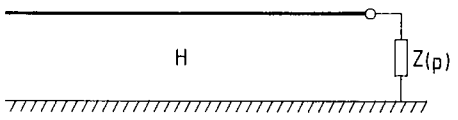
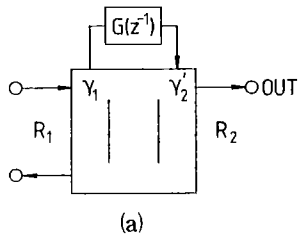


Fig. 7 Representation of GDU in analog domain.



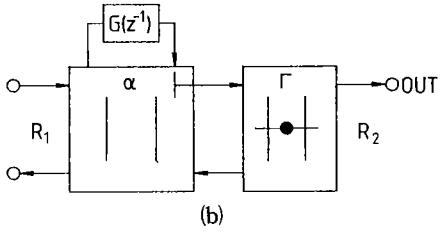


Fig. 8 Conventional port matching scheme.
(a) Using a 3-port parallel adaptor.
(b) Using a 2-port adaptor.

3. Physical Interpretation of GDU's

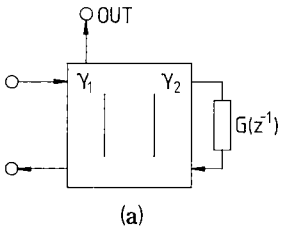
Since the new sections have been constructed by the adaptors and GDU's, it becomes possible to consider the physical meaning of GDU's. Section 2 shows that they are connected with the adaptors at the port 3 which has port resistance H given by Eq. (1). Therefore, it can be said that GDU is the digital-domain simulation of the reflection coefficient which is measured at the connecting point between $Z(p)$ and the semi-infinite length transmission line with characteristic impedance H as shown in Fig. 7. This can also be proved by modifying (4) as

$$G(z^{-1})=\frac{Z(z^{-1})-H}{Z(z^{-1})+H} \tag{10}$$

If Richards' theorem is applied to $Z(p)$, the characteristic impedance of the first extracted unit element is H due to Eq. (2). When such $Z(p)$ is connected to the semi-infinite transmission line with characteristic impedance H, direct reflection of waves does not occur at the connecting point. Hence, $G(z^{-1})$ is a allpass function which has always delay, and represented as

$$G(z^{-1})=\pm z^{-1}\frac{a_n+a_{n-1}z^{-1}+a_{n-2}z^{-1}+\cdots+z^{-1}}{1+a_1z^{-1}+a_2z^{-1}+\cdots+a_nz^{-1}}. \tag{11}$$

Table 1 shows the direct form realization of GDU's.



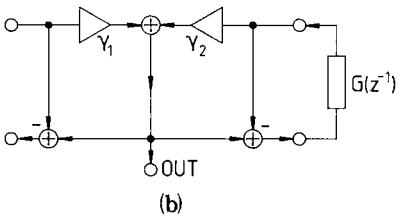


Fig. 9 (a) New port matching scheme.
(b) Its internal circuit.

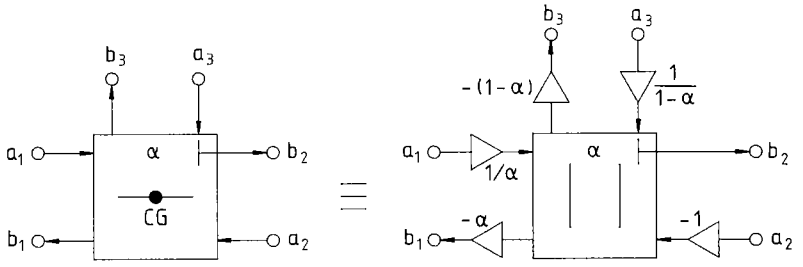


Fig. 10 Equivalent arrangement between series CG-adaptor and parallel adaptor.

In addition, other circuit realizations of GDU's exist corresponding to each synthesis of reactance function $Z(p)$. Fettweis' circuits are considered to realize GDU's using 3-port adaptors.

4. Port Matching Scheme

In the design of wave digital filters, port resistances of two neighboring ports should be equal. If those sections mentioned above are used to simulate LC ladder filters, each port resistance is related by Eqs. (5) and (8). In order to match port resistances of all neighboring ports, one section should be free from such relation. This port matching is achieved by using the sections which have delay free paths in both ports. Two port matching schemes have usually been used to realize such sections. One is to use the 2-port adaptor [8], and the other is to use the 3-port adaptor without a reflection-free port [9]. If an output section is a parallel section and a port matching scheme is used there, a simpler scheme exists. The conventional circuit using a 3-port parallel adaptor and a 2-port adaptor are shown in Figs. 8(a) and (b) respectively. The new scheme is obtained by exchanging the roles of the port 2 and 3 of Fig. 8(a) as shown in Fig. 9.

The multiplier coefficients are given by

$$\gamma_1 = \frac{2HG}{H(G_1+G_2)+1} \tag{12}$$

$$\gamma_2 = \frac{2}{H(G_1+G_2)+1} \tag{13}$$

where G_1 and G_2 simply $1/R_1$ and $1/R_2$ respectively.

Figure 9 contains only three adders excluding ones contained in the GDU, while both Figs. 8(a) and (b) have five adders. Therefore, it is found that the new port matching scheme needs fewer adders than the conventional schemes.

5. Equivalent Transformation of Adaptors

In the previous sections, the first simplification has been obtained. Then, this and the following sections deal with the second simplification. It is attained by constructing WDF's with identical 3-port adaptors except for the matching section. High modularity of such WDF's is quite favorable for the implementation both by software and by hardware. First of all, the equivalent transformations of adaptors to make up the series section with a parallel adaptor and vice versa are considered.

These transformations are derived by making use of the equivalent arrangement between an n-port series adaptor and an n-port parallel adaptor introduced by Fettweis and Meerkötter[9]. Applying their arrangement to the 3-port adaptor with some modifications, Figure 10 is obtained. Next, replacing the adaptor in Fig. 3 by its equivalences, then Fig. 11 is obtained.

Similarly, the inverse arrangement of Fig. 10 can be derived, and then the parallel section is realized using a series

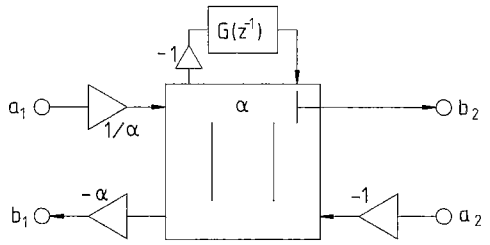


Fig. 11 Series section with a parallel adaptor.

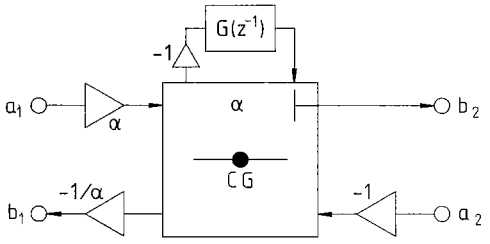


Fig. 12 Parallel section with a series CG-adaptor.

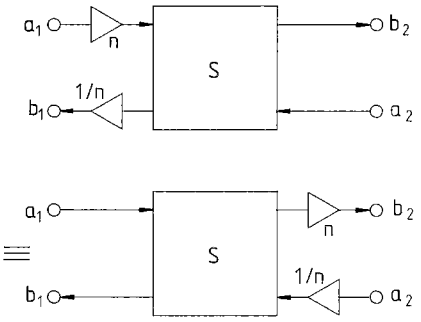


Fig. 13 Transformation of multiplier movement.

CG-adaptor as shown in Fig. 12.

Since the pair multipliers of Fig. 11 and Fig. 12 are the WDF representations of gyrators [10], these transformations correspond to the equivalent transformations using gyrators in the analog domain.

The alternative approach to derive these transformations is achieved by modifying the scattering matrices of Eqs. (1) and (7). For example, Eq. (7) can be modified as

$$\begin{bmatrix} -\alpha b_1 \\ b_2 \end{bmatrix} = \frac{1}{1-\alpha\{-G(z^{-1})\}} \begin{bmatrix} 1-\alpha & \alpha[1-\{-G(z^{-1})\}] \\ 1-\{-G(z^{-1})\} & (1-\alpha)\{-G(z^{-1})\} \end{bmatrix} \begin{bmatrix} \alpha a_1 \\ -a_2 \end{bmatrix} \tag{14}$$

Since Eq. (14) has the same form as Eq. (1), the parallel section is found to be built using a series CG-adaptor as

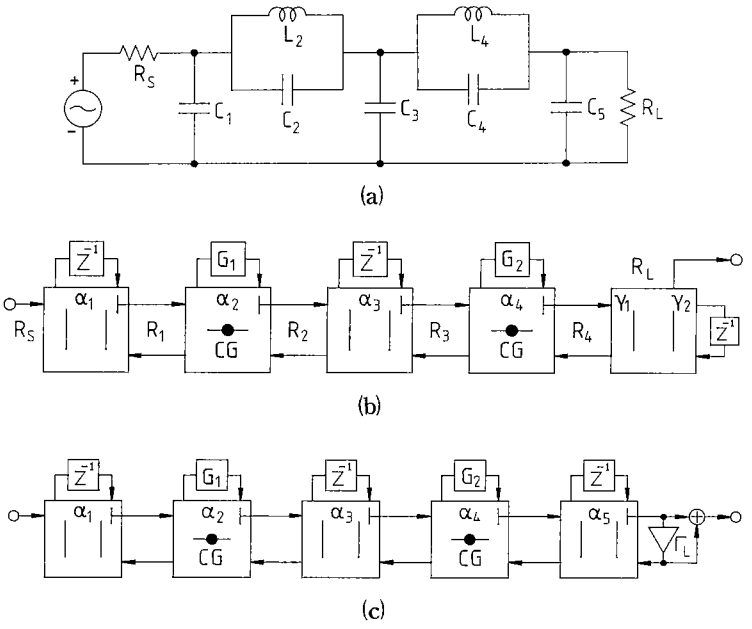


Fig. 14 Example of WDF's using new series and parallel sections.
(a) Analog prototype filter.
(b) WDF with new matching section.
(c) WDF with 2-port adaptor matching section.

shown in Fig. 12.

6. Equivalent Transformations of Multiplier Movement

Making use of the transformation of the previous section, it is possible to construct WDF's with identical 3-port adaptors. For example, combining the circuits of Figs. 3 and 12 leads to the WDF with series CG-adaptors only. In such circuits, some extra multipliers are added corresponding to gyrators in the analog domain.

In order to reduce the number of multipliers, the equivalent transformations of multiplier movement are used. If a digital 2-port network is given by

$$\begin{bmatrix} n\,b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} n a_1 \\ a_2 \end{bmatrix}, \tag{15}$$

it can be rewritten as

$$\begin{bmatrix} b_1 \\ b_2/n \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2/n \end{bmatrix}. \tag{15'}$$

Signal flow graph representation of Eqs. (15) and (15)' is shown in Fig. 13. The multipliers at one port can be moved to the other port.

In a similar manner, other transformations can be obtained[11]

Since the pair multipliers of Fig. 13 are the WDF representations of ideal transformers, this transformation is corresponding to the equivalent transformation using ideal transformers in the analog domain.

When internal variables are scaled to prevent overflow[12], these transformations are used to insert scaling multipliers instead of moving the additional multipliers mentioned above. Each additional multiplier is combined with a scaling multiplier to form one multiplier.

Table 2 The number of adders.

Fig. 14(b)	Fig. 14(c)	Sedlmeyer & Fettweis	Erfani & Peikari
22	24	28	29

7. Design Example

In this section design examples of WDF's with simplified structures are presented. A 5th order elliptic lowpass filter shown in Fig. 14(a) is selected to be an analog prototype filter. Using the fundamental sections of Figs. 3 and 5, wave quantity of it is simulated in the z-domain as shown in Fig. 14(b), where the new port matching scheme is used at the output section. The multipler coefficients of the circuit are as follows;

$$\frac{1}{R_1} = \frac{1}{R_s} + C_1, \quad \alpha_1 = \frac{R_1}{R_s} \tag{16a}$$

$$R_2 = R_1 + \frac{L_2}{1 + L_2 C_2}, \quad \alpha_2 = \frac{R_1}{R_2} \tag{16b}$$

$$G_1(z^{-1}) = -z^{-1}\frac{\beta_1 + z^{-1}}{1 + \beta_1 z^{-1}}, \quad \beta_1 = \frac{1 - L_2 C_2}{1 + L_2 C_2} \tag{16c}$$

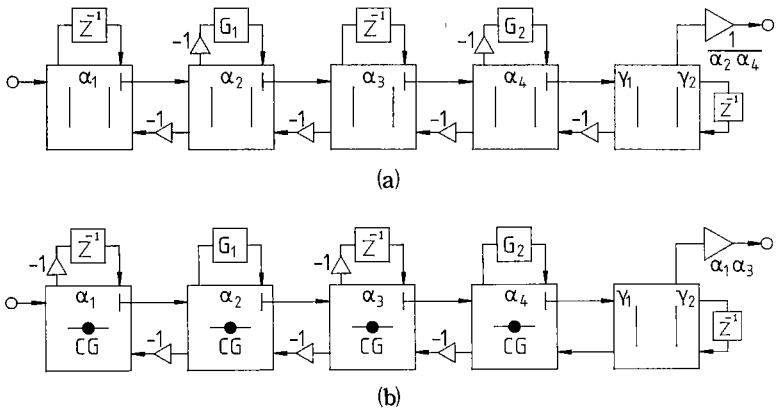


Fig. 15 (a) WDF with identical parallel adaptors.
(b) WDF with identical series CG-adaptors.

$$\frac{1}{R_3}=\frac{1}{R_2}+C_3\,,\quad \alpha_3=\frac{R_3}{R_2} \tag{16d}$$

$$R_4=R_3+\frac{L_4}{1+L_4C_4}\,,\quad \beta_2=\frac{R_3}{R_4} \tag{16e}$$

$$G_2(z^{-1})=-z^{-}\frac{\beta_2+z^{-1}}{1+\beta_2 z^{-1}}\,,\quad \beta_2=\frac{1-L_4C_4}{1+L_4C_4} \tag{16f}$$

$$\gamma_1=\frac{2R_L}{R_4+R_L+R_4R_LC_5} \tag{16g}$$

$$\gamma_2=\frac{2R_4R_LC_5}{R_4+R_L+R_4R_LC_5} \tag{16h}$$

In addition, Fig. 14(c) shows the WDF using the conventional port matching scheme by a 2-port adaptor.

Now, the numbers of digital elements of Fig. 14 are compared with Sedlmeyer and Fettweis' circuit[2] and Erfani and Peikari's one with GDU's[5]. Each circuit derived from the same prototype of Fig. 14(a) contains seven delay units and eight multipliers. The numbers of adders are given in Table 2.

It is found from Table 2 that the circuit of Fig. 14(b) contains fewer adders than others, and thus the first simplification has been achieved.

Secondly, Fig. 14(b) is transformed into the WDF with identical 3-port adaptors except for the matching section. Replacing the series sections of Fig. 14(b) by Fig. 11, the new circuit is obtained with two additional multipliers. In order to move these multipliers to the output port, the equivalent transformation of Fig. 13 is applied. As a result, the circuit of Fig. 15(a) is obtained, which contains four identical 3-port parallel adaptors. Then second simplification has been attained. In this case, the additional multiplier at the output port affects the gain level only. Similarly the circuit using four series CG-adaptors can also be constructed and is shown in Fig. 15(b).

Table 3 shows the numbers of program steps, which are required to implement the WDF's of Figs. 14(b), 14(c), 15(a) and 15(b) on NEC's μPD7720 signal processor. The

Table 3 The number of program steps.

	program step
Fig. 14(b)	39
Fig. 14(c)	40
Fig. 15(a)	34
Fig. 15(b)	33

number of program steps is related to the program size which decides the program memory area.

It is found from Table 3 that the number of program steps of Figs. 15(a) and (b) is compressed compared with others. The programs of WDF's with identical 3-port adaptors contain only one subroutine describing adaptors, while others contain two subroutines. This makes it possible to make shorter programs. Therefore, it can be said that complexity is reduced in such structures.

8. Conclusion

This paper has presented the design of wave digital filters with simplified structures. Two kinds of the simplification techniques have been proposed. The first method is to reduce the number of adders. It is attained by introducing the new series and parallel sections and the new port matching scheme. The new sections are constructed by the adaptors and GDU's, and therefore can be considered the general representation of these sections. On the other hand, the new port matching scheme is based on the 3-port parallel adaptor without reflection free port, and can be applied to the output section. The use of these circuits enables one to design WDF's using fewer adders than conventional structures.

The second method is to form WDF's using identical 3-port adaptors except for the one to match the port resistance. Thus the higher modularity is achieved.

Examples of the implementation of the proposed structures on DSP has shown the effectiveness of the proposed

techniques.

The structure simplification of C- and D-sections still remains to be studied.

Acknowledgement

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