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SMAFTI Packaging Technology for New Interconnect Hierarchy

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Abstract
We have developed a 3-D packaging technology called SMAFTI (SMArt chip connection with FeedThrough Interposer), which enables the implementation of a new memory/logic-interconnect hierarchy. Through experiments, we were able to confirm practical performance of this technology. We implemented a new die bonding process and the multilayer interconnect technology to form over a thousand parallel interconnects between memory and logic dies. Implementation of the new process was achieved with high productivity and low process costs. We characterized the interlaminar horizontal wiring by S-parameter measurement up to 40 GHz and confirmed its potential for high-speed signal transmission at over 10 Gb/s.

Introduction
Due to a dramatic increase in parallelism in computer architecture, a new interconnect system for logic and memory semiconductor devices is needed to satisfy the demand for explosive expansion of memory bandwidth. 3-D die stacking with 2-D interconnects in parallel is the most natural way to form highly-parallel interconnects between memory and logic; however 3-D integration of planar circuits on silicon substrates is problematic in terms of providing power to and exchanging I/O signals with the devices in the external system. SMAFTI packaging technology[1-3] features interlaminar horizontal wiring layers between memory and logic devices, called the FTI (Feedthrough Interposer). The FTI consists of Cu/PI (Polyimide) and includes high-density feedthrough vias and interlaminar horizontal wiring with a line width of about 10 μm. This structure enables highly-parallel die-to-die communication and power/signal transmission from/to the external system. The on-chip interconnects and FTI form a new interconnect hierarchy that provides massive memory bandwidth. This hierarchy can also eliminate an excess number of TSVs (Through Silicon Vias)

and standardize TSV locations in stacked memories.

From the viewpoint of practical use of this technology, a higher throughput assembly process is an important factor in reducing manufacturing costs. SMAFTI packaging technology employs wafer-level processes except die-to-wafer bonding, so development of a highly productive bonding process is a key point in achieving large-scale production.

Clarifying the high-frequency electrical characteristics of the interlaminar horizontal wiring is also important because the 3-D integrated devices with the highest processing power require a higher I/O bandwidth for communicating with the external system. Consequently, a signal transmission capability of over 10 Gb/s will be needed for the interconnect.

Highly-Parallel Vertical Interconnect
A new SMAFTI packaging process using a multilayer FTI and metal/adhesive simultaneous bonding was developed to enable practical use of this technology. The memory-TEG (Test Element Group) and logic-TEG dies shown in Table I were used for this experiment. All packaging processes were carried out at the wafer level, as shown in Fig. 2.

First, an FTI with two metal wiring layers was formed on a supporting wafer. Photolithography and planarization processes for the electroplated Cu and spin coated PI were used to fabricate a fine multilayer FTI. Cu pillars capped with Sn-Ag solder were plated on the TEG dies as bonding electrodes at a pitch of 50 μm, and the die surfaces, including the Cu pillars, were coated by epoxy-based adhesive at the

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Fig. 1: Concept and structure of new memory/logic-interconnect hierarchy used in SMAFTI packaging technology.
wafer level using a NCF (Non Conductive Film) lamination process.

Singulated memory-TEG dies were aligned and temporarily bonded onto the FTI-formed-wafer by a flip chip bonder using an on-chip adhesive. After temporary bonding, a thermo-compression process was used to form a solder connection between the Cu pillars and FTI pads in the melted adhesive resin. After metallic bond formation, the adhesive was cured. The thermo-compression process can be executed in the block or at the wafer level to achieve high throughput.

The memory-TEG dies on the FTI-formed-wafer were encapsulated by a wafer molding technique. Removal of the supporting wafer from the resin-wafer resulted in a resin-wafer with an exposed FTI and embedded memory-TEG dies. The logic-TEG dies were also bonded in the same way on the resin-wafer.

Fig. 3 shows a cross-sectional view of the die-to-die interconnect and interlaminar horizontal wiring. Fig. 4 shows a cross-sectional SEM (Scanning Electron Microscopy) image of the die-to-die interconnect section. The number of interconnects was 1,296 per die, and all interconnects passed an electrical test.

Table I  Specifications of TEG dies and package

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<tr>
<td>Memory-TEG Die size</td>
<td>10 mm × 10 mm × 550 μm</td>
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<tr>
<td>Number of Cu pillars</td>
<td>1,424</td>
</tr>
<tr>
<td>Logic-TEG Die size</td>
<td>7.0 mm × 6.3 mm × 120 μm</td>
</tr>
<tr>
<td>Number of Cu pillars</td>
<td>2,076</td>
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Dense-Serial Horizontal Interconnect

The high-speed signal transmission capability of the interlaminar horizontal wiring in the FTI was evaluated using transmission line patterns on test vehicles. G-S-G type coplanar transmission lines were designed and placed at the "on-die area", "off-die area", and "die-edge crossing" locations shown in Fig. 5, based on the assumed real situation shown in Fig. 6. They were designed to have a characteristic.
We developed SMAFTI packaging technology for highly-parallel memory/logic communication, which uses a new high-throughput interconnection process. We measured scattering parameters of the interlaminar horizontal wiring up to 40 GHz and confirmed its great potential for signal transmission at over 10 Gb/s in on-die and off-die areas and through transitions between those areas.

**Conclusion**

The authors would like to thank Professor T. Sato, Professor N. Ishihara, and Dr. H. Ito of Tokyo Institute of Technology for their helpful discussions and suggestions in planning the high-frequency characterization of interlaminar horizontal wiring.

**References**