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Loss Reduction of Si Wire Waveguide Fabricated by Edge-Enhancement Writing for Electron Beam Lithography and Reactive Ion Etching using Double layer Resist Mask with C₆₀

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Loss reduction methods of single-mode photonic wire in Silicon on Insulator have been investigated. with Si core 200×440 nm size, fabricated with electron beam lithography and dry etching using double layer of EB resist mask. The propagation loss of TE mode measured at a wavelength of 1550 nm was 4.5 dB/cm, which is, to the best of our knowledge, the lowest value among the Si wire waveguides fabricated by parallel plate RIE method.

[DOI:]

KEYWORDS: silicon photonics, reactive ion etching, electron beam lithography, silicon on insulator, fullerene(C₆₀), line edge roughness

A silicon on Insulator (SOI) substrate is of prime importance for optoelectronic integrated circuits as it offers potentiality for monolithic integration of optical and electronic functions on a single substrate¹⁾. The silicon is transparent at wavelengths longer than 1.1 μm and can be used for waveguide at telecommunication wavelengths. A Si wire waveguide based on the SOI has the high refractive index difference between the silicon core (the refractive index is 3.45) and the buried oxide (BOX) layer (the refractive index is 1.44), inducing strong optical confinement in the silicon core layer. It allows to reduce the waveguide size to sub-micrometer to provide single-mode propagation at a wavelength of 1.55 μm. Therefore, Si wire waveguides enable us to make smaller and high density optical circuits. In such narrow waveguides, a scattering loss due to sidewall roughness is severe. Therefore, fabrication processes providing very smooth surface as well as a high accuracy in lithography and etching are crucial. Recently Si wire waveguide with very low loss (1.7 dB/cm) and the bending radius of 2μm with 0.01 dB/90° scattering loss have been realized using high density plasma etching such as inductively coupled plasma (ICP) and electron cycrotron resonance (ECR)^{2),3)}. However, there are not so many reports about the characteristics of Si wire waveguide by conventional parallel plate reactive ion etching (RIE) due to poor etching selectivity between photoresist and Si.

In this letter, we propose the fabrication method of Si wire waveguides using conventional parallel plate RIE and double layered EB resists containing C₆₀. Moreover, we introduced an edge enhancement writing method in the electron beam lithography (EBL) process to suppress the sidewall roughness of Si wire waveguides.

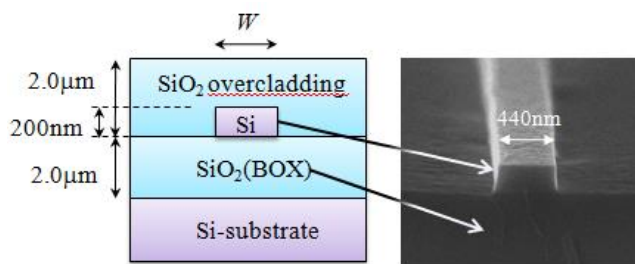


Fig. 1. Structure of silicon wire waveguide based on SOI wafer.

Figure 1 shows the cross sectional structure of the silicon wire waveguide fabricated on a SOI substrate. The BOX layer serves as an undercladding layer. An overcladding layer was 2-μm-thick SiO₂ layer, which was deposited by plasma enhanced chemical vapor deposition (PECVD). A SOI wafer consists of 200 nm-thick surface Si layers and a 2-μm-thick BOX layer, which is enough thick to prevent light leakage to the Si substrate side. The core size was 440 nm-wide and 200 nm-thick to provide the single-mode condition at the wavelength of 1.55 μm.

The fabrication processes are the followings. After cleaning a SOI substrate by typical RCA solution⁴⁾, ZEP520 EB positive resist was spin coated at a speed of 2000 rpm. Then it was prebaked in an oven at 180 °C for 20 min followed by coating micro-composite of ZEP520 and C₆₀⁵⁾ (10% weight), to be called ZEP-C₆₀ hereafter at 2000 rpm and baking on a hotplate at 200 °C for 2min. The thicknesses of ZEP 520 and ZEP-C₆₀ are 550 nm and 60 nm, respectively. EBL exposure was carried out with a JEOL JBX-5FE EBL system operating at 50 kV accelerating voltage and 100 pA beam current. The EB dosage was 138 μC/cm². After the EB patterning, samples were developed in ZED-N50 developer, followed by rinsing in isopropyl alcohol (IPA). A magnetic stirrer was used to obtain a constant developing rate for good re-productivity⁶⁾. Next, Si waveguide was formed by RIE

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with CF_4 (gas pressure: 0.3 Pa, bias power: 20 W, gas flow: 10 sccm, etching time: 26 min). After removing the EB resist, a $2\mu\text{m}$ -thick SiO_2 layer was deposited by PCVD for coated Si wire waveguide.

The cross sectional SEM view of the Si wire waveguide using ZEP520/ZEP- C_{60} is shown in Fig.2 (b). For comparison, that by using ZEP520 resist is also shown in Fig. 2(a). The micro-composite ZEP520 resist has higher dry etching resistance than ZEP520 resist due to C_{60} molecules which act as a highly resistant agent⁷⁾⁻⁹⁾. Double layered resist could achieve a better anisotropic waveguide shape than that using single layered resist. When only ZEP- C_{60} was used, several time spin coating and baking were needed to coat enough thickness and the bottom resist degraded due to over baking. Therefore, one conventional ZEP layer and one ZEP- C_{60} is suit combination to obtain good waveguide shape.

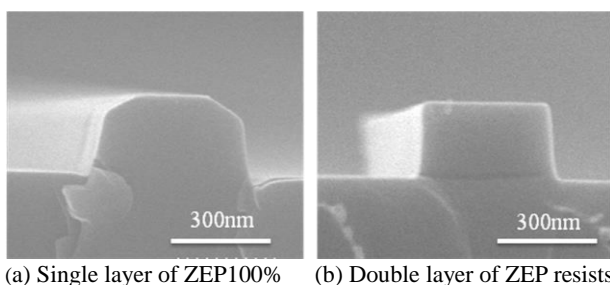


Fig. 2. Cross sectional SEM images of Si waveguide shape using ZEP.

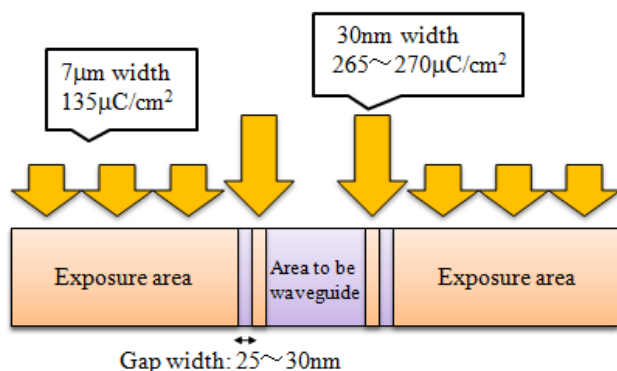


Fig. 3. The exposure design of edge enhancement writing for the reduction of sidewall roughness and proximity effects.

To achieve low optical loss in Si waveguides, reducing the sidewall roughness is the other important factor. We introduced edge enhancement writing EBL method. This method means that high exposure dose breaks up aggregates of resist polymer at the edge in order to reduce roughness of resist patterns, though inner area was dosed uniformly^{10),11)}. Figure 3 shows how the edge enhancement writing was carried out by our process. Exposure dose conditions were optimized at the pattern edge to obtain both the reduction of proximity effects and the reduction of sidewall roughness. The exposure dose of

fine lines along the pattern edges needed twice as much as that used for wide exposure of the inner area. Its dosage is $266\mu\text{C}/\text{cm}^2$ with the width of 30 nm. Moreover, we made non exposure gap between the edge writing and the inner exposure area to reduce influence of proximity effects. The gap width was around 25 nm as shown in Fig. 3 and it was actually gone after the development.

The top cross sectional SEM views of the resist patterns for conventional (uniform writing in inner area) and improvement (edge-enhancement writing) are shown in Fig. 4 (a) and (b), respectively. The sidewall roughness was measured by commercial critical dimension (CD) measurement software. The sidewall roughness (3σ value) of the resists was reduced from 8.4 nm to 4.8 nm by the improvement of the EBL. Figure 5 (a) and (b) show the top cross sectional SEM view of Si waveguide after CF_4 -RIE for these exposures, respectively. The sidewall roughness of the Si waveguides was reduced from 5.1 nm to 3.2 nm after the dry etching processes.

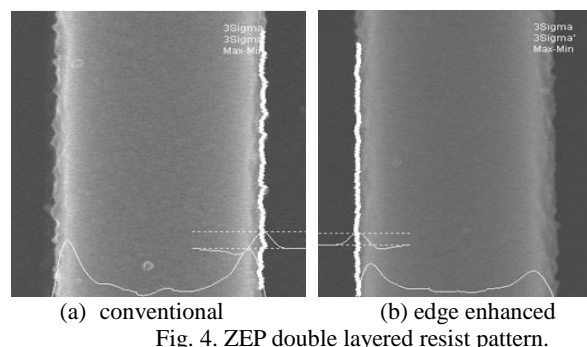


Fig. 4. ZEP double layered resist pattern.

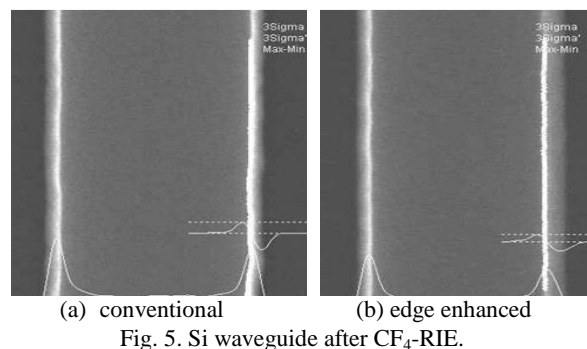


Fig. 5. Si waveguide after CF_4 -RIE.

The reduction of propagation loss was expected by the reduction of sidewall roughness. The calculated scattering loss is smaller than 4.5 dB/cm with the measured 3σ value of 3.2 nm for Si waveguide^{12), 13)}.

Figure 6 shows the measured propagation loss of the fabricated Si wire waveguides with the size of 200×440 nm. The loss for TE mode was measured using Si wire waveguides of various lengths (2 mm, 6 mm, and 8 mm) at the wavelength of 1550 nm. A spherical lensed optical polarization maintaining fibers (PMF) with a $4.5\mu\text{m}$ radius core size was used to couple the light from cleaved facets of the Si waveguide. The polarimeter and controller was used to control the polarization of the input light. As mentioned above, the side wall roughness of Si waveguide was reduced from 5.1 nm to 3.2 nm (3σ value)

by introducing the edge enhancement writing, and the propagation loss of Si waveguide was reduced from 6.0 dB/cm to 4.5 dB/cm for TE mode at 1550 nm as shown in Fig. 6. The propagation loss of the waveguide fabricated by using single ZEP520 layer (Fig. 2(a)) could not be measured because of its bad shape. As a result, we achieved the reduction of propagation loss due to reduction of sidewall roughness. As can be seen in Fig. 6, the coupling loss was around 11 dB of both facets, hence that between with the sample and the optical spherical lensed PMF was around 5.5 dB/facet for TE mode.

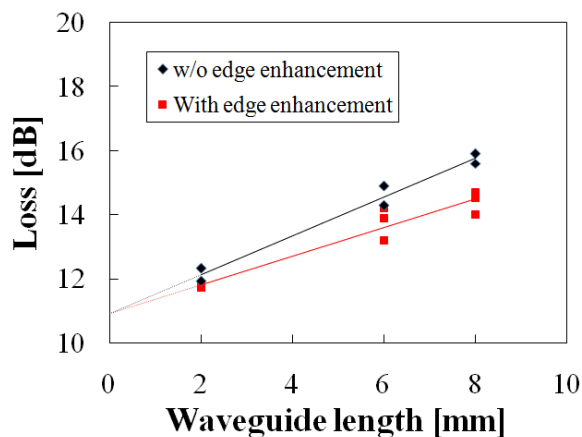


Fig. 6. Propagation loss and coupling loss of Si wire waveguide for TE mode at 1550nm using conventional writing and edge enhancement writing.

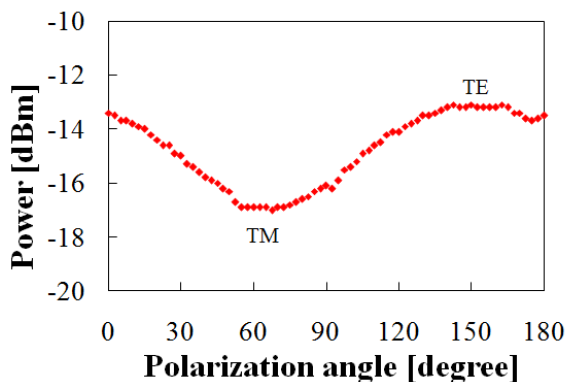


Fig. 7. The polarization characteristics of Si waveguide with 200×440 nm core.

Figure 7 shows the polarization characteristic of Si waveguide of 6 mm length measured at 1550 nm. The polarization dependence of propagation loss was obtained due to difference of optical field distribution of TE/TM mode. The polarization characteristics show sinusoidal wave-like as shown in Fig. 7. TE/TM polarization dependent loss was about 4 dB.

In conclusion, the technique for coating the micro-composite ZEP520 resist with 10% C₆₀ onto the ZEP520 resist is better for vertical shaping with CF₄-RIE. The propagation loss of the Si waveguide using the

double layer resist was measured to be 6.0 dB/cm at 1550 nm. Moreover, we achieved the reduction of the sidewall roughness of Si core using edge enhancement EBL method. The sidewall roughness was 3.2nm (3σ value) for Si core, and then the propagation loss of Si waveguide with 200×440 nm was reduced to 4.5 dB/cm for TE mode at wavelength of 1550 nm. This is the lowest value of Si waveguide loss realized by parallel plate RIE etching and technologies proposed in this letter can be applicable to achieve other etching methods.

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