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Top Layer Plating Lead Maximization for BGA Packages

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1 Introduction

Although a ball grid array (BGA) package can realize a number of connections between a chip and a printed circuit board, its routing design takes much time to realize a small package with high reliability and low fabrication cost. In BGA package manufacturing, electrical plating is one of the important technologies to protect wires with low fabrication cost. However, in order to enable the electrical plating, an extra route for each net, called plating lead, needs to be generated on one of routing layers. In order to obtain a reasonable package with as few layers as possible, layer assignment of plating leads that efficiently utilizes the routing resource on each layer is important.

Several routing methods related to BGA packages have been proposed in [1, 2, 3, 4, 5]. However, layer assignment of plating leads is not considered in these methods. While, a layer assignment method of plating leads for 2-layer BGA packages has been proposed in [6]. The method is fast, but may not obtain a feasible routing pattern with two layers since the routing resource on the top layer is inefficiently used. In this paper, a basic problem is considered, such that a set of plating leads generated on the top layer is maximized under a certain design rule. We showed that the problem can be solved in almost linear time in terms of the number of nets.

2 Preliminaries

We consider a fanout type BGA package with some routing layers. A chip is placed on an interior region of the top layer. A bonding finger, which is referred to as a finger, is placed on the perimeter of a rectangle enclosing the chip, and is connected to the chip by a bonding wire. A solder ball, which is referred to as a ball, is an I/O terminal of the package, and is placed in a grid array pattern on the bottom layer. Each net consists of a finger and a ball, and is realized by wires on each layer and vias which connect wires on different layer. In addition, each route is extended to the package boundary on one of the layers for electrical plating.

The routing area is divided into four sectors. In the following, the top layer of the bottom sector is focused on. We consider two kinds of restrictions for routing structure. First, a via is placed in a grid array pattern called via grid array, and each net exactly has one via that connects the top layer and other layer. The route of a net on the top layer connects from its finger to its via. If the plating lead of the net is routed on the top layer, then it is extended from the via to the package boundary. Second, the route of a net including its plating lead on the top layer is restricted to be *monotonic* so that they intersects any horizontal lines at most once.

We assume that the position of the via of each net on the top layer is given and fixed. If a layer assignment of plating leads is given, then the global routing on the top layer is accordingly determined since the routing is restricted to be monotonic.

The interval between adjacent two vias on the same row in the via grid array is called via-interval. The capacity of via-interval I is the number of possible routes intersecting I, and is denoted by $\mathtt{cap}(I)$. For a layer assignment of plating leads, let $\mathtt{ex}(I)$ be the number of excess routes of I. That is, $\mathtt{ex}(I) = \mathtt{n}(I) - \mathtt{cap}(I)$ where $\mathtt{n}(I)$ is the number of routes intersecting I for the assignment. A via-interval I is said to be *violated* if $\mathtt{ex}(I) > 0$.

3 Top layer plating lead maximization

In the following, the definition of top layer plating lead maximization problem is given, and we showed that the problem is solved in polynomial time if the number of rows is fixed, though the proof is omitted for space.

Definition 1 *Given routing between fingers and balls for a BGA package, Top layer Plating lead Maximization (TPM) problem is to obtain a maximum set of plating leads routed on the top layer so that no violated via-interval exists.*

Theorem 1 *TPM problem can be solved in $O((v+1)^{r-1}rN)$ where N is the number of nets, r is the number of row in the via grid array, and v is the maximum number of excess routes on via-intervals in the case that all plating leads are routed on the top layer.*

In actual package design, the number of rows in the via grid array and the maximum number of excess routes can be regarded as small constant number. TPM problem can be efficiently solved in almost linear time in terms of the number of nets. By solving TPM problem, a reasonable packages with fewer layers is expected to be obtained since plating leads to be routed on layers except the top layer are reduced.

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