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3 Single-electron logic based on multiple-tunnel junctions

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Abstract

This is a review of our work on logic circuits based on electron pumps which consist of semiconductor multiple-tunnel-junction (MTJ) single-electron transistors. The MTJ transistors are formed in side-gated GaAs wires δ-doped with Si. Being semiconductor, the MTJ transistor not only works as a single-electron transistor but can also be completely pinched off to an off state that is far better than is achievable by Coulomb blockade alone. This added degree of controllability, missing in the metallic counterpart, gives distinct on-off characteristics even at relatively high temperatures. MTJ pumps are used to implement a binary decision diagram (BDD) logic circuit. The two-way switching function required in the BDD circuit is realised by using the pinch-off state. A simple theoretical analysis is carried out to estimate the best possible performance of the pump.

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The reasons behind adopting such a circuit architecture are discussed in detail.

1 Introduction

Numerous proposals have been made of logic applications of single-electron devices, of which we can cite only some [1–18]. Some are analogous to existing circuit architectures, and some try to be more "single-electron" specific. However, no single approach seems to stand out as a winner.

In this article, we review an approach we took and discuss the design decisions. A key ingredient in our approach is the use of semiconductor multiple tunnel junctions (MTJs). MTJs are very effective for preventing leakage due to cotunnelling [19]. In addition, semiconductor single-electron devices [20,21] offer some more useful features than metallic devices. Our MTJs are implemented in very narrow side-gated GaAs constrictions heavily δ-doped with Si. When a negative voltage is applied to a side-gate, the two-dimensional electron gas (2DEG) is split into microsegments due to potentials of dopant atoms, and typically more than five tunnel junctions are formed in series. [22–25]. Within a certain range of side-gate bias voltage, the MTJ can be gated to work as a single-electron transistor. With still higher negative side-gate voltages, the channel is completely pinched off.

In the next section, we explain some basics of single-electron devices. In §3, we discuss some points which we considered when designing our single-electron logic circuit. Experimental results are presented in the following three sections. Experimental investigation of the multi-clock MTJ pump, which is an essential component of our circuit, is described in §4. Experiment on two-way switching operation, required in the circuit, receives treatment in §5. The demonstration of a single-electron logic circuit is presented in §6. §7 deals with a simple performance analysis of the multi-clock MTJ pump. Finally in §8 we discuss some prospects for the future.

2 Semiclassical theory

The characteristics of our MTJs are well-described by the semiclassical theory of single-electron charging and Coulomb blockade of single-electron transfer.

2.1 Coulomb blockade

Electrical characteristics of various *voltage-biased* circuit elements are compared in Fig. 1 [23]. In a resistor, carriers respond to any small change of voltage, and a current flows as shown in Fig. 1(b). In a capacitor, no steady current flows as shown in Fig. 1(c).

An ideal voltage-biased ultrasmall tunnel junction would show a similar current-voltage characteristic to a resistor's, as shown in Fig. 1(d). If the junction is very small and the barrier is quite opaque,[1] it is reasonable to assume that the current flows by successive tunnelling of single electrons. The charge lost by tunnelling is immediately supplied by the voltage source through the ideal leads (the global rule [26]), and the electro-static energy U of the system remains constant; $U = CV^2/2$. Therefore, there is

[1] Opaque here means that the tunnel resistance R_T in Fig. 1(d) is larger than the resistance quantum.

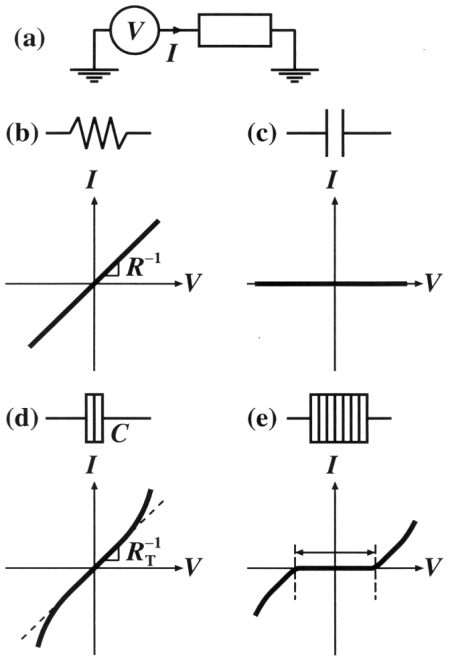

Figure 1. *I-V* characteristics of ideally voltage-biased circuit elements as in (a). (b) Resistor. (c) Capacitor. (d) Ultrasmall tunnel junction. (e) MTJ.

no correlation between tunnelling events. Suppose that the circuit is in thermal equilibrium with the environment at temperature T. Then, in a steady state, the forward direction single-electron tunnelling rate Γ_+ and the rate for its reverse process Γ_- should satisfy the following detailed balance relationship.

$$\frac{\Gamma_+}{\Gamma_-} = \frac{\exp(0/k_{\mathrm{B}}T)}{\exp(-eV/k_{\mathrm{B}}T)}. \tag{1}$$

Here e is the elementary charge, and eV is the amount of energy dissipated to the environment by forward tunnelling and equals the amount of work, ΔW_e, done by the voltage source. Dissipation is assumed to take place by some (unspecified) fast physical processes. The net electron transfer rate in the forward direction is

$$\Gamma_{\mathrm{net}} = \Gamma_+ - \Gamma_- = \Gamma_+ \left[1 - \exp(-eV/k_{\mathrm{B}}T)\right], \tag{2}$$

whence the current is

$$I(V) = e\Gamma_{\mathrm{net}}. \tag{3}$$

From Eqs. (2) and (3), the rate of forward tunneling is [27]

$$\Gamma_+ = \frac{I(V)}{e}\frac{1}{1-\exp(-eV/k_{\mathrm{B}}T)}. \tag{4}$$

In the popular "tunnel resistance" model, the current-voltage relationship is approximated by an Ohmic relationship $I(V) = V/R_{\mathrm{T}}$, as shown by the broken line in Fig. 1(d).[2]

The characteristic of an MTJ looks like a combination of both resistor and capacitor characteristics as shown in Fig. 1(e). When $|V|$ is smaller than a certain value, no tunnelling event takes place in any of the tunnel junctions at $T \to 0$ K. To see how this can happen, we again look at the tunneling rate. Since in this case each tunnel junction is no longer voltage-biased, Eq. (4) cannot be used as is. The difference here is that when an electron tunnels, part of the energy supplied from the voltage source is not immediately dissipated but stored in the capacitances of tunnel junctions, that is to say, $\Delta U \neq 0$. By the principle of conservation of energy (the first law),

$$đW_{\mathrm{e}} = \mathrm{d}U - đQ_{\mathrm{irrev}}, \tag{5}$$

where $đQ_{\mathrm{irrev}}$ is the heat added to the system, and hence $-đQ_{\mathrm{irrev}}$ is the energy transferred to the environment [28]. Let us introduce an energy function F as follows.[3]

$$F = U - W_{\mathrm{e}}. \tag{6}$$

Then, $đQ_{\mathrm{irrev}} = \Delta F = F_{\mathrm{f}} - F_{\mathrm{i}}$, where F_{f} and F_{i} are the values of F after and before tunnelling, respectively. In the case of a voltage-biased tunnel junction, Fig. 1(d), ΔU happened to be zero, so that $\Delta F = -\Delta W_{\mathrm{e}} = -eV < 0$. $\Delta F < 0$ means that some energy is dissipated to the environment. In an MTJ, however, ΔF can become positive even when $\Delta W_{\mathrm{e}} > 0$ if $\Delta U > 0$. [4] This can happen if $|V|$ is within a certain range. Processes with $\Delta F > 0$ are suppressed because of the second law. As a result, a gap appears in the *I*-*V* curve as shown in Fig. 1(e). This phenomenon is called *Coulomb blockade of single-electron tunnelling* because the Coulomb energy plays a key role in suppressing tunnelling.[5] In the absence of tunneling events, no energy dissipation takes place in equilibrium, and therefore F takes an extremum. Since F reaches the extremum by dissipating energy ($\Delta F < 0$), it is a minimum. In this respect, F is analogous to a free energy. However, unlike Helmholtz or Gibbs free energy in thermodynamics, Eq. (6) is not a function of state because it includes work, which is not an attribute of the system but depends on the history of the system. Alternatively, Eq. (6) may also be understood as the sum of electrostatic energy and available chemical energy in "batteries" ($U_{\mathrm{chem}} = \mathrm{const} - W_{\mathrm{e}}$). In any case, what usually matters is only the difference in F, *viz*. ΔF.

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[2] If one wishes to stick to the concept of tunnel resistance even for non-Ohmic $I(V)$, the bias-dependent tunnel resistance would be $R_{\mathrm{T}}(V) = \partial I/\partial V$.

[3] F is sometimes called electrostatic energy in the literature. In this article, we refer to U as electrostatic energy.

[4] $\Delta F > 0$ can also be met (very easily) if $\Delta W_{\mathrm{e}} < 0$, but this is not a special situation at all. This is a situation where an electron is trying to tunnel against a bias. Such a tunnelling event is obviously forbidden.

[5] In fact, the single-charge transfer need not take place by tunnelling. For example, thermal hopping also gives similar results [29].

Now the eV in Eq. (4) has to be replaced by $-\Delta F$ to give

$$\Gamma_+ = \frac{I(V_{\text{eff}})}{e}\frac{1}{1-\exp(-eV_{\text{eff}}/k_{\text{B}}T)}, \tag{7}$$

where

$$V_{\text{eff}} = -\Delta F/e = \frac{V_{\text{i}}+V_{\text{f}}}{2}. \tag{8}$$

V_{eff} is the effective bias voltage across the tunnel junction in question [30]. V_{i} is the voltage across the junction before tunnelling and V_{f} is that after tunnelling.[6] Equation (7) is plotted in Fig. 2.

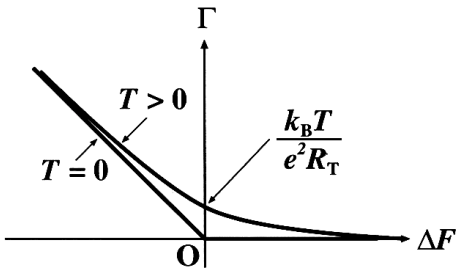

Figure 2. Tunnelling rate Γ as a function of $\Delta F = -eV_{\text{eff}}$. $I(V) = V/R_{\text{T}}$ is assumed.

Note that it has been assumed in the above that the energy level spacings in the MTJ islands are the same (continuous) as in the case of a voltage-biased junction. If this is not the case, tunneling between individual energy levels should be considered [31–34]. In such cases, it is common to look at the zero-bias conductance of the entire structure (transistor) [33, 35–37].

2.2 Single-electron transistor

A circuit diagram of a capacitively-coupled single-electron transistor [10] with two tunnel junctions is shown in Fig. 3. Its Coulomb blockade (stability) condition at absolute zero is derived as follows. Supposing that all bias voltages are fixed, the electrostatic free energy Eq. (6) may be written as

$$\begin{aligned} F(m_1,m_2) &= \frac{Q_1^2}{2C_1}+\frac{Q_2^2}{2C_2}+\frac{Q_{\text{g}}^2}{2C_{\text{g}}}+\frac{Q_0^2}{2C_0} \\ &- Q_{\text{g}}V_{\text{g}} - (m_1 e + Q_1)V_1 \\ &- (-m_2 e - Q_2)V_2, \end{aligned} \tag{9}$$

[6] $V_{\text{i}} \neq V_{\text{f}}$ if $\Delta U \neq 0$.

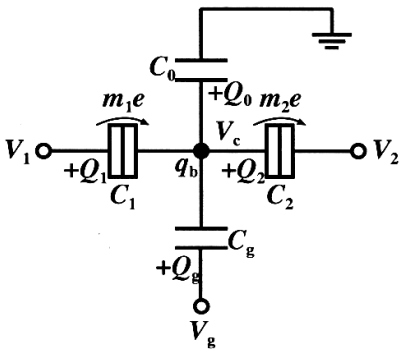

Figure 3. Two-junction single-electron transistor with a capacitively-coupled gate. m_1 and m_2 are the numbers of charges that have tunneled through C_1 and C_2, respectively. q_b is the background charge.

where m_1 and m_2 are the numbers of charges that have tunnelled through junctions C_1 and C_2, respectively. The charge on the central island satisfies

$$(m_1 - m_2)e + q_b = -Q_1 + Q_2 - Q_g + Q_0, \tag{10}$$

where q_b is the background charge which gives fractional offset to the island charge. Also, the voltage differences between electrodes can be written in terms of Q_i using Kirchoff's voltage law. By eliminating all the Q_i in Eq. (9), we obtain

$$\begin{aligned} F(m_1, m_2) \;=\; & \frac{1}{2C_\Sigma}\left[(m_1 - m_2)e + q_b + C_g V_g\right]^2 \\ & - \frac{m_1 e}{C_\Sigma}\left[(C_2 + C_g + C_0)V_1 - C_2 V_2\right] \\ & - \frac{m_2 e}{C_\Sigma}\left[C_1 V_1 - (C_1 + C_g + C_0)V_2\right] \\ & + \text{const}, \end{aligned} \tag{11}$$

where

$$C_\Sigma = C_1 + C_2 + C_g + C_0. \tag{12}$$

The constant term in Eq. (11) does not contain m_1 nor m_2. The total capacitance of the dot, C_Σ, rather than tunnel capacitances, determines the characteristic energy scale e^2/C_Σ, and hence the operation temperature.

The stability condition for the neutral state ($m_1 - m_2 = 0$) is given by $F(\pm 1, 0) - F(0, 0) > 0$ and $F(0, \pm 1) - F(0, 0) > 0$. [7] In the present case, the three voltage sources V_1, V_2

[7]These inequalities only define the stable region for the state $m_1 - m_2 = 0$ and do not explicitly assert the instability of the region outside the said stable region. However, it is straightforward to confirm the instability of, say, $m_1 - m_2 = 1$ by noticing $F(1, 1) - F(1, 0) = F(0, 0) - F(0, -1)$, etc.

and V_g span a three-dimensional space. Two different cross sections of the stable region are shown in Fig. 4 as shaded areas. When V_g is swept, $(m_1 - m_2)e$ in the first term of Eq. (11) changes such that it cancels out C_gV_g. As a result, the current changes periodically as shown in Fig. 5. The current I changes so sensitively on C_gV_g (especially near the border of stability) that a single-electron transistor can be used as an electrometer [38]. In the I-V_1 plane, the "Coulomb gap" around $V_1 = 0$ [Fig. 1(e)] repeatedly stretch and shrink with V_g.

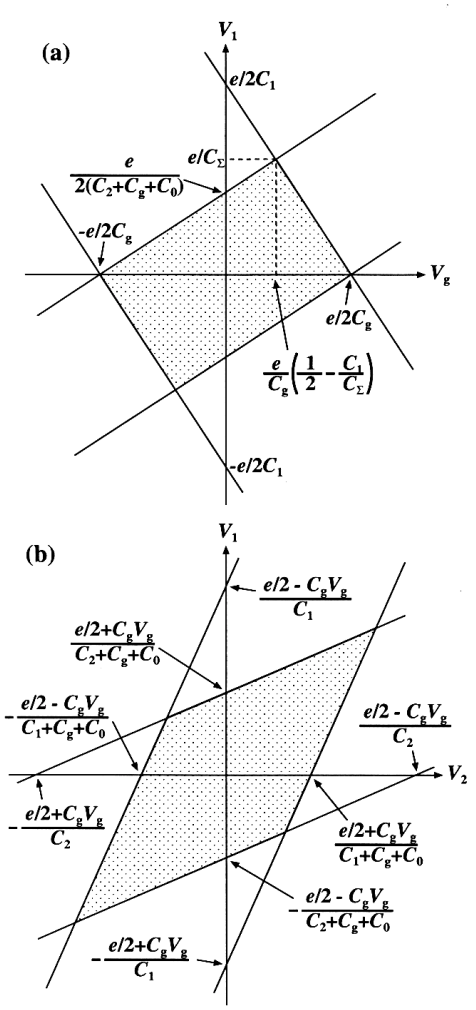

Figure 4. Stability diagrams of the single-electron transistor. Shaded areas are the Coulomb blockade regions, and current is blocked at $T = 0$ K. Background charge q_b is assumed to be zero. (a) V_1-V_g plane at $V_2 = 0$. The cross section at $V_1 = 0$ (V_2-V_g plane). can be obtained by substituting V_2, C_1 and C_2 for V_1, C_2 and C_1, respectively. (b) V_1-V_2 plane. The rhomboid moves along the line V_1=V_2 if V_g is changed. After [28].

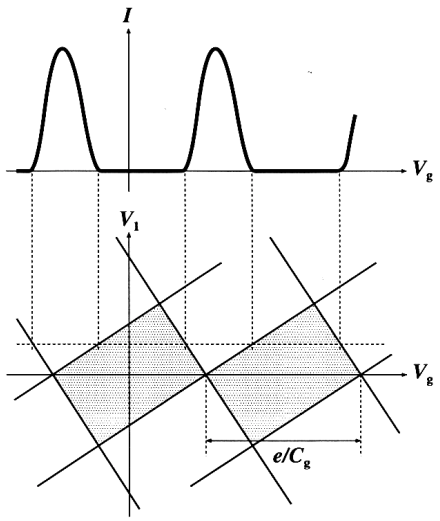

Figure 5. Current of a single-electron transistor when small bias V_1 is applied. It oscillates with the period e/C_g as V_g is swept. $V_2 = 0$ is assumed.

2.3 Frequency-locked charge transfer

Time-correlated single-electron tunnelling was observed in arrays of tunnel junctions irradiated with microwave fields [39, 40], where the intervals between tunnelling events were almost the same. Later, frequency-locked single-electron transfer by external gating was realised in the turnstile device [41]. The single-electron turnstile is an array of four tunnel junctions with a gate which is capacitively coupled to the island in the middle of the array, as shown in Fig. 6(a). The turnstile was designed so that only one extra electron can enter/leave the central island if a proper rf signal is applied to the gate. When an rf clock signal of frequency f is applied, a current plateau of $I = ef$ appears within a certain range of bias voltage [41]. The following years saw various rf-driven

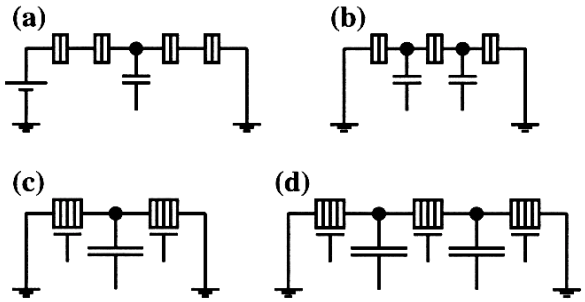

Figure 6. Various frequency-locked single-electron transfer devices. (a) Single-electron turnstile [41]. (b) Single-electron pump [45]. (c) Bidirectional MTJ pump [67]. (d) Multi-clock MTJ pump [71].

single-electron transfer devices. Another kind of turnstile device was demonstrated in semiconductor [42]. It had two tunnel barriers and an island in between like a single-electron transistor (Fig. 3), and the barriers were modulated by two rf signals with different phases to alternately lower the barriers [43]. This type of turnstile is also known as the oscillating-barrier turnstile [44], and its operation principle is somewhat different from the original turnstile [41].

The single-electron pump [45,46], driven by two or more rf clock signals, allows more precise single-electron transfer. In contrast to the turnstile device [41], no dc bias is required for frequency-locked electron transfer. It is also possible to pump up electrons against a small bias voltage. Another difference from the turnstile is that in the pump, electrons could in principle be transferred quasi-statically (tunnelling with $\Delta F = 0$), whereas in the turnstile the charge transfer process is always dissipative [47]. The first single-electron pump had three tunnel junctions as shown in Fig. 6(b) and was driven by two rf signals [45, 46]. Accuracy of the frequency-locked current can be improved by the use of many tunnel junctions and driving rf-signals. The turnstile and the pump opened up a realistic possibility of establishing frequency-determined current standard [48] and other applications [12, 49]. Great efforts have been made to establish accurate charge transfer and to understand the mechanisms which hinder it [50–66].

The bidirectional electron pump reported by Tsukagoshi *et al.* consists of a pair of MTJ transistors connected in series [67, 68] as shown in Fig. 6(c). It is driven by one ac clock signal and resembles the turnstile [41] at first glance. Indeed, electron transfer is dissipative as in the turnstile [47]. However, it can pump up electrons against a small bias [67] like the original single-electron pump [45]. Moreover, the direction of pumping can be changed by properly adjusting the side-gate biases [67, 68]. The number of electrons transferred per clock cycle is typically a few tens to several hundred. These differences originate in the magnitude of capacitances in a device. In the original turnstile and pump, all the capacitances in a device are of the same order. On the other hand, there are two different capacitance scales involved in the bidirectional pump. One is of the capacitances that constitute the MTJs and the other is of the capacitance of the clocking-gate. The clocking-gate capacitance, which is situated between the MTJ transistors, is significantly larger than the other capacitances in the pump. The total capacitance of the clocked node is so large that single-electron charging effect is almost negligible. As a result, the MTJ transistors work virtually independently of each other as if being voltage-biased. The pump operation reflects MTJ transistors' nonlinear *I*-*V* characteristics [Fig. 1(e)] rather than the precise charge configuration in the circuit [67, 68]. In other words, the bidirectional pump is essentially a series connection of two ac-biased single-electron transistors [69], which work as rectifiers.[8] Detailed analysis of the bidirectional pump was carried by Jalil et al. [68] using the semiclassical model.

We later reported a similar MTJ pump [71]. It consists of three or more MTJs as shown in Fig. 6(d) and is driven by unipolar multi-phase clock signals. This is the pump which we used as a building block to construct a logic circuit [72]. Its operation also relies on the nonlinear current-voltage characteristics of MTJs, but the direction of pumping is determined by the choice of the phase difference between clock pulses. Details will be described in later sections.

[8] A similar kind of rectifier includes the quantum-dot ratchet [70].

3 Design considerations

There are a number of issues that should be considered to realise single-electron logic. Some are interrelated.

3.1 Information representation

One most straightforward way of representing bit information is to use a certain number of excess electrons for "1" and the absence of them for "0," although this is certainly not the only option [73]. The ultimate *single-electron* logic sounds very attractive. However, the number of charges used to represent a bit should be at least three. If a bit is represented by presence or absence of one extra charge, only one tunnelling event would result in bit flip. If only two charges are used, one tunnelling event would lead to the intermediate state with one extra charge, from which error recovery is not possible. With three charges, off-by-one errors could be corrected. More than three is still better, but we certainly do not want to increase the number indefinitely.[9]

3.2 Interaction between components

A circuit component (element) that works nicely on its own (i.e. when biased by voltage sources) might not work as expected in a more complex circuit. Elements might interact with one another in a non-obvious way if the capacitance of the node which connects them together is small [75]. For instance, the CMOS-like inverter proposed by Tucker [16] may not work as an inverter if the capacitance of the node between the p-type and the n-type single-electron transistors is too small [76].[10] This is because the interconnecting node makes some additional contribution to the electrostatic energy U in Eq. (6), which in turn affects the tunnelling rate, Eq. (7). This not only makes the design of large circuits difficult but also makes SPICE-type circuit simulation impractical [75, 77]. Besides, such circuits would inevitably have very tight tolerances for circuit parameter dispersion, and any unexpected stray capacitances may lead to a failure. Components should therefore be made independent of one another by requiring that the interconnecting nodes have relatively large capacitances. In the bidirectional [67,68] and multi-clock [28] MTJ pumps, the MTJ transistors are independent in this sense.

3.3 Transistor gain

If single-electron transistors are to be used in a similar fashion to conventional transistors [4, 16], they must have voltage gain much greater than unity. This guarantees signal propagation with signal-level recovery. Let V_c be the voltage of the central island of a single-electron transistor (Fig. 3). Then, $\partial V_c/\partial V_g = C_g/C_\Sigma$ and $\partial V_c/\partial V_1 = C_1/C_\Sigma$, where C_Σ is given by Eq. (12). The voltage gain is maximised when a fixed current is flowing. If the fixed current I is small, I is almost proportional to V_c. Then the voltage gain is [10, 78]

$$G = \frac{\partial V_1}{\partial V_g} = \frac{\partial I/\partial V_g}{\partial I/\partial V_1} \simeq \frac{\partial V_c/\partial V_g}{\partial V_c/\partial V_1} = C_g/C_1, \tag{13}$$

[9] If the charge number is not too small, then the bit energy is a more important parameter than the number itself for reliability [74]. The number should nevertheless be kept small for speed.

[10] In this example, the elements are the single-electron transistors, and the circuit is the inverter.

where V_2 is assumed to be grounded. Equation (13) suggests that C_g should be made much larger than C_1. However, C_1 is a tunnel capacitor which has a very thin insulating layer, whereas C_g is a non-tunnel capacitor, so that it is difficult to make $C_g \gg C_1$. Relatively high voltage gains of transistors and inverters reported so far [79–84] are still far from ideal for real applications. Also, making C_g large contradicts the requirement that C_Σ be as small as possible to have a large charging energy. Since the gain rapidly decreases as the temperature rises, the requirement of gain imposes a severe upper limit to the operation temperature. Conversely, if single-electron transistors are used in a way that does not require gain, operation temperature could be much higher. Therefore, architectures which do not require transistor gain are preferable.

3.4 Turn-off mechanism

Although Coulomb blockade of single-charge transfer can in principle keep current from flowing for small biases [Fig. 1(e)], it is not a very good "turn-off" mechanism for practical purposes. The blockade region is determined by capacitance parameters as shown in Fig. 4. However, the tunnelling rate for $\Delta F > 0$ is quickly lifted up from zero when $T > 0$ K as illustrated in Fig. 2. Leakage due to co-tunnelling [19] becomes a problem only after thermal leakage is eliminated [85]. Although a constant tunnel resistance is used in Fig. 2, the actual $I(V)$ in Eq. (7) may be temperature dependent [29, 86, 87], making the leakage current even larger. In order to realise a good "turn-off" state, which is important for proper circuit operation and reduction of power dissipation, some different mechanism should be used in concert or instead.

Good "turn-off" can be realised more easily in semiconductor single-electron devices than in metallic devices. If an extreme gate bias is applied, the conduction channel can be completely pinched off, and a very wide, high-resistance region ("gap") appears as schematically shown in Fig. 7. The "turn-off" thus obtained is much better than that by Coulomb blockade.

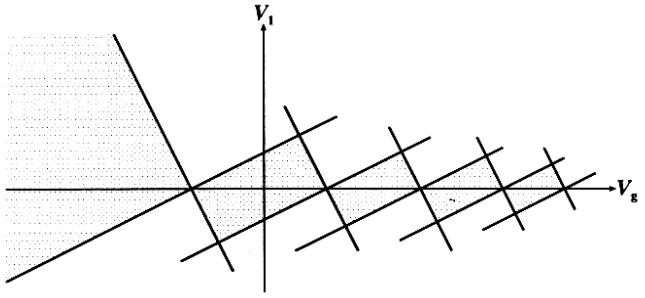

Figure 7. A schematic stability diagram of a semiconductor single-electron transistor.

In some cases, enhancement of Coulomb blockade could be observed in an intermediate gate voltage range, where the gap is much wider than the normal Coulomb gap, and also the current oscillations persist with roughly the same period in V_g as in normal Coulomb blockade [13, 81, 88]. The origin of the enhancement is presumed to be the formation of space-charge regions around the tunnel junctions [81, 88]. This effect is also useful for improving voltage gain [81, 88].

3.5 Background charge

Random background charge, which gives some un-predictable offset to the island charge, is one of the most serious problems in the application of single-electron devices. As is clear from Eq. (11), the background charge q_b on an island has exactly the same effect as C_gV_g, and therefore q_b shifts the threshold gate voltage for Coulomb blockade. A single-electron transistor, which is extremely sensitive to C_gV_g, is equally sensitive to q_b. Background charge often fluctuates with time, and in such a case the effect is recognised as noise [89–91]. Possible origins include charged defects and impurities in the substrate. Recently long-term background-charge stabilities in Si-based single-electron devices have been reported [92,93]. Short-term noise and long-term drift are considered to have different origins [92].

Nakazato and Ahmed proposed the use of MTJs as a possible means by which to address the background charge problem [13]. Here we discuss in exactly what sense this could be a practical solution. In the analyses reported previously, it has commonly been assumed that the background charges on islands in an MTJ are statistically independent from one another [Fig. 8(a)] and take completely random values [94–96]. The question is whether such modelling appropriately describes real devices, especially semiconductor devices. We are inclined to postulate that apparently random background charges are actually correlated [97] as shown in Fig. 8(b). In state-of-the-art Si process technologies, for instance, a defect density of 0.01 cm^{-2} and a surface trap density of 10^{10} cm^{-2} have been achieved.[11] Then the number of stray charges in close vicinity to an MTJ is most likely at most a few, and background charges should not be completely random. Coulomb blockade may be lifted in some junctions near a stray charge. However, Coulomb blockade in the rest of junctions should not be affected, thereby still maintaining a finite Coulomb gap [97]. If MTJs are used in a circuit architecture in which only the existence of the Coulomb gap is essential, the background charge problem could be circumvented with "correct nanofabrication techniques [100]."

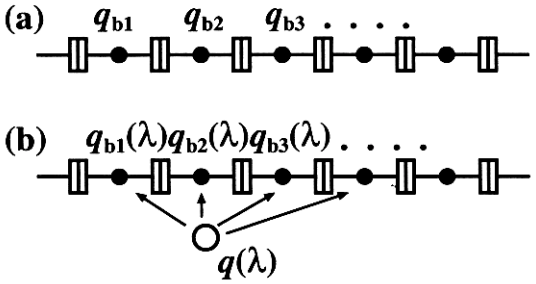

Figure 8. Models of background charges in an array of tunnel junctions. (a) Background charges q_{b1}, q_{b2}, q_{b3}, … are statistically independent and take completely random values. (b) q_{b1}, q_{b2}, q_{b3}, … are correlated, characterised by a parameter (or a set of parameters) λ associated with a stray charge $q(\lambda)$ at a nearby site.

[11] Although the MTJ pumps described in this article are GaAs-based, Si MTJ pumps have also been demonstrated [98, 99].

3.6 Our strategy

We proposed a single-electron logic circuit that addressed most of the problems which we discussed above [72]. Our method is to use an architecture based on the binary decision diagram (BDD) [101]. A BDD has a tree structure which consists of nodes with a "two-way switching" function and can represent any logic function. The BDD tree shown in Fig. 9(a) represents an AND function. Each two-way switching node receives a "token"[12] from the preceding node through the entry lead and then sends it to a following device through one of the branches in accordance with the input to the node [X_1 or X_2 in Fig. 9(a)]. The node devices need not have high gain, but only a distinct on-off switching characteristic is required. The use of BDD architecture for single-electron circuits was first proposed by Asahi *et al.* [102] Their proposed implementation was of an ultimate single-electron type in which one electron was used as the token [3, 103]. For the reasons discussed earlier, our implementation is different and is based on the multi-clock MTJ pumps [71], shown in Fig. 9(b)(c). Typically several hundred electrons flow per clock cycle rather than one. Electrons flow only by clocking, and no dc power supply is used for charge transfer, which might result in lower power consumption due to absence of steady leakage. Each MTJ transistor works as if being voltage-biased because of the large total capacitances of the clocked nodes [28], so that many pumps can be connected

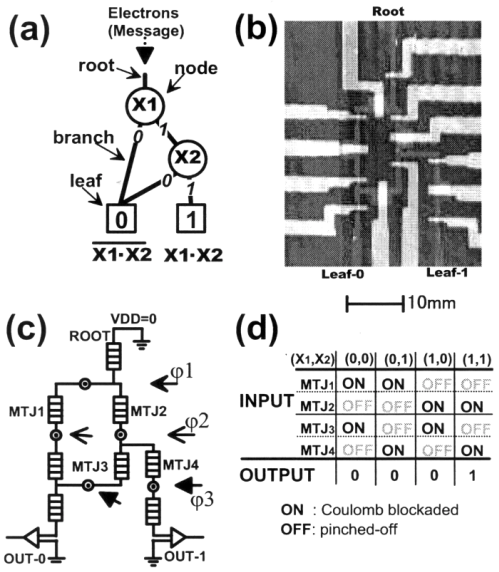

Figure 9. (a) A BDD representing the AND logic function. (b) An AFM image of the AND function device. Ti/Au Schottky gates cover the 0.3 μm wires to form MTJs. The gates on the wide pads are used for clocking. (c) An equivalent circuit of the device including measurement equipment. (d) Truth table relating input to output for the AND device. Reprinted with permission from [72]. Copyright 1998, American Institute of Physics.

[12] Referred to as "messenger" in [3].

with ease to constitute complex BDD trees. As mentioned in §2.3, the operation of the multi-clock MTJ pump relies on the nonlinear current-voltage characteristics of the component MTJs [Fig. 1(e)] rather than precise conditions for Coulomb blockade. It works as long as a Coulomb gap exists. Our circuit is therefore quite tolerant for dispersion of circuit parameters, including background charges and other uncontrollable effects such as quantum mechanical effects. This also means that it does not require subtle tuning of side-gate biases, which is commonly required. In fact, the necessity to fine-tune the gate voltage of each individual transistor, which can actually be done for only very small circuits, is a problem that hamper many proposed circuit architectures from being practical.

Since our MTJ is naturally formed in an electrically squeezed semiconductor channel, its overall size is much smaller than those made by connecting many single tunnel junctions [40, 104, 105]. In the implementation of Asahi *et al.*, Coulomb blockade alone was used for switching [3, 103]. In our implementation, we make use of the extra degree of controllability available in our MTJ, namely the pinch-off state, to realise the two-way switching function [106]. It provides much better "turn-off" than Coulomb blockade up to much higher temperatures. An implementation of BDD reported later by Yamada *et al.* [107] uses a similar idea in which resistance of tunnel junctions are modulated.

4 Multi-clock MTJ pump

The multi-clocked MTJ pump is the building block of our logic circuit. Figure 10(a) shows a scanning electron micrograph of a multi-clock pump composed of three MTJs with two clocked nodes (node1 and node2) [71], corresponding to Fig. 6(d). The device was made from a δ-doped GaAs wafer. The Si δ-doped layer was 30 nm below the

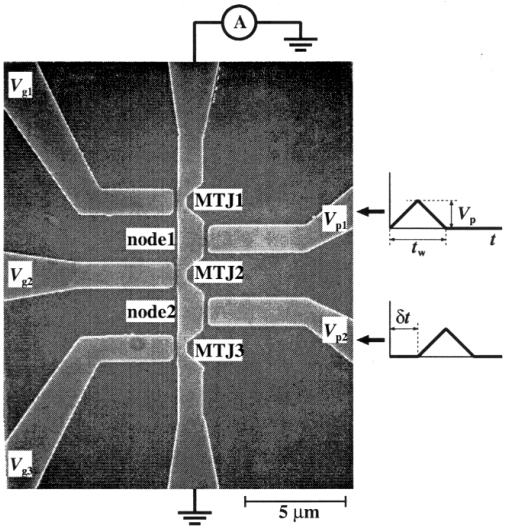

Figure 10. Scanning electron micrograph of a multi-clock MTJ pump device with two clocked nodes. After [71].

surface. The structure was defined by electron-beam lithography and reactive ion etching. A proper negative voltage applied to a side-gate electrically squeezes the conduction channel and splits it into series of islands with tunnel junctions in between [108]. The size of the islands varies, but the typical size was estimated to be about 10 nm in diameter. Further negative side-gate bias completely pinches off the conduction channel. In this experiment, the three MTJs were set in the Coulomb blockade regime.

To transfer electrons, two clock signals (V_{p1} and V_{p2}) of frequency f were applied to the side-gates with various phase delays δt. We experimentally investigated the optimum phase delay between the two voltage pulses. The pulse height V_p was high enough to overcome the Coulomb gap of the MTJs. The resulting pump current was measured at 1.8 K under zero source-drain bias with a current preamplifier.

Figure 11 shows the net pump currents as a function of the phase delay δt over one clock cycle $1/f$ for different pulse shapes. As δt was increased, pump currents appeared

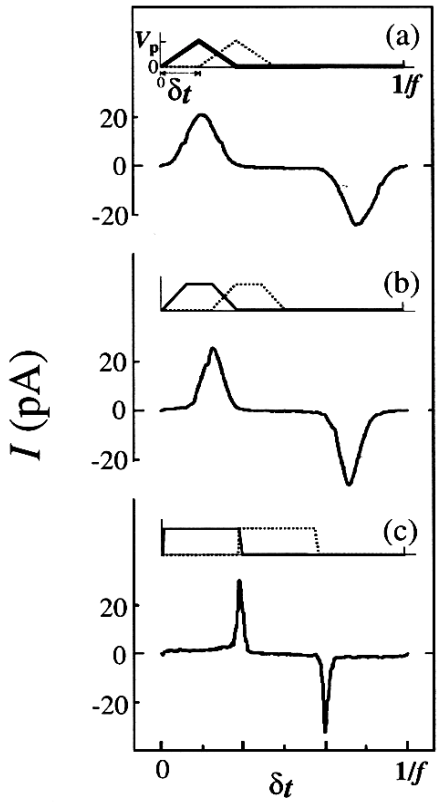

Figure 11. Pump currents versus the phase delay δt between V_{p1} and V_{p2}. The driving frequency f is 0.5 MHz, and the pulse height V_p is 0.5 V. The insets show the pulse overlap conditions which give the maximum currents. (a) Triangular pulses. (b) Trapezium pulses. (c) Slightly tapered square pulses. Reprinted with permission from [71]. Copyright 1997, American Institute of Physics.

and peaked at particular phase delays, where the falling part of V_{p1} exactly overlapped with the rising part of V_{p2} as illustrated in the insets of Fig. 11. The troughs in currents can be understood as the opposite combination of the pulses where the rising part of V_{p1} overlapped with the falling part of V_{p2}. For phase delays with-out overlap, however, no pump current was observed. For instance, no current is produced if the two pulses are synchronised ($\delta t = 0$) because the voltage drop across MTJ2 is always zero. For efficient pumping, overlap of the pulses has to be optimised. For Fig. 11(a)–(c), triangular, trapezium, and slightly tapered square pulses were used, respectively. The pulse widths (t_w in Fig. 10) were the same. Although the pump currents were maximised at different δt values, the pulse overlapping conditions for the maxima were the same for all the pulse shapes, as illustrated in the insets of Fig. 11(a)–(c). The proper overlap of the falling part of V_{p1} and the rising part of V_{p2} therefore is essential for pumping.

Pump currents were found to be proportional to the clock frequency f up to 1.5 MHz. Within this frequency range, the current could be expressed as

$$I = N_c e f \tag{14}$$

where N_c is the number of electrons transferred per clock cycle. The frequency dependence of the peak current is graphed in Fig. 12. In this measurement, triangular pulses were used. Although the slope of the clock pulses became steeper with frequency, the necessary phase delay for the peak current in the $1/f$ scale did not change, as shown in the inset of Fig. 12. From the slope of the linear part of Fig. 12, N_c was estimated to be around 750.

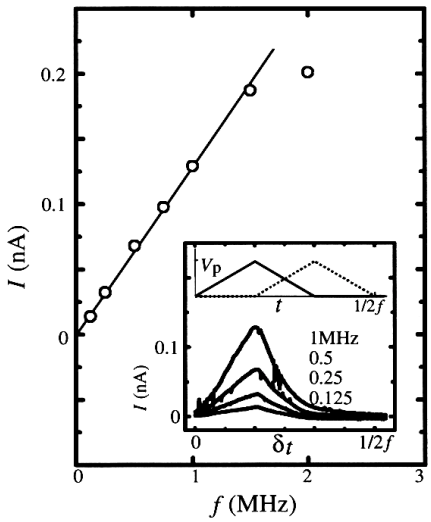

Figure 12. Frequency dependence of the peak pump current when triangular pulses are applied. The solid line is a visual guide. Inset: Pump currents as a function of δt. Reprinted with permission from [71]. Copyright 1997, American Institute of Physics.

5 Two-way switching device

At a branching point of a BDD tree is a two-way switching device that sends off a token to one of two possible pathways depending on the logic input to the node. The two-way switching device shown in Fig. 13 consists of three MTJ transistors with one clocked node [106]. It can be seen as a bi-directional MTJ pump [67] with two branches. An equivalent circuit is shown in Fig. 14(a). When rf sinusoidal waves are applied to the clocking gate, a current I_0 flows into the node through the entry MTJ, which is set to be in the Coulomb blockade regime. The pump current flows out through one of the two output branches as I_1 or I_2. Two complementary side-gate biases $\pm V_g$ are applied to the output MTJ transistors to switch them between ON (Coulomb blockade regime) and OFF (pinched off) states. In the measurement, a small dc bias of 5 mV was applied to the entry lead. This was done in order to avoid the switching of the pumping direction (i.e. bidirectional pumping [67, 68]) due to the change in V_g. In the actual logic circuit described in §6, multi-phase clock pulses are used without a dc bias to determine the pumping direction.

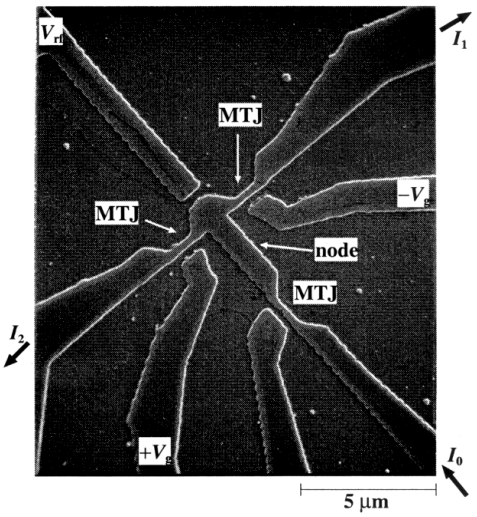

Figure 13. Scanning electron micrograph of a two-way switching device. It consists of three MTJ transistors. After [106].

Figure 14(b)(c) shows the two-way switching characteristics measured at 4.2 K. Gradual switching of the current output between the two branches was observed as V_g was swept. The output current, I_1 or I_2, in the ON state ($V_g = -0.5$ V for I_1 and $V_g = +0.5$ V for I_2) increased linearly with the frequency of the rf waves up to 5 MHz, following Eq. (14). N_c was about 800 in the ON state. The output current was almost zero in the OFF state ($V_g = +0.5$ V for I_1 and $V_g = -0.5$ V for I_2).

The number of electrons transferred in one clock cycle can be reduced by lowering the amplitude of the clocking waves. Two-way switching operation with N_c being as few as 100 was achieved [106].

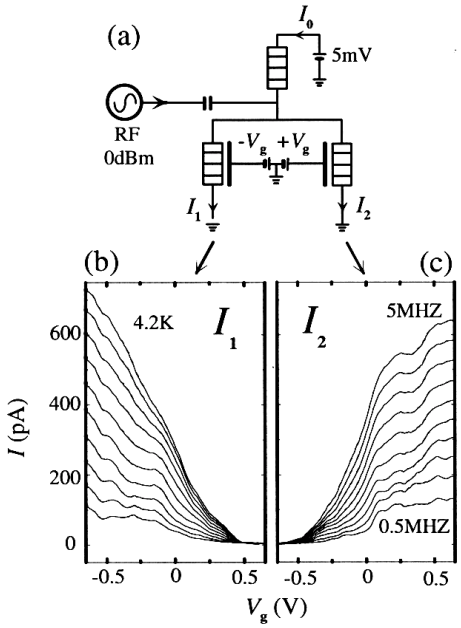

Figure 14. (a) An equivalent circuit of the two-way switching device. (b) (c) Experimental frequency dependence of the output currents I_1 and I_2 at 4.2 K. The clock frequency was changed from 0.5 MHz to 5 MHz. Reprinted with permission from [106]. Copyright 1998, American Institute of Physics.

6 Demonstration of logic operation

We experimentally demonstrated the operation of a single-electron BDD circuit [72]. This was the first experimental demonstration of a single-electron BDD circuit. Our BDD AND circuit consisted of eight MTJ transistors. An atomic-force microscope (AFM) image of the circuit is shown in Fig. 9(b), and its equivalent circuit is depicted in Fig. 9(c). Each MTJ transistor consisted of a gated narrow wire defined in the channel of δ-doped GaAs as illustrated in Fig. 15(a). Typical characteristics of an MTJ at 1.8 K are shown in Fig. 15(b)–(e). X_1 and X_2 in Fig. 9(a) are the inputs for decision making at the two-way switching nodes on the current paths. A token (electrons) starting from the root can either take path 0, or path 1. If both X_1 and X_2 are 1, the token will arrive at the leaf 1, indicating $X_1 \cdot X_2 = 1$. If either X_1 or X_2 is 0, the token will arrive at the leaf 0 ($X_1 \cdot X_2 = 0$). The structure thus distinguishes $X_1 = 1$ AND $X_2 = 1$ from all other cases. By redefining the branching conditions, NAND, OR and NOR functions can also be realised with the same structure.

There are three possible current pathways as shown in Fig. 9(c), each consisting of a series of four MTJs, i.e. multi-clock MTJ pumps. The pumps were operated under zero dc supply voltage as schematically shown in Fig. 15(f). The phase delay between the triangular clock pulses was set to be half the pulse width as per the result of §4. The MTJs 1 through 4 in Fig. 9(c) were placed in either an ON or OFF state to perform two-way switching as was explained in §5, while the four unmarked MTJs were kept in an

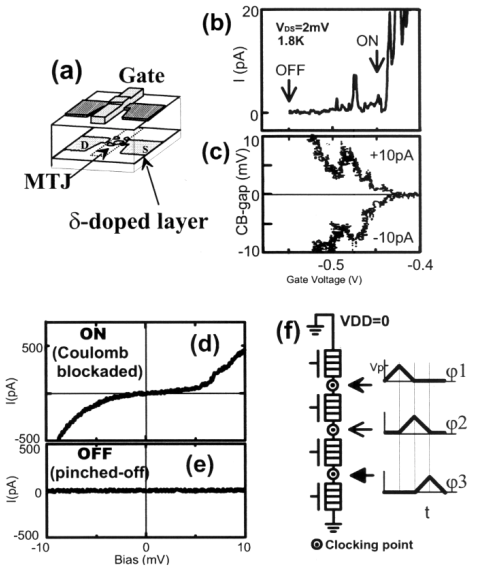

Figure 15. (a) Schematic view of an MTJ transistor in δ-doped GaAs. (b) Typical dc characteristics of an MTJ transistor showing current oscillations. (c) Coulomb gap oscillations due to the Coulomb blockade effect in one of the MTJ transistors in the integrated device. In the MTJ transistor, the periodic rhombic (diamond) Coulomb gap as in Fig. 5 is not observed because multiple size-varied islands contribute to the conduction. Typical current-voltage characteristics in the (d) ON and (e) OFF states. (f) Clocking scheme used to transfer electrons. V_p is the height of clock pulses. Reprinted with permission from [72]. Copyright 1998, American Institute of Physics.

ON state. In the ON state [Fig. 15(d)], the MTJ is in the Coulomb blockade regime, so that a voltage across the MTJ larger than the Coulomb gap results in passage of electrons by single-electron tunnelling. In the OFF state [Fig. 15(e)], a larger negative side-gate bias is applied to completely pinch off the conduction channel, and the voltage pulses have no effect.

In our AND device, the first two-way switching node X_1 is formed by the combined operation of MTJ1 and MTJ2 [Fig. 9(c)]. If MTJ1 is ON and MTJ2 is OFF, corresponding to $X_1 = 0$, electrons flows out through the left-hand branch, towards OUT-0. If MTJ1 is OFF and MTJ2 is ON, corresponding to $X_1 = 1$, electrons move through the right-hand branch. Likewise, MTJ3 and MTJ4 together form the second two-way switching node X_2. The state with MTJ3 = ON and MTJ4 = OFF corresponds to the input $X_2 = 0$. This relation is summarised in Fig. 9(d). If both X_1 and X_2 are set to 1, a current is detected at the current amplifier OUT-1, otherwise, a current is detected at OUT-0.

Figure 16 shows the results of measurements of the logic circuit at 1.8 K that demonstrate the AND function.[13] As shown in Fig. 16(a), there are four possible

[13]In a more recent experiment of a single-electron BDD circuit, a much higher operation temperature of 120 K was achieved [109].

combinations of inputs to X_1 and X_2. The input signals were maintained for 2.4 s. Figure 16(b) shows the clear distinction between the high and low states at the leaves, depending on whether a token have arrived or not. For the pulse height of V_p = 100 mV with f = 1 MHz, the output current in the high state was − 800 pA, and that in the low state was less than the noise level (approximately 1 pA). Note that the shape of the output pulses matches that of the input pulses and that overall, the output corresponds to that presented in the truth table of Fig. 9(d). The amplitude of the output current decreased as V_p was reduced. At V_p = 25 mV, the logic function was still operational, but fluctuations in the output currents were pronounced [Fig. 16(c)]. As shown in Fig. 16(d), output current was proportional to V_p as long as V_p lay above the Coulomb gap.

In Fig. 17, we plot the change in the output current as a function of the clock frequency f for V_p = 40 mV. The open circles show the current measured at OUT-0, and the filled circles show the current measured at OUT-1, for frequencies between 0.2 MHz and 1.5 MHz. The amplitude of the pump current at OUT-1 was zero (within the noise level) and independent of f, while the amplitude at OUT-0 increased linearly with f up to 1 MHz. The linear frequency dependence indicates that the pump current might be generated by sequential transfer of electron packets, each of which contains a fixed

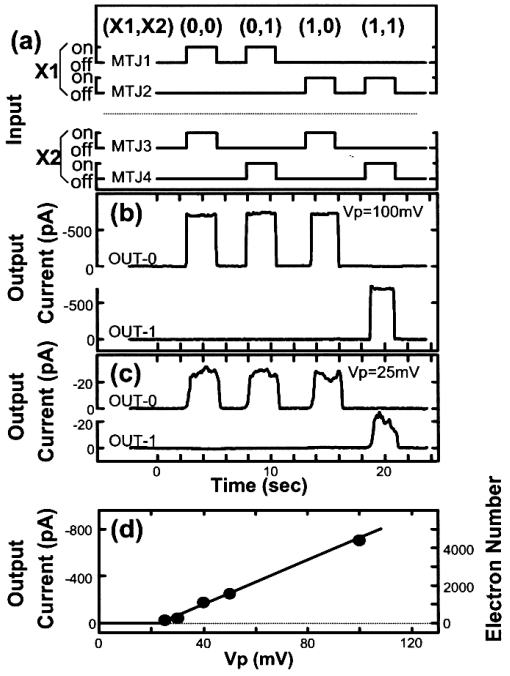

Figure 16. (a) Input signals to the gates of MTJ1–MTJ4. The typical voltage is − 0.55 V for the pinch-off (OFF), and − 0.45 V for the Coulomb blockade (ON) state. Output current for V_p = 100 mV (b) and 25 mV (c). The clock frequency is 1 MHz. (d) Output current as a function of V_p at 1 MHz. The right axis shows the electron number transferred in each clocking modulation cycle calculated from Eq. (14). The solid line is a guide to the eye. Reprinted with permission from [72]. Copyright 1998, American Institute of Physics.

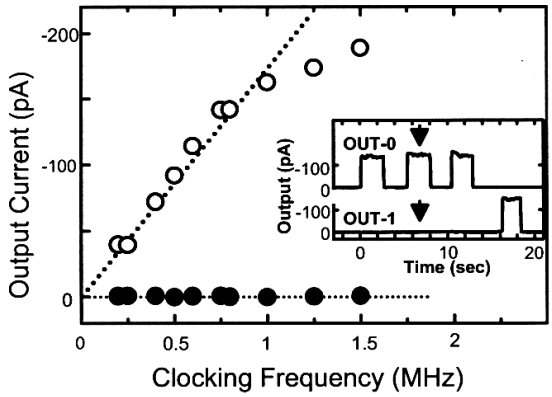

Figure 17. Frequency dependence of the output current for V_p = 40 mV at OUT-0 (open circle) and OUT-1 (solid circle) measured at the point indicated by the arrows in the inset. The dotted lines are guides to the eye. Reprinted with permission from [72]. Copyright 1998, American Institute of Physics.

number of electrons. If so, the number of electrons per packet would depend on V_p as shown in Fig. 16(d), but should be independent of f below 1 MHz. Using Eq. (14) and the slope of the data, we estimated N_c to be 1080 for V_p = 100 mV. An estimate made for V_p = 25 mV showed that a minimum of 160 electrons per packet was needed for measurable logic operation.

Previously, BDD logic architecture has been Clocking Frequency (MHz) used in conjunction with MOS devices to create what is known as MOS pass-transistor logic circuits [110]. The MOS pass-transistor circuits have several advantages over conventional circuits based on logic gates, including higher packing density, lower power consumption, higher speed. The main disadvantage is that repeated connection of MOS switches results in a high series resistance, requiring higher supply voltage. With the standard supply voltage, the number of switching nodes in series is limited to four or five. The multi-clocking scheme we employed overcomes this problem, and in principle allows the series connection of a large number of switching nodes without dc supply. Since this system will only allow combinational logic, any feedback functions, such as latch function, have to be implemented by some other means.

7 Performance estimation

The experimental demonstration of the operation of a BDD circuit [72], described in § 6, served as proof of the concept which we discussed in § 3.6. The circuit, however, is still not so useful for practical purposes. Much higher operation temperature and also large-scale integration should be pursued. For such pursuits to be fruitful, it must have a real advantage (e.g. lower power) over existing circuits when fabricated with more advanced technology yet to appear in the future. In the conventional CMOS logic circuits, the power consumption of a logic gate is given by

$$P = f \times q \times V_{dd}, \tag{15}$$

where $q = C_L V_{dd}$ is the amount of the charge that flows from the dc supply line to the ground per clock cycle, V_{dd} is the dc supply voltage, and C_L is the effective load capacitance [111]. Since our circuit is operated under zero dc bias, Eq. (15) is not directly applicable. To assess the possibilities of our circuit architecture, we analysed the operation of the building block of the circuit, the multi-clock pump, within the semiclassical model [28]. The primary purpose of this analysis was not the fitting of experimental data—the general agreement between experimental data and an account given by semiclassical theory was satisfactory. Rather, we were interested in the best possible performance of the pump in idealised situations. Such an analysis makes it clearer whether the architecture, in principle, has the potential for real application.

A circuit diagram of a multi-clock MTJ pump is shown in Fig. 18(a). As mentioned in §2.3, clocking-gate capacitances C_{Gi} are assumed to be much larger than other capacitances in the circuit. It ensures that tunnelling of an electron onto or out of a clocked node does not change its voltage very much. Each MTJ transistor, therefore, may be regarded as being voltage-biased with relevant island potential(s) ϕ_i and side-gate bias V_{gi} [28,68]. The virtual isolation of the component transistors enables us to analyse the pump circuit using the Coulomb blockade stability diagrams of each transistor.

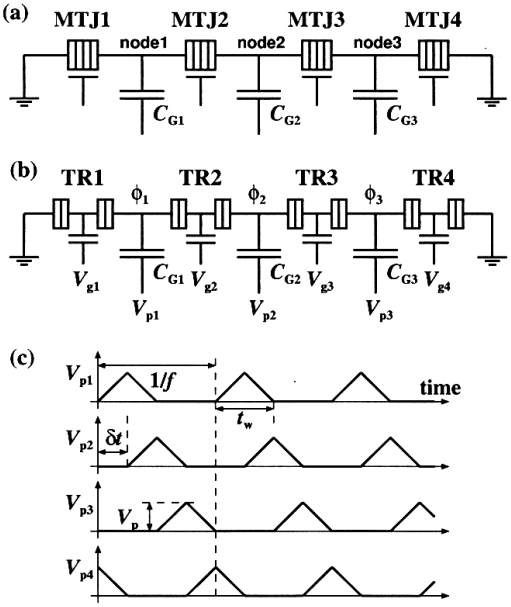

Figure 18. (a) Multi-clock MTJ pump with four MTJ transistors. Clocking-gate capacitances C_{Gi} are much larger than other capacitances. (b) Simpler model of the multi-clock pump, where MTJ transistors are replaced by two-junction transistors of Fig. 3. (c) Up to four triangular pulses are used to drive the pump. Each pulse overlaps with the pulses applied to adjacent clocked nodes. $t_w = 1/2f$ and $f\delta t = 0{:}25$ unless otherwise specified. Electrons are pumped from the left to the right in this example. V_{p4} is not used in (a). It is used if a pump contains more than four MTJ transistors. After [28].

We make the following simplifications. First, MTJ transistors are replaced with two-junction single-electron transistors (Fig. 3) as shown in Fig. 18(b). Then the Coulomb blockade diagrams are given by Fig. 4. This approximation was also employed to analyse the bidirectional electron pump [67,68]. Second, background charge shall be assumed to be zero. Third, the pump is assumed to be uniform; that is, all transistors and C_{Gi} are the same. We analyse the operation of multi-clock pumps under these constraints. As a numerical example, we used the following values: $C_1 = C_2 = 2$ aF, $C_g = 1$ aF, $C_0 = 0.5$ aF [not drawn in Fig. 18(b)], $C_G = 100$ aF and $R_T = 200$ kΩ.[14] With these parameters, the change in ϕ_i due to tunnelling of a single electron is approximately [68] $\delta\phi \approx e/C_G \simeq 1.6$ mV and sufficiently smaller than the other relevant voltage scale $e/C_\Sigma \simeq 29$ mV.

7.1 Charge transport at low temperature

The analysis at the low temperature limit was carried out by extensively using the stability rhomboids of Fig. 4 [28]. A state of a pump can be represented by a point in the high-dimensional space spanned by all ϕ_i and V_{gi}. The point can be projected onto two-dimensional planes corresponding to each transistor, on which the stability rhomboids appear. The state point moves in the space as clock pulses are applied. The locus of the state point at $T = 0$ K is reasonably simple and facilitates understanding of pumping mechanism.

The charge transport mechanism is in fact not so obvious as it might seem. In the case of the four-transistor pump shown in Fig. 18, electrons are pumped from the left end to the right end. When a clock voltage V_{pi} rises, the corresponding island voltage ϕ_i also rises and electrons flow onto the island. Since single-electron transistors are not rectifiers like semiconductor pn diodes, there is no particular reason why electrons should flow only in the "right" direction through them. In general electrons may flow onto the island through both transistors that are connected to it. Which transistor becomes conducting depends on the potential balance in the circuit. Similarly, when V_{pi} falls, electrons may flow out of the island through both transistors. We expressed the pump current by Eq. (14). The N_c in Eq. (14) is the *net* number of electrons transferred per clock cycle, and not necessarily the number of electrons contained in a packet that would move along the pump, if such a packet existed. Electrons that flow in the reverse direction (right to left) consume energy but do not contribute to the net current. For the pump operation to be efficient, electrons should flow only in one direction (left to right). One condition for rectifying electrons is to make the clock pulses appropriately overlap with each other as shown in Fig. 18(c). This is of crucial importance to get a net current as we saw in §4 [71]. Under this condition, we found for $T = 0$ K that almost perfect rectification is possible by properly choosing the side-gate biases of "edge transistors" [TR1 and TR4 in Fig. 18(b)] while setting all other side-gate biases to zero volts [28].[15]

In this optimal condition, the single-electron transistors become conducting one after another, and packets of N_c electrons are indeed conveyed in the pump. Then, the power is given by

$$P = f \times N_c e \times \sum_i V_{\mathrm{diff}}^{(i)}, \tag{16}$$

[14] These are more optimistic than experimental values.

[15] Such "gate-bias tweaking" is something we do not want to do in practice, as discussed in §3.6. We did it in order to find an approximate formula for the power consumption.

where $V_{\mathrm{diff}}^{(i)}$ is the voltage drop across the ith transistor while that is conducting. Equation (16) is readily comparable with Eq. (15). $N_{\mathrm{c}}e$ corresponds to q, and $\Sigma_i V_{\mathrm{diff}}^{(i)}$ corresponds to V_{dd}. $V_{\mathrm{diff}}^{(i)}$ reflects the size of stability rhomboids, and the approximate values of N_{c} and $V_{\mathrm{diff}}^{(i)}$ can be written in terms of the circuit parameters [28]. The estimates thus obtained agree well with results of numerical simulation. A numerical example: $N_{\mathrm{c}} \simeq 46.7$ and $P \simeq 0.6$ pW at $V_{\mathrm{p}} = 100$ mV and $f = 1$ MHz by the derived formulae; $N_{\mathrm{c}} \simeq 45{:}4$ and P $\simeq 0.6$ pW by simulation.

7.2 Temperature and frequency limits

The main effect of non-zero temperature on the pump operation is to cause unwanted leakage current. At $T = 0$ K, the stability rhomboids are delineated by the points with $\Delta F = 0$. However, when $T > 0$ K, there is no clear border between stable and unstable regions; see Fig. 2. At higher temperatures, the locus of the state point is too complex to be useful. Qualitatively, stability rhomboids shrink with temperature, so that pumping survive only near the middle of stability rhomboids. What was optimal at $T = 0$ K is no longer optimal.

Figure 19 shows pump currents in a three-transistor pump as a function of the normalised phase delay $f\delta t$ [Fig. 18(c)] for two different sets of side-gate biases for the

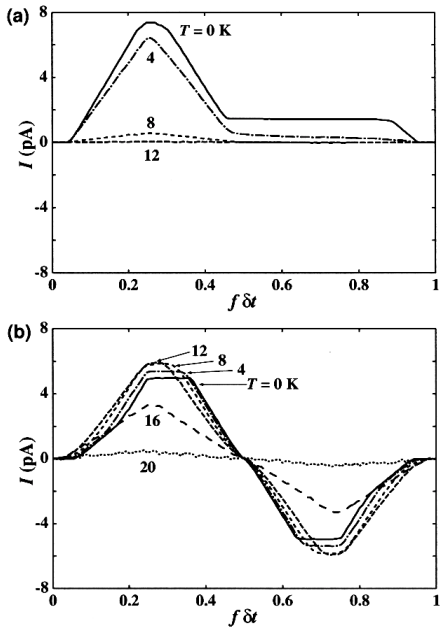

Figure 19. Net pump current versus normalised phase delay $f\delta t$ [Fig. 18(c)] for different temperatures. $V_{\mathrm{p}} = 100$ mV and $f = 1$ MHz. (a) $V_{\mathrm{g1}} = -42$ mV, $V_{\mathrm{g2}} = 0$ V and $V_{\mathrm{g3}} = 42$ mV, which gives an optimal condition at $T = 0$ K. (b) $V_{\mathrm{g1}} = V_{\mathrm{g2}} = V_{\mathrm{g3}} = 0$ V, which gives the "middle-of-rhomboids" condition. Reprinted with permission from [28]. Copyright 2001, American Institute of Physics.

edge transistors. We saw in §4 that experimentally, $f\delta t = 0.25$ was optimal [71]. Also both positive and negative currents were observed as the phase delay was changed, as shown in Fig. 11. Figure 19(a), which is in an optimal condition at $T = 0$ K, shows very different results, indicating the strong rectification in that condition—positive current is seen even for non-optimal ($f\delta t$ 6 = 0.25) phase delays. However, as the temperature becomes higher, the net current vanishes rather quickly. In contrast, in the "middle-of-rhomboids" condition, pumping persists up to much higher temperatures as shown in Fig. 19(b). The higher temperature results in Fig. 19(b) are in good qualitative agreement with the experimental results of Fig. 11. [16] We suppose the experiment was carried out in this regime.

The two characteristic temperature scales involved in the pump are $e^2/(C_\Sigma k_B) \simeq 338$ K and $e^2/(C_G k_B) \simeq 18$ K. The highest operation temperature is determined not by the small island capacitance C_Σ of the transistors but by the comparatively large clocking-gate capacitance C_G [28]. This is because the state point spends much of the time near Coulomb blockade borders, where the energy barrier for unwanted tunnelling is of the order of $e\delta\phi \approx e^2/C_G$ [68]. Figure 20 plots the current and the power versus temperature for pumps with different numbers of transistors. Figure 20(a) and (c) are in an optimal condition at $T = 0$ K and Fig. 20(b) and (d) are with zero side-gate biases ("middle-of-rhomboids"). Again, the latter tends to give more current at higher temperatures. The results confirm that the highest operation temperature is determined by C_G. The results of Fig. 20 also suggest that the estimates of N_c and P [Eq. (16)] for $T = 0$ K can still be used for moderate temperatures.

Too high a clock frequency f leads to missed tunnelling events. After a state point has crossed a stability border, there is a finite time delay before tunnelling takes place.

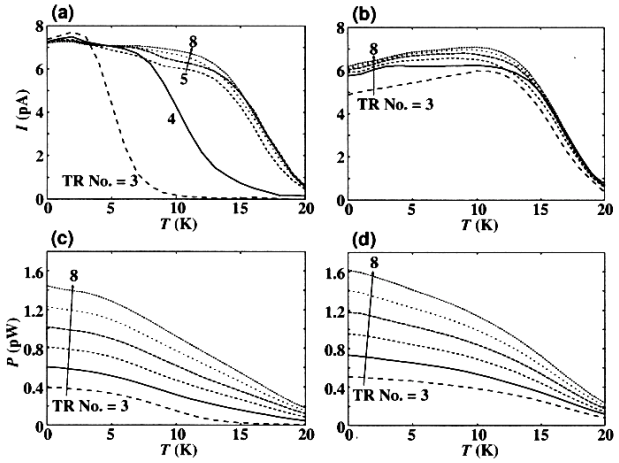

Figure 20. Current and power versus temperature for different numbers of transistors in a pump. (a) and (c) are in an optimal condition at $T = 0$ K. (b) and (d) are in the "middle-of-rhomboids" condition. Reprinted with permission from [28]. Copy-right 2001, American Institute of Physics.

[16] The absence of a flat region between the peak and the trough in Fig. 19(b) is due to the different pulse width (in $1/f$), shown in Fig. 18(c), from that in Fig. 11(a).

At moderate frequencies, the delay is less than the time it takes ϕ_i to change by $\delta\phi$, which we write as $t_{\delta\phi} \approx (\delta\phi/V_p) \times (1/4f)$. If the delay is comparable to or longer than $t_{\delta\phi}$, a pump cannot fully respond to the clock signals and the pumping operation deviates from ideal [28,68]. The upper frequency limit f_{max} for vanishing temperatures can be estimated as follows. The time delay $t_{\delta\phi}$ approximates to the inverse of tunneling rate Γ^{-1}. On a border of Coulomb blockade, $V_{i,f} \approx \pm e/2C_\Sigma$, and at a sufficiently low frequency $V_i + V_f \to 0$ and, of course, $\Delta F \to 0$ [see Eq. (8)]. In the higher frequency range in which we are interested now, $V_i + V_f \approx \delta\phi$ because of the delay, and hence $\Delta F \approx -e^2/2C_G$. Using Eq. (7) and $I(V) = V/R_T$ at $T \to 0$ K,

$$\frac{4V_p f_{max}}{\delta\phi} \approx \Gamma \approx \frac{\delta\phi}{2eR_T}. \tag{17}$$

We therefore obtain

$$f_{max} \approx \frac{e}{8V_p R_T C_G^2} \tag{18}$$

as a rough estimate of the frequency above which the pump operation is expected to degrade. Our numerical example gives $f_{max} \approx 1 \times 10^8$ Hz, which is also confirmed by simulation [28].

At non-zero temperatures, the delay becomes shorter and thermally activated tunnelling (with $\Delta F > 0$) also occurs. Thermal errors affect pumping more at low frequencies [68]. The upper frequency limit does not differ significantly from that for the zero-temperature case [28].

8 Discussion

8.1 Power consumption

The estimated operation temperature and frequency are not particularly high even with the relatively optimistic numerical values we used as an example. The power consumption, on the other hand, is very low. This is because of the small number of electrons involved and the low operation voltage [28]. Operation with a much higher clock frequency, e.g. f_{max}, is perfectly acceptable in this capacitance range, as far as power is concerned. With present-day technology, we usually have very small $V_{diff}^{(i)}$; less than 10 mV in Fig. 15(c). If the entire circuit is scaled down with keeping the ratio C_Σ/C_G constant, higher operation temperature and frequency would be achieved in theory. At the same time, $V_{diff}^{(i)}$ will become larger. Consequently, the power consumption increases by the scaling if f and N_c are held constant. If the voltage and the frequency become comparable with those used in conventional circuits, the difference in power consumption would essentially arise from the difference in the amount of charge used, namely $N_c e$ in Eq. (16) and q in Eq. (15).[17] Typically q/e is over 10^5, whereas $N_c < 10^3$ in our experiment. N_c could be made smaller by reducing the clock amplitude V_p. Of

[17] Note that in Eq. (16) what changes automatically by scaling is only $V_{diff}^{(i)}$. Although f_{max} and N_c are affected by scaling, choice of f and N_c, which is controllable through V_p [28], is still left to the user.

course, whether such miniaturisation is possible is another issue. Also, we did not consider the change in R_T by scaling. It is possible that R_T becomes larger by scaling down and limits f_{max}.

8.2 BDD token

In the experiment of § 6, many electron packets were used as a token for BDD [72]. It is hoped that only one electron packet is sufficient as a token, thereby realising a high throughput. We found by simulation that it takes several cycles for a pump to settle into a steady operation mode [28]. Furthermore, the longer the pump is, the longer it takes to settle. This implies possible difficulty with the single-packet operation scheme. Further study is needed to explore the prospects for efficient operation.

8.3 "Single-electron" logic?

There are, in theory, a number of ways to utilise characteristics of single-electron devices. The operation of our multi-clock MTJ pump and BDD circuit are based only on the nonlinear current-voltage characteristics of MTJs [Fig. 1(e)], which are fairly robust. Even the exact shape of the current-voltage curves is not so important. Some immunity to uncontrollable circuit parameter dispersion was procured precisely because of this,[18] as was discussed in §3.6. Indeed, the origin of the nonlinear *I-V* need not be Coulomb blockade of single-electron transfer. If some different physical effects were in use, it would no longer be "single-electron" logic. We think this is a strength of our circuit architecture rather than weakness. After all, our ultimate aim is to establish a technology for constructing low-power, high-density circuits for the future. Use of the single-electron charging effect is just one of many possible options. If more robust physical effects are found which exhibit similar *I-V* characteristics, our architecture could be reused.

8.4 Operation temperature

In order to realise high-temperature (or room-temperature) operation, the devices have to be made much smaller. No device reported so far, perhaps apart from some memory devices, appears to be sufficiently small—small at the level which enables one to construct useful circuits, rather than just showing a trace of Coulomb blockade. Accordingly, a great deal of effort has gone into attempts at miniaturisation. Some estimates have already been made of miniaturisation requirements for some specific systems [4,113]. Here we give an estimate of how far we could go on a very rough but quite general argument.

The quantity of interest is capacitance. In principle, no lower limit exists for capacitance between two conducting bodies. One can make it arbitrarily small by placing them far apart. However, a lower limit does exist for tunnel capacitance because the two conductors have to be in close proximity to each other for charged carriers to be able to tunnel between them in a realistic time. If one makes the conducting bodies smaller and smaller, the capacitance between them approaches that between two spheres, regardless of the shapes of the conducting bodies. Therefore, we will consider two spherical conductors as shown in Fig. 21.

[18] Still more aggressive defect-tolerant approach might be necessary in practice [112].

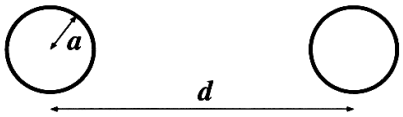

Figure 21. Two conductive spheres of radius a, separated by distance d.

Let the radius of both spheres be a. To make the mutual capacitance small, a must be as small as possible, and the distance d between them must be long, yet tunnelling has to occur.[19] The approximate capacitance in a vacuum is, provided $a \ll d$,

$$C \approx 4\pi\varepsilon_0 \frac{a^2}{d}. \tag{19}$$

Note that $4\pi\varepsilon_0 \simeq 1 \times 10^{-10}$ F/m. With rather optimistic values of $a = 5$ Å and $d = 50$ Å, $C \simeq 5 \times 10^{-21}$ F. In practical systems, the dielectric constant is larger, and therefore C is larger. We speculate that the smallest possible tunnel capacitance might not be much smaller than around 0.1 aF. Very small capacitances close to this value have recently been reported [114, 115]. If we naively scale down the numerical example in §7.2 to have the smallest tunnel capacitance of 0.1 aF, room-temperature operation could be only just possible. Note that what determines the operation temperature is not the tunnel capacitance but the total capacitance of the islands involved. The limit to the smallest possible total capacitance of a dot may therefore be even tighter. It might seem that room-temperature single-electron logic is rather difficult to realise.

Our experimental data showed some characteristics presumably due to some kind of quantum mechanical effect. Quantum mechanical effects could possibly be exploitable for raising the operation temperature. However, we have ignored them in this article because so far they have hardly been useful for application. They add more dispersion in device characteristics and are not as robust as the single-electron charging effect at high temperatures. From a practical standpoint, we think that at least some proof-of-concept experiments have to be conducted before we can invoke them with confidence as a possible solution to real problems [116].

Finally, we would like to emphasise that our argument about the miniaturisation limit is valid only within the very simple model that we used. No result will be obtained that cannot be produced from the model. To make better predictions, the model has to be modified. Also, the reservations mentioned in the last paragraph is not even based on any model. The continuous efforts being made may prove such concern inconsequential.

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[19] Actually, d could be made large if the use of a high voltage is acceptable. However, that might defeat the low-power advantage.

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