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On-die parameter extraction from path-delay measurements

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***Abstract*— Device-parameter estimation through path-delay measurement, which facilitates fast on-die performance prediction and diagnosis, is proposed. With the proposed technique, delays of a set of paths consisting of different logic cells are monitored. Based on the pre-characterized parameter to delay sensitivity, the process variation of a chip is estimated as an inverse problem. Discussion of desirable logic cell combination to form paths that maximize estimation accuracy is presented. Measurement of ring oscillator arrays composed of standard and customized logic cells resulted in consistent estimation of threshold voltages. Measurement accuracy is greatly enhanced by the proposed good logic cell combinations.**

I. Introduction

With the progress of technology scaling, process variation is beginning to significantly impact on product performances such as maximum operation frequency, power consumption, etc. The variation of the number of dopant atoms in the device-channel region and the thickness variations of the gate oxide are unignorable in designs using recent technologies. This results in threshold voltage mismatch between transistors on a chip and delay variation of logic gates.

In order to improve yield and reliability, several methods have been proposed. Post-fabrication tuning of substrate bias is proposed [1] trying to compensate threshold-voltage variation. The adaptive test technique, which alters test-paths chip by chip, has been proposed to evaluate path delays accurately [2], [3]. Those techniques are based on the assumption that accurate device parameters of each chip are readily available. Traditionally, the device parameters are obtained through I-V curve measurement [4]. It provides us with sufficiently reliable information for device modeling. However, it requires analog voltage and current measurements, which can only be measurable by the special equipments outside of a chip. For simple and fast characterization of AC characteristics of digital CMOS circuits, ring oscillators are often used [5]. Ring oscillators can be easily embedded in a product chip to diagnose chip performance at wafer-test time or even after product shipment. Change of the measured oscillation frequency indicates process variation or temperature change. However, what the frequency of a ring oscillator tells us is that the chip can operate how fast or slow. It has been impossible to know exact parameter variations by a ring oscillator measurement alone.

In this paper, we propose an estimation method of the device parameters, such as threshold voltages or device-channel lengths, which have dominant influence on delay fluctuation. Path-delay measurement of different logic cells with their pre-characterized delay sensitivity to individual process parameters enables reverse calculation of process variations. Using logic cells that have different delay-sensitivity to parameter variations, parameter extraction becomes possible. We first describe parameter estimation framework, then discuss design guideline including the choice of logic cell combination. We then propose a special cell that is suitable for parameter extraction. Test-chip measurement results of a 65-nm process will be also presented.

II. Parameter estimation through path-delay measurements

A. Key concept

Path delay t_d is expressed using the following first order canonical form [6].

$$t_d = td_{typ} + \sum_{i=1}^{n} s_i \Delta p_i + N(0, \sigma_{rnd}^2) \quad (1)$$

Here, td_{typ} is the nominal delay, Δp_i and s_i represents the global variation of an i-th parameter p_i and its sensitivity, and the random component $N(0, \sigma_{rnd}^2)$. This form is often an output of statistical static timing analyzers (SSTA).

The aim of our work is to estimate Δp_i from measured path-delays. By measuring two or more number of paths that have different sensitivities to the device parameters, we can estimate parameters as follows.

$$\Delta P = S^{-1} \cdot \Delta T_D \quad (2)$$

In this equation, the random component in Eq.(1) is ignored. This situation can be achieved either a path is composed of a large number of logic cells, or large number of paths are used for averaging. As a realistic example, when nMOS and pMOS threshold voltages are the device parameters of interest, Eq.(2) becomes

$$\begin{bmatrix} \Delta v_{tn} \\ \Delta v_{tp} \end{bmatrix} = \begin{bmatrix} S_{vtn1} & S_{vtp1} \\ S_{vtn2} & S_{vtp2} \end{bmatrix}^{-1} \begin{bmatrix} td_1 - td_{typ1} \\ td_2 - td_{typ2} \end{bmatrix}. \quad (3)$$

Here, S_{vtn1}, S_{vtp1} are the sensitivities of the first path to nMOS and pMOS threshold voltages, respectively. S_{vtn2} and S_{vtp2} are defined similarly. As long as the paths are chosen so that sensitivity matrix S becomes non-singular, we can estimate Δvtn and Δvtp by measuring two path delays. The sensitivity matrix can be obtained by circuit simulations, or from SSTA report. Here, delay-average of the path over all chips can be used as the typical delay td_{typ}.

This idea can be extended to quadratic delay model to improve accuracy for wider variation range.

$$td = td_{typ} + S'_{vtn} \cdot \Delta v_{tn}^2 + S_{vtn} \cdot \Delta v_{tn} + S'_{vtp} \cdot \Delta v_{tp}^2 + S_{vtp} \cdot \Delta v_{tp} + S_{vtnp} \cdot \Delta v_{tn} \cdot \Delta v_{tp} \quad (4)$$

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The quadratic model improves estimation accuracy significantly. Resultant simultaneous equation does not have closed-form solution thus solving them for threshold voltages involve numerical calculation. In the similar manner, the estimation of three parameters such as adding channel-length variation ΔL becomes possible.

B. Choice of logic cell combination

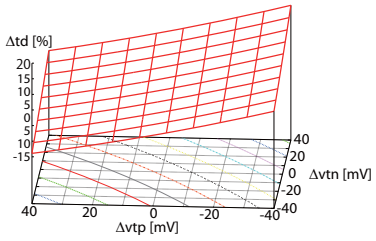


Fig. 1. Response surface of 20-stages inverter delay.

In order to realize parameter estimation, we first need to calculate delay-sensitivities of each parameter. Figure 1 shows the response surface of delay as function of threshold voltages Δvtn and Δvtp for 20-stages inverter chain. Even for this limited range of parameter variation, it is necessary to use quadratic delay model due to its non-linearity.

Now, we discuss a good choice of logic cell combination and draw guidelines to achieve accurate parameter estimation. We here consider five standard logic cells, inv, nand2, nand4, nor2, and nor3, and two special cells, nnmos and ppmos, as the path-component. The nnmos (ppmos) is newly designed so that it has stronger sensitivity to threshold voltage of nMOS (pMOS) than other logic cells. The detailed composition of the cell is described in Sec. III-B. Figure 2 shows the sensitivity vectors $\vec{s}$ of seven ring oscillators composed of each cell. The sensitivity vector is defined as a first derivative of delay-response surface at the origin. In other words, components of $\vec{s}$ are coefficients of Δv_{tn} and Δv_{tp} in Eq. (4).

Each logic cell has similar but different sensitivity to nMOS and pMOS threshold voltages, thus the choice of the cell is important to attain accuracy. In general, the estimation error is well described by the *condition number* of sensitivity matrix.

$$cond = \|S\|_\infty \cdot \|S^{-1}\|_\infty \tag{5}$$

Here, $\|S\|_\infty$ is infinity norm of matrix S. When the angle formed by any pair of sensitivity vectors increases, condition number becomes large. The error is also affected by the maximum Δtd, i.e. the length of the sensitivity vector. In order to make normalized comparison, the number of stages of each path is adjusted to have the same maximum Δtd. Figure 3 shows the estimation error of the Δvtn and Δvtp with different cell combinations. The parameters are estimated by solving quadratic delay-equations numerically for 25 points (Δvtn and Δvtp are changed by 20 mV step from -40 mV to 40 mV). An error of ± 31.25 psec is added to the delay to represent timing error of a tester. It is shown that the estimation error becomes small as the condition number becomes small.

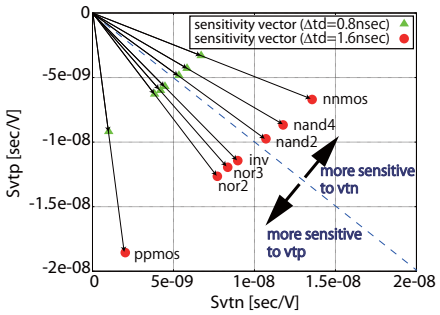
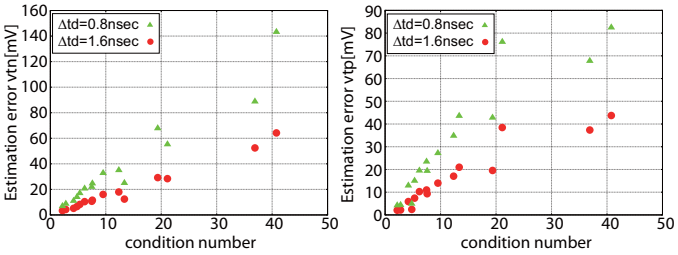


Fig. 2. Sensitivity vectors of seven paths.



(a) Δvtn estimation (b) Δvtp estimation

Fig. 3. Estimation accuracy vs. condition number of sensitivity matrix.

Similarly, the larger maximum Δtd improves estimation accuracy for a constant delay-measurement error. It is concluded that we should choose cell combination so that the condition number of sensitivity matrix becomes small.

III. Test Chip Measurement

A. Circuit structure

As a proof of concept, the ring oscillator array (ROA) is designed. The implemented ROA consists of 512 ring oscillators having different logic-cell types and different number of stages. Each ring oscillator is composed of a single type of logic cell. Table I shows cell types in the ROA. Number of ring oscillators included in an ROA is also listed. All ring oscillators have four different stages — 21, 41, 81, and 161. Output of each ring oscillator is locally divided by 2^4, 2^3, 2^2, and 2^1, respectively. Output frequency becomes almost the same regardless of the number of stages, which makes supply voltage drop almost equal.

TABLE I
LOGIC CELLS USED FOR RING OSCILLATORS.

cell name	number	cell name	number
nand2	16	inverter	24
nand4	8	ppmos	8
nor2	16	nnmos	8
nor3	8	others	32
mux2	8		

A simplified block diagram of the ROA is illustrated in Fig. 4. A block of ring oscillator is selected using one-hot shift resister. Each block is composed of four ring oscillators having different number of stages and local frequency divider. One

of the ring oscillators is chosen by the combination of shift register and the ring-length selection signal RLEN. Output of each ring oscillator is led to multiplexer tree to the output pad. The multiplexer tree and output buffer utilize dedicated power supply to avoid power supply noise for ring oscillators.

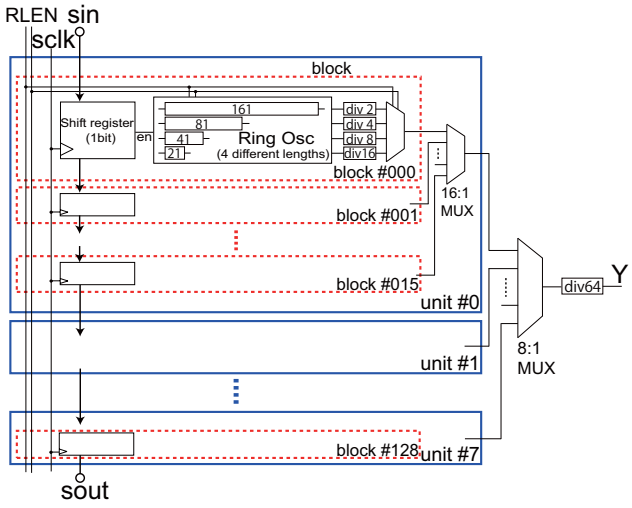


Fig. 4. A structure of a ring oscillator array.

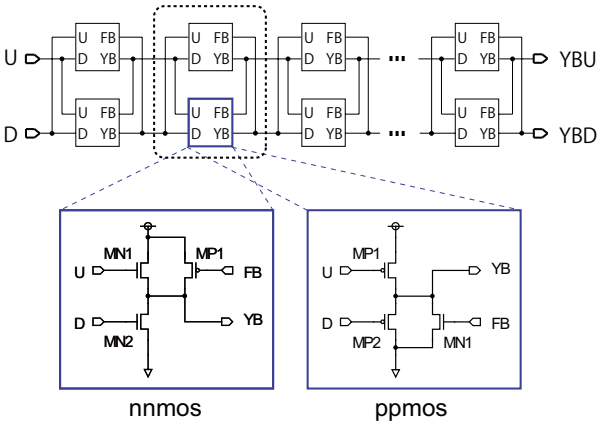


Fig. 5. The proposed custom cells (nnmos and ppmos) suitable for threshold voltage extraction.

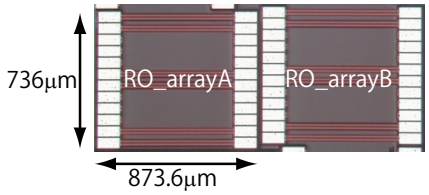


Fig. 6. Chip micrograph of the two ROA.

B. *Special logic cells*

In addition to the standard logic cell, special cells dedicated for the parameter extraction are implemented. For the purpose of accurate estimation of parameters Δvtn and Δvtp, it is desirable to use the cells that have higher sensitivities to a parameter of interest. Considering the simulation result in the previous section, we newly devise cells that are particularly sensitive to either nMOS or pMOS threshold voltages. The schematics of the proposed cells are shown in Fig. 5. In a standard inverter cell, nMOS (pMOS) transistor is responsible for the discharging (charging) of the load capacitance. In contrast, the proposed cells form inverter by a pair of nMOS (pMOS). In order to restore signal level pull-up pMOS (pull-down nMOS) is connected. In the proposed cells, both charging and discharging time are mainly determined by either nMOS (pMOS) only, thus the cells are more sensitive to Δvtn (Δvtp). By using long-channel devices, it can minimize the effects of the channel length variation.

IV. Experimental Results

The ROA is fabricated using 65-nm, 12-metal layer CMOS process. Figure 6 shows chip micrograph. The area of the circuit block of the ROA is 7.2 x 210 μm^2. Total area of the circuit is 736 x 873.6 μm^2. Two ROA circuits are placed on a chip for verification of the measurement result. The two ROA are located next to each other, i.e. the equivalent points of the two ROA are apart by 25 x 880 μm.

Two ROA on 38 chips in a single wafer are measured. Threshold voltages of nMOS and pMOS transistors are estimated using measured frequencies of two ring oscillators composed of different cell types. Figure 7 shows frequency variation over the chips. We see that the oscillation frequency fluctuates more than 6% over the chips in a wafer. We also see that the frequencies are different depending on logic cells. Frequencies of different cell types are following similar trend, but a few chips behave differently. For example, nand4 and nor3 has different sensitivities because of its structural difference in types of stacked transistors. Inv and nor3 are slow in chip-2, which suggests the pMOS threshold voltage of the chip is higher. The threshold voltages of other chips can be examined more systematically by the proposed framework.

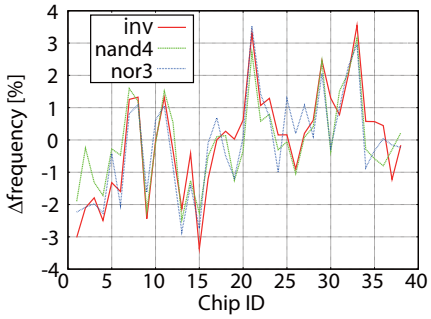


Fig. 7. Measured frequencies of ring oscillators composed of different chips and logic-cell types.

Figure 8 shows the effect of random variation component as functions of number of logic stages. As expected, σ/μ is in proportion to $1/\sqrt{n}$ where n is the number of ring oscillator

stages. The influence of the random variation can be ignored in ring oscillators of 81 and 161-stages. Thus, the results of 161-stages are used in the following analysis.

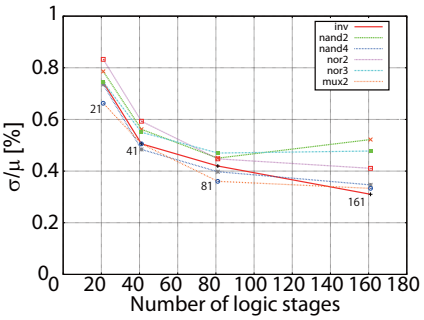
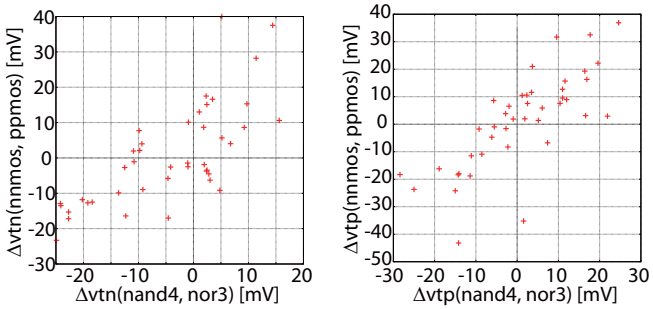


Fig. 8. Vanishing random component as the increase of logic stages of ring oscillator.

Threshold voltages by two sets of cell combinations are extracted and compared in order to confirm consistency of our estimation methodology. The cell combinations used here are (nand4, nor3) and (nnmos, ppmos). Correlations of estimated results are depicted in Fig. 9. The extracted threshold voltages from different pairs of cell coincide very well. The correlation coefficients of the threshold voltages from two different cell sets are 0.728 and 0.767, respectively. It means that the proposed estimation framework works very well and the both pairs are good combination for parameter estimation.



(a) Δvtn. (b) Δvtp.

Fig. 9. Consistency of the estimation using different cell pairs.

Figure 10 compares difference of extracted threshold voltages between circuits A and B. If the threshold voltages calculated by ring oscillators in the two circuits are equal, difference becomes nearly zero indicating that the extraction is consistent. The averaged parameter difference over 38 chips is shown for four cell combinations. The difference of the estimation by using combinations of (nand4, nor3) and (nnmos, ppmos) are less than 5 mV, showing very good match. The combinations of (nand4, nnmos) and (nand2, nand4) cause large error because both cells are sensitive to Δvtn thus have large condition number. Normally, the estimation difference between two identical circuits has to be very small within a few mV, even if we consider possible error components such as systematic trend of a parameter within a chip, delay measurement error, approximation error of response surface

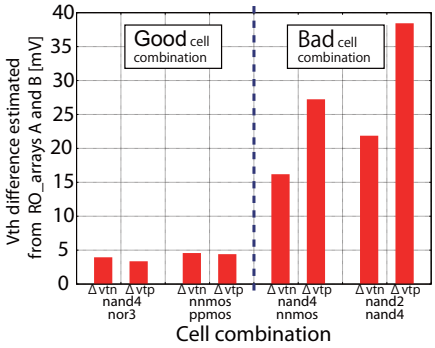


Fig. 10. Difference of vth estimation between circuits A and B.

function, and remaining random variation. The paths of good combination cells apparently give good approximation of the device parameters, as their difference between near-by circuits is very small. The consistency of the estimated result in the ROA circuit confirms that the proposed parameter extraction works well. It is also possible that redundant number of paths can be used to further improve estimation accuracy.

V. Conclusion

A parameter-estimation method suitable for adaptive circuit techniques is proposed. By comprehensive circuit simulations, good logic-cells to form delay-measurement path that yields accurate estimation is discussed. It has been clarified that paths of large delay, and cells combination having condition number as small as possible are important. Following to the above design guideline, a ring oscillator array composed of good path combinations for extracting threshold voltages of nMOS and pMOS transistors is designed. Measurement results showed that the consistency within a chip is less than 5 mV, and estimation accuracy will be greatly enhanced by the newly proposed cells that are particularly sensitive to either nMOS or pMOS threshold voltages.

Acknowledgements

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