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A Scalable Wideband Low-Noise Amplifeir consisting of CMOS Inverter Circuits for Multi-Standard RF Receivers

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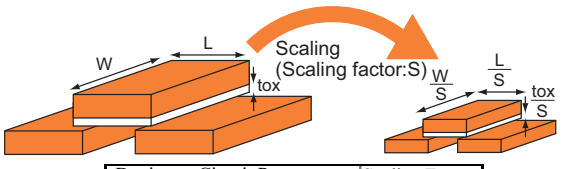
***Abstract*—This paper presents a wideband low-noise amplifier (LNA) architecture that is scalable in terms of the chip area and supply voltage and therefore is expected to offer superior performance with technology scaling. In order to secure low-voltage scalability and allow for potential rail-to-rail operation under an ultralow supply voltage, the CMOS inverter is chosen as the basic amplifier stage. The core of the LNA gain stage comprises two CMOS inverters. To realize wideband operation with area scalability, two band broadening techniques that require neither inductors nor capacitors are adopted. First, to reduce the Miller capacitance, the classic Cherry-Hooper band broadening technique is applied to the CMOS inverter-based amplifier. Second, an active frequency peaking technique is introduced with the use of feedback through another CMOS inverter. The scalability and wideband characteristics of the proposed LNA are confirmed by comparing chips fabricated using 180 nm and 90 nm CMOS process technologies. The LNA in 90 nm CMOS achieved 18.0 dB gain, 0.1–6.8 GHz bandwidth, 3.0–5.5 dB noise figure, and 14.5 mW power dissipation with occupying only 0.0032 mm^2, which is 48 % of the 180 nm CMOS LNA area.**

***Keywords*—Scalability, CMOS, Low-Noise Amplifier, Wideband, CMOS Inverter**

I. Introduction

Si MOS transistors have been achieving higher and higher maximum transit frequency f_{T} and maximum oscillation frequency f_{max}. This has enabled Si CMOS processes to be used for RF circuits in place of conventional compound semiconductor or Si bipolar technologies. Modern multi-standard mobile terminals contain multiple RF CMOS front-end chips. Ideally, all wireless communication standards in the frequency range below 10 GHz should be covered by one low-cost RF CMOS front-end.

CMOS technology scaling has brought enormous progress of digital circuits. It has offered more computing power, smaller area, and lower power. Fig.1 shows the concept of the scaling law. However, RF circuits cannot enjoy the benefits of scaling as much aside from the higher operation frequency of MOS transistors. A large area occupied by inductors and capacitors is a considerable problem. What is worse, they are unlikely to shrink as much as transistors with technology advancement and are expected to account for a growing part of the chip cost [1]. The reduction of supply voltage with technology scaling is another issue. Many conventional RF



Device or Circuit Parameter	Scaling Factor
Device dimension : L, W, Tox	1/S
Doping concentration	S
Voltage	1/S
Electric field	1
Current	1/S
Delay time per circuit	1/S
Dissipation power per circuit	1/S^2

Fig. 1. Scaling results for circuit performance.

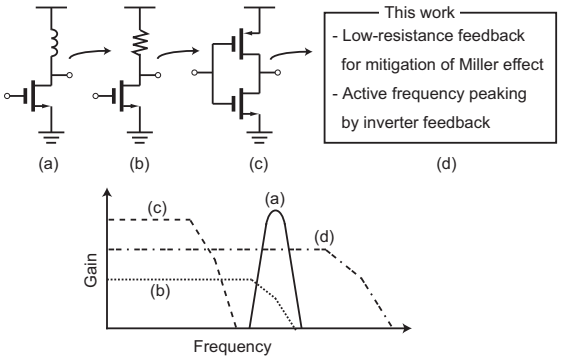


Fig. 2. Design concept.

building-block circuits are becoming unusable or difficult to use because of severely limited voltage headroom. As such, wideband circuits for multi-standard RF applications have to be designed with scalability in mind. Some inductorless LNAs with feedback have been proposed [2]–[4]. In this paper, we present a wideband LNA architecture that is scalable both in terms of area and supply voltage.

II. Design Considerations

Basic common-source amplifier configurations are shown in Fig. 2. The inductor load type amplifier in Fig. 2(a) is suitable for achieving high gain at a high frequency. The design, however, is inherently narrowband and is not suitable for multiband applications. It also lacks scalability because of the inductor.

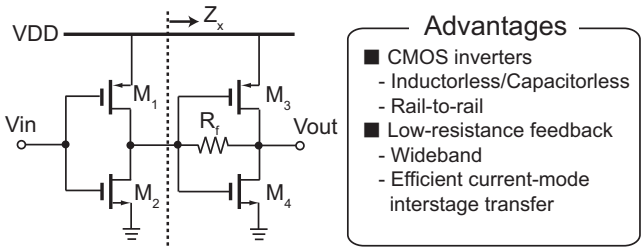


Fig. 3. CMOS inverter-based amplifier with low-resistance feedback.

Fig. 2(b) is the resistor load type amplifier. Its gain is not as high as the inductor load type, but it can be more wideband. The downside is that the MOS transistor has to operate in the saturation region, and the voltage headroom is rather limited under a low supply voltage. A cascode stage suffers from the same problem more badly. In contrast, the CMOS inverter, shown in Fig. 2(c), is free from such a problem. Its output signal swing can be rail-to-rail ($V_{\rm DD}$ to ground) and has excellent low-voltage scalability. We, therefore, choose the CMOS inverter as the core amplifier configuration. Furthermore, in order to get scalable wideband operation, two scalable band broadening techniques are applied.

A. Cascade connection of transconductance and transimpedance type inverters

The Cherry-Hooper amplifier achieves wideband characteristics by cascading amplifiers with an appropriate mismatch [5], [6]. By adapting the same concept to CMOS inverters, one arrives at the cascaded amplifier shown in Fig. 3. Its voltage gain G_{21} at low frequencies is given by

$$G_{21} \simeq (g_{\rm m1} + g_{\rm m2}) \left[R_{\rm f} - (g_{\rm m3} + g_{\rm m4})^{-1} \right], \qquad (1)$$

where $g_{\rm m1}$ through $g_{\rm m4}$ are the transconductances of the transistors M1 through M4, respectively.

The first inverter stage has high input and output impedances and can be regarded as a transconductance amplifier. The second stage, on the other hand, has low input and output impedances because of the feedback resistance $R_{\rm f}$. The second stage, therefore, is a transimpedance amplifier. The effective input capacitance $C_{\rm in}$ of the first inverter stage including the Miller effect is given by

$$C_{\rm in} = C_{\rm gs1} + C_{\rm gs2} + (C_{\rm gd1} + C_{\rm gd2})[1 + (g_{\rm m1} + g_{\rm m2}) Z_{\rm x}], \quad (2)$$

where $Z_{\rm x}$ is the input impedance of the second inverter stage. It is given approximately by

$$Z_{\rm x} \simeq \frac{1}{g_{\rm m3} + g_{\rm m4}}. \qquad (3)$$

and is lower than without $R_{\rm f}$. The Miller effect is thus reduced. Overall, the circuit in Fig. 3 works as a wideband voltage amplifier.

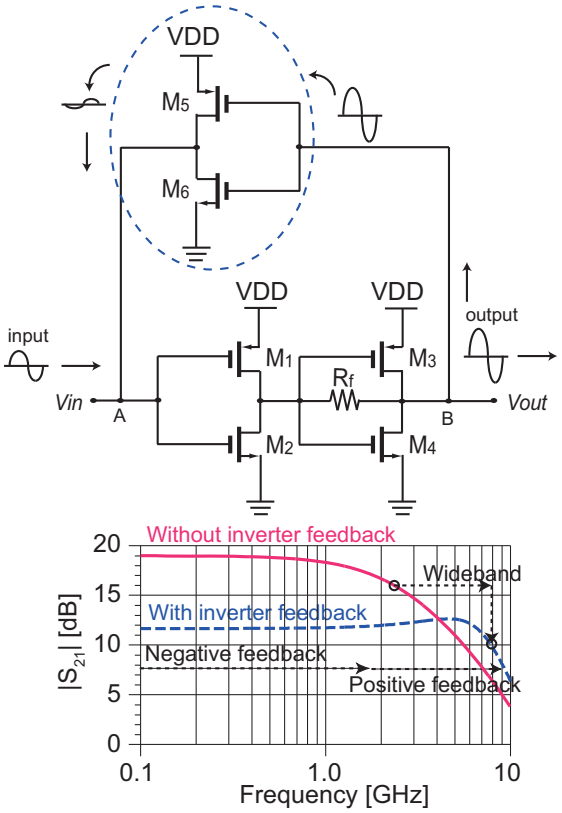


Fig. 4. CMOS inverter-based multi-feedback LNA.

B. Broadbanding by inverter feedback

Inductive or capacitive peaking is a well known and widely used broadbanding technique. Large passive devices, however, seriously impair area scalability. In order to achieve further wideband without inductors and capacitors, we introduce an active peaking technique using a CMOS inverter, which is scalable.

Fig. 4 shows the schematic of the CMOS inverter-based feedback amplifier and frequency dependence of the magnitude of its 50 Ω gain S_{21}. The feedback inverter is much smaller than the two amplifying inverters.

At a low frequency, the phase rotation around the feedback loop is negligible, and the feedback is negative. As the frequency becomes higher, the feedback changes from negative to positive. However, since the loop gain is small enough at such a frequency, oscillation is avoided. Incidentally, the feedback inverter also gives better matching with a 50 Ω signal source.

C. Scalable LNA design

Fig. 5 shows a schematic of the inductorless/capacitorless LNA with the two scalable broadbanding techniques. PMOS transistors are three times as wide as the corresponding NMOS transistors. An additional low-resistance feedback amplifier (Fig. 3) is added to the multi-feedback amplifier shown in Fig. 4. This is to provide a high load impedance to the voltage

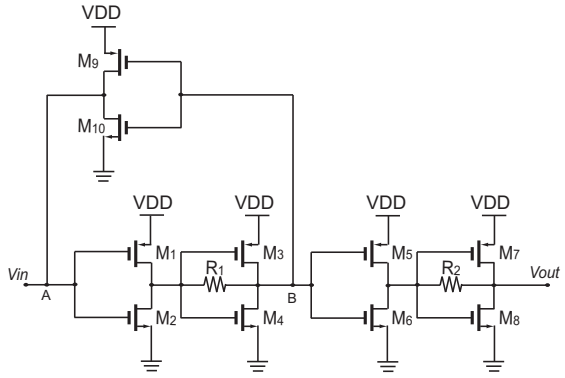
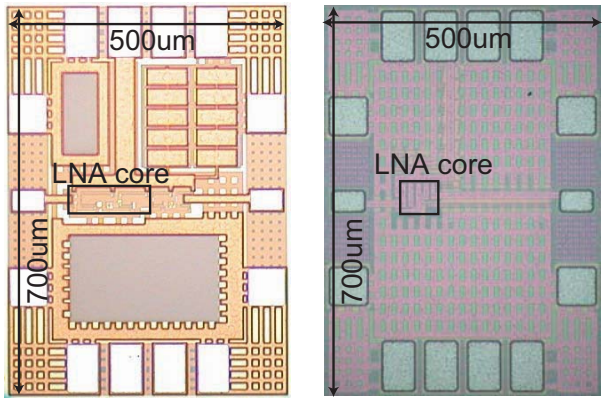


Fig. 5. Schematic of the LNA with output buffer.



(a) 180 nm process chip (b) 90 nm process chip

Fig. 6. LNA chip micrographs.

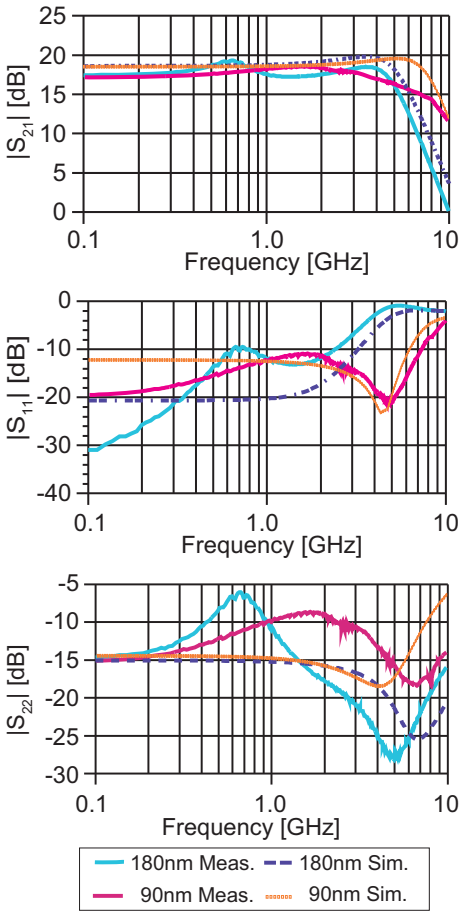


Fig. 7. Measured and simulated S-parameter characteristics.

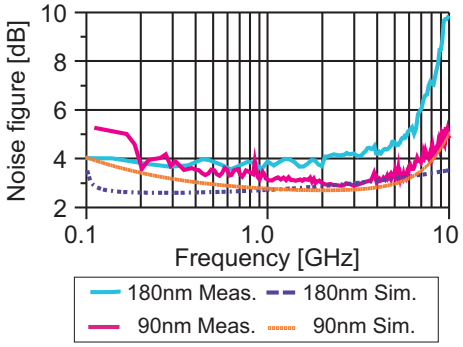


Fig. 8. Measured and simulated noise figure.

amplifier (Fig. 4) and better 50 Ω output matching.

III. Measurement Results

To verify the circuit scalability and the efficacy of the band broadening techniques, the LNA circuit was fabricated with 90 nm and 180 nm triple-well CMOS processes. Fig. 6 shows the chip micrographs of the LNAs. Since the only passive devices used are resistors, the LNA core areas are much smaller than a conventional LNA's with inductors [7]. The area can be further reduced by using advanced process technologies. As shown in Fig 6, the 90 nm CMOS LNA core (Fig. 4) without the output buffer occupies only $54 \times 60\ \mu\text{m}^2$, which is 48 % of the 180 nm CMOS LNA's core area.

Fig. 7 shows the measured S-parameter characteristics. Wideband characteristics of 0.1–6.8 GHz were achieved in the 90 nm CMOS chip. This is 39 % wider than the 180 nm chip. Power consumption was also reduced from 30.6 mW in the 180 nm chip to 14.5 mW in the 90 nm chip. The measured noise figure (NF) characteristics are shown in Fig. 8. NF in the 90 nm chip was 3.0–5.5 dB within 0.1–6.8 GHz. This NF is better than the 180 nm chip's.

A two-tone input signal test was performed. 1 GHz ± 1 MHz were fed to the chips. Fig. 9 shows measured input and output power characteristics. In spite of the low power supply voltage of 1 V, the 90 nm chip achieved higher input third-order intercept point (IIP3) of −12 dBm.

As described above, the proposed LNA can achieve broadband characteristic with lower power and smaller area when more advanced CMOS process technology is used, as shown in Fig. 10. Over-10 GHz operation could be possible when a 45 nm CMOS process is used. Table I gives a performance summary of the proposed inductorless/capacitorless LNA and comparison with other designs.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH OTHER CMOS LNAS.

Source	CMOS technology	Bandwidth [GHz]	Gain [dB]	NF [dB]	IIP3 [dBm]	V_{DD} [V]	Power [mW]	Area [mm^2]
This work	180 nm	0.1–4.9	19.3	3.5–4.7	−14	1.8	30.6	0.0067
	90 nm	0.1–6.8	18.0	3.0–5.5	−12	1.0	14.5	0.0032
[2]	90 nm	0–6.0	15.3	3.4–4.3	NA	1.0	3.4	0.0017
[3]	90 nm	1.0–7.0	17.0	2.4–3.5	−4	1.4	25.0	0.019
[4]	90 nm	0.5–8.2	25.0	1.9–2.6	−5	3	42.0	0.025
[8]	130 nm	2.0–9.6	11.0	3.6–4.8	−7	1.5	19.0	0.05
[9]	65 nm	0.2–5.2	15.6	2.9–3.5	3	1.2	14.0	0.009
[10]	90 nm	0.4–1.0	12.0	4.0–4.5	−16	1.2	18.0	0.12
[11]	90 nm	0.1–8.0	16.0	3.4–5.8	−9	1.4	1.4	0.034

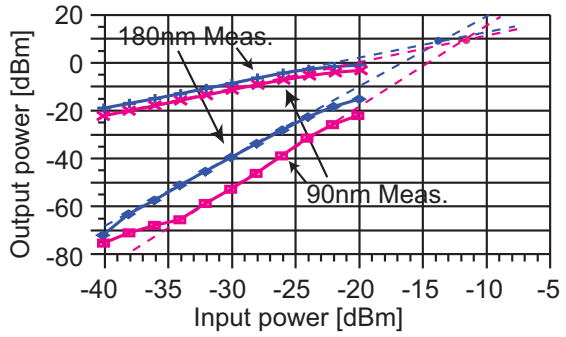


Fig. 9. Measured and simulated fundamental and third-order intermodulation powers versus input power.

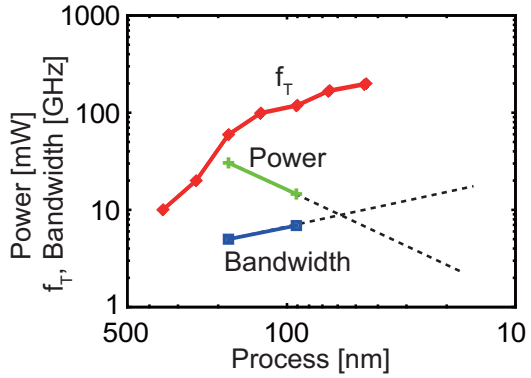


Fig. 10. Process dependence of NMOS f_T, power and bandwidth of the proposed LNA.

IV. CONCLUSION

We proposed a scalable wideband LNA architecture that is expected to give superior performance and smaller area when advanced CMOS processes are used. In order to make it scalable in terms of the power supply voltage, CMOS inverters are chosen as the basic building blocks. The core of the LNA gain stage consists of two CMOS inverters. To make it wideband without area penalties, two kinds of scalable broadening techniques that do not require inductors or capacitors are adopted. First, to reduce the Miller effect, the two inverters are cascaded with a designed mismatch as in the Cherry-Hooper amplifier [5], [6]. Second, active feedback through another CMOS inverter provides high-frequency peaking.

We demonstrated the scalability and wideband characteristics of the proposed LNA by comparing the fabricated chips in 180 nm and 90 nm CMOS. The 90 nm CMOS LNA achieved high performance with a smaller area. Its −3 dB bandwidth was 0.1–6.8 GHz and the peak small-signal gain was 18.0 dB. The NF was 3.0–5.5 dB in the 0.1–6.8 GHz frequency range. The LNA core consumed 14.5 mA from a voltage supply of 1.0 V. It occupied only 0.0032 mm^2.

The scalable wideband LNA architecture proposed is expected to offer wider bandwidth, lower power, and smaller area when used with more advanced technologies.

ACKNOWLEDGMENTS

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