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An 8.9mW 25Gb/s Inductorless 1:4 DEMUX in 90nm CMOS

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***Abstract*—A low-power inductorless 1:4 DEMUX in 90 nm CMOS is presented. It is capable of operating at 25 Gb/s with a power supply voltage of 1.05 V, and the power consumption is 8.9 mW. Its area is $29 \times 40\,\mu\mathrm{m}^2$. The DEMUX consists primarily of latches in differential pseudo-NMOS logic style. This logic style has a near-rail-to-rail logic swing and is much more scalable under low V_{dd} than the current-mode logic, commonly used for high-performance SerDes. It is also compatible with the conventional CMOS logic, and direct connection with CMOS logic gates is possible without logic level conversion. The low power, small footprint, and reasonable speed could be beneficial for chip-to-chip communication within a multi-chip module.**

***Keywords*—DEMUX, divider, multi-phase clock architecture, near-rail-to-rail logic swing, CMOS**

I. Introduction

The amount of data that today's processors have to handle has been growing ever larger. Until recently, performance increase was achieved by raising the clock frequency. Currently, performance increase is gained by using multiple cores on a chip and/or multiple chips packaged together. Efficient communication between cores and chips, therefore, is very important.

With regard to multi-chip modules, various options for chip-to-chip communication are becoming available thanks to recent advances in packaging technology. However, it is not always practical or desirable to have highly parallel interconnects between chips except between a processor chip and memory chips. This is because upper level interconnects involving pads or through-substrate vias (TSVs) impose significant area penalty (e.g. [1]). Interconnects high up in the interconnection hierarchy, therefore, have to be used sparingly. The use of serializers/deserializers (SerDes) could allow high-bandwidth chip-to-chip communication with limited interconnect resources. The SerDes for this purpose has to be small and low-power, as well as high-speed. The requirement is very different from that for optical communication systems.

Another important design consideration for such SerDes is scalability. Ideally, the circuit design adopted should be usable for several technology generations. However, that is often not possible. Majority of CMOS implementations of high-speed SerDes use the MOS current-mode logic (CML) [3], [4]. A schematic of a CML latch is shown in Fig. 1. Since CML is based on a differential amplifier, it has a constant current source, typically realized by a MOS transistor operating in the saturation region. The voltage drop across the current source can easily reach $V_{\mathrm{dd}}/2$ in 90 nm CMOS or beyond, and the source-coupled pair might not have sufficient voltage drop across them required for proper operation.

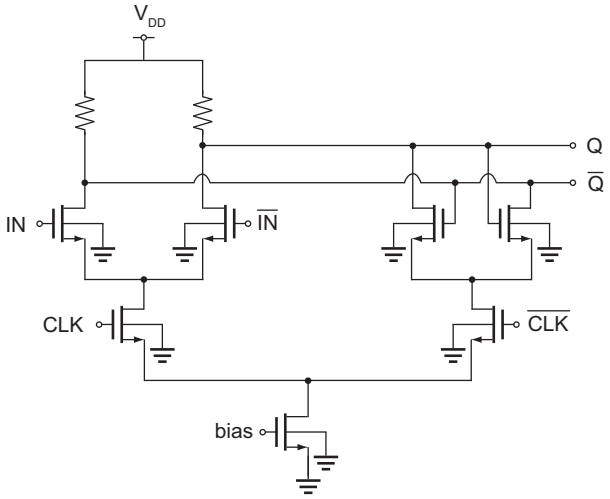

Fig. 1. Current-mode logic type D-latch schematic.

In this paper, we present a DEMUX circuit that is implemented with differential pseudo-NMOS logic style, which we believe is more scalable than and nearly as fast as CML. The differential pseudo-NMOS logic has a near rail-to-rail logic swing, as opposed to less than $V_{\mathrm{dd}}/2$ in typical CML.

The rest of the paper is organized as follows. In Section II, we explain the design of basic circuit blocks used in the DEMUX. Section III describes the architecture of the DEMUX. Section IV presents measurement results and comparison with other work. Finally, Section V concludes the paper.

II. Circuit Design

Component circuit of DEMUX, for example, D flip-flop and frequency divider, consist of combination of D-latches. Performance of the D-latch circuit substantially determines the performance of DEMUX. In this work, we use the differential pseudo-NMOS logic style, introduced earlier in [5] for the D-latch.

Fig. 2 shows a schematic of a D-latch in the differential pseudo-NMOS logic style. A conventional CML type D-latch is shown in Fig. 1. The differential pseudo-NMOS type D-

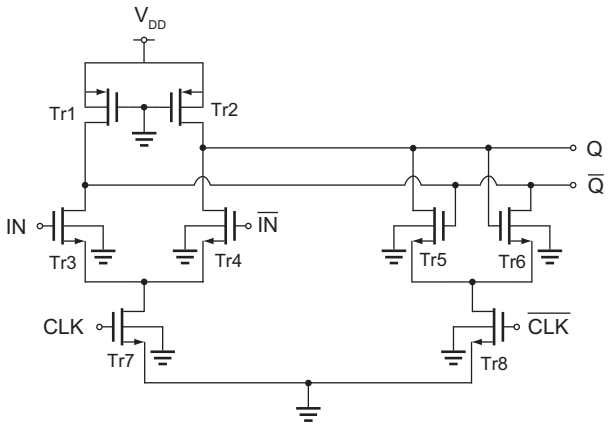

Fig. 2. Differential pseudo-NMOS logic style D-latch schematic.

latch has the tail transistor eliminated as was done in [6], [7], thereby giving larger voltage headroom. In addition, the load resistors are replaced with PMOS transistors operating in the triode region, as in the ordinary single-ended pseudo-NMOS logic [8]. We will refer to this type of load as the PMOS triode [9]. The area occupied by the loads was significantly reduced by the use of PMOS triodes [5]. Furthermore, differential pseudo-NMOS type D-latches operates with a near-tail-to-rail logic swing. The transistors that receive the clock signal are wide, and the voltage drops across them are small.

Frequency divider is a component circuit of the DEMUX. The DEMUX uses a multi-phase clock architecture [5] and is driven by 90-degree phase-shifted clock signals generated by the frequency divider from a half-rate clock. Then, DEMUX needs a high-speed frequency divider. In this circuit, a master-slave type divider [10] consisting of two D-latches is used. Fig. 3 shows the schematic. In the DEMUX, a half-rate clock signal CLK is fed into the divider and 90-degree phase-shifted outputs CLK1 and CLK2 come out.

III. DEMUX ARCHITECTURE

The 1:4 DEMUX architecture is shown in Fig. 4. It uses a multi-phase clock architecture [5]. Fig. 5 shows a timing chart. This architecture splits the input bitstream into four output bitstreams using 90-degree shifted clock signals generated by the frequency divider.

Fig. 6 shows a chip micrograph of the 1:4 DEMUX. The DEMUX comprises a clock divider, clock buffer, and the main DEMUX circuit consisting of D-Latches. One of the four output bitstreams is chosen by the selector circuit, and the selected differential output signal is transform into a single-ended signal before the output buffer. The area of the DEMUX circuit including the divider and the clock buffer is as small as $29 \times 40\,\mu\mathrm{m}^2$.

IV. MEASUREMENT RESULT

A pulse pattern generator (PPG) was used to generate the input pseudo-random binary sequence (PRBS). The output error was measured using and an error detector. We judged the output to be error-free if the error rate was less than 10^{-10}.

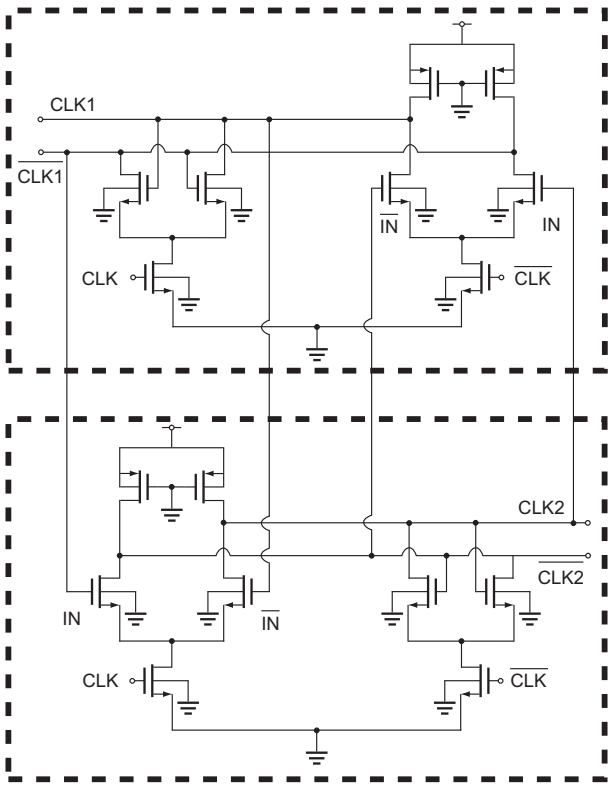

Fig. 3. Divider schematic.

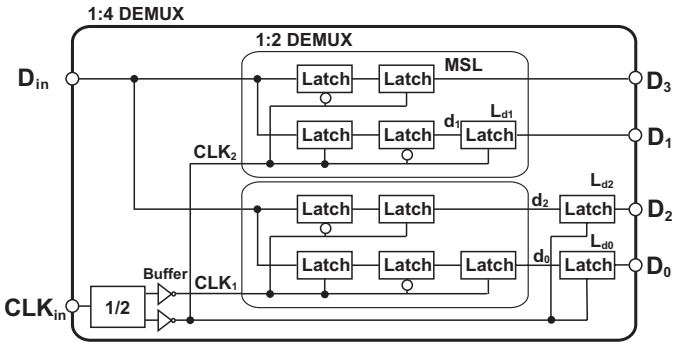

Fig. 4. DEMUX architecture.

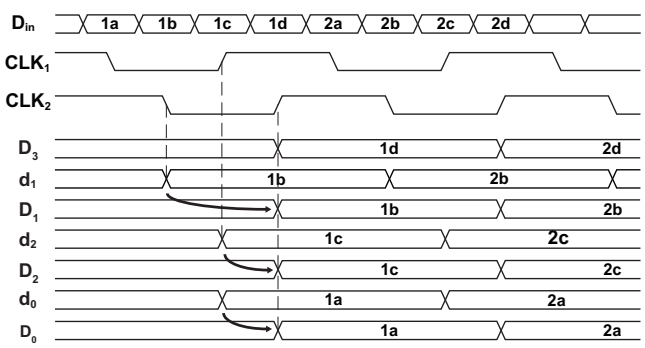

Fig. 5. DEMUX timing chart.

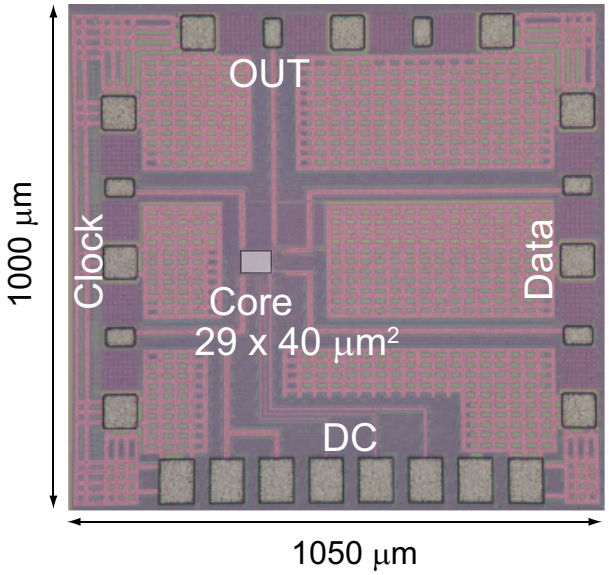

Fig. 6. Chip micrograph of 1:4 DEMUX.

Error-free 25 Gb/s operation was observed at a power supply voltage of 1.05 V. The input was $2^7 - 1$ PRBS. The power dissipation of the DEMUX core (DEMUX + divider + clock buffer) was 8.9 mW. The power dissipation including the output buffer was 20.2 mW. Measurement was also made with a lower power supply voltage of 0.9 V. The maximum data rate was 15 Gb/s. The power dissipation of DEMUX core was 4.8 mW, and the power dissipation including the output buffer was 13.5 mW.

Fig. 7 shows an output eye diagram when the input was 10 Gb/s $2^{31} - 1$ PRBS. The data rate at the output, therefore, is 2.5 Gb/s. Fig. 8 shows an output eye diagram when the input was 25 Gb/s $2^7 - 1$ PRBS. The eye diagrams were observed by using a sampling oscilloscope. The eye opening was large when the input was 10 Gb/s. The phase margin was 874 mUI (peak-to-peak), and the threshold margin was 317 mV (peak-to-peak). In contrast, when the input was 25 Gb/s, the phase margin was 345 mUI (peak-to-peak), and the threshold margin was 146 mV (peak-to-peak).

Table. I shows performance of high-speed CMOS DEMUXes [5], [6], [11]–[13].

Since DEMUX outputs are usually connected to other circuit blocks on the same chip, we think the power consumption without the output buffer is a more important metric than that with the output buffer. However, our power consumption value with the output buffer is also quite low.

Power efficiency of DEMUXes running at different data rates could be compared by looking at power per data rate mW/Gb/s [14]. Our DEMUX showed a value of 0.36 mW/Gb/s. The DEMUX in [5] showed 0.48 mW/Gb/s.

With regard to the circuit core area, ours is very small. The area of out DEMUX is less than half of [5] and [13].

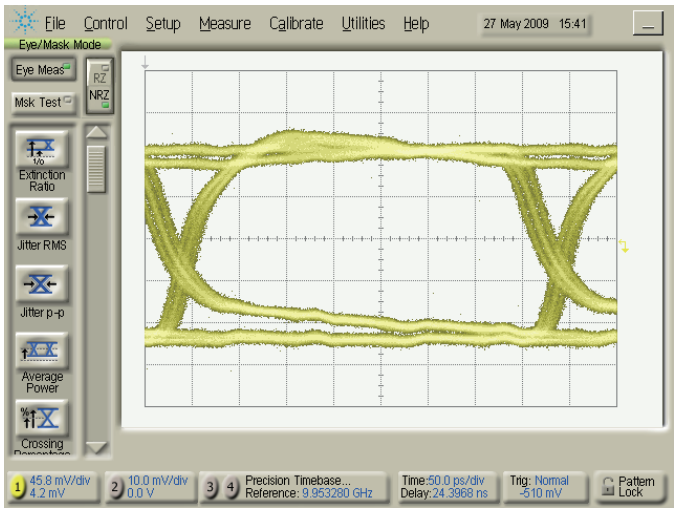

Fig. 7. Measured output eye diagram at 2.5 Gb/s (10 Gb/s input).

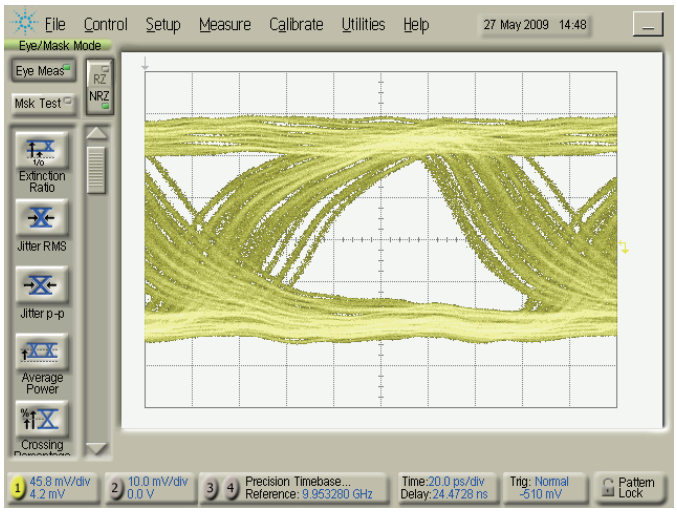

Fig. 8. Measured output eye diagram at 6.25 Gb/s output (25 Gb/s input).

V. Conclusion

A 8.9 mW 25 Gb/s 1:4 DEMUX was implemented in a 90nm CMOS process. When the power supply voltage was reduced to 0.9 V, it operated at 15 Gb/s and the power dissipation was 4.8 mW. The DEMUX core circuit area is $29 \times 40\ \mu\mathrm{m}^2$. Using the differential pseudo-NMOS logic style and a multi-phase clock architecture, high speed, low power, and small footprint were achieved. Considering these advantages and the near-rail-to-rail logic swing, this circuit could be suitable for chip-to-chip communication within a package.

Acknowledgments

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TABLE I
PERFORMANCE OF HIGH-SPEED CMOS DEMUXES

Reference	[11]	[12]	[13]	[6]	[5]	This work	
DEMUX	1:8	1:4	1:2	1:4	1:4	1:4	
Circuit type	Feedback MOS CML	Coupled latch CML	CML	Current-sourceless CML	Differential pseudo-NMOS	Differential pseudo-NMOS	
Load	PMOS triode	R	R	R+L	PMOS triode	PMOS triode	
Data rate /Gb/s	10	19	40	40	20	25	15
Power consumption /mW (with output buffer)	48	(210)	(108)	(62)	9.5	8.9 (20.2)	4.8 (13.5)
Power supply voltage /V	2.0	1.2	1.5	1.2	1.2	1.05	0.9
Core circuit area /μm^2	300×420	280×410	60×70	1400×1800	40×70	29×40	
CMOS technology	0.18 μm	0.13 μm	0.12 μm	90 nm	90 nm	90 nm	

REFERENCES

[1] D. H. Kim, S. Mukhopadhyay, and S. K. Lim, "TSV-aware interconnect length and power prediction for 3D stacked ICs," *Proc. International Interconnect Technology Conf.*, pp. 26–28, 2009.

[2] M. Anis, M. Allam, and M. Elmasry, "Impact of technology scaling on CMOS logic styles," *IEEE Trans. Circuits Syst. II*, vol. 49, no. 8, pp. 577–588, Aug. 2002.

[3] M. Yamashina and H. Yamada, "An MOS current mode logic (MCML) circuit for low-power sub-GHz processors," *IEICE Trans. Electron.*, vol. E75-C, no. 10, pp. 1181–1187, Oct. 1992.

[4] Y. Liu, J. Quan, H. Yang, and H. Wang, "MOS current mode logic circuits: design consideration in high-speed low-power applications and its future trend, a tutorial," *International J. High Speed Electronics and Systems*, vol. 15, no. 3, pp. 599–614, Sep. 2005.

[5] A. Mineyama, T. Suzuki, H. Ito, S. Amakawa, N. Ishihara, and K. Masu, "A 20Gb/s 1:4 DEMUX with near-rail-to-rail logic swing in 90nm CMOS process" *IEEE International Workshop Series on Signal Integrity and High-Speed Interconnects*, pp. 119–122, Feb. 2009.

[6] K. Kanda, D. Yamazaki, T. Yamamoto, M. Horinaka, J. Ogawa, H. Tamura, and H. Onodera, "40Gb/s 4:1 MUX/1:4 DEMUX in 90nm standard CMOS," *ISSCC Dig. Tech. Papers*, pp. 152–153, Feb. 2005.

[7] K. Kanda, D. Yamazaki, T. Yamamoto, M. Horinaka, J. Ogawa, H. Tamura, and H. Onodera, "40Gb/s 4:1 MUX/1:4 DEMUX in 90nm standard CMOS technology," *IEICE Tech. Rep.*, VLD2005-55, pp. 7–14, 2005 (in Japanese).

[8] J. P. Uyemura, *CMOS Logic Circuit Design*, Kluwer Academic Publishers, 2001.

[9] W. J. Dally and J. W. Poulton, *Digital Systems Engineering*, Cambridge University Press, 1998.

[10] H.-D.Wohlmuth, D.Kehrer, "A high sensitivity static 2:1 frequency divider up to 27GHz in 120nm CMOS," *European Solid-State Circuits Conference*, pp. 823–826, Sep. 2002.

[11] A. Tanabe, M. Umetani, I. Fujiwara, T. Ogura, K. Kataoka, M. Okihara, H. Sakuraba, T. Endoh, and F. Masuoka, "A 10Gb/s demultiplexer IC in 0.18μm CMOS using current mode logic with tolerance to the threshold voltage fluctuation," *ISSCC Dig. Tech. Papers*, pp. 62–63, Feb. 2000.

[12] B.-G. Kim, L.-S. Kim, S. Byun, and H.-K. Yu, "A 20Gb/s 1:4 DEMUX without inductors in 0.13μm CMOS," *ISSCC Dig. Tech. Papers*, pp. 528–529, Feb. 2006.

[13] D. Kehrer, H.-D. Wohlmuth, H. Knapp, M. Wurzer, and A. L. Scholtz, "40-Gb/s 2:1 multiplexer and 1:2 demultiplexer in 120-nm standard CMOS," *IEEE J. Solid-State Circuits*, pp. 344–345, Feb. 2003.

[14] S. Henzler and S. Koeppe, "Design and application of power optimized high-speed CMOS frequency dividers," *IEEE Trans. VLSI Syst.*, vol. 16, no. 11, pp. 1513–1520, Nov. 2008.