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Proposal, Logical Analysis, and Circuit Design of D, T, SR Fuzzy Flip-Flops and Fuzzy Memory Elements

Shin-ichi Yoshida

supervised by

Professor Kaoru Hirota

Doctoral Thesis

Tokyo Institute of Technology

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D, T, SR ファジィフリップフロップと ファジィメモリ基本素子の提案・論理解析及び回路設計

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Abstract

This thesis proposes D, T, SR fuzzy flip-flops and two types of fuzzy memory elements in order to give a foundation of fuzzy temporal hardware system—fuzzy sequential circuits.

First, D, T, and SR fuzzy flip-flops are defined as basic elements of a fuzzy memory module. Their characteristics are shown under four operation systems: max-min logical $(1-\cdot, \wedge, \vee)$, algebraic $(1-\cdot, \cdot, \dot{+})$, bounded $(1-\cdot, \odot, \oplus)$, and drastic $(1-\cdot, \barwedge, \barvee)$ operation systems. And then the inequalities between maxterm-expressed and minterm-expressed T fuzzy flip-flops, and between set-type and reset-type SR fuzzy flip-flops are analytically shown. The circuit areas of D, T, and SR fuzzy flip-flops decrease 2/3 to 1/2 of JK's, and delay times of them decrease 2/3 of JK's.

Next, the characteristics of D, T, and SR fuzzy flip-flops are logically analyzed when the fuzzy logical operation system $(\cdot^{\textcircled{n}}, \textcircled{t}, \textcircled{s})$ is restricted to max-min logical operation system $(1-\cdot, \wedge, \vee)$. Using the theory of B-ternary logic, fuzzy logical characteristics of the D, T, and SR fuzzy flip-flops are represented in B-ternary truth table, and fuzzy logical forms of all their characteristic functions are derived. Their structures of the partially ordered sets are distributive lattices, in particular, they are boolean lattices in the case of D and T fuzzy flip-flops under two kinds of partially ordered relation.

Finally, two type of fuzzy memory elements suitable for fuzzy inference are proposed. These fuzzy memory elements are able to memorize any fuzzy logical values $[0, 1]$ and able to execute fuzzy logical operations between a input value and the current value of a memory. Their circuits are also designed and the circuit areas and the delay times of these fuzzy memory elements are compared with those of fuzzy flip-flops. From these results, max-min type fuzzy memory element uses a half of the circuit area of SR fuzzy flip-flops and its delay time is 2/3 of that of SR fuzzy flip-flops.

This thesis concludes the advantage of proposed fuzzy memory elements for the fuzzy hardware system from the above-mentioned facts.

要旨

本論文は，ファジィ順序回路構築のために必要とされているファジィメモリ基本素子に関するものであり，D，T，SRファジィフリップフロップと2種類のファジィメモリ基本素子を提案し，それらをファジィメモリ及びファジィ推論システムへ適用する際の有用性について述べており，全5章から成っている。

第1章「Introduction」では，本研究の背景として，ファジィ順序回路構成におけるファジィメモリ基本素子の重要性，既存のファジィフリップフロップの問題点，並列ファジィ処理の有用性及び既存の並列ファジィプロセッサの問題点を述べている。

第2章「D, T, and SR fuzzy flip-flops」では，D，T，SRファジィフリップフロップのそれぞれの論理式を2値最簡形式で定義し，論理・代数・限界・激烈の四ファジィ論理演算系において，それらの特性をグラフで示すとともに，異なる論理式間で成り立つ大小関係を証明している。また，FPGAをターゲットデバイスとした回路設計・シミュレーションを計算機上で行い，回路規模・遅延時間に関して既存のJKファジィフリップフロップと比較し，T，SRファジィフリップフロップは，それぞれ回路規模で2／3，1／2，遅延時間で2／3，2／3になることを示している。Dファジィフリップフロップは，ラッチのみで構成されるため，組み合わせ回路部分の面積は0，遅延時間はラッチと配線のみ（2.8ns）となっている。このことから，ファジィメモリ基本素子として，限定した機能のみを用いる場合，汎用的なJKファジィフリップフロップよりも提案したファジィフリップフロップを用いることが，回路規模・動作速度の点で優れていると結論づけている。

第3章「Logical analysis using max-min operation system」では，Max-Min論理演算系における，D，T，SRファジィフリップフロップの論理的特性の詳細を示している。Max-Min論理においてはファジィ論理とB3値論理が等価であることを用いて，D，T，SRファジィフリップフロップの3値真理値表を示し，2値の特性のMax-Min論理への拡張として許される特性は，それぞれ4，1，136種類しかないことを示し，それらの特性方程式をすべて導出している。SRファジィフリップフロップに関してはセット優先型及びリセット優先型の双方について求めている。また，ファジィ論理値及びあいまいさの2種の半順序関係において，それらの特性方程式間でブール束や分配束を成すことを

示し，それにより，異なる特性のファジィフリップフロップを組み合わせても，またファジィフリップフロップになることを示している。

第4章「Fuzzy memory elements」では，ファジィフリップフロップと独立して，Max-Min型，限界型の2種類のファジィメモリ基本素子を提案している。ファジィフリップフロップの特性やファジィ推論で多用される機能から，ファジィ情報処理で重要な機能をメモリ素子に付加し，その状態遷移を定義している。それらをＦＰＧＡをターゲットとして回路設計を行い，回路規模・遅延時間の観点から，Ｄ，Ｔ，ＳＲ，ＪＫファジィフリップフロップと比較しており，特にMax-Min型は，メモリ基本素子として用いることのできるＳＲファジィフリップフロップよりも，回路規模で１／２，遅延時間で１／２になることを示している。また，ＪＫファジィフリップフロップによるファジィレジスタ，Ｔファジィフリップフロップによるファジィ時制推論回路，及び並列汎用ファジィプロセッサＫＡＦＡと比較し，同じ要素数のファジィ集合を記憶するための回路面積を，それぞれの18%，27%，3.4% に減少できることを示している。

第5章「Conclusions」では，本論文の成果をまとめ，それが将来のファジィ順序回路構築の基礎になっていること，また大規模並列ファジィ情報処理回路の要素としても有用なことを述べており，将来的なハードウェアファジィシステムの記憶部に関する基礎を構築したと述べている。

以上，本論文は，ファジィメモリの基本回路として，Ｄ，Ｔ，ＳＲファジィフリップフロップと2種のファジィメモリ基本素子を提案し，回路設計・シミュレーションを通して，回路規模・動作速度において既存の回路では不可能であった実用性の見通しをつけたものである.

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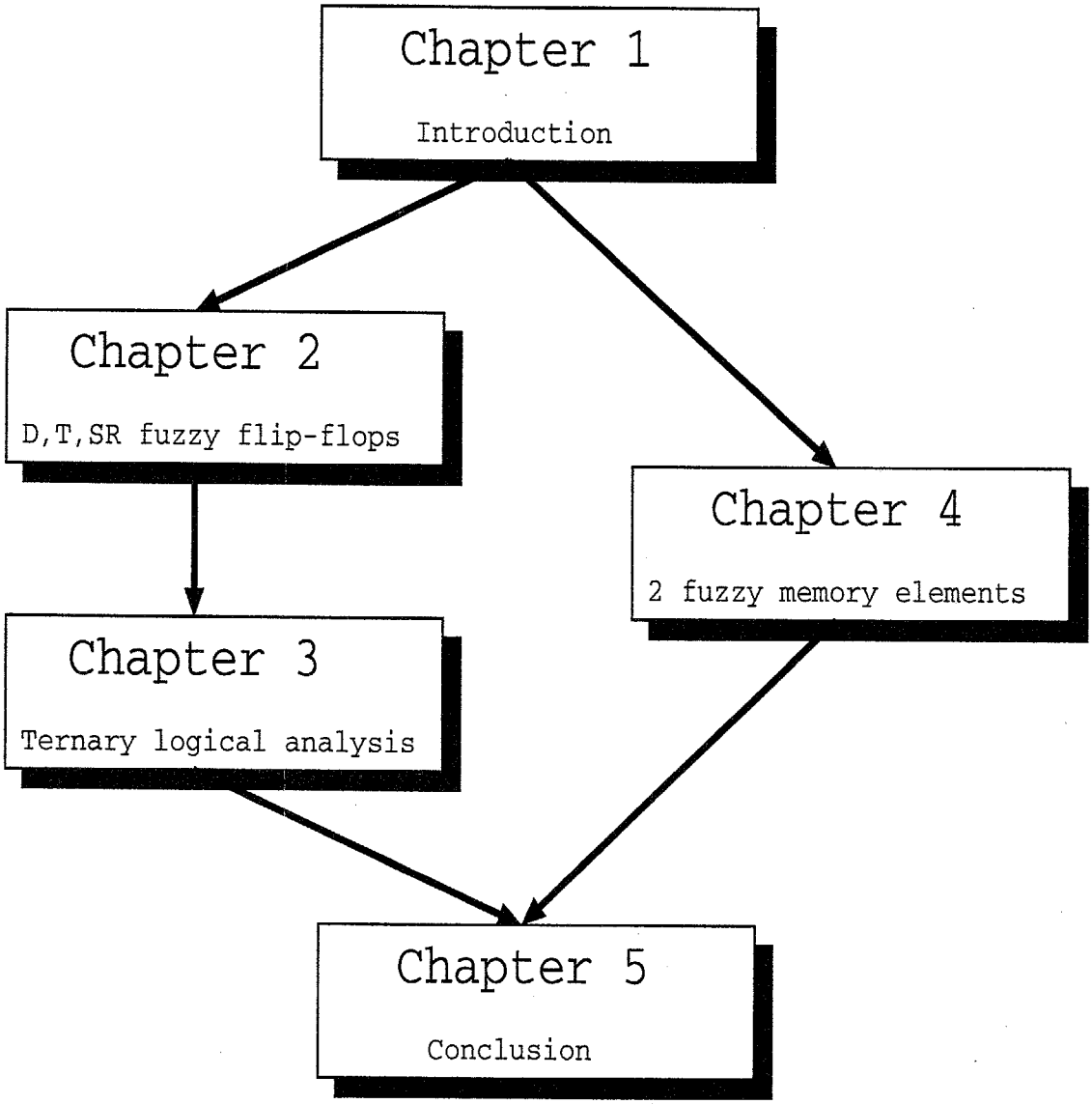
Chapter Organization



Chapter 1

Introduction

1.1 Background

Since 1980's, many electronic circuits that deal with fuzzy logical processing have been proposed. There are 2 streams of the research of fuzzy hardwares. One is fuzzy inference processors. The first fuzzy inference processor was proposed by Togai and Watanabe in 1986[29]. It is implemented as 4 bit parallel digital circuit using CMOS logic, and is able to do the Mamdani inference with 16 rules. Since the fuzzy inference is one of the most important applications of fuzzy logic, the research of fuzzy inference processor become a main stream of the research of fuzzy hardwares. Another stream of the fuzzy hardware research is concerned with analog fuzzy logic circuits. Since the fuzzy logic is a continuous multiple-valued logic, it can be regarded as an analog logic. Yamakawa et al. have proposed the fundamental analog fuzzy logic circuits[31][32][33][34]. They have implemented primitive fuzzy operations, i.e., fuzzy negation, maximum and minimum operations, and other t-norms and s-norms using current-mode analog circuits. In 1990s, more complicated analog mode fuzzy processors have been proposed, e.g., a fuzzy membership memory and a fuzzy inference processor[35][36][37].

All these fuzzy hardwares and processors are combinatorial circuits, whose output only depends on their input of the current time, while the past data or the contexts of circuits' inner states are ignored. This means that these conventional fuzzy circuits cannot realize

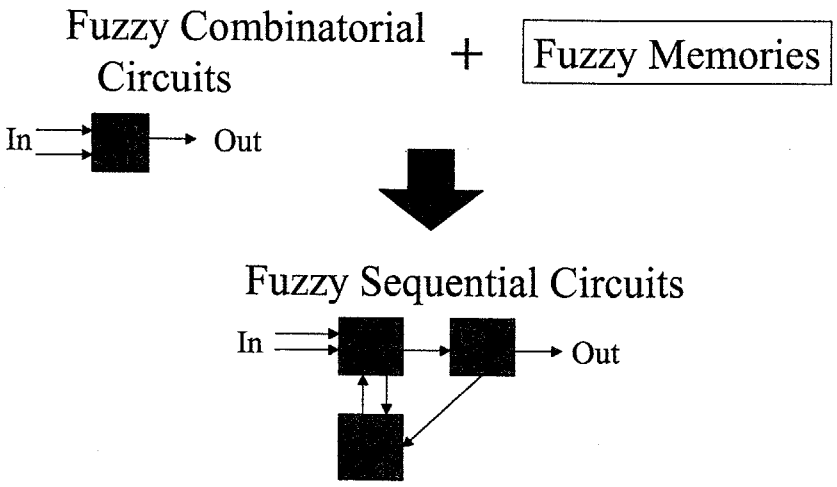


Figure 1: A fuzzy combinatorial and sequential circuits

the temporal functions like a memory (Figure 1).

For these problems, the concept of fuzzy flip-flop, which is a fundamental circuit of fuzzy memory element, was proposed in 1989[10] and implemented with analog transistor and TTL digital circuit[11]. Their theoretical consideration from a viewpoint of max-min fuzzy logic has been studied[21], and some experimental applications of JK fuzzy flip-flop have been proposed[4][6][12][14][30]. However, almost all the JK fuzzy flip-flops have been studied under max-min logical operation system $(1-\cdot, \wedge, \vee)$. Furthermore, JK flip-flop, which is widely used for general purpose in binary logic, requires large circuit resources when generalized from binary logic $\{0,1\}$ to multiple-valued fuzzy logic $[0,1]$.

A fuzzy flip-flop cannot only memorize a fuzzy logical value, but is also able to perform some fuzzy logical operations—e.g. t-norms and s-norms. This shows that a fuzzy flip-flop can be considered as a small, simple fuzzy processor with a memory—i.e. a fuzzy logic in memory. In fact, Ozawa[11] and other researches of JK fuzzy flip-flops have treated several fuzzy logical operations between fuzzy sets and fuzzy inferences. However, these

researches were intended to search effective applications of fuzzy flip-flops, and did not be discussed from a viewpoint of cost and performance.

Most of the conventional fuzzy processors aim at the application of fuzzy logic control, and they are designed for fuzzy inference processing. Recently, the application area of fuzzy information processing has spread widely to, e.g., fuzzy data (knowledge) base, fuzzy information retrieval, and fuzzy image processing. In these applications, not only fuzzy inference but also other types of fuzzy information processing—e.g., fuzzy data matching, modifying membership functions—are required.

Previous works for these purposes have been realized in the form of software on conventional (binary) computers. But fuzzy set operations treat large data (many elements of fuzzy membership functions), and the total system performance is often low. Fuzzy set operations are essentially performed concurrently and parallelly. For these applications, general-purpose (not only for a fuzzy inference) fuzzy processors have been required. Li et al. have proposed the high performance general fuzzy processor KAFA(KAist Fuzzy Accelerator) using a FPGA device. KAFA adopts the SIMD parallel architecture, but each processing element has the potential of a small computer, and their circuits become complicated and large. Therefore, it is difficult to realize the system that treats the large membership memories using KAFA.

From this reason, the parallel architecture using smaller processing elements (fine grain) than KAFA is required (Figure 2).

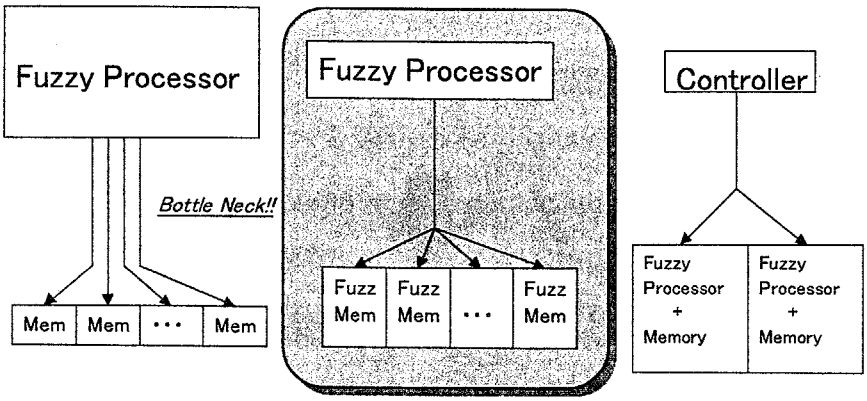


Figure 2: Parallel architecture of fuzzy hardwares

1.2 Purpose

In this dissertation, D, T, SR fuzzy flip-flops are proposed for the purpose of giving a foundation to realize fuzzy temporal hardware systems, namely fuzzy sequential circuits.

First, the characteristics of fuzzy flip-flops are shown under four typical fuzzy operation systems, in particular, they are logically analyzed in detail under max-min fuzzy logical operation systems $(1-\cdot, \wedge, \vee)$. These analysis of the characteristics is expected to support the future construction of the design methodology of fuzzy sequential circuits and fuzzy temporal systems.

In addition to fuzzy flip-flops, for the application of general fuzzy information processing, 2 types of fuzzy memory elements are also proposed. These can be used for the future fuzzy temporal applications as well as fuzzy flip-flops, furthermore they can also be used for conventional fuzzy applications existing in the real world. These can be considered to

belong to fine grain SIMD parallel fuzzy processors. Their circuit performance is shown to be higher than the conventional general fuzzy processors and fuzzy flip-flops when they are used for membership memories of fuzzy sets and for simple fuzzy set processors between the fuzzy sets. And for the purpose proposed in [11], [16] etc., it is more reasonable to use fuzzy memory elements proposed in this dissertation.

1.3 Overview

In Chapter 2, D, T, and SR fuzzy flip-flops are proposed as the fuzzy memory elements in order to treat the problems of the JK fuzzy flip-flop. Their logical characteristics are clarified in four—max-min $(1-\cdot, \wedge, \vee)$, algebraic $(1-\cdot, \cdot, \dot{+})$, bounded $(1-\cdot, \odot, \oplus)$, and drastic $(1-\cdot, \wedge, \forall)$—fuzzy logical operation systems. Their circuits for the four operation systems are implemented using VHDL and circuit simulator/synthesizer on a workstation, and are compared with each other in terms of the circuit area and the delay times. The results show the circuit areas and the delay times of the proposed fuzzy flip-flops are improved to $1/2 \sim 1/3$ compared with those of the conventional JK fuzzy flip-flop.

In Chapter 3, from the viewpoint of fuzzy state machine, the details of the logical property of the D, T, and SR fuzzy flip-flops are analyzed using max-min logical operation system $(1-\cdot, \wedge, \vee)$. All their characteristics that are possibly realized in the fuzzy logic $(1-\cdot, \wedge, \vee)$ as extensions of the form in the binary logic are shown, and all logical forms that corresponds to them are derived. It is clarified that for all fuzzy flip-flops, their logical forms construct distributed lattices both under the partially order by fuzzy values and under the partially order by ambiguity. Moreover, the lattices constructed by the forms of D and T fuzzy flip-flops are boolean lattices and so are the lattices of conventional JK fuzzy flip-flop.

In Chapter 4, 2 types of fuzzy memory elements, which are max-min type and bounded type, are proposed for the general-purpose parallel fuzzy processors and fuzzy flip-flops. These fuzzy memory elements are proposed from the aspects of functions required for

fuzzy memory elements and state transitions to realize the functions. Proposed fuzzy memory elements can input and output an arbitrary fuzzy value at an arbitrary point of time and hold their memory values for an arbitrary length of time. In addition to these functions required for memory elements, fuzzy memory elements can execute the fuzzy logical operations between fuzzy input and fuzzy memory. Compared with the fuzzy memory using SR fuzzy flip-flops, the circuit area and the delay times of the max-min type fuzzy memory element are improved to 1/2, 2/3, respectively. Those of bounded type fuzzy memory elements equals to those of the JK fuzzy flip-flop, although it has 4 more fuzzy logical operations than the JK fuzzy flip-flop. From the viewpoint of the SIMD parallel architecture, max-min type and bounded type fuzzy memory elements are fine grain SIMD processors which can perform fuzzy logical operations. Therefore, membership memories using these memory elements can perform fuzzy set operations (e.g. maximum or minimum) between a input fuzzy set and a fuzzy set in the memory fast and easily. The number of elements of fuzzy set membership functions is more than 30 times bigger than that of KAFA for a same chip.

Chapter 2

D, T, and SR fuzzy flip-flops

2.1 Introduction

Concept of fuzzy flip-flop, which is a fundamental circuit of fuzzy memory element, was proposed in 1989[10] and implemented with analog transistor and TTL digital circuit[11]. Although their theoretical consideration from a viewpoint of max-min fuzzy logic has been studied[21], they dealt with only JK flip-flop and mainly used under max-min logical operation system $(1 - \cdot, \wedge, \vee)$. Furthermore, JK flip-flop, which is widely used in binary logic for general purpose, requires large circuit resources when generalized from binary logic $\{0, 1\}$ to multiple-valued fuzzy logic $[0, 1]$.

This chapter presents D, T, and SR fuzzy flip-flops, that are less functional but simpler and faster compared with JK fuzzy flip-flop, with their characteristics. Their FPGA circuits are also designed on Synopsys Design Compiler and its circuit areas and delay times are compared with those of conventional JK fuzzy flip-flop.

In Section 2.2, a fundamental definition of D, T, and SR fuzzy flip-flops are given, and Section 2.3 shows a result of circuit implementation to FPGA device. Finally, their performances are compared with each other in Section 2.4.

2.2 Definition of D, T, and SR fuzzy flip-flops

This section defines characteristic equations of D, T, and SR fuzzy flip-flops as fuzzification of their simplest logical forms in binary logic.

2.2.1 D fuzzy flip-flop

Characteristic function of D fuzzy flip-flop is

$$Q(t+1) = D(t). \tag{1}$$

Eq.(1) is a natural extension of the irredundant form of binary D flip-flop.

In the case of D fuzzy flip-flop, the output $Q(t+1)$ is equal to the input $D(t) \in [0,1]$. It is the one clock delay element.

Figure 3 shows the characteristic of Eq.(1). In the Eq.(1), there is no logical operation, and the characteristics of all fuzzy logical operation systems are the same.

2.2.2 T fuzzy flip-flop

Characteristic functions of T fuzzy flip-flop are shown in Eq.(2) and Eq.(3), that are the extension of minterm expression and maxterm expression in binary logic, respectively.

$$Q(t+1)_{\mathrm{MIN}} = (T \textcircled{t} Q^{\textcircled{n}}) \textcircled{s} (T^{\textcircled{n}} \textcircled{t} Q) \tag{2}$$

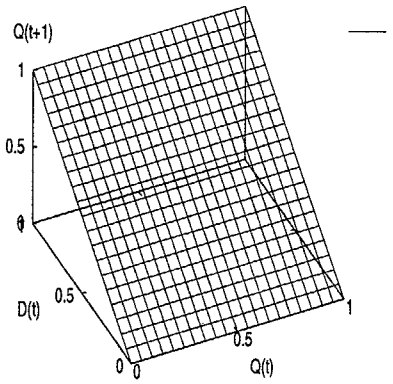


Figure 3: Characteristic of D fuzzy flip-flop

$$Q(t+1)_{\mathrm{MAX}} = (T \textcircled{s} Q) \textcircled{t} (T^{\textcircled{n}} \textcircled{s} Q^{\textcircled{n}}) \tag{3}$$

In the case of T flip-flop, minterm expression and maxterm expression are irredundant forms and they are not unique. Although Eq. (2) and Eq. (3) are equivalent in binary logic, they are not in fuzzy logic. Now the differences between them are shown in the case of max-min, algebraic, bounded, and drastic fuzzy logical operation systems.

Theorem 1 When the fuzzy logical operation system $(\cdot^{\textcircled{n}}, \textcircled{t}, \textcircled{s})$ is max-min $(1 - \cdot, \wedge, \vee)$, algebraic $(1 - \cdot, \cdot, \dot{+})$, bounded $(1 - \cdot, \odot, \oplus)$, or drastic $(1 - \cdot, \barwedge, \barvee)$, then the inequality

$$Q_{\mathrm{MIN}}(t+1) \leq Q_{\mathrm{MAX}}(t+1), \tag{4}$$

holds. The equality always holds if and only if $(\cdot^{\textcircled{n}}, \textcircled{t}, \textcircled{s}) = (1 - \cdot, \wedge, \vee)$.

Proof

(i) Case of $(1 - \cdot, \wedge, \vee)$. For a simplified notation, time variable t will be omitted later.

$$\begin{aligned} Q^{\log}_{\mathrm{MAX}}(t+1) &= (T(t) \vee Q(t)) \wedge (T^{\textcircled{n}}(t) \vee Q^{\textcircled{n}}(t)) \\ &= (T \wedge Q^{\textcircled{n}}) \vee (T^{\textcircled{n}} \wedge Q) \\ &\quad \vee (T \wedge T^{\textcircled{n}}) \vee (Q \wedge Q^{\textcircled{n}}) \end{aligned} \tag{5}$$

Since the value of the third and the fourth terms in the right hand side are at most $1/2$, minimum operations between them and the other terms whose values are greater than or

equal to 1/2 keeps the same value (Kleene's equality).

$$\begin{aligned}(5) &= (T \wedge Q^{\textcircled{n}}) \vee (T^{\textcircled{n}} \wedge Q) \\ &\quad \vee\{(T \wedge T^{\textcircled{n}}) \wedge (Q \vee Q^{\textcircled{n}})\} \\ &\quad \vee\{(Q \wedge Q^{\textcircled{n}}) \wedge (T \vee T^{\textcircled{n}})\} \\ &= (T \wedge Q^{\textcircled{n}}) \vee (T^{\textcircled{n}} \wedge Q) \\ &\quad \vee(T \wedge T^{\textcircled{n}} \wedge Q) \vee (T \wedge T^{\textcircled{n}} \wedge Q^{\textcircled{n}}) \\ &\quad \vee(T \wedge Q \wedge Q^{\textcircled{n}}) \vee (T^{\textcircled{n}} \wedge Q \wedge Q^{\textcircled{n}}) \\ &= (T(t) \wedge Q^{\textcircled{n}}(t)) \vee (T^{\textcircled{n}}(t) \wedge Q(t)) \\ &= Q^{\log}_{\mathrm{MIN}}(t+1) \end{aligned} \tag{6}$$

(ii) Case of $(1-\cdot, \cdot, \dot{+})$.

$$\begin{aligned} Q^{\mathrm{alg}}_{\mathrm{MIN}}(t+1) &= (T(t) \cdot Q^{\textcircled{n}}(t)) \dot{+} (T^{\textcircled{n}}(t) \cdot Q(t)) \\ &= T(1-Q) + (1-T)Q - T(1-T)Q(1-Q) \\ &\leq T(1-Q) + (1-T)Q + T(1-T)Q(1-Q) \\ &= (T + Q - TQ) \cdot (T^{\textcircled{n}} + Q^{\textcircled{n}} - T^{\textcircled{n}}Q^{\textcircled{n}}) \\ &= (T(t) \dot{+} Q(t)) \cdot (T^{\textcircled{n}}(t) \dot{+} Q^{\textcircled{n}}(t)) \\ &= Q^{\mathrm{alg}}_{\mathrm{MAX}}(t+1) \end{aligned} \tag{7}$$

(iii) Case of $(1-\cdot, \odot, \oplus)$.

$$\begin{aligned} Q^{\mathrm{bdd}}_{\mathrm{MIN}}(t+1) &= (T(t) \odot Q^{\textcircled{n}}(t)) \oplus (T^{\textcircled{n}}(t) \odot Q(t)) \\ &= \begin{cases} Q - T & (T \leq Q) \\ T - Q & (T \geq Q) \end{cases} \end{aligned} \tag{8}$$

$$\begin{aligned} Q^{\mathrm{bdd}}_{\mathrm{MAX}}(t+1) &= (T(t) \oplus Q(t)) \odot (T^{\textcircled{n}}(t) \oplus Q^{\textcircled{n}}(t)) \\ &= \begin{cases} T + Q & (T + Q \leq 1) \\ 2 - T - Q & (T + Q \geq 1) \end{cases} \end{aligned} \tag{9}$$

Since $Q^{\mathrm{bdd}}_{\mathrm{MIN}}(t+1)$ is less than or equal to $Q^{\mathrm{bdd}}_{\mathrm{MAX}}(t+1)$ in all cases,

$$Q^{\mathrm{bdd}}_{\mathrm{MIN}}(t+1) \leq Q^{\mathrm{bdd}}_{\mathrm{MAX}}(t+1). \tag{10}$$

(iv) Case of $(1-\cdot, \wedge, \vee)$.

$$Q_{\mathrm{MIN}}^{\mathrm{dra}}(t+1) = (T(t) \wedge Q^{\textcircled{n}}(t)) \vee (T^{\textcircled{n}}(t) \wedge Q(t))$$
$$= \begin{cases} Q & (T=0) \\ T & (Q=0) \\ 1-Q & (T=1) \\ 1-T & (Q=1) \\ 0 & (0<T<1,\ 0<Q<1) \end{cases} \tag{11}$$

$$Q_{\mathrm{MAX}}^{\mathrm{dra}}(t+1) = (T(t) \vee Q(t)) \wedge (T^{\textcircled{n}}(t) \vee Q^{\textcircled{n}}(t))$$
$$= \begin{cases} Q & (T=0) \\ T & (Q=0) \\ 1-Q & (T=1) \\ 1-T & (Q=1) \\ 1 & (0<T<1,\ 0<Q<1) \end{cases} \tag{12}$$

From the above results,

$$Q_{\mathrm{MIN}}^{\mathrm{dra}}(t+1) \le Q_{\mathrm{MAX}}^{\mathrm{dra}}(t+1). \tag{13}$$

Q.E.D.

More general results, discussed below, are also obtained.

Theorem 2 If $(\cdot^{\textcircled{n}}, \textcircled{t}, \textcircled{s})$ always satisfies the following semi-distributive law

$$A \textcircled{t} (B \textcircled{s} C) \ge (A \textcircled{t} B) \textcircled{s} (A \textcircled{t} C),$$
$$A \textcircled{s} (B \textcircled{t} C) \le (A \textcircled{s} B) \textcircled{t} (A \textcircled{s} C), \tag{14}$$

then the inequality

$$Q_{\mathrm{MIN}}(t+1) \le Q_{\mathrm{MAX}}(t+1), \tag{15}$$

holds true.

Proof

$$\begin{aligned} Q_{\mathrm{MAX}}(t+1) &= (T(t)\textcircled{s}Q(t))\textcircled{t}(T^{\textcircled{n}}(t)\textcircled{s}Q^{\textcircled{n}}(t)) \\ &\geq (T\textcircled{t}Q^{\textcircled{n}})\textcircled{s}(T^{\textcircled{n}}\textcircled{t}Q) \\ &\quad \textcircled{s}(T\textcircled{t}T^{\textcircled{n}})\textcircled{s}(Q\textcircled{t}Q^{\textcircled{n}}) \\ &\geq (T\textcircled{t}Q^{\textcircled{n}})\textcircled{s}(T^{\textcircled{n}}\textcircled{t}Q) \\ &= Q_{\mathrm{MIN}}(t+1) \end{aligned} \tag{16}$$

Q.E.D.

Figure 4 shows the characteristics of the equation (2) using logical, algebraic, bounded, and drastic operation systems, respectively, while Figure 5 shows those of equation (3). These figures show the value of $Q(t+1)$ as a function of $Q(t)$ and $T(t)$.

From these figures, we can see that

$$\begin{aligned} Q^{\mathrm{dra}}_{\mathrm{MIN}}(t+1) \leq Q^{\mathrm{bdd}}_{\mathrm{MIN}}(t+1) \leq Q^{\mathrm{alg}}_{\mathrm{MIN}}(t+1) \\ \leq Q^{\mathrm{log}}_{\mathrm{MIN}}(t+1) = Q^{\mathrm{log}}_{\mathrm{MAX}}(t+1) \leq Q^{\mathrm{alg}}_{\mathrm{MAX}}(t+1) \\ \leq Q^{\mathrm{bdd}}_{\mathrm{MAX}}(t+1) \leq Q^{\mathrm{dra}}_{\mathrm{MAX}}(t+1) \end{aligned} \tag{17}$$

holds true.

2.2.3 SR fuzzy flip-flop

Binary SR flip-flop which has three functions—bit set, bit reset, and hold—is a basic element of memory modules. If the set input $S = 1$, then the next state $Q(t+1) = 1$. If the reset input $R = 1$, then the next state $Q(t+1) = 0$. If $S = R = 0$, then the next state holds the current state, i.e., $Q(t+1) = Q(t)$. Although the input $S = R = 1$ is forbidden, there exist two types of SR fuzzy flip-flop in order to construct the characteristic function of SR flip-flop. One is set-type, whose $Q(t+1) = 1$ when $S = R = 1$, and another is reset-type, whose $Q(t+1) = 0$ when $S = R = 1$.

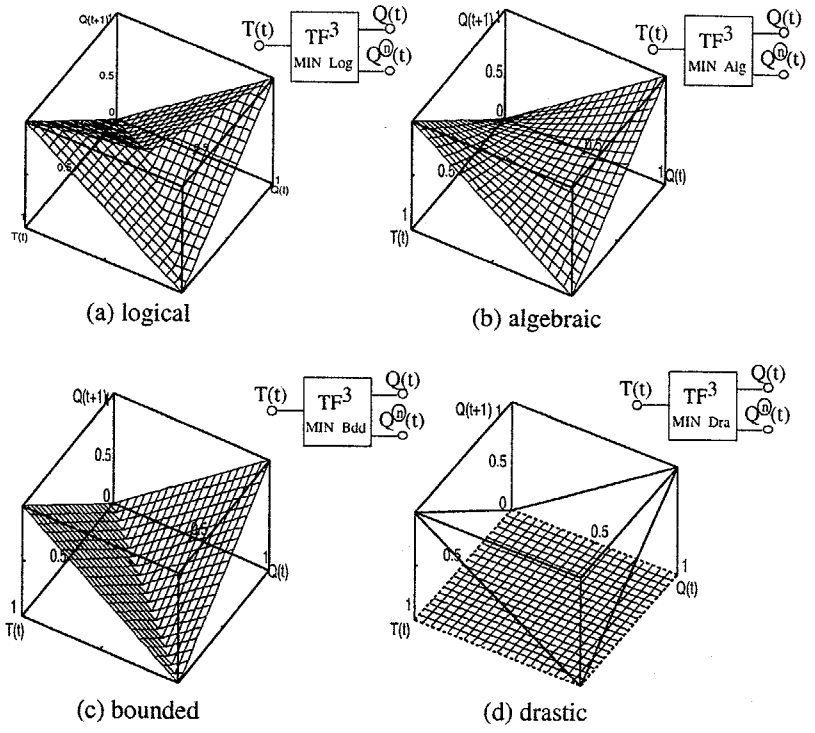


Figure 4: Characteristics of T fuzzy flip-flop (minterm)

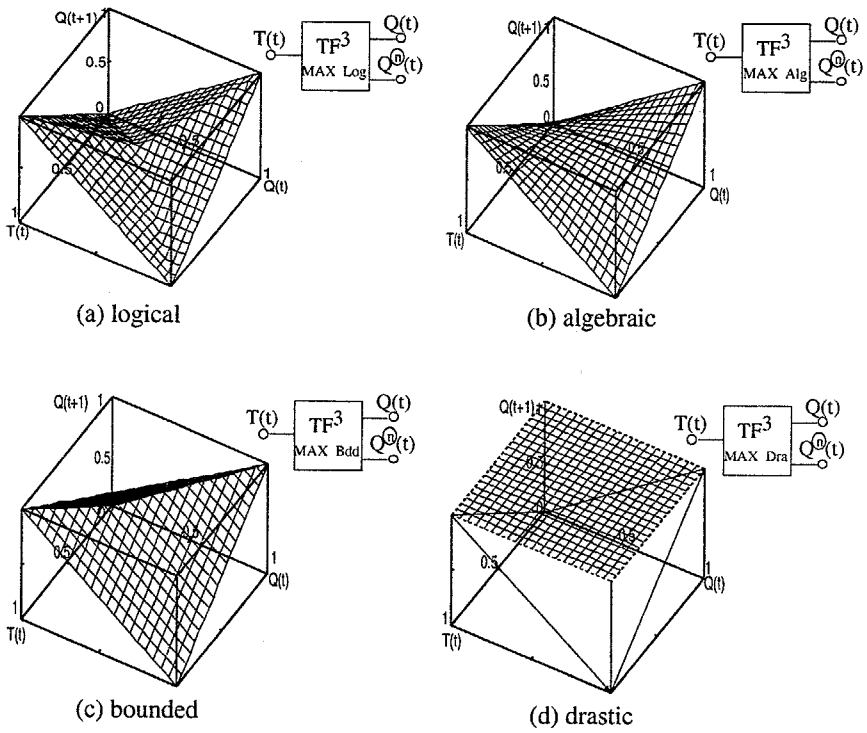


Figure 5: Characteristics of T fuzzy flip-flop (maxterm)

Eq. (18) and Eq.(19) are the characteristic functions of set-type and reset-type SR fuzzy flip-flop, respectively.

$$Q_{\mathrm{S}}(t+1) = S \textcircled{s} (R^{\textcircled{n}} \textcircled{t} Q) \tag{18}$$

$$Q_{\mathrm{R}}(t+1) = R^{\textcircled{n}} \textcircled{t} (S \textcircled{s} Q) \tag{19}$$

Now an order relation between set-type and reset-type SR fuzzy flip-flop is shown in some cases. Under max-min, algebraic, and bounded operation systems, fuzzy truth value of set-type SR fuzzy flip-flop is always greater than or equal to that of reset-type. Needless to say, such a relation stands in binary logic.

Theorem 3 If an operation system $(\cdot^{\textcircled{n}}, \textcircled{t}, \textcircled{s})$ satisfies inverse semi-distributive law

$$\begin{aligned} A \textcircled{t} (B \textcircled{s} C) &\leq (A \textcircled{t} B) \textcircled{s} (A \textcircled{t} C), \\ A \textcircled{s} (B \textcircled{t} C) &\geq (A \textcircled{s} B) \textcircled{t} (A \textcircled{s} C), \end{aligned} \tag{20}$$

then it satisfies

$$Q_{\mathrm{S}}(t+1) \geq Q_{\mathrm{R}}(t+1). \tag{21}$$

Proof

$$\begin{aligned} Q_{\mathrm{S}}(t+1) &= S(t) \textcircled{s} (R^{\textcircled{n}}(t) \textcircled{t} Q(t)) \\ &\geq (R^{\textcircled{n}} \textcircled{t} S) \textcircled{s} (R^{\textcircled{n}} \textcircled{t} Q) \\ &\geq R^{\textcircled{n}} \textcircled{t} (S \textcircled{s} Q) \\ &= Q_{\mathrm{R}}(t+1) \end{aligned} \tag{22}$$

Q.E.D.

Corollary 3 If $(\cdot^{\textcircled{n}}, \textcircled{t}, \textcircled{s})$ is logical operation system $(1 - \cdot, \wedge, \vee)$ or algebraic operation system $(1 - \cdot, \cdot, \dot{+})$, then the SR fuzzy flip-flop satisfies Eq.(21).

Theorem 4 If the operation system $(\cdot^{\textcircled{n}}, \textcircled{t}, \textcircled{s})$ is bounded operation system $(1-\cdot, \odot, \oplus)$, Eq.(21) holds true.

Proof

$$
\begin{aligned}
Q_{\mathrm{S}}(t+1) &= S(t) \oplus (R^{\textcircled{n}}(t) \odot Q(t)) \\
&= \begin{cases} S+Q-R & (0 \le Q-R \le 1-S) \quad \text{(SA)} \\ 1 & (0 \le 1-S \le Q-R) \quad \text{(SB)} \\ S & (Q-R \le 0) \quad \text{(SC)} \end{cases}
\end{aligned} \tag{23}
$$

$$
\begin{aligned}
Q_{\mathrm{R}}(t+1) &= R^{\textcircled{n}}(t) \odot (S(t) \oplus Q(t)) \\
&= \begin{cases} S+Q-R & (R \le S+Q \le 1) \quad \text{(RA)} \\ 0 & (S+Q \le R \le 1) \quad \text{(RB)} \\ 1-R & (1 \le S+Q) \quad \text{(RC)} \end{cases}
\end{aligned} \tag{24}
$$

(SB) of Eq.(23) is always greater than or equal to all cases of (RA), (RB), and (RC) of Eq.(24), and (RB) of Eq.(24) is always smaller than or equal to all cases of (SA), (SB), and (SC) of Eq.(23), and (SA)-(RA) is 0. Therefore,

$$
\begin{aligned}
\text{(SA)-(RC)} &= S+Q-R-(1-R) \\
&= S+Q-1 \\
&\ge 0 \quad (\because 1 \le S+Q)
\end{aligned} \tag{25}
$$

$$
\begin{aligned}
\text{(SC)-(RA)} &= S-(S+Q-R) \\
&= -(Q-R) \\
&\ge 0 \quad (\because Q-R \le 0)
\end{aligned} \tag{26}
$$

$$
\begin{aligned}
\text{(SC)-(RC)} &= S-(1-R) \\
&= R-(1-S) \\
&\ge 0 \quad (\because Q-R \le 0,\ 1 \le S+Q\ . \\
&\qquad \text{then } R \ge 1-S)
\end{aligned} \tag{27}
$$

Hence $Q_{\mathrm{S}}(t+1) \ge Q_{\mathrm{R}}(t+1)$ is obtained.

Q.E.D.

Next the characteristics of SR fuzzy flip-flop when the operation system is logical operation system $(1-\cdot, \wedge, \vee)$, algebraic operation system $(1-\cdot, \cdot, \dot{+})$, bounded operation system $(1-\cdot, \odot, \oplus)$, and drastic operation system $(1-\cdot, \barwedge, \barvee)$ are shown. Figure 6 shows the characteristics of set-type SR fuzzy flip-flop, and Figure 7 shows that of the reset-type under the max-min logical operation system $(1-\cdot, \wedge, \vee)$. Figure 8 and Figure 9 show the characteristics of set-type and reset-type in the algebraic operation system $(1-\cdot, \cdot, \dot{+})$, respectively. Figure 10 and Figure 11 show the characteristics of set-type and reset-type in the bounded operation system $(1-\cdot, \odot, \oplus)$, respectively. Figure 12 and Figure 13 show the characteristics of set-type and reset-type in the drastic operation system $(1-\cdot, \barwedge, \barvee)$, respectively. These figures show the value of $Q(t+1)$ when $Q(t)=0$, $Q(t)=0.5$, and $Q(t)=1$, respectively.

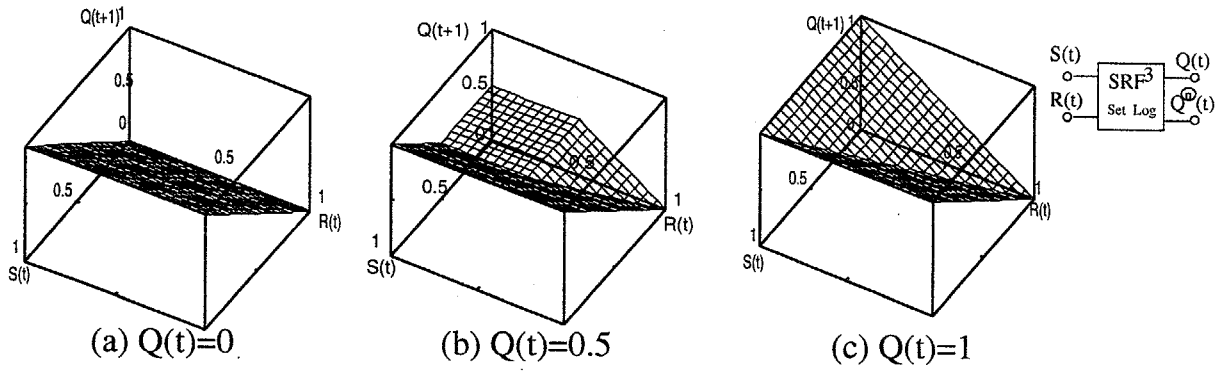


Figure 6: Characteristics of SR fuzzy flip-flop (set type, logical)

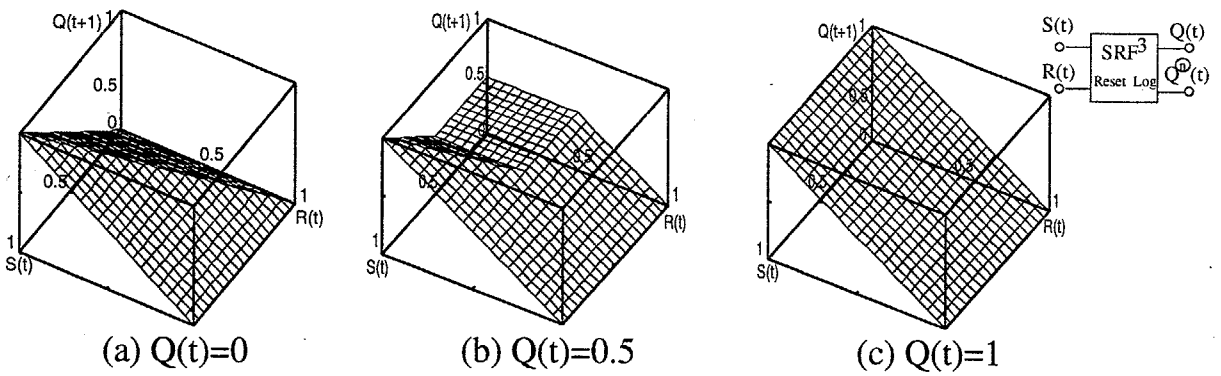
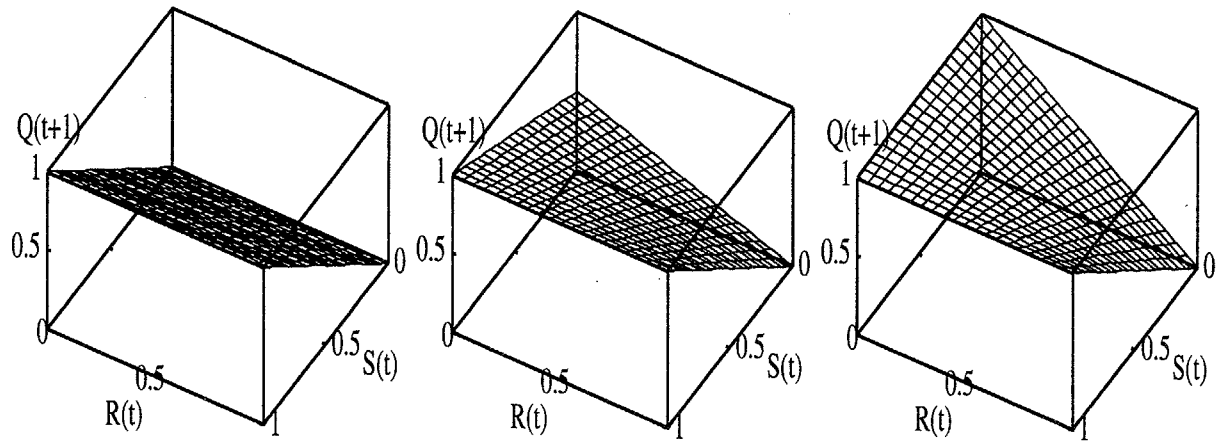
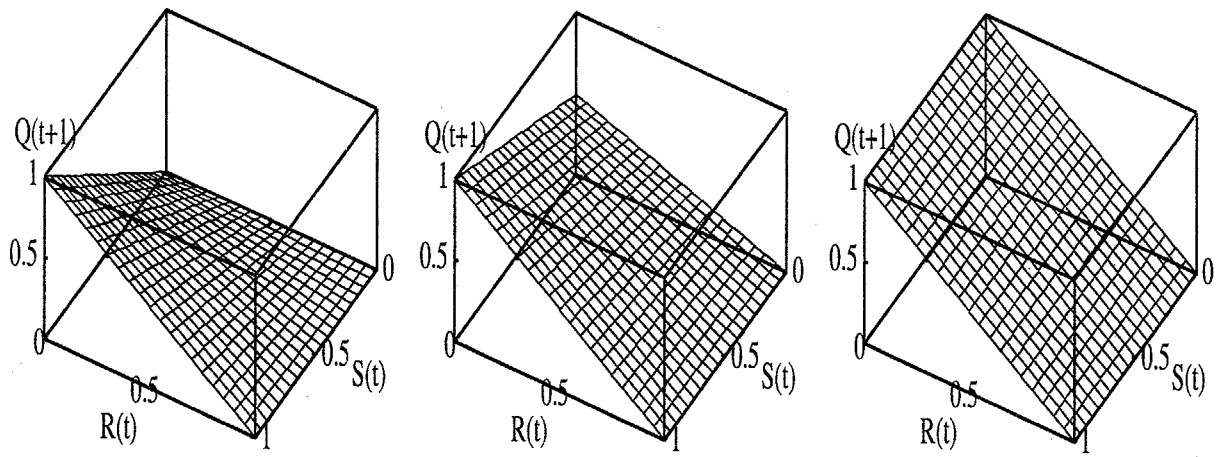


Figure 7: Characteristics of SR fuzzy flip-flop (reset type, logical)



(a) Q(t)=0 (b) Q(t)=0.5 (c) Q(t)=1

Figure 8: Characteristics of SR fuzzy flip-flop (set type, algebraic)



(a) Q(t)=0 (b) Q(t)=0.5 (c) Q(t)=1

Figure 9: Characteristics of SR fuzzy flip-flop (reset type, algebraic)

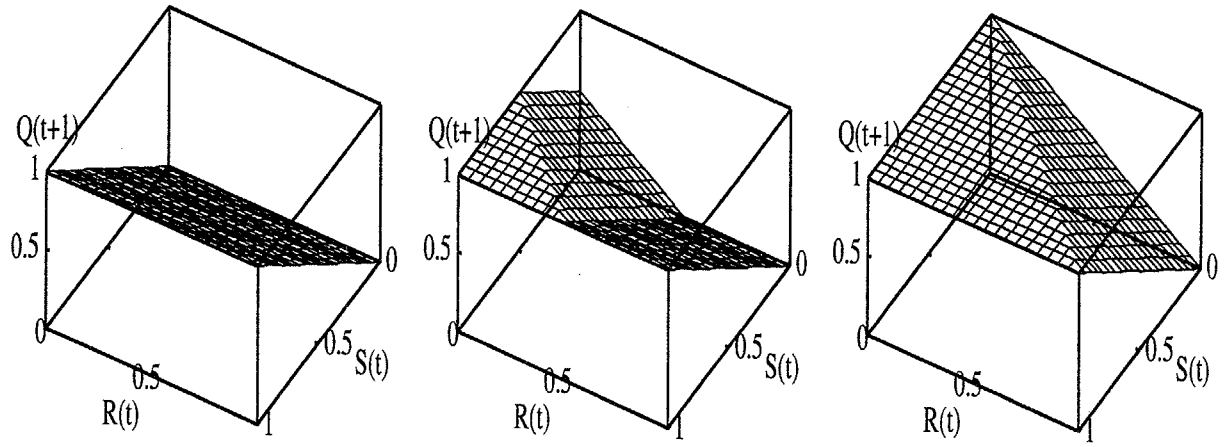


Figure 10: Characteristics of SR fuzzy flip-flop (set type, bounded)

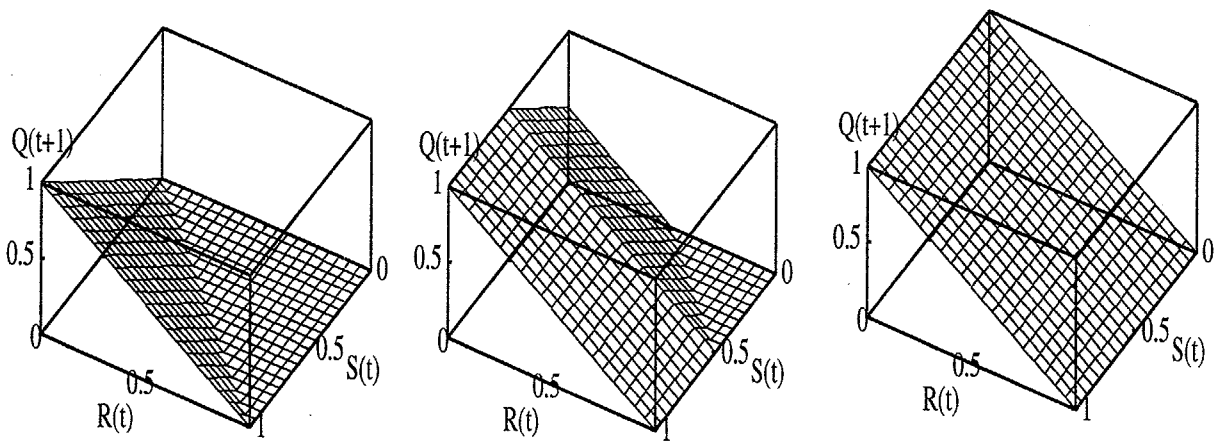
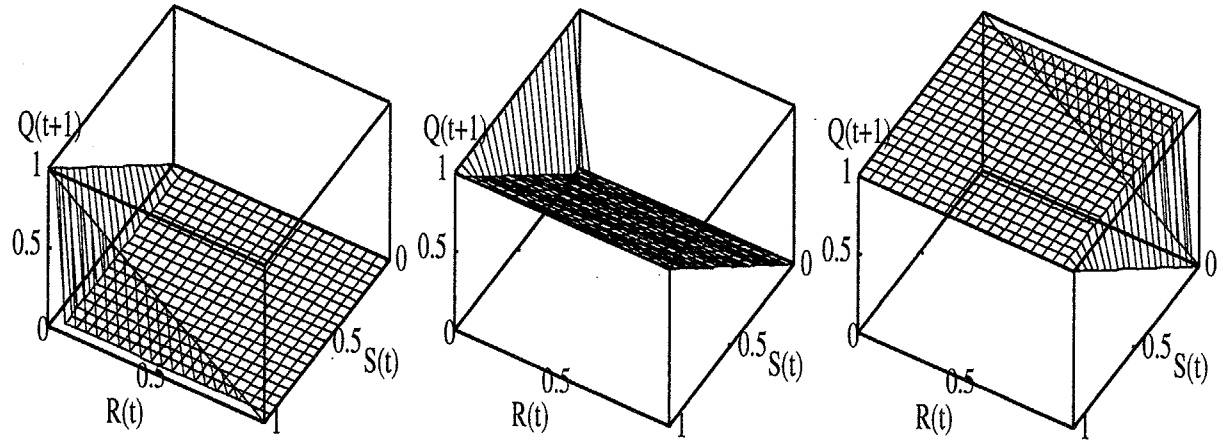
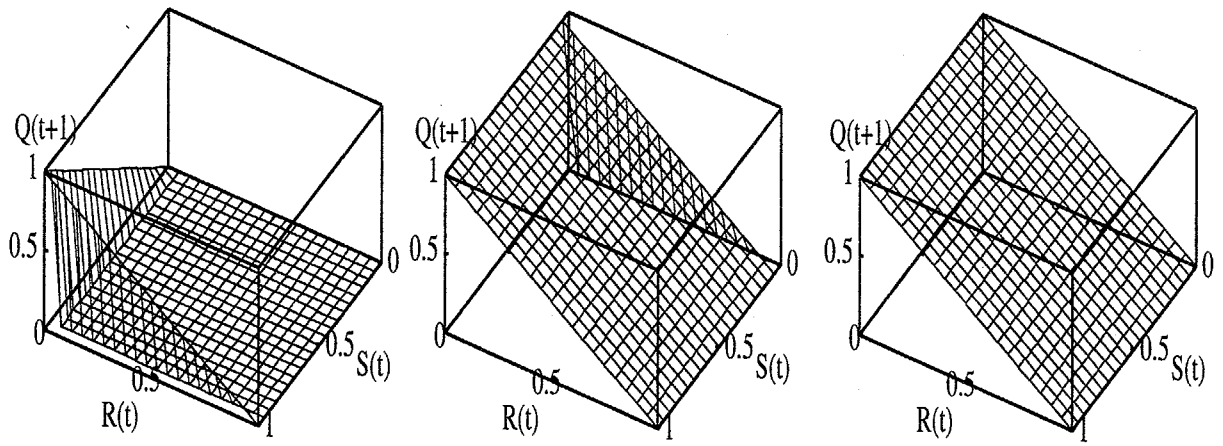


Figure 11: Characteristics of SR fuzzy flip-flop (reset type, bounded)



(a) Q(t)=0 (b) Q(t)=0.5 (c) Q(t)=1

Figure 12: Characteristics of SR fuzzy flip-flop (set type, drastic)



(a) Q(t)=0 (b) Q(t)=0.5 (c) Q(t)=1

Figure 13: Characteristics of SR fuzzy flip-flop (reset type, drast)

In the logical operation system $(1-\cdot, \wedge, \forall)$, there is no uniform inequality between set-type and reset-type, which can be shown as follows. When $S = 0.5, R = 0.1, Q(t) = 0.9$

$$\begin{aligned} Q_{\mathrm{S}}(t+1) &= S \forall ((1-R) \wedge Q(t)) && (28) \\ &= 0.5, && (29) \end{aligned}$$

$$\begin{aligned} Q_{\mathrm{R}}(t+1) &= (1-R) \wedge (S \forall Q(t)) && (30) \\ &= 0.9. && (31) \end{aligned}$$

Therefore

$$Q_{\mathrm{S}}(t+1) < Q_{\mathrm{R}}(t+1). \quad (32)$$

And when $S = 0.5, R = 0.9, Q(t) = 0.9$

$$\begin{aligned} Q_{\mathrm{S}}(t+1) &= S \forall ((1-R) \wedge Q(t)) && (33) \\ &= 0.5, && (34) \end{aligned}$$

$$\begin{aligned} Q_{\mathrm{R}}(t+1) &= (1-R) \wedge (S \forall Q(t)) && (35) \\ &= 0.1. && (36) \end{aligned}$$

Therefore

$$Q_{\mathrm{S}}(t+1) > Q_{\mathrm{R}}(t+1). \quad (37)$$

2.3 Circuit design of D, T, and SR fuzzy flip-flops using FPGA

In this section, the results of FPGA circuit design of D, T, and SR fuzzy flip-flop are shown. Four-bit parallel architecture is used for the quantization of fuzzy value in order to compare with JK fuzzy flip-flop proposed in [11]. Namely, the value of fuzzy variable 0 is assigned to "0000" $(0)_{10}$, and 1 to "1111" $(15)_{10}$. But only in algebraic logical operation

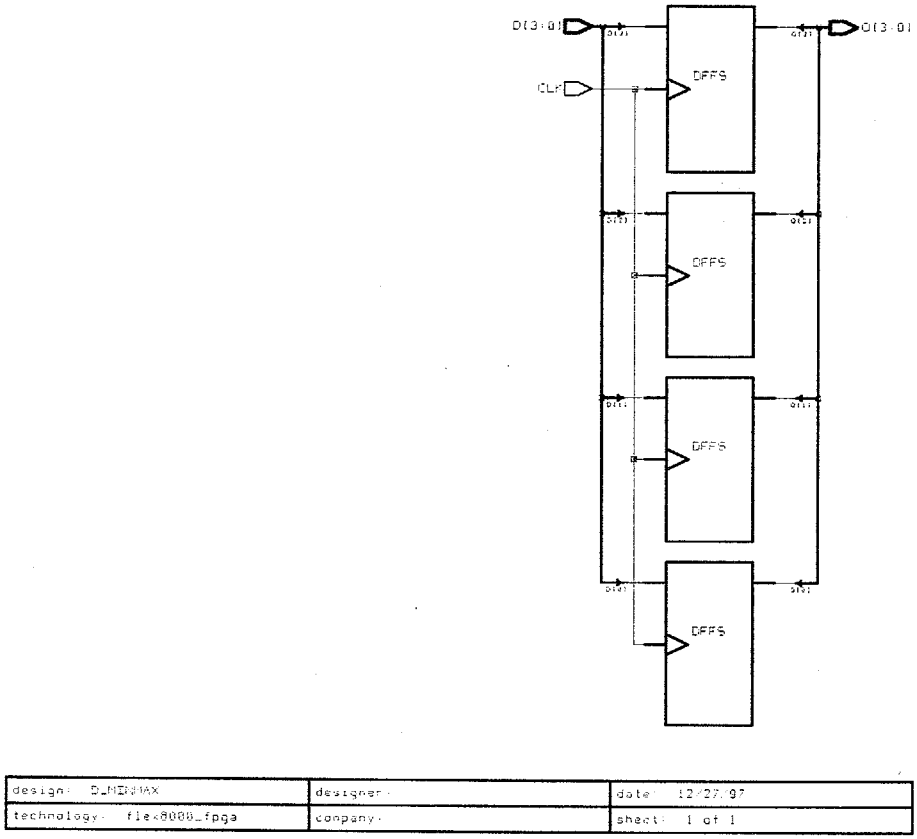


Figure 14: Circuit of D fuzzy flip-flop

system, one more bit is added and 0 is assigned to "00000" $(0)_{10}$, and 1 to "10000" $(16)_{10}$ in order to use normal adders and multipliers for convenience of circuit design.

Regarding the design of circuits, first, the behavior model is written using VHDL, and it is synthesized using Synopsys Design Compiler V1997.8. The library of target architecture is FLEX8000 which is FPGA of Altera. The computer used for the simulation is Sun SPARC Station 20, SunOS 4.1.4.

2.3.1 D fuzzy flip-flop

Figure 14 shows the circuit of D fuzzy flip-flop. It is the parallel connection of four binary D flip-flops.

Since D fuzzy flip-flop is composed of binary D flip-flops for output latches, the combinatorial part of its circuit area is 0. Delay time is 2.8ns for latches.

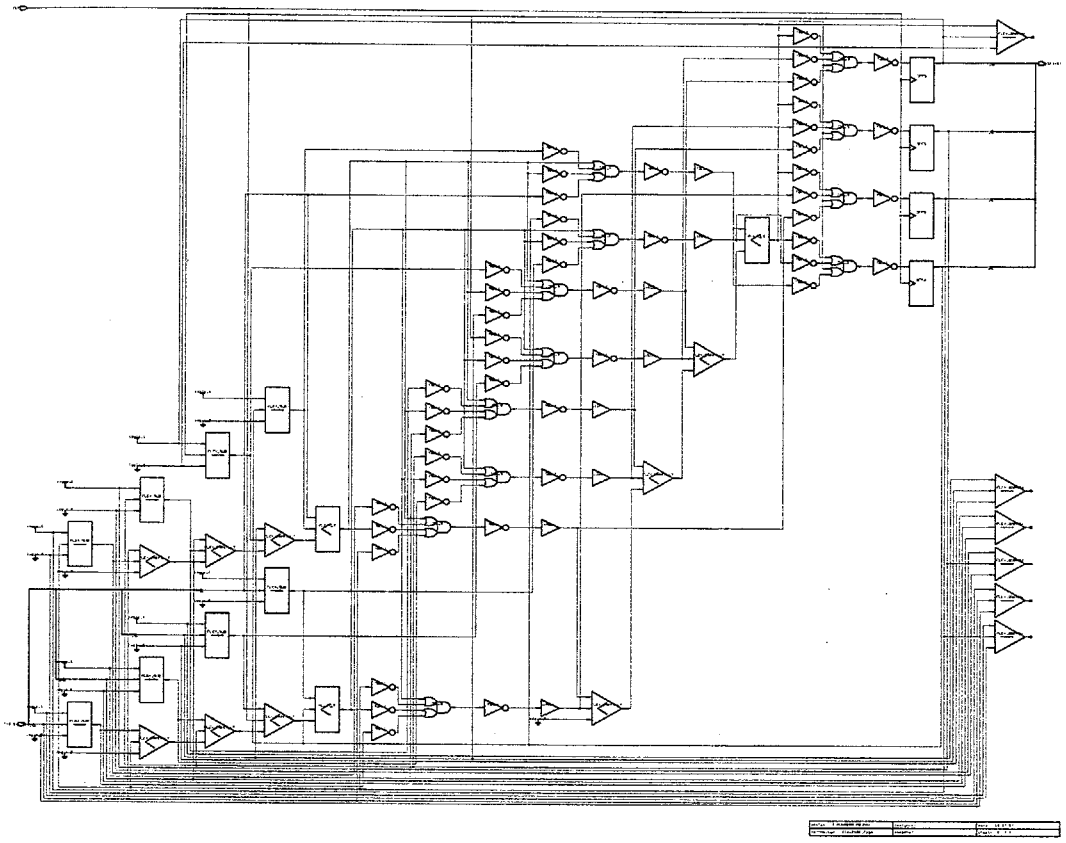


Figure 15: Circuit of T fuzzy flip-flop (minterm, max-min operation)

2.3.2 T fuzzy flip-flop

Max-min logical operation system Figure 15 shows the circuit of Eq. (2) in the logical operation system $(1-\cdot, \wedge, \vee)$. The logical product and sum are realized as comparators.

Algebraic operation system Figure 16 shows the circuit of Eq. (2) in the operation system $(1-\cdot, \cdot, \dot{+})$. An algebraic product is realized as a multiplier, and an algebraic sum as a multiplier and an adder.

Bounded operation system Figure 17 shows the circuit of Eq. (2) in the operation system $(1-\cdot, \odot, \oplus)$. A bounded product and sum are composed of comparators and adders.

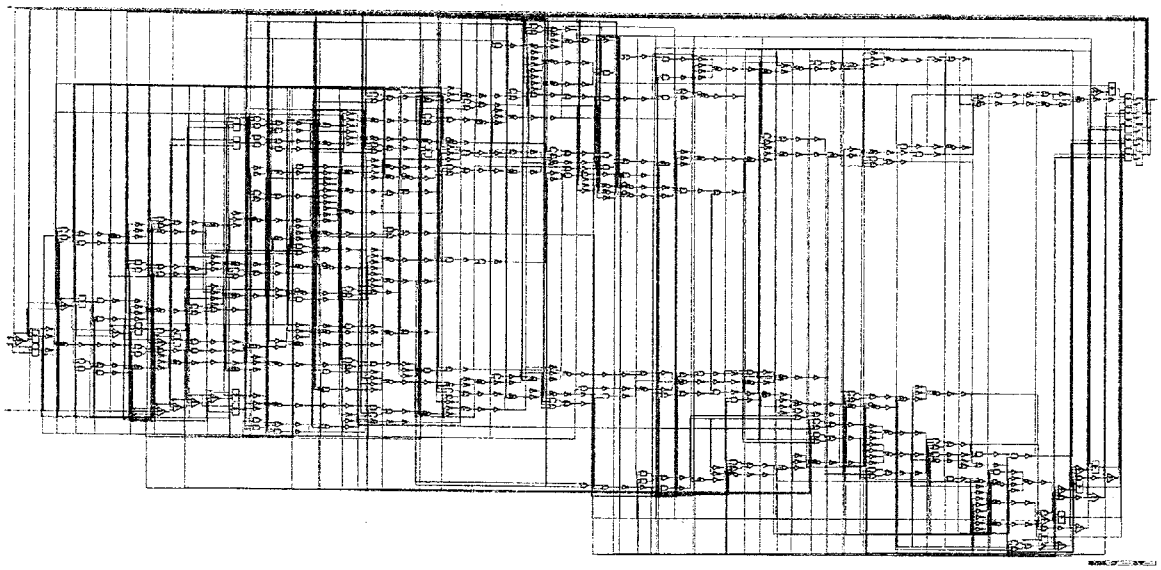


Figure 16: Circuit of T fuzzy flip-flop (minterm, algebraic operation)

Drastic operation system Figure 18 shows the circuit of Eq. (2) in the logical operation system $(1-\cdot, \barwedge, \barvee)$. A drastic product and sum are composed of comparator with constants.

2.3.3 SR fuzzy flip-flop

Max-min logical operation system Figure 19 and Figure 20 show the circuit of set-type and reset-type SR fuzzy flip-flops in the logical operation system $(1-\cdot, \wedge, \vee)$, respectively.

Algebraic operation system Figure 21 and Figure 22 show the circuit of set-type and reset-type SR fuzzy flip-flops in the algebraic operation system $(1-\cdot, \cdot, \dot{+})$, respectively.

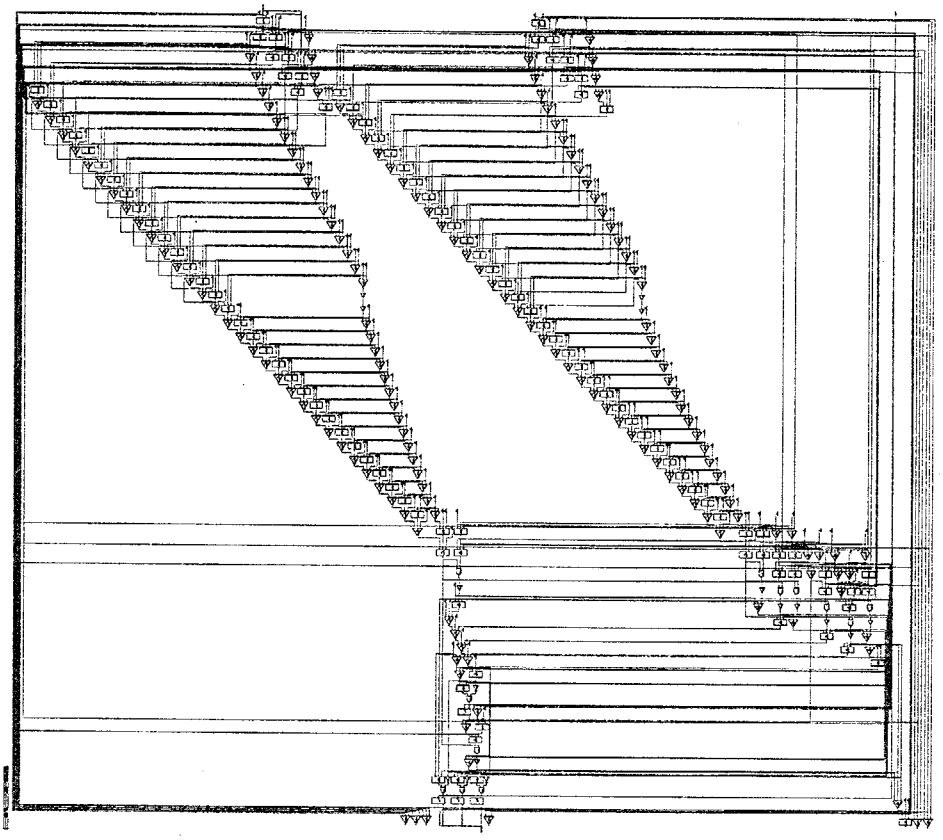


Figure 17: Circuit of T fuzzy flip-flop (minterm, bounded operation)

Bounded operation system Figure 23 and Figure 24 show the circuit of set-type and reset-type SR fuzzy flip-flops in the bounded operation system $(1-\cdot, \odot, \oplus)$, respectively.

Drastic operation system Figure 25 and Figure 26 show the circuit of set-type and reset-type SR fuzzy flip-flops in the drastic operation system $(1-\cdot, \wedge, \vee)$, respectively.

SR fuzzy flip-flop requires 2 inputs while T fuzzy flip-flop requires 1. But its logical form is simpler than T fuzzy flip-flop, hence its circuit area is smaller than that of T fuzzy flip-flop. Although set-type and reset-type SR fuzzy flip-flop have the same number of logical operations, their operation sequences are different. This fact does not affect their circuit areas but their delay times. In all cases of reset-type SR fuzzy flip-flops, the fuzzy negation $R(t)^{\textcircled{n}}$ and the t-norm $S(t)\textcircled{t}Q(T)$ can be performed at the same time, then,

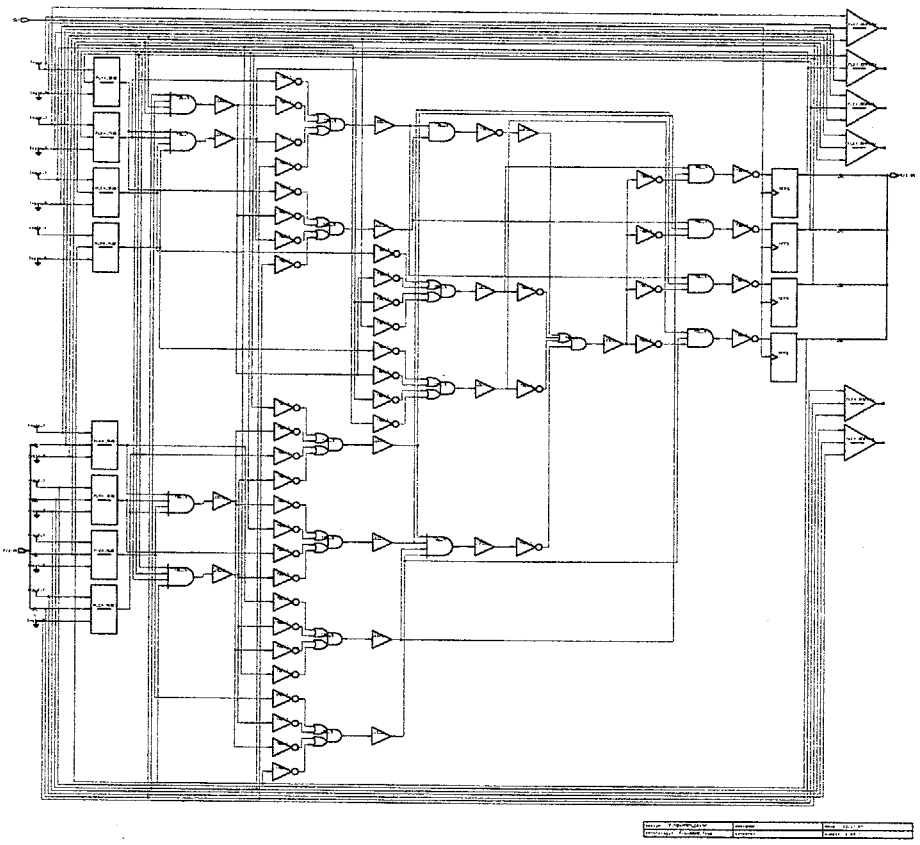


Figure 18: Circuit of T fuzzy flip-flop (minterm, drastic operation)

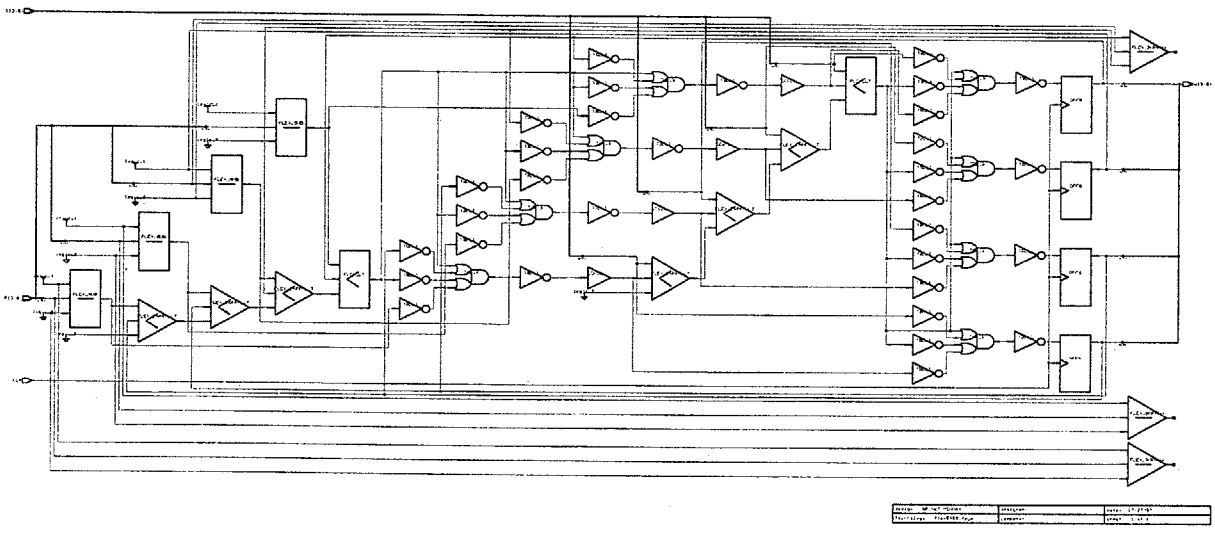


Figure 19: Circuit of set-type SR fuzzy flip-flop (max-min)

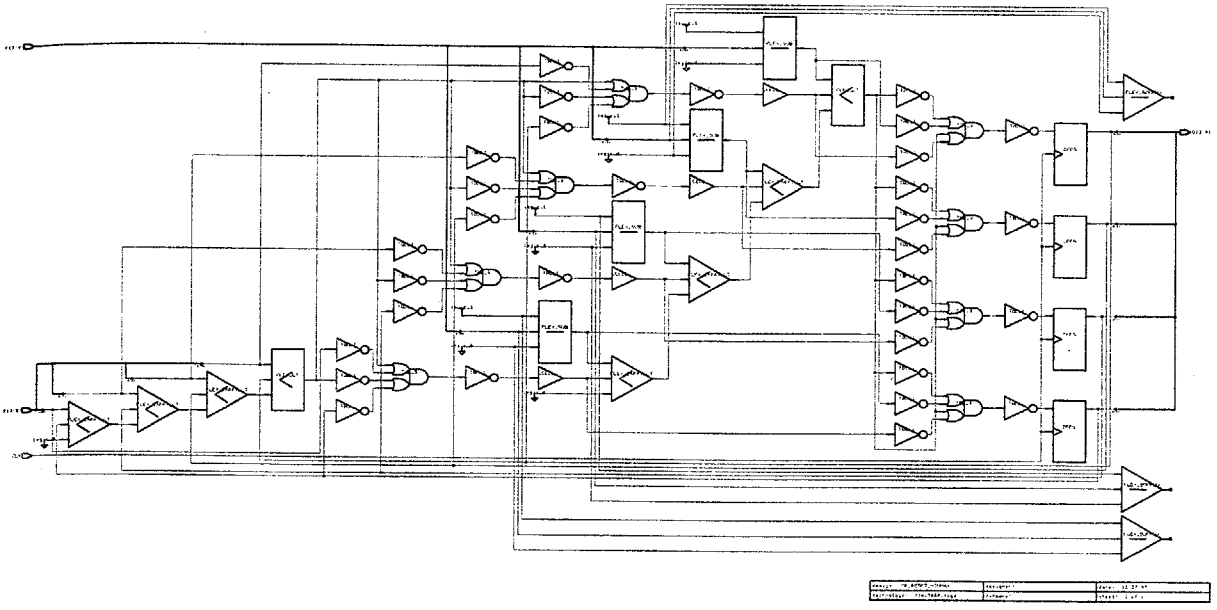


Figure 20: Circuit of reset-type SR fuzzy flip-flop (max-min)

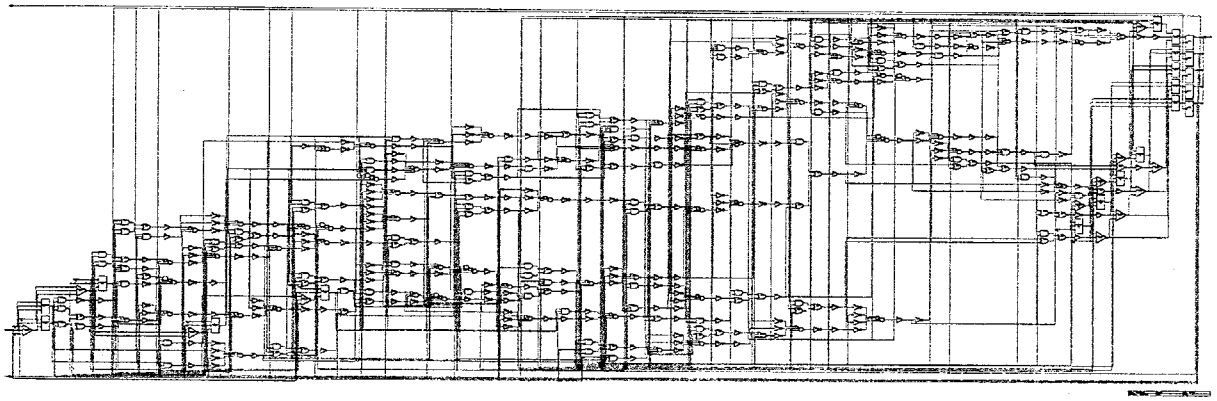


Figure 21: Circuit of set-type SR fuzzy flip-flop (algebraic)

the total delay time decreases, while all fuzzy operations are sequentially performed in the case of set-type. The processing speed of a fuzzy negation almost equals to that of a maximum or a minimum operation, and the advantage of the reset-type increases when the processing speed of t-norm is high—e.g. max-min logical or drastic operation systems.

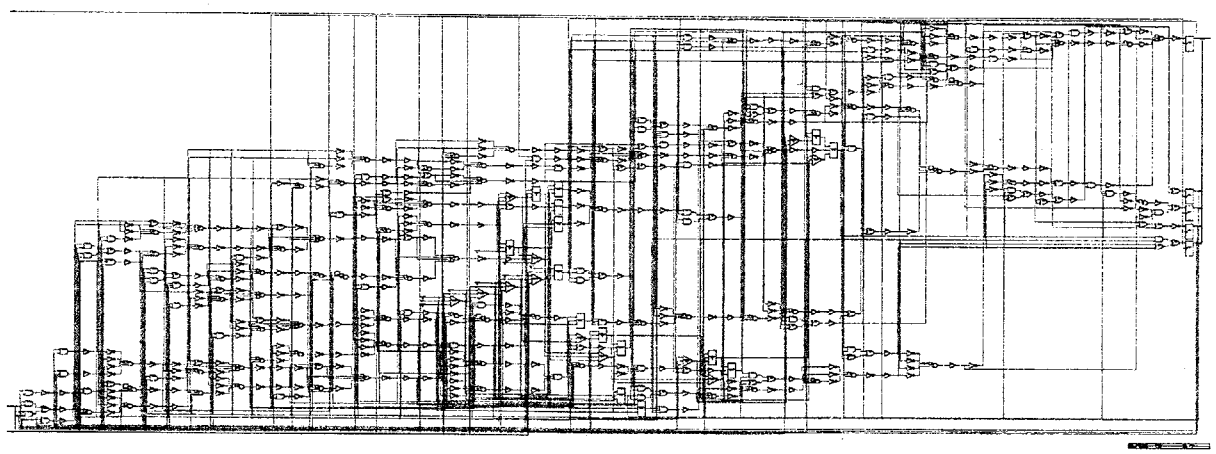


Figure 22: Circuit of reset-type SR fuzzy flip-flop (algebraic)

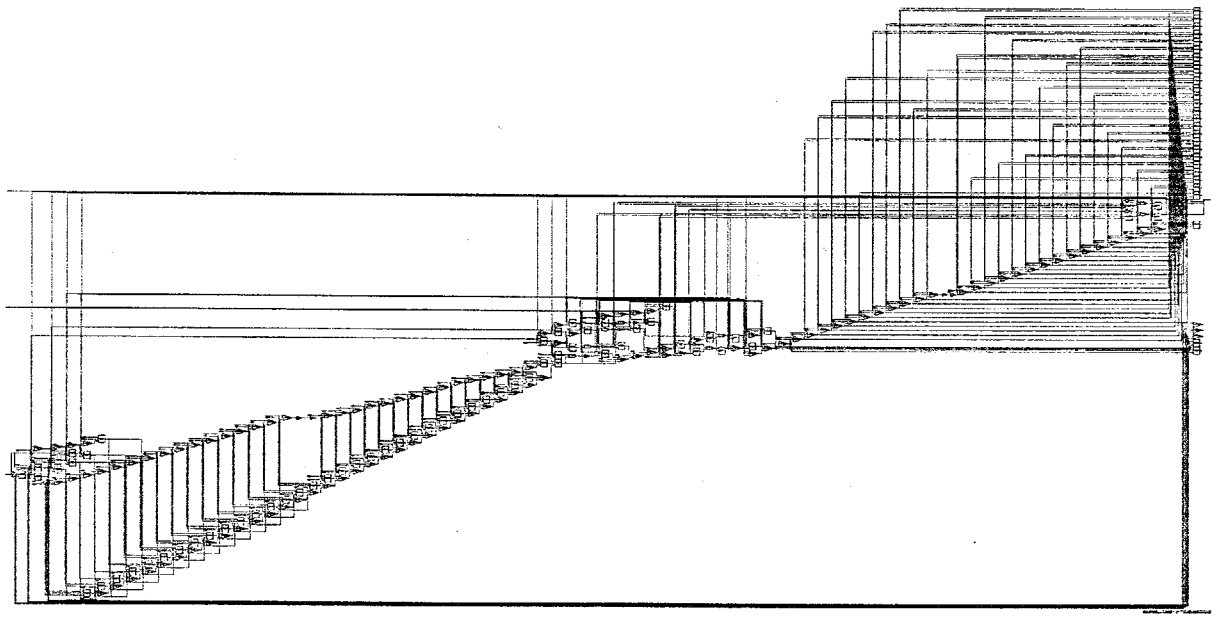


Figure 23: Circuit of set-type SR fuzzy flip-flop (bounded)

2.4 Performance of fuzzy flip-flops

Table 1 shows the comparison of functions that can be performed by various fuzzy flip-flops. The symbol "△" in JK-FFF[10] means that it can input arbitrary value only if both set-type and reset-type are used together and are configured appropriately.

Figure 27 shows circuit areas of D, T, and SR fuzzy flip-flops and that of unified form of JK fuzzy flip-flops[11][21] using logical, algebraic, bounded, and drastic operation

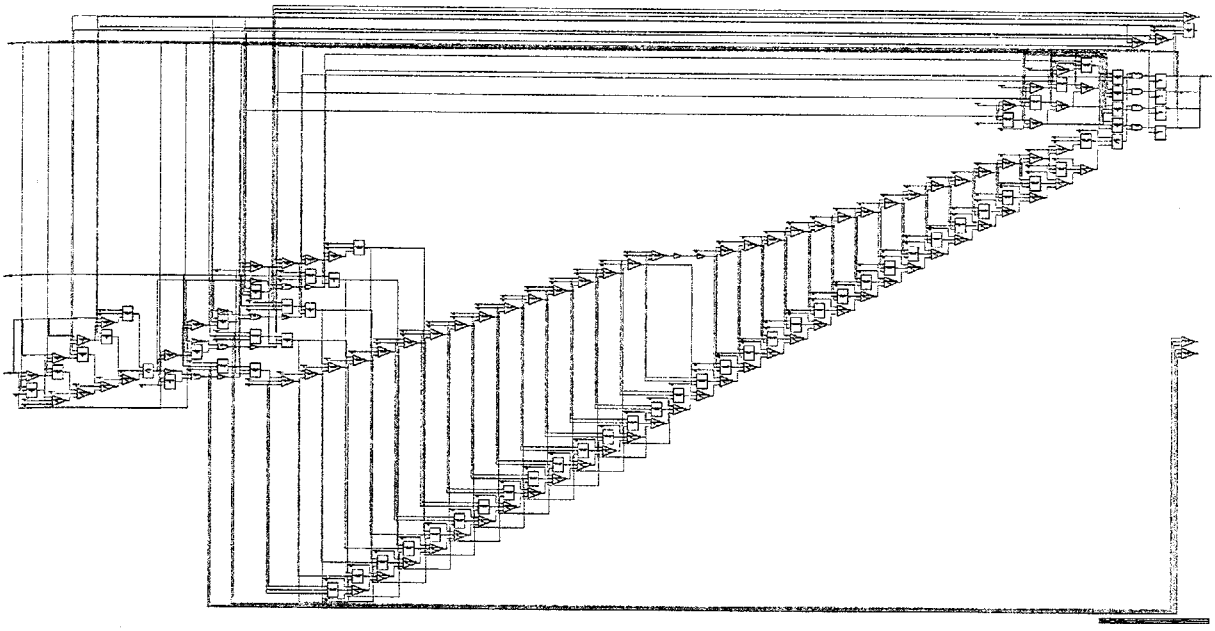


Figure 24: Circuit of reset-type SR fuzzy flip-flop (bounded)

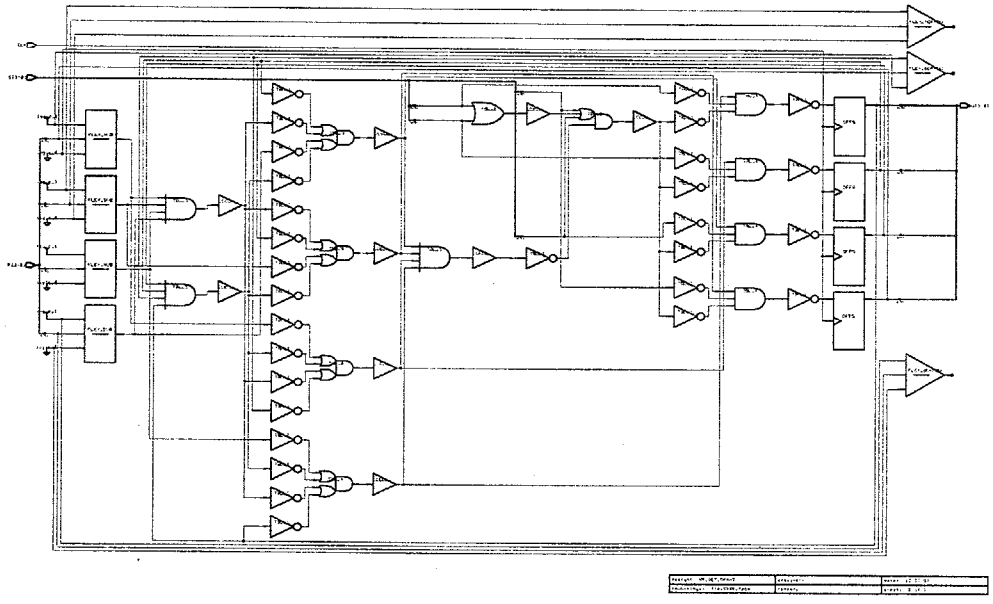


Figure 25: Circuit of set-type SR fuzzy flip-flop (drastic)

systems, respectively. Figure 28 shows their delay times. "Area" in Figure 27 indicates the number of gates, while "Delay" in Figure 28 indicates the time(ns) that the signal runs from inputs to outputs.

Compared with JK fuzzy flip-flops[11][21], T and SR fuzzy flip-flops use 2/3 and 1/2

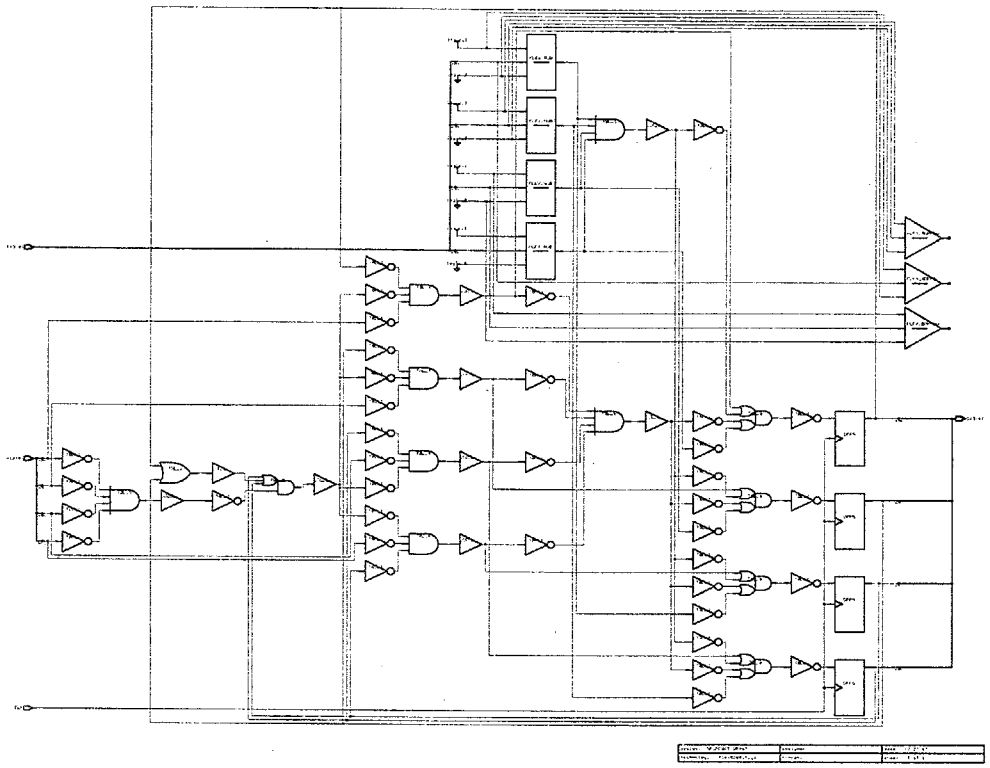


Figure 26: Circuit of reset-type SR fuzzy flip-flop (drastic)

Table 1: Comparison of functions

	Input	Hold	Negation
D-FFF	○	×	*times*
T-FFF	×	○	×
SR-FFF	○	○	×
JK-FFF[10]	△	○	○
JK-FFF[11][21]	○	○	○

area of circuit resources respectively, and their delay times are improved to 2/3 of that of JK's in every operation system. This fact shows that the circuit area of fuzzy flip-flops is proportional to the number of t-norm, s-norm, and fuzzy negation. As D fuzzy flip-flop is composed of output latches only, both its circuit area and delay time are negligible.

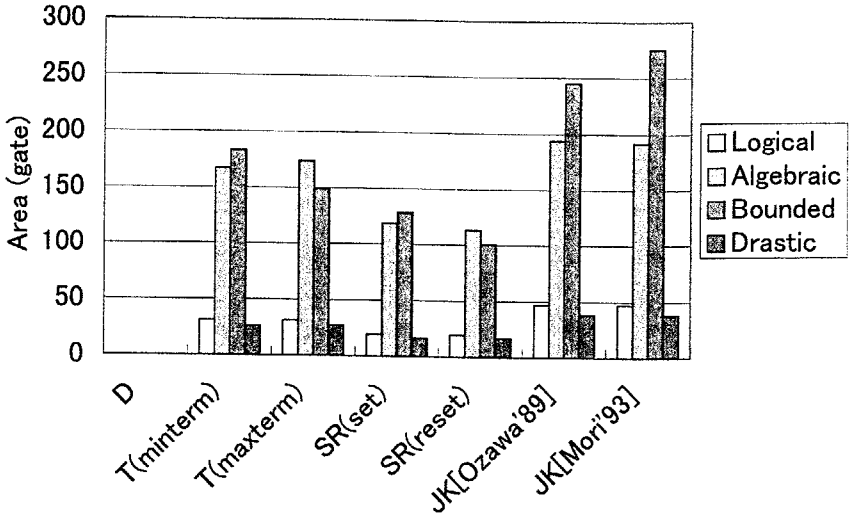


Figure 27: Circuit area (gates)

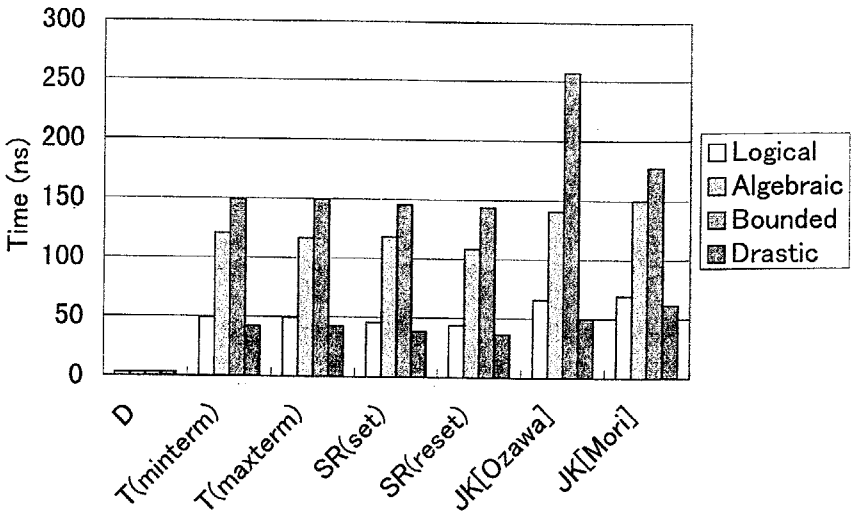


Figure 28: Delay time (ns)

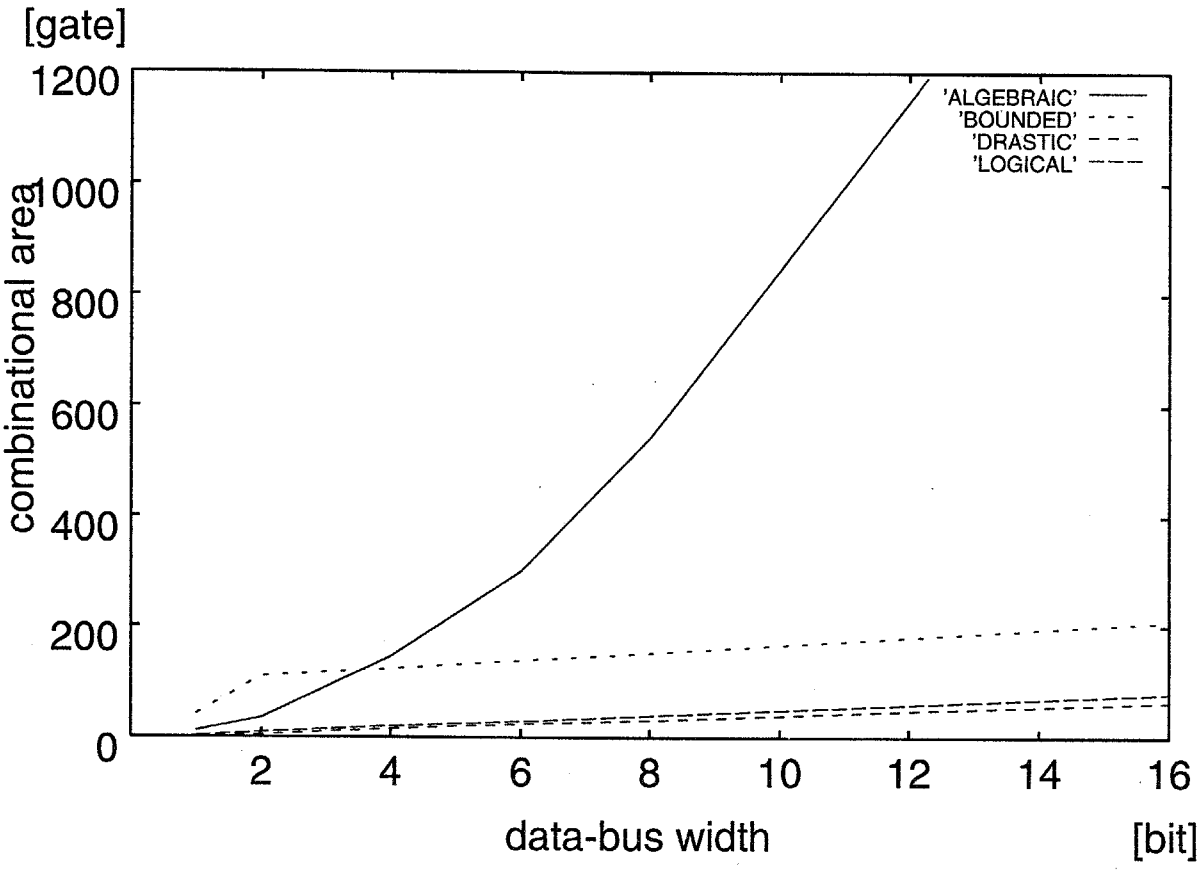


Figure 29: Quantization bits and circuit area of set-type SR-FFF

These results show that, proposed fuzzy flip-flops are improved with respect to circuit area and delay time, although their functions are more restricted than those of JK fuzzy flip-flop. This is because the number of operations, t-norm, s-norm, and fuzzy negation, is less than that of JK. Therefore, JK fuzzy flip-flop can be used for general purpose, whereas D, T, and SR fuzzy flip-flops, that are smaller than JK, are suitable for restricted cases. In particular, as SR fuzzy flip-flop has the functions for a memory, it can also be used as a fuzzy memory element like JK fuzzy flip-flop, while its circuit area is half of that of JK.

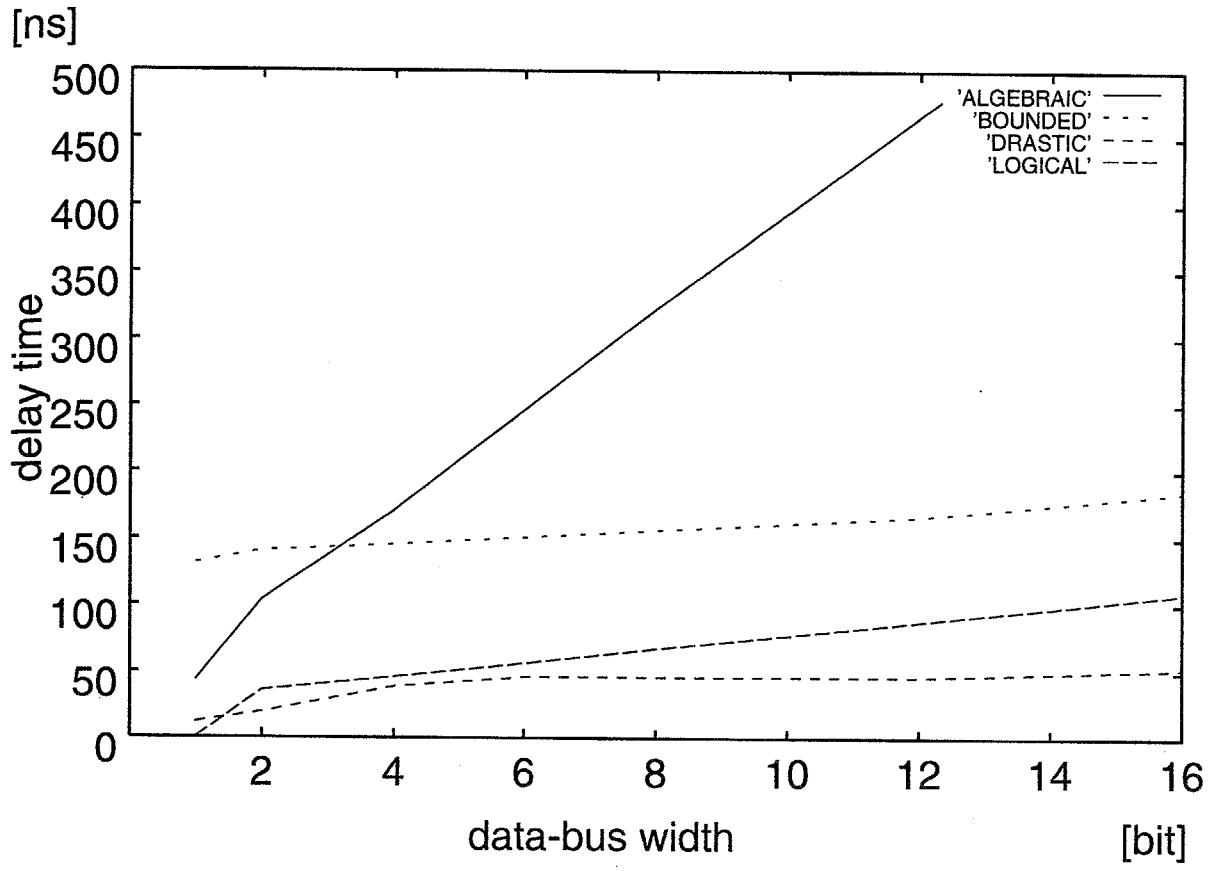


Figure 30: Quantization bits and delay time of set-type SR-FFF

2.5 Number of quantization bits

Figure 29 shows the relation between the number of quantization bits and the circuit area, and Figure 30 shows the relation between the number of quantization bits and the delay time in the case of set-type SR fuzzy flip-flop.

Under the fuzzy operation system $(1 - \cdot, \wedge, \vee)$, $(1 - \cdot, \odot, \oplus)$, and $(1 - \cdot, \barwedge, \barvee)$, the circuit area increases in proportion to the number of quantization bits. The reason of this is that they are constructed of comparator and adder, whose areas are in proportion to the quantization bits. Under $(1 - \cdot, \cdot, \dot{+})$, the circuit area increases in proportion to the square of the quantization bits because it requires the multiplier.

Under $(1 - \cdot, \wedge, \vee)$, $(1 - \cdot, \cdot, \dot{+})$, and $(1 - \cdot, \odot, \oplus)$, the delay time is proportion to the quantization bits. Under $(1 - \cdot, \barwedge, \barvee)$, the delay time does not increase with the

quantization bits because it only performs the comparison with a constant. In another word, $(1-\cdot, \barwedge, \barvee)$ does not deal with the fuzziness.

The realization under $(1-\cdot, \cdot, \dot{+})$ and $(1-\cdot, \odot, \oplus)$ requires more circuit resources than under $(1-\cdot, \wedge, \vee)$, $(1-\cdot, \barwedge, \barvee)$ except the case of only 1 or 2 bits are used for the quantization of fuzzy values. The fuzzy operation system $(1-\cdot, \barwedge, \barvee)$ hardly handle the fuzzy medium values and it is uncontinuous. Therefore max-min fuzzy logical operation $(1-\cdot, \wedge, \vee)$ is the most useful for the real applications.

2.6 Summary

In this chapter, D, T, and SR fuzzy flip-flop are defined as basic elements of a fuzzy memory module. Their characteristics are shown under four operation systems: max-min logical $(1-\cdot, \wedge, \vee)$, algebraic $(1-\cdot, \cdot, \dot{+})$, bounded $(1-\cdot, \odot, \oplus)$, and drastic $(1-\cdot, \barwedge, \barvee)$ operation systems. And then the inequalities between maxterm-expressed and minterm-expressed T fuzzy flip-flops, and between set-type and reset-type SR fuzzy flip-flops are analytically shown. The circuit ares of D, T, and SR fuzzy flip-flops decrease 2/3 to 1/3 of JK's, and delay times of them decrease 2/3 to 1/2 of JK's.

Chapter 3

Logical analysis using max-min operation system

3.1 Introduction

In 1993, Mori and Mukaidono studied JK fuzzy flip-flop using max-min operation systems[21]. The methods are based on B-ternary logic[22], which is a model of Kleenean algebra. When its t-norm and s-norm are restricted to minimum and maximum operations, respectively, the fuzzy logic and B-ternary logic are equivalent[8][23][24][28]. Therefore, it is sufficient to analyze fuzzy logical functions only when the values of their fuzzy logical variables are $\{0, 1/2, 1\}$.

Using this property, Mori and Mukaidono made the B-ternary logical truth table (constituted by the values $\{0, 1/2, 1\}$) of the characteristic function of the JK fuzzy flip-flop, in which the values of the binary compatible parts are defined strictly, while those of the other parts are defined with ambiguity. From this result, they obtained 64 types of fuzzy principal disjunctive canonical equations, and showed that the equations constitute a distributive lattice.

In this chapter, logical properties of D, T, and SR fuzzy flip-flops, which have defined in the preceding chapter, are analyzed using the max-min logical operation system. All logical forms that are fuzzy extensions of binary flip-flops are obtained. Using 2 kinds

of partially ordered relations between different logical functions, which are equivale under Boolean algebra (binary logic), partially ordered sets which the fuzzy extend logical forms of D, T, and SR fuzzy flip-flop constitute are shown as Hasse diagrams distributive lattices. In particular, these of D and T fuzzy flip-flops are Boolean lattic like the case of JK fuzzy flip-flop.

This result shows that a logical form of a fuzzy flip-flop, which is obtained by maximu and minimum operations between other logical forms of fuzzy flip-flop, is always valid a fuzzy logical function. In the case of D, T, and JK fuzzy flip-flops, the characteristi of logical functions as the extensions of binary maxterm and minterm expressions of flip-flop can be obtained from every other logical form by doing maximum and minimu operations with their complement. Furthermore, any characteristics of these fuzzy fli flops can be obtained from any other logical functions of the fuzzy flip-flops by doi maximum or minimum operation with its relative complement.

Since this chapter treats only max-min logical operation system $(1-\cdot, \wedge, \vee)$ as a fuz operation system, $\wedge$ may be omitted for the convenience.

3.2 Preliminaries

Definition Partially ordered relation of ambiguity[22].

Let $a, b \in [0,1]$, $a \overset{a}{\succeq} b$ if and only if $1/2 \geq a \geq b$ or $b \geq a \geq 1/2$.

Let $\boldsymbol{x}, \boldsymbol{y} \in [0,1]^n$ be fuzzy vectors of n dimensions $\{x_1, x_2, \cdots, x_n\}$, $\{y_1, y_2, \cdots, y_n$ $\boldsymbol{x} \overset{a}{\succeq} \boldsymbol{y}$ if and only if $x_i \overset{a}{\succeq} y_i$ for every $i \in \{0, \cdots, n\}$.

Let $f(\boldsymbol{x}), g(\boldsymbol{x})$ be fuzzy logical functions of n variables, $f \overset{a}{\succeq} g$ if and only if $f(\boldsymbol{x}) \overset{a}{\succeq} g($ for all $\boldsymbol{x} \in [0,1]^n$

It is clear that $1/2$ is the most ambiguous, and 0 and 1 are the least ambiguous. Figu 31 shows the Hasse diagram of the partially ordered relation of ambiguity.

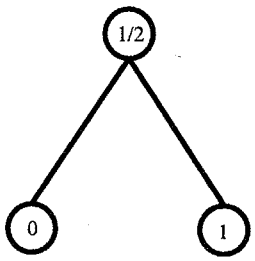


Figure 31: Partially ordered relation of ambiguity

Figure 32: Partially ordered relation of fuzzy values

Definition Partially ordered relation of fuzzy values[22].

Let $a, b \in [0,1]$, $a \overset{v}{\succeq} b$ if and only if $a \geq b$.

Let $\boldsymbol{x}, \boldsymbol{y} \in [0,1]^n$ be fuzzy vectors of n dimensions $\{x_1, x_2, \cdots, x_n\}$, $\{y_1, y_2, \cdots, y_n\}$, $\boldsymbol{x} \overset{v}{\succeq} \boldsymbol{y}$ if and only if $x_i \overset{v}{\succeq} y_i$ for every $i \in \{0, \cdots, n\}$.

Let $f(\boldsymbol{x}), g(\boldsymbol{x})$ be fuzzy logical functions of n variables, $f \overset{v}{\succeq} g$ if and only if $f(\boldsymbol{x}) \overset{v}{\succeq} g(\boldsymbol{x})$ for all $\boldsymbol{x} \in [0,1]^n$

□

This is a natural extension of ordered relation of boolean logic, and is generally considered as ordinary ordered relation in multiple-valued logic. In fact, this is a totally (linear) ordered relation. In this order, 0 and 1 are minimum and maximum, respectively, and 1/2 is the half.

Theorem 3.1[23] $f \equiv g$ in max-min fuzzy logic if and only if $f \equiv g$ in B-ternary logic.

Using this theorem, 3 important facts for max-min fuzzy logic are obtained.

- There are finite number of fuzzy extensions of a binary logical function.
- It is sufficient that the characteristics of a logical function are considered only when its fuzzy variables are $\{0, 1/2, 1\}$.
- The partially ordered sets of logical functions in B-ternary logic and max-min fuzzy logic have the same property.

Theorem 3.2[23] Let $\boldsymbol{x}$, $\boldsymbol{y}$ be n-dimensional ternary vector $\{0, 1/2, 1\}^n$, and let $f : \{0, 1/2, 1\}^n \to \{0, 1/2, 1\}$ be a fuzzy logical function,

$$\boldsymbol{x} \overset{a}{\succeq} \boldsymbol{y} \Longrightarrow f(\boldsymbol{x}) \overset{a}{\succeq} f(\boldsymbol{y}).$$

From this theorem, fuzzy logical functions hold ambiguity.

A fuzzy logical function $f(\boldsymbol{x})$ of n variables is called C-type logical function $f_C(\boldsymbol{x})$ if $\boldsymbol{x} \in \{0, 1/2, 1\}^n - \{0, 1\}^n \Rightarrow f(\boldsymbol{x}) = 1/2$. That is, if there is at least one variable whose value is $1/2$ in $f(\boldsymbol{x})$ then the value of $f(\boldsymbol{x})$ is $1/2$. The C means "canonical form" in binary logic. The C-type fuzzy logical function is the most ambiguous.

A fuzzy logical function $f(\boldsymbol{x})$ of n variables is called P-type logical function $f_P(\boldsymbol{x})$ if $f(\boldsymbol{x}) = 1/2 \Leftrightarrow \{f(\boldsymbol{x}')|\boldsymbol{x}' \in \{0, 1\}^n, \boldsymbol{x} \overset{a}{\succeq} \boldsymbol{x}'\} = \{0, 1\}$, $f(\boldsymbol{x}) < 1/2 \Leftrightarrow \{f(\boldsymbol{x}')|\boldsymbol{x}' \in \{0, 1\}^n, \boldsymbol{x} \overset{a}{\succeq} \boldsymbol{x}'\} = \{0\}$, $f(\boldsymbol{x}) > 1/2 \Leftrightarrow \{f(\boldsymbol{x}')|\boldsymbol{x}' \in \{0, 1\}^n, \boldsymbol{x} \overset{a}{\succeq} \boldsymbol{x}'\} = \{1\}$. The P means "prime implicant expansion" in binary logic. P-type fuzzy logical function is the least ambiguous.

From now on, for a logical function $f(\boldsymbol{x})$, $f_{CD}(\boldsymbol{x})$ indicates that f is a principal disjunctive canonical form in binary logic, and $f_{CC}(\boldsymbol{x})$ indicates that f is a principal conjunctive canonical form in binary logic.

D(t) \ Q(t)	0	1
0	0	0
1	1	1

Figure 33: Truth table of binary flip-flop

D(t) \ Q(t)	0	1/2	1
0	0	1/2 0	0
1/2	1/2	1/2	1/2
1	1	1 1/2	1

Figure 34: Truth table of D fuzzy flip-flop

3.3 D fuzzy flip-flop

In the boolean logic, D fuzzy flip-flop is defined as

$$Q(t+1) = D(t). \tag{38}$$

Its truth table is shown in Figure 33.

It can be generalized to B-ternary logic truth table(Figure 34).

The domain of the characteristic function is $D(t) \times Q(t) \in \{0, 1/2, 1\}^2$. When $(D(t), Q(t)) = (1/2, 0), (1/2, 1/2), (1/2, 1)$, the value of $Q(t+1)$ is uniquely determined as $1/2$ because both 0 and 1 exists as the value of their neighbor boxes. In such a case, the value of characteristics changes halfway from 0 to 1 or from 1 to 0, and it must take $1/2$ as its value. When $(D(t), Q(t)) = (0, 1/2)$, the value of $Q(t+1)$ can take 0 or $1/2$, while it can take $1/2$ or 1 in the case $(D(t), Q(t)) = (1, 1/2)$.

Therefore, 4 cases of characteristics of D flip-flop in B-ternary logic are considered according to the value of $Q(t+1)$ for $(D(t), Q(t)) = (0, 1/2), (1, 1/2)$. Principal disjunctive canonical forms of these characteristics are derived and shown in the following equations.

$$
\begin{array}{lrcl}
\text{(D1)} & Q(t+1) & = & DQ \vee DQ^{ⓝ} \\
\text{(D2)} & Q(t+1) & = & DQ \vee DQ^{ⓝ} \vee D^{ⓝ}QQ^{ⓝ} \\
\text{(D3)} & Q(t+1) & = & D \\
\text{(D4)} & Q(t+1) & = & D \vee D^{ⓝ}QQ^{ⓝ}
\end{array}
$$

Eq.(D3), which is the fuzzy extension of the simplest binary form of the D flip-flop's logical function (eq.(38)), is also valid as characteristic function of D flip-flop in B-ternary logic.

These 4 types of D fuzzy flip-flops constitute a boolean lattice 2^2 of 4 elements in the partially ordered relation $\overset{a}{\succeq}$. Figure 35 shows its Hasse diagram. Eq.(D3) is the least ambiguous and eq.(D2) is the most. Figure 36 shows the Hasse diagram of the relation $\overset{v}{\succeq}$ of D fuzzy flip-flops. In the case of D fuzzy flip-flops, the partially ordered sets of the forms of D fuzzy flip-flops with these 2 relations are (order-, lattice-)isomorphic, which constitute boolean lattices 2^2 containing 4 elements.

In the case of eq.(D2), when $Q(t) = 1/2$, $Q(t+1)$ cannot take any value except $1/2$ whatever any value of $D(t)$ is inputted. In general, when $Q(t)$ is an arbitrary value, $Q(t+1)$ can only take the value between $Q(t)$ and $Q(t)^{ⓝ}$. This means, in the case of eq.(D2), that a set operation cannot be done freely, and particularly when $Q(t+1) = 1/2$, any set operation cannot be done at all (cannot change to different value from $1/2$).

In the case of Eq.(D1), $Q(t+1)$ can only take the value less than $\max\{Q(t), Q(t)^{ⓝ}\}$. In particular, $Q(t+1)$ can only take the value less than $1/2$ when $Q(t) = 1/2$. In the case of eq.(D1), it can be set to the value between 0 and $1/2$ freely, but not to the value larger than $1/2$.

The characteristics of Eq.(D4) is dual of that of (D1). It can be set to the value between $1/2$ and 1 freely, but not to the value less than $1/2$.

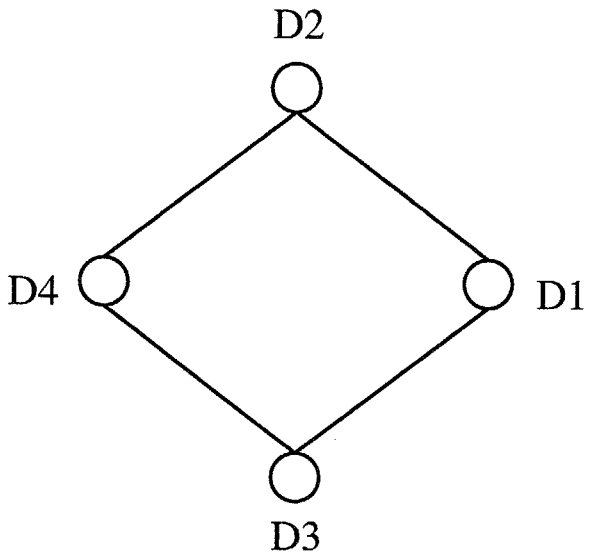


Figure 35: Partially ordered relation of ambiguity of D fuzzy flip-flops

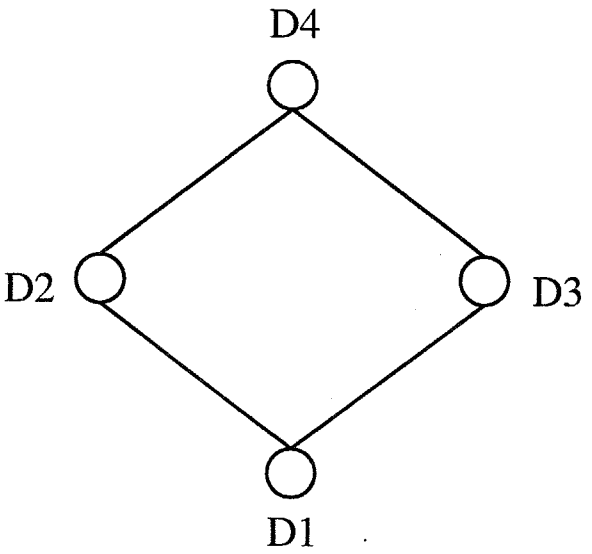


Figure 36: Partially ordered relation of fuzzy values of D fuzzy flip-flops

In the case of eq.(D2) and eq.(D4), once the value 0 and 1 are set to their $D(t)$, respectively, their $Q(t+1)$ are 0 and 1, and then, any value can be set to $Q(t+2) = D(t+1)$. Therefore, it is controllable, but cannot be directly controlled.

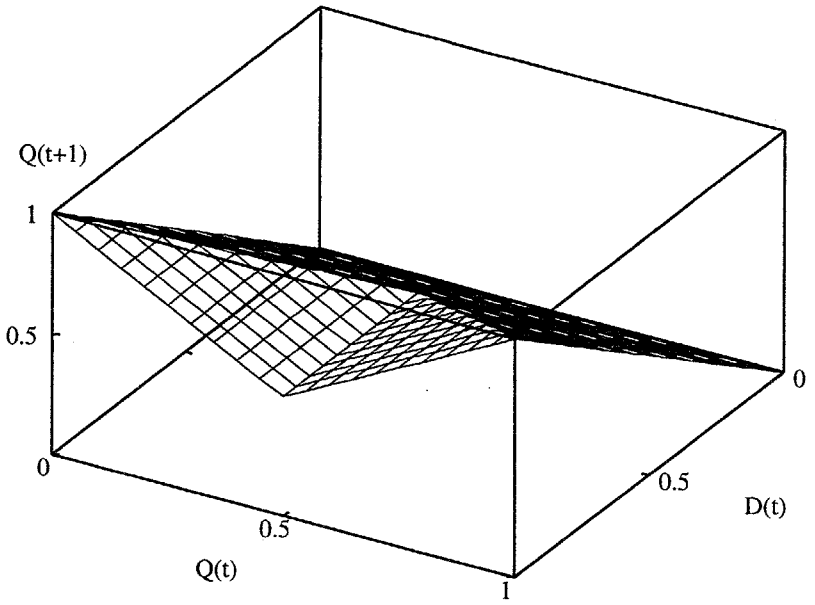


Figure 37: Characteristics of eq.(D1)

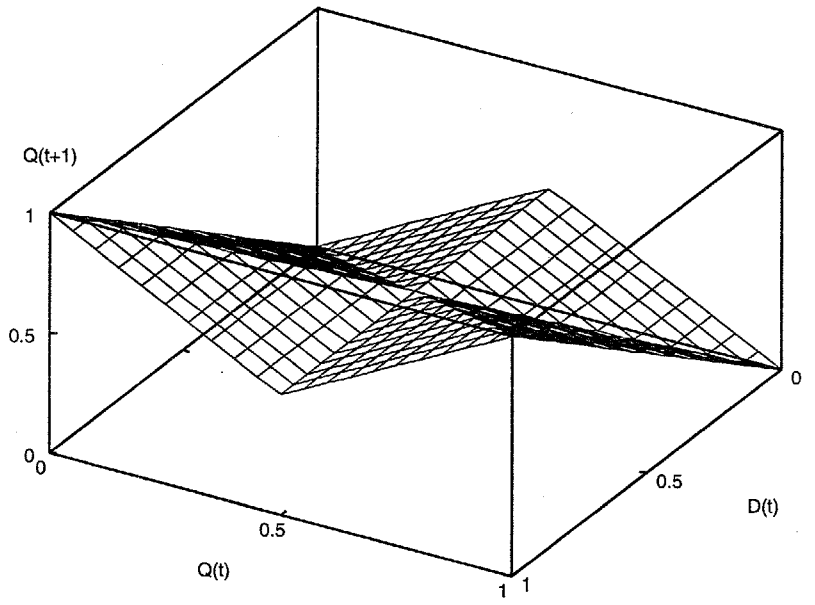


Figure 38: Characteristics of eq.(D2)

3.4 T fuzzy flip-flop

In the boolean logic, T fuzzy flip-flop is defined as

$$Q(t+1) = (T \wedge Q^{\textcircled{n}}) \vee (T^{\textcircled{n}} \wedge Q) \tag{39}$$

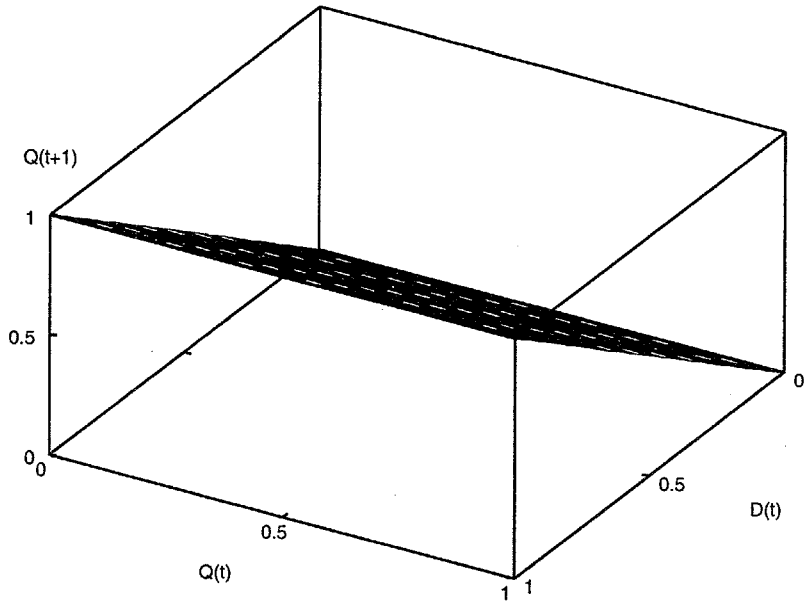


Figure 39: Characteristics of eq.(D3)

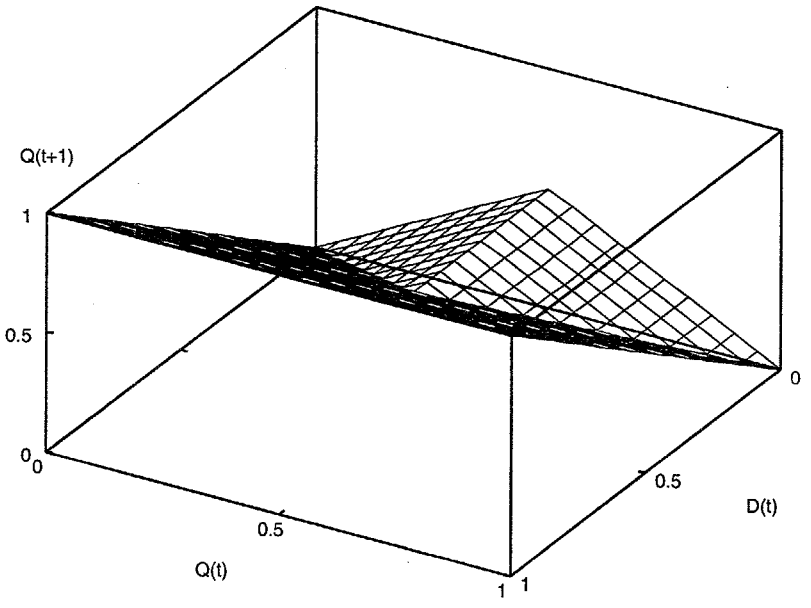


Figure 40: Characteristics of eq.(D4)

$$Q(t+1) = (T \vee Q) \wedge (T^{\textcircled{n}} \vee Q^{\textcircled{n}}) \tag{40}$$

Eq.(39) is the principal disjunctive canonical form and eq.(40) is the principal conjunctive canonical form of a characteristic function of T flip-flop.

Its truth table is as follows.

T(t) \ Q(t)	0	1
0	0	1
1	1	0

Figure 41: Truth table of binary T flip-flop

T(t) \ Q(t)	0	1/2	1
0	0	1/2	1
1/2	1/2	1/2	1/2
1	1	1/2	0

Figure 42: Truth table of T fuzzy flip-flop

It can be generalized to B-ternary logic truth table(Figure 42).

In the case of T fuzzy flip-flop, there exists only one fuzzy extension of binary T flip-flop. For all $\{D(t), Q(t)\} \in \{0, 1/2, 1\}^2$, $Q(t+1)$ is uniquely defined.

3.5 SR fuzzy flip-flop

Figure 43 shows the truth table of SR flip-flop, where S means set function and R means reset function. When the set input of the current time S(t) is 1, the output of the next time Q(t+1) is 1, and when reset input R(t) is 1, Q(t+1) is 0. Both of S(t) and R(t) are 0, then the next output Q(t+1) holds the current output Q(t). If both of S(t) and R(t) are 1, then the next output Q(t+1) is undefined. This is called "don't care term" and indicated by "*" in the truth table.

In order to realize the SR flip-flop in binary logic, "don't care term" is necessarily defined as 0 or 1. The former is called reset (preferred) type, the latter set (preferred) type. Figure 44 and figure 45 show the truth table of the set type and the reset type, respectively. Figure 46 and figure 47 show the extension of figure 44 and figure 45 to B-ternary logic, respectively.

In both of figure 46 and 47, there are 8 points whose values are compatible to that of binary logic, 11 points whose values are defined as 1/2 uniquely, and 8 points, from ① to ⑧, undefined, i.e., whose values are able to take one of 2 values. In the 7 points, from ① to ⑦ of 8 undefined points, the values are chosen independently from the values of other points. However, the value of the point indicated by "*", ⑧, depends on the values of other points. From this reason, the logical forms of SR fuzzy flip-flops do not constitute

R \ Q, S	0, 0	0, 1	1, 0	1, 1
0	0	1	1	1
1	0	1	0	*

*: Don't care

Figure 43: Truth table of binary SR flip-flop

R \ Q	0	0	1	1
S	0	1	0	1
0	0	1	1	1
1	0	1	0	1

Figure 44: Truth table of set type SR flip-flop

R \ Q	0	0	1	1
S	0	1	0	1
0	0	1	1	1
1	0	1	0	0

Figure 45: Truth table of reset type SR flip-flop

a boolean lattice.

R \ Q	0	0	0	$\frac{1}{2}$	$\frac{1}{2}$	$\frac{1}{2}$	1	1	1
S	0	$\frac{1}{2}$	1	0	$\frac{1}{2}$	1	0	$\frac{1}{2}$	1
0	0	$\frac{1}{2}$	1	$\frac{1}{2}$	$\frac{1}{2}$	1 / $\frac{1}{2}$ ⑤	1	1 / $\frac{1}{2}$ ③	1
$\frac{1}{2}$	0 / $\frac{1}{2}$ ①	$\frac{1}{2}$	1 / $\frac{1}{2}$ ④	$\frac{1}{2}$	$\frac{1}{2}$	1 / $\frac{1}{2}$ * ⑧	$\frac{1}{2}$	$\frac{1}{2}$	1 / $\frac{1}{2}$ ⑦
1	0	$\frac{1}{2}$	1	0 / $\frac{1}{2}$ ②	$\frac{1}{2}$	1 / $\frac{1}{2}$ ⑥	0	$\frac{1}{2}$	1

Figure 46: Truth table of set type SR fuzzy flip-flop

R \ Q	0	0	0	$\frac{1}{2}$	$\frac{1}{2}$	$\frac{1}{2}$	1	1	1
S	0	$\frac{1}{2}$	1	0	$\frac{1}{2}$	1	0	$\frac{1}{2}$	1
0	0	$\frac{1}{2}$	1	$\frac{1}{2}$	$\frac{1}{2}$	1 / $\frac{1}{2}$ ①	1	1 / $\frac{1}{2}$ ②	1
$\frac{1}{2}$	0 / $\frac{1}{2}$ ③	$\frac{1}{2}$	$\frac{1}{2}$	$\frac{1}{2}$	$\frac{1}{2}$	$\frac{1}{2}$	$\frac{1}{2}$	$\frac{1}{2}$	$\frac{1}{2}$
1	0	0 / $\frac{1}{2}$ ④	0	0 / $\frac{1}{2}$ ⑤	0 / $\frac{1}{2}$ * ⑧	0 / $\frac{1}{2}$ ⑥	0	0 / $\frac{1}{2}$ ⑦	0

Figure 47: Truth table of reset type SR fuzzy flip-flop

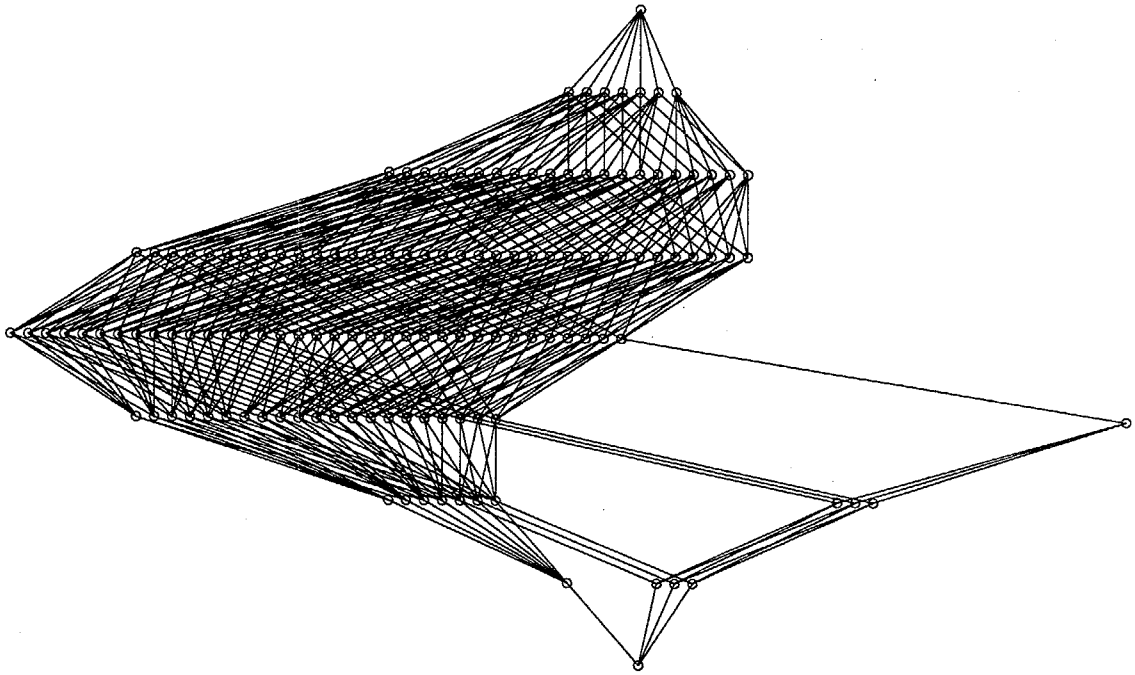


Figure 48: Hasse diagram of set type SR fuzzy flip-flop by partial order of ambiguity

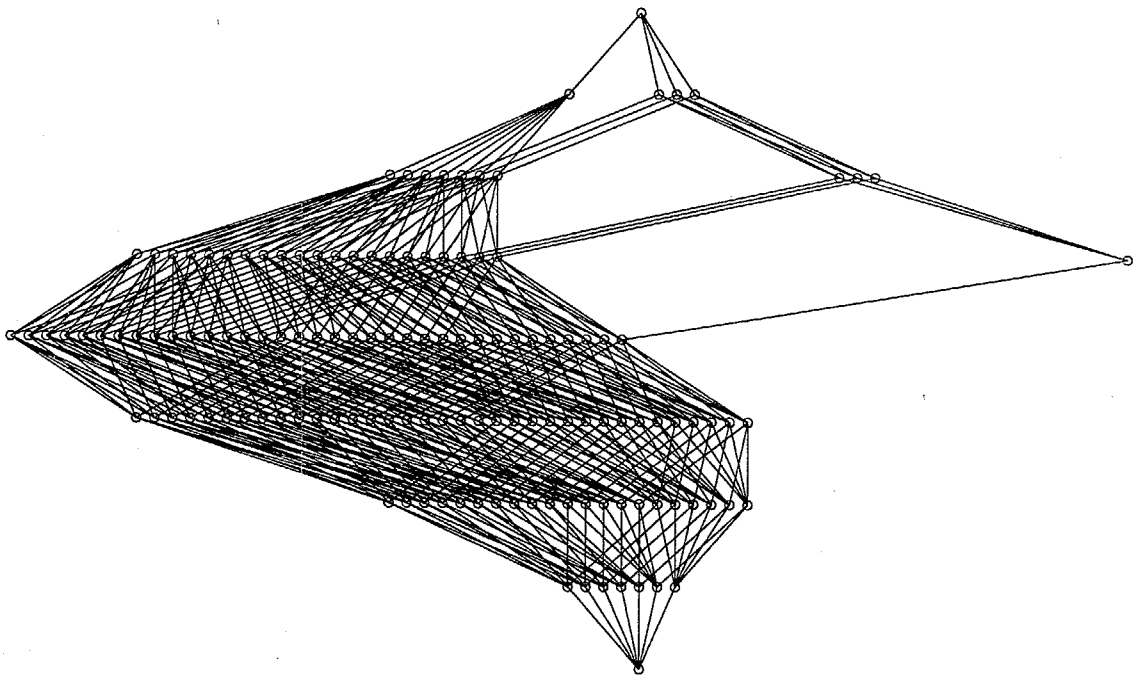


Figure 49: Hasse diagram of set type SR fuzzy flip-flop by partial order of values

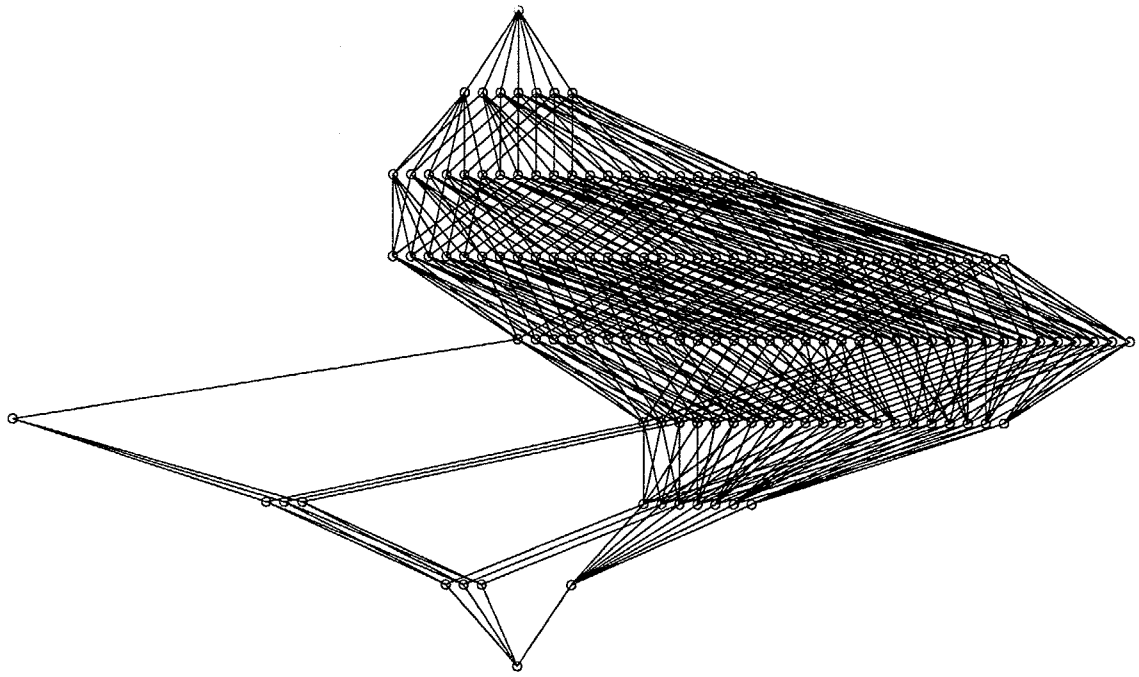


Figure 50: Hasse diagram of reset type SR fuzzy flip-flop by partial order of ambiguity

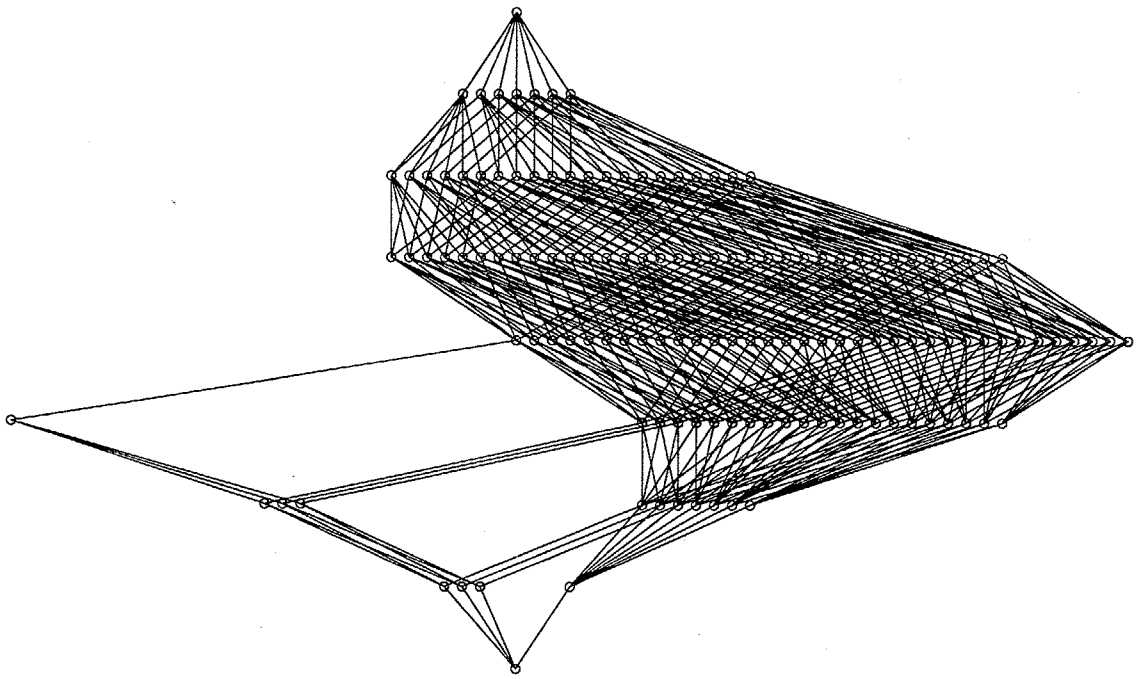


Figure 51: Hasse diagram of reset type SR fuzzy flip-flop by partial order of values

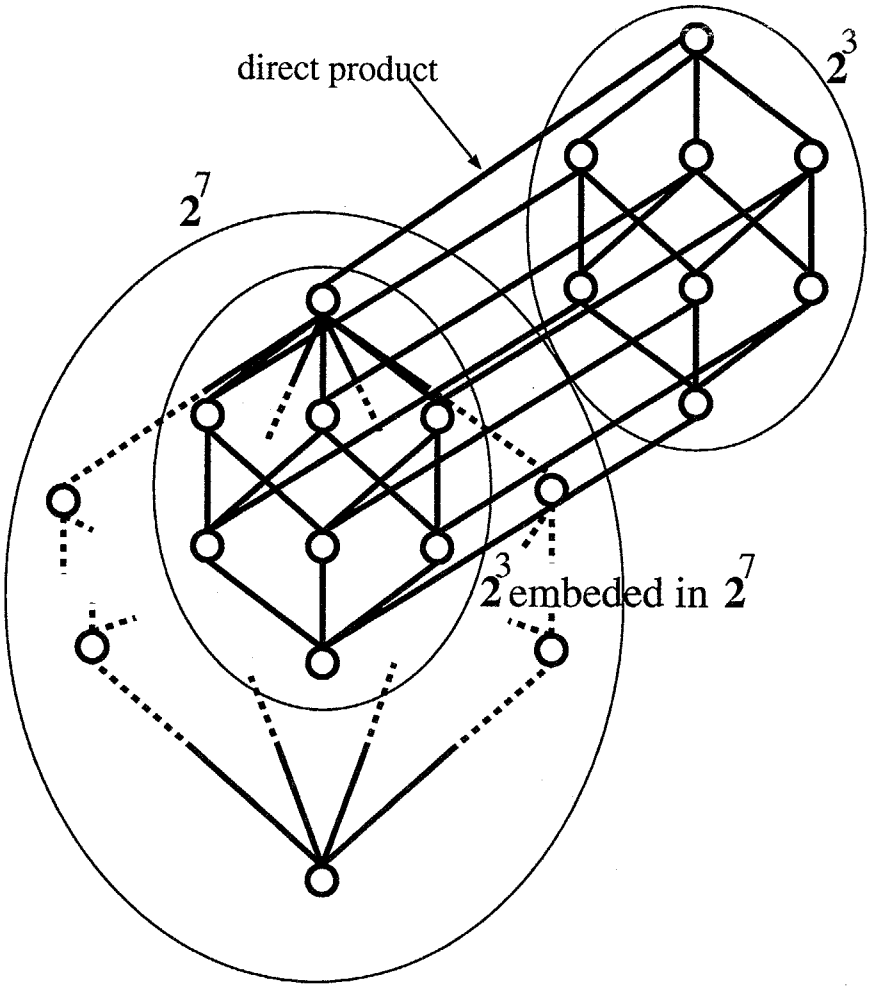


Figure 52: Concatenated structure of a lattice

Figure 48, figure 49, figure 50, figure 51 show the Hasse diagrams of the partial orders of ambiguity and values for the set type and reset type of SR fuzzy flip-flops, respectively. All of them show the distributive but not Boolean lattices. Their common structure is that each of them constitute the distributive sublattice of the Boolean lattice of order 256 (2^8). They are also concatenation of 2^7 (Boolean lattice of order 128) and 2^3 (Boolean lattice of order 8) which are sublattices of them. Concatenation means 2^3 and sublattice 2^3 in 2^7 are connected as direct product (Figure 52).

All 136 logical forms of set-type SR fuzzy flip-flop are shown in the followings table. The numbers of "value of undefined points" indicate same meaning as those in the figure 46 and figure 47.

value of undefined points 1 2 3 4 5 6 7 8	logical form of $Q(t+1)$
$00\frac{1}{2}\frac{1}{2}\frac{1}{2}\frac{1}{2}\frac{1}{2}\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{R}\bar{Q} \vee S\bar{R}Q \vee SR\bar{Q} \vee SRQ$
$\frac{1}{2}0\frac{1}{2}\frac{1}{2}\frac{1}{2}\frac{1}{2}\frac{1}{2}\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{R}\bar{Q} \vee S\bar{R}Q \vee SR\bar{Q} \vee SRQ \vee \bar{S}R\bar{R}\bar{Q}$
$0\frac{1}{2}\frac{1}{2}\frac{1}{2}\frac{1}{2}\frac{1}{2}\frac{1}{2}\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{R}\bar{Q} \vee S\bar{R}Q \vee SR\bar{Q} \vee SRQ \vee \bar{S}RQ\bar{Q}$
$\frac{1}{2}\frac{1}{2}\frac{1}{2}\frac{1}{2}\frac{1}{2}\frac{1}{2}\frac{1}{2}\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{R}\bar{Q} \vee S\bar{R}Q \vee SR\bar{Q} \vee SRQ \vee \bar{S}R\bar{R}\bar{Q} \vee \bar{S}RQ\bar{Q}$
$001\frac{1}{2}\frac{1}{2}\frac{1}{2}\frac{1}{2}\frac{1}{2}$	$\bar{R}Q \vee S\bar{R}\bar{Q} \vee SR\bar{Q} \vee SRQ$
$\frac{1}{2}01\frac{1}{2}\frac{1}{2}\frac{1}{2}\frac{1}{2}\frac{1}{2}$	$\bar{R}Q \vee S\bar{R}\bar{Q} \vee SR\bar{Q} \vee SRQ \vee \bar{S}R\bar{R}\bar{Q}$
$0\frac{1}{2}1\frac{1}{2}\frac{1}{2}\frac{1}{2}\frac{1}{2}\frac{1}{2}$	$\bar{R}Q \vee S\bar{R}\bar{Q} \vee SR\bar{Q} \vee SRQ \vee \bar{S}RQ\bar{Q}$
$\frac{1}{2}\frac{1}{2}1\frac{1}{2}\frac{1}{2}\frac{1}{2}\frac{1}{2}\frac{1}{2}$	$\bar{R}Q \vee S\bar{R}\bar{Q} \vee SR\bar{Q} \vee SRQ \vee \bar{S}R\bar{R}\bar{Q} \vee \bar{S}RQ\bar{Q}$
$00\frac{1}{2}1\frac{1}{2}\frac{1}{2}\frac{1}{2}\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{R}Q \vee S\bar{Q} \vee SRQ$
$\frac{1}{2}0\frac{1}{2}1\frac{1}{2}\frac{1}{2}\frac{1}{2}\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{R}Q \vee S\bar{Q} \vee SRQ \vee \bar{S}R\bar{R}\bar{Q}$
$0\frac{1}{2}\frac{1}{2}1\frac{1}{2}\frac{1}{2}\frac{1}{2}\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{R}Q \vee S\bar{Q} \vee SRQ \vee \bar{S}RQ\bar{Q}$
$\frac{1}{2}\frac{1}{2}\frac{1}{2}1\frac{1}{2}\frac{1}{2}\frac{1}{2}\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{R}Q \vee S\bar{Q} \vee SRQ \vee \bar{S}R\bar{R}\bar{Q} \vee \bar{S}RQ\bar{Q}$
$0011\frac{1}{2}\frac{1}{2}\frac{1}{2}\frac{1}{2}$	$\bar{R}Q \vee S\bar{Q} \vee SRQ$
$\frac{1}{2}011\frac{1}{2}\frac{1}{2}\frac{1}{2}\frac{1}{2}$	$\bar{R}Q \vee S\bar{Q} \vee SRQ \vee \bar{S}R\bar{R}\bar{Q}$
$0\frac{1}{2}11\frac{1}{2}\frac{1}{2}\frac{1}{2}\frac{1}{2}$	$\bar{R}Q \vee S\bar{Q} \vee SRQ \vee \bar{S}RQ\bar{Q}$
$\frac{1}{2}\frac{1}{2}11\frac{1}{2}\frac{1}{2}\frac{1}{2}\frac{1}{2}$	$\bar{R}Q \vee S\bar{Q} \vee SRQ \vee \bar{S}R\bar{R}\bar{Q} \vee \bar{S}RQ\bar{Q}$
$00\frac{1}{2}\frac{1}{2}1\frac{1}{2}\frac{1}{2}\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{R} \vee SR\bar{Q} \vee SRQ$
$\frac{1}{2}0\frac{1}{2}\frac{1}{2}1\frac{1}{2}\frac{1}{2}\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{R} \vee SR\bar{Q} \vee SRQ \vee \bar{S}R\bar{R}\bar{Q}$
$0\frac{1}{2}\frac{1}{2}\frac{1}{2}1\frac{1}{2}\frac{1}{2}\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{R} \vee SR\bar{Q} \vee SRQ \vee \bar{S}RQ\bar{Q}$
$\frac{1}{2}\frac{1}{2}\frac{1}{2}\frac{1}{2}1\frac{1}{2}\frac{1}{2}\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{R} \vee SR\bar{Q} \vee SRQ \vee \bar{S}R\bar{R}\bar{Q} \vee \bar{S}RQ\bar{Q}$
$001\frac{1}{2}\frac{1}{2}1\frac{1}{2}\frac{1}{2}$	$\bar{R}Q \vee S\bar{R} \vee SR\bar{Q} \vee SRQ$
$\frac{1}{2}01\frac{1}{2}\frac{1}{2}1\frac{1}{2}\frac{1}{2}$	$\bar{R}Q \vee S\bar{R} \vee SR\bar{Q} \vee SRQ \vee \bar{S}R\bar{R}\bar{Q}$
$0\frac{1}{2}1\frac{1}{2}\frac{1}{2}1\frac{1}{2}\frac{1}{2}$	$\bar{R}Q \vee S\bar{R} \vee SR\bar{Q} \vee SRQ \vee \bar{S}RQ\bar{Q}$
$\frac{1}{2}\frac{1}{2}1\frac{1}{2}\frac{1}{2}1\frac{1}{2}\frac{1}{2}$	$\bar{R}Q \vee S\bar{R} \vee SR\bar{Q} \vee SRQ \vee \bar{S}R\bar{R}\bar{Q} \vee \bar{S}RQ\bar{Q}$
$00\frac{1}{2}1\frac{1}{2}1\frac{1}{2}\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{R}Q \vee S\bar{Q} \vee SR$
$\frac{1}{2}0\frac{1}{2}1\frac{1}{2}1\frac{1}{2}\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{R}Q \vee S\bar{Q} \vee SR \vee \bar{S}R\bar{R}\bar{Q}$
$0\frac{1}{2}\frac{1}{2}1\frac{1}{2}1\frac{1}{2}\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{R}Q \vee S\bar{Q} \vee SR \vee \bar{S}RQ\bar{Q}$
$\frac{1}{2}\frac{1}{2}\frac{1}{2}1\frac{1}{2}1\frac{1}{2}\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{R}Q \vee S\bar{Q} \vee SR \vee \bar{S}R\bar{R}\bar{Q} \vee \bar{S}RQ\bar{Q}$
$0011\frac{1}{2}1\frac{1}{2}\frac{1}{2}$	$\bar{R}Q \vee S\bar{Q} \vee SR$
$\frac{1}{2}011\frac{1}{2}1\frac{1}{2}\frac{1}{2}$	$\bar{R}Q \vee S\bar{Q} \vee SR \vee \bar{S}R\bar{R}\bar{Q}$
$0\frac{1}{2}11\frac{1}{2}1\frac{1}{2}\frac{1}{2}$	$\bar{R}Q \vee S\bar{Q} \vee SR \vee \bar{S}RQ\bar{Q}$
$\frac{1}{2}\frac{1}{2}11\frac{1}{2}1\frac{1}{2}\frac{1}{2}$	$\bar{R}Q \vee S\bar{Q} \vee SR \vee \bar{S}R\bar{R}\bar{Q} \vee \bar{S}RQ\bar{Q}$
$00\frac{1}{2}\frac{1}{2}1\frac{1}{2}1\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{R} \vee SR\bar{Q} \vee SR$
$\frac{1}{2}0\frac{1}{2}\frac{1}{2}1\frac{1}{2}1\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{R} \vee SR\bar{Q} \vee SR \vee \bar{S}R\bar{R}\bar{Q}$
$0\frac{1}{2}\frac{1}{2}\frac{1}{2}1\frac{1}{2}1\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{R} \vee SR\bar{Q} \vee SR \vee \bar{S}RQ\bar{Q}$
$\frac{1}{2}\frac{1}{2}\frac{1}{2}\frac{1}{2}1\frac{1}{2}1\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{R} \vee SR\bar{Q} \vee SR \vee \bar{S}R\bar{R}\bar{Q} \vee \bar{S}RQ\bar{Q}$
$001\frac{1}{2}\frac{1}{2}1\frac{1}{2}1\frac{1}{2}$	$\bar{R}Q \vee S\bar{R}\bar{Q} \vee SR$
$\frac{1}{2}01\frac{1}{2}\frac{1}{2}1\frac{1}{2}1\frac{1}{2}$	$\bar{R}Q \vee S\bar{R}\bar{Q} \vee SR \vee \bar{S}R\bar{R}\bar{Q}$
$0\frac{1}{2}1\frac{1}{2}\frac{1}{2}1\frac{1}{2}1\frac{1}{2}$	$\bar{R}Q \vee S\bar{R}\bar{Q} \vee SR \vee \bar{S}RQ\bar{Q}$
$\frac{1}{2}\frac{1}{2}1\frac{1}{2}\frac{1}{2}1\frac{1}{2}1\frac{1}{2}$	$\bar{R}Q \vee S\bar{R}\bar{Q} \vee SR \vee \bar{S}R\bar{R}\bar{Q} \vee \bar{S}RQ\bar{Q}$
$00\frac{1}{2}1\frac{1}{2}1\frac{1}{2}1\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{R}Q \vee S\bar{Q} \vee SR$
$\frac{1}{2}0\frac{1}{2}1\frac{1}{2}1\frac{1}{2}1\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{R}Q \vee S\bar{Q} \vee SR \vee \bar{S}R\bar{R}\bar{Q}$
$0\frac{1}{2}\frac{1}{2}1\frac{1}{2}1\frac{1}{2}1\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{R}Q \vee S\bar{Q} \vee SR \vee \bar{S}RQ\bar{Q}$
$\frac{1}{2}\frac{1}{2}\frac{1}{2}1\frac{1}{2}1\frac{1}{2}1\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{R}Q \vee S\bar{Q} \vee SR \vee \bar{S}R\bar{R}\bar{Q} \vee \bar{S}RQ\bar{Q}$
$0011\frac{1}{2}1\frac{1}{2}1\frac{1}{2}$	$\bar{R}Q \vee S\bar{Q} \vee SR$

$\frac{1}{2}011\frac{1}{2}1\frac{1}{2}\frac{1}{2}$	$\bar{R}Q \vee S\bar{Q} \vee SR \vee \bar{S}R\bar{R}\bar{Q}$
$0\frac{1}{2}11\frac{1}{2}1\frac{1}{2}\frac{1}{2}$	$\bar{R}Q \vee S\bar{Q} \vee SR \vee \bar{S}RQ\bar{Q}$
$\frac{1}{2}\frac{1}{2}11\frac{1}{2}1\frac{1}{2}\frac{1}{2}$	$\bar{R}Q \vee S\bar{Q} \vee SR \vee \bar{S}R\bar{R}\bar{Q} \vee \bar{S}RQ\bar{Q}$
$00\frac{1}{2}\frac{1}{2}11\frac{1}{2}\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{R} \vee SR$
$\frac{1}{2}0\frac{1}{2}\frac{1}{2}11\frac{1}{2}\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{R} \vee SR \vee \bar{S}R\bar{R}\bar{Q}$
$0\frac{1}{2}\frac{1}{2}\frac{1}{2}11\frac{1}{2}\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{R} \vee SR \vee \bar{S}RQ\bar{Q}$
$\frac{1}{2}\frac{1}{2}\frac{1}{2}\frac{1}{2}11\frac{1}{2}\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{R} \vee SR \vee \bar{S}R\bar{R}\bar{Q} \vee \bar{S}RQ\bar{Q}$
$001\frac{1}{2}11\frac{1}{2}\frac{1}{2}$	$\bar{R}Q \vee S\bar{R} \vee SR$
$\frac{1}{2}01\frac{1}{2}11\frac{1}{2}\frac{1}{2}$	$\bar{R}Q \vee S\bar{R} \vee SR \vee \bar{S}R\bar{R}\bar{Q}$
$0\frac{1}{2}1\frac{1}{2}11\frac{1}{2}\frac{1}{2}$	$\bar{R}Q \vee S\bar{R} \vee SR \vee \bar{S}RQ\bar{Q}$
$\frac{1}{2}\frac{1}{2}1\frac{1}{2}11\frac{1}{2}\frac{1}{2}$	$\bar{R}Q \vee S\bar{R} \vee SR \vee \bar{S}R\bar{R}\bar{Q} \vee \bar{S}RQ\bar{Q}$
$00\frac{1}{2}111\frac{1}{2}\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{R} \vee S\bar{Q} \vee SR$
$\frac{1}{2}0\frac{1}{2}111\frac{1}{2}\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{R} \vee S\bar{Q} \vee SR \vee \bar{S}R\bar{R}\bar{Q}$
$0\frac{1}{2}\frac{1}{2}111\frac{1}{2}\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{R} \vee S\bar{Q} \vee SR \vee \bar{S}RQ\bar{Q}$
$\frac{1}{2}\frac{1}{2}\frac{1}{2}111\frac{1}{2}\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{R} \vee S\bar{Q} \vee SR \vee \bar{S}R\bar{R}\bar{Q} \vee \bar{S}RQ\bar{Q}$
$001111\frac{1}{2}\frac{1}{2}$	$\bar{R}Q \vee S\bar{R} \vee S\bar{Q} \vee SR$
$\frac{1}{2}01111\frac{1}{2}\frac{1}{2}$	$\bar{R}Q \vee S\bar{R} \vee S\bar{Q} \vee SR \vee \bar{S}R\bar{R}\bar{Q}$
$0\frac{1}{2}1111\frac{1}{2}\frac{1}{2}$	$\bar{R}Q \vee S\bar{R} \vee S\bar{Q} \vee SR \vee \bar{S}RQ\bar{Q}$
$\frac{1}{2}\frac{1}{2}1111\frac{1}{2}\frac{1}{2}$	$\bar{R}Q \vee S\bar{R} \vee S\bar{Q} \vee SR \vee \bar{S}R\bar{R}\bar{Q} \vee \bar{S}RQ\bar{Q}$
$00\frac{1}{2}\frac{1}{2}\frac{1}{2}1\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{R}\bar{Q} \vee SQ \vee SR\bar{Q}$
$\frac{1}{2}0\frac{1}{2}\frac{1}{2}\frac{1}{2}1\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{R}\bar{Q} \vee SQ \vee SR\bar{Q} \vee \bar{S}R\bar{R}\bar{Q}$
$0\frac{1}{2}\frac{1}{2}\frac{1}{2}\frac{1}{2}1\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{R}\bar{Q} \vee SQ \vee SR\bar{Q} \vee \bar{S}RQ\bar{Q}$
$\frac{1}{2}\frac{1}{2}\frac{1}{2}\frac{1}{2}\frac{1}{2}1\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{R}\bar{Q} \vee SQ \vee SR\bar{Q} \vee \bar{S}R\bar{R}\bar{Q} \vee \bar{S}RQ\bar{Q}$
$001\frac{1}{2}\frac{1}{2}\frac{1}{2}1\frac{1}{2}$	$\bar{R}Q \vee S\bar{R}\bar{Q} \vee SQ \vee SR\bar{Q}$
$\frac{1}{2}01\frac{1}{2}\frac{1}{2}\frac{1}{2}1\frac{1}{2}$	$\bar{R}Q \vee S\bar{R}\bar{Q} \vee SQ \vee SR\bar{Q} \vee \bar{S}R\bar{R}\bar{Q}$
$0\frac{1}{2}1\frac{1}{2}\frac{1}{2}\frac{1}{2}1\frac{1}{2}$	$\bar{R}Q \vee S\bar{R}\bar{Q} \vee SQ \vee SR\bar{Q} \vee \bar{S}RQ\bar{Q}$
$\frac{1}{2}\frac{1}{2}1\frac{1}{2}\frac{1}{2}\frac{1}{2}1\frac{1}{2}$	$\bar{R}Q \vee S\bar{R}\bar{Q} \vee SQ \vee SR\bar{Q} \vee \bar{S}R\bar{R}\bar{Q} \vee \bar{S}RQ\bar{Q}$
$00\frac{1}{2}1\frac{1}{2}\frac{1}{2}1\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{Q} \vee SQ$
$\frac{1}{2}0\frac{1}{2}1\frac{1}{2}\frac{1}{2}1\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{Q} \vee SQ \vee \bar{S}R\bar{R}\bar{Q}$
$0\frac{1}{2}\frac{1}{2}1\frac{1}{2}\frac{1}{2}1\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{Q} \vee SQ \vee \bar{S}RQ\bar{Q}$
$\frac{1}{2}\frac{1}{2}\frac{1}{2}1\frac{1}{2}\frac{1}{2}1\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{Q} \vee SQ \vee \bar{S}R\bar{R}\bar{Q} \vee \bar{S}RQ\bar{Q}$
$0011\frac{1}{2}\frac{1}{2}1\frac{1}{2}$	$\bar{R}Q \vee S\bar{Q} \vee SQ$
$\frac{1}{2}011\frac{1}{2}\frac{1}{2}1\frac{1}{2}$	$\bar{R}Q \vee S\bar{Q} \vee SQ \vee \bar{S}R\bar{R}\bar{Q}$
$0\frac{1}{2}11\frac{1}{2}\frac{1}{2}1\frac{1}{2}$	$\bar{R}Q \vee S\bar{Q} \vee SQ \vee \bar{S}RQ\bar{Q}$
$\frac{1}{2}\frac{1}{2}11\frac{1}{2}\frac{1}{2}1\frac{1}{2}$	$\bar{R}Q \vee S\bar{Q} \vee SQ \vee \bar{S}R\bar{R}\bar{Q} \vee \bar{S}RQ\bar{Q}$
$00\frac{1}{2}\frac{1}{2}1\frac{1}{2}1\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{R} \vee SQ \vee SR\bar{Q}$
$\frac{1}{2}0\frac{1}{2}\frac{1}{2}1\frac{1}{2}1\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{R} \vee SQ \vee SR\bar{Q} \vee \bar{S}R\bar{R}\bar{Q}$
$0\frac{1}{2}\frac{1}{2}\frac{1}{2}1\frac{1}{2}1\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{R} \vee SQ \vee SR\bar{Q} \vee \bar{S}RQ\bar{Q}$
$\frac{1}{2}\frac{1}{2}\frac{1}{2}\frac{1}{2}1\frac{1}{2}1\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{R} \vee SQ \vee SR\bar{Q} \vee \bar{S}R\bar{R}\bar{Q} \vee \bar{S}RQ\bar{Q}$
$001\frac{1}{2}1\frac{1}{2}1\frac{1}{2}$	$\bar{R}Q \vee S\bar{R} \vee SQ \vee SR\bar{Q}$
$\frac{1}{2}01\frac{1}{2}1\frac{1}{2}1\frac{1}{2}$	$\bar{R}Q \vee S\bar{R} \vee SQ \vee SR\bar{Q} \vee \bar{S}R\bar{R}\bar{Q}$
$0\frac{1}{2}1\frac{1}{2}1\frac{1}{2}1\frac{1}{2}$	$\bar{R}Q \vee S\bar{R} \vee SQ \vee SR\bar{Q} \vee \bar{S}RQ\bar{Q}$
$\frac{1}{2}\frac{1}{2}1\frac{1}{2}1\frac{1}{2}1\frac{1}{2}$	$\bar{R}Q \vee S\bar{R} \vee SQ \vee SR\bar{Q} \vee \bar{S}R\bar{R}\bar{Q} \vee \bar{S}RQ\bar{Q}$
$00\frac{1}{2}11\frac{1}{2}1\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{R} \vee S\bar{Q} \vee SQ$
$\frac{1}{2}0\frac{1}{2}11\frac{1}{2}1\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{R} \vee S\bar{Q} \vee SQ \vee \bar{S}R\bar{R}\bar{Q}$

$0\frac{1}{2}\frac{1}{2}11\frac{1}{2}1\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{R} \vee S\bar{Q} \vee SQ \vee \bar{S}RQ\bar{Q}$
$\frac{1}{2}\frac{1}{2}\frac{1}{2}11\frac{1}{2}1\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{R} \vee S\bar{Q} \vee SQ \vee \bar{S}R\bar{R}\bar{Q} \vee \bar{S}RQ\bar{Q}$
$00111\frac{1}{2}1\frac{1}{2}$	$\bar{R}Q \vee S\bar{R} \vee S\bar{Q} \vee SQ$
$\frac{1}{2}0111\frac{1}{2}1\frac{1}{2}$	$\bar{R}Q \vee S\bar{R} \vee S\bar{Q} \vee SQ \vee \bar{S}R\bar{R}\bar{Q}$
$0\frac{1}{2}111\frac{1}{2}1\frac{1}{2}$	$\bar{R}Q \vee S\bar{R} \vee S\bar{Q} \vee SQ \vee \bar{S}RQ\bar{Q}$
$\frac{1}{2}\frac{1}{2}111\frac{1}{2}1\frac{1}{2}$	$\bar{R}Q \vee S\bar{R} \vee S\bar{Q} \vee SQ \vee \bar{S}R\bar{R}\bar{Q} \vee \bar{S}RQ\bar{Q}$
$00\frac{1}{2}\frac{1}{2}\frac{1}{2}11\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{R}\bar{Q} \vee SQ \vee SR$
$\frac{1}{2}0\frac{1}{2}\frac{1}{2}\frac{1}{2}11\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{R}\bar{Q} \vee SQ \vee SR \vee \bar{S}R\bar{R}\bar{Q}$
$0\frac{1}{2}\frac{1}{2}\frac{1}{2}\frac{1}{2}11\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{R}\bar{Q} \vee SQ \vee SR \vee \bar{S}RQ\bar{Q}$
$\frac{1}{2}\frac{1}{2}\frac{1}{2}\frac{1}{2}\frac{1}{2}11\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{R}\bar{Q} \vee SQ \vee SR \vee \bar{S}R\bar{R}\bar{Q} \vee \bar{S}RQ\bar{Q}$
$001\frac{1}{2}\frac{1}{2}11\frac{1}{2}$	$\bar{R}Q \vee S\bar{R}\bar{Q} \vee SQ \vee SR$
$\frac{1}{2}01\frac{1}{2}\frac{1}{2}11\frac{1}{2}$	$\bar{R}Q \vee S\bar{R}\bar{Q} \vee SQ \vee SR \vee \bar{S}R\bar{R}\bar{Q}$
$0\frac{1}{2}1\frac{1}{2}\frac{1}{2}11\frac{1}{2}$	$\bar{R}Q \vee S\bar{R}\bar{Q} \vee SQ \vee SR \vee \bar{S}RQ\bar{Q}$
$\frac{1}{2}\frac{1}{2}1\frac{1}{2}\frac{1}{2}11\frac{1}{2}$	$\bar{R}Q \vee S\bar{R}\bar{Q} \vee SQ \vee SR \vee \bar{S}R\bar{R}\bar{Q} \vee \bar{S}RQ\bar{Q}$
$00\frac{1}{2}1\frac{1}{2}11\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{Q} \vee SQ \vee SR$
$\frac{1}{2}0\frac{1}{2}1\frac{1}{2}11\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{Q} \vee SQ \vee SR \vee \bar{S}R\bar{R}\bar{Q}$
$0\frac{1}{2}\frac{1}{2}1\frac{1}{2}11\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{Q} \vee SQ \vee SR \vee \bar{S}RQ\bar{Q}$
$\frac{1}{2}\frac{1}{2}\frac{1}{2}1\frac{1}{2}11\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{Q} \vee SQ \vee SR \vee \bar{S}R\bar{R}\bar{Q} \vee \bar{S}RQ\bar{Q}$
$0011\frac{1}{2}11\frac{1}{2}$	$\bar{R}Q \vee S\bar{Q} \vee SQ \vee SR$
$\frac{1}{2}011\frac{1}{2}11\frac{1}{2}$	$\bar{R}Q \vee S\bar{Q} \vee SQ \vee SR \vee \bar{S}R\bar{R}\bar{Q}$
$0\frac{1}{2}11\frac{1}{2}11\frac{1}{2}$	$\bar{R}Q \vee S\bar{Q} \vee SQ \vee SR \vee \bar{S}RQ\bar{Q}$
$\frac{1}{2}\frac{1}{2}11\frac{1}{2}11\frac{1}{2}$	$\bar{R}Q \vee S\bar{Q} \vee SQ \vee SR \vee \bar{S}R\bar{R}\bar{Q} \vee \bar{S}RQ\bar{Q}$
$00\frac{1}{2}\frac{1}{2}111\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{R} \vee SQ \vee SR$
$\frac{1}{2}0\frac{1}{2}\frac{1}{2}111\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{R} \vee SQ \vee SR \vee \bar{S}R\bar{R}\bar{Q}$
$0\frac{1}{2}\frac{1}{2}\frac{1}{2}111\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{R} \vee SQ \vee SR \vee \bar{S}RQ\bar{Q}$
$\frac{1}{2}\frac{1}{2}\frac{1}{2}\frac{1}{2}111\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{R} \vee SQ \vee SR \vee \bar{S}R\bar{R}\bar{Q} \vee \bar{S}RQ\bar{Q}$
$001\frac{1}{2}111\frac{1}{2}$	$\bar{R}Q \vee S\bar{R} \vee SQ \vee SR$
$\frac{1}{2}01\frac{1}{2}111\frac{1}{2}$	$\bar{R}Q \vee S\bar{R} \vee SQ \vee SR \vee \bar{S}R\bar{R}\bar{Q}$
$0\frac{1}{2}1\frac{1}{2}111\frac{1}{2}$	$\bar{R}Q \vee S\bar{R} \vee SQ \vee SR \vee \bar{S}RQ\bar{Q}$
$\frac{1}{2}\frac{1}{2}1\frac{1}{2}111\frac{1}{2}$	$\bar{R}Q \vee S\bar{R} \vee SQ \vee SR \vee \bar{S}R\bar{R}\bar{Q} \vee \bar{S}RQ\bar{Q}$
$00\frac{1}{2}1111\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{R} \vee S\bar{Q} \vee SQ \vee SR$
$\frac{1}{2}0\frac{1}{2}1111\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{R} \vee S\bar{Q} \vee SQ \vee SR \vee \bar{S}R\bar{R}\bar{Q}$
$0\frac{1}{2}\frac{1}{2}1111\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{R} \vee S\bar{Q} \vee SQ \vee SR \vee \bar{S}RQ\bar{Q}$
$\frac{1}{2}\frac{1}{2}\frac{1}{2}1111\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{R} \vee S\bar{Q} \vee SQ \vee SR \vee \bar{S}R\bar{R}\bar{Q} \vee \bar{S}RQ\bar{Q}$
$0011111\frac{1}{2}$	$\bar{R}Q \vee S\bar{R} \vee S\bar{Q} \vee SQ \vee SR$
$\frac{1}{2}011111\frac{1}{2}$	$\bar{R}Q \vee S\bar{R} \vee S\bar{Q} \vee SQ \vee SR \vee \bar{S}R\bar{R}\bar{Q}$
$0\frac{1}{2}11111\frac{1}{2}$	$\bar{R}Q \vee S\bar{R} \vee S\bar{Q} \vee SQ \vee SR \vee \bar{S}RQ\bar{Q}$
$\frac{1}{2}\frac{1}{2}11111\frac{1}{2}$	$\bar{R}Q \vee S\bar{R} \vee S\bar{Q} \vee SQ \vee SR \vee \bar{S}R\bar{R}\bar{Q} \vee \bar{S}RQ\bar{Q}$
$00\frac{1}{2}11111$	$\bar{S}\bar{R}Q \vee S$
$\frac{1}{2}0\frac{1}{2}11111$	$\bar{S}\bar{R}Q \vee S \vee \bar{S}R\bar{R}\bar{Q}$
$0\frac{1}{2}\frac{1}{2}11111$	$\bar{S}\bar{R}Q \vee S \vee \bar{S}RQ\bar{Q}$
$\frac{1}{2}\frac{1}{2}\frac{1}{2}11111$	$\bar{S}\bar{R}Q \vee S \vee \bar{S}R\bar{R}\bar{Q} \vee \bar{S}RQ\bar{Q}$
00111111	$\bar{R}Q \vee S$
$\frac{1}{2}0111111$	$\bar{R}Q \vee S \vee \bar{S}R\bar{R}\bar{Q}$
$0\frac{1}{2}111111$	$\bar{R}Q \vee S \vee \bar{S}RQ\bar{Q}$
$\frac{1}{2}\frac{1}{2}111111$	$\bar{R}Q \vee S \vee \bar{S}R\bar{R}\bar{Q} \vee \bar{S}RQ\bar{Q}$

All 136 logical forms of reset-type SR fuzzy flip-flop are shown in the followings table.

value of undefined points 1 2 3 4 5 6 7 8	logical form of $Q(t+1)$
$\frac{1}{2}\frac{1}{2}000000$	$\bar{S}\bar{R}Q \vee S\bar{R}\bar{Q} \vee S\bar{R}Q$
$1\frac{1}{2}000000$	$\bar{S}\bar{R}Q \vee S\bar{R}$
$\frac{1}{2}1000000$	$\bar{R}Q \vee S\bar{R}\bar{Q}$
11000000	$\bar{R}Q \vee S\bar{R}$
$\frac{1}{2}\frac{1}{2}\frac{1}{2}00000$	$\bar{S}\bar{R}Q \vee S\bar{R}\bar{Q} \vee S\bar{R}Q \vee \bar{S}R\bar{R}\bar{Q}$
$1\frac{1}{2}\frac{1}{2}00000$	$\bar{S}\bar{R}Q \vee S\bar{R} \vee \bar{S}R\bar{R}\bar{Q}$
$\frac{1}{2}1\frac{1}{2}00000$	$\bar{R}Q \vee S\bar{R}\bar{Q} \vee \bar{S}R\bar{R}\bar{Q}$
$11\frac{1}{2}00000$	$\bar{R}Q \vee S\bar{R} \vee \bar{S}R\bar{R}\bar{Q}$
$\frac{1}{2}\frac{1}{2}00000\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{R}\bar{Q} \vee S\bar{R}Q \vee S\bar{S}RQ\bar{Q}$
$1\frac{1}{2}00000\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{R} \vee S\bar{S}RQ\bar{Q}$
$\frac{1}{2}100000\frac{1}{2}$	$\bar{R}Q \vee S\bar{R}\bar{Q} \vee S\bar{S}RQ\bar{Q}$
$1100000\frac{1}{2}$	$\bar{R}Q \vee S\bar{R} \vee S\bar{S}RQ\bar{Q}$
$\frac{1}{2}\frac{1}{2}\frac{1}{2}0000\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{R}\bar{Q} \vee S\bar{R}Q \vee \bar{S}R\bar{R}\bar{Q} \vee S\bar{S}RQ\bar{Q}$
$1\frac{1}{2}\frac{1}{2}0000\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{R} \vee \bar{S}R\bar{R}\bar{Q} \vee S\bar{S}RQ\bar{Q}$
$\frac{1}{2}1\frac{1}{2}0000\frac{1}{2}$	$\bar{R}Q \vee S\bar{R}\bar{Q} \vee \bar{S}R\bar{R}\bar{Q} \vee S\bar{S}RQ\bar{Q}$
$11\frac{1}{2}0000\frac{1}{2}$	$\bar{R}Q \vee S\bar{R} \vee \bar{S}R\bar{R}\bar{Q} \vee S\bar{S}RQ\bar{Q}$
$\frac{1}{2}\frac{1}{2}0\frac{1}{2}000\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{R}\bar{Q} \vee S\bar{R}Q \vee S\bar{S}R\bar{Q}$
$1\frac{1}{2}0\frac{1}{2}000\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{R} \vee S\bar{S}R\bar{Q}$
$\frac{1}{2}10\frac{1}{2}000\frac{1}{2}$	$\bar{R}Q \vee S\bar{R}\bar{Q} \vee S\bar{S}R\bar{Q}$
$110\frac{1}{2}000\frac{1}{2}$	$\bar{R}Q \vee S\bar{R} \vee S\bar{S}R\bar{Q}$
$\frac{1}{2}\frac{1}{2}1\frac{1}{2}000\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{R}\bar{Q} \vee S\bar{R}Q \vee \bar{S}R\bar{R}\bar{Q} \vee S\bar{S}R\bar{Q}$
$1\frac{1}{2}\frac{1}{2}000\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{R} \vee \bar{S}R\bar{R}\bar{Q} \vee S\bar{S}R\bar{Q}$
$\frac{1}{2}1\frac{1}{2}000\frac{1}{2}$	$\bar{R}Q \vee S\bar{R}\bar{Q} \vee \bar{S}R\bar{R}\bar{Q} \vee S\bar{S}R\bar{Q}$
$11\frac{1}{2}000\frac{1}{2}$	$\bar{R}Q \vee S\bar{R} \vee \bar{S}R\bar{R}\bar{Q} \vee S\bar{S}R\bar{Q}$
$\frac{1}{2}\frac{1}{2}00\frac{1}{2}00\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{R}\bar{Q} \vee S\bar{R}Q \vee \bar{S}RQ\bar{Q}$
$1\frac{1}{2}00\frac{1}{2}00\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{R} \vee \bar{S}RQ\bar{Q}$
$\frac{1}{2}100\frac{1}{2}00\frac{1}{2}$	$\bar{R}Q \vee S\bar{R}\bar{Q} \vee \bar{S}RQ\bar{Q}$
$1100\frac{1}{2}00\frac{1}{2}$	$\bar{R}Q \vee S\bar{R} \vee \bar{S}RQ\bar{Q}$
$\frac{1}{2}\frac{1}{2}\frac{1}{2}0\frac{1}{2}00\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{R}\bar{Q} \vee S\bar{R}Q \vee \bar{S}R\bar{R}\bar{Q} \vee \bar{S}RQ\bar{Q}$
$1\frac{1}{2}\frac{1}{2}0\frac{1}{2}00\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{R} \vee \bar{S}R\bar{R}\bar{Q} \vee \bar{S}RQ\bar{Q}$
$\frac{1}{2}1\frac{1}{2}0\frac{1}{2}00\frac{1}{2}$	$\bar{R}Q \vee S\bar{R}\bar{Q} \vee \bar{S}R\bar{R}\bar{Q} \vee \bar{S}RQ\bar{Q}$
$11\frac{1}{2}0\frac{1}{2}00\frac{1}{2}$	$\bar{R}Q \vee S\bar{R} \vee \bar{S}R\bar{R}\bar{Q} \vee \bar{S}RQ\bar{Q}$
$\frac{1}{2}\frac{1}{2}0\frac{1}{2}\frac{1}{2}00\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{R}\bar{Q} \vee S\bar{R}Q \vee \bar{S}RQ\bar{Q} \vee S\bar{S}R\bar{Q}$
$1\frac{1}{2}0\frac{1}{2}\frac{1}{2}00\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{R} \vee \bar{S}RQ\bar{Q} \vee S\bar{S}R\bar{Q}$
$\frac{1}{2}10\frac{1}{2}\frac{1}{2}00\frac{1}{2}$	$\bar{R}Q \vee S\bar{R}\bar{Q} \vee \bar{S}RQ\bar{Q} \vee S\bar{S}R\bar{Q}$
$110\frac{1}{2}\frac{1}{2}00\frac{1}{2}$	$\bar{R}Q \vee S\bar{R} \vee \bar{S}RQ\bar{Q} \vee S\bar{S}R\bar{Q}$
$\frac{1}{2}\frac{1}{2}\frac{1}{2}\frac{1}{2}\frac{1}{2}00\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{R}\bar{Q} \vee S\bar{R}Q \vee \bar{S}R\bar{R}\bar{Q} \vee \bar{S}RQ\bar{Q} \vee S\bar{S}R\bar{Q}$
$1\frac{1}{2}\frac{1}{2}\frac{1}{2}\frac{1}{2}00\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{R} \vee \bar{S}R\bar{R}\bar{Q} \vee \bar{S}RQ\bar{Q} \vee S\bar{S}R\bar{Q}$
$\frac{1}{2}1\frac{1}{2}\frac{1}{2}\frac{1}{2}00\frac{1}{2}$	$\bar{R}Q \vee S\bar{R}\bar{Q} \vee \bar{S}R\bar{R}\bar{Q} \vee \bar{S}RQ\bar{Q} \vee S\bar{S}R\bar{Q}$
$11\frac{1}{2}\frac{1}{2}\frac{1}{2}00\frac{1}{2}$	$\bar{R}Q \vee S\bar{R} \vee \bar{S}R\bar{R}\bar{Q} \vee \bar{S}RQ\bar{Q} \vee S\bar{S}R\bar{Q}$
$\frac{1}{2}\frac{1}{2}000\frac{1}{2}0\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{R}\bar{Q} \vee S\bar{R}Q \vee SRQ\bar{Q}$
$1\frac{1}{2}000\frac{1}{2}0\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{R} \vee SRQ\bar{Q}$
$\frac{1}{2}1000\frac{1}{2}0\frac{1}{2}$	$\bar{R}Q \vee S\bar{R}\bar{Q} \vee SRQ\bar{Q}$
$11000\frac{1}{2}0\frac{1}{2}$	$\bar{R}Q \vee S\bar{R} \vee SRQ\bar{Q}$
$\frac{1}{2}\frac{1}{2}\frac{1}{2}00\frac{1}{2}0\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{R}\bar{Q} \vee S\bar{R}Q \vee \bar{S}R\bar{R}\bar{Q} \vee SRQ\bar{Q}$

$1\frac{1}{2}\frac{1}{2}00\frac{1}{2}0\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{R} \vee \bar{S}R\bar{R}\bar{Q} \vee SRQ\bar{Q}$
$\frac{1}{2}1\frac{1}{2}00\frac{1}{2}0\frac{1}{2}$	$\bar{R}Q \vee S\bar{R}\bar{Q} \vee \bar{S}R\bar{R}\bar{Q} \vee SRQ\bar{Q}$
$11\frac{1}{2}00\frac{1}{2}0\frac{1}{2}$	$\bar{R}Q \vee S\bar{R} \vee \bar{S}R\bar{R}\bar{Q} \vee SRQ\bar{Q}$
$\frac{1}{2}\frac{1}{2}0\frac{1}{2}0\frac{1}{2}0\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{R}\bar{Q} \vee S\bar{R}Q \vee S\bar{S}R\bar{Q} \vee SRQ\bar{Q}$
$1\frac{1}{2}0\frac{1}{2}0\frac{1}{2}0\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{R} \vee S\bar{S}R\bar{Q} \vee SRQ\bar{Q}$
$\frac{1}{2}10\frac{1}{2}0\frac{1}{2}0\frac{1}{2}$	$\bar{R}Q \vee S\bar{R}\bar{Q} \vee S\bar{S}R\bar{Q} \vee SRQ\bar{Q}$
$110\frac{1}{2}0\frac{1}{2}0\frac{1}{2}$	$\bar{R}Q \vee S\bar{R} \vee S\bar{S}R\bar{Q} \vee SRQ\bar{Q}$
$\frac{1}{2}\frac{1}{2}\frac{1}{2}0\frac{1}{2}0\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{R}\bar{Q} \vee S\bar{R}Q \vee \bar{S}R\bar{R}\bar{Q} \vee S\bar{S}R\bar{Q} \vee SRQ\bar{Q}$
$1\frac{1}{2}\frac{1}{2}0\frac{1}{2}0\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{R} \vee \bar{S}R\bar{R}\bar{Q} \vee S\bar{S}R\bar{Q} \vee SRQ\bar{Q}$
$\frac{1}{2}1\frac{1}{2}0\frac{1}{2}0\frac{1}{2}$	$\bar{R}Q \vee S\bar{R}\bar{Q} \vee \bar{S}R\bar{R}\bar{Q} \vee S\bar{S}R\bar{Q} \vee SRQ\bar{Q}$
$11\frac{1}{2}0\frac{1}{2}0\frac{1}{2}$	$\bar{R}Q \vee S\bar{R} \vee \bar{S}R\bar{R}\bar{Q} \vee S\bar{S}R\bar{Q} \vee SRQ\bar{Q}$
$\frac{1}{2}\frac{1}{2}00\frac{1}{2}0\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{R}\bar{Q} \vee S\bar{R}Q \vee \bar{S}RQ\bar{Q} \vee SRQ\bar{Q}$
$1\frac{1}{2}00\frac{1}{2}0\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{R} \vee \bar{S}RQ\bar{Q} \vee SRQ\bar{Q}$
$\frac{1}{2}100\frac{1}{2}0\frac{1}{2}$	$\bar{R}Q \vee S\bar{R}\bar{Q} \vee \bar{S}RQ\bar{Q} \vee SRQ\bar{Q}$
$1100\frac{1}{2}0\frac{1}{2}$	$\bar{R}Q \vee S\bar{R} \vee \bar{S}RQ\bar{Q} \vee SRQ\bar{Q}$
$\frac{1}{2}\frac{1}{2}\frac{1}{2}0\frac{1}{2}0\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{R}\bar{Q} \vee S\bar{R}Q \vee \bar{S}R\bar{R}\bar{Q} \vee \bar{S}RQ\bar{Q} \vee SRQ\bar{Q}$
$1\frac{1}{2}\frac{1}{2}0\frac{1}{2}0\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{R} \vee \bar{S}R\bar{R}\bar{Q} \vee \bar{S}RQ\bar{Q} \vee SRQ\bar{Q}$
$\frac{1}{2}1\frac{1}{2}0\frac{1}{2}0\frac{1}{2}$	$\bar{R}Q \vee S\bar{R}\bar{Q} \vee \bar{S}R\bar{R}\bar{Q} \vee \bar{S}RQ\bar{Q} \vee SRQ\bar{Q}$
$11\frac{1}{2}0\frac{1}{2}0\frac{1}{2}$	$\bar{R}Q \vee S\bar{R} \vee \bar{S}R\bar{R}\bar{Q} \vee \bar{S}RQ\bar{Q} \vee SRQ\bar{Q}$
$\frac{1}{2}\frac{1}{2}0\frac{1}{2}\frac{1}{2}0\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{R}\bar{Q} \vee S\bar{R}Q \vee \bar{S}RQ\bar{Q} \vee S\bar{S}R\bar{Q} \vee SRQ\bar{Q}$
$1\frac{1}{2}0\frac{1}{2}\frac{1}{2}0\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{R} \vee \bar{S}RQ\bar{Q} \vee S\bar{S}R\bar{Q} \vee SRQ\bar{Q}$
$\frac{1}{2}10\frac{1}{2}\frac{1}{2}0\frac{1}{2}$	$\bar{R}Q \vee S\bar{R}\bar{Q} \vee \bar{S}RQ\bar{Q} \vee S\bar{S}R\bar{Q} \vee SRQ\bar{Q}$
$110\frac{1}{2}\frac{1}{2}0\frac{1}{2}$	$\bar{R}Q \vee S\bar{R} \vee \bar{S}RQ\bar{Q} \vee S\bar{S}R\bar{Q} \vee SRQ\bar{Q}$
$\frac{1}{2}\frac{1}{2}\frac{1}{2}\frac{1}{2}0\frac{1}{2}0\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{R}\bar{Q} \vee S\bar{R}Q \vee \bar{S}R\bar{R}\bar{Q} \vee \bar{S}RQ\bar{Q} \vee S\bar{S}R\bar{Q} \vee SRQ\bar{Q}$
$1\frac{1}{2}\frac{1}{2}\frac{1}{2}0\frac{1}{2}0\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{R} \vee \bar{S}R\bar{R}\bar{Q} \vee \bar{S}RQ\bar{Q} \vee S\bar{S}R\bar{Q} \vee SRQ\bar{Q}$
$\frac{1}{2}1\frac{1}{2}\frac{1}{2}0\frac{1}{2}0\frac{1}{2}$	$\bar{R}Q \vee S\bar{R}\bar{Q} \vee \bar{S}R\bar{R}\bar{Q} \vee \bar{S}RQ\bar{Q} \vee S\bar{S}R\bar{Q} \vee SRQ\bar{Q}$
$11\frac{1}{2}\frac{1}{2}0\frac{1}{2}0\frac{1}{2}$	$\bar{R}Q \vee S\bar{R} \vee \bar{S}R\bar{R}\bar{Q} \vee \bar{S}RQ\bar{Q} \vee S\bar{S}R\bar{Q} \vee SRQ\bar{Q}$
$\frac{1}{2}\frac{1}{2}0000\frac{1}{2}\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{R}\bar{Q} \vee S\bar{R}Q \vee S\bar{S}RQ$
$1\frac{1}{2}0000\frac{1}{2}\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{R} \vee S\bar{S}RQ$
$\frac{1}{2}10000\frac{1}{2}\frac{1}{2}$	$\bar{R}Q \vee S\bar{R}\bar{Q} \vee S\bar{S}RQ$
$110000\frac{1}{2}\frac{1}{2}$	$\bar{R}Q \vee S\bar{R} \vee S\bar{S}RQ$
$\frac{1}{2}\frac{1}{2}\frac{1}{2}000\frac{1}{2}\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{R}\bar{Q} \vee S\bar{R}Q \vee \bar{S}R\bar{R}\bar{Q} \vee S\bar{S}RQ$
$1\frac{1}{2}\frac{1}{2}000\frac{1}{2}\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{R} \vee \bar{S}R\bar{R}\bar{Q} \vee S\bar{S}RQ$
$\frac{1}{2}1\frac{1}{2}000\frac{1}{2}\frac{1}{2}$	$\bar{R}Q \vee S\bar{R}\bar{Q} \vee \bar{S}R\bar{R}\bar{Q} \vee S\bar{S}RQ$
$11\frac{1}{2}000\frac{1}{2}\frac{1}{2}$	$\bar{R}Q \vee S\bar{R} \vee \bar{S}R\bar{R}\bar{Q} \vee S\bar{S}RQ$
$\frac{1}{2}\frac{1}{2}0\frac{1}{2}00\frac{1}{2}\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{R}\bar{Q} \vee S\bar{R}Q \vee S\bar{S}R\bar{Q} \vee S\bar{S}RQ$
$1\frac{1}{2}0\frac{1}{2}00\frac{1}{2}\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{R} \vee S\bar{S}R\bar{Q} \vee S\bar{S}RQ$
$\frac{1}{2}10\frac{1}{2}00\frac{1}{2}\frac{1}{2}$	$\bar{R}Q \vee S\bar{R}\bar{Q} \vee S\bar{S}R\bar{Q} \vee S\bar{S}RQ$
$110\frac{1}{2}00\frac{1}{2}\frac{1}{2}$	$\bar{R}Q \vee S\bar{R} \vee S\bar{S}R\bar{Q} \vee S\bar{S}RQ$
$\frac{1}{2}\frac{1}{2}\frac{1}{2}\frac{1}{2}00\frac{1}{2}\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{R}\bar{Q} \vee S\bar{R}Q \vee \bar{S}R\bar{R}\bar{Q} \vee S\bar{S}R\bar{Q} \vee S\bar{S}RQ$
$1\frac{1}{2}\frac{1}{2}\frac{1}{2}00\frac{1}{2}\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{R} \vee \bar{S}R\bar{R}\bar{Q} \vee S\bar{S}R\bar{Q} \vee S\bar{S}RQ$
$\frac{1}{2}1\frac{1}{2}\frac{1}{2}00\frac{1}{2}\frac{1}{2}$	$\bar{R}Q \vee S\bar{R}\bar{Q} \vee \bar{S}R\bar{R}\bar{Q} \vee S\bar{S}R\bar{Q} \vee S\bar{S}RQ$
$11\frac{1}{2}\frac{1}{2}00\frac{1}{2}\frac{1}{2}$	$\bar{R}Q \vee S\bar{R} \vee \bar{S}R\bar{R}\bar{Q} \vee S\bar{S}R\bar{Q} \vee S\bar{S}RQ$
$\frac{1}{2}\frac{1}{2}00\frac{1}{2}0\frac{1}{2}\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{R}\bar{Q} \vee S\bar{R}Q \vee \bar{S}RQ\bar{Q} \vee S\bar{S}RQ$
$1\frac{1}{2}00\frac{1}{2}0\frac{1}{2}\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{R} \vee \bar{S}RQ\bar{Q} \vee S\bar{S}RQ$
$\frac{1}{2}100\frac{1}{2}0\frac{1}{2}\frac{1}{2}$	$\bar{R}Q \vee S\bar{R}\bar{Q} \vee \bar{S}RQ\bar{Q} \vee S\bar{S}RQ$

$1100\frac{1}{2}0\frac{1}{2}\frac{1}{2}$	$\bar{R}Q \vee S\bar{R} \vee \bar{S}RQ\bar{Q} \vee S\bar{S}RQ$
$\frac{1}{2}\frac{1}{2}\frac{1}{2}0\frac{1}{2}0\frac{1}{2}\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{R}\bar{Q} \vee S\bar{R}Q \vee \bar{S}R\bar{R}\bar{Q} \vee \bar{S}RQ\bar{Q} \vee S\bar{S}RQ$
$1\frac{1}{2}\frac{1}{2}0\frac{1}{2}0\frac{1}{2}\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{R} \vee \bar{S}R\bar{R}\bar{Q} \vee \bar{S}RQ\bar{Q} \vee S\bar{S}RQ$
$\frac{1}{2}1\frac{1}{2}0\frac{1}{2}0\frac{1}{2}\frac{1}{2}$	$\bar{R}Q \vee S\bar{R}\bar{Q} \vee \bar{S}R\bar{R}\bar{Q} \vee \bar{S}RQ\bar{Q} \vee S\bar{S}RQ$
$11\frac{1}{2}0\frac{1}{2}0\frac{1}{2}\frac{1}{2}$	$\bar{R}Q \vee S\bar{R} \vee \bar{S}R\bar{R}\bar{Q} \vee \bar{S}RQ\bar{Q} \vee S\bar{S}RQ$
$\frac{1}{2}\frac{1}{2}0\frac{1}{2}0\frac{1}{2}\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{R}\bar{Q} \vee S\bar{R}Q \vee \bar{S}RQ\bar{Q} \vee S\bar{S}R\bar{Q} \vee S\bar{S}RQ$
$1\frac{1}{2}0\frac{1}{2}\frac{1}{2}0\frac{1}{2}\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{R} \vee \bar{S}RQ\bar{Q} \vee S\bar{S}R\bar{Q} \vee S\bar{S}RQ$
$\frac{1}{2}10\frac{1}{2}\frac{1}{2}0\frac{1}{2}\frac{1}{2}$	$\bar{R}Q \vee S\bar{R}\bar{Q} \vee \bar{S}RQ\bar{Q} \vee S\bar{S}R\bar{Q} \vee S\bar{S}RQ$
$110\frac{1}{2}\frac{1}{2}0\frac{1}{2}\frac{1}{2}$	$\bar{R}Q \vee S\bar{R} \vee \bar{S}RQ\bar{Q} \vee S\bar{S}R\bar{Q} \vee S\bar{S}RQ$
$\frac{1}{2}\frac{1}{2}\frac{1}{2}\frac{1}{2}0\frac{1}{2}\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{R}\bar{Q} \vee S\bar{R}Q \vee \bar{S}R\bar{R}\bar{Q} \vee \bar{S}RQ\bar{Q} \vee S\bar{S}R\bar{Q} \vee S\bar{S}RQ$
$1\frac{1}{2}\frac{1}{2}\frac{1}{2}0\frac{1}{2}\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{R} \vee \bar{S}R\bar{R}\bar{Q} \vee \bar{S}RQ\bar{Q} \vee S\bar{S}R\bar{Q} \vee S\bar{S}RQ$
$\frac{1}{2}1\frac{1}{2}\frac{1}{2}0\frac{1}{2}\frac{1}{2}$	$\bar{R}Q \vee S\bar{R}\bar{Q} \vee \bar{S}R\bar{R}\bar{Q} \vee \bar{S}RQ\bar{Q} \vee S\bar{S}R\bar{Q} \vee S\bar{S}RQ$
$11\frac{1}{2}\frac{1}{2}0\frac{1}{2}\frac{1}{2}$	$\bar{R}Q \vee S\bar{R} \vee \bar{S}R\bar{R}\bar{Q} \vee \bar{S}RQ\bar{Q} \vee S\bar{S}R\bar{Q} \vee S\bar{S}RQ$
$\frac{1}{2}\frac{1}{2}000\frac{1}{2}\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{R}\bar{Q} \vee S\bar{R}Q \vee S\bar{S}RQ \vee SRQ\bar{Q}$
$1\frac{1}{2}000\frac{1}{2}\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{R} \vee S\bar{S}RQ \vee SRQ\bar{Q}$
$\frac{1}{2}1000\frac{1}{2}\frac{1}{2}$	$\bar{R}Q \vee S\bar{R}\bar{Q} \vee S\bar{S}RQ \vee SRQ\bar{Q}$
$11000\frac{1}{2}\frac{1}{2}$	$\bar{R}Q \vee S\bar{R} \vee S\bar{S}RQ \vee SRQ\bar{Q}$
$\frac{1}{2}\frac{1}{2}\frac{1}{2}00\frac{1}{2}\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{R}\bar{Q} \vee S\bar{R}Q \vee \bar{S}R\bar{R}\bar{Q} \vee S\bar{S}RQ \vee SRQ\bar{Q}$
$1\frac{1}{2}\frac{1}{2}00\frac{1}{2}\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{R} \vee \bar{S}R\bar{R}\bar{Q} \vee S\bar{S}RQ \vee SRQ\bar{Q}$
$\frac{1}{2}1\frac{1}{2}00\frac{1}{2}\frac{1}{2}$	$\bar{R}Q \vee S\bar{R}\bar{Q} \vee \bar{S}R\bar{R}\bar{Q} \vee S\bar{S}RQ \vee SRQ\bar{Q}$
$11\frac{1}{2}00\frac{1}{2}\frac{1}{2}$	$\bar{R}Q \vee S\bar{R} \vee \bar{S}R\bar{R}\bar{Q} \vee S\bar{S}RQ \vee SRQ\bar{Q}$
$\frac{1}{2}\frac{1}{2}0\frac{1}{2}0\frac{1}{2}\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{R}\bar{Q} \vee S\bar{R}Q \vee S\bar{S}R\bar{Q} \vee S\bar{S}RQ \vee SRQ\bar{Q}$
$1\frac{1}{2}0\frac{1}{2}0\frac{1}{2}\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{R} \vee S\bar{S}R\bar{Q} \vee S\bar{S}RQ \vee SRQ\bar{Q}$
$\frac{1}{2}10\frac{1}{2}0\frac{1}{2}\frac{1}{2}$	$\bar{R}Q \vee S\bar{R}\bar{Q} \vee S\bar{S}R\bar{Q} \vee S\bar{S}RQ \vee SRQ\bar{Q}$
$110\frac{1}{2}0\frac{1}{2}\frac{1}{2}$	$\bar{R}Q \vee S\bar{R} \vee S\bar{S}R\bar{Q} \vee S\bar{S}RQ \vee SRQ\bar{Q}$
$\frac{1}{2}\frac{1}{2}\frac{1}{2}\frac{1}{2}0\frac{1}{2}\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{R}\bar{Q} \vee S\bar{R}Q \vee \bar{S}R\bar{R}\bar{Q} \vee S\bar{S}R\bar{Q} \vee S\bar{S}RQ \vee SRQ\bar{Q}$
$1\frac{1}{2}\frac{1}{2}\frac{1}{2}0\frac{1}{2}\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{R} \vee \bar{S}R\bar{R}\bar{Q} \vee S\bar{S}R\bar{Q} \vee S\bar{S}RQ \vee SRQ\bar{Q}$
$\frac{1}{2}1\frac{1}{2}\frac{1}{2}0\frac{1}{2}\frac{1}{2}$	$\bar{R}Q \vee S\bar{R}\bar{Q} \vee \bar{S}R\bar{R}\bar{Q} \vee S\bar{S}R\bar{Q} \vee S\bar{S}RQ \vee SRQ\bar{Q}$
$11\frac{1}{2}\frac{1}{2}0\frac{1}{2}\frac{1}{2}$	$\bar{R}Q \vee S\bar{R} \vee \bar{S}R\bar{R}\bar{Q} \vee S\bar{S}R\bar{Q} \vee S\bar{S}RQ \vee SRQ\bar{Q}$
$\frac{1}{2}\frac{1}{2}00\frac{1}{2}\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{R}\bar{Q} \vee S\bar{R}Q \vee S\bar{S}RQ \vee S\bar{S}R\bar{Q} \vee S\bar{S}RQ \vee SRQ\bar{Q}$
$1\frac{1}{2}00\frac{1}{2}\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{R} \vee S\bar{S}RQ \vee S\bar{S}R\bar{Q} \vee S\bar{S}RQ \vee SRQ\bar{Q}$
$\frac{1}{2}100\frac{1}{2}\frac{1}{2}$	$\bar{R}Q \vee S\bar{R}\bar{Q} \vee \bar{S}RQ\bar{Q} \vee S\bar{S}RQ \vee SRQ\bar{Q}$
$1100\frac{1}{2}\frac{1}{2}$	$\bar{R}Q \vee S\bar{R} \vee \bar{S}RQ\bar{Q} \vee S\bar{S}RQ \vee SRQ\bar{Q}$
$\frac{1}{2}\frac{1}{2}\frac{1}{2}0\frac{1}{2}\frac{1}{2}\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{R}\bar{Q} \vee S\bar{R}Q \vee \bar{S}R\bar{R}\bar{Q} \vee \bar{S}RQ\bar{Q} \vee S\bar{S}RQ \vee SRQ\bar{Q}$
$1\frac{1}{2}\frac{1}{2}0\frac{1}{2}\frac{1}{2}\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{R} \vee \bar{S}R\bar{R}\bar{Q} \vee \bar{S}RQ\bar{Q} \vee S\bar{S}RQ \vee SRQ\bar{Q}$
$\frac{1}{2}1\frac{1}{2}0\frac{1}{2}\frac{1}{2}\frac{1}{2}$	$\bar{R}Q \vee S\bar{R}\bar{Q} \vee \bar{S}R\bar{R}\bar{Q} \vee \bar{S}RQ\bar{Q} \vee S\bar{S}RQ \vee SRQ\bar{Q}$
$11\frac{1}{2}0\frac{1}{2}\frac{1}{2}\frac{1}{2}$	$\bar{R}Q \vee S\bar{R} \vee \bar{S}R\bar{R}\bar{Q} \vee \bar{S}RQ\bar{Q} \vee S\bar{S}RQ \vee SRQ\bar{Q}$
$\frac{1}{2}\frac{1}{2}0\frac{1}{2}\frac{1}{2}\frac{1}{2}\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{R}\bar{Q} \vee S\bar{R}Q \vee \bar{S}RQ\bar{Q} \vee S\bar{S}R\bar{Q} \vee S\bar{S}RQ \vee SRQ\bar{Q}$
$1\frac{1}{2}0\frac{1}{2}\frac{1}{2}\frac{1}{2}\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{R} \vee \bar{S}RQ\bar{Q} \vee S\bar{S}R\bar{Q} \vee S\bar{S}RQ \vee SRQ\bar{Q}$
$\frac{1}{2}10\frac{1}{2}\frac{1}{2}\frac{1}{2}\frac{1}{2}$	$\bar{R}Q \vee S\bar{R}\bar{Q} \vee \bar{S}RQ\bar{Q} \vee S\bar{S}R\bar{Q} \vee S\bar{S}RQ \vee SRQ\bar{Q}$
$110\frac{1}{2}\frac{1}{2}\frac{1}{2}\frac{1}{2}$	$\bar{R}Q \vee S\bar{R} \vee \bar{S}RQ\bar{Q} \vee S\bar{S}R\bar{Q} \vee S\bar{S}RQ \vee SRQ\bar{Q}$
$\frac{1}{2}\frac{1}{2}\frac{1}{2}\frac{1}{2}\frac{1}{2}\frac{1}{2}\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{R}\bar{Q} \vee S\bar{R}Q \vee \bar{S}R\bar{R}\bar{Q} \vee \bar{S}RQ\bar{Q} \vee S\bar{S}R\bar{Q} \vee S\bar{S}RQ \vee SRQ\bar{Q}$
$1\frac{1}{2}\frac{1}{2}\frac{1}{2}\frac{1}{2}\frac{1}{2}\frac{1}{2}\frac{1}{2}$	$\bar{S}\bar{R}Q \vee S\bar{R} \vee \bar{S}R\bar{R}\bar{Q} \vee \bar{S}RQ\bar{Q} \vee S\bar{S}R\bar{Q} \vee S\bar{S}RQ \vee SRQ\bar{Q}$
$\frac{1}{2}1\frac{1}{2}\frac{1}{2}\frac{1}{2}\frac{1}{2}\frac{1}{2}\frac{1}{2}$	$\bar{R}Q \vee S\bar{R}\bar{Q} \vee \bar{S}R\bar{R}\bar{Q} \vee \bar{S}RQ\bar{Q} \vee S\bar{S}R\bar{Q} \vee S\bar{S}RQ \vee SRQ\bar{Q}$
$11\frac{1}{2}\frac{1}{2}\frac{1}{2}\frac{1}{2}\frac{1}{2}\frac{1}{2}$	$\bar{R}Q \vee S\bar{R} \vee \bar{S}R\bar{R}\bar{Q} \vee \bar{S}RQ\bar{Q} \vee S\bar{S}R\bar{Q} \vee S\bar{S}RQ \vee SRQ\bar{Q}$

3.6 Lattice structure of flip-flops

As described in the preceding section, logical forms of all fuzzy flip-flops constitute a distributive lattice both in partial order of ambiguity and in partial order of values. More generally, the following theorem can be derived.

Theorem 3.3 At every point $\boldsymbol{x}$ in the B-ternary truth table of the fuzzy extension of a binary logical function using max-min logic $(1-, \wedge, \vee)$, the value of the function $f(\boldsymbol{x})$ can be defined as unique value or one of 2 values.

Proof Suppose $f(\boldsymbol{x})$ can take any value of $\{0, 1/2, 1\}$ at $\boldsymbol{x} \in \{0, 1/2, 1\}^n$, $\boldsymbol{x}$ must not be a binary vector $\{0,1\}^n$ ($\because \boldsymbol{x} \in \{0,1\}^n \Rightarrow f(\boldsymbol{x}) \in \{0,1\}$). Then, there exist some binary vectors $\boldsymbol{x}' \in \{0,1\}^n$ s.t. $\boldsymbol{x} \overset{a}{\succeq} \boldsymbol{x}'$. At such a point $\boldsymbol{x}'$, $f(\boldsymbol{x}')$ takes 0 or 1 uniquely. Since $\boldsymbol{x} \overset{a}{\succeq} \boldsymbol{x}' \Rightarrow f(\boldsymbol{x}) \overset{a}{\succeq} f(\boldsymbol{x}')$, the value of $f(\boldsymbol{x})$ takes one of the following three cases. $f(\boldsymbol{x})$ takes one of $\{0, 1/2\}$, if $f(\boldsymbol{x}')$ takes 0 at all binary $\boldsymbol{x}'$. $f(\boldsymbol{x})$ takes one of $\{1/2, 1\}$, if $f(\boldsymbol{x}')$ takes 1 at all binary $\boldsymbol{x}'$. If there exist both $f(\boldsymbol{x}')$ which takes 0 and $f(\boldsymbol{x}')$ which takes 1, $f(\boldsymbol{x})$ takes $1/2$ uniquely. □

Fuzzy logical forms as extensions of a binary logical form constitute a partially ordered set when the partial order is $\overset{a}{\succeq}$ or $\overset{v}{\succeq}$. The structure is essentially defined by the points whose value is not defined uniquely. Let n be a number of these points, the partially ordered structure is order-isomorphic to that of a subset V of n-dimensional binary vectors $\boldsymbol{v}$. But there may exist a combination of the values that it can not be a B-ternary logical function, V may not be a Boolean lattice of 2^n order—e.g. SR fuzzy flip-flops. However, in the cases of D, T, and SR fuzzy flip-flops, fuzzy extensions of a binary logical function using max-min logic $(1-, \wedge, \vee)$ constitute a distributive lattice under the partial order $\overset{a}{\succeq}$.

Theorem 3.4 Let S be the set of 136 set-type SR fuzzy flip-flops. Any $\boldsymbol{s} \in S$ can be represented as a 8-dimensional ternary vector $(s_1, s_2, \cdots, s_8)$ of undefined points ①, $\cdots$, ⑧, where $s_1, s_2 \in \{0, 1/2\}$, $s_3, s_4, \cdots, s_8 \in \{1/2, 1\}$. Then $(S, \overset{a}{\succeq})$ and $(S, \overset{v}{\succeq})$ are dual order-isomorphic.

Proof Let ϕ be as a following map.

$$\begin{array}{rccc} \phi: & \{0, \frac{1}{2}\} & \longrightarrow & \{0, \frac{1}{2}\} \\ & \cup & & \cup \\ & 0 & \longmapsto & \phi(0) = \frac{1}{2} \\ & \frac{1}{2} & \longmapsto & \phi(\frac{1}{2}) = 0 \end{array}$$

Let Φ be a map $\Phi(S) = \{\phi(s_1), \phi(s_2), s_3, s_4, \cdots, s_8\}$. Because the values of s_1 and s_2 can be selected independently from other values, the image of Φ is S, i.e., $\Phi : S \longrightarrow S$. Clearly, Φ is a bijective.

For any $\boldsymbol{a}, \boldsymbol{b} \in S$, if $\boldsymbol{a} \overset{a}{\succeq} \boldsymbol{b}$, then $a_i \overset{a}{\succeq} b_i \ \ (i = 1, 2, \cdots, 8)$. This means $a_i \overset{v}{\succeq} b_i$ for $i = 1, 2$. And then $\phi(b_i) \overset{v}{\succeq} \phi(a_i)$. For $i = 3, 4, \cdots, 8$, $a_i \overset{a}{\succeq} b_i$ is equivalent to $b_i \overset{v}{\succeq} a_i$. Therefore $\Phi(\boldsymbol{b}) = (\phi(b_1), \phi(b_2), b_3, b_4, \cdots, b_8) \overset{v}{\succeq} (\phi(a_1), \phi(a_2), a_3, a_4, \cdots, a_8) = \Phi(\boldsymbol{a})$.

Hence Φ is a dual order-isomorphism from $(S, \overset{a}{\succeq})$ to $(S, \overset{v}{\succeq})$. □

For example, the minimum set-type SR fuzzy flip-flop under the order of ambiguity $(0, 0, 1, 1, 1, 1, 1, 1)$ is mapped to $(1/2, 1/2, 1, 1, 1, 1, 1, 1)$, which is the maximum one under the order of values. The maximum set-type SR fuzzy flip-flop under the order of ambiguity $(1/2, 1/2, 1/2, 1/2, 1/2, 1/2, 1/2, 1/2)$ is mapped to $(0, 0, 1/2, 1/2, 1/2, 1/2, 1/2, 1/2)$ which the minimum one under the order of values.

Theorem 3.5 Let R be the set of 136 reset-type SR fuzzy flip-flops. Any $\boldsymbol{r} \in R$ is represented as a 8-dimensional ternary vector $(r_1, r_2, \cdots, r_8)$ of undefined points ①, $\cdots$, ⑧, where $r_1, r_2 \in \{1/2, 1\}$, $r_3, r_4, \cdots, r_8 \in \{0, 1/2\}$. Then $(R, \overset{a}{\succeq})$ and $(R, \overset{v}{\succeq})$ are dual order-isomorphic.

Proof Let ψ be as a following map.

$$\begin{array}{rccc} \psi: & \{\frac{1}{2}, 1\} & \longrightarrow & \{\frac{1}{2}, 1\} \\ & \cup & & \cup \\ & \frac{1}{2} & \longmapsto & \psi(\frac{1}{2}) = 1 \\ & 1 & \longmapsto & \psi(1) = \frac{1}{2} \end{array}$$

Let Ψ be a map $\Psi(R) = \{\psi(r_1), \psi(r_2), r_3, r_4, \cdots, r_8\}$. Because the values of r_1 and r_2 can be selected independently from other values, the image of Ψ is R, i.e., $\Psi : R \longrightarrow R$. Clearly, Ψ is a bijective.

For any $\boldsymbol{a}, \boldsymbol{b} \in R$, if $\boldsymbol{a} \overset{a}{\succeq} \boldsymbol{b}$, then $a_i \overset{a}{\succeq} b_i$ $(i = 1, 2, \cdots, 8)$. This means $b_i \overset{v}{\succeq} a_i$ for $i = 1, 2$. And then $\psi(a_i) \overset{v}{\succeq} \psi(b_i)$. For $i = 3, 4, \cdots, 8$, $a_i \overset{a}{\succeq} b_i$ is equivalent to $a_i \overset{v}{\succeq} b_i$. Hence $\Psi(\boldsymbol{a}) = (\psi(a_1), \psi(a_2), a_3, a_4, \cdots, a_8) \overset{v}{\succeq} (\psi(b_1), \psi(b_2), b_3, b_4, \cdots, b_8) = \Psi(\boldsymbol{b})$.

Ψ is a order isomorphism from $(R, \overset{a}{\succeq})$ to $(R, \overset{v}{\succeq})$. □

Corollary 3.6 Let $\boldsymbol{f}_1$ and $\boldsymbol{f}_2$ be fuzzy extensions of a binary logical function $\boldsymbol{f}$ of D, T, SR flip-flops, then maximum $\boldsymbol{f}_{\max} = \boldsymbol{f}_1 \vee \boldsymbol{f}_2$ and minimum $\boldsymbol{f}_{\min} = \boldsymbol{f}_1 \wedge \boldsymbol{f}_2$ are also fuzzy extension of $\boldsymbol{f}$ under both $\overset{a}{\succeq}$ and $\overset{v}{\succeq}$.

For example, in 1989, Hirota and Ozawa proposed the unified logical form of JK fuzzy flip-flop, i.e., when $J(t) \geq K(t)$, the logical form of the characteristic function is the maxterm expression, when $J(t) \leq K(t)$, the minterm expression. Such a composition is always valid as a fuzzy extension of the original function.

$$Q(t+1) = \begin{cases} (J \vee Q) \wedge (K^{⓪} \vee Q^{⓪}) & (J \geq K) \\ (J \wedge Q^{⓪}) \vee (K^{⓪} \wedge Q) & (J \leq K) \end{cases}$$

From this theorem, such a composition is always valid as a fuzzy logical function.

In the case of D, T, and JK fuzzy flip-flop, the partially ordered relations of their fuzzy logical forms are Boolean lattices of 4, 1, and 64 elements, respectively. The reason of this is that the values of their logical functions are defined independently. And the binary vectors that represent the structure of partially ordered relation always valid as representations of logical forms.

All elements of a Boolean lattice have a unique complement. This means that all logical forms of D, T, and JK fuzzy flip-flops have a "unique complement" as a logical form. Characteristics of binary maxterm and minterm logical forms can be obtained from every logical form by doing maximum and minimum operations with their complement, respectively. Moreover, since a Boolean lattice is also relatively complemented, any characteristics as a fuzzy extension of a binary logical function can be obtained from any another fuzzy extended logical forms by doing maximum or minimum operation.

3.7 conclusion

The characteristics of D, T, and SR fuzzy flip-flop are logically analyzed when the fuzzy logical operation system $(\cdot^{\textcircled{n}}, \textcircled{t}, \textcircled{s})$ is max-min logical operation system $(1-\cdot, \wedge, \vee)$. Using the theory of B-ternary logic, fuzzy logical characteristics of the D, T, and SR fuzzy flip-flops are represented in B-ternary truth table, and fuzzy logical forms of all their characteristic functions are proposed. Using 2 kinds of partially ordered relation, it is shown that their structures of the partially ordered sets are distributive lattices, in particular, they are Boolean lattices in the case of D and T fuzzy flip-flops.

From this result, it is proved that the maximum or minimum operations between the different logical functions provide logical forms of valid logical functions. For example, Hirota and Ozawa's composition of set type and reset type JK fuzzy flip-flops produces a new types of JK fuzzy flip-flop.

Chapter 4

Fuzzy memory elements

4.1 Introduction

In this chapter, 2 types of fuzzy memory elements are proposed. Fuzzy flip-flops, which have already been proposed in preceding chapter, are also considered as fuzzy memory elements. In fact, flip-flops are widely used as memory elements in binary logic. They can expressed by logical forms, and then, their characteristics can be computed numerically and shown graphically. In particular, they can be derived analytically under the max-min logical operation system. Some mathematical properties are also derived and they gives the foundation of fuzzy sequential system design methodology. However, in order to apply fuzzy flip-flops to fuzzy application existing in the real world, it has still the redundancy of the circuit resources.

Since binary flip-flops are widely used as a memory element in conventional binary computers, fuzzy flip-flops have been proposed as a fuzzy memory element. In binary flip-flops, 4 types—D, T, SR, and JK type—of flip-flops are available. As a memory element, SR flip-flop and JK flip-flop can be used. After their circuit implementation using some transistors (multi vibrator) are proposed, they are logically expressed as boolean logical forms for their logical analysis. Unfortunately, these kinds of logical forms have not been proposed so far from the viewpoint of memory elements, conventional fuzzy flip-flops are not optimized for realizing memory elements. Hence, when they are extended to fuzzy

logic, the corresponding fuzzy flip-flops expressed by the logical forms are not optimized for a fuzzy memory element. In binary logic, a memory element (1 bit memory) is realized by 4 or 6 transistors, and the optimization as the memory elements is not so important. In fuzzy logic, however, the circuit scale of the memory element is larger (50 or 500 transistors) than that of binary logic, and the optimized fuzzy memory element is needed.

In this chapter, the functions required for applying to fuzzy applications are proposed. The main application of fuzzy logic is Mamdani inference, which is widely used, in particular, in the control area. Based on the fuzzy operations that is needed for Mamdani inference, the functions for operating on the membership memory are implemented on a memory element. The behavior model of the fuzzy memory element is described by VHDL (Very high speed integrated circuit Hardware Description Language), while their electronic circuit model are designed and simulated by a circuit simulator and a circuit synthesizer on a work station. For the circuit synthesis, the FPGA (Field Programmable Gate Array), which is widely used for the trial design of a LSI, libraries are used for the target architecture. The circuit areas, the delay times (processing speed), and their functions of them are compared with conventional D, T, SR, and JK fuzzy flip-flops. Moreover, proposed fuzzy memory elements are compared with the KAFA[15][16], a general parallel fuzzy processor for the Mamdani inference. They are also compared with Ozawa's JK fuzzy flip-flops in terms of a fuzzy membership register, and are compared with Virant's T fuzzy memory cells from a viewpoint of a fuzzy temporal inference. In all cases, the circuit performance of proposed fuzzy memory elements are higher than all of them, and cardinality of fuzzy membership functions can be increased to 10 or 30 times of these of them.

4.2 Fuzzy memory element model

In this section, the functions required for a fuzzy memory are discussed. In binary logic, the following three functions are needed for a memory element[9].

- Input set data and reset data, i.e. memorize 0 and 1 at any point of time
- Hold a memory data for any length of time
- Output a memory data at any point of time

In multiple-valued logic, these three functions are realized for not only 0 and 1, but also for any multiple-valued value as a data to input, output, and memorize. As a fuzzy logical memory is one of the multiple-valued logical memory, a fuzzy memory element needs to realize these functions. In addition to these functions for a multiple-valued logical memory, a fuzzy memory element has to operate fuzzy functions which are suitable for fuzzy information processing.

Mamdani inference is a fuzzy processing which is widely used for real world applications, particularly in control area. In Mamdani inference, minimum and maximum operations are used. In general, minimum and maximum operations are most important and fundamental operations in fuzzy logic and are often used in various scene. First, these operations must be implemented in a fuzzy memory element. From this reason, the most fundamental fuzzy memory element is proposed as a figure 54. $I \in [0,1]$, $Q \in [0,1]$, $C \in \{0,1,2,3\}$ indicate a fuzzy input value, a fuzzy memory and output value, and a control value, respectively. A control value C selects a behavior of a fuzzy memory element. When $C = 0$, the memory holds the current memory value, $C = 1$, a fuzzy value is inputted as a memory, $C = 2$, a minimum operation between a input and a memory is performed and the result is stored, $C = 3$, a maximum operation between a input and a memory is performed and the result is stored.

As for the other types of fuzzy inference, product-sum inference[13] and simple inference[13] are known. In these inference, algebraic product and sum (or algebraic sum) are used as

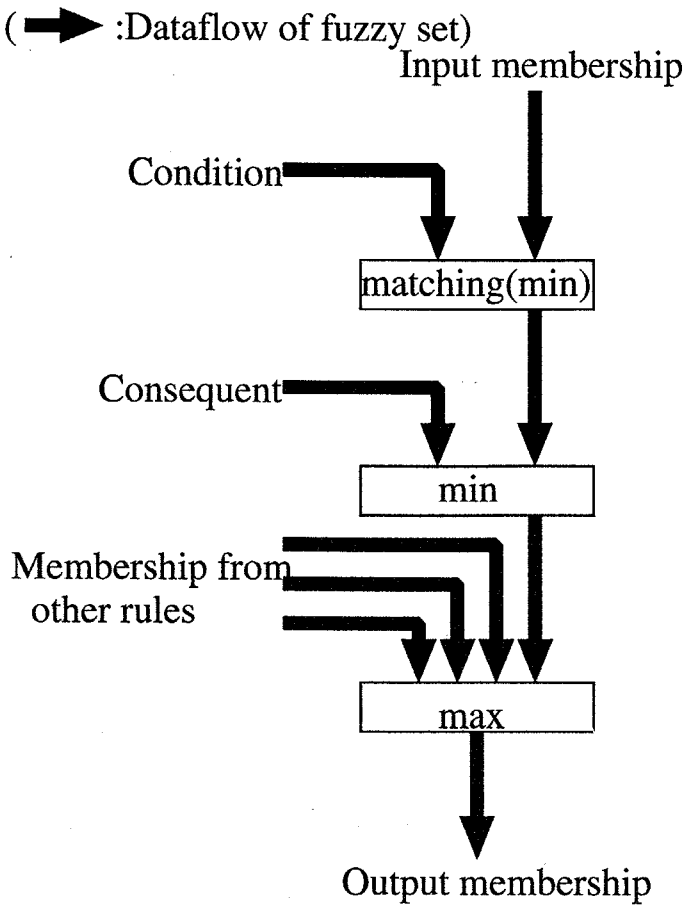


Figure 53: Dataflow of Mamdani fuzzy inference

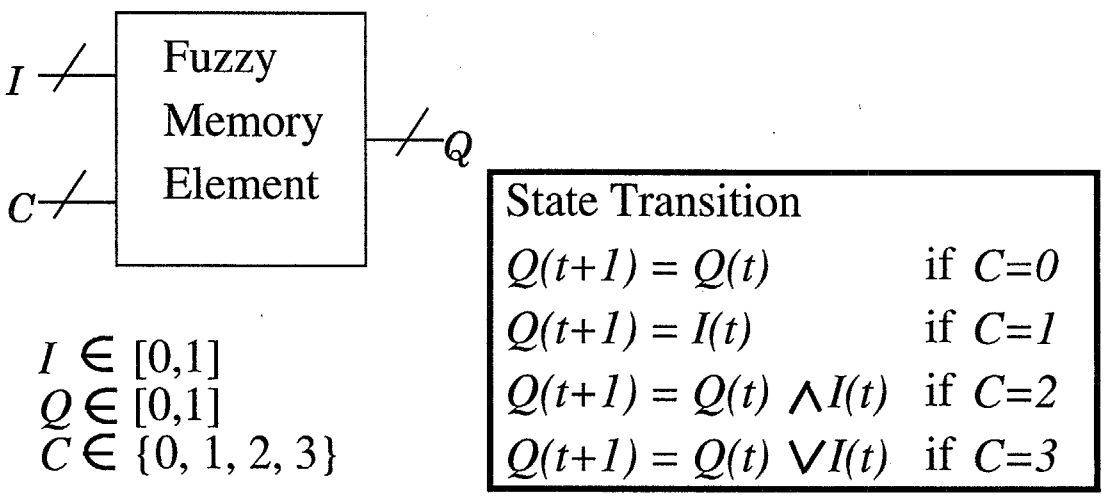


Figure 54: Max-Min type fuzzy memory element

t-norm and s-norm, respectively. In order to implement the algebraic product and algebraic sum to circuits, the circuit areas have to be more than 5 times larger and the delay time is more than 5 times longer than those of minimum and maximum circuits. Using multipliers leads to such results, and including multipliers in memories is not realistic.

Bounded product and bounded sum are also occasionally used as t-norm and s-norm, respectively. Bounded product and bounded sum are the operations used in classical multiple-valued logic—Lukasiewicz logic, and they are valuable in terms of not only a practical viewpoint but also a theoretical viewpoint. Their implementations to the circuits are not difficult, because comparators and full adders, which are needed by bounded operations, are simple circuits. Moreover, for the application areas other than fuzzy inference—e.g. fuzzy expert system or knowledge base—, fuzzy negation is required. Fuzzy negation is realized by inverters (1 bit NOT circuit) and incrementers (a variation of adders), which are able to be simply implemented. Therefore, including these operations in memories is meaningful.

Based on the above discussion, the bounded-type fuzzy memory element is shown in figure 55 that is an extension of figure 54. As for the control signal C, new signal $C = 4, 5, 6$ are added for three new operations—fuzzy negation, bounded product, and bounded sum.

4.3 Circuit design

2 types of fuzzy memory element, which are discussed in the preceding section, are implemented to circuits. The behavioral model of their circuits are described using VHDL, while they are synthesized to real circuits using synthesis tool on a computer. Target architecture of the synthesis is a FPGA device, which is widely used for a experimental circuit design. Input and output fuzzy value $[0, 1]$ are expressed in 8 bit discrete value, 0 corresponds to "00000000"$_{(2)}$, 1 to "10000000"$_{(2)}$. It is noted that although the values larger than "10000000"$_{(2)}$ do not appear in the input and the output, they may appear

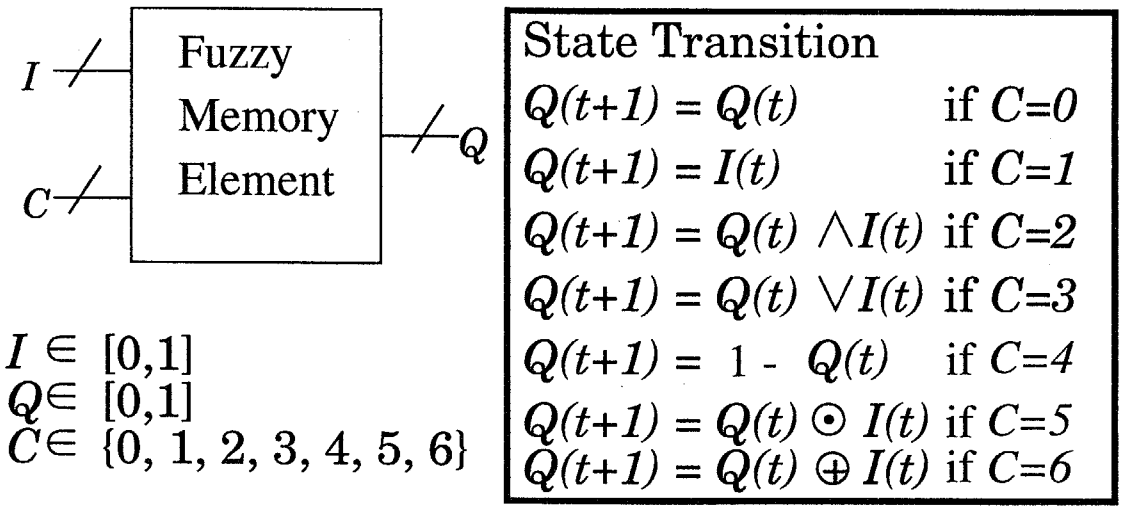


Figure 55: Bounded type fuzzy memory element

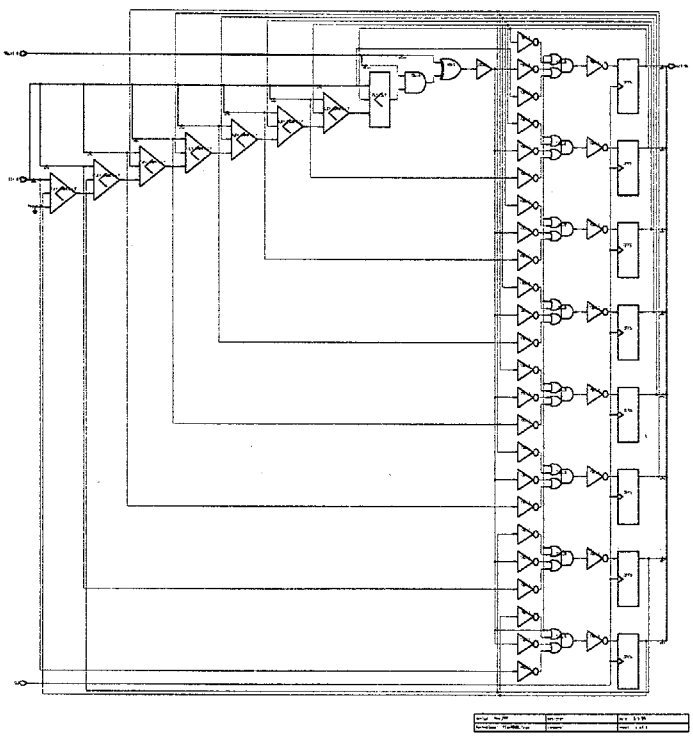


Figure 56: Circuit of max-min type fuzzy memory element

temporarily in the process.

Figure 56 shows the circuit of the max-min type fuzzy memory element. Figure 57 shows the circuit of the bounded type fuzzy memory element.

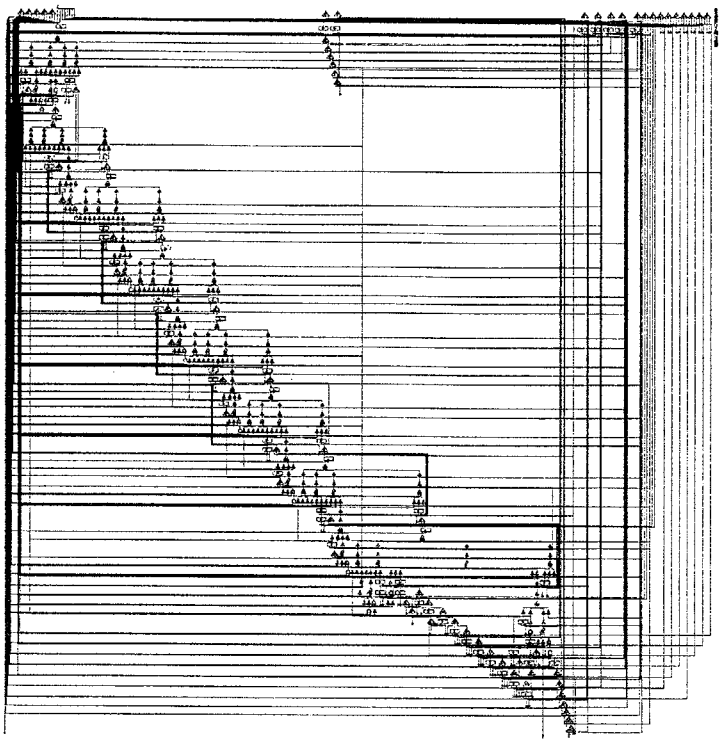


Figure 57: Circuit of bounded type fuzzy memory element

4.4 Discussion in terms of circuit areas and delay times

4.4.1 Comparison with fuzzy flip-flops

The circuit areas and the delay times of the circuits of the fuzzy memory elements designed in the preceding section are compared with those of the conventional fuzzy flip-flops. Concerning the max-min type fuzzy memory element and fuzzy flip-flops (realized by max-min fuzzy logic), figure 58 and figure 59 show the comparison of circuit areas and delay times, respectively. Concerning the bounded type fuzzy memory element and SR and JK fuzzy flip-flops (realized by max-min and bounded fuzzy logic), figure 60 and figure 61 show the comparison of circuit areas and delay times, respectively.

From the figure 58 and figure 59, the max-min type fuzzy memory element uses smaller circuit area and has faster delay time than those of any other fuzzy flip-flops except the D

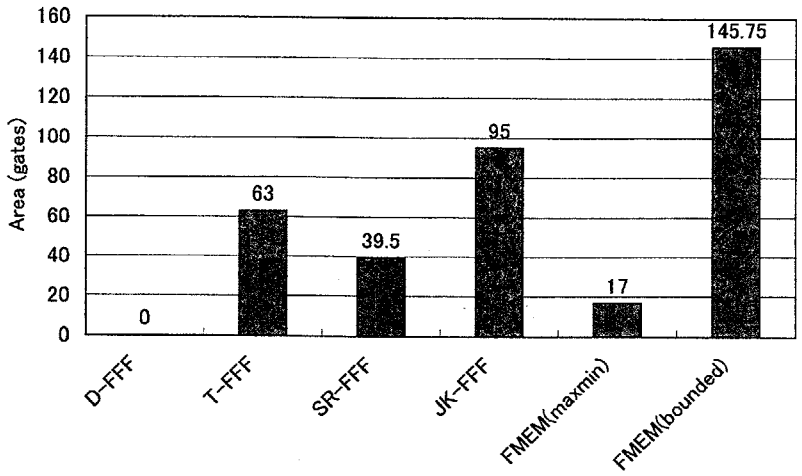


Figure 58: Circuit areas of the max-min type fuzzy memory element and max-min fuzzy flip-flops

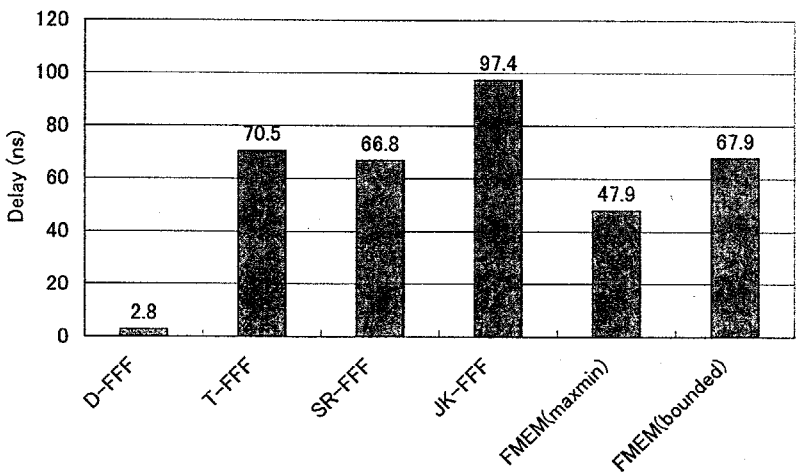


Figure 59: Delay times of the max-min type fuzzy memory element and max-min fuzzy flip-flops

fuzzy flip-flop, which is just a latch. The delay time of the bounded-type fuzzy memory element is almost equal to that of max-min SR fuzzy flip-flop and its circuit area is 1.5 or

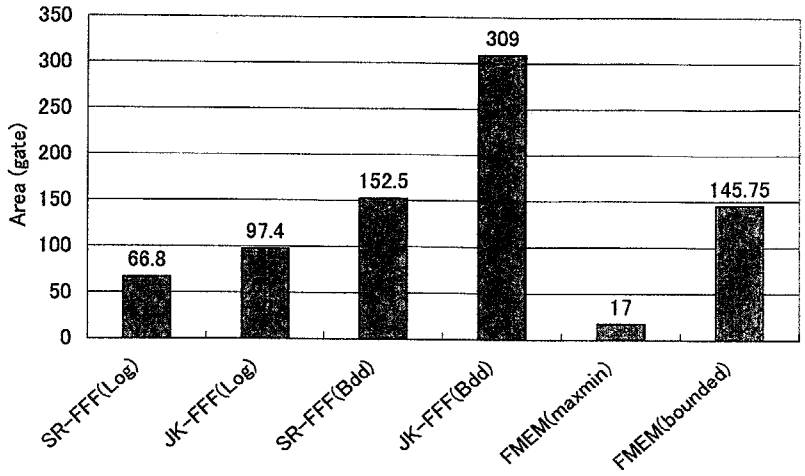


Figure 60: Circuit areas of the bounded type fuzzy memory element and fuzzy flip-flops

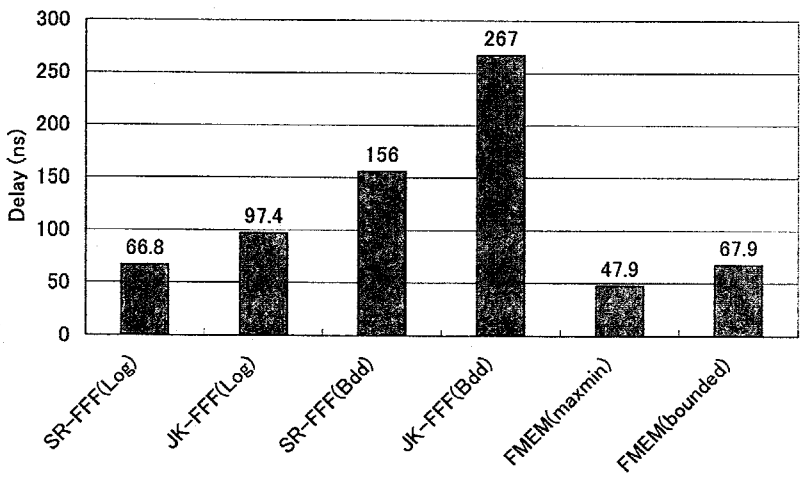


Figure 61: Delay times of the bounded type fuzzy memory element and fuzzy flip-flops

2 times of that of conventional max-min type fuzzy flip-flops. Compared with bounded fuzzy flip-flops, the circuit area of the bounded fuzzy memory element is almost equal to that of bounded SR fuzzy flip-flop and is a half of that of JK fuzzy flip-flop. Its delay time is a half of SR's and 1/3 of JK's.

Also the functions realized by fuzzy memory elements and fuzzy flip-flops are compared in the table 2. To input any value and to hold the memory for any length of time are required as a minimum memory element. D fuzzy flip-flop does not satisfy the hold function and T fuzzy flip-flop does not satisfy the input function. Therefore, they can not be used for a fuzzy memory element. Although SR fuzzy flip-flop satisfies the minimum functions for a memory element, and it can be used for a memory element, it does not include any other functions, i.e., fuzzy operations, which is only a multiple-valued logical memory element. JK fuzzy flip-flop is also used as a memory element and it also includes the fuzzy negation as an additional fuzzy logical function. Max-min type fuzzy memory element has minimum memory functions, and minimum and maximum operations for fuzzy logical operations. Bounded type fuzzy memory element has the functions of bounded product, bounded sum, and fuzzy negation in addition to the functions of the max-min type fuzzy memory element.

Including the minimum and maximum operations in the memory element is the advantage, because these operations often occur for all elements in the fuzzy memberships in fuzzy information processing, e.g., Mamdani inference. Compared with performing these operations on the elements of a fuzzy subsets piece by piece sequentially, it is clear that the operation speed of the proposed approach is much faster. From another viewpoint, it can be viewed as a variation of SIMD (Single Instruction stream Multiple Data stream) parallel processing architecture.

Since the bounded type fuzzy memory element includes the fuzzy negation, bounded product, and bounded sum, it can be applied to fuzzy application area more widely, e.g. fuzzy database, and fuzzy expert system.

4.4.2 Comparison with Ozawa's JK fuzzy flip-flop with respect to the fuzzy membership memory

Fuzzy membership memory (also called as "fuzzy register" in [11]) has been proposed using JK fuzzy flip-flops[11]. Its fundamental diagram is shown in figure 62. Because a JK fuzzy

Table 2: Functions of fuzzy memory elements and fuzzy flip-flops

	Input	Hold	Min	Max	negation	Bdd pro	Bdd sum
D-FFF	o	×	×	×	×	×	×
T-FFF	×	o	×	×	×	×	×
SR-FFF	o	o	×	×	×	×	×
JK-FFF	o	o	×	×	o	×	×
Maxmin FMEM	o	o	o	o	×	×	×
Bdd FMEM	o	o	o	o	o	o	o

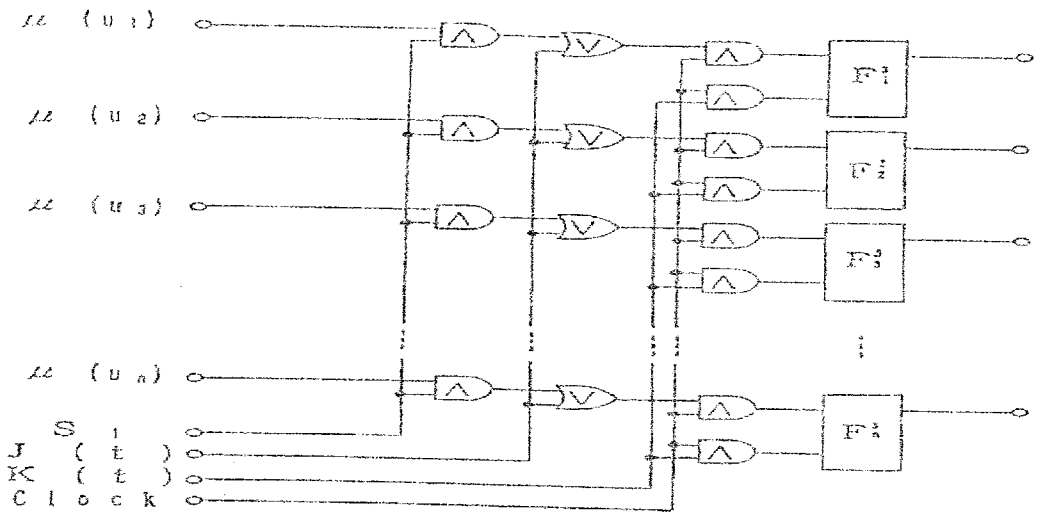


Figure 62: Diagram of a Ozawa's fuzzy register (Ozawa 1989[11])

flip-flop can represent a fuzzy value, the fuzzy membership memory is constituted by n JK fuzzy flip-flops, where n indicates the cardinal number of the universe of discourse of the support set. It can set and reset arbitrary shaped fuzzy membership function. Also it can perform fuzzy (e.g. maximum and minimum) composition.

Compared with the case of using JK fuzzy flip-flops, max-min type fuzzy memory element occupies 18% circuit area of JK's. On the occasion of constructing a fuzzy membership memory on a same LSI chip, the number of elements of fuzzy sets can be increased to 5 times as many as the case of JK fuzzy flip-flops. For example, when a

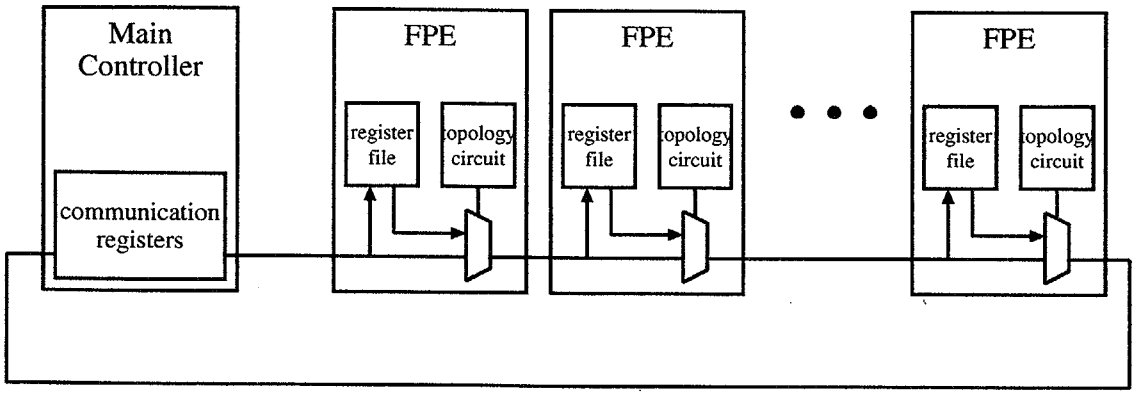


Figure 63: The architecture of KAFA (Kim 1997[16])

10000-gate-chip is used to realize the fuzzy membership memory, the maximum number of the elements of fuzzy membership functions is 588 using max-min type fuzzy memory elements, while that is 104 using JK fuzzy flip-flops.

4.4.3 Comparison with KAFA with respect to the SIMD parallel general fuzzy processor

As a general fuzzy processor, KAFA(KAist Fuzzy Accelerator) has been proposed[15][16]. KAFA is composed of a main controller and 128 fuzzy processing elements, and it is connected with a host computer. The main controller accepts some instruction from the host computer, controls all fuzzy processing elements parallelly. A fuzzy processing element has some 8bit-registers, a fuzzy arithmetic logical unit, and some 8bit-memories. KAFA can memorize some membership functions and perform the fuzzy logical operation between them concurrently. In this viewpoint, KAFA can be considered as a fuzzy membership memory with a fuzzy logical operators.

The KAFA architecture is shown in Figure 63

KAFA is designed as a general fuzzy information processor, and it has a large ability. For example, KAFA also has the ability to perform some types of defuzzifications, e.g., the center of gravity method and the highest grade method. It can perform a fuzzy inference like other fuzzy controllers only by itself. From this reason, a fuzzy processing element

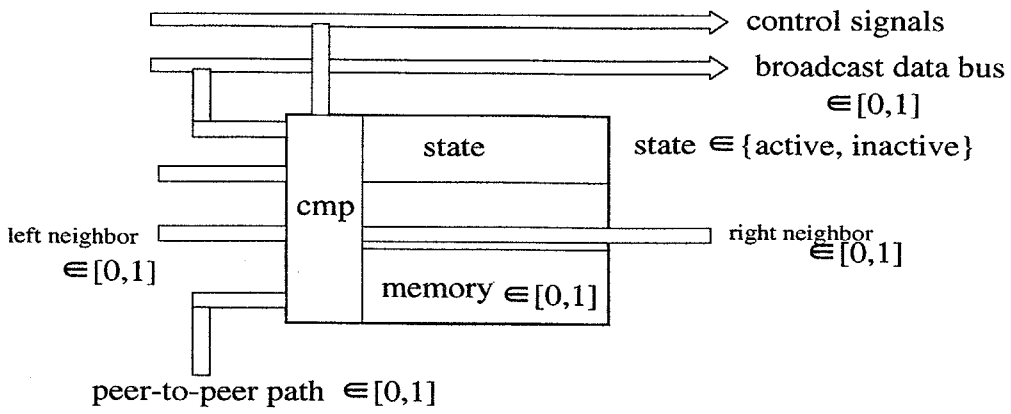


Figure 64: The block diagram of modified fuzzy memory element

becomes large and complicated. In fact, a fuzzy processing element has the same ability as an 8bit micro-processor. One fuzzy processing element uses 3000 gates of its area (using XC3804 device).

In order to compare with KAFA, some ports and buffers are added to proposed max-min type fuzzy memory element. Its block diagram is shown in Figure 64 and the ports are indicated in Figure 65. Its state transition is shown in Figure 66. Its circuit design is shown in Figure 67. From the result of the circuit synthesis, its circuit area is 103.5 gates and the minimum delay time is 20.8ns.

Modified max-min type fuzzy memory elements are placed as Figure 68 to memorize the fuzzy membership functions. The fuzzy membership matching for Mamdani inference can be performed like in Figure 69, and Mamdani inference can be performed like in Figure 70.

If the fuzzy processing elements are replaced to max-min type fuzzy memory elements, the circuit area is reduced to 3.4% of that of KAFA. The number of elements of a fuzzy

Control(Ctrl) $\in$ {input, output, hold, operation}

Operation(Op) $\in$ {min, max}

Input Select (IS) $\in$ {peer-to-peer, broadcast,
left neighbor, right neighbor}

Output Select(OS) $\in$ {peer-to-peer, broadcast,
left neighbor, right neighbor}

State Control (SC) $\in$ {all, only active, only inactive}

Figure 65: The ports of modified fuzzy memory element

if SC='all'
or (SC='only active' and state='active')
or (SC='only inactive' and state='inactive')
then

1. mem(t+1) $\leftarrow$ input(t) (Ctrl = input)
   mem(t+1) $\leftarrow$ mem(t) (Ctrl = output, hold)
   mem(t+1) $\leftarrow$ input(t) $\wedge$ mem(t) (Ctrl = operation, Op=min)
   (if mem(t+1) = mem(t) then state $\leftarrow$ active)
   mem(t+1) $\leftarrow$ input(t) $\vee$ mem(t) (Ctrl = operation, Op=max)
   (if mem(t+1) = mem(t) then state $\leftarrow$ active)
   The input is selected by IS
2. output(t+1) $\leftarrow$ mem(t) (Ctrl = output)
   output(t+1) $\leftarrow$ output(t) (Ctrl : otherwise)

Figure 66: State transitions of modified fuzzy memory element

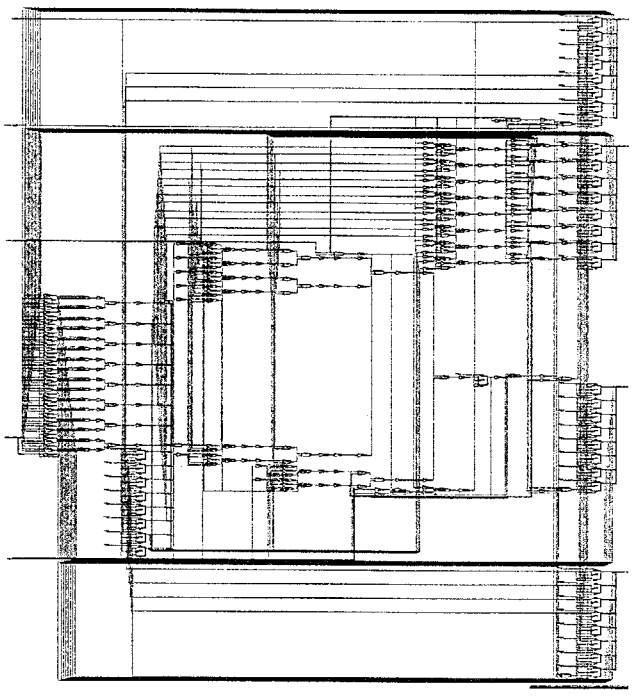


Figure 67: Circuit design of modified fuzzy memory element

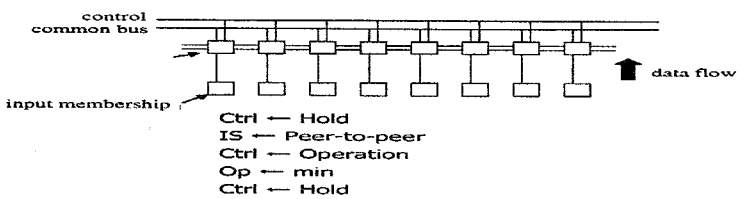


Figure 68: Fuzzy membership memory using modified fuzzy memory elements

membership function can be increased to 30 times or more of KAFA's. Therefore, when only the simple fuzzy operations, e.g., Mamdani inference or max-min operation between membership functions, are performed, KAFA's fuzzy processing elements can be replaced to the proposed fuzzy memory elements, and cardinality of membership functions can be increased to 30 times of KAFA's or more.

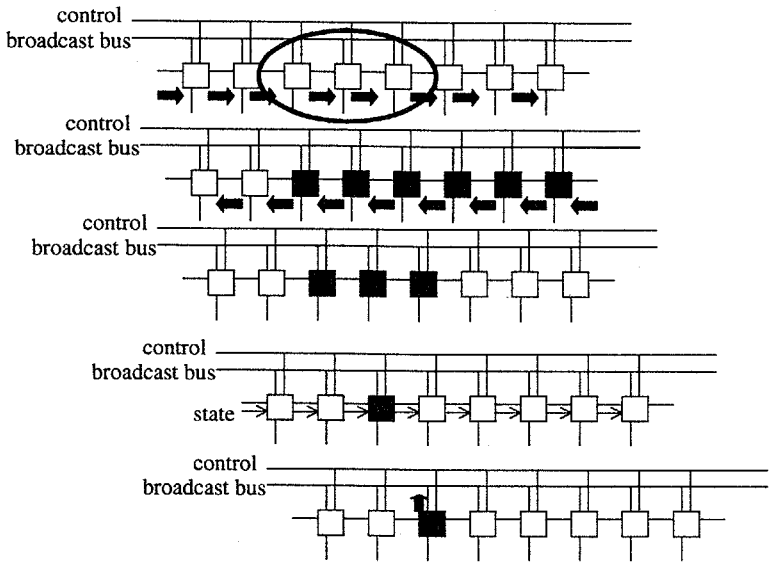


Figure 69: Fuzzy membership matching procedure using modified fuzzy memory elements

4.4.4 Comparison with Virant's T fuzzy memory cell with respect to the temporal fuzzy inference

In 1999, some applications of T fuzzy flip-flop (also called T fuzzy memory cell) were proposed[30]. From the problem of T fuzzy flip-flop, some types of modified T fuzzy flip-flops were proposed in [30]. Using the max-min logical operation system, T fuzzy flip-flop cannot input and memorize any new value when it takes 1/2 as a value of $Q(t)$. Therefore, in [30], "Set" and "Reset" functions were attached by adding new input ports, and were called "FTU cell" and "FTD cell", respectively (Figure 71, 72).

Using these T fuzzy flip-flops, applications to fuzzy temporal inference were proposed. The architecture is shown in Figure 73.

In [30], however, only the functions and roles were discussed, and circuit implementation was out of the discussion. For these applications, T fuzzy flip-flops (T fuzzy memory cells) can also be replaced to proposed fuzzy memory elements. And the circuit area

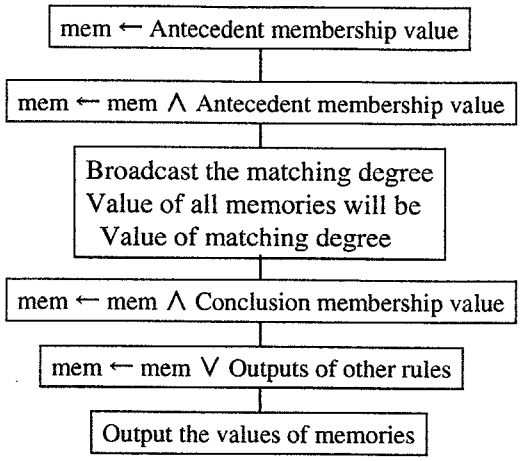


Figure 70: Mamdani inference procedure using modified fuzzy memory elements

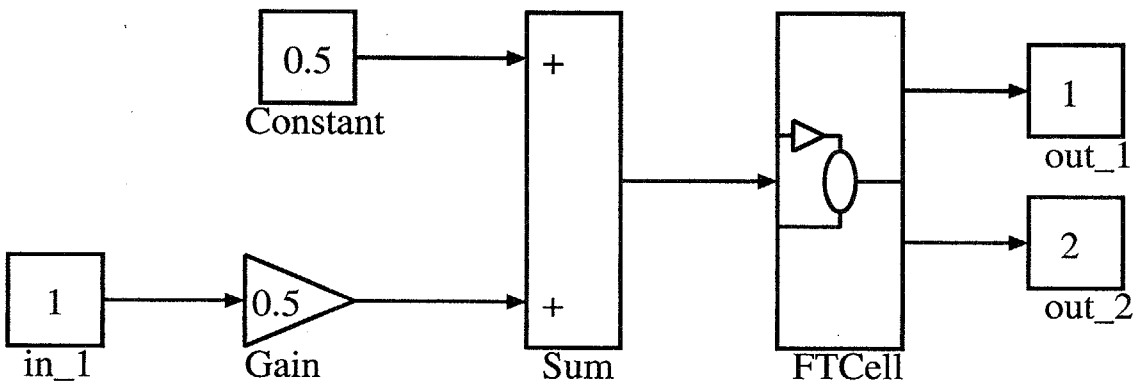


Figure 71: The block diagram of FTU cell (Virant 1999 [30])

of each cells can be reduced to 27% and delay time can be reduced to 68% of T fuzzy memory cells proposed in [30].

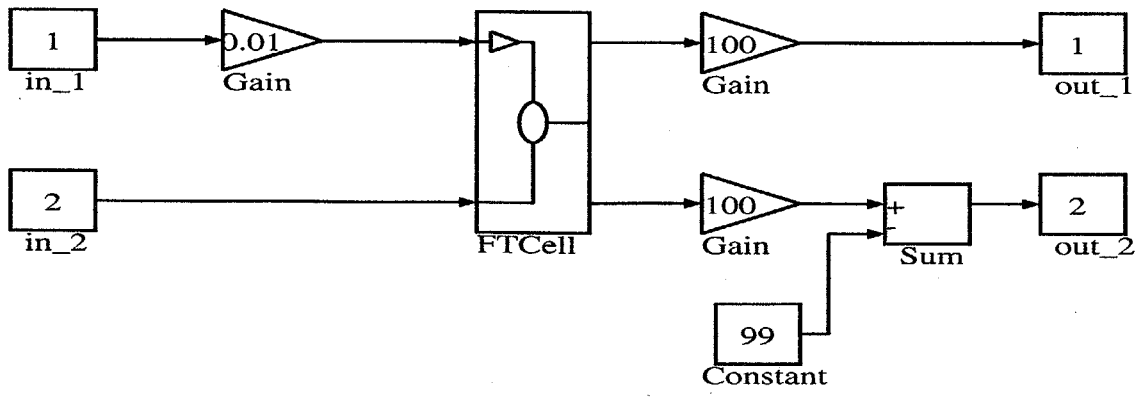


Figure 72: The block diagram of FTD cell (Virant 1999 [30])w

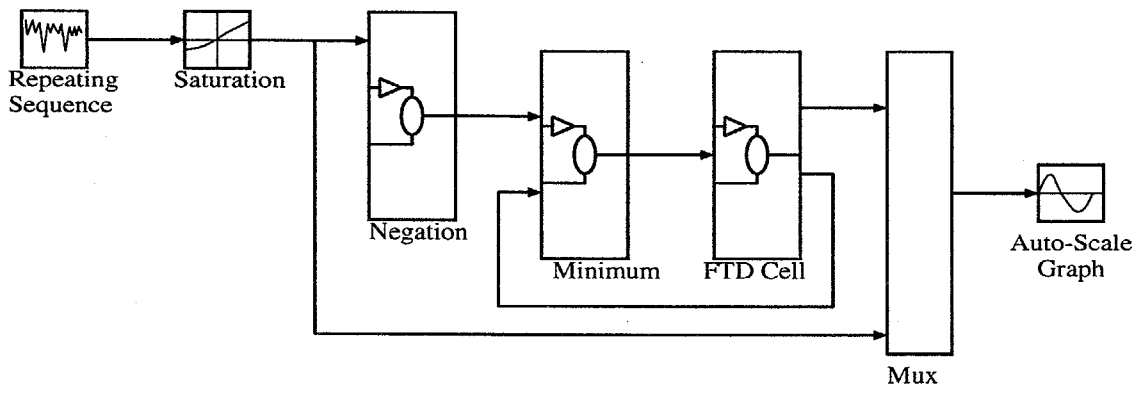


Figure 73: The architecture of Virant's fuzzy temporal inference (Virant 1999 [30])

4.5 Conclusion

In this chapter, 2 type of fuzzy memory elements suitable for fuzzy inference are proposed. These fuzzy memory elements are able to memorize any fuzzy logical values $[0, 1]$ and able to operate fuzzy logical operations between a input value and the current value of a memory. Max-min type fuzzy memory element is able to operate minimum and maximum fuzzy logical operation. In addition to them, bounded type fuzzy memory element is able to operate fuzzy negation, bounded product, and bounded sum. Their behavioral model are described by VHDL, and their circuit are designed using a circuit design and synthesis tool. For the library of the target architecture of the circuit synthesis, FPGA library is used. The circuit areas and the delay times of these fuzzy memory elements and fuzzy

flip-flops are compared. From these results, max-min type fuzzy memory element uses a half of the circuit area of SR and JK fuzzy flip-flops (realized by minimum and maximum operations), which can be used as a memory element. And its delay time is 2/3 of that of SR and JK fuzzy flip-flops. Bounded type fuzzy memory element uses 1.5 or 2 times of the circuit area of JK fuzzy flip-flop (max-min type) and uses 1/2 of that of JK fuzzy flip-flop (realized by bounded operations). It is almost equal to the circuit area of SR fuzzy flip-flop realized by bounded operations, while its delay time is almost equal to that of SR fuzzy flip-flop realized by max-min operations and is 1/2 or 1/3 of SR and JK fuzzy flip-flops realized by bounded operations.

Fuzzy memory elements are realized in smaller circuit areas and have faster processing speed than the fuzzy flip-flops. Furthermore, additional fuzzy operations are also implemented. In fuzzy information processing, fuzzy logical operation between membership functions are often used. Since fuzzy memory elements support fuzzy functions, it makes processors' loads light by processing fuzzy logical operation between membership functions parallelly. It makes total system performances high compared with using conventional memories and fuzzy inference processors.

Chapter 5

Conclusions

In this chapter, the research on fuzzy memory elements in this dissertation is concluded. After summarizing the content of this dissertation, the conclusion of this dissertation is drawn from the viewpoints of the foundation of fuzzy sequential circuit, the fuzzy logic theory, and the parallel fuzzy hardware architecture. The future prospects of the research on fuzzy memories and fuzzy hardwares are discussed at the end of this chapter.

5.1 Summary

In this dissertation, at first, D, T, and SR fuzzy flip-flops were proposed and their characteristics were clarified in four—max-min, algebraic, bounded, drastic—fuzzy logical operation systems. Their circuits for the four operation systems were designed using VHDL and circuit simulator/synthesizer on a workstation, and were compared with each other in terms of the circuit area and the delay times.

Next, the details of the logical property of the D, T, and SR fuzzy flip-flops were analyzed using max-min logical operation system $(1 - \cdot, \wedge, \vee)$. All their characteristics that are possibly realized in the fuzzy logic $(1 - \cdot, \wedge, \vee)$ as extensions of the form in the binary logic are shown, and the corresponding logical forms are derived completely. The number of fuzzy extended logical forms of D, T, and SR flip-flops are 4, 1, and 136 respectively. In the case of SR flip-flops, 2 types of logical characteristics exist in binary

logic regarding the treatment of "Don't care", which are "set preferred type" and "reset preferred type". In both case, there are 136 fuzzy logical forms for each type. In all cases of fuzzy flip-flops, their logical forms construct distributed lattices both in the partial order by fuzzy values and in the partial order by ambiguity. In particular, the lattices constructed by the forms of D and T fuzzy flip-flops are boolean lattice as well as that of JK fuzzy flip-flop.

2 types of fuzzy memory elements were proposed from the viewpoint of the functions required for memory elements in order to apply them to the fuzzy membership memories. Fuzzy memory elements can input and output any fuzzy value at any point of time, while holding their memory value for any length of time. In addition to the functions required for memory elements, fuzzy logical operations between fuzzy input and fuzzy memory can be operated. From this reason, membership memories using these memory elements can perform fuzzy set operations (e.g. maximum and minimum) between input fuzzy set and fuzzy set in the memory fast and easily. In most fuzzy applications—e.g. Mamdani fuzzy inference and fuzzy set matching, these fuzzy set operations occur frequently, whereas conventional fuzzy processors and memories cannot do them efficiently and flexibly.

5.2 Concluding remarks

Totally, 5 types of fuzzy memory elements were proposed in this dissertation, which are D, T, SR fuzzy flip-flops, max-min type fuzzy memory element, and bounded type fuzzy memory elements. These memory elements can be regarded as a kind of fuzzy sequential circuits. For the use of general purposes—e.g. a memory—, the sequential circuits must be controllable, in other words, their state diagrams must be strongly connected. The irredundant form of D fuzzy flip-flop is not a state machine because it does not have the term including $Q(t)$ in its right-hand side. All forms of T fuzzy flip-flop are not controllable because they cannot set any input value except $1/2$ when their $Q(t) = 1/2$. Therefore D and T fuzzy flip-flops cannot be used for the fuzzy memory elements.

D, T, and SR fuzzy flip-flops can be represented by logical form, and then they can be analyzed logically in terms of the max-min fuzzy logic(Kleenean Algebra). As opposed to fuzzy flip-flops, max-min type and bounded type fuzzy memory elements cannot be represented by fuzzy logical form, but are represented as state transition tables. This fact leads to that it is difficult to analyze them logically. However, their circuits are small (1/2 of SR fuzzy flip-flop) and fast (2/3 delay of SR fuzzy flip-flop), and they also realize some fuzzy operations between input fuzzy value and memory. In particular, when the membership memories of fuzzy sets are constructed by proposed fuzzy memory elements, these operations make the performance of fuzzy set operation between inputs and memories can be increased effectively.

These memory elements (including fuzzy flip-flops) can be considered a memory that has simple logical operation, i.e., "Login In Memory". For more than 50 years, all general computers have been designed as the Neumann architecture. On the other hand, in application-specific areas, ASICs have been used—e.g. fuzzy logic controller. Proposed memory elements give the foundation of making a general fuzzy hardware (i.e., fuzzy computer) that is not a Neumann computer. From the viewpoint of computer architecture, proposed fuzzy memory elements are SIMD(Single Instruction Stream Multiple Data Stream) parallel architecture. Generally speaking, fuzzy set operations are essentially SIMD parallel—i.e., a single fuzzy logical operation is performed on multiple elements in fuzzy sets, and SIMD parallel architecture is well suited to fuzzy set operation. Moreover, in order to apply them to fuzzy database, a fuzzy set tends to be large, and a fine grain parallel architecture like a Logic In Memory, compared with a coarse grain parallel architecture like the KAFA that has difficulty in realizing large membership memories, is required.

5.3 Perspective

Two main prospects are considered for proposed fuzzy memory elements, one is SIMD parallel fuzzy processor, and another is fuzzy temporal circuits, i.e., sequential circuits, finite state machines, and fuzzy automata.

Applications of a SIMD parallel fuzzy processor are many fuzzy processing proposed previously including fuzzy logic control using fuzzy inference. Other than fuzzy logic control that have been studied as its application so far, fuzzy clustering, fuzzy data/knowledge base and processing, fuzzy image processing, and more applications that have been realized by software and conventional computers are possibly the target of proposed memory elements, and the performance of these applications is expected to be improved by them. Furthermore, compared with conventional fuzzy logic controller, proposed fuzzy memory elements are general purpose and are flexibly used.

Recently, the some experimental applications of the fuzzy temporal processing have been proposed[7][18][20]. Proposed fuzzy memory elements can be used for these applications. In order to develop the knowledge base, intelligent systems, human-like systems, and etc., temporal logics are important and some fuzzy temporal logics have been researched experimentally. These research areas are now developing and proposed fuzzy memory will be useful for making more complicated fuzzy logic circuits in the future.

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