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Fundamental Study of Metal/Insulator Heterostructure Electron Devices

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Contents

Chapter 1

Introduction

1.1 The Advantages of Using Metal-Insulator Combinations

Owing to developments in telecommunications, higher-speed communication systems and information processing systems have been required. Therefore, high-speed transistors have become extremely important components for such systems.

To decrease the switching time of a transistor, it is necessary to reduce the size of the transistor and to use high-velocity electrons in such a small device. However, the down-scaling of conventional semiconductor devices leads to a significant increase in resistance in the emitter and base regions. Furthermore, in nanometer-size semiconductor structures, statistical fluctuation of the carrier concentrations ocurr. For example, if a 10nm×10nm×10nm box can be made using a semiconductor with a carrier concentration of $1\times10^{18}\mathrm{cm}^{-3}$, there is only one carrier in the box.

From this point of view, metals are suitable for device materials. In comparison with semiconductors, metals have higher carrier concentrations ($\sim10^{22}\mathrm{cm}^{-3}$) and lower resistivities ($\sim10^{-6}\Omega\cdot\mathrm{cm}$). These properties

contribute significantly to the reduction in the device size and obtaining a high current density and hence, decrease in the charging time. Moreover, if we use metals as device materials, there is also the advantage in the reduction of contact resistances and capacitances.

Insulators can also be considered suitable for the device materials in combination with metals. Since in general insulators have lower dielectric constants than semiconductors, capacitances between electrodes can be reduced by the use of insulators. Moreover, the energy band gap of an insulator is relatively large and therefore the breakdown field can be expected to be higher than semiconductor materials. Consequently, electrons in the conduction band of insulator can be accelerated by large electric field, which is advantageous for reducing the response time.

The down-scaling of devices brings out the wave nature of electrons. The quantum interference of electron waves due to multiple reflections i.e. electron resonance, has been discussed as a possible mechanism for transport control in double barriers [1, 2], superlattice structures [3, 4], and transverse potential gratings [5]. Such a mechanism is considered to be suitable for the control of high-velocity electrons.

In certain combinations of metal-insulator materials, the conduction band discontinuity at the heterointerface is larger than 10eV which is more than ten times that of a semiconductor heterointerface. One consequence of this fact is that the metallic well energy subband at the Fermi level is a high index level (~15th subband) and the subsequent spacing between levels is 0.5~1eV. Not only is this interesting from a physics standpoint, but it also makes devices based on quantum mechan-

ical effects more attractive since, contrary to the case of semiconductor quantum wells, the intersubband energies are widely spaced relative to kT even at room temperature where one would strongly prefer to operate such devices.

In this chapter, metal and insulator material combinations suitable for M-I heterostructure electron devices are introduced. Electronic characteristics and crystal structures of various kinds of metal and insulator bulk materials are surveyed to find out the best M-I combinations. For particular combinations, the conduction band offsets at heterointerfaces are estimated, which is very important for electron transport through M-I heterointerfaces.

1.2 Material Components

1.2.1 Crystal structure & lattice mismatch

Single crystalline metal-insulator heterostructures are considered to be more suitable for realizing metal-insulator electron devices than poly-crystalline or amorphous type superlattices. One reason for this is that electron scattering in a single crystal is suppressed to a relatively low level, which makes it possible to utilize high speed electrons in the device materials. Moreover, in single crystalline superlattice, the wave properties of electrons can be expected to be significant and they can be utilized for new devices.

In order to realize single crystalline metal-insulator heterostructures, materials which have nearly the same crystal structure and lattice constant should be chosen.

Figure 1.1 schematically shows the crystal structure and lattice constant near room temperature for various kinds of metals and insulators including semiconductors. Black squares indicate materials which have an energy band gap, i.e. semiconductors and insulators. White ones represent metals.

One of the candidates of lattice matched metal-insulator combinations is the C(diamond)-Cu,Ni,Co system and another one is the Si,CaF_2-$CoSi_2$,$NiSi_2$ system. These materials have nearly the same crystal structure and lattice constant.

Table 1.1 shows the physical properties of C (diamond), Cu, Ni and Co. [6, 7, 8] Co, Ni, Cu are relatively well lattice matched to diamond with mismatches of -0.6%, -1.2% and +1.3%, respectively. Although the lattice mismatch with diamond is rather large, Cu is more attractive than Ni and Co from electron device point of view since the resistivity of Cu is the lowest and its thermal conductance is the highest of all the metals. Metals with low resistivity have advantages in the down scaling of devices. Moreover, diamond has the highest thermal conductivity of all the materials. Therefore electron devices using the C-Cu combination have the highest thermal conductance than any other material combinations.

Table 1.2 shows the material constants of the CaF_2- metal silicide system. CaF_2, $CoSi_2$ and $NiSi_2$ are lattice matched to Si with mismatches of +0.6%, -1.2% and -0.5% at room temperature, respectively. These materials were grown epitaxially on a silicon substrate by conventional molecular beam epitaxy. Although a novel epitaxial growth technique for CaF_2- Metal silicide was required to be developed, the Si-CaF_2-Metal sili-
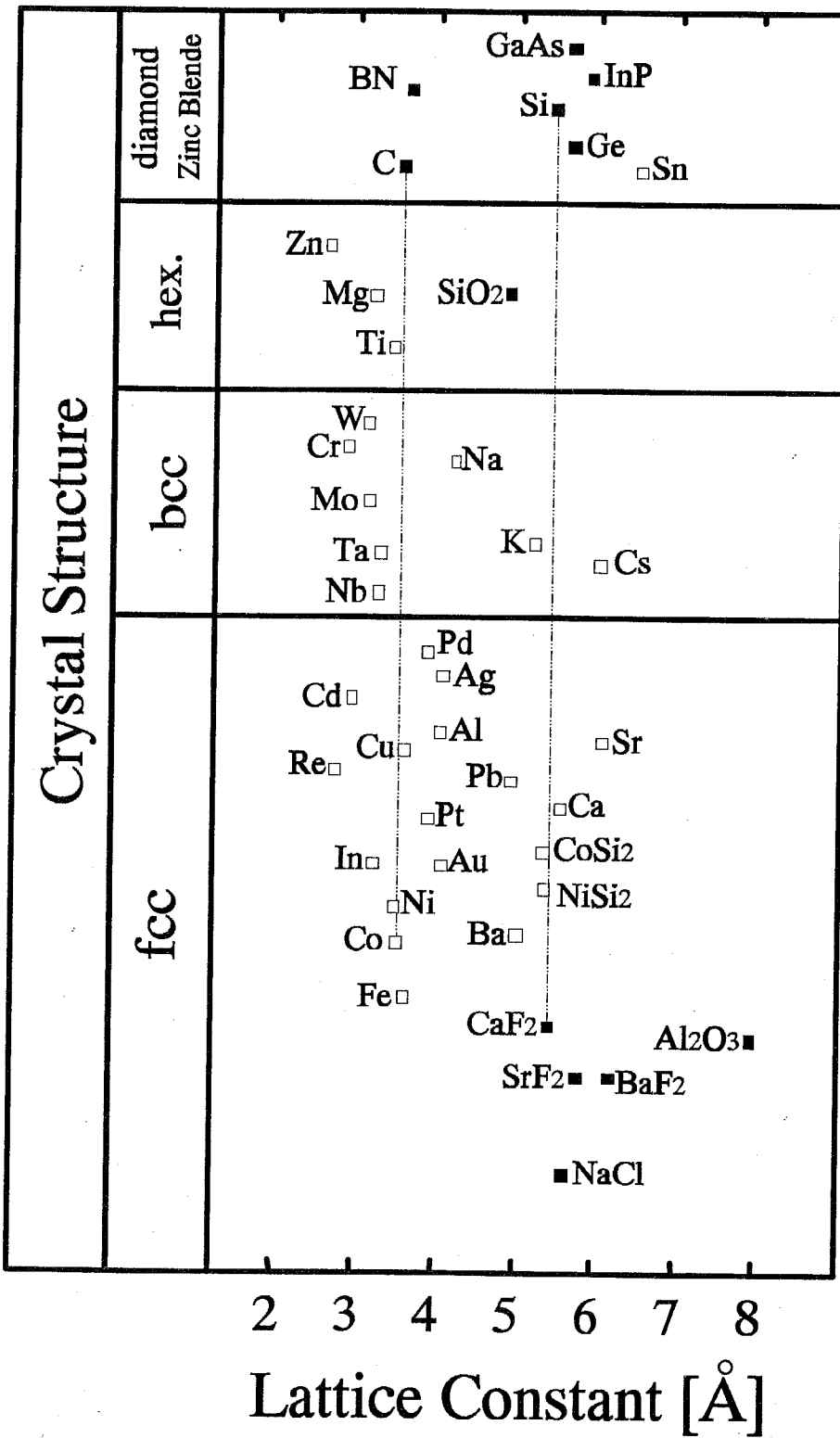
Fig. 1.1: Lattice constant of metals and insulators

Material	C(diamond)	Cu	Ni	Co
Crystal Structure	diamond	fcc	fcc	fcc
Lattice Constant [Å]	3.567	3.6147	3.5236	3.544
Misfit with C [%]	0	+1.34	-1.22	-0.64
Fermi level E_F [eV]	—	7	9	9
Work Function [eV]	—	4.59	5.15	4.79
Electron Affinity [eV]	0.9			
Band Gap E_g [eV]	5.2	—	—	—
Resistivity $\rho[\mu\Omega{\cdot}cm]$		1.55	7.6	6.2
Dielectric Constant ε_r	5.5			
Heat Conduct. [W/m/K]	900-2300	398	90.5	99.2
Melting Point [°C]		1084.6	1455	1494

Table 1.1: Physical constant of diamond, Cu, Co system at 300K

Material	Si	CaF$_2$	CoSi$_2$	NiSi$_2$
Crystal Structure	diamond	fluorite	fluorite	fluorite
Lattice Constant [Å]	5.4305	5.462	5.365	5.406
Misfit with Si [%]	0	+0.58	-1.21	-0.45
Fermi level E$_F$ [eV]	—	—	13	14
Work Function [eV]	—	—	5	5
Electron Affinity [eV]	4	3.1		
Band Gap E$_g$ [eV]	1.11	10	—	—
Resistivity $\rho[\mu\Omega\cdot$cm]	1.40×10^6		10	2
Dielectric Constant ε_r	12	6.7		
Heat Conduct. [W/m/K]	148	10	90	
Melting Point [°C]	1412	1402	1495	993

Table 1.2: Physical constant of CaF$_2$-CoSi$_2$ system at 300K

cide system was chosen from the point of the realisation of heteroepitaxy for the first demonstration of M-I heterostructure devices.

In the following section, physical constants including electric properties of other materials are surveyed to show the position of the C-Cu system and Si- CaF_2- silicide system in other materials.

1.2.2 Electric properties of the Si-CaF_2-silicide and the C-Cu system

In this section, the electric conductance and the work function of metals are surveyed.

Figure 1.2 shows the resistivity near room temperature of metals [6]-[8]. In general, the resistivity of metals is distributed from a few $\mu\Omega$cm to a few hundreds of $\mu\Omega$cm. For applications in electron devices, metals with a resistivity of less than $10\mu\Omega$cm are more attractive than high-doped semiconductors. In principle, we can realize control electrodes with low resistances buried in the devices using single crystalline metals without impurity doping. From that stand point, Cu, Ag, Au, Al are very attractive metals. The resistivity of $CoSi_2$ is about 5 times larger than Cu, however, this value is still attractive compared with doped semiconductor materials.

Figure 1.3 shows the work function of metals [7]-[8]. Metals are suitable for an electron source material in electron devices since metals have high carrier densities ($\sim 10^{22}$cm^{-3}). Metals with low work functions are appropriate for the emitter material because electrons can be extracted more easily by applying relatively low external voltages. From this stand point, alkaline and alkaline-earth metals like Na, Ba, Cs are candidates
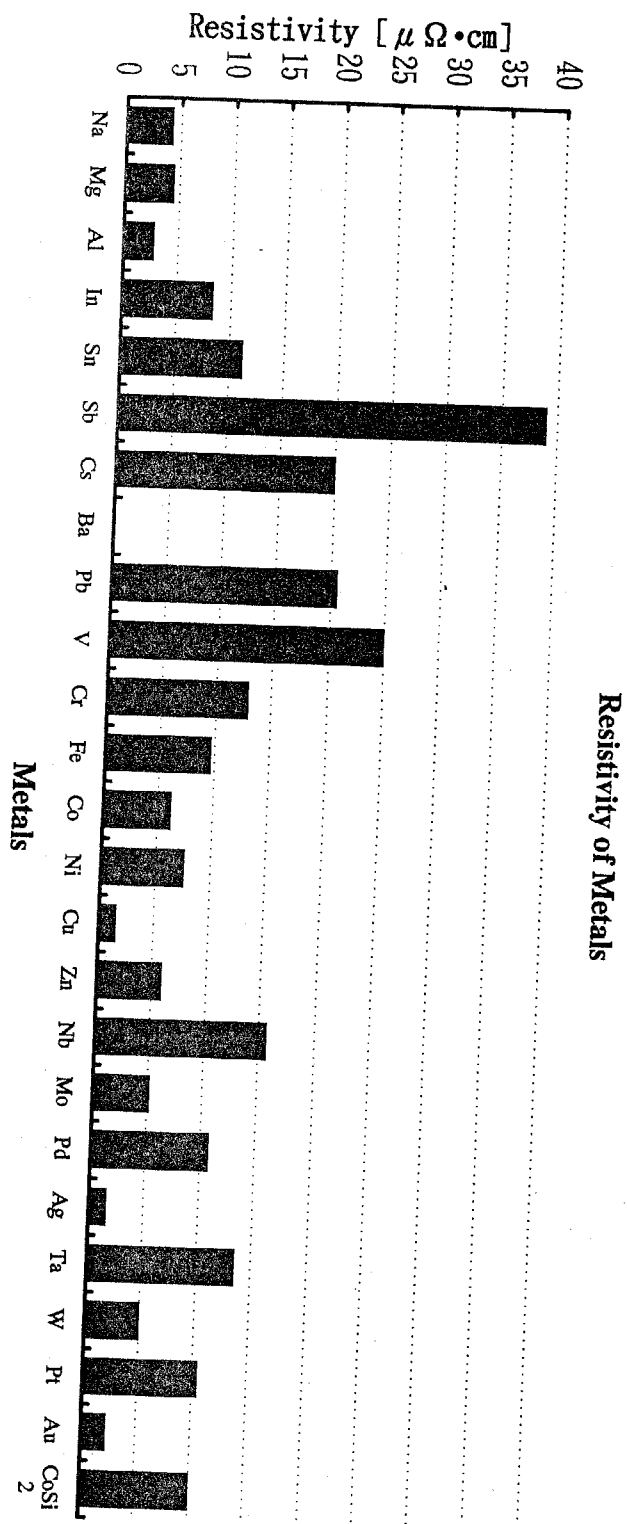
Fig. 1.2: Resistivity of Metals

for the emitter material, however, these metals are chemically radical and melting point is relatively low. The work function of Cu, Co, Ni and $CoSi_2$ ($NiSi_2$) is distributed around 5eV (Cu:~4.5eV). This value is not small compared with other metals but these metals have a high melting point so they are relatively thermally stable.

Table 1.4 shows the fermi energy (E_F) of metals. In general, metals with a large fermi energy have high carrier densities and can provide high speed electrons near the fermi level. From that point of view, $CoSi_2$, $NiSi_2$ (E_F ~13eV), Cu(7eV), Co and Ni(9eV) are attractive materials for electron devices even compared with Au, Ag(5.5eV), which have relatively low resistivities.

From aspects of thermal stability of the devices, high melting point materials are desirable since high speed operation requires a large driving current so that the thermal stability of the material limits the response time of the device. Si, Co, Ni, $CoSi_2$, C(diamond) and CaF_2 have melting points larger than 1400°C so these materials have better thermal stability compared with Cu, Au (~1000°C) or Al (~660°C) and alkaline metals (Na,K,Cs:M.P.<100°C).

1.2.3 The conduction band offset at the M-I heterointerface

In general, the conduction band offset at a metal-insulator heterointerface is more than ten times larger than that of semiconductor, which means that we can expect strong quantum interference at the metal-insulator heterointerface. In this section, the conduction band offset (ΔE_C) of the Si-CaF_2-silicide and the C-Cu,Co heterojunctions are roughly estimated
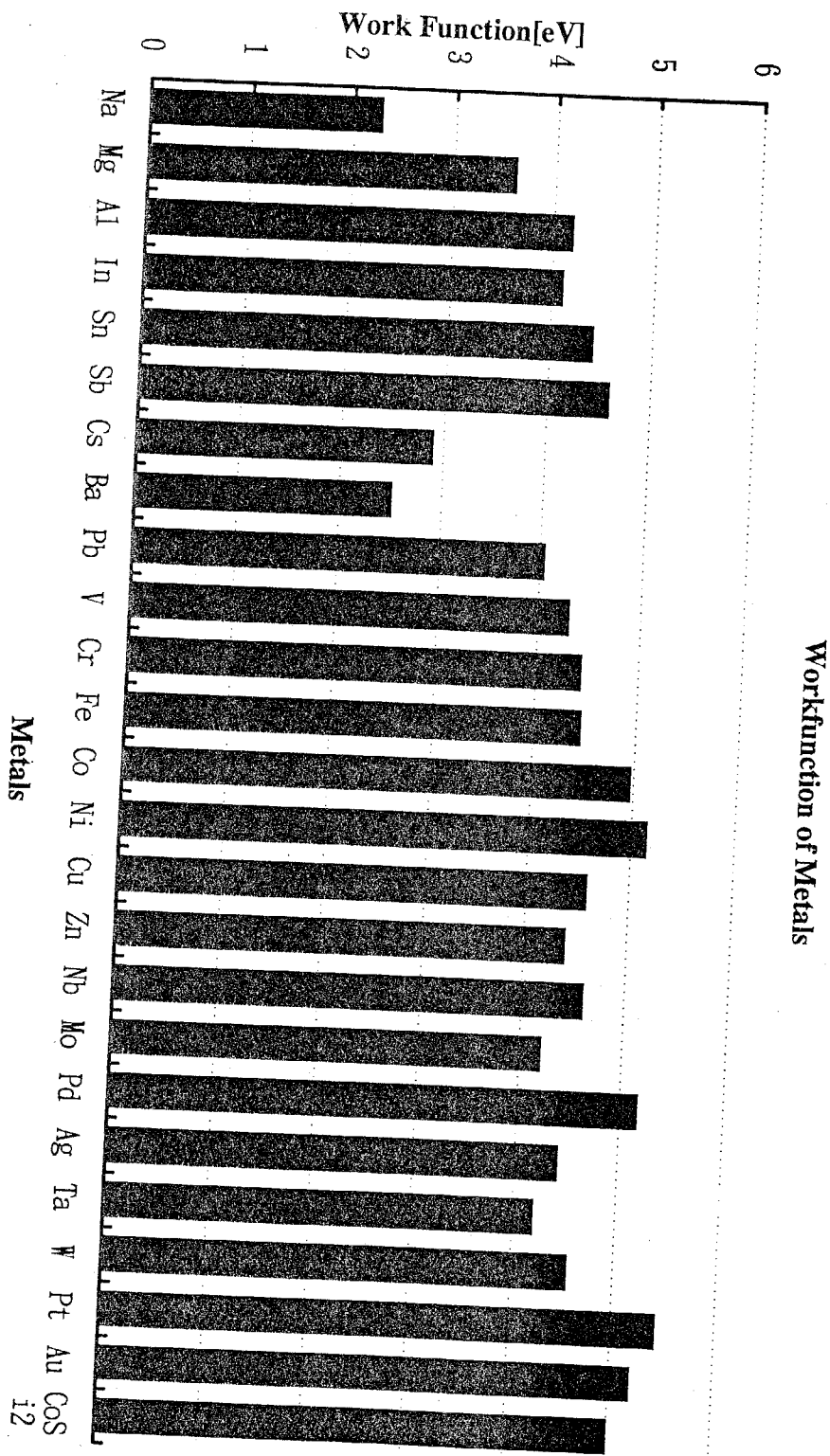
Fig. 1.3: Work function of Metals
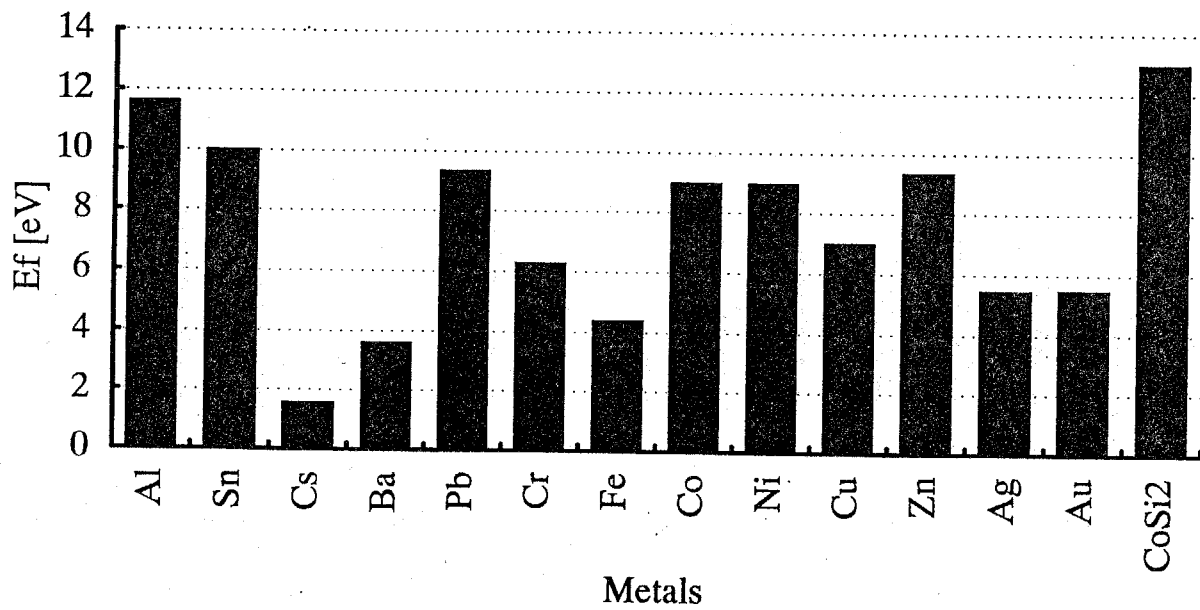
Fermi Level of Metals

Fig. 1.4: Fermi level of Metals

from the work function and the electron affinity of the bulk metals and insulators.

Figure 1.5 shows the energy band diagram of CaF_2, $CoSi_2$ and Si (using table 1.2). Each constant was referred from the bulk materials, many of which were estimated by experiment. C and V means conduction band edge and valence band edge, respectively. The hatched region in the metal area indicates the energy range in which conduction band is filled with electrons.

The Conduction band offset between CaF_2 and $CoSi_2$ was estimated as shown in Fig.1.7. The band discontinuity shown here was the difference between the conduction band edge of each material. Other effects were not considered. The ΔE_C between CaF_2- $CoSi_2$ ($NiSi_2$) heterojunction is about 15eV and that of Si-$CoSi_2$ is 14eV. In the case of Si-$CoSi_2$, the barrier height from the fermi level (E_F) of $CoSi_2$ to the conduction band edge of Si (ϕ) is 1eV. On the other hand, in the case of CaF_2- $CoSi_2$, ϕ is about 2eV. In order to inject electrons from metal emitter to conduction band of insulator or semiconductor, an excitation energy equal to or larger than ϕ is required. Therefore, material combinations with low ϕ have advantages for low power operation of the device. From that stand point, Si-$CoSi_2$ is an attractive combination compared with CaF_2- $CoSi_2$. On the other hand, CaF_2 has wide band gap(E_g) $\sim$10eV (Si:E_g $\sim$1.1eV) so the break down voltage is relatively high, which means that electrons moving through CaF_2 can be accelerated by relatively high applied fields, which leads to a high speed response of the device.

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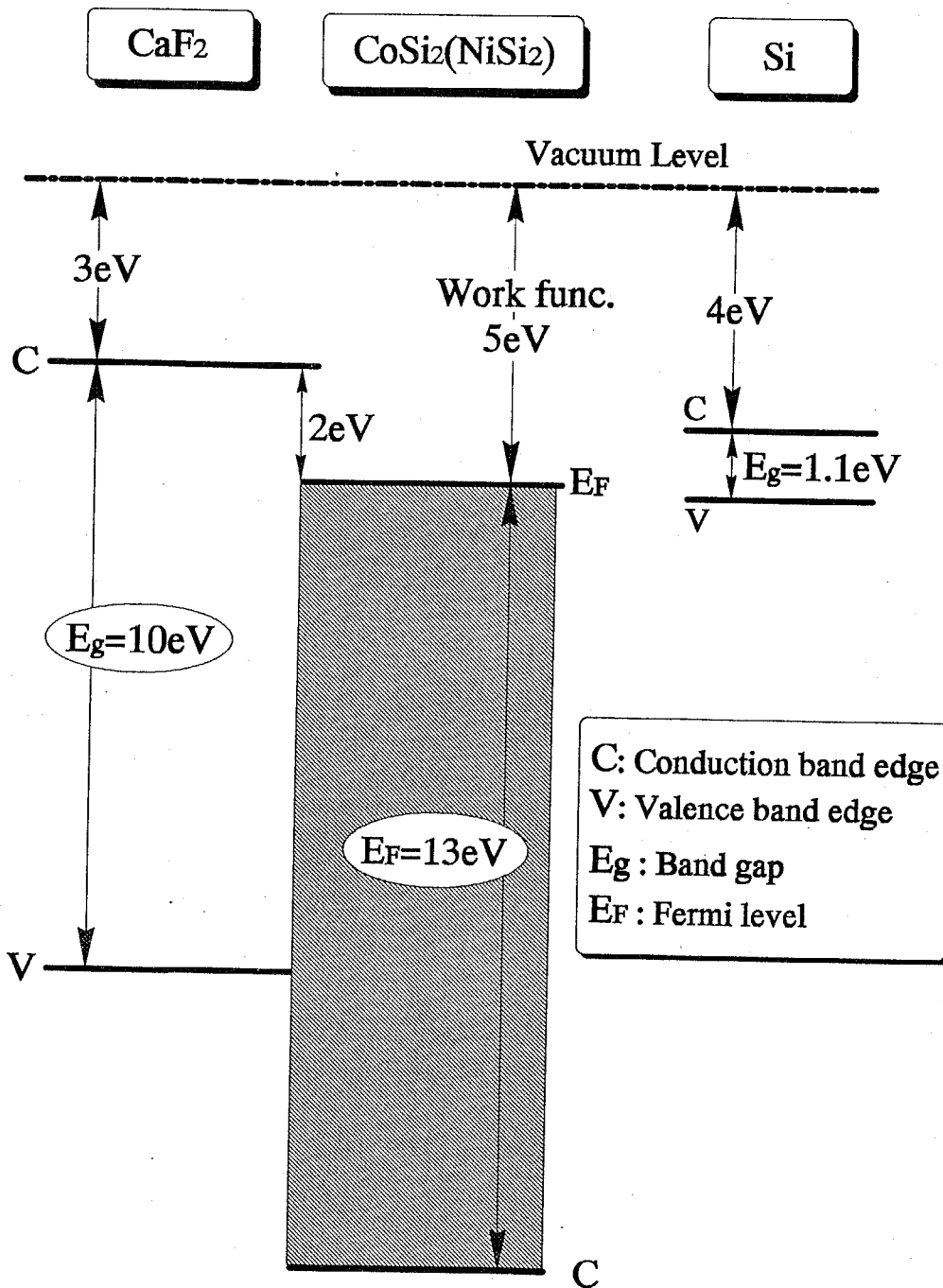
CaF₂   CoSi₂(NiSi₂)   Si

Fig. 1.5: Energy band profile of CaF₂, CoSi₂, Si

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C (diamond)   Cu   Co   Ni

Vacuum Level

0.9eV

C

E_g=5.2eV

3.7eV

Work func.
4.6eV

5eV

E_F

V

E_F=7eV

E_F=9eV
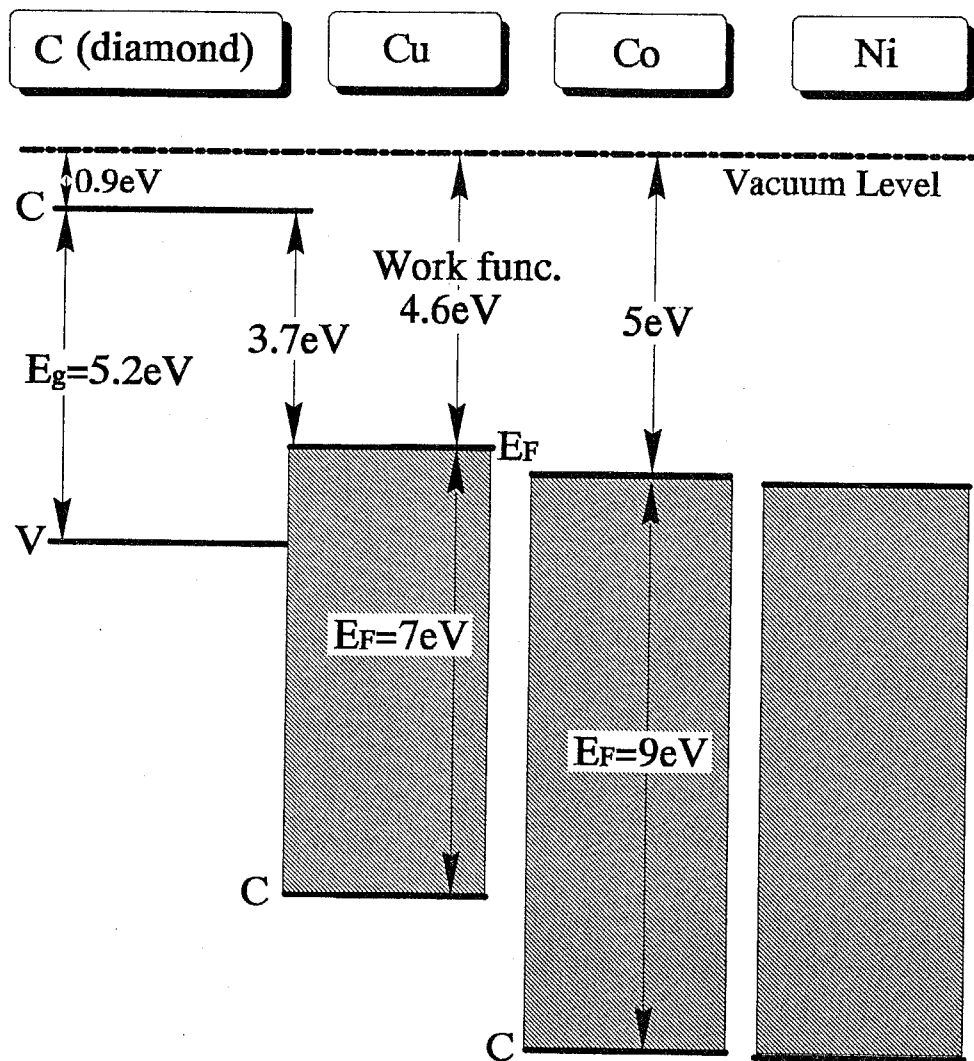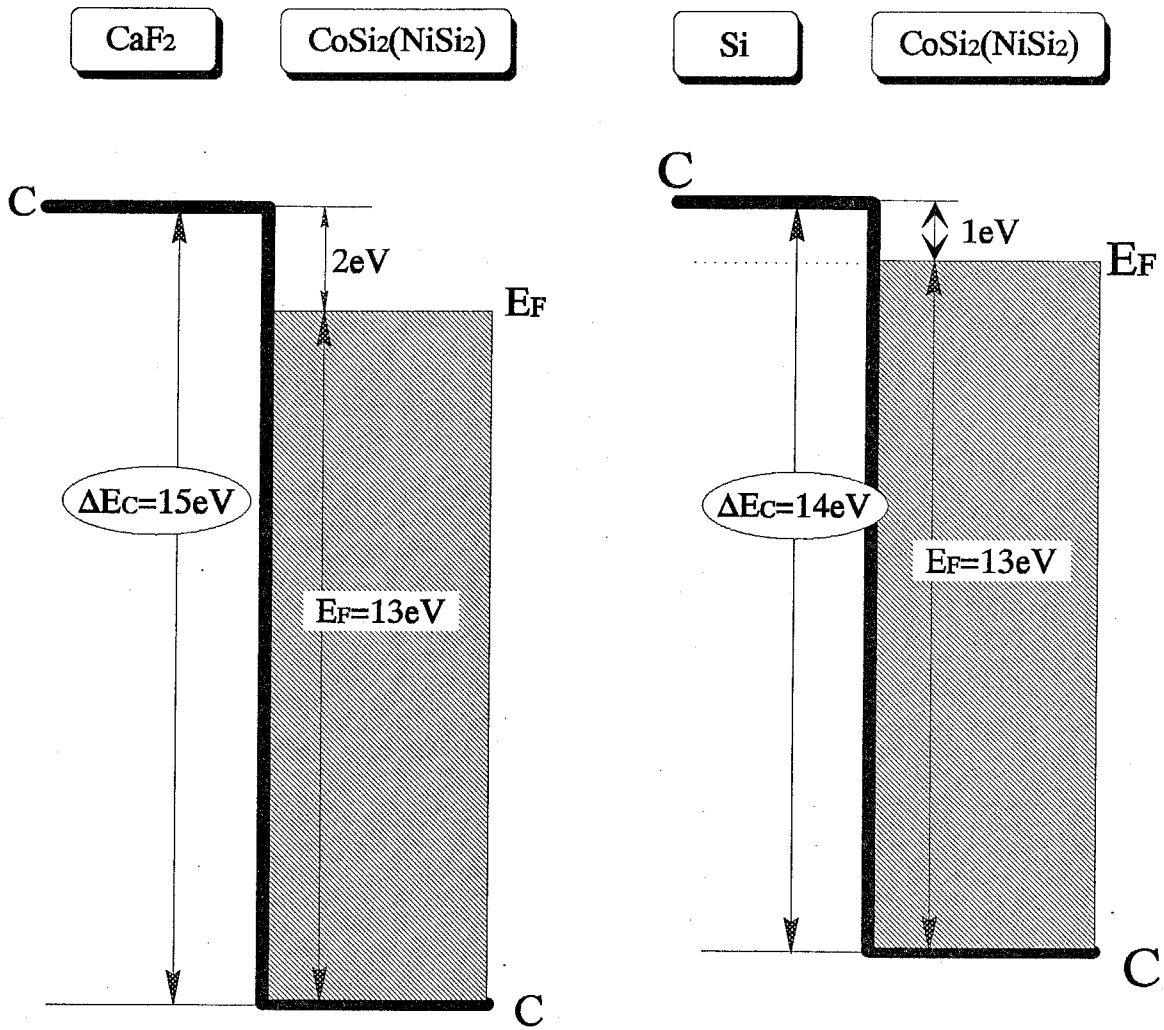
C

C

Fig. 1.6: Energy band profile of C, Cu, Co

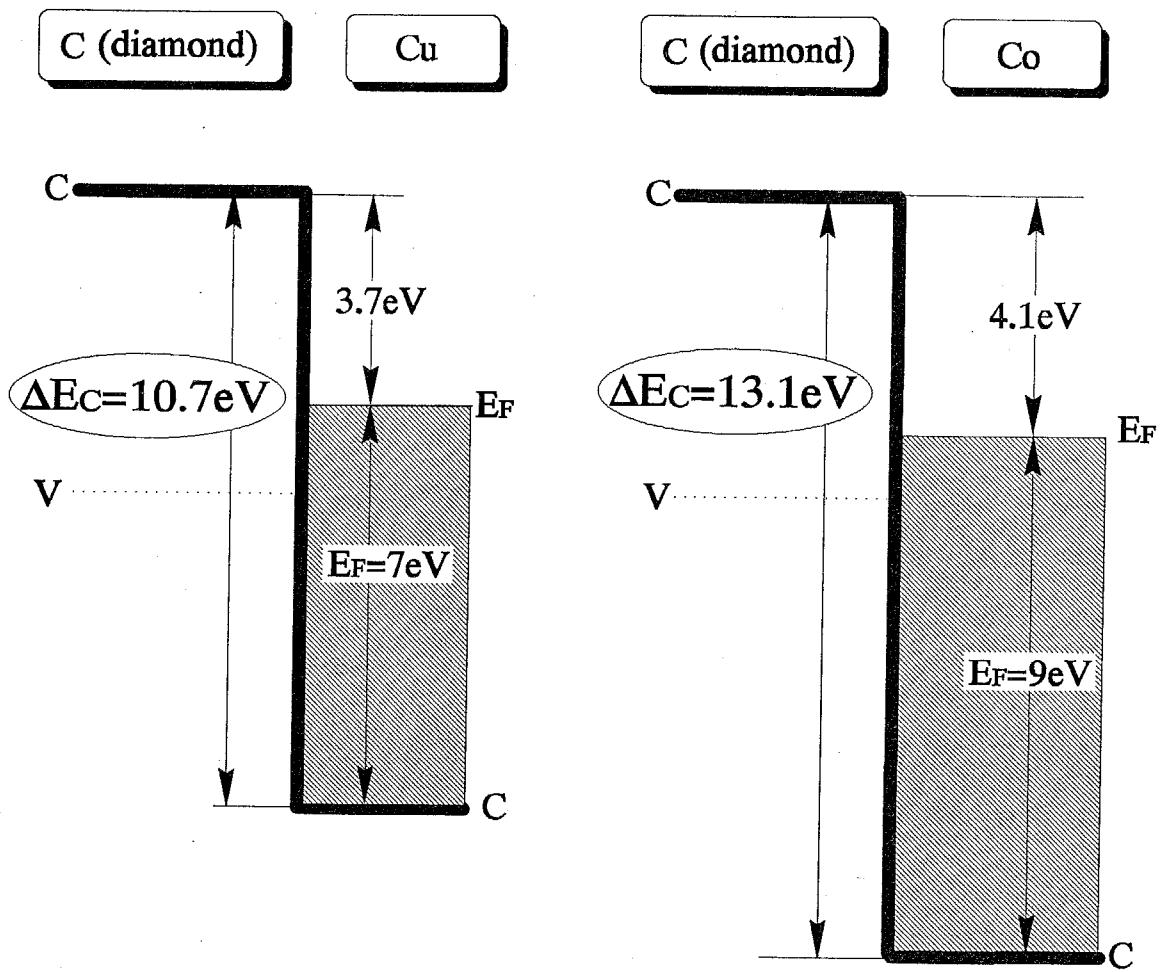Fig. 1.7: Band profile of metal-insulator heterointerface (CaF$_2$-Silicide)

Fig. 1.8: Band profile of metal-insulator heterointerface (C-Cu,Co)

1.2.4 Summary: Metal/Insulator Used in This Study

In comparison with semiconductors, metals have higher carrier concentrations ($\sim 10^{22} \mathrm{cm}^{-3}$) and lower resistivities ($\sim 10^{-6} \Omega \cdot \mathrm{cm}$) without impurity doping. These properties contribute significantly to the reduction of the device size and obtaining a high current density, which results in a decrease in the charging time.

The down-scaling of the device brings out the wave nature of electrons. In metal-insulator combination, the conduction band discontinuity at heterointerface is larger than 10eV. That is more than ten times larger than that of semiconductor heterointerface. One consequence of this fact is that we can expect much stronger quantum mechanical effects than semiconductor heterojunctions, which makes it possible to produce nanometer or even atomic size quantum effect electron devices.

As a metal-insulator material, Si-CaF$_2$-silicide and C-Cu,Co system were proposed from the point of the similarity of the crystal structure and lattice constant. For the first demonstration of heteroepitaxy and realization of metal-insulator devices, Si-CaF$_2$- CoSi$_2$ was chosen. The main features of this material system are follows.

1. Availability of materials (Si,Co,CaF$_2$) compared with C(diamond).

2. High melting point ($\sim 1500°C$)

3. Low barrier energy ϕ (CoSi$_2$-CaF$_2$:2eV, CoSi$_2$-Si:1eV)

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1.3 Purpose and Contents of this Thesis

The major purpose of this study is an investigation into novel metal-insulator heterostructure electron devices. Before this doctoral study started, the idea of a novel ultrahigh-speed electron device using a metal and insulator was proposed theoretically by Y. Nakata, M. Asada and Y. Suematsu [3]. The device principle was based on the electron resonance in the subband of metal-insulator superlattices, therefore the device was named RETT (Resonant electron tunneling triode). At the next stage, non quantum effect type electron device named SCLIT, using Space Charge Limit effect in the conduction band in Insulator was proposed by Y. Chaki, T. Sakaguchi, M. Asada and Y. Suematsu[9]. In this study, a novel of metal-insulator high speed electron device is proposed using hot electron resonance in conduction band of insulator, which can overcome the weakpoint of the RETT and the SCLIT.

At the initial stage of this study, however, there was no-epitaxial growth technique for metal- insulator heterostructures. Therefore, this research was done with emphasis upon the establishment of the epitaxial technique of metal-insulator heterostructures and experimental confirmation of the device operation of the nanometer-thick metal-insulator heterostructure transistor or resonant tunneling diode.

According to these purposes, the outline of this thesis is described as shown in Fig.1.9.

Chapter 1 is devoted to the introduction of the metal and insulator by emphasizing the advantage of these materials for electron devices in

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Introduction

Chapter 2
Metal-Insulator Quantum
Interference Electron Devices

Chapter 3
Metal(CoSi2)/Insulator(CaF2)
Heteroepitaxy on Si(111)

Chapter 4
Metal-Insulator Triple-Barrier
Resonant Tunneling Diode

Chapter 5
Metal-Insulator
Hot Electron Transistor
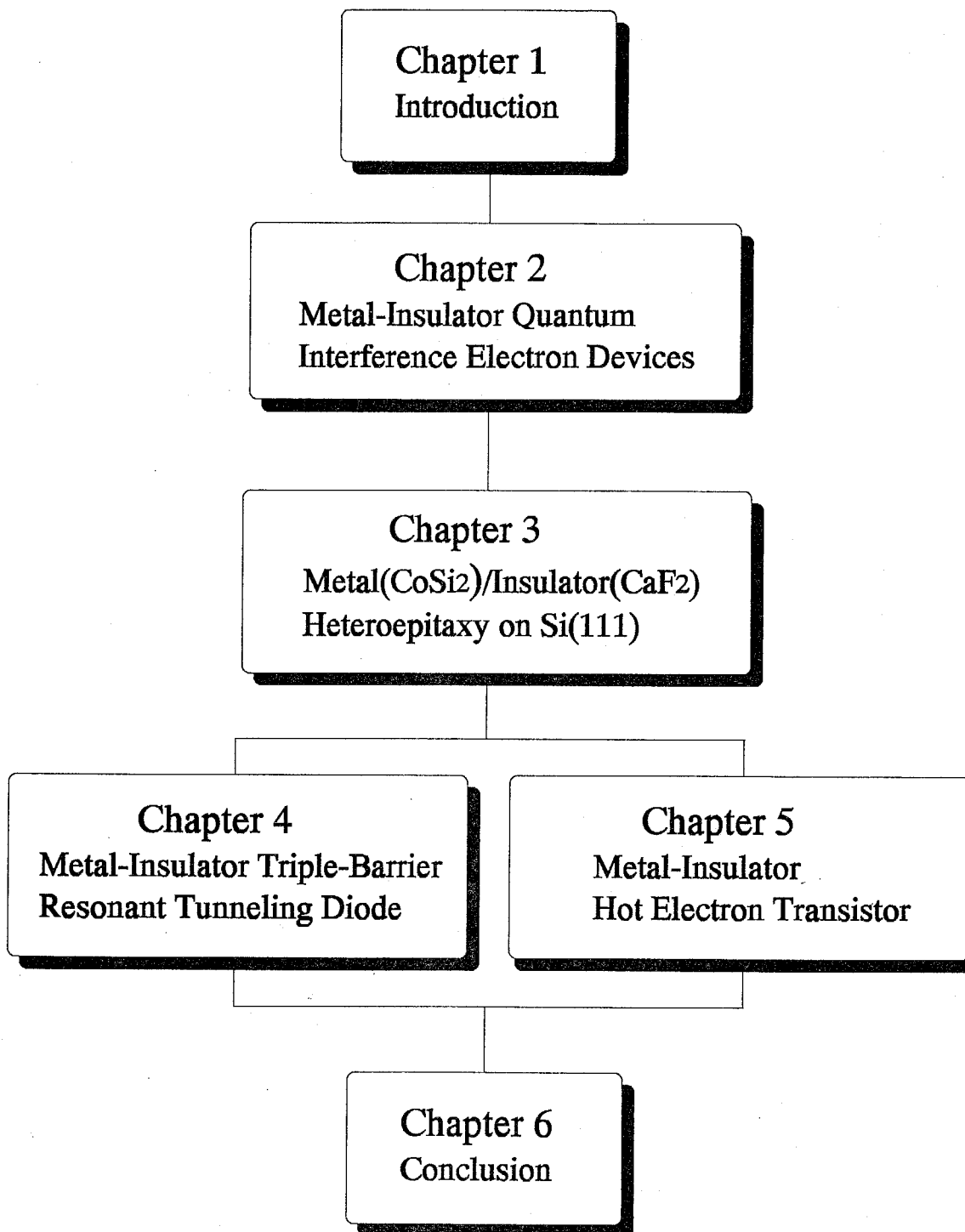
Chapter 6
Conclusion

Fig. 1.9: Flow chart of this thesis.

comparison with conventional semiconductor materials.

In chapter 2, a novel metal-insulator heterostructure device is proposed. This device utilizes hot electron and therefore can be expected to reduce the transit time in comparison with the RETT. Furthermore, the current is controlled by electron resonance, which can realize higher transconductance than the SCLIT, which controls current by the space charge limiting effect. The structure and operation principle of the device is firstly shown and then the static characteristics and response time is analyzed.

In chapter 3, epitaxial growth techniques for metal- insulators are developed. $CoSi_2$ was chosen as the metal and CaF_2 as the insulator and Si(111) as the substrate. Low temperature epitaxy of CaF_2 using ionized beam epitaxy is demonstrated and the conditions of $CoSi_2$ growth by two step growth are made clear, which makes it possible to avoid agglomeration of the metal. Finally, the electric conductance of the nanometer-thick $CoSi_2$ metal layer sandwiched by epitaxial CaF_2 was estimated and the possibility of device application of a few monolayer thick metal epi-layers embedded in an insulator is shown.

In chapter 4, electron transport in metal-insulator heterostructures is demonstrated and negative differential resistance in a resonant tunneling diode structure was observed for the first time. The conduction band offset at metal-insulator heterointerface is quite large, so we can expect strong quantum interference even at room temperature. In the three barrier resonant tunneling diode structure, negative differential resistance characteristics at 77K and room temperature is shown and the obtained

I-V characteristics and resonant bias voltage is discussed by comparing with a simple theoretical estimation.

In chapter 5, the first transistor action of nanometer-thick metal-insulator hot electron transistor is demonstrated. Initially, the fabrication process was introduced and then the static characteristics of metal-insulator hot electron transistor at 77K is shown and current gain is estimated. Finally, the physical interpretations of the static characteristics and current gain is discussed.

As a conclusion, the results obtained in this study are summarized in Chapter 6.

Chapter 2

Metal-Insulator Quantum-Interference High-Speed Electron Devices

2.1 Introduction

Owing to developments in telecommunications, higher-speed communication systems and information processing systems have been required. Therefore, high-speed transistors have become extremely important components for such systems.

To decrease the switching time of a transistor, it is necessary to reduce the size of the transistor and to use high-velocity electrons in such a small device. However, the down scaling of conventional semiconductor devices leads to a significant increase of resistances in the emitter and the base regions. Furthermore, in a nanometer-size semiconductor structure, this brings a statistical fluctuation of carrier concentration. For example, if we can make a 10nm×10nm×10nm box using a semiconductor with carrier concentration of 1×10^{18}cm^{-3}, there is only one carrier in it.

From this point, metals are suitable for the material of devices. In

comparison with semiconductors, metals have higher carrier concentration ($\sim 10^{22}$cm^{-3}) and lower resistivity ($\sim 10^{-6}\Omega$·cm) as shown in previous chapter. These properties contribute significantly to the reduction of the device size and obtaining high current density, which results in the decrease of the charging time. Moreover, metal has the advantage in the reduction of contact resistances and capacitances.

Insulators are also considered to be suitable since it has lower dielectric constant than those of semiconductors, which result that capacitances between electrodes can be reduced.

The down scaling of the device brings out the wave nature of electrons. The quantum interference of electron wave due to multiple reflections has been discussed as a possible mechanism for transport control in double barriers[1, 2], superlattice structures[1, 3, 4], and transverse potential grating[5]. Such a mechanism is considered to be suitable for the control of high-velocity electrons.[5] At metal-insulator (M-I) heterointerface, large conduction band offset exist and we can utilize quantum effect even at room temperature for the device operation principle.

In this chapter, a novel transistor using metal and insulator is proposed from the above mentioned view points. The quantum interference of electrons in the conduction band of an insulator is used as the operation mechanism of the device. The possibility of subpicosecond response is discussed theoretically.

2.2 Structure and Operation Principle of the Device

The transistor discussed in this chapter is shown in Fig.2.1. This device consists of metal ($CoSi_2$), insulator (CaF_2) and semiconductor (Si) grown on Si(111) substrate. The device has four terminals termed "source", "cathode", "grid", and "plate" as indicated in the figure. Input signal is superimposed on the grid voltage V_g between the cathode and the grid, and output signal is obtained as a change in the plate current. The source voltage V_s is applied between the source and the cathode to emit electrons from the source. Ballistic transport is assumed all the from the source to the plate.

Layers between the source and the cathode from the resonant tunneling (RT) emitter which emits high velocity electrons with a narrow energy distribution toward the plate at a constant rate. The narrow energy distribution of electrons is essential for this device based on quantum interference effect.

The electrons emitted from the RT-emitter enter the conduction band of the insulator between the cathode and the grid, and the interference of electron wave occurs between the two interfaces of the insulator. The transmission coefficient of electron wave through this region has quite strong wavelength selectivity due to the interference. To see this property, we calculated the transmission coefficient in the structure shown in Fig.2.2(a). The transmission coefficient T of the electron, the energy of which is higher than the potential energy of this rectangular barrier, is shown in Fig.2.2(b) as a function of electron energy. Note that the

Fig. 2.1: Metal-Insulator Quantum Interference Transistor

change of the transmission coefficient for the high barrier case (V_0 =15eV for $CoSi_2$/ CaF_2 [14, 15, 16, 17, 18, 19]) is very sharp in comparison with that for the low barrier case (V_0 =0.2eV for GaInAs/InP as an example of semiconductor heterostructures). This sharp change of the transmission coefficient is applied to the control of current density in the present device by changing the voltage (V_g) between the cathode and the grid. A large transconductance can be obtained due to the strong wavelength selectivity.

Reflection takes place also at the right interface of the grid. However, this reflection is little influential due to the following reason. Actually, there is a beat between the two waves reflected toward the left direction at the left and right sides of the grid layer. Due to this beat, amplitude modulation occurs in the transmission characteristics in Fig.2.2(b). However, the period of this amplitude modulation (inversely proportional to the grid layer thickness), is much larger than the intervals between the peaks in Fig.2.2(b) (inversely proportional to the cathode-grid insulator layer thickness), and therefore, the change in the transmission characteristics is small in the electron energy range discussed here.

Electrons are repelled back to the RT-emitter due to the above mentioned interference in the cathode-grid insulator layer if their energy is located at the off-resonant level of the interface. These electrons may go back to the source through the resonant tunneling levels if scattering is negligible, and thus, the total current from the source decrease equivalently. In an exact treatment, the whole potential profile from the source to the plate must be regarded as one transmitter. In this case, the

(a)

electron wave interference
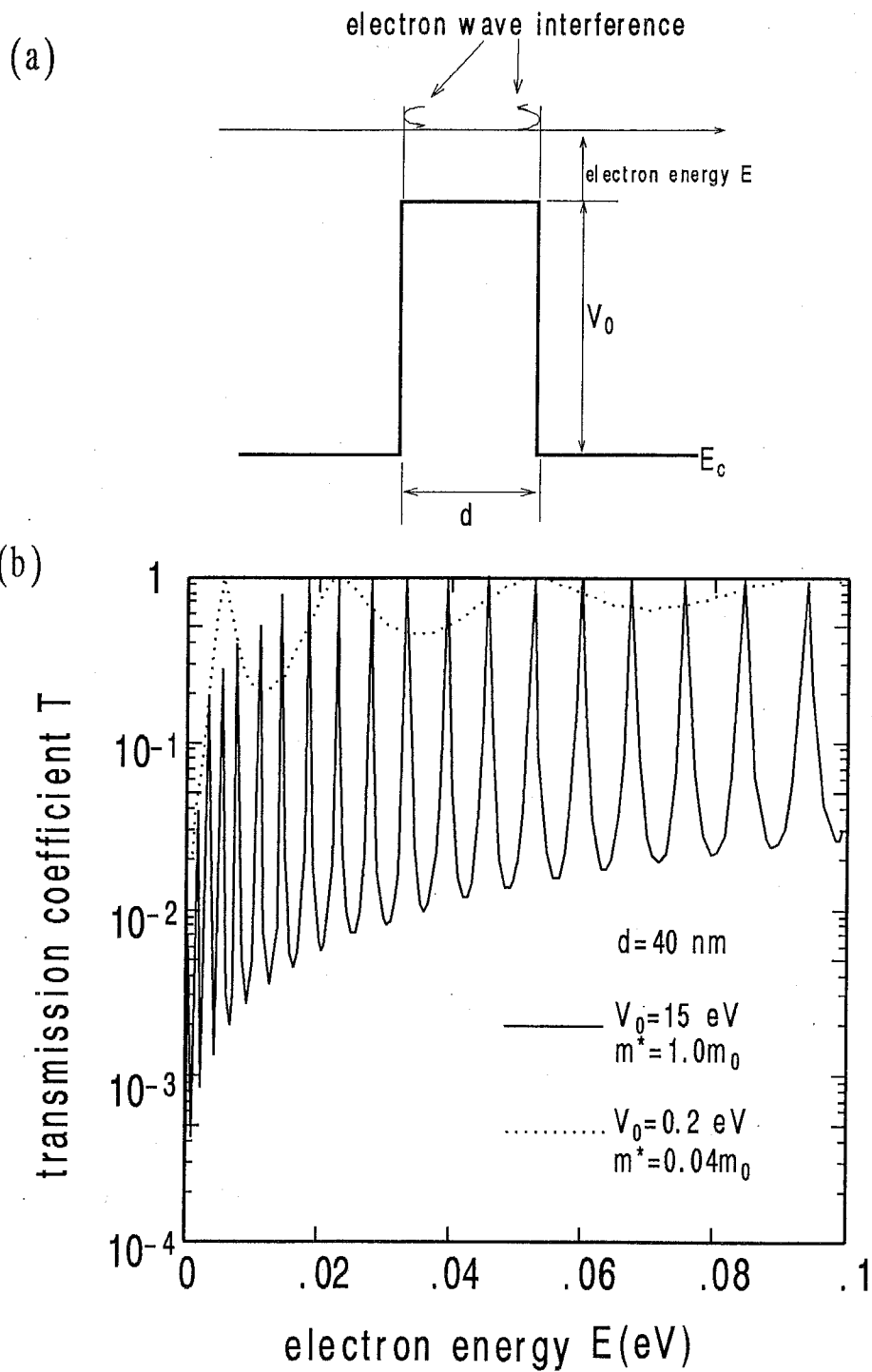
electron energy E

V_0

E_c

d

(b)

Fig. 2.2: (a) The conduction band diagram of the rectangular barrier. (b) The transmission coefficients T for the barriers in (a) as a function of the electron energy measured upward from the top of the barrier.

equivalent decrease of the total current is expressed as that in the total transmission coefficient.

The electrons transmitting through the insulator between the cathode and the grid enter the i-Si between the grid and the plate. Then the electrons attain to the plate (n^+-Si) and they become the plate current. We assume an Si layer between the grid and the plate instead of CaF_2. This is because (i) the electrons through the grid can gain the energy and the electron velocity increases, since the conduction band difference between CaF_2 and Si is 1eV ([15, 18, 19]), and (ii) the reflection at the interface between i-Si and n^+-Si (plate) is quite small, e.g., the reflection of the probability flux is less than only 1.5% assuming electron energy larger than 1.6eV and abrupt interface between i-Si and n^+-Si with the bandedge difference less than 1eV. According to (ii), the plate current is nearly equal to the current through the i-Si layer, and is kept constant with the change of the plate voltage V_p. Thus, the plate current changes with the change in the grid voltage V_g.

The device shown here is similar to the hot electron transistor (HET). In the present device, however, the base-emitter region in HET's has been separated into two regions with different functions, i.e., the emitter (source to cathode region) and the controller (cathode to grid region). As a result, small capacitance between the cathode and the grid and the tunneling current density sufficient to drive loads at high speed[5] can be ensured at the same time by designing the thickness of insulator layers in the emitter and controller regions separately.

Small capacitance between the cathode and the grid results in high

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speed operation due to small charging time in the common-cathode configuration, although the capacitance between the source and cathode is influential in the common-grid configuration if the source is grounded.

Crystal growth of metal and insulator thin layers is a key technology to realize this device. Epitaxy technique and device fabrication method is described in the following chapter.

2.3 Analysis of Device Characteristics

2.3.1 Calculation of Transmission Coefficient

We treat the collision-free electrons in the device using the Schrödinger's equation. One-dimensional potential distribution $V(z)$ is assumed here, i.e., the potential is constant along the x and y directions. Using the effective mass approximation [21], the equation of the electron wave function (envelope function) ϕ_z is written as

$$\frac{\hbar^2}{2m^*}\frac{\partial^2\psi_z}{\partial z^2} + [E_z - V(z)]\psi_z = 0 \qquad (2.1)$$

where E_z is the electron energy along the z direction and m^* is the effective mass.

To solve Eq.(2.1), $V(z)$ of the device is divided into piecewise-linear potentials as schematically shown in Fig.2.3. A solution of the equation in the region i $(z_{i-1}\leq z\leq z_i)$, $\psi_i(z)$, will be given as

$$\psi_i = C_i^+\phi_i(z) + C_i^-\chi_i(z) \qquad (2.2)$$

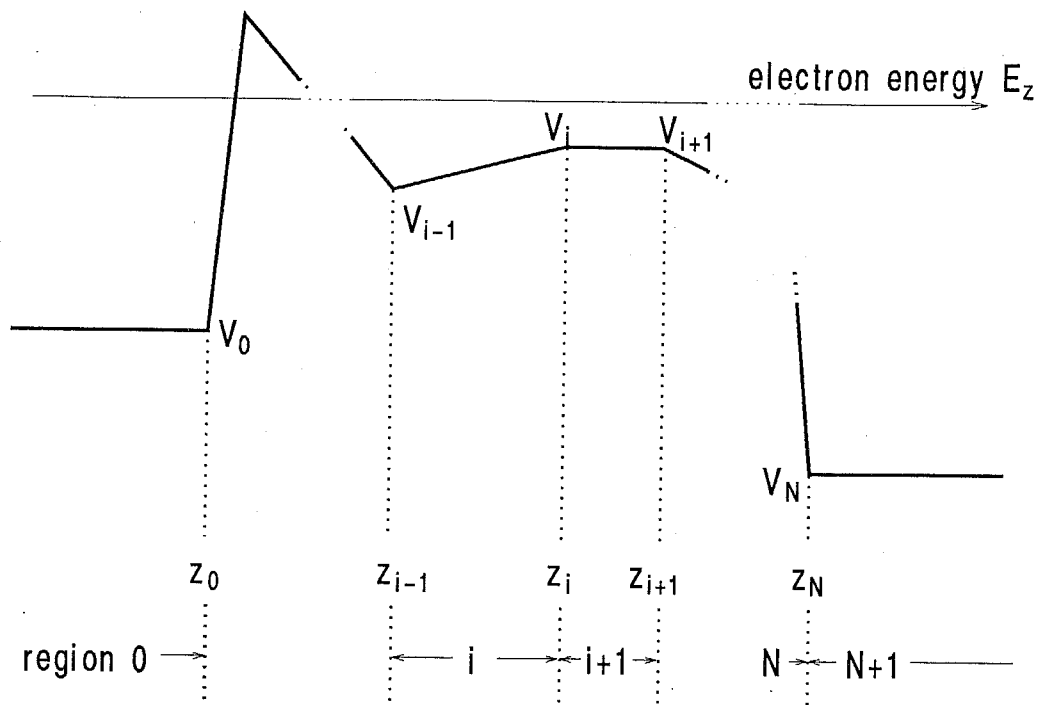where C_i^+ and C_i^- are constants. When the potential in the region i

Fig. 2.3: The piecewise-linear potential for the calculation of the transmission coefficient in the potential of the device.

is constant, i.e., $V_{i-1} = V_i$, ϕ_i and χ_i are represented as

$$\begin{cases} \psi_i(z) = exp(jk_i z) \\ \chi_i(z) = exp(-jk_i z) \end{cases} \quad (2.3)$$

with

$$k_i = \frac{\sqrt{2m_i^*(E_z - V_i)}}{\hbar}$$

where m_i^* is the effective mass in the region. When $V_{i-1} \neq V_i$, ϕ_i and χ_i are described using the Airy functions Ai and Bi[22],

$$\begin{cases} \psi_i(z) = Ai(s) \\ \chi_i(z) = Bi(s) \end{cases} \quad (2.4)$$

with

$$s = r_i(z + a_i)$$
$$r_i = \left(\frac{V_i - V_{i-1}}{z_i - z_{i-1}} \frac{2m_i^*}{\hbar^2} \right)^{\frac{1}{3}}$$
$$a_i = \frac{z_i - z_{i-1}}{V_i - V_{i-1}}(V_i - E_z)$$

For the boundary condition at the interface z_i, we assume the continuity of the wave function (envelope function) and its first derivative divided by the effective mass[23, 24];

$$\begin{cases} \psi_i(z_i) = \psi_{i+1}(z_i) \\ \frac{\psi_i'(z_i)}{m_i^*} = \frac{\psi_{i+1}'(z_i)}{m_{i+1}^*} \end{cases} \quad (2.5)$$

This assumption ensures the continuity of the probability current. Using Eqs.(2.2)-(2.5), we have

$$M_i(z_i) \begin{pmatrix} C_i^+ \\ C_i^- \end{pmatrix} = M_{i+1}(z_i) \begin{pmatrix} C_{i+1}^+ \\ C_{i+1}^- \end{pmatrix}, i = 1, 2, \cdots, N - 1 \quad (2.6)$$

where

$$M_i(z) = \begin{pmatrix} \phi_i(z) & \chi_i(z) \\ \phi_i'(z)/m_i^* & \chi_i'(z)/m_i^* \end{pmatrix}$$

At the left- and right-hand sides of the potential ($z < z_0$ and $z_N < z$, respectively),

$$\begin{aligned} \psi_0 &= exp(jk_0 z) + C_{ref} exp(-jk_0 z) \\ \psi_{N+1} &= C_{trans} exp(jk_{n+1}z) \end{aligned} \qquad (2.7)$$

where C_{ref} and C_{trans} are the reflection and transmission amplitudes. Using the boundary conditions 2.5 at $z = z_0$ and z_N, we obtain

$$\begin{pmatrix} C_{trans} \\ 0 \end{pmatrix} = K_N K_{N-1} \cdots K_0 \begin{pmatrix} 1 \\ C_{ret} \end{pmatrix} \qquad (2.8)$$

where

$$K_i = M_{i+1}^{-1}(z_i) M_i(z_i)$$

The reflection coefficient R and transmission coefficient T are given by

$$R = C_{ref}^* C_{ref} \qquad (2.9)$$

$$T = C_{trans}^* C_{trans} \times \frac{k_{N+1}}{k_0} \qquad (2.10)$$

2.3.2 RT-Emitter

In this section, we analyze the RT-emitter in the device of Fig.2.1.

When the voltage V_s is applied across the barriers between the source and the cathode, the emitted current density J_0 is given by[20]

$$J_0 = \frac{em^* k_B \theta}{2\pi^2 \hbar^3} \int_0^\infty T \cdot ln \left(\frac{1 + exp[(E_f - E_z)/k_B\theta]}{1 + exp[(E_f - E_z - eV_s)/k_B\theta]} \right) dE_z \qquad (2.11)$$

where e is the electron charge, k_B is the Boltzmann's constant, E_f is the Fermi energy of the metal, θ is the temperature, and T is the transmission coefficient across the source-to-cathode potential. The barrier height is 15eV and the Fermi energy of the metal ($CoSi_2$) is 13eV[16, 17]. The applied voltage V_s is therefore required exceed 2V to emit electrons into the conduction band of the insulator. The electric field over 10^7V/cm is required within the 1nm-thick barrier. Breakdown phenomena in bulk insulator is caused by (i) Zener effect, (ii) electron emission from the trap level of impurities of defects, and (iii) avalanche effect caused by (i) and (ii). Zener effect, however, is expected to be negligibly small due to a large energy gap in the insulator (for example, the energy gap of CaF_2 is 10eV). The effects (ii) and (iii) can be averted by making a high quality crystal by an epitaxial growth and by making the insulator layer thinner than the mean free path. These problems are discussed in Ref.[4] in detail.

The emitted current density J_0 as a function of the source applied voltage V_s is shown in Fig.2.4. As can be seen, extremely large current density, which contributes to the reduction of the charging time, can be obtained by the RT-emitter, because the state density of the metal used as the source is very large and the thickness of the barrier is very thin.

The $J_0 - V_s$ characteristic shown in Fig.2.4 has a dip at V_s =4.3V. This is understood from the change in the energy distribution of emitted electrons shown in Fig.??. The figure shows the distribution of the energy E_z of the tunneling electrons for various applied voltage V_s. The electron energy E_z is measured upward from the bottom of the conduction band
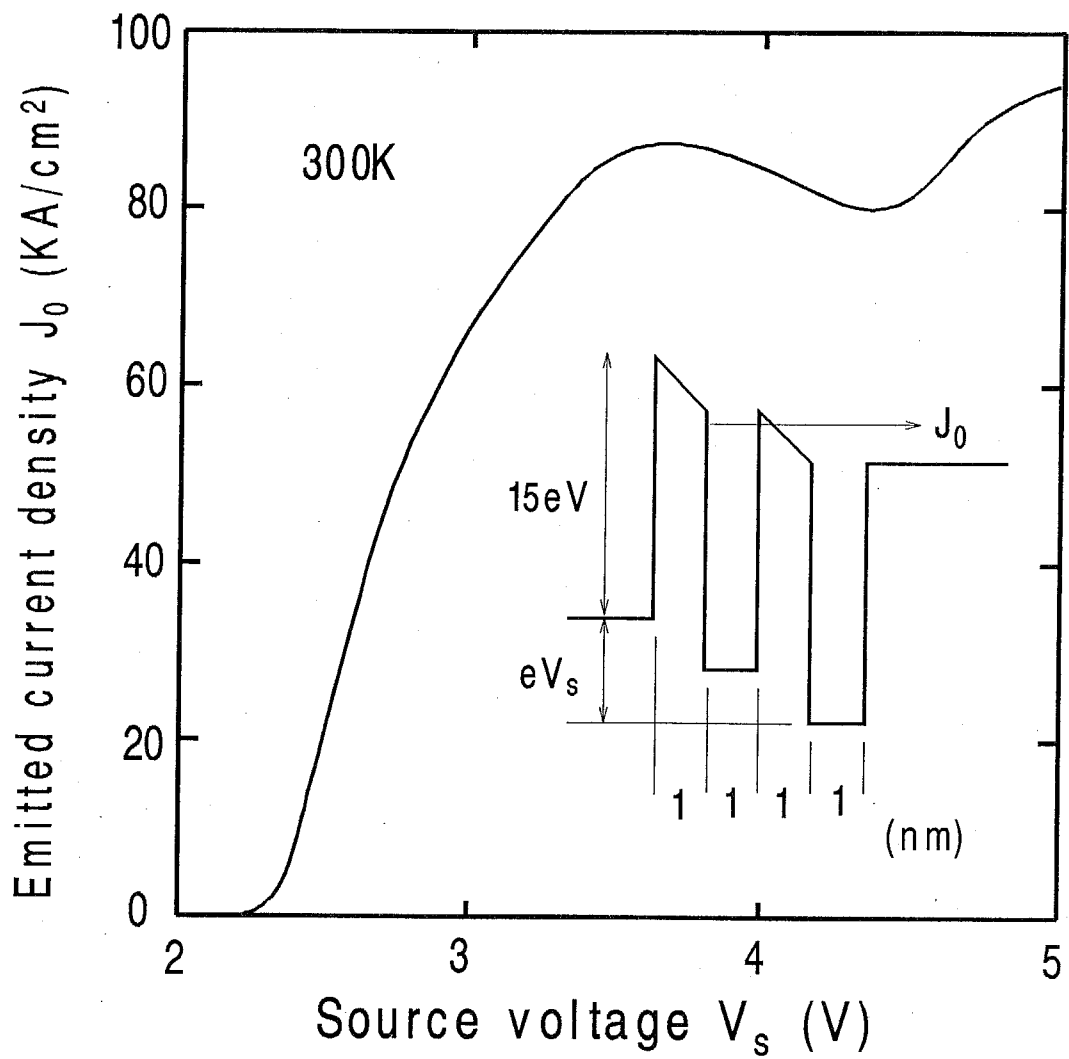
Fig. 2.4: The emitted current density from the RT-emitter as a function of source applied voltage V_s at 300K. The thickness of each barrier and well is 1nm.

of the insulator between the cathode and the grid. When V_s =2.1V, the Fermi level of the source metal E_{fs} is lower than the resonant point, and thus, the peak value of electron distribution is not so high, as shown in Fig.??. When V_s =2.5V, the Fermi level is nearly equal to the resonant revel, thus the distribution becomes δ-functionlike shape (a few meV-wide spike-like shape). Such a sharp distribution is obtained in spite of 300K because the barrier height for the incident electrons ($\sim$15eV$-$the first resonant level) is high. The Fermi level exceeds the resonant level when V_s >2.5V. However, the total amount of electrons and the current density are still increasing with V_s as shown in Fig.2.4. The second resonant peak appears near the Fermi level at V_s =3.0V, but this is substantially smaller the first resonant peak ($\sim 10^{-4}$). Therefore, the distribution is still nearly the δ-function. When V_s =3.5 and 4V, however, the height of the second resonant peak becomes comparable to that of the first one, and thus, the distribution deviates from the monoenergetic shape and becomes broad. Since the resonant levels move to deeper position, the emitted current density decreases. When V_s =4.5V, since the third resonant peak appears near the Fermi level, the emitted current density is again increasing with V_s.

Since the narrow energy distribution of emitted electrons is required in this device, the distribution at V_s =2.1-3V is preferred to that at V_s =3.5-5V though the current density is smaller. Thus, the source voltage V_s is assumed to be 3V in the estimation below, and the emitted current density J_0 is 65kA/cm^2. This current density is enough to drive the device in a high speed as shown later.
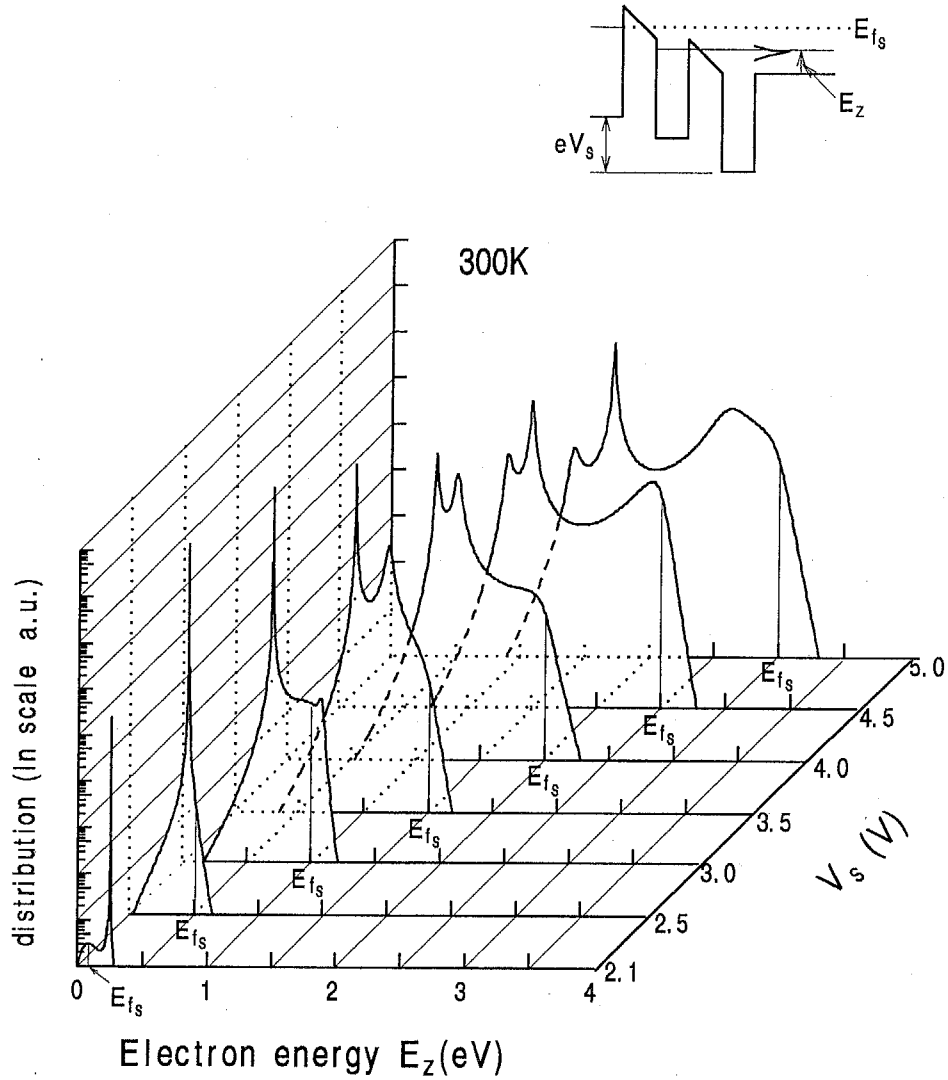
Fig. 2.5: Energy distribution of electrons emitted from the RT-emitter for various value of source voltage V_s. The electron energy along the z direction, E_z, is measured upward from the bottom of the conduction band of the insulator between the cathode and grid.

2.3.3 Static Characteristics

The plate current is controlled by varying the transmission coefficient T of the cathode-grid barrier with the voltage across the barrier V_g. In this case, T is a function of both the applied voltage V_g and the electron energy E_z, described as $T(V_g, E_z)$. Since the energy distribution of electrons from the emitter is very narrow, it is well approximated by δ-function with respect to E_z. Thus, the current density over the barrier J_p is obtained as follows.

$$
\begin{aligned}
J_p &= J_0 \int_0^\infty T(V_g, E_z) \delta(E_z - E_0) dE_z \\
&= J_0 T(V_g, E_0)
\end{aligned}
\tag{2.12}
$$

Since the electron wave reflection at the plate is quite small, J_p is nearly equal to the plate current density. Moreover, even if plate voltage V_p is changed, J_p is kept constant. This means that the J_p-V_p characteristics of this device have a saturation region.

Figure 2.6 shows the calculated results of the relation between the plate current density J_p and the grid voltage V_g. We assumed d_{cg} =40nm, d_g =1nm, and d_{gp} =20nm. The multiple peak $I - V$ characteristics of this device as shown in the figure is useful for a variety of signal processing and logic applications[1]. In addition, since the gradient between each peak and valley in Fig.2.6 is steep, the device used as an amplifier has a high transconductance which contributes to the reduction of the response time.
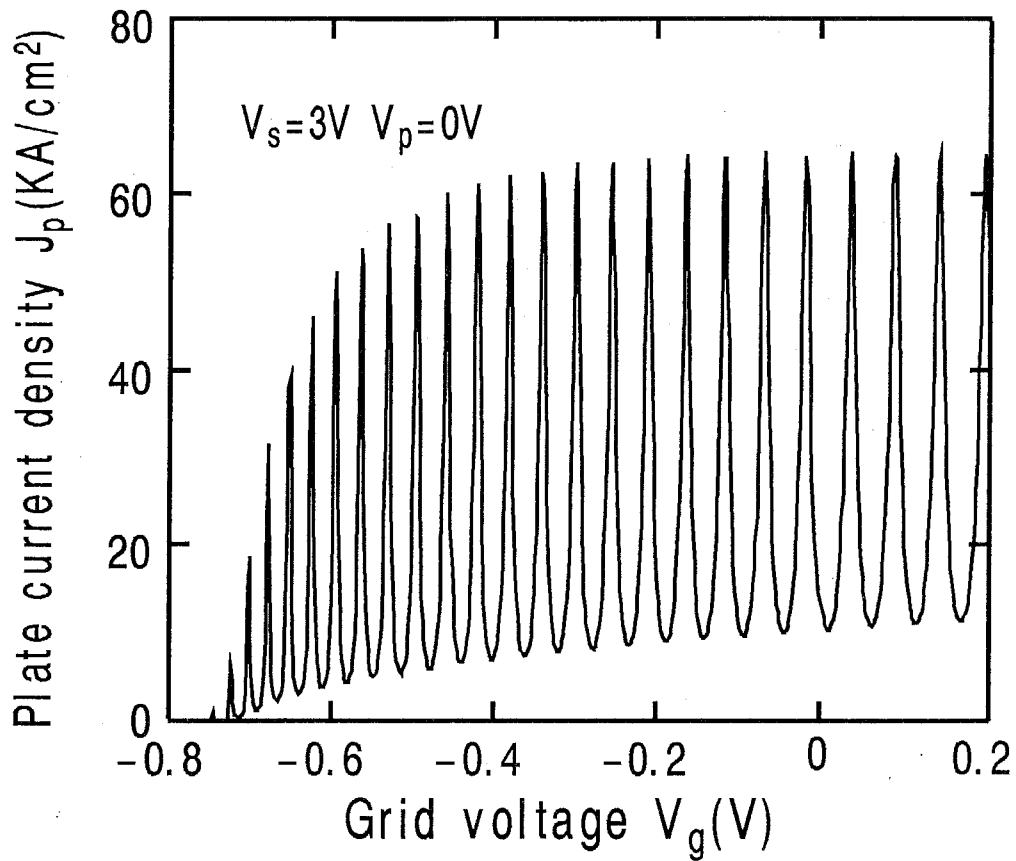
Fig. 2.6: Calculated result of static characteristics of the device (plate current density J_p vs. grid voltage V_g at source voltage V_s =3V and plate voltage V_p =0V). d_{cg} =40nm, d_g =1nm,d_{gp} =20nm.

2.4 Response Time

We analyze the response time of the device used as an amplifier. The operating point is settled in between the peak and valley in Fig.2.6, and the input signal is assumed to be smaller than the difference in V_g between the peak and valley. The response time of this device τ_T is given by the sum of the transit time and the charging time as

$$\tau_T = \tau_{TR} + \tau_{CR} \qquad (2.13)$$

where τ_{TR} is the sum of the transit times of each part, τ_{CG}, (from the cathode to the grid), τ_g (in the grid layer) and τ_{gp} (from the grid to the plate). τ_{CR} is the sum of the charging times of the cathode-grid and the grid-plate capacitances.

The transit time is given by the group delay time of the wavepacket going through the potential barriers and is expressed as the sum of the time for an electron to transit in real space without potential barriers and the group delay distortion[4, 25]. The latter has peaks corresponding to the peaks of the transmission coefficient T, because electrons at the resonance points go forward and back many times, resulting in a long time to transit through the potential barriers. In our device, however, large transconductances can be obtained at non-resonance points (i.e., the points in between the peak and the valley in Fig.2.6), where the group delay distortion is negligibly small. Thus, the transit time of the ballistic electron τ is given semiclassically by

$$\tau = \int_0^W \frac{dz}{v(z)} \qquad (2.14)$$

where v(z) is the group velocity of electron. Neglecting the space charge effect, each of the transit times is evaluated from this equation as

$$\tau_{cg} = \frac{d_{cg} m_0 (v_{g1} - v_0)}{eV_g} \qquad (2.15)$$

$$\tau_g = \frac{d_g}{v_{g2}} \qquad (2.16)$$

$$\tau_{gp} = \frac{1}{2} \frac{d_{gp} m_0 (v_p - v_{g3})}{e(V_p - V_g)} \qquad (2.17)$$

with

$$v_0 = \sqrt{2E_0/m_0}$$
$$v_{g1} = \sqrt{2(E_0 + eV_g)/m_0}$$
$$v_{g2} = \sqrt{2(E_0 + eV_g + V_0)/m_0}$$
$$v_{g3} = \sqrt{2(E_0 + eV_g + E_1)/m_0}$$
$$v_p = \sqrt{2(E_0 + eV_p)/m_0}$$

where d_g is the thickness of the grid layer (assumed here to be 1nm), d_{cg} (=40nm) and d_{gp} (=20nm) are the cathode-grid and the grid-plate spacings, respectively. E_0, V_0 (=15eV), and E_1 (1.6eV) are the kinetic energy of the electron, the conduction band and discontinuity, and the conduction band difference between CaF$_2$ and Si, respectively. The factor 1/2 has been multiplied in Eq.(2.17) to take into account the effect of the induction current as in an usual analysis of bipolar transistors.

The charging time τ_{CR} is given by

$$\tau_{CR} = \frac{1}{g_m} \left(\frac{\varepsilon_{CaF_2}}{d_{cg}} + \frac{\varepsilon_{Si}}{d_{gp}} \right) \qquad (2.18)$$

41

where ε_{CaF_2} and ε_{Si} are the dielectric constants of CaF_2 ($=6.76\varepsilon_0$) and Si ($11.8\varepsilon_0$), respectively. g_m is the transconductance and can be computed from Eq.(2.12) as follows.

$$g_m = \frac{\partial J_p}{\partial V_g} = J_0 \frac{T}{V_g} \qquad (2.19)$$

When the source voltage V_s is 3V and the plate voltage V_p is 0V, the maximum value of g_m is obtained from the gradient of the $V_g - J_p$ curve in Fig.2.6 to be $1.2 \times 10^7 S/cm^2$ at $V_g = -0.65V$ and $J_p = 38kA/cm^2$, and the electron velocities, v_0, v_{g1}, v_{g2}, v_{g3} and v_p are of the order of $10^7 cm/s$. From the above results, the transit time τ_{TR} and the charging time τ_{CR} at 300K are obtained as 0.14ps and 0.056ps, respectively. The response time τ_T, which is the sum of τ_{TR} and τ_{CR}, is 0.2ps and the cutoff frequency $f_T = 1/2\pi\tau_T = 800GHz$. In this case, the response time is dominated by the transit time. The situation is dependent of the device structure, and there is also a case in which the charging time dominates in the response time at a certain value of the cathode-grid thickness d_{cg}. If d_{cg} becomes smaller, the gradient between the peak and the valley of $V_g - J_p$ characteristics shown in Fig.2.6 becomes smaller, and thus, the transconductance g_m becomes smaller. The maximum value of g_m is approximately proportional to d_{cg}. Then, from Eq.(2.18), the charging time τ_{CR} is inversely proportional to d_{cg}^2. On the other hand, the transit time τ_{TR} is proportional to d_{cg}. For example, when d_{cg} decreases from 40nm to 20nm and the other values are kept same as the above assumption, τ_{TR} decrease to 0.078ps and τ_{CR} increases to 0.14ps. τ_T and f_T are calculated as 0.21ps and 740GHz, respectively.

2.5 Concluding Remarks

In this chapter, a novel transistor using ultra-thin metal and insulator layer was proposed. The wave nature of high-velocity ballistic electrons in metal-insulator heterostructure was utilized as the device operation principle. The metal-insulator combination contributes to obtaining high current density, low resistivity and small capacitance. Also, since this combination has the extremely high conduction band discontinuity, strong quantum interference can be obtained.

The static characteristics was analyzed, and the multiple peak $I - V$ characteristics was obtained. It was shown that this device has a potential of attaining subpicosecond response. Thus, this device is quite suitable for a variety of ultrahigh-speed signal processing and logic applications.

Chapter 3

Metal(CoSi$_2$)/Insulator(CaF$_2$) heteroepitaxy on Si(111)

3.1 Introduction

The subject of this chapter is the epitaxial growth technique for a nanometer-thick CoSi$_2$/CaF$_2$ layered structure on Si(111) substrates and the resistivity of a nm-thick CoSi$_2$ epilayer sandwiched by CaF$_2$.

In order to create CoSi$_2$/ CaF$_2$ multilayered structures, it is necessary to determine proper growth conditions for CaF$_2$ on CoSi$_2$ and CoSi$_2$ on CaF$_2$ separately, because these two materials require different growth conditions due to differences in their bonding mechanisms (CaF$_2$: ionic, CoSi$_2$: metallic). Epitaxy of CaF$_2$ /CoSi$_2$/ Si(111) and CoSi$_2$ /CaF$_2$ / Si(111) by the conventional molecular-beam epitaxy (MBE) technique have already been reported[26, 27, 28]. However, epitaxy of nanometer-thick CaF$_2$/ CoSi$_2$/ CaF$_2$ heterostructures, which is discussed here and is required for the devices in refs. [3] and [42], is much more difficult to perform because it is much easier to agglomerate CoSi$_2$ on CaF$_2$ than on Si(111), due to the difference in surface energies. This becomes problematic not only in the growth of CoSi$_2$ on CaF$_2$ but also in that of CaF$_2$ on

$CoSi_2/$ CaF_2.

3.1.1 Insulator epitaxy on Metal

In the growth of CaF_2 on $CoSi_2/$ CaF_2, the substrate temperature must be low enough ($< 500°C$) to avoid the agglomeration of $CoSi_2$ layers. However, we have found that epitaxial growth of CaF_2 on $CoSi_2$ is difficult at such low temperature using conventional MBE technique used for CaF_2 epitaxy on $Si(111)$[12, 29] because of the lack of migration energy for crystallization. In order to overcome this problem, we applied external kinetic energy to the evaporated CaF_2 particles to enhance migration with electron impact ionization and acceleration[30, 31].

3.1.2 Metal epitaxy on Insulator

In the case of the growth of $CoSi_2$ on CaF_2, the agglomeration of Co on CaF_2 is a critical problem if we use co-deposition of Si and Co. Thermodynamically, metal atoms tend to agglomerate on the insulator to minimize the large interface energy at the boundary between the two dissimilar materials. As is shown later, we introduced the two-step growth technique, i.e., solid phase epitaxy with a Si epitaxial layer grown on CaF_2 in the first step and Co deposited on Si in the second step, to avoid this problem.

3.2 Apparatus

The apparatus used in the epitaxial growth of $CoSi_2$ / CaF_2 is shown in Fig.3.1. The growth chamber is equipped with 3 evaporation sources,

each of which consists of a crucible, heater, and ionization and acceleration unit. Each source material was solid CaF_2, Si and Co. Crystalline quality can be evaluated by *in-situ* RHEED observation and evaporation rate was monitored and controlled using quartz mass sensors. The growth chamber was equipped with a liquid-nitrogen shroud and was evacuated by ion pump with a background pressure of less than 1×10^{-9} Torr. Fig.3.2 shows an evaporation source with ionization and acceleration unit. Crucibles were made of graphite for CaF_2, Co, and boron nitride for Si with an impurity content less than 5ppm. The nozzle of the crucible for CaF_2 and Si had a diameter and length of 1mm, while those for Co measured 2mm. Each source material in the crucible was heated by carbon heater to be melted and evaporated from the nozzle of the crucible. In the CaF_2 and Si growth, the evaporated particles are partially ionized by electron bombardment and accelerated toward the surface of the substrate by an applied field of a few kV. The kinetic energy given by this process to the deposited particles is expected to enhance migration[31].

The ionization ratio of CaF_2 ion beam as a function of acceleration voltage is shown in Fig.3.3. The ionization ratio was evaluated by growth rate and ion current density measured by Faraday cup. Ionization ratio was about 3% at impact ionization electron current I_e=400mA, acceleration voltage of ionization electron V_e=500V and acceleration voltage of ions V_a=2KV, which condition was typically used for the growth shown later. Ionization ratio of Si was almost the same as that of CaF_2. Co beam was not ionized and accelerated in $CoSi_2$ solid phase epitaxy because any advantage of acceleration was not observed.
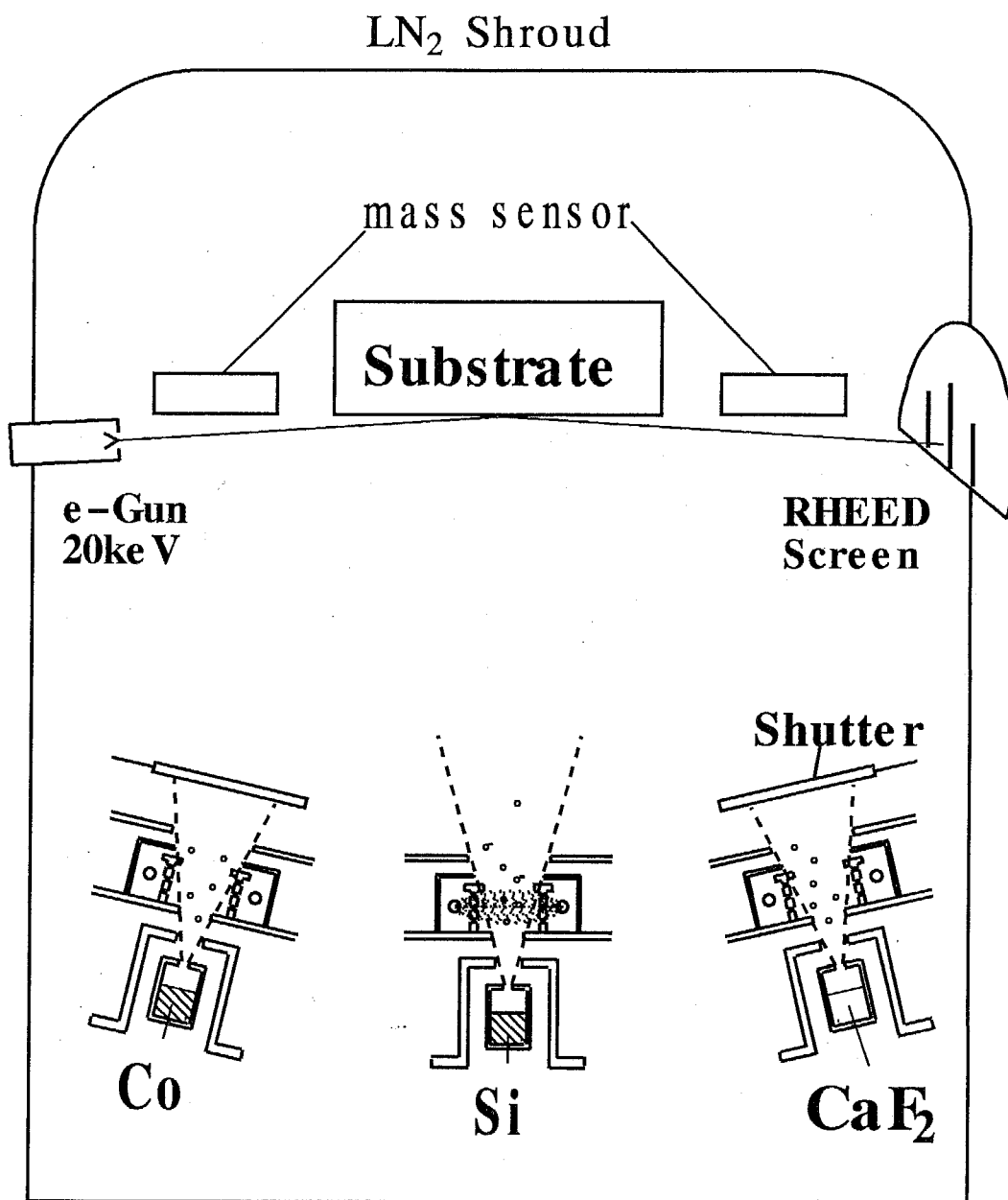
Fig. 3.1: Schematic view of the growth chamber equipped with 3 evaporation sources with ionization and acceleration units used in this study. Crystalline quality can be evaluated by *in-situ* RHEED observation and evaporation rate was monitored and controlled using quartz mass sensors.
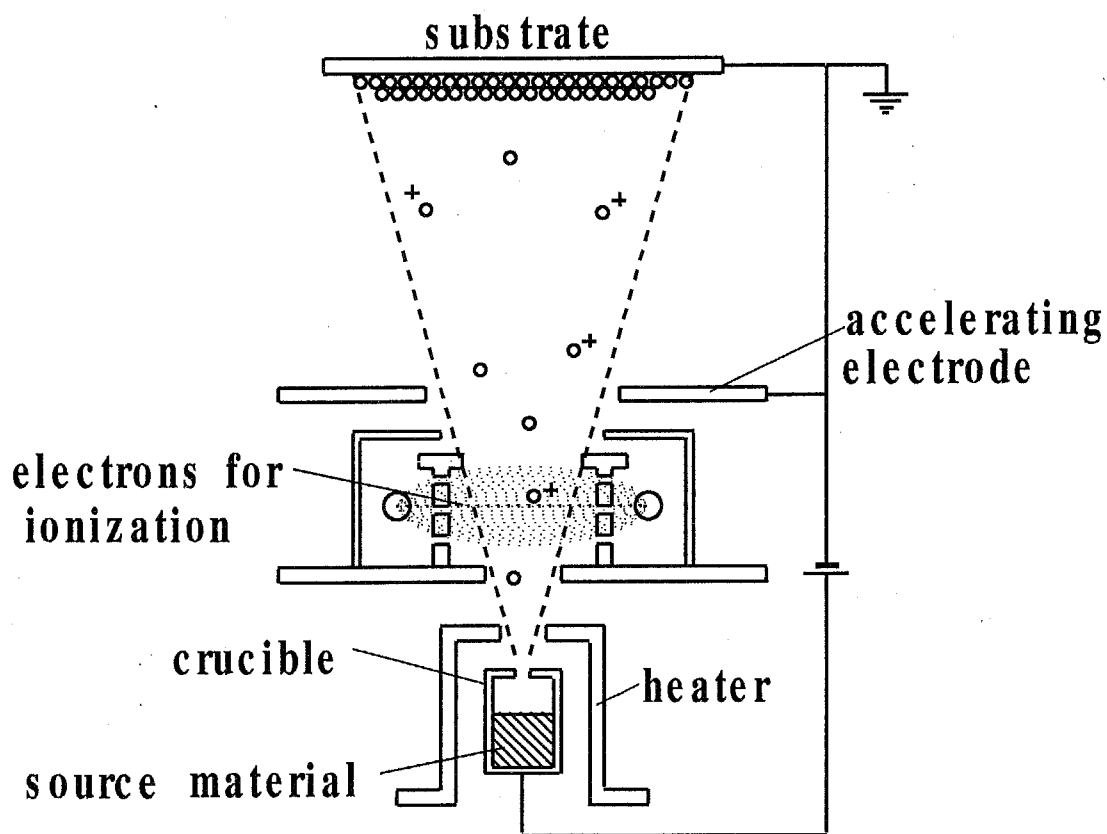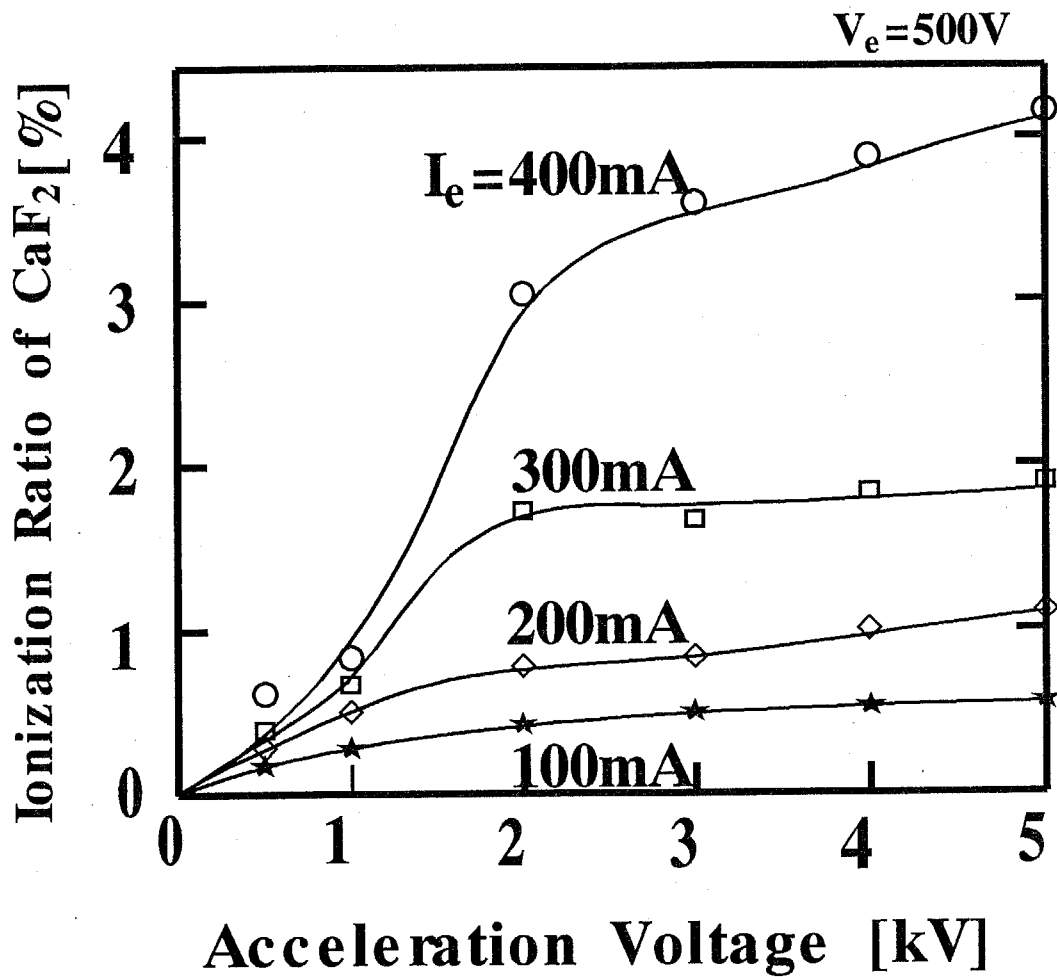
Fig. 3.2: Schematic view of the evaporation source with ionization
and acceleration unit. The evaporated particles are par-
tially ionized by electron bombardment and accelerated to-
ward the surface of the substrate by an applied field of a
few kV.

Fig. 3.3: Ionization ratio of partially ionized CaF_2 beam as a function of acceleration voltage V_a for different ionization electron current I_e. Ionization ratio was around 3% at V_a=2kV and I_e=400mA.

3.3 Low temperature CaF$_2$ epitaxy by partially Ionized Beam Epitaxy

3.3.1 CaF$_2$ epitaxy on Si(111)

It is known that CaF$_2$ grows epitaxially on Si(111) substrates at 600°C–800°C by molecular beam epitaxy (MBE) [12, 29]. However, in the formation of CaF$_2$/CoSi$_2$ multilayers, which requires the growth of CaF$_2$ on CoSi$_2$ and *vice versa*, it is necessary to grow CaF$_2$ epitaxially at temperatures less than 500°C so as to avoid the formation of pinholes in CoSi$_2$ layers due to thermal deformation. But in conventional MBE growth, CaF$_2$ on the Si(111) substrate will become a polycrystal if the temperature is decreased to such low levels. Ionized cluster beam growth technique is one of the candidates to overcome this problem because an external kinetic energy can be applied so as to artificially enhance migration to the evaporated particles [32]. We report here the low-temperature ($\sim$420°C) epitaxial growth of CaF$_2$ layers on Si(111) by ICB epitaxial technique as a first step to realize metal/insulator single-crystal ultrathin layers.

The principle of ICB technique is as follows. Clusters which consist of 100$\sim$1000 particles are ionized by electron bombardment and accelerated toward the surface of the substrate by an applied field of a few kV. The kinetic energy of the deposited particles is expected to enhance migration, which will lead to the epitaxial growth of the deposited layers [30].

We used an ICB crucible made of graphite with impurities of less than 5ppm. The nozzle of the crucible had a diameter of 1mm and a length of 1mm. The ICB chamber had a liquid-nitrogen shroud and was evacuated by ion pump with a background pressure of less than 1 $\times$

10^{-9}Torr. A polished Si substrate with (111) orientation was chemically cleaned and protective oxide layer was grown [33] and was loaded into the ICB chamber through a load lock. Subsequently, the substrate was heated to a temperature of around 860°C by the radiant heat of a tantalum heater for 30 minutes to remove the protective oxide layer. Then the substrate temperature T_s was reduced to the growth temperature, i.e., 420°C. The pressure in the chamber during the growth was maintained below 2×10^{-8}Torr. CaF_2 layers were grown at the electron ionization current I_e =100–400mA and the acceleration voltage V_a =0–7kV. Around 60nm of CaF_2 was grown at a growth rate of 3nm/min.

Reflection high energy electron diffraction (RHEED) patterns of two CaF_2 samples grown at $T_s = 420$°C, $V_a = 3$kV, I_e =100 and 400mA are shown in Fig.3.4. For $I_e = 100$mA , the CaF_2 layer shows a polycrystalline nature, as can be observed from the ring pattern in Fig.3.4(a) . On the other hand, when $I_e = 400$mA, a streaky pattern was observed, as shown in Fig.3.4(b), which indicates that single crystallinity of CaF_2 layers was obtained even at a low growth temperature of 420°C. We attribute this result to the enhancement of migration due to the increase of ionization. The ionization ratio, i.e., the ratio of ionized molecules in the CaF_2 beam, was a few tens of percent at $I_e = 400$mA and $V_a = 3$kV, which was about nine times that at $I_e = 100$mA.

Figure 3.5 shows $\langle 111 \rangle$ axial Rutherford backscattering (RBS) channeling χ_{min} of CaF_2 layers as a function of acceleration voltage at I_e of 400mÅ with the T_s of 420°C. It is seen that the best crystalline quality was obtained when the acceleration voltage V_a was 1~2kV, whereas it
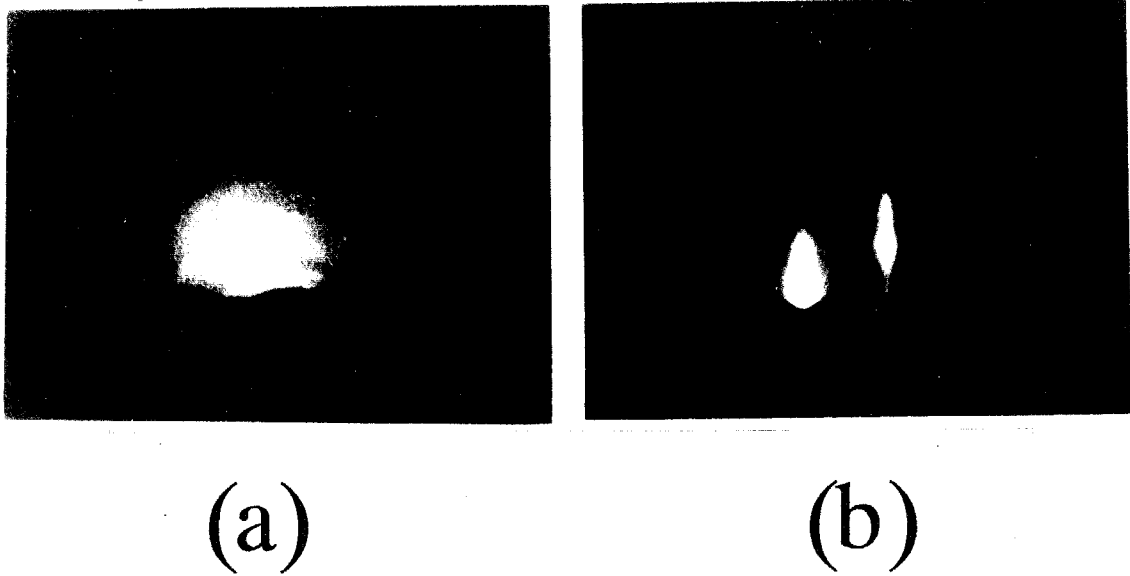
(a)　　　　　　　　　(b)

Fig. 3.4: RHEED pattern of CaF_2 on Si(111) grown at 420°C by ion
assisted epitaxy with acceleration voltage V_a=3kV
(a) electron current for ionization I_e=100mA.
(b) I_e=400mA

becomes worse when the V_a is higher than 2kV . This is probably because the ions with high energy, which destroy the crystal structure of the CaF_2 layers, increase with the increase of acceleration voltage.

In conclusion, we have shown that CaF_2 grows epitaxially $(\chi_{min} \sim 13\%)$ on Si(111) substrates using the ICB technique at a low temperature of 420°C, at which temperature it is difficult to obtain epitaxial CaF_2 layers using the conventional MBE technique. This technique is particularly useful for the epitaxial growth of CaF_2 on metal $CoSi_2$ epitaxial layers because $CoSi_2$ is easily damaged by thermal deformation at high temperature.

3.3.2 CaF_2 epitaxy on $CoSi_2$

A 1nm-thick $CoSi_2$ layer was formed by the deposition of Co on Si(111) substrate and solid phase epitaxy near room temperature (<100°C) [34]. The deposition rate of Co was about 0.5nm/min. Subsequently a 4nm-thick CaF_2 layer was grown on the $CoSi_2$ by ion assisted epitaxy at the substrate temperature T_s =450°C , acceleration voltage V_a =2kV and impact ionization electron current I_e =400mA. A streaky RHEED pattern was observed as shown in Fig.3.6, which indicates that a single-crystalline CaF_2 layer was obtained even at 450°C on the $CoSi_2$ due to enhancement of migration by the acceleration energy. If the acceleration voltage is higher than 2kV, damage of the crystal tends to increase [31] due to accelerated particles with high energy, therefore V_a =2kV is used for CaF_2 throughout the experiment.
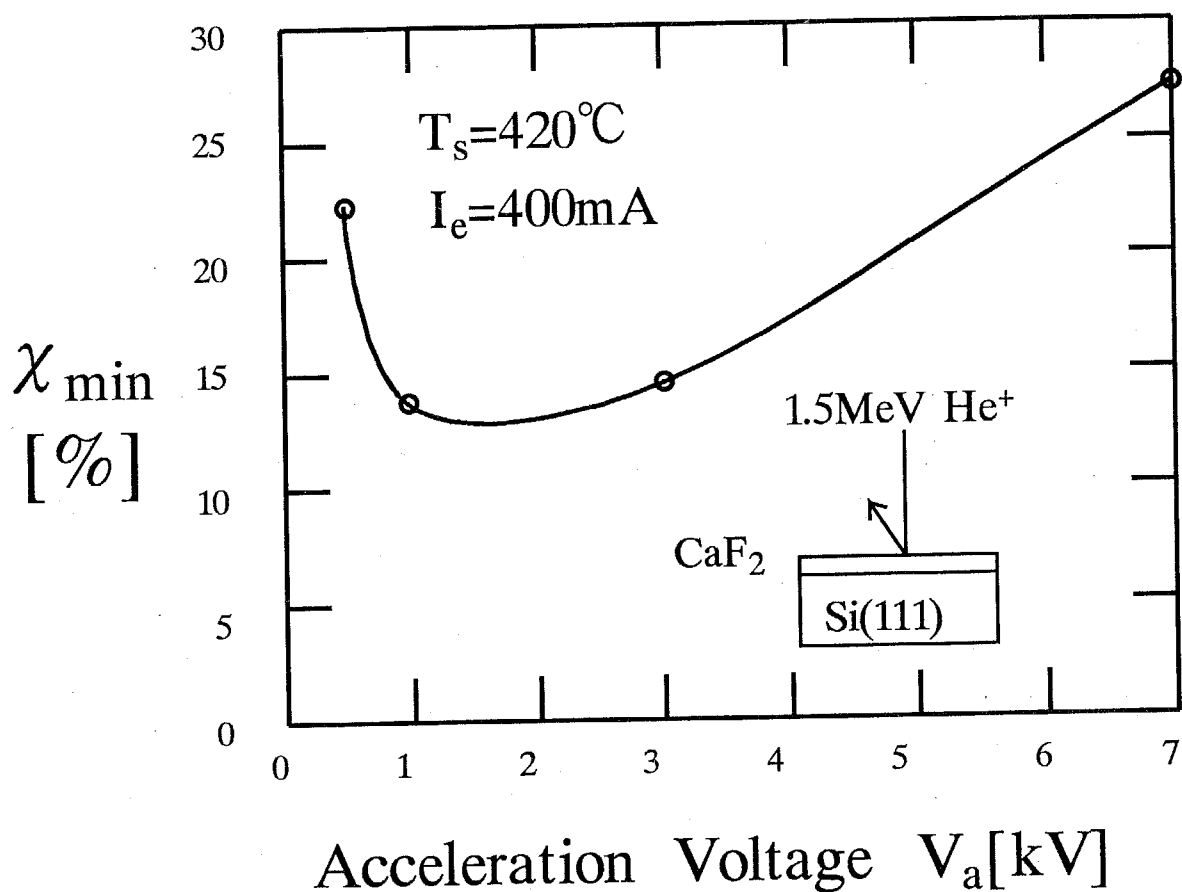
Fig. 3.5: The $\langle 111 \rangle$ axial Rutherford backscattering (RBS) channeling χ_{min} of CaF_2 layers as a function of acceleration voltage at $I_e = 400$mA with substrate temperature of 420°C.
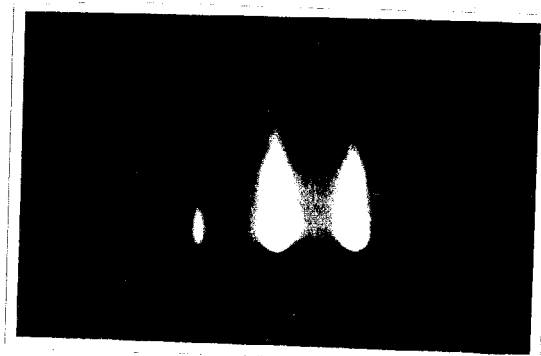
Fig. 3.6: RHEED pattern of 4nm-thick CaF_2 on $CoSi_2/Si(111)$ grown by ion assisted epitaxy with acceleration voltage V_a=2kV and ionization current I_e=400mA.

3.4 CoSi$_2$ epitaxy on CaF$_2$

3.4.1 Codeposition method

For the growth of CoSi$_2$ on the CaF$_2$, we initially investigated the co-deposition method. Co and Si were evaporated simultaneously on the CaF$_2$ at a ratio of 1:2, at T_s =500°C. Only the Si beam was ionized and accelerated with I_e =350mA and V_a =2kV. The Co beam was not ionized because any advantage of ionization and acceleration was not observed. The deposition rate of each material was monitored and controlled using quartz mass sensors. The growth rate was around 0.7nm/min. RHEED pattern and SEM view of the surface of CoSi$_2$ grown by co-deposition are shown in Fig.3.7(a). A broad spot pattern of RHEED indicates that the CoSi$_2$ layer obtained here was barely single-crystalline, but, as can be seen from the SEM view of the surface, many agglomerates presumed to be Co were observed. As long as we use the co-evaporation, it seems difficult to avoid the agglomeration of Co on the CaF$_2$ at T_s =500°C because the difference between the surface energy of CaF$_2$ and Co is too large.

3.4.2 Two-step growth

To solve this problem, we introduced the two-step process as follows. Firstly, epitaxial 4 monolayer(ML) Si was formed on CaF$_2$ at T_s =600°C, I_e =350mA and V_a =2kV. Subsequently, Co was deposited on the Si layer near room temperature (<100°C) without acceleration to grow epitaxial 2ML CoSi$_2$ by solid phase epitaxy. Using the two-step growth, the agglomeration of Co was efficiently suppressed because the difference be-
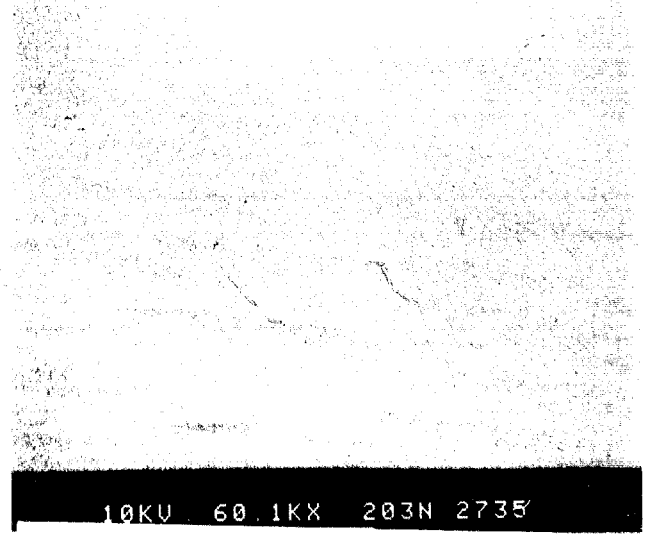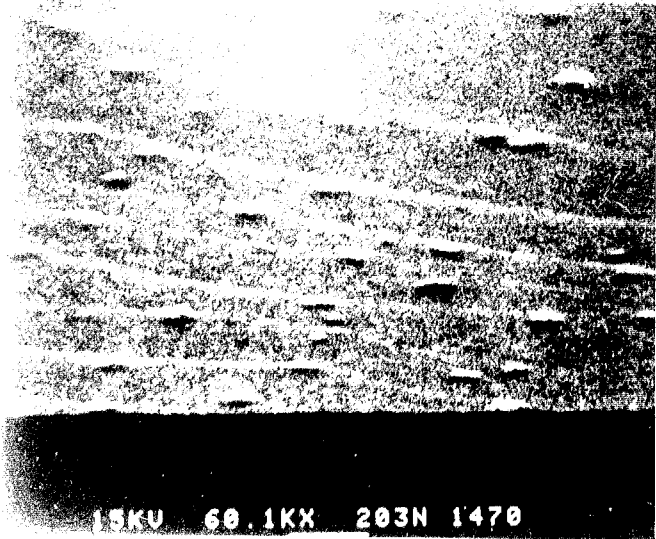
Fig. 3.7: RHEED patterns and SEM surface view of $CoSi_2$ on CaF_2
grown by
(a) co-deposition process, and
(b) two-step process.

tween the surface energies of Co and Si is smaller than that between Co and CaF_2. $CoSi_2$ layers thicker than 2MLs were obtained by repeating this process with the same condition except T_s =550°C at the growth of Si layers to avoid agglomeration of $CoSi_2$ already formed. RHEED pattern and a SEM view of 2nm-thick $CoSi_2$ grown by the two-step growth are shown in Fig.3.7(b), which indicates that the crystallinity and flatness are obviously improved compared with $CoSi_2$ obtained by co-deposition shown in Fig.3.7(a).

3.4.3 $CoSi_2$/CaF_2 superlattice structure

Figure 3.8 shows a cross-sectional transmission electron microscopy (TEM) lattice image of a 2.7nm-thick $CoSi_2$ layer sandwiched between CaF_2 layers. Bright lines indicates one monolayer of (111) orientation of fluorite structure and distance between each line is 0.31nm. This image clearly confirms the epitaxial growth between $CoSi_2$ and CaF_2 although the epitaxial relation between each layer, i.e., type A or type B, is not clear at present. Undulation of some monolayers observed in both $CoSi_2$ and CaF_2 layers as well as at the interface is probably due to dislocations in the underlayer.

3.5 Electric conductance of nanometer-thick $CoSi_2$ sandwiched by CaF_2

3.5.1 Resistivity of as-grown sample

In electron devices, low resistivity of the terminals is essential for high speed operation. Also, the resistivity is a measure of the crystalline qual-
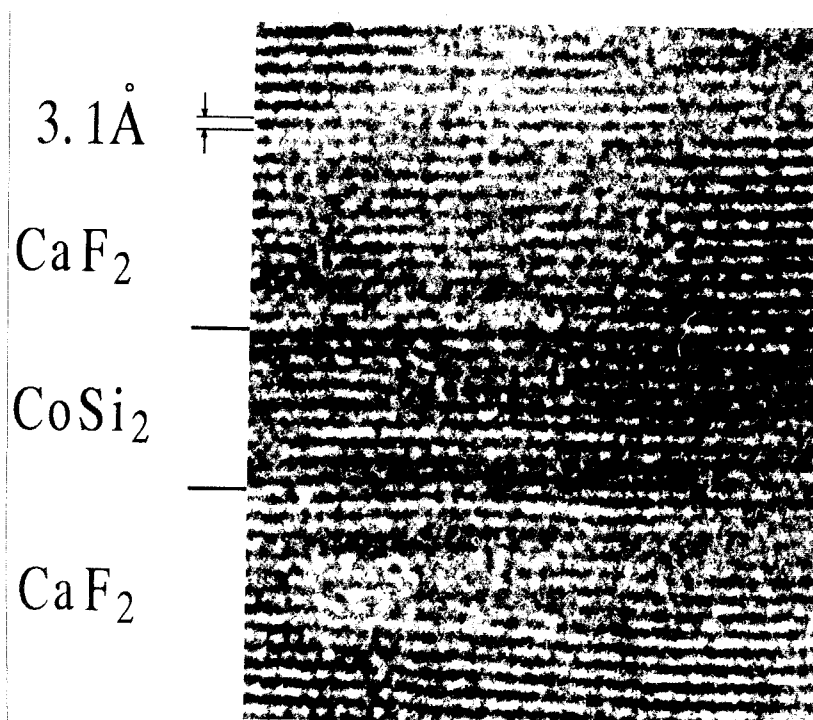
3.1Å

CaF$_2$

CoSi$_2$

CaF$_2$

Fig. 3.8: Cross sectional TEM image of a 2.7nm CoSi$_2$ layer sandwiched between CaF$_2$ layers. Each bright line indicates one monolayer of (111) orientation of fluorite structure. (Courtesy of JEOL)

ity of the grown layers. Here, resistivity was investigated for the $CoSi_2$ epilayer sandwiched by CaF_2. The growth conditions for the samples were the same as that described in the previous section. The layer structure of the samples for resistivity measurement was CaF_2 /$CoSi_2$/ CaF_2/ $Si(111)$, as shown schematically in Fig.3.9. The thickness of CaF_2 underlayer on $Si(111)$ substrate was 30nm and that of $CoSi_2$ layer was 1.2−4.0nm. The CaF_2 protection layer on the $CoSi_2$ was 20nm-thick. Ohmic contact to $CoSi_2$ metal layer was fabricated by photolithography and selective wet chemical etching process as shown in Fig.3.10. Firstly, 100nm-thick SiO_2 layer was grown on the CaF_2 /$CoSi_2$/ CaF_2/ $Si(111)$ structure by chemical vapor deposition. The SiO_2 layer was etched by buffered HF (7% wt.) and subsequently CaF_2 underlayer was etched by H_2SO_4 (98% wt.) : H_2O = 1:4 at room temperature. Etching rate was 2nm/sec and 1nm/sec, respectively. The diameter of an Au electrode for contact to $CoSi_2$ layer was 20μm and the distance between electrodes was 1mm. Resistivity was measured by the four-terminal method at room temperature as shown in Fig.3.9. Three samples with 1.2nm-, 1.8nm-, 4.0nm-thick $CoSi_2$ layers were measured. Figure 3.11 shows measured resistivity of nm-thick $CoSi_2$ epilayer as a function of layer thickness. The minimum resistance ρ_{min} ~60$\mu\Omega$cm was obtained for 1.8nm-thick $CoSi_2$. The increase of ρ for the thinnest layer can be explained by electron scattering at the $CoSi_2$−CaF_2 interface as proposed in the case of the Si-$CoSi_2$ interface [35, 36, 37, 38] although details are not clear at present. On the other hand, the increase of ρ for the thickest layer implies that the crystalline quality of the samples becomes worse with thickness and

remains to be improved, because the RHEED pattern of 4nm-thick $CoSi_2$ was the broadest of the three samples.

3.5.2 Effect of Annealing

Insufficient crystalline quality of the $CoSi_2$ layers mentioned above was improved by the *in-situ* thermal annealing. Figure 3.12 shows the distribution of resistivity for 2nm-thick $CoSi_2$ layers with different *in situ* annealing temperature. 64 sets of four-terminal measurements were carried out at room temperature for each wafer. The structure of the samples was the same as that of non-annealed samples mentioned above. Improvement of the resistivity by annealing is clearly observed in Fig.3.12.

As the annealing temperature was increased from 600°C to 860°C, the number of lower resistivity data increased. At annealing temperature 860°C, ρ_{min} ~$30\mu\Omega$cm (sheet resistivity = $167\Omega/\square$) was obtained and more than 50% of the data distributed below $60\mu\Omega$cm, while only 6% in the case of non-annealed samples. This is probably because crystallization of $CoSi_2$ was promoted by annealing without metal agglomeration. During the growth, substrate temperatures higher than 600°C bring upon agglomeration of $CoSi_2$. On the other hand, after the growth of CaF_2 protective layer on $CoSi_2$, agglomeration of $CoSi_2$ is presumed to be avoided even at 860°C because the dangling bonds of the $CoSi_2$ surface were terminated by CaF_2, which results in the reduction of the interface energy compared to $CoSi_2$ without a CaF_2 overlayer.

The resistivity of nm-thick $CoSi_2$ on Si(111) substrate has been already reported in refs. [39, 35, 36, 37, 38]. The result obtained in the present
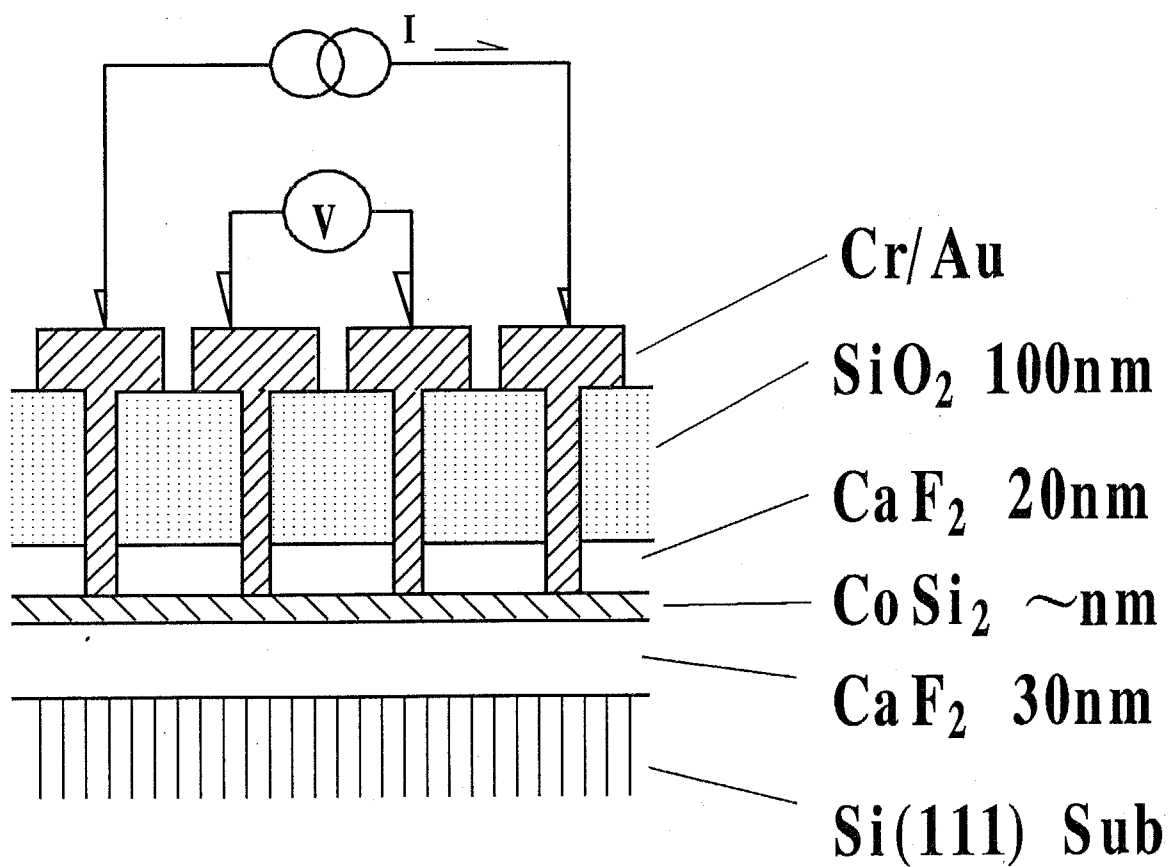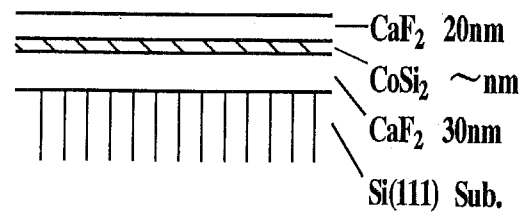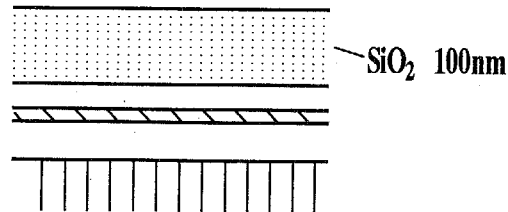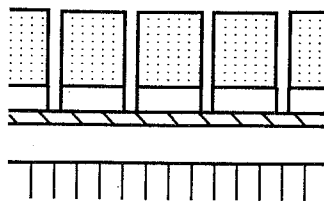
Fig. 3.9: Schematic view of the structure for resistivity measurement. Diameter of an Au electrode for contact to $CoSi_2$ layer was $20\mu m$ and distance between electrodes was 1mm. Measurement was carried out with HP-4142B.
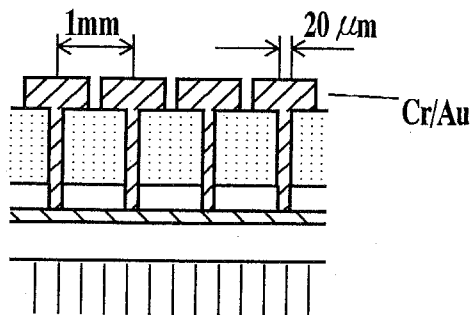
1) as grown sample

CaF₂ 20nm
CoSi₂ ~nm
CaF₂ 30nm
Si(111) Sub.

2) SiO₂ CVD deposition

SiO₂ 100nm

3) Selective wet etching

SiO₂: BHF(7%) ~45sec.
CaF₂: H₂SO₄:H₂O=1:4 ~20sec.

4) Electrode: Cr/Au

Au evaporation
lift-offprocess

1mm   20 μm
Cr/Au

Fig. 3.10: Fabrication process of ohmic contact to CoSi₂ buried layer for four-terminal resistivity measurement. SiO₂ protection layer was grown by chemical vapor deposition (CVD) after the growth of CaF₂/CoSi₂/CaF₂/Si(111). Au/Cr contact electrode was fabricated by selective wet chemical etching and photolithography followed by lift off process.
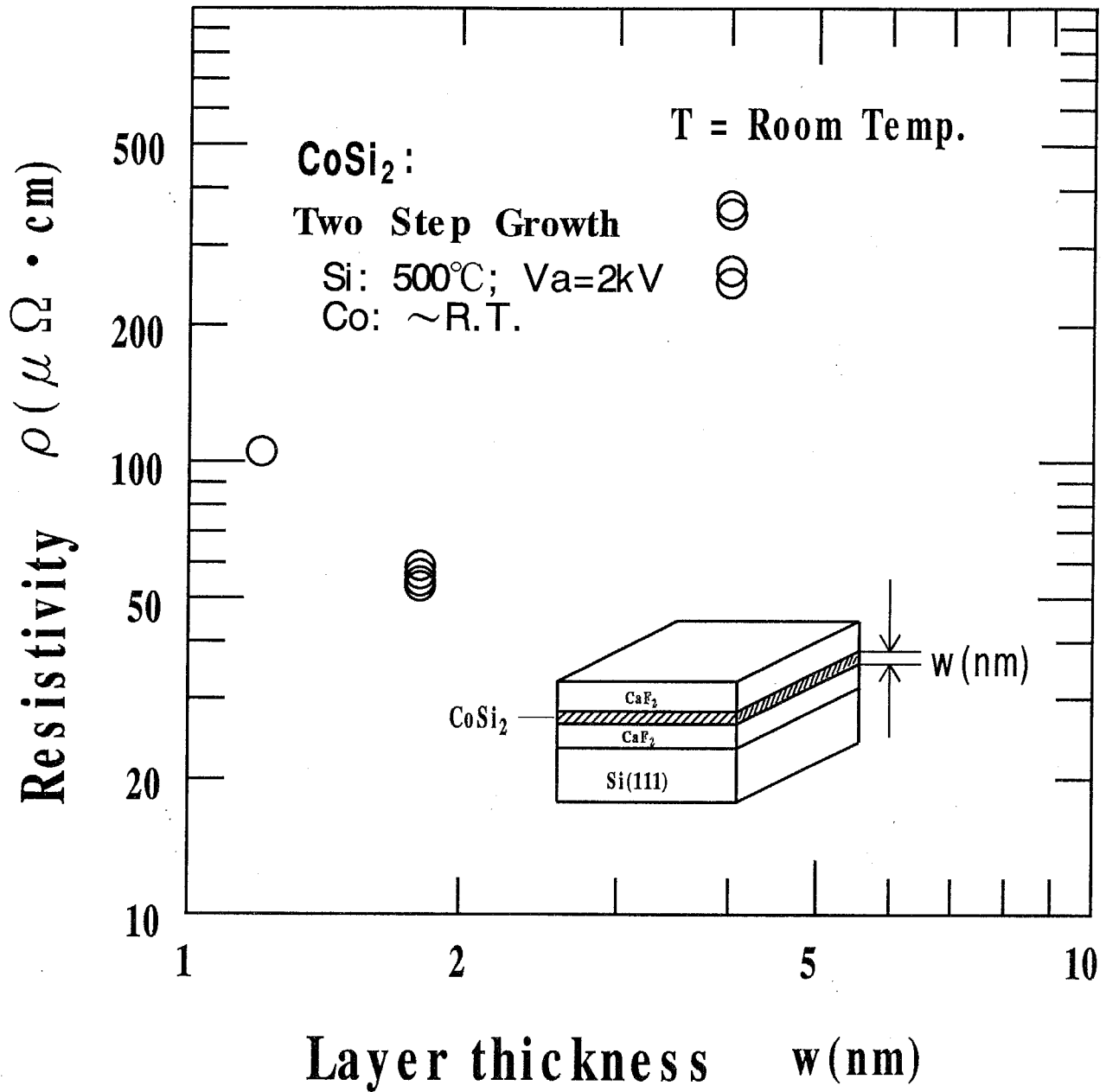
Fig. 3.11: Resistivity of nm-thick CoSi$_2$ epilayer sandwiched by CaF$_2$ as a function of layer thickness, which was measured by four-terminal method at room temperature.

1.8nm CoSi$_2$

T=Room Temp.

a) as grown

b) annealed at 600°C

c) annealed at 860°C
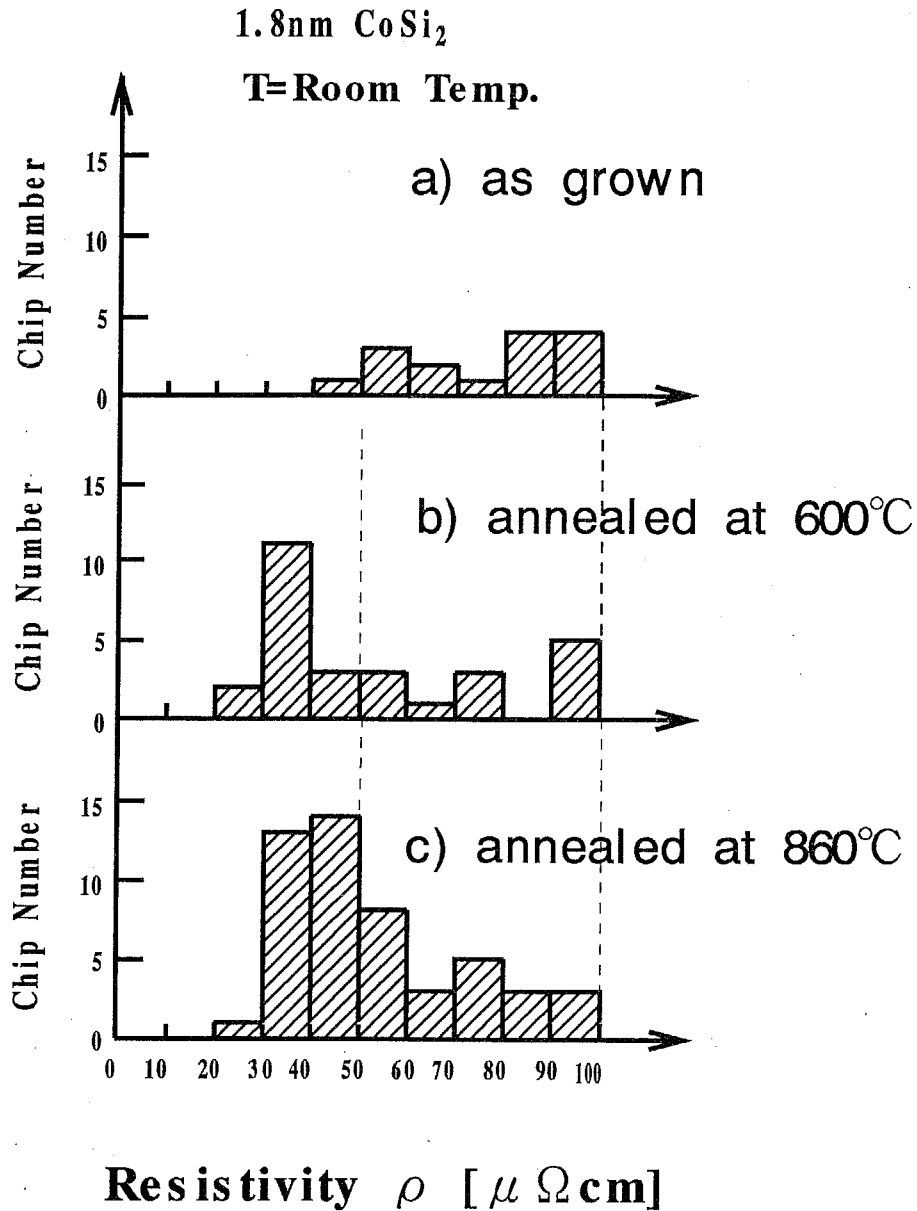
Resistivity ρ **[$\mu\,\Omega\,$cm]**

Fig. 3.12: Distribution of resistivity of 2nm-thick CoSi$_2$ layers with different *in situ* annealing temperature. 64 sets of four-terminal measurements were carried out at room temperature in each wafer. Results of ρ <100$\mu\Omega$cm are shown.

study for 2nm-thick $CoSi_2$ sandwiched by CaF_2 is the same order as that of 2nm-thick $CoSi_2$ layers on Si(111) substrates ($\sim80\mu\Omega cm$).

3.6 RHEED oscillation during CaF_2 growth on Si(111)

Recently, we have investigated nanometer-thick multilayered heteroepitaxy of $CoSi_2/CaF_2$ on Si(111) [45, 46] and demonstrated negative differential resistance of metal-insulator(MI) resonant tunneling diode [40] and transistor action of MI-hot electron transistor [41]. In order to realize metal-insulator electron-resonance three terminal device [42], layer thickness control is essential for designing the quantum resonance energy level. As a first step of layer-by-layer epitaxy of $CoSi_2/CaF_2$ heterostructure, we report the observation of RHEED intensity variation during CaF_2 growth on Si(111) substrate by means of ion-assisted epitaxy as well as conventional non-ion-assisted growth.

3.6.1 RHEED measurement system

RHEED features were monitored using a charge coupled device (CCD) video camera and digital image processing system. Background intensity on RHEED screen from substrate heater, crucible and acceleration unit was subtracted from RHEED intensity data by this system, so that high-contrast RHEED pattern can be obtained even during the ion-assisted growth. RHEED intensity was defined as integration of intensity over one of the brightest streaks in RHEED patterns.

3.6.2 Experiment & result

Firstly, we investigated RHEED intensity variation during CaF_2 growth on Si(111) without ionization and acceleration. Prior to opening the CaF_2 source a streaked 7×7 pattern of Si(111) was observed and intensity of the brightest streak of the RHEED pattern was monitored. Upon opening the CaF_2 shutter the pattern changes to a streaked 1×1 CaF_2(111) pattern. Figure 3.13(a) shows the RHEED intensity variation during the growth and its pattern after the growth at substrate temperature T_s=740°C, the growth rate $\sim 9\times10^{-3}$nm/sec. At early stage of the growth, RHEED intensity immediately got brighter and then gradually decreased to constant level. RHEED pattern in Fig.3.13(a) indicates the grown CaF_2 was single-crystalline. However, intensity oscillation related to CaF_2 growth was not observed throughout the growth at T_s=740°C. We have found that RHEED oscillation is not observed at T_s >600°C in non-acceleration growth.

Figure 3.13(b) shows the RHEED intensity variation during the growth and its pattern after the growth at T_s=480°C. As shown here, RHEED intensity oscillation at initial stage of the growth was observed probably due to the two dimensional (2D) growth mode instead of step growth mode. However, as shown in the RHEED pattern, obtained CaF_2 crystal implied poly-crystalline CaF_2 because of the lack of migration energy. In order to obtain single-crystalline CaF_2, we enhanced migration by means of ionization and acceleration of evaporated CaF_2 particles [31].

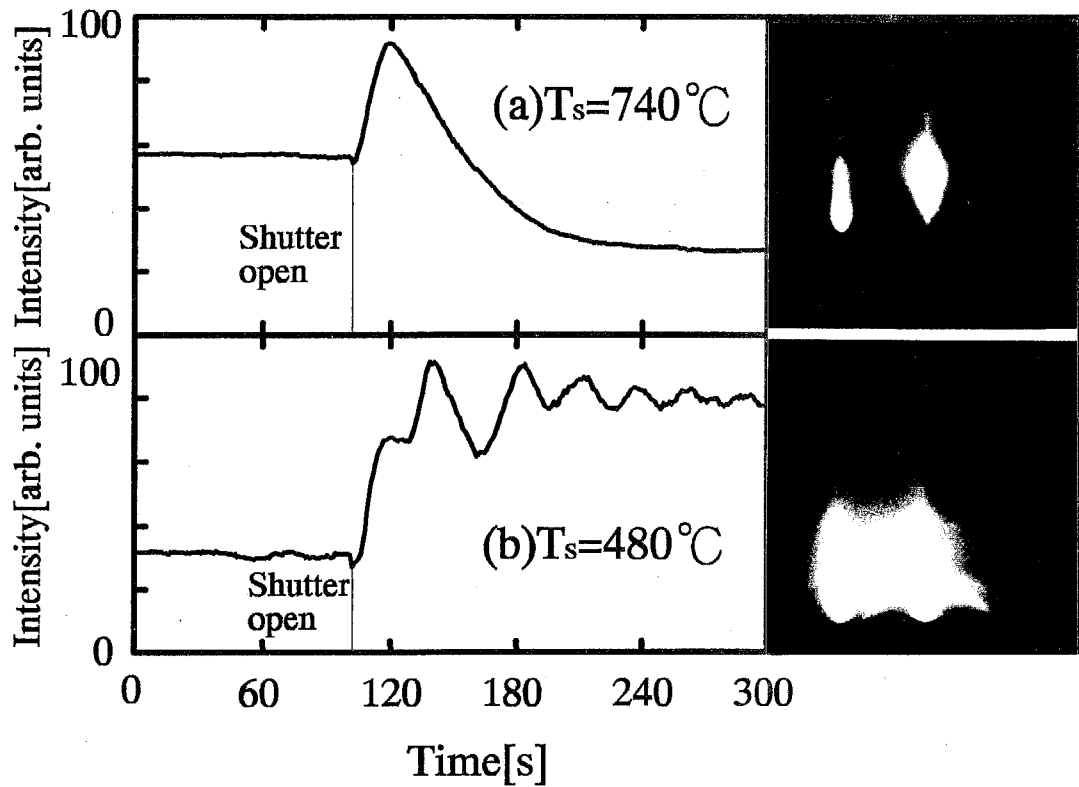Figure 3.14 shows the RHEED intensity variation and its pattern after the growth at T_s=440°C with the acceleration voltage of 2KV, and

Fig. 3.13: (a) RHEED intensity variation during the growth and its pattern after the growth at substrate temperature T_s=740°C and the growth rate was 9×10^{-3}nm/s.
(b) At T_s=480°C.

the ionization ratio $\sim 2\%$. About five period of RHEED oscillation at the early stage of the growth was observed and the RHEED pattern after the growth was a sharp-streak, which indicates that obtained CaF_2 was single-crystalline due to enhancement of migration. The damping of the RHEED oscillation observed here was probably because the growth mechanism gradually changed from 2D mode to 3D mode. However, we have found that RHEED feature was kept in sharp streak instead of spot streak even after RHEED oscillation was damped, which indicates that the fluctuation of the surface was suppressed to quite low level.

These results indicate that two dimensional growth was dominant at the early stage of the growth in the use of partially ionized beam epitaxy of CaF_2 at $T_s = 440°C$ and also that the 3D growth gradually becomes dominant after several period of the 2D growth. In the non-acceleration condition, although the RHEED oscillation was observed at $T_s = 480°C$, poly-crystalline CaF_2 was grown.

3.6.3 Conclusion

In conclusion, we have observed RHEED intensity oscillation at initial stage of partially ionized beam epitaxy of CaF_2 on $Si(111)$ at growth temperature $T_s = 440°C$ with the acceleration voltage $V_a = 2KV$ and the ionization ratio of a few percent. To our knowledge, this is the first report of the observation of RHEED intensity oscillation for the CaF_2 growth on $Si(111)$. During and after the growth, RHEED pattern of the CaF_2 shows single-crystalline nature in our epitaxial technique, whereas polycrystalline CaF_2 is grown without ionization and acceleration at such
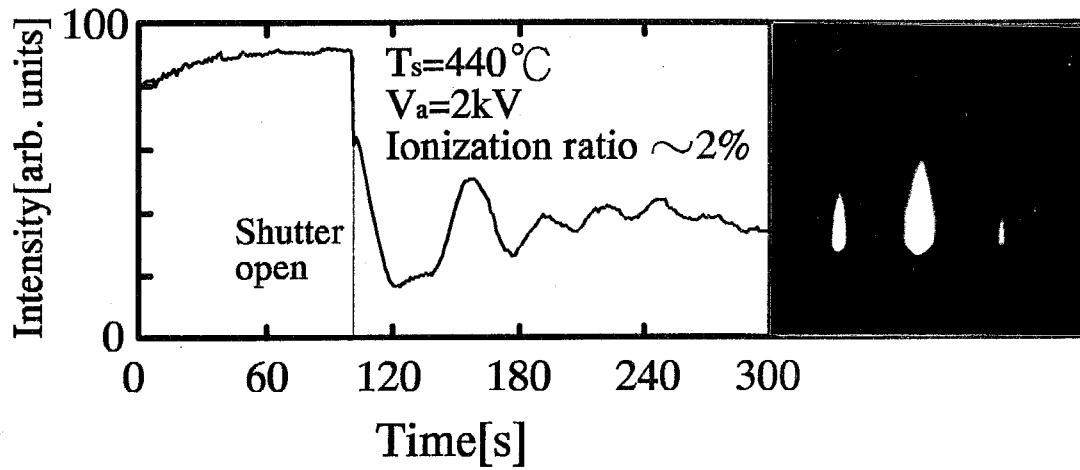
Fig. 3.14: The RHEED intensity variation and RHEED pattern after the growth at T_s=440°C, acceleration voltage V_a=2kV, ionization ratio ~2%.

low temperature. At high temperature range (>600°C), although single-crystalline CaF$_2$ is obtained without acceleration, RHEED oscillation is not observed during the growth. Intensity oscillation obtained here can be utilized in the in-situ monitoring of a few monolayer thick CaF$_2$ growth for metal-insulator nanometer-thick heterostructure devices [40, 41, 43, 44].

3.7 Concluding Remarks

We have reported epitaxial growth of metal(CoSi$_2$)/ insulator(CaF$_2$) nanometer-thick layered structures on Si(111) with ion assisted epitaxy for CaF$_2$ and two-step growth of CoSi$_2$. The agglomeration of Co was a problem for the growth of CoSi$_2$ on CaF$_2$ and that of CaF$_2$ on CoSi$_2$/ CaF$_2$. For the CoSi$_2$ growth, this has been solved by introducing the two-step process instead of co-deposition. For the CaF$_2$ growth, an epitaxial CaF$_2$ layer has been formed on CoSi$_2$ at low substrate temperature (<500°C) with ionization and acceleration to solve this problem. With this technique, we have grown a few nm thick CoSi$_2$/ CaF$_2$ heterostructures on (111)Si substrate, which have shown single-crystalline nature in the RHEED and cross sectional TEM observation. Using this technique, a nm-thick CoSi$_2$ epilayer sandwiched by CaF$_2$ was grown and the resistivity of the metal layer was studied. In 2nm-thick CoSi$_2$, the minimum resistivity ρ_{min} ~60$\mu\Omega$cm was obtained for as-grown sample. After the *in-situ* annealing at 860°C, the resistivity was improved. The resistivity became lower than 60$\mu\Omega$cm for most of the samples, and ρ_{min} ~30$\mu\Omega$cm was obtained. The CoSi$_2$ sandwiched by CaF$_2$ obtained here is considered to have relatively good electrical conductance comparable to CoSi$_2$ thin

films on Si(111) ever reported.

we have observed RHEED intensity oscillation at initial stage of partially ionized beam epitaxy of CaF_2 on Si(111) at growth temperature $T_s=440°C$ with the acceleration voltage $V_a=2KV$ and the ionization ratio of a few percent. To our knowledge, this is the first report of the observation of RHEED intensity oscillation for the CaF_2 growth on Si(111). During and after the growth, RHEED pattern of the CaF_2 shows single-crystalline nature in our epitaxial technique, whereas polycrystalline CaF_2 is grown without ionization and acceleration at such low temperature. At high temperature range ($>600°C$), although single-crystalline CaF_2 is obtained without acceleration, RHEED oscillation is not observed during the growth. Intensity oscillation obtained here can be utilized in the in-situ monitoring of a few monolayer thick CaF_2 growth for metal-insulator nanometer-thick heterostructure devices [40, 41, 43, 44].

Chapter 4

Metal-Insulator Triple-Barrier Resonant Tunneling Diode

4.1 Introduction

Superlattice and ultrathin layers with the metal and insulator combination have been discussed as good candidates for ultrahigh-speed electronic devices[3, 42, 49], because of the possibility of utilizing the electron interference due to the large band offset at the metal-insulator (M-I) heterointerface, high carrier density of the metal, and low dielectric constant and high break down field of the insulator. Experimentally, however, the electric properties of the ultrathin M-I heterostructures have not been studied very much at the present stage. In particular, the quantum-size-effect expected in these structures has not yet been observed. Only a report for structures similar to metal-insulator system is negative differential resistance due to the resonant tunneling in AlAs/ NiAl/AlAs semiconductor-metal heterostructures[50].

In this chapter, I will describe the first measurement of vertical electron transport and the negative differential resistance in nanometer-thick multilayered M-I heterostructures.

4.2 Structure and design

In contrast to semiconductor or semiconductor - metal heterostructures, the double-barrier diode with the M-I combination, i.e., the M-I-M-I-M structures may not be suitable for the observation of the negative differential resistance in the current voltage characteristics, even if the electron resonance takes place. This is because the conduction band edge of the emitter metals is far below the Fermi level E_F of the order of 10eV and does not exceed the resonant levels above E_F in the middle metal at applied voltage of a few volts. A structure with at least triple barriers is therefore necessary for the observation of the negative differential resistance as discussed later. By this reason, we use a structure shown schematically in Fig.4.1, which consists of metal($CoSi_2$)-insulator(CaF_2) heterostructures grown on the n-type ($N_D \sim 2 \times 10^{18} cm^{-3}$) Si(111) substrate. Thickness of $CoSi_2$ layers are 1.9nm and 2.8nm, and that of CaF_2 layers is 0.9nm. CaF_2 and $CoSi_2$ were chosen for insulator and metal, respectively, because they possess the fluorite lattice structure and are relatively well lattice-matched to Si with mismatches of +0.6% and −1.2%, respectively.

The samples were prepared by the epitaxial growth technique including the partially ionized beam epitaxy for CaF_2 and the two step growth technique for $CoSi_2$, the details of which have been reported elsewhere[31, 45]. We have obtained a few-nanometer thick $CoSi_2$ sandwiched by CaF_2 without metal agglomeration which was efficiently suppressed using these techniques. Atomically flat CaF_2-$CoSi_2$-CaF_2 heterointerfaces have been
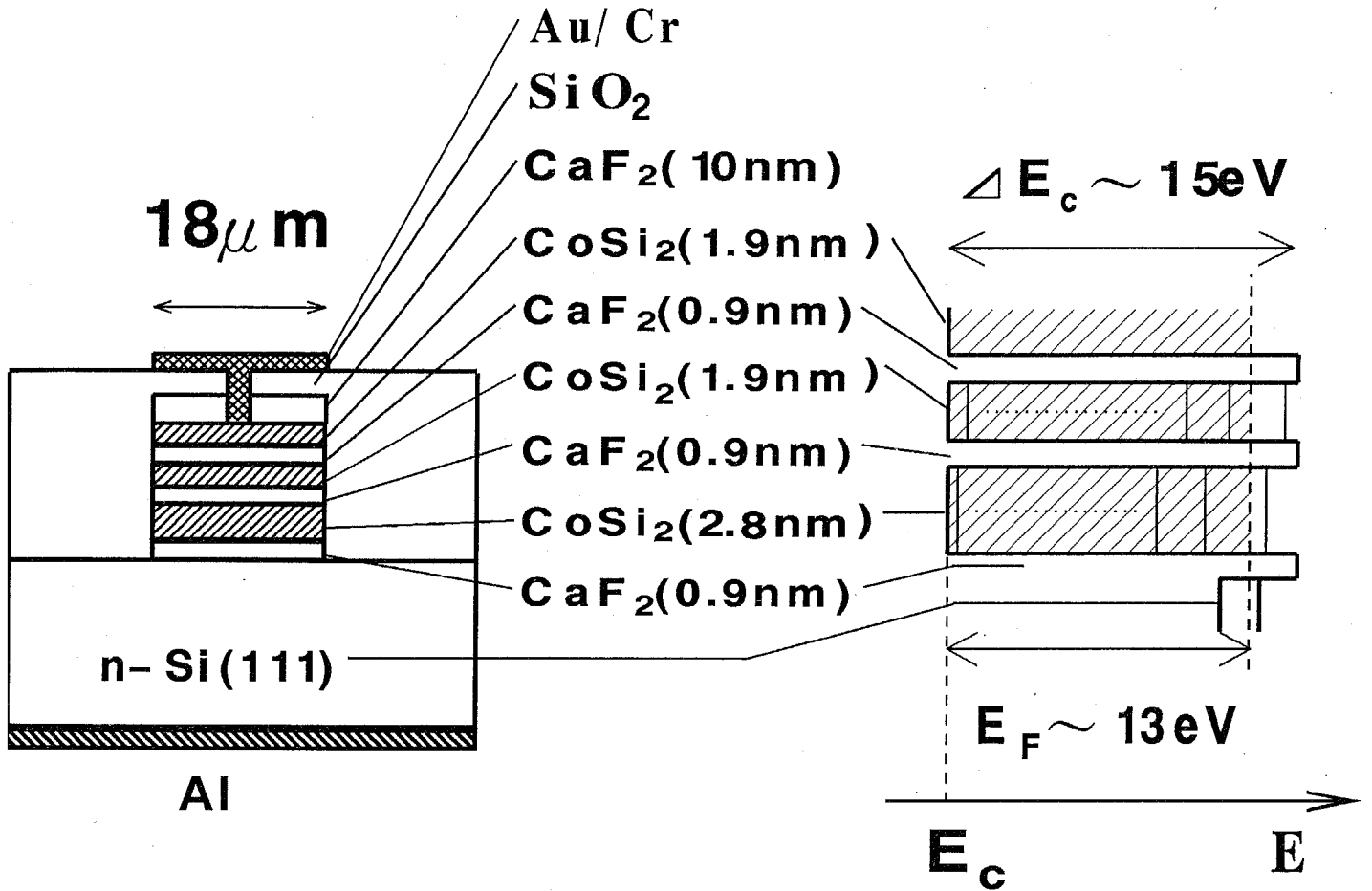
Fig. 4.1: Schematic cross section and band diagram of $CoSi_2/CaF_2$ resonant tunneling diode structure

confirmed by cross sectional transmission electron microscopy (TEM)[45]. Furthermore, the in-situ annealing was done for 15 minutes at 860°C after the growth to improve crystalline quality. We have reported that the resistivity of 2nm-thick $CoSi_2$ layer parallel to the heterointerface was reduced by this procedure[46] to 20-30$\mu\Omega$cm, a few times of the bulk resistivity.

For the measurement of electron transport perpendicular to the M-I heterointerface, the mesa-isolated diode structure with the diameter of 18μm was fabricated by photolithography and selective wet chemical etching. An Au electrode was contacted a $CoSi_2$ layer through 100nm-thick SiO_2 and 10nm-thick CaF_2 top protective layers. A thick Au padding electrode was formed on the SiO_2 top layer for lead bonding. Al was evaporated on the back of the substrate and annealed for ohmic contact. The current-voltage (I-V) characteristics were measured with a parameter analyzer HP-4142B at 77K.

4.3   I-V characteristics in 77K

Figure 4.2(a) shows one of the typical examples of the I-V characteristics of the diodes measured at 77K with the Si substrate being the positive bias side. As can be seen, the negative differential resistance was clearly observed at the positive bias of 3.3V, where the peak-to-valley (P/V) ratio was evaluated to be about 2.1. The significant number of samples showed negative differential resistance and the typical peak-to-valley ratio was around 2. Figure 4.2(b) shows one of the best negative differential resistance characteristics at present stage. P/V ratio as high as 15 was

obtained at 77K.

The bias voltage range of negative differential resistance distributed between 2.5-3.5V, which is probably due to the fluctuation of the layer thickness. We presumed that the reason for the distribution of the current range among different diodes is also the insufficient flatness of the barrier layer since the tunnel current is very sensitive to the barrier thickness. The steep current variation at the negative differential resistance region was responsible for the small series parasitic resistance in the measurement circuit, which is estimated from the gradient of the negative differential resistance region as about 50Ω at 77K. This value of the resistance is consistent with the measurement of the resistance of the substrate and the electrode contact of a sample tip. In most cases, repeated measurements lead to the deteriorate of the peak-to-valley ratio and the current level tends to increase, which appears similar to metal-semiconductor double barrier diodes[50]. The mechanism of this phenomenon is not clear at present.

We have measured I-V characteristics at 4K, and the negative differential resistance was also observed. The observed I-V curve at 4K was almost the same as that at 77K and typical peak-to-valley ratio was about 2. At room temperature, negative differential resistance was not observed in the same sample mainly because of the additional leakage current which increases with temperature. However, in the different structure, we could managed to observe room temperature negative differential resistance. More details will be described in the next section.
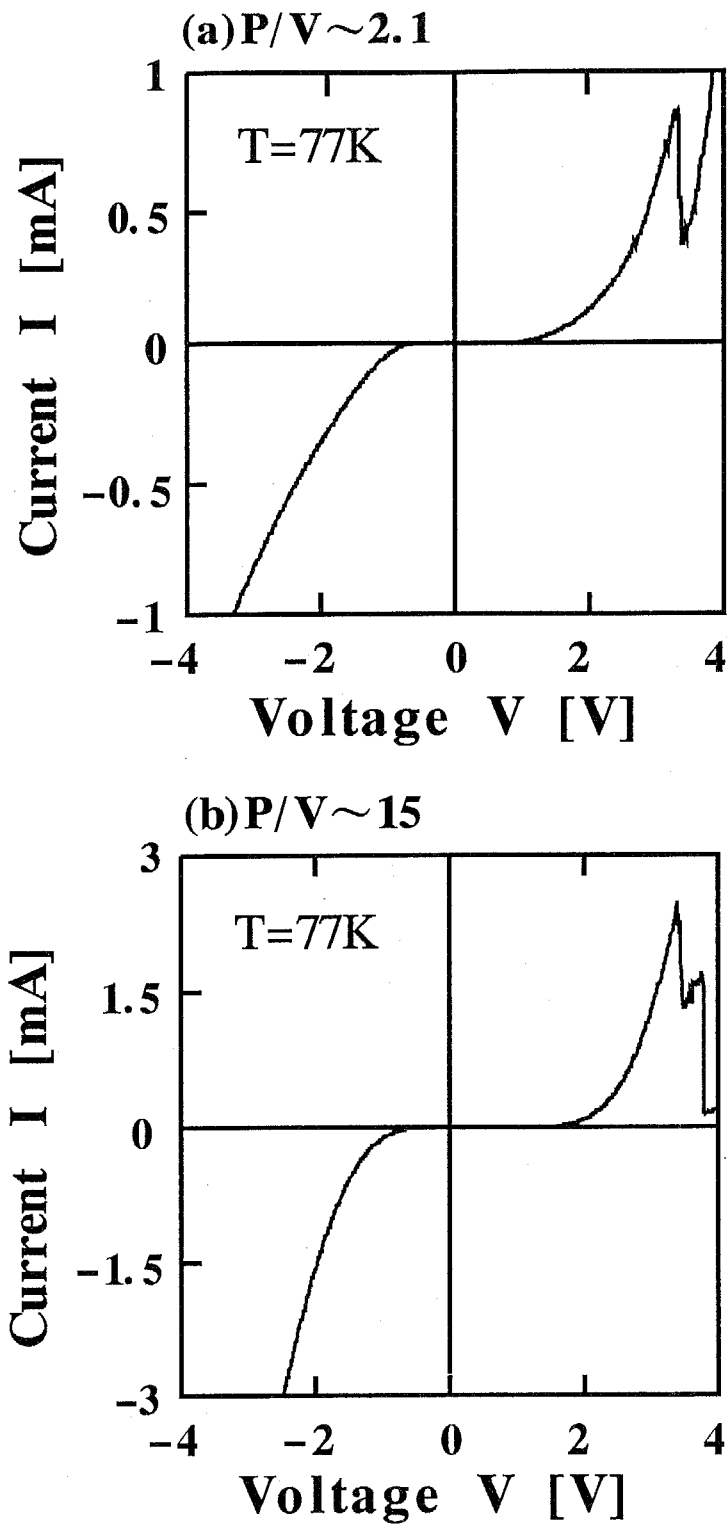
(a) P/V ~ 2.1

(b) P/V ~ 15

Fig. 4.2: (a) One of the typical examples of the I-V characteristics of the diodes measured at 77K with the Si substrate being the positive bias side.

(b) The best negative differential resistance characteristics at 77K at present stage. P/V ratio as high as 15 was obtained.

4.4 Discussion

We believe that the observed negative differential resistance as well as its asymmetry in the I-V characteristics can be attributed to the electron transport through the resonant levels in metallic quantum wells, based on the following discussion.

Although the energy band diagram and electron transport mechanism of $CoSi_2$-CaF_2 heterostructures are not clearly understood at present stage, we simply expanded the discussion made in the semiconductor resonant tunneling devices in order to estimate the voltage range of negative differential resistance region. The energy band diagram of the diode structure was assumed as shown in Fig.4.3. The values of energy band gap of CaF_2 (10eV) and Fermi energy E_F of $CoSi_2$ (13eV) were assumed to be almost the same as those of bulk materials[18, 17, 51, 52]. The bandedge offset at $CoSi_2$-CaF_2 heterointerface was estimated as around 15eV from the electron affinity and the work function of each bulk material.

Formation of the resonant levels can be expected in nm-thick metallic quantum wells. Since the insulator barrier is quite high ($\sim$2eV above E_F), quantized levels are almost the same as those in a single quantum well. The electron transport can be understood with the Fabry-Perot resonant effect or the sequential resonant tunneling effect[54, 53]. The current becomes maximum when quantized levels in the two wells coincide and also E_F of the emitter electrode becomes higher than these levels at the same time. In the calculation of resonant levels, effective electron mass was approximated by the free electron mass both in CaF_2 and $CoSi_2$,
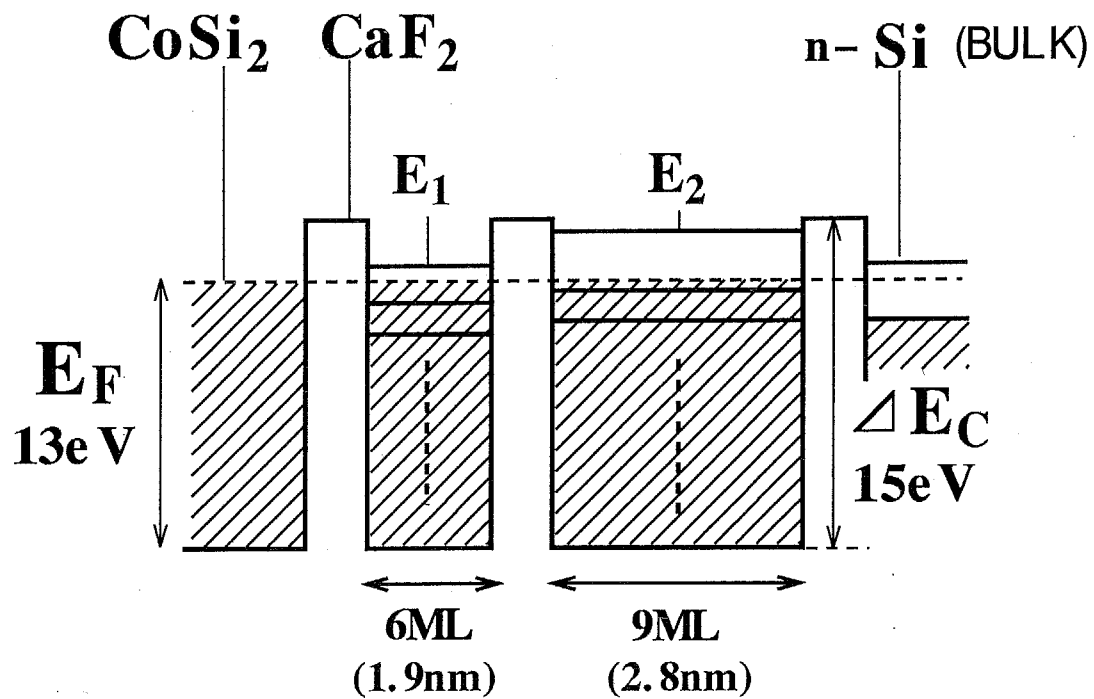
Fig. 4.3: The energy band diagram and quantum levels in metallic wells of the M-I diode structure. Fermi energy of $CoSi_2$ and the bandedge offset at $CoSi_2$-CaF_2 heterointerface were assumed as 13eV and 15eV, respectively. The first resonant level above the Fermi level is labeled E_1 and E_2 in each well.

based on the band structure calculation near the conduction band edge for CaF_2 and the empty-lattice free electron model for $CoSi_2$. The first resonant level above the Fermi level is labeled E_1 and E_2 in each well, as shown in Fig.4.3. If the two wells have different widths, E_1, E_2 and E_F are usually unequal. In the present case, E_2-E_1 and E_1-E_F $\sim 0.6 eV$. By applying a voltage with the Si substrate being positive, E_1 and E_2 approach and become equal with each other. At this voltage, current through the diode becomes maximum since E_F of the left metal nearly coincides with E_1. With increasing voltage, E_1 exceeds E_2 and thus the negative differential resistance brings about. In this operation, E_1 acts as the energy filter for widely distributed electrons in the left side metal, and thus at least triple barriers are necessary for negative differential resistance.

Assuming that the voltage is applied equally to the three barriers, the bias voltage where the first negative differential resistance can be observed is estimated as $3(E_2-E_1) \sim 1.8V$ in the positively biased case. As mentioned before, the position of the observed current peak was in the range of 2.5-3.5V. The deviation of about 1V from the calculated value can be responsible partly for the voltage drop due to the serial resistance of the substrate and contact electrodes ($\sim 0.3V$), and partly for the fluctuation of thickness of the layers. In the reversely biased case, negative differential resistance is not expected to be observed because E_1, E_2 and conduction band edge of n-doped Si at the right side do not become the same height. Asymmetry and the position of negative differential resistance of experimental I-V characteristics can thus be explained

semi-quantitatively by the simplified transport model. The validity of the assumed value of conduction band offset, electron effective mass and free electron approximation model in the M-I structure must be examined in detail in further investigation.

4.5 Negative Differential Resistance at Room Temperature

In this section I will describe on the first room temperature NDR and large peak-to-valley current (P/V) ratio as high as 25 at 77K of metal $(CoSi_2)$/ insulator (CaF_2) resonant tunneling diode.

The device structure and energy-band diagram are shown in Fig.4.4. The structure of the devices is 18μm-diam mesa composed of $CoSi_2(1.9nm)$ /CaF_2 (0.9nm)/$CoSi_2(1.9nm)$ /$CaF_2(0.9nm)$ /$CoSi_2(2.8nm)$ /$CaF_2(0.9nm)$ on n-Si(111)($N_D \sim 2 \times 10^{18} cm^{-3}$) substrate, which makes up a resonant tunneling diode(RTD) with triple CaF_2 barriers and double $CoSi_2$ wells.

The current-voltage(I-V) characteristics were measured first at 77K and afterwards at 300K for the devices with large values of the low temperature P/V ratio of NDR. The largest P/V ratio obtained so far was 25 at 77K. Figure 4.5 shows (a) I-V curve of the device with the largest P/V ratio at 77K and (b) its room temperature operation. The positive bias stands for that applied to Si substrate. For this sample, the NDR with P/V ratio as high as 2 was obtained at 300K. This was the first observation of NDR at room temperature in the metal-insulator system.

Between the I-V characteristics at 77K and 300K, the bias voltage at
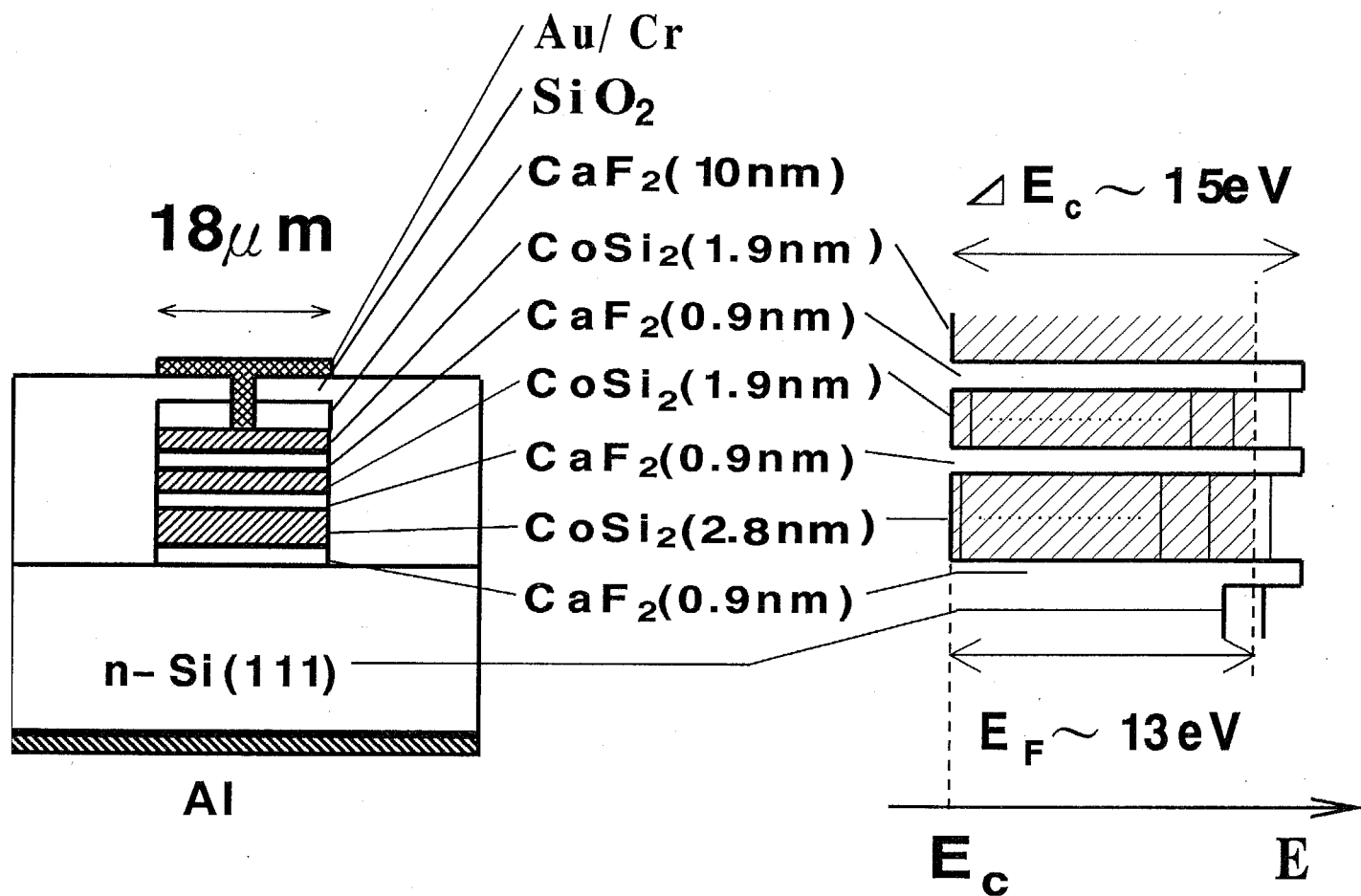
Fig. 4.4: Schematic cross section and band diagram of $CoSi_2/CaF_2$ resonant tunneling diode which operates at room temperature.
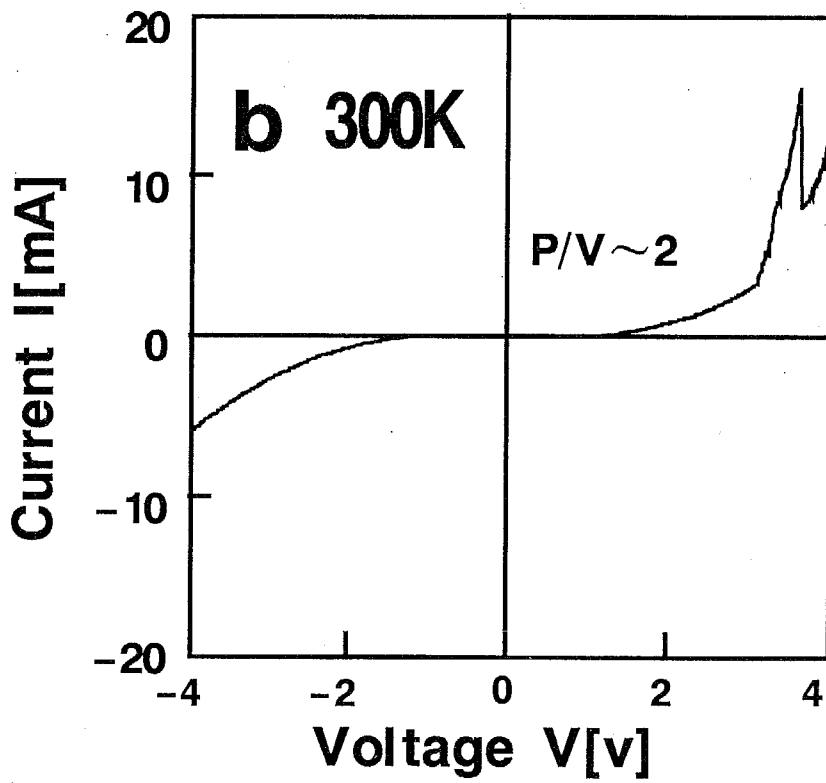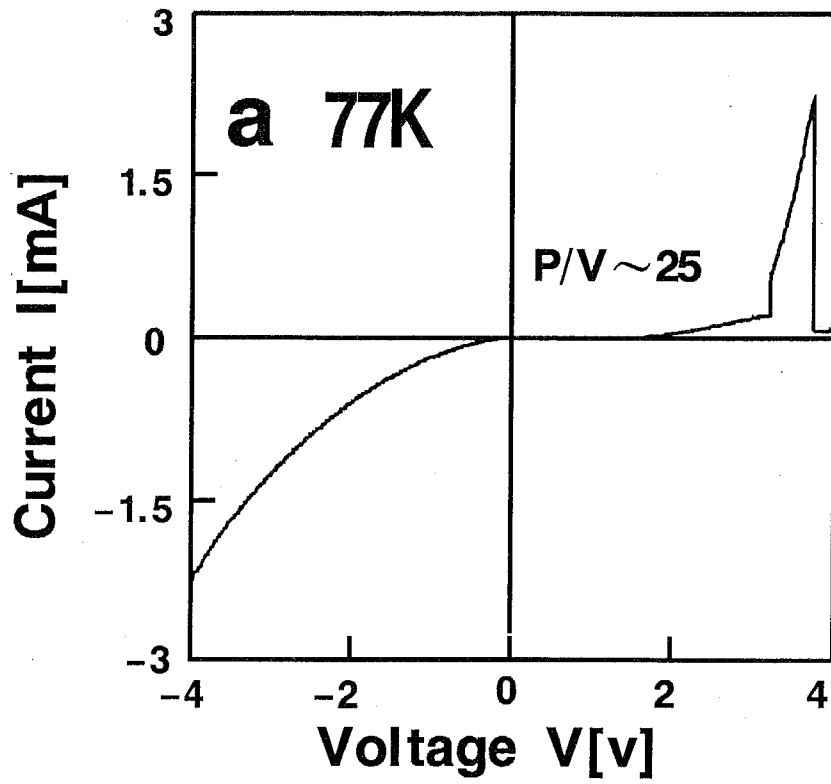
Fig. 4.5: Current-voltage characteristics at 77K and 300K Peak-to-
valley ratio was as high as 25 at 77K and 2 at 300K
a 77K
b 300K

the NDR is almost the same except a small difference probably due to that of the substrate resistance, because the carrier density of n-Si substrate depends on temperature. The change in the width of current peaking region is also small, but the amount of current at 300K was much larger than that at 77K over the all region of applied voltage. Although the reason for this current increase is not clear at present, this result implies the existence of a temperature-dependent leakage current. Because of the large barrier height from the Fermi level($\sim$2eV), the diode itself is inherently less temperature dependent.

Since this leakage current reduces the P/V ratio at room temperature, I-V characteristics with a sharp peak and large P/V ratio at low temperature were necessary for the room temperature operation. In order to get such characteristics, the following two conditions must be satisfied simultaneously at the NDR for the present structure :

(i) the Fermi energy of the negative electrode must exceed the resonance level, and (ii) the quantized levels in the two quantum wells must coincide with each other. Otherwise, the electron transmission coefficient and the carrier density for the current are very small and therefore, we can not observe the sharply peaked I-V characteristics. The present RTDs seemed to satisfy the above conditions, which we expected from the simple calculation with the free-electron approximation[6]. However, as the band structure of M-I superlattice is not known well yet, more detailed analysis will be the future problem.

In conclusion, we have investigated the electron transport and observed negative differential resistance in metal-insulator nanometer-thick

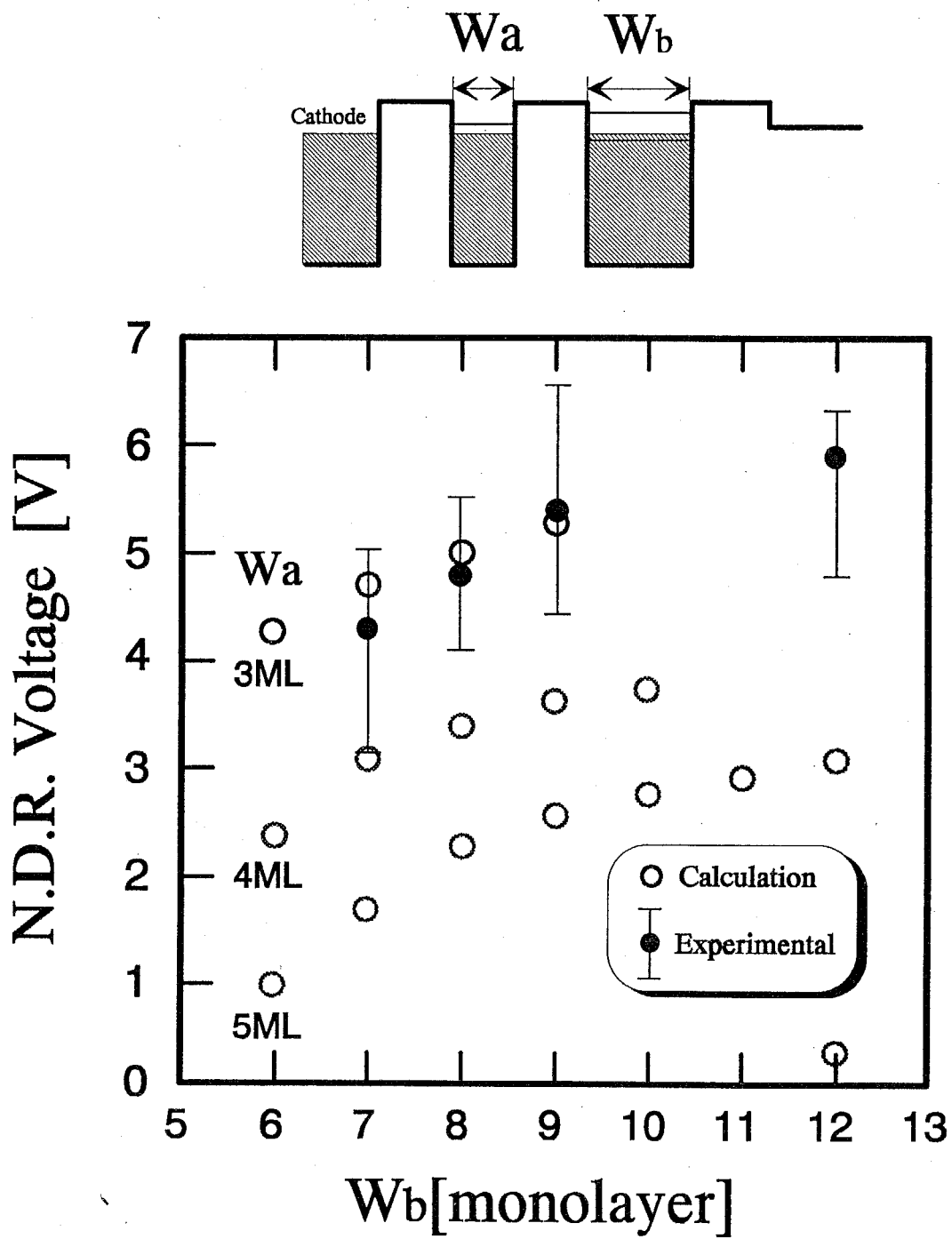heterostructures for the first time. The heterostructures consists of nm-thick double metallic $CoSi_2$ quantum wells and triple CaF_2 barriers grown by means of partially ionized beam epitaxy for CaF_2 and two step growth technique for $CoSi_2$. In the I-V characteristics at 77K, negative differential resistance was clearly observed with the typical and best peak-to-valley ratio of about 2 and 15, respectively. This property can be explained semi-quantitatively by the resonant tunneling transport model in metal ($CoSi_2$)- insulator (CaF_2) heterostructures. We believe that the result obtained here is a strong evidence of the existence of resonant levels in nm-thick metal-insulator multilayered heterostructures and also is an important step toward the realization of novel metal-insulator transistors.

4.6 Layer Thickness Dependence of Negative Differential Resistance

In order to realize metal-insulator quantum resonant electron devices, it is essential to control the resonant level by controlling the layer thickness. As a first demonstration of quantum level control in metal-insulator superlattice, the layer thickness dependence of resonance voltage of triple-barrier resonant tunneling diode has been investigated.

Device structure studied here was the same as the one shown in previous section and all the measurement was carried out at 77K. Figure 4.6 shows the metallic well thickness dependence of the resonance voltage. X-axis represents the layer thickness of the right metallic quantum well (W_b) and left well thickness (W_a) is a parameter (3,4,5ML). Y-axis represents resonance voltage, which was defined as the bias voltage which

gave the peak current in negative differential resistance characteristics. White circle indicates the resonance voltage calculated with free electron approximation as discussed in previous section. Error bars represent the distribution of the resonance voltage experimentally measured and black circle indicates the mean value. This figure shows the experimental resonance voltage qualitatively well agreed with calculated value. However, the experimental value was expected to fit W_a=5ML line instead 3ML line. This deviation is probably due to the problem of our thickness control technique. Monolayer thickness control technique such as atomic layer epitaxy using RHEED oscillation (as discussed in Chapter 3) is essential for quantum level control in metal-insulator superlattices. The distribution of the resonance voltage ($\sim \pm1.5$V) is probably due to the fluctuation of the layer thickness. The deviation of metallic layer thickness $\pm$1ML leads the deviation of resonance voltage $\sim \pm1.5$V. Moreover, the fluctuation of barrier thickness $\pm$1ML results in the nearly random fluctuation of the resonance voltage $\sim \pm2$V.

Although the result obtained here is in a very primitive stage, we can conclude that this study has pioneered the new field of quantitative research on quantum resonance transport in the metal-insulator multi-layered heterostructures.

4.7 Concluding Remarks

In summary, we have investigated the electron transport and observed negative differential resistance in metal-insulator nanometer-thick heterostructures for the first time. The heterostructures consists of nm-thick

Fig. 4.6: Metallic layer thickness dependence of resonance voltage

double metallic CoSi$_2$ quantum wells and triple CaF$_2$ barriers grown by means of partially ionized beam epitaxy for CaF$_2$ and two step growth technique for CoSi$_2$. In the I-V characteristics at 77K, negative differential resistance was clearly observed with the typical and best peak-to-valley ratio of about 2 and 15, respectively. This property can be explained semi-quantitatively by the resonant tunneling transport model in metal(CoSi$_2$)-insulator(CaF$_2$) heterostructures.

Layer thickness dependence of resonance voltage of the diode at 77K has been investigated. The resonance voltage experimentally obtained was qualitatively well agreed with the calculated result based on the free electron approximation.

We believe that the result obtained here is a strong evidence of the existence of resonant levels in nm-thick metal-insulator multilayered heterostructures and also is an important step toward the realization of novel metal-insulator transistors.

Chapter 5

Metal-Insulator Hot Electron Transistor

5.1 Introduction

To realize metal-insulator heterostructure three terminal electron tunnel-ing device proposed in chapter 2 or Ref.[42], we have to study the electron transport through nanometer-thick M-I heterostructures, especially, the transport properties in conduction band of the insulator layers. This property has been extensively studied [55, 56, 57] after M-I hot electron devices were proposed [58] using the combination of an oxide tunnel bar-rier and a relatively thick metal layer. To our knowledge, however, no reports have been made on the transport property through an epitaxial metal layer with a thickness of a few nanometers sandwiched by insulator epi-layers.

In this chapter, I will describe on the transport properties and the first transistor action of the M-I tunnelling hot electron transistor (HET) structure fabricated using the technique described in chapter 3.

5.2 Hot electron transistor

5.2.1 Structure and design

The device structure and its energy band diagram are shown in Fig. 5.1.
The transistor is composed of a $CoSi_2$ (1.9nm)/ CaF_2 (1.9nm) MIM tunnel emitter and a CaF_2 (5nm) collector barrier on an n-Si(111) ($N_D \sim$ $2\times10^{18}cm^{-3}$) substrate. $CoSi_2$/ CaF_2 heterostructures were grown on Si(111) by ionized beam epitaxy for CaF_2, and two step growth technique for $CoSi_2$ as described in chapter 3 or Ref.[45, 46]. The agglomeration of metal on the insulator layer was suppressed and a nanometer-thick continuous film was obtained by these techniques. After the growth, the wafer was annealed at 860°C for $\sim$15min. The single-crystalline nature was confirmed by the transmission electron microscope (TEM) cross-sectional lattice image of the heterointerface.

5.2.2 Fabrication process

Mesa structures for emitter and device isolation were made by using material selectivity of the wet chemical etching (H_2SO_4:H_2O_2=1:4 for CaF_2 etching and 7% buffered HF for $CoSi_2$ etching). The etching rate at 0°C were 1nm/s and 2nm/s for CaF_2 and $CoSi_2$, respectively. The emitter-base junction area was $6\times6\mu m^2$. Emitter and base electrodes with Au/Cr nonalloy contact were formed by the liftoff process, and the collector electrode was formed with Al at the bottom of the substrate.

The detail of the fabrication process was as follows.

1. Emitter electrode formation

(a)

Emitter

Base

CaF$_2$ 5.0nm

CoSi$_2$ 1.9nm

Au/Cr

CaF$_2$ 1.9nm

CoSi$_2$ 1.9nm

CaF$_2$ 5.0nm

n–Si substrate

Al

Collector

2 μm

Base electrode window

16 μm

10 μm

6 μm

Emitter

Emitter electrode window

(b)

CaF$_2$ 1.9nm

CaF$_2$

ϕ=2eV

E$_f$=13eV

n–Si

Al Collector

E$_{C0}$=0eV

CoSi$_2$ Emitter

CoSi$_2$ Base 1.9nm
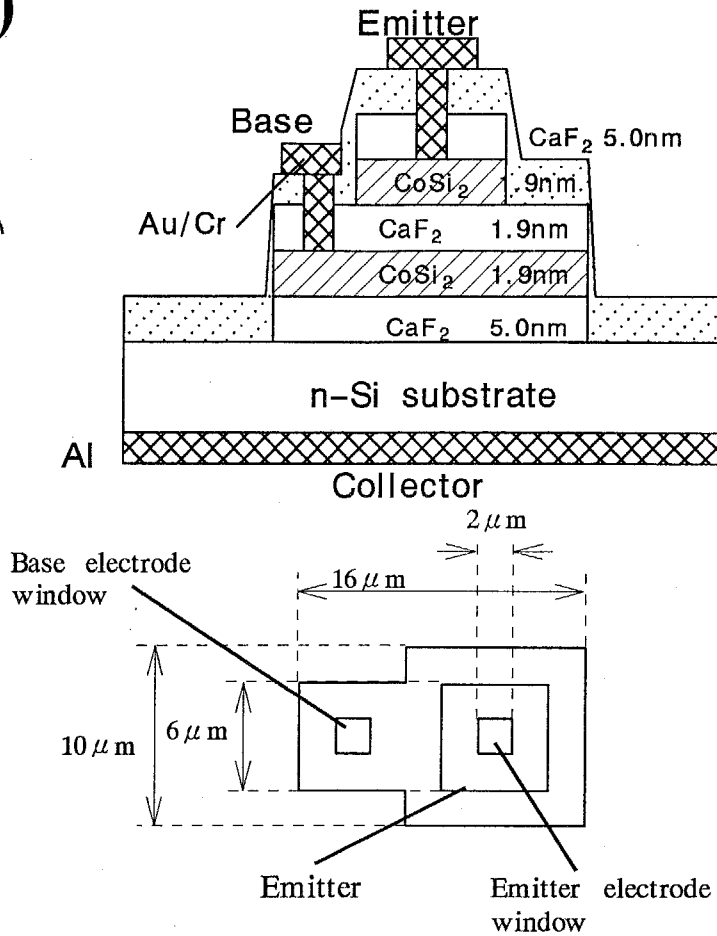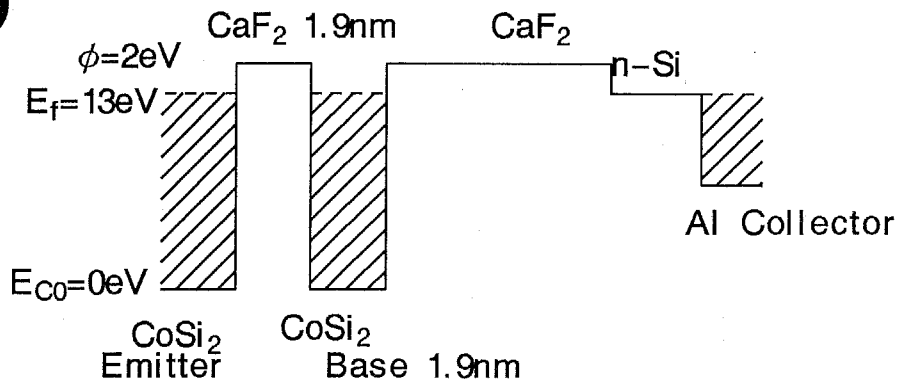
Fig. 5.1: Schematic diagram of CoSi$_2$/CaF$_2$ HET structure
  (a) Cross section of device
  (b) Band diagram

(a) SiO$_2$ deposition

    i. Substrate cleaning by trichloroethylene boiling

    ii. SiO$_2$ CVD 100nm (blue)

(b) Photolithography (Resist:Az) Mask #1(Fig. 5.2)

    i. Substrate cleaning by trichloroethylene boiling

    ii. Baking for drying substrate (120°C 5min.)

    iii. Resist spin coating

        A. Primer (7000rpm. 30sec)

        B. Az (7000rpm. 30sec)

    iv. Pre-baking (80°C 30min.)

    v. Exposure (60mJ/cm^2)

    vi. Development (3-5sec.)

    vii. Rinse (pure water 30sec.)

    viii. Blowing

    ix. Post-baking (120°C 30min.)

(c) SiO$_2$ Etching

    i. Etching by BHF (40sec. at room temp.)

    ii. Rinse (pure water 30sec.)

    iii. Blowing

(d) Selective etching

    i. CaF$_2$ cap layer Etching
        H$_2$SO$_4$:H$_2$O=1:4 0°C (1nm/s) 10sec.

    ii. rinse by pure water

iii. Blowing

iv. CoSi$_2$ Emitter layer etching

BHF 2sec at room temp. (3nm/s) .

v. Rinse by pure water

vi. Blowing

vii. Removing Az (by acetone boiling)

2. Device isolation

(a) SiO$_2$ deposition

i. Substrate cleaning by trichloroethylene boiling

ii. Blowing

iii. SiO$_2$ CVD 100nm(blue)

(b) Photolithography (Resist:Az) Mask #2(Fig. 5.2)

i. Substrate cleaning by trichloroethylene boiling

ii. Baking for drying sub. (120°C 5min.)

iii. Spin coating

A. Primer (7000rpm. 30sec)

B. Az (7000rpm. 30sec)

iv. Pre-baking (80°C 30min.)

v. Exposure(60mJ/cm^2)

vi. Development(3-5sec.)

vii. Rinse (pure water 30sec.)

viii. Blowing

ix. Post-baking (120°C 30min.)

(c) SiO$_2$Etching

    i. Etching by BHF (40sec. at room temp.)

    ii. Rinse (pure water 30sec.)

    iii. Blowing

(d) Selective etching

    i. CaF$_2$ cap layer etching

       H$_2$SO$_4$:H$_2$O=1:4   0°C(1nm/s) 10sec.

    ii. Rinse by pure water

    iii. Blowing

    iv. CoSi$_2$ emitter layer etching

       BHF 2sec. at room temp. (3nm/s)

    v. Rinse by pure water

    vi. Blowing

    vii. CaF$_2$ emitter barrier layer etching

       H$_2$SO$_4$:H$_2$O=1:4   0°C (1nm/s) 2sec.

    viii. Rinse by pure water

    ix. Blowing

    x. CoSi$_2$ Base layer etching

       BHF 2sec at room temp. (3nm/s)

    xi. Rinse by pure water

    xii. Blowing

    xiii. CaF$_2$ Collector barrier etching

       H$_2$SO$_4$:H$_2$O=1:4   0°C (1nm/s) 30sec.

    xiv. Rinse by pure water

xv. Blowing

(e) Removing Az by acetone boiling

3. Window open for Base electrode

(a) SiO$_2$ deposition

    i. Substrate cleaning by trichloroethylene boiling

    ii. Drying sub.

    iii. SiO$_2$ CVD 100nm(blue)

(b) Photolithography (Resist:Az) Mask #3(Fig. 5.2)

    i. Substrate cleaning by trichloroethylene boiling

    ii. Baking for drying sub. (120°C 5min.)

    iii. Spin coating

        A. Primer (7000rpm. 30sec)

        B. Az (7000rpm. 30sec)

    iv. Pre-baking (80°C 30min.)

    v. Exposure (60mJ/cm^2)

    vi. Development (3-5sec.)

    vii. Rinse by pure water (30sec.)

    viii. Drying

    ix. Post-baking (120°C,30min.)

(c) SiO$_2$Etching

    i. Etching by BHF (40sec. at room temp.)

    ii. Rinse (pure water 30sec.)

iii. Blowing

(d) CaF$_2$ layer (cap, Emitter barrier) Etching

    i. H$_2$SO$_4$:H$_2$O=1:4   0°C (1nm/s) 10sec.

    ii. Rinse (pure water)

    iii. Blowing

(e) Electrode evaporation

    i. Preparing Au (50mg)

    ii. Trichloroethylene boiling Cr,Au

    iii. Au Cleaning by etching

        • Etching by HCl 1min at room temp.

        • Rinse in pure water

        • Rinse in methanol

        • Blowing

    iv. Cr rinse in acetone

    v. Drying Cr

    vi. Cr evaporation at 4-5×10^{-6}Torr

        A. Filament Degass

        B. Shutter open V=100V → 180V

        C. Cr evaporation 3min.

        D. Filament cooling

            • Shutter close

            • V=0V

            • waiting 1min.

E. V=180V

F. Shutter open

G. Evaporation 3min.

H. Shutter close

I. V=0V

J. Au evaporation at $6\text{-}7\times10^{-6}$Torr

vii. Lift off (removing Az)

- Boiling in acetone

4. Window open for Emitter electrode

(a) SiO_2 deposition

i. Substrate cleaning by trichloroethylene boiling

ii. Drying sub.

iii. SiO_2 CVD 100nm(blue)

(b) Photolithography (Resist:Az) Mask #4(Fig. 5.2)

i. Substrate cleaning by trichloroethylene boiling

ii. Baking for drying sub. (120°C 5min.)

iii. Spin coating

A. Primer (7000rpm. 30sec)

B. Az (7000rpm. 30sec)

iv. Pre-baking (80°C 30min.)

v. Exposure (60mJ/cm^2)

vi. Development (3-5sec.)

vii. Rinse by pure water (30sec.)

viii. Blowing

ix. Post-baking (120°C,30min.)

(c) SiO$_2$ Etching

    i. Etching by BHF (40sec. at room temp.)

    ii. Rinse (pure water 30sec.)

    iii. Blowing

(d) CaF$_2$ layer (cap, Emitter barrier) Etching

    i. H$_2$SO$_4$:H$_2$O=1:4   0°C (1nm/s) 10sec.

    ii. Rinse (pure water)

    iii. Blowing

(e) Electrode evaporation

    i. Preparing Au (50mg)

    ii. Trichloroethylene boiling Cr,Au

    iii. Au Cleaning by etching

- Etching by HCl 1min at room temp.

- Rinse in pure water

- Rinse in methanol

- Drying

    iv. Cr rinse in acetone

    v. Drying Cr

    vi. Cr evaporation at 4-5×10^{-6}Torr

        A. Filament Degass

        B. Shutter open V=100V → 180V

C. Cr evaporation 3min.

D. Filament cooling

- Shutter close

- V=0V

- waiting 1min.

E. V=180V

F. Shutter open

G. Evaporation 3min.

H. Shutter close

I. V=0V

J. Au evaporation at $6\text{-}7\times10^{-6}$Torr

vii. Lift off (removing Az)

- Boiling in acetone

(f) Formation of electrode pad #1

i. Photolithography (OFPR) Mask #5(Fig. 5.2)

A. Substrate cleaning by trichloroethylene boiling

B. Baking for drying (at 120°C for 10min.)

C. Spincoating OFPR (500rpm. 5sec. + 6000rpm. 30sec.)×2. d=2μm

D. Prebaking (90°C 30min)

E. Exposure (40mJ/cm^2)

F. Development developer:H_2O=2:1 (10sec.)

G. Rinse in pure water

H. Postbaking (80°C 30min)

ii. Cr,Au evaporation (Au:100mg)

iii. Lift off (removing OFPR)

- Boiling in OFPR remover

5. Formation of electrode pad #2

(a) Photolithography (OFPR) Mask #6(Fig. 5.2)

i. Substrate cleaning by trichloroethylene boiling

ii. Baking for drying (at 120°C for 10min.)

iii. Spincoating OFPR (500rpm. 5sec. + 6000rpm. 30sec.)×2. d=2μm

iv. Prebaking (90°C 30min)

v. Exposure (40mJ/cm^2)

vi. Development developer:H_2O=2:1 (10sec.)

vii. Rinse in pure water

viii. Postbaking (80°C 30min)

(b) Cr,Au evaporation (Au:100mg)

(c) Lift off (removing OFPR)

- Boiling in OFPR remover

5.2.3 I-V Characteristics at 77K

After dicing and wire-bonding, transistor characteristics were measured using a YHP-4142B parameter analyzer in 77K as shown in Fig.5.4. Figure 5.5 shows the common-emitter characteristics at 77K. The emitter-

#1 Emitter formation
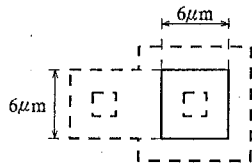
#2 Device Isolation
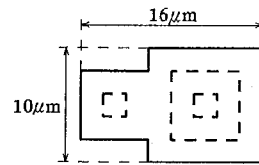
#3 Base electrode window
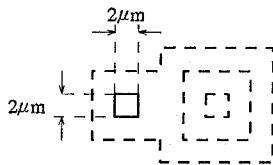
#4 Emitter electrode window
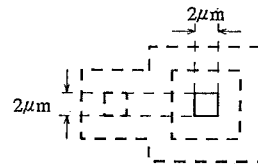
#5 Padding electrode No.1
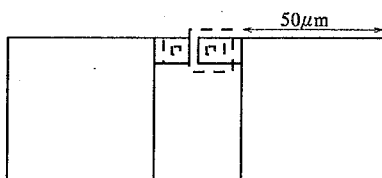
#6 Padding electrode No.2
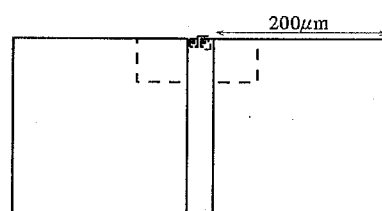
Fig. 5.2: Cr Mask pattern of HET

Grown wafer

$CoSi_2$ Emitter Layer 1.9nm

CaF_2 Cap Layer 5.0nm

CaF_2 Emitter Barrier 1.9nm

$CoSi_2$ Base Layer 1.9nm

CaF_2 Collector Barrier 5.0nm

Si (111) Sub.

Device isolation

Si (111) Sub.

Emitter formation

Si (111) Sub.

Electrode formation

Au/Cr

Si (111) Sub.

Al
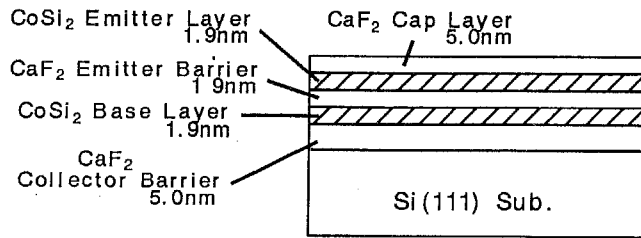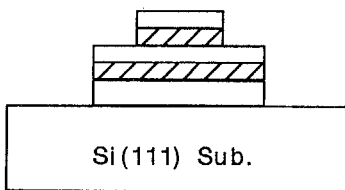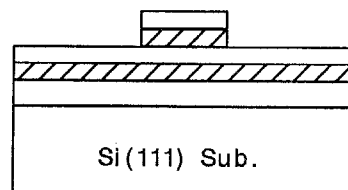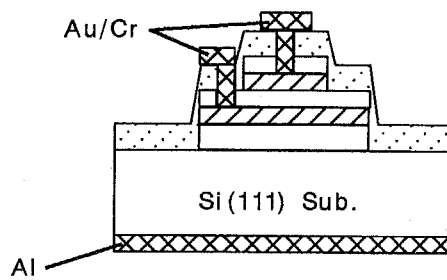
Fig. 5.3: Fabrication process of HET

base voltage V_{BE} was varied from 3.0 to 4.2V in 0.3V steps. As shown in Fig.5.5b, I_B decreased dramatically at $V_{CE} \geq V_{BE}$. This may be because the electrons which were captured in the base layer at $V_{CB} < 0$ were driven to the collector by the electric field between the collector and base at $V_{CB} > 0$. When V_{CE} satisfies the condition $V_{CB} > 1.5 - 2V$, the base current decreases to nearly zero. In this range of V_{CE}, we observed a small amount ($\sim 1 \mu A$) of inverted base current because of the collector-to-base leakage current comparable to the intrinsic base current.

5.2.4 Discussion

The transfer efficiency $\alpha (= I_C/I_E)$ was estimated to be 0.96 at V_{CE} =5V and V_{BE}=3.9V ($I_B \sim 30 \mu A$) where the above leakage current is negligible. With the increase of V_{CE}, α becomes higher, although the exact value is difficult to estimate because of the leakage current. Such a high efficiency probably resulted from the ultrathin metal base layer. Because the leakage current does not influence the AC characteristics, the differential current gain $\Delta\beta (= \Delta I_C/\Delta I_B)$ was estimated, for example, at V_{CE} =6V and V_{BE}=3.9V to be ~ 150, which shows that the device operates as a current amplifier.

The collector current increases with V_{CE} without saturation, unlike semiconductor HETs [59]. Although various mechanisms, such as the space charge effect, fluctuation of the layer thickness, quantum reflection of electrons and leakage current through the flank of the device, could be responsible for this result, details are unknown at present. If the fluctuation of the thickness is the dominant factor, we can expect that
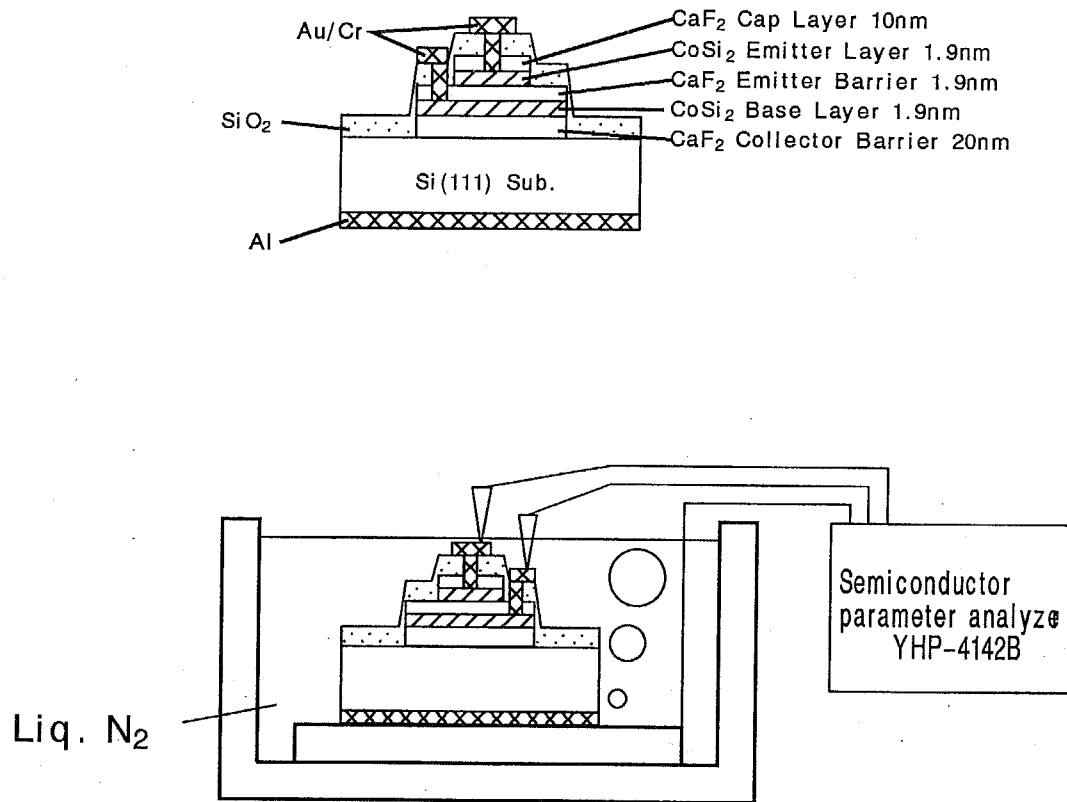
Fig. 5.4: Measurement system of HET in 77K by YHP-4142B

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(a)

IC [mA]

T=77K

3.6V

3.9V

4.2V

4.5V

3.3V

$V_{BE}=3.0V$

VCE [V]

(b)

IB [mA]

T=77K

4.5V

4.2V

3.9V

3.6V

3.3V

$V_{BE}=3.0V$

VCE [V]
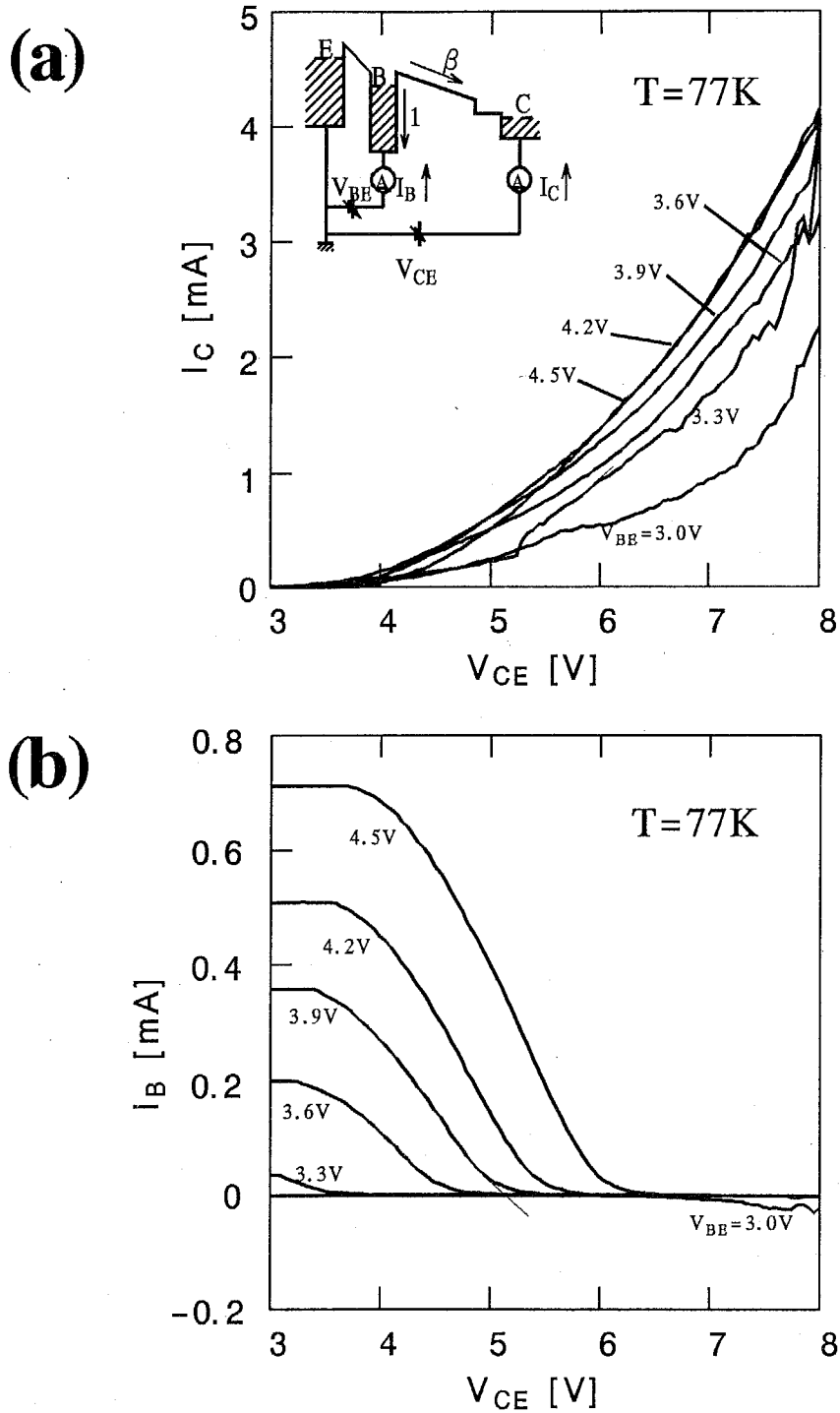
Fig. 5.5: Common-emitter characteristics at 77K for MI-HET
V_{BE} =0.3V/step, T =77K
(a) I_C-V_{CE}
(b) I_C-V_{CE}

conventional transistor characteristics can be observed by improvement of the layer flatness and reducing the device area.

5.3   Concluding Remarks

We have observed transistor action in metal-insulator ($CoSi_2/CaF_2$) HETs for the first time. The hot electron transfer coefficient was >0.9 for hot electrons through 1.9nm-$CoSi_2$ metal base layer at 77K. We believe that the hot electron transport in the metal-insulator reported here is an important step towards realizing three-terminal quantum effect devices.

Chapter 6

Conclusion

The purpose of this study is to realize a novel high-speed electron devices using nanometer-thick metal/insulator heterostructures. According to this purpose, a novel transistor introducing metal and insulator layers and using wavenature of electrons was proposed theoretically and show the possibility of high-speed response. To realize metal-insulator heterostructure devices, the metal-insulator heteroepitaxy technique was experimentally developed. Using the epitaxy technique, metal-insulator resonant tunneling diode was fabricated and the negative differential resistance characteristics was firstly observed even at room temperature. Moreover, the transistor action of M-I hot electron transistor was attained at 77K.

The results obtained in this study are summarized as follows.

[I] Advantage of metal and insulator as a material of high-speed electron devices was shown.

    (a) Metals have higher carrier concentration ($\sim 10^{22}$cm^{-3}) and lower resistivity ($\sim 10^{-6}\Omega\cdot$cm). These properties contribute significantly to the reduction of the device size and obtaining high

current density, which results in the decrease of the charging time. Moreover, if we use metals as materials of devices, there is also the advantage in the reduction of contact resistances and capacitances.

(b) Since insulators generally have lower dielectric constants than those of semiconductors, capacitances between electrodes can be reduced by the use of insulators. Moreover, the energy band gap of insulator is relatively large therefore the breakdown field expected to be higher than semiconductor materials. Consequently, electrons transporting in conduction band of insulator can be accelerated by large electric field, which is advantageous to high speed response of the devices.

(c) In metal-insulator heterostructure, we can utilize the strong quantum interference even at room temperature. In various combination of metal-insulator materials, the conduction band discontinuity at heterointerface is larger than 10eV which is more than ten times larger than that of semiconductor heterointerface. It makes devices based on quantum mechanical effects more attractive since, contrary to the case of semiconductor quantum wells, the intersubband energies here are widely spaced relative to kT even at room temperature where one would strongly prefer to operate such devices.

(d) CaF_2, $CoSi_2$ and $NiSi_2$ is lattice matched to Si with mismatches of +0.6%, -1.2% and -0.5% at room temperature, respectively. These materials were known to grow epitaxially on silicon sub-

strate by conventional molecular beam epitaxy. Although the novel epitaxial growth technique for CaF_2- Metal silicide was required to be developed, Si-CaF_2-Metal silicide system was chosen from the point of the realizability of heteroepitaxy for the first demonstration of M-I heterostructure devices.

[II] A novel metal-insulator high-speed electron device was proposed.

(a) The metal-insulator combination contributes to obtaining high current density, low resistivity and small capacitance. Also, since this combination has the extremely high conduction band discontinuity, strong quantum interference can be obtained. The wave nature of high-velocity ballistic electrons in metal-insulator heterostructure was utilized as the device operation principle.

(b) The static characteristics was analyzed, and the multiple peak $I-V$ characteristics was obtained due to the strong electron resonance at metal-insulator interfaces. It was shown that this device has a potential of attaining subpicosecond response mainly because the layer was very thin and ballistic hot electron has quite high velocity. Thus, this device is quite suitable for a variety of ultrahigh-speed signal processing and logic applications.

[III] It was established the epitaxial growth technique of metal($CoSi_2$)/ insulator(CaF_2) nanometer-thick layered structures on $Si(111)$ with ion assisted epitaxy for CaF_2 and two-step growth of $CoSi_2$.

(a) For the $CoSi_2$ growth, the agglomeration of Co has been solved by introducing the two-step process instead of co-deposition.

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(b) For the CaF_2 growth, an epitaxial CaF_2 layer has been formed on $CoSi_2$ at low substrate temperature ($<500°C$) with ionization and acceleration to avoid the agglomeration of $CoSi_2$ base layer.

(c) With this technique, a few nm thick $CoSi_2/ CaF_2$ heterostructures was grown on $Si(111)$ substrate, which have shown single-crystalline nature in the RHEED and cross sectional TEM observation.

(d) Using this technique, a nm-thick $CoSi_2$ epilayer sandwiched by CaF_2 was grown and the resistivity of the metal layer was studied. In 2nm-thick $CoSi_2$, the minimum resistivity ρ_{min} $\sim60\mu\Omega$cm was obtained for as-grown sample. After the *in-situ* annealing at 860°C, the resistivity was improved. The resistivity became lower than $60\mu\Omega$cm for most of the samples, and ρ_{min} $\sim30\mu\Omega$cm was obtained. The $CoSi_2$ sandwiched by CaF_2 obtained here is considered to have relatively good electrical conductance comparable to $CoSi_2$ thin films on $Si(111)$ ever reported.

(e) RHEED intensity oscillation at initial stage of partially ionized beam epitaxy of CaF_2 on $Si(111)$ was firstly observed. The growth temperature $T_s=440°C$ and the acceleration voltage $V_a=2KV$ and the ionization ratio of a few percent. Intensity oscillation obtained here can be utilized in the in-situ monitoring of a few monolayer thick CaF_2 growth for metal-insulator nanometer-thick heterostructure devices.

[IV] The electron transport in metal-insulator heterostructure was stud-

ied and negative differential resistance was firstly observed in the I-V characteristics of M-I resonant tunneling diode structure even at room temperature.

(a) The heterostructures consists of nm-thick double metallic $CoSi_2$ quantum wells and triple CaF_2 barriers grown by means of partially ionized beam epitaxy for CaF_2 and two step growth technique for $CoSi_2$. In the I-V characteristics at 77K, negative differential resistance was clearly observed with the typical and best peak-to-valley ratio of about 2 and 15, respectively.

(b) This property can be explained semi-quantitatively by the resonant tunneling transport model in metal($CoSi_2$)-insulator(CaF_2) heterostructures. The result obtained here is a strong evidence of the existence of resonant levels in nm-thick metal-insulator multilayered heterostructures and also is an important step toward the realization of novel metal-insulator transistors.

[V] The transistor action in metal-insulator ($CoSi_2/CaF_2$) HETs was observed for the first time.

(a) The device consists of $CoSi_2/CaF_2$ heterojunctions grown on n-Si(111) substrate by ionized beam epitaxy for CaF_2 and a two step growth technique for $CoSi_2$.

(b) The hot electron transfer coefficient was >0.9 for hot electrons through 1.9nm-$CoSi_2$ metal base layer at 77K. The hot electron transport in the metal-insulator described in this chapter is an

important step towards realizing three-terminal quantum effect devices.

Acknowledgements

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