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PAPER Special Section on Analog Circuit Techniques and Related Topics

Design of Wideband Linear Voltage-to-Current Converters

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SUMMARY This paper proposes a voltage-to-current converter with nested feedback loop configuration to achieve high loop gain without reducing the bandwidth. Simulation results using 0.18-μm CMOS process parameters show that the proposed circuit has a good linearity performance. The simulated bandwidth is 350 MHz. The THD improvement of the proposed circuit is more than 60 dB compared to the one of a common gate circuit under a same total current consumption of 10.4 mA.

key words: *current-mode, voltage-to-current converter*

1. Introduction

Along with the advance scaling of integrated circuit process, the device breakdown voltage is also decreased. This forces circuit designers to reduce the power supply voltage which makes it more difficult to guarantee that circuits have enough dynamic range. The current-mode approach has been proposed as an alternative solution for the limitation of dynamic range by power supply voltage in the voltage-mode circuits [1].

One of the significant part in a current-mode signal processing is a voltage-to-current converter. A voltage-to-current converter needs to have sufficient linearity to suppress signal degradation due to distortions. Highly linear voltage-to-current converters with MOSFETs as input devices has been proposed [2]–[5]. However, in the meantime, the amplitude of voltage signals inputed into integrated circuits are determined by standards. For example, the signal amplitude for USB standard is 5 V. Since the circuits in [2]–[5] use MOSFETs as input devices, they still affected by power supply voltage limitation. High-voltage I/O MOSFETs might be used as input devices, however, it will need additional power supply voltage which increases design cost.

In order to enable voltage-to-current conversion of high-voltage inputs using standard low-voltage devices, the use of a passive device such as resistor is one of the solutions. The proposed circuit in [6] is one of the examples. However, since this type of voltage-to-current converters use feedback loops, bandwidth improvement is one of design challenges.

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This paper proposes a feedback loop design method which removes the trade off between loop gain and bandwidth. The principle of voltage-to-current conversion using passive resistor and the conventional feedback configuration will be explained in Sect. 2. The proposed circuit and its design strategy will be discussed in Sect. 3. Finally, simulation results of the proposed voltage-to-current converter will be shown in Sect. 4.

2. Principle of Linear V-I Converter

An easy method of voltage-to-current conversion is use of a single transistor. However, this method does not offer good linearity which might be a critical requirement in some applications. Many ideas have been proposed in order to obtain better linearity, however, many of them still use active devices as the main part of the voltage-to-current converter. Considering again that breakdown voltage as well as power-supply voltage is getting lower while the signal voltage which is determined by standard is not getting lower at all, use of a passive device (resistor) as a voltage-to-current converter might be the only solution in a standard CMOS process.

The principle of a voltage-to-current conversion using a resistor is shown a nullator and norator model in Fig. 1. Here either one of the resistor terminals is virtually connected to ground by nullator and the current flows through the resistor will be given by

$$I_{IN} = \frac{V_{IN}}{R}. \tag{1}$$

It is clear that the input voltage is converted into current by a resistor. This implies a voltage-to-current conversion with high linearity. However, in practical implementations, nullator and norator are implemented using active devices. As a result, there will be a non-zero impedance Z_{IN}, which represents the input impedance of the circuit and is con-

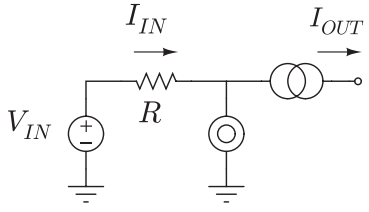

Fig. 1 Nullator-norator model of ideal V-I converter.

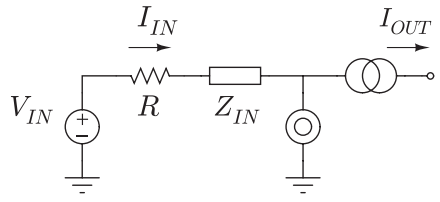

Fig. 2 V-I converter with a non-zero input impedance.

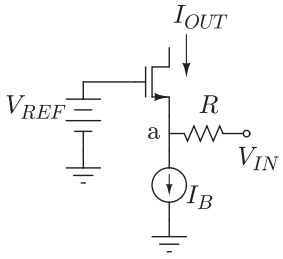

Fig. 3 Conventional voltage-to-current converter.

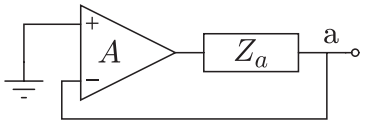

Fig. 4 Lowering impedance of a node using feedback.

nected in series with the voltage-to-current converting resistor (Fig. 2). The input current now will be given by

$$I_{IN} = \frac{V_{IN}}{R + Z_{IN}}. \tag{2}$$

Input current I_{IN} is not only determined by R, but also another element, Z_{IN}. Here, Z_{IN} has non-linearities since the impedance is a property of active devices. Those non-linearities will appear as the non-linearities in the voltage-to-current conversion. For an arbitrary value of R, the larger Z_{IN} is, the worse the linearity will be. A simple example of conventional voltage-to-current converter implementation is shown in Fig. 3. The input impedance seen from node **a**, Z_a is approximately

$$Z_a \approx \frac{1}{g_m}, \tag{3}$$

where g_m is the transconductance of a MOS transistor.

In order to reduce the non-linearities, the voltage-to-current converter circuit should be designed to have an input impedance as small as possible. One of the conventional ways to reduce the impedance of an arbitrary node is by applying a feedback loop to the node as shown in Fig. 4. Here Z_a is the impedance seen from node **a** without any feedback. When a feedback is applied, assuming that the DC-gain of the operational amplifier is A, then the impedance at node **a** will be reduced to

$$Z'_a = \frac{Z_a}{1 + A}. \tag{4}$$

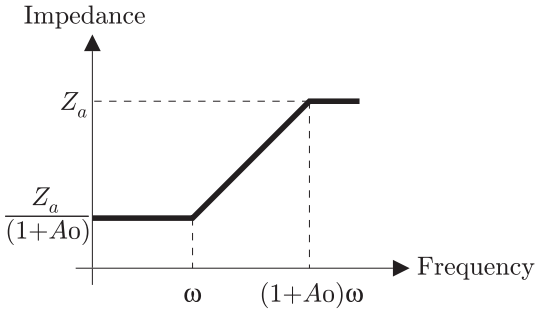

Fig. 5 Frequency response of $Z'_a(s)$.

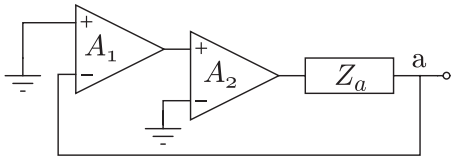

Fig. 6 Improving loop gain using cascaded gain stages.

If the operational amplifier has a 1st-order frequency characteristic, such that

$$A(s) = \frac{A_0}{1 + s/\omega} \tag{5}$$

where A_0 and ω are the DC-gain and the cutoff angular frequency of the operational amplifier respectively, then

$$Z'_a(s) = \frac{Z_a(\omega + s)}{(1 + A_0)\omega + s}. \tag{6}$$

Here the frequency response of $Z'_a(s)$ has a pole at $(1 + A_0)\omega$ and a zero at ω as shown in Fig. 5.

Another gain stage can be added to further reduce the impedance as shown in Fig. 6. In this case the impedance of node **a** is given by

$$Z'_a = \frac{Z_a}{1 + A_1 A_2}. \tag{7}$$

Again, assume that both amplifiers A_1 and A_2 have a 1st-order frequency characteristic, the total gain of a two-stage operational amplifier (by A_1 and A_2), $G_C(s)$ is given by

$$G_C(s) = \frac{A_{01}}{1 + s/\omega_1} \frac{A_{02}}{1 + s/\omega_2} \tag{8}$$

where A_{01}, A_{02}, ω_1 and ω_2 are the DC-gains and the cutoff angular frequencies of the first and second amplifiers respectively. Assume that the frequency characteristics of $A_1(s)$ and $A_2(s)$ are given by the curves in Fig. 7. The loop gain $G_C(s)$ should have enough phase margin to guarantee the stability of the loop. In order to obtain a minimum phase margin of 45 degrees, the second pole of $G_C(s)$ should be at least equal to its unity gain frequency. From Fig. 7, since ω_1 will be the dominant pole while ω_2 will be the second pole, the condition can be derived by solving $|G_C(j\omega)| = 1$ for $\omega = \omega_2$, which gives

$$\omega_1 = \sqrt{\frac{2}{A_{01}^2 A_{02}^2 - 2}} \times \omega_2. \tag{9}$$

Assume that $A_{01}A_{02} \gg 2$, then

$$\omega_1 \approx \frac{\sqrt{2}}{A_{01}A_{02}} \times \omega_2. \tag{10}$$

Since the gain-bandwidth product of $G_C(s)$, GB_C is given by

$$GB_C = A_{01}A_{02}\omega_1, \tag{11}$$

substituting Eq. (10) into (11) gives

$$GB_C \approx \sqrt{2}\omega_2 \tag{12}$$

$$= \frac{\sqrt{2}}{A_{02}} GB_2, \tag{13}$$

where $GB_2 = A_{02}\omega_2$ is the gain-bandwidth product of the second stage. If GB_2 is the affordable maximum gain-bandwidth product (GB_{max}), then the gain-bandwidth product of the two-stage operational amplifier by cascading A_2 will be smaller than GB_{max} by a factor of $\sqrt{2}/A_{02}$ (see Fig. 8). Furthermore, in practical cases, the second pole is set to $2\omega_0$ (ω_0:unity gain frequency) or higher frequencies to avoid peaking in the frequency response. As a result,

$$GB_C \leq \frac{GB_2}{2A_{02}} \tag{14}$$

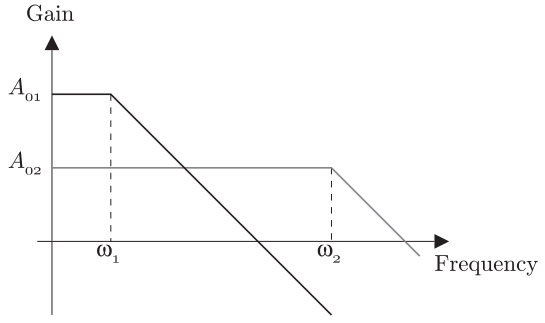

Fig. 7 Frequency response of gain stages in Fig. 6.

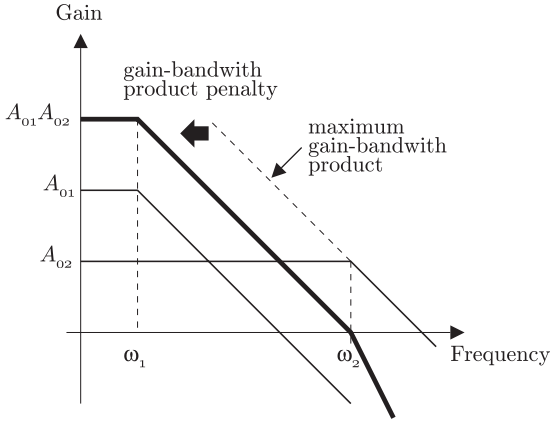

Fig. 8 Frequency characteristic of a cascaded two-stage operational amplifier.

is a reasonable value in practical implementation. Furthermore, cascading more stages will result in a greater gain-bandwidth product penalty.

3. Proposed Circuit

The proposed method of lowering an impedance without having a penalty on the bandwidth is shown in Fig. 9. In the proposed configuration, each stages have a direct feedback loop (nested-feedback loop). Here, the impedance seen from node **a** will be found as

$$Z'_a = \frac{Z_a}{1 + A_2 + A_1A_2}. \tag{15}$$

Again, assuming that each operational amplifiers have a first order frequency response, the impedance seen from node **a** will be

$$Z'_a(s) = \frac{Z_a}{1 + \dfrac{A_{02}}{1 + s/\omega_2} + \dfrac{A_{01}}{1 + s/\omega_1}\dfrac{A_{02}}{1 + s/\omega_2}} \tag{16}$$

$$= \frac{Z_a}{1 + \dfrac{A_{02}(1 + s/\omega_1) + A_{01}A_{02}}{(1 + s/\omega_2)(1 + s/\omega_2)}} \tag{17}$$

$$= \frac{Z_a}{1 + \dfrac{(1 + A_{01} + s/\omega_1)A_{02}}{(1 + s/\omega_1)(1 + s/\omega_2)}}. \tag{18}$$

If $\omega_2 = (1 + A_{01})\omega_1$, which is approximately the unity gain frequency of A_1, then $Z'_a(s)$ can be rewritten as

$$Z'_a(s) = \frac{Z_a}{1 + \dfrac{(1 + A_{01})A_{02}}{(1 + s/\omega_1)}}. \tag{19}$$

From Eq. (19), the open loop gain $G_P(s)$ is given by

$$G_P(s) = \frac{(1 + A_{01})A_{02}}{1 + s/\omega_1} \tag{20}$$

which is a first order frequency response with a DC-gain of $(1 + A_{01})A_{02}$ and a cutoff frequency at ω_1. The equivalent gain bandwidth product GB_P is

$$GB_P = (1 + A_{01})A_{02} \times \omega_1. \tag{21}$$

Assuming that $A_{01} \gg 1$, the gain bandwidth product is approximately

$$GB_P \approx A_{01}A_{02}\omega_1. \tag{22}$$

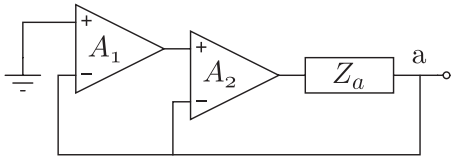

Fig. 9 Proposed nested feedback configuration.

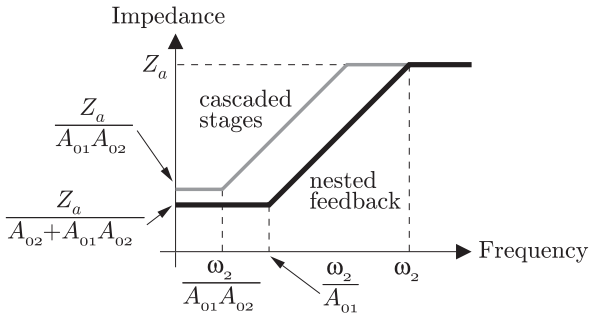

Fig. 10 Frequency characteristics of conventional and proposed configurations.

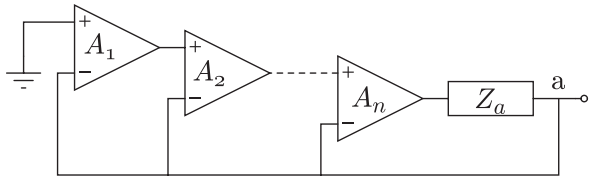

Fig. 11 Proposed nested feedback configuration in general from.

Table 1 The value of poles for each stages.

Stage	Pole
2	$\omega_2 = (1 + A_1)\omega_1$
3	$\omega_3 = (1 + A_2 + A_1A_2)\omega_1$
4	$\omega_4 = (1 + A_3 + A_2A_3 + A_1A_2A_3)\omega_1$

Remember that since $\omega_2 = (1 + A_{01})\omega_1 \approx A_{01}\omega_1$, then

$$GB_P \approx A_{02}\omega_2 = GB_2. \tag{23}$$

Compared to Eq. (14), Eq. (23) shows that there is no penalty in the bandwidth of the proposed configuration (Fig. 10).

The proposed configuration can be expanded into a general form as shown in Fig. 11. Assuming that each stages have a first order frequency characteristic, the general form of Eq. (15) can be expressed as

$$Z'_a = \frac{Z_a}{1 + \sum_{i=1}^{n}\prod_{j=i}^{n}\frac{A_j}{1 + s/\omega_j}}, \tag{24}$$

where A_j and ω_j are the DC gain and the cutoff angular frequency of the j-th amplifier respectively. Repeating the procedure of poles cancellation as shown in Eqs. (18) and (19), the poles for each stages are given by equations in Table 1. Here the pole of n-th stage amplifier $\omega_n$will be given by

$$\omega_n = \left(1 + \sum_{i=1}^{n-1}\prod_{j=i}^{n-1} A_j\right)\omega_1 \tag{25}$$

$$= \omega_1 + \left(\sum_{i=1}^{n-1}\prod_{j=i}^{n-1} A_j\right)\omega_1 \tag{26}$$

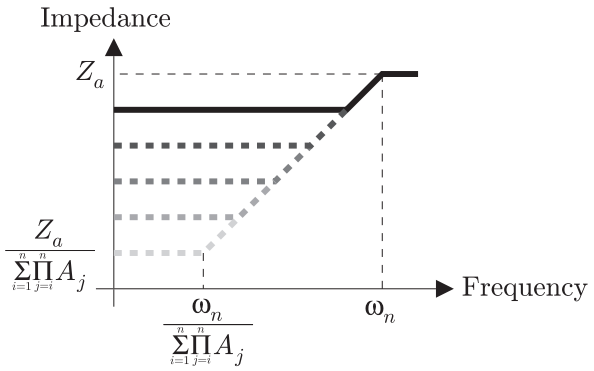

Fig. 12 Effect of increasing gain stage.

$$= \omega_1 + A_{n-1}\left(1 + \sum_{i=1}^{n-2}\prod_{j=i}^{n-2} A_j\right)\omega_1 \tag{27}$$

$$= \omega_1 + A_{n-1}\omega_{n-1}. \tag{28}$$

Assume that $A_{n-1}\omega_{n-1} \gg \omega_1$, then the pole of n-th stage ω_n will be approximately

$$\omega_n \approx A_{n-1}\omega_{n-1}, \tag{29}$$

where $A_{n-1}\omega_{n-1}$ is the unity gain frequency of $(n-1)$-th stage. This means that a multi-stage feedback loop in Fig. 11 will have a first order frequency response by setting the pole of a stage to the unity gain frequency of the preceding stage. The impedance will be given by

$$Z'_a = \frac{Z_a}{1 + \dfrac{\sum_{i=1}^{n}\prod_{j=i}^{n} A_j}{1 + s/\omega_1}} \tag{30}$$

$$= \frac{Z_a(1 + s/\omega_1)}{1 + \sum_{i=1}^{n}\prod_{j=i}^{n} A_j + s/\omega_1}. \tag{31}$$

Considering that the maximum gain-bandwidth product depends on the process and assuming that $A_n \times \omega_n$ is equal to the maximum gain-bandwidth product GB_{max}, then

$$GB_{max} = A_n\left(1 + \sum_{i=1}^{n-1}\prod_{j=i}^{n-1} A_j\right)\omega_1 \tag{32}$$

$$\omega_1 = \frac{GB_{max}}{\sum_{i=1}^{n}\prod_{j=i}^{n} A_j}. \tag{33}$$

Since the denominator of Eq. (33) is equal to the total loop gain, the maximum gain-bandwidth product of the proposed nested-feedback configuration is equal to the maximum available gain-bandwidth product for a given process. The effect of increasing the number of stages is illustrated in Fig. 12.

3.1 Stability Analysis

Unlike nested miller configuration [7], [8], which creates ze-

ros in the right hand side of the s-plane, the proposed configuration has a straight forward and easier compensation scheme. The loop gain of the proposed configuration, $G_P(s)$ can be found from Eq. (24) as

$$G_P(s) = \frac{N(s)}{D(s)} = \sum_{i=1}^{n} \prod_{j=i}^{n} \frac{A_j}{1 + s/\omega_j}. \tag{34}$$

This means that as long as $A_j > 0 (j = 1 \sim n)$ and the poles of each gain stages are in the left hand side of s-plane, the zeros of $G_P(s)$ will also lay on the left hand side of s-plane. As a result, all pole-zero cancellations in the proposed nested feedback configuration are stable (pole-zero cancellation of right hand side zero is unstable). A feedback loop incorporating pole-zero cancellations will be stable if and only if there is no unstable pole-zero cancellations in $G_P(s)$ and if $\frac{1}{1+G_P(s)}$ is stable [9]. The second condition means the real part of every roots of polynomial $P(s) = N(s) + D(s)$ must be negative. From Eq. (34), $P(s)$ is given by

$$P(s) = \sum_{i=1}^{n-1} \left(\prod_{j=1}^{i} (1 + s/\omega_j) \right) \left(\prod_{k=i+1}^{n} A_k \right)$$

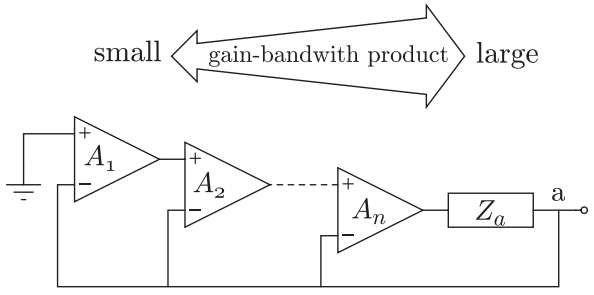

Fig. 13 Relation of gain-bandwidth product between stages.

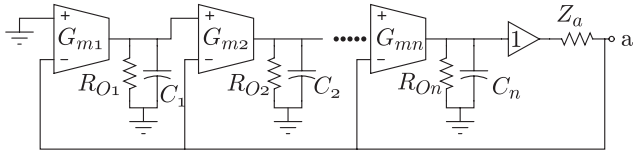

Fig. 14 An implementation of gain stages.

$$+ \prod_{i=1}^{n} (1 + s/\omega_i) + \prod_{i=1}^{n} A_i. \tag{35}$$

Since the poles of each gain stages, ω_i must lay on the left hand side of s-plane and A_i are positive, all coefficients of $P(s)$ are positive. It means the real part of every roots of $P(s)$, which is also the poles of $\frac{1}{1+G_P(s)}$, are negative.

3.2 Design Strategy

It is clear from Eq. (28) that the poles have the following relation

$$\omega_1 < \omega_2 < \ldots < \omega_{n-1} < \omega_n. \tag{36}$$

The stage which is directly connected to Z_a has the largest gain-bandwidth product (and determines the overall bandwidth) while stages far away from node **a** will have smaller gain-bandwidth products (Fig. 13). Assume that the amplifier stages are realized by the configuration in Fig. 14. Here G_{mi}, R_{Oi} and $C_i (i = 1, \ldots, n)$ are the transconductance, the output resistance and the capacitance which determines the pole of the amplifier stage respectively. Equation (29) shows that the gain-bandwidth product of a stage should be equal to the pole of the following stage. Therefore, the capacitance ratio of nearby stages is given by

$$\omega_n = A_{n-1}\omega_{n-1} \tag{37}$$

$$\frac{1}{C_n R_{On}} = G_{m(n-1)} R_{O(n-1)} \frac{1}{C_{n-1} R_{O(n-1)}} \tag{38}$$

$$\frac{C_{n-1}}{C_n} = G_{m(n-1)} R_{On}. \tag{39}$$

In an n-stage configuration with equal gain for each stages ($G_{mi}R_{Oi} = G_m R_O$ = constant), the n-th stage will have the smallest capacitance while the largest one is the capacitance of the 1-st stage which is given by

$$C_1 = (G_m R_O)^n C_n. \tag{40}$$

For a 3-stage amplifier with a gain of 10 for each stages, C_1 will be as large as 1000 times of C_n. It is clear that this design strategy is not a practical one since the capacitances will consume a large chip area.

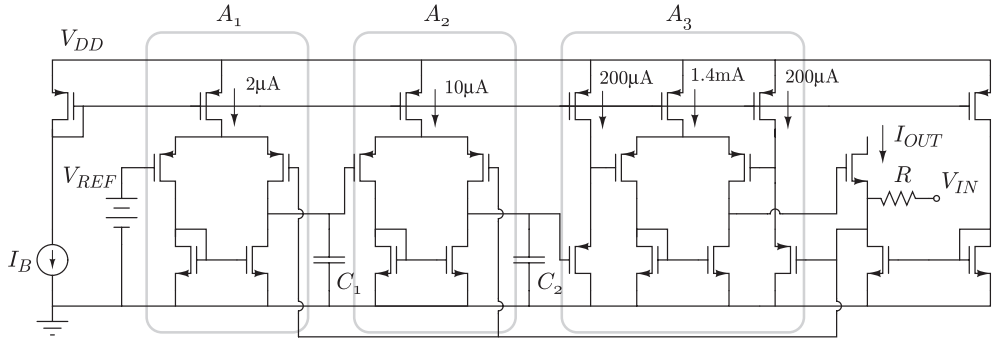

Fig. 15 Proposed voltage-to-current converter.

Table 2 Parameters of each stages.

	A_1	A_2	A_3	Unit
DC gain	39	32	25	dB
$f_{-3\,\mathrm{dB}}$	0.01	0.69	21.7	MHz
Tail current	2	10	1800	μA
Differential pair Tr. size (W/L)	2/1.5	4/0.5	280/0.18	μm/μm

(V_{DD} = 1.8V, C_1 = 2 pF, C_2 = 0.3 pF)

Equation (39) shows that the ratio between capacitances of n-th stage and $(n-1)$-th stage depends on the transconductance of $(n-1)$-th stage $G_{m(n-1)}$ and the output resistance of n-th stage R_{On}. It is clear that a reasonable way to reduce the gain-bandwidth product of $(n-1)$-th stage is by reducing its transconductance. In a simple single-ended amplifier with a differential pair, this can be done by simply reducing the bias current and the size of the input MOS transistors.

Figure 15 shows the proposed voltage-to-current converter which is realized using a 3-stage nested feedback amplifier, a common gate circuit and a resistor. Source follower circuits are added to the input of final stage to provide a proper bias for the differential pair of the stage. Here the values of tail currents, differential pair MOSFETs' sizes and capacitances C_1, C_2 are set to meet the condition in Eq. (29). Table 2 shows the simulated parameters for each gain stages which is designed with 0.18 μm CMOS process parameters. The total DC gain and gain-bandwidth product are approximately 96 dB and 700 MHz respectively. It is possible to improve the DC gain further, however the equations to find the circuit parameters will be different because there is a high possibility that the MOSFETs will fall into weak inversion region (referring to Table 2, the current flows in each MOSFETs will be smaller than 1 μA).

4. Simulation Results

The proposed circuit in Fig. 15 is simulated using Spectre with 0.18 μm CMOS process parameters. The other parameters are shown in Table 3. The DC characteristics of the proposed circuit is shown in Fig. 16. The characteristics of a conventional voltage-to-current converter using a common gate circuit (Fig. 3) are also shown for comparison. The transistors sizes of common gate stages in Figs. 3 and 15 have been set such that both the conventional and proposed circuits have equal total bias currents of 10.4 mA. The linearity of the proposed circuit can be confirmed from transconductance which is obtained from the derivation of output current. The proposed circuit has a constant transconductance which is equal to $1/R$, while the conventional one has a curved characteristic with fluctuation of more than 6%. The good linearity performance of the proposed circuit is due to the low input impedance by the proposed nested feedback configuration. The frequency characteristic of input impedance Z_{in} is shown in Fig. 17. While the conventional circuit has an input impedance of approximately 5.4 Ω, the input impedance of the proposed circuit

Table 3 Simulation parameters.

Parameter	Value
V_{REF}	0.3 [V]
I_B	10 [μA]
R	600 [Ω]
V_{IN}	0–5 [V]
V_{DD}	1.8 [V]

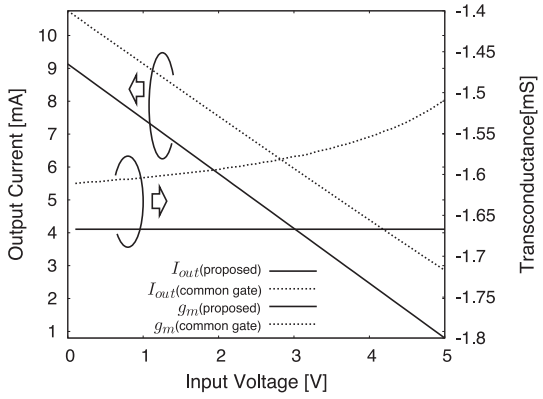

Fig. 16 Output currents and transconductances.

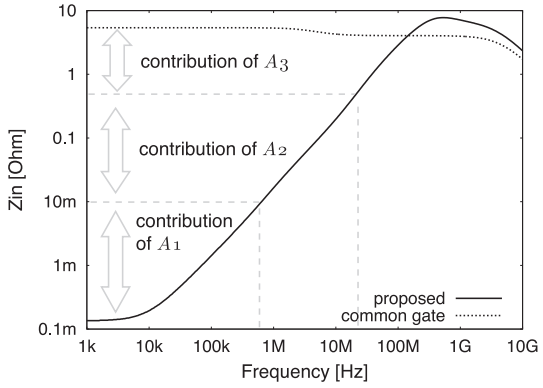

Fig. 17 Input impedances.

is approximately 130 $\mu\Omega$ at frequencies up to 10 kHz. Considering that the total DC gain is 96 dB, the theoretical input impedance of the proposed circuit is 86 $\mu\Omega$. The difference between simulation and theoretical values are mainly caused by an attenuation at common gate stage and parasitic resistances, which are not considered in the analysis.

From Fig. 18, the bandwidth (−3 dB frequency) of the proposed circuit is found to be 350 MHz. The output current of conventional common gate circuit decreases slightly at frequency of a few MHz. This is caused by the parasitic elements in MOS transistor of the common gate circuit. In contrary, the proposed circuit compensates the effect of parasitics and extends the bandwidth. This property is not discussed in this paper but will be included in future publications.

The linearity of the voltage-to-current converter is evaluated using Total Harmonic Distortion (THD). First, the input voltage amplitude is varied from 0.5 V to 2.5 V while

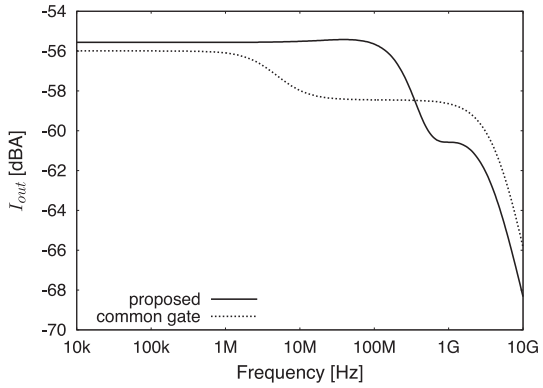

Fig. 18 Frequency characteristics of output currents.

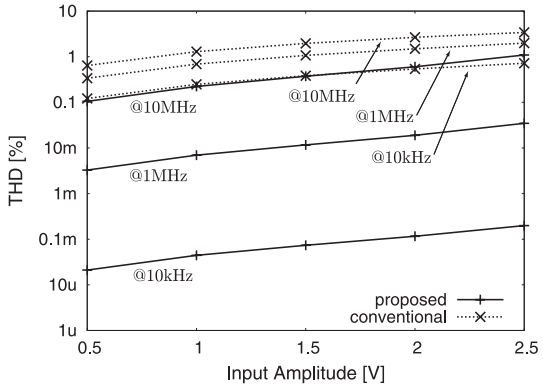

Fig. 19 THD with various input voltage amplitudes.

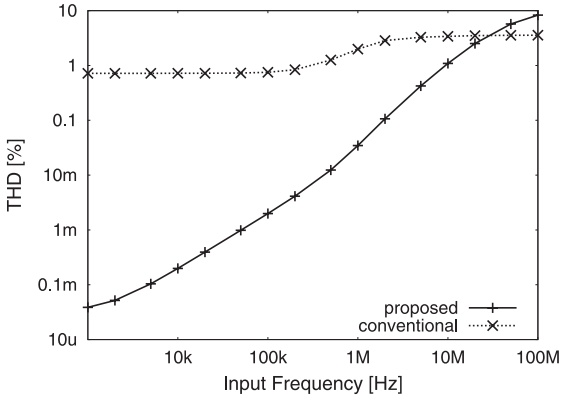

Fig. 20 THD with various input frequency (input amplitude: 2.5 V).

the input signal frequency is kept constant at 10 kHz, 1 MHz and 10 MHz. The results are shown in Fig. 19. These results show that for input frequency of 10 kHz, proposed circuit has a THD as low as 0.1m% for input amplitude up to 2 V. On the other hand, the THD of common gate circuit is higher than 0.1%. This means a THD improvement of more than 60 dB is achieved.

Figure 20 shows the simulation results of THD for various input frequencies with a fixed input voltage amplitude of 2.5 V. The simulation results show that the THD of the conventional circuit exceeds 1% for input frequencies higher than 500 kHz. On the other hand, the proposed circuit keeps the THD lower than 1% for frequencies up to 10 MHz. The THD of the proposed circuit is getting lower as the frequency decreases. Finally, the performance comparison is summarized in Table 4.

Table 4 Performance comparison.

Parameter	This work	[6]
Process	0.18 μm	0.5 μm
Bandwidth	350 [MHz]	30 [MHz]
Input range	0–5 [V]	0–3.3 [V]
Supply voltage	1.8 [V]	-
Conversion resistance (R)	600 [Ω]	1 [MΩ]
Total bias current	10.4 [mA]	1 [μA]

5. Conclusions

A voltage-to-current converter with a nested feedback configuration is proposed. The proposed configuration enables a design of a high loop-gain configuration without reducing the bandwidth. The proposed configuration allows the implementation of a wideband voltage-to-current converter with high linearity. Simulation results using 0.18 μm CMOS process parameters show a highly linear voltage-to-current conversion characteristic. The simulated bandwidth of the proposed circuit is 350 MHz. A THD as low as 0.1m% is achieved using a 3-stage configuration of the proposed topology. The THD improvement of the proposed circuit is more than 60 dB compared to the one of a common gate circuit under a same total current consumption of 10.4 mA.

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