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Low-Phase-Noise Wide-Frequency-Range Ring-VCO-Based Scalable PLL with Subharmonic Injection Locking in 0.18 μm CMOS

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***Abstract*— A low-phase-noise ring-VCO-based PLL (frequency tuning range: 0.65–1.6 GHz) with subharmonic injection locking was realized (PLL area: 0.1 mm^2) by adopting 0.18 μm CMOS technology and combining pMOS resistive loads with a circuit for shifting bias levels; this makes the rail-to-rail range of voltages usable as control voltages.**

For a 90-MHz input reference signal, without injection locking, the 0.2-MHz-offset phase noise was -108 dBc/Hz (PLL output frequency: 1.44 GHz $=$ 16 $\times$ 90 MHz); with injection locking, the noise was -122 dBc/Hz (spurious level: -35 dBc; power consumption from a 1.8 V power supply: 39 mW).

***Index Terms*— Phase-locked loops, injection locked oscillators, ring VCO, phase noise, CMOS integrated circuits**

I. INTRODUCTION

Conventional multistandard wireless mobile terminals contain multiple RFICs. To reduce production costs, one-chip RF LSI systems are needed. A great effort is being made to develop wideband and/or multiband RF solutions using highly scaled advanced CMOS processes. The use of such processes is beneficial to A/D and D/A converters and digital baseband circuits. However, it is very difficult to reduce the scale of RF/analog circuit blocks, especially power amplifiers and oscillator circuits, including voltage-controlled oscillators (VCOs) and phase-locked loops (PLLs), because of the presence of inductors that do not scale with advancements in technology.

This paper describes a study on a ring-VCO-based PLL as a potential solution to realize scalable high-performance PLLs. In order to improve its phase-noise performance, the proposed PLL is augmented with injection locking.

This paper is organized as follows. In Section II, the proposed circuit topology for realizing a ring VCO with a relatively constant $K_{\rm VCO}$ is shown. In Section III, the design of the proposed PLL with injection locking is described. In Section IV, the measurement results obtained from an implementation in a 0.18 μm CMOS process are presented. The conclusions of this study are presented in Section V.

II. DESIGN OF THE DIFFERENTIAL INJECTION-LOCKED RING-VCO

A. *Tuning Linearity*

From the VCO gain, $K_{\rm VCO}$, the change in the output frequency in response to an incremental change in the control voltage can be determined. The linearity of the frequency tuning of a VCO can be seen from the functional dependence of $K_{\rm VCO}$ on the control voltage. The linearity is an important consideration when designing a PLL. The closed-loop transfer function of a PLL, $H(s)$, is proportional to $K_{\rm VCO}$ [1]. The loop bandwidth of a PLL can be expressed as

$$\omega_{\rm n} = \sqrt{\frac{K_{\rm VCO} I_{\rm P}}{2\pi N C_{\rm f}}}, \tag{1}$$

where $I_{\rm P}$ is the charge pump (CP) current, N is the division ratio of the feedback loop, and $C_{\rm f}$ is the filter capacitance. We can see that the loop bandwidth of a PLL can be varied by changing $K_{\rm VCO}$.

The total phase noise, $S_{\rm PLL}$, of a PLL can be expressed as

$$S_{\rm PLL} = |H(s)|^2 S_{\rm REF} + |1 - H(s)|^2 S_{\rm VCO} + \left| \{1 - H(s)\} \frac{K_{\rm VCO}}{s} F(s) \right|^2 S_{\rm PFD}, \tag{2}$$

where $S_{\rm REF}$, $S_{\rm VCO}$, and $S_{\rm PFD}$ are the phase noise of the reference signal, the VCO output signal, and the phase frequency detector (PFD); $F(s)$ is the loop-filter transfer function of the PLL [2]. The in-band phase noise power of the PLL changes with $K_{\rm VCO}$ because $H(s)$ is proportional to $K_{\rm VCO}$. Further, the power levels of the spurious output are proportional to $K_{\rm VCO}$ [3]. From these facts, we know that nonlinearity in the tuning degrades the performance of PLLs. Therefore, it is desirable to minimize the variation in $K_{\rm VCO}$ across the tuning range.

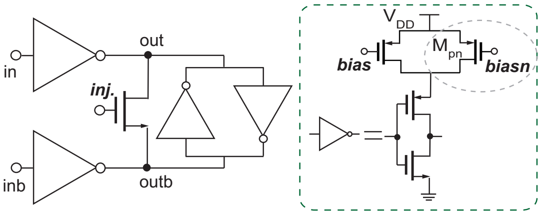


Fig. 1. Proposed differential delay cell.

B. *Topology of the Proposed Ring VCO*

Fig. 1 shows the topology of the proposed delay cell. The delay cell of this ring VCO contains a latch that generates a delay by positive feedback in order to satisfy the oscillation condition [1]. The pMOS resistive loads are used for tuning the output oscillation frequency. In the commonly used delay cells with pMOS resistive loads, the range of control voltages

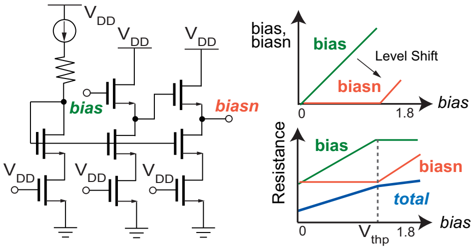


Fig. 2. Concept of a bias-level-shift circuit.

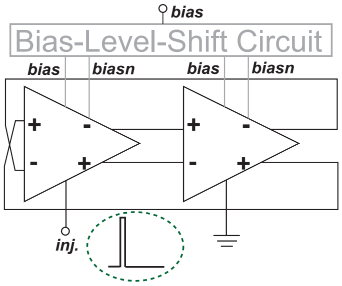


Fig. 3. Two-stage direct injection-locked differential ring VCO.

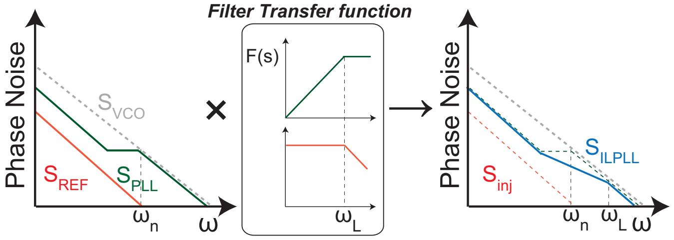


Fig. 4. Phase noise shaping with injection locking when $\omega_\mathrm{n} < \omega_\mathrm{L}$.

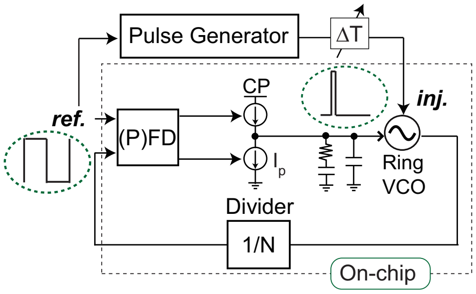


Fig. 5. Configuration of the proposed PLL.

with reasonable sensitivity is limited to that from 0 V to the pMOS threshold voltage. In the proposed delay cell, the pMOS transistors M_pn are added in order to make the range of sensitive voltages identical to the rail-to-rail voltage range (0 V to 1.8 V); this helps achieve superior controllability. For this purpose, the bias level shifted by 1 V, biasn, is applied to M_pn (Fig. 2). As a result, the total equivalent resistance of the two pMOS transistors in parallel changes fairly linearly with the main control voltage, bias. Thus, the oscillation frequency can be tuned linearly. Fig. 2 also shows the schematic of the bias-level-shift circuit.

The proposed ring VCO is shown in Fig. 3. It is based on a two-stage differential ring oscillator. The reference signal is injected into the left delay cell in the form of rail-to-rail pulses for subharmonic injection locking.

III. SUBHARMONICALLY INJECTION-LOCKED PLL

Eq. (2) shows that the phase noise originating from the reference signal is dominant at low offset frequencies because of the low-pass transfer function $H(s)$. Conversely, the phase noise of the VCO is dominant at high offset frequencies. It is known that the shape of the in-band phase noise of a PLL is identical to that in a free-running VCO and is flat at moderate offset frequencies up to the loop bandwidth, ω_n, of the PLL (Fig. 4, left) [4]. Let S_ILPLL, S_inj, and S_PLL be the phase noise power functions of an injection-locked PLL, an injected signal ($\approx S_\mathrm{REF}$), and a PLL, respectively. S_ILPLL can be expressed as

$$S_\mathrm{ILPLL} = S_\mathrm{inj} \cdot F_\mathrm{LP}(s) + S_\mathrm{PLL} \cdot F_\mathrm{HP}(s), \tag{3}$$

where $F_\mathrm{LP}(s)$ and $F_\mathrm{HP}(s)$ are low-pass and high-pass transfer functions, respectively [5]. Both $F_\mathrm{LP}(s)$ and $F_\mathrm{HP}(s)$ have the same cutoff frequency ω_L, which is known as the locking range of injection locking. The locking range is proportional to the power and the frequency of the injected signal and can be expressed as

$$\omega_\mathrm{L} \approx \frac{\omega_\mathrm{o}}{2Q} \cdot \frac{I_\mathrm{inj}}{I_\mathrm{OSC}} \cdot \frac{1}{N}, \tag{4}$$

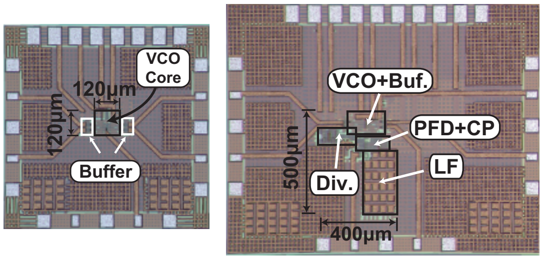
where ω_0 is the output frequency of the PLL, I_OSC is the tail current of the VCO, and I_inj is the current injected into I_OSC [6].

Eq. (3) and Fig. 4 show that the phase noise of the reference signal mainly affects the output phase noise at low offset frequencies and that the phase noise of the PLL becomes dominant as the offset frequency approaches the edge of the locking range [2], [4].

Fig. 5 shows the configuration of the proposed PLL. The injected pulses are generated by an external pulse generator that is synchronized with the reference signal. The divider used in the proposed PLL consists of differential pseudo-nMOS latches for minimizing the chip area and achieving low power consumption [7], [8]. The frequency divider can divide by 16, 24, or 36.

IV. MEASUREMENT RESULTS

Fig. 6 shows a chip micrograph of the differential ring VCO and PLL. They were fabricated by a 0.18 μm CMOS process. The area of the ring-VCO core is $120 \times 120\,\mu\mathrm{m}^2$, including the bias-level-shift circuit. The PLL circuit occupies an area of $0.1\,\mu\mathrm{m}^2$. They were measured in 1.8 V supply condition. During free-running operation, the frequency tuning range of the VCO was 0.65 GHz–1.6 GHz, and K_VCO ranged from -640 MHz/V to -380 MHz/V (Fig. 7). At an oscillation frequency of $f_0 = 1.44$ GHz, the power consumption of the VCO core was 22 mW.



(a) (b)

Fig. 6. A micrograph of (a) the proposed ring VCO and (b) PLL.

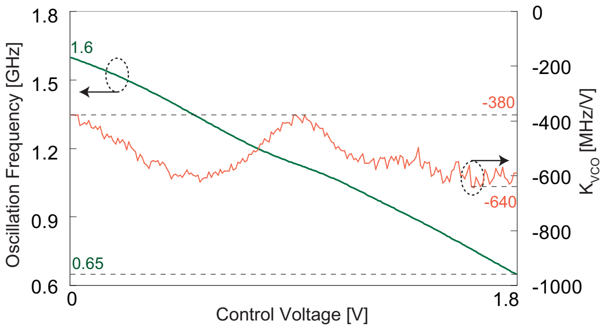
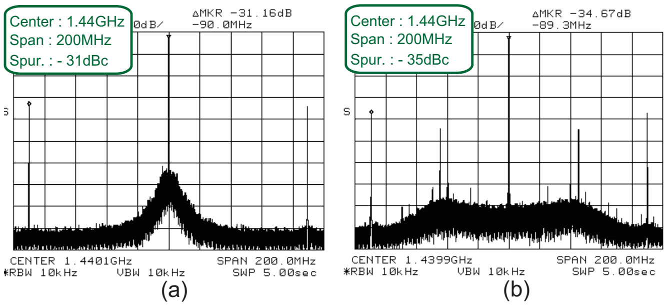


Fig. 7. Measured oscillation frequency f_0 and K_{VCO} of the free-running ring VCO, plotted against the control voltage.

Fig. 8 shows a measurement system for measuring the proposed injection-locked PLL. The reference signal is generated by an Anritsu MP1761B pulse pattern generator. 80-ps-wide injection pulses are generated by an Agilent Technologies 8133A pulse generator, which is synchronized with the MP1761B.

Fig. 9 shows frequency spectra of the PLL at $f_0 = 1.44\,\mathrm{GHz}$ with a reference signal of $f_{\mathrm{ref}} = 90\,\mathrm{MHz}$. It shows that the spurious levels without and with injection locking are, respectively, $-31\,\mathrm{dBc}$ and $-35\,\mathrm{dBc}$. They were measured using an Agilent Technologies 8563EC spectrum analyzer.

Fig. 10 shows the phase-noise characteristics at $f_0 = 1.44\,\mathrm{GHz}$, as measured by an Agilent Technologies E5052B signal source analyzer. At this frequency, the power consumption of the PLL was 39 mW. Without injection locking, a 0.2-MHz-offset phase noise of $-108\,\mathrm{dBc/Hz}$ was generated in the PLL. With injection locking, the measured phase noise was $-122\,\mathrm{dBc/Hz}$ at an offset of 0.2 MHz.



(a) (b)

Fig. 9. Measured output frequency spectra of the PLL (ref. = 90 MHz) (a) without and (b) with injection locking.

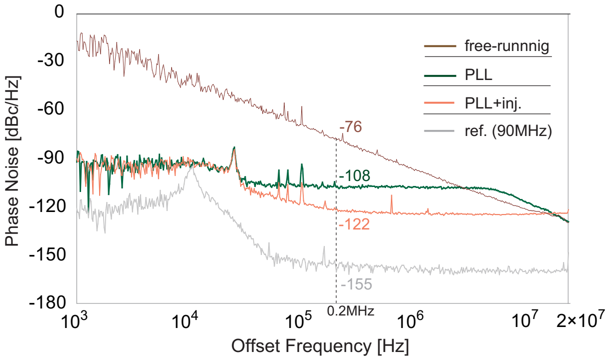


Fig. 10. Phase noise measured at $f_0 = 1.44\,\mathrm{GHz}$.

Fig. 11 shows the measured spurious level and phase noise without injection locking for a divider ratio of 16. The spurious level and the phase noise do not change significantly with the reference frequency within the stable operating region of the charge pump (I_{P} = constant), as indicated in the graph.

Fig. 12 shows the jitter characteristics at $f_0 = 1.44\,\mathrm{GHz}$, as measured by an Agilent Technologies 86100C digital communication analyzer. Without injection locking, the measured overall rms and peak-to-peak jitters were 2.4 ps and 16 ps, respectively. With injection locking, the rms jitter was 1.9 ps and the peak-to-peak jitter was 16 ps.

A performance summary and comparison with other PLLs that employ various phase-locking techniques are presented in Table I. The proposed circuit shows good phase noise value

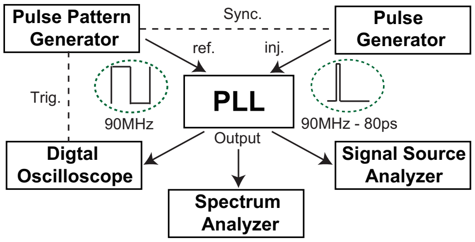


Fig. 8. Measurement system.

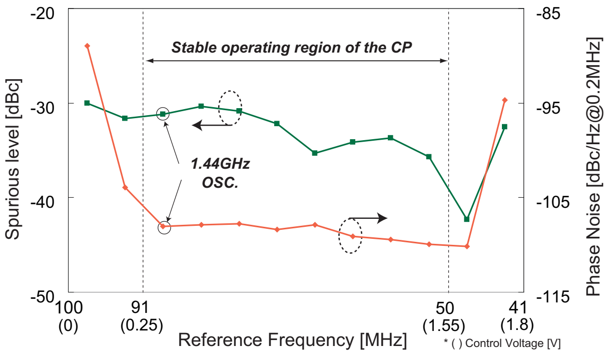


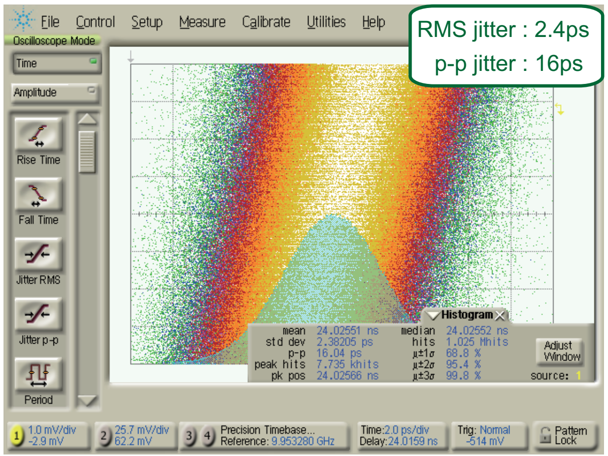
Fig. 11. Measured spurious level and phase noise without injection locking versus the reference frequency of the PLL ($N = 16$).

TABLE I

PERFORMANCE SUMMARY AND COMPARISON OF PLLS.

Ref.	CMOS Technology	f_o [GHz]	f_o/f_{ref}	FTR* [%]	Phase Noise [dBc/Hz]	Offset [MHz]	Power [mW]	Area [mm^2]	VCO	Method
This work	0.18 μm	1.44	16	84	**−108**	0.2	39	0.1	Ring	PLL
	·	·	·	·	**−122**	0.2	·	·	·	PLL + Injection locking
[5]	0.18 μm	1.92	24	75	−126	1	55**	0.031	Ring	Injection locking
[9]	0.13 μm	2.0	8	100	−125	0.6	23	0.07	Ring	PLL
[10]	90 nm	0.8	8	143	−122	0.2	15	0.048	Ring	PLL + MDLL
[11]	0.18 μm	2.2	40	N/A	−126	0.2	7.6	0.18	LC	PLL
[12]	0.13 μm	2.0	50	27	−102	in-band	25	0.8	LC	ADPLL

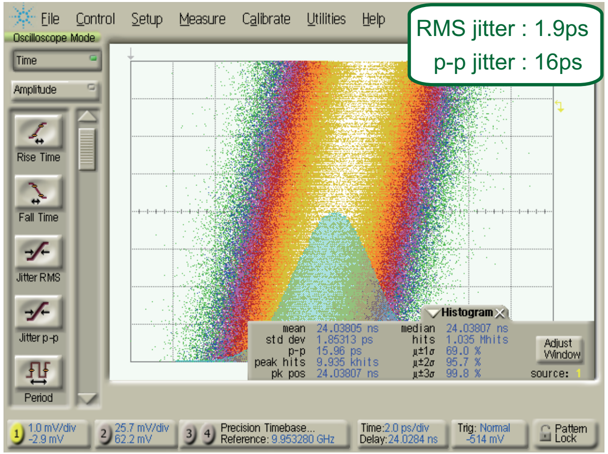
*(Frequency tuning ratio) = (Tuning range)/(Center frequency). **Includes current in the LDO.



```
     mean  24.02551 ns     median  24.02552 ns
  std dev  2.38205 ps        hits  1.025 Mhits
      p-p  16.04 ps          µ±1σ  68.8 %
peak hits  7.735 khits       µ±2σ  95.4 %
   pk pos  24.02566 ns       µ±3σ  99.8 %
source: 1
```

1.0 mV/div -2.9 mV | 25.7 mV/div 62.2 mV | Precision Timebase... Reference: 9.953280 GHz | Time: 2.0 ps/div Delay: 24.0159 ns | Trig: Normal -514 mV

(a)



```
     mean  24.03805 ns     median  24.03807 ns
  std dev  1.85313 ps        hits  1.035 Mhits
      p-p  15.96 ps          µ±1σ  69.0 %
peak hits  9.935 khits       µ±2σ  95.7 %
   pk pos  24.03807 ns       µ±3σ  99.8 %
source: 1
```

1.0 mV/div -2.9 mV | 25.7 mV/div 62.2 mV | Precision Timebase... Reference: 9.953280 GHz | Time: 2.0 ps/div Delay: 24.0284 ns | Trig: Normal -514 mV

(b)

Fig. 12. Measured jitter characteristics (a) without injection locking and (b) with injection locking at $f_0 = 1.44$ GHz.

and wide frequency tuning range with a comparable area.

V. CONCLUSION

We proposed a low-phase-noise wide-frequency-range injection-locked PLL based on a differential ring VCO. By using a bias-level-shift circuit and pMOS resistive loads, we successfully suppressed variations in the spurious level and the phase noise across the tuning range in the stable operating region of the charge pump.

The injection-locked PLL was fabricated by adopting 0.18 μm CMOS technology. A 0.2-MHz-offset phase noise of -122 dBc/Hz was achieved at an output frequency of 1.44 GHz. The area of the PLL was as small as 0.1 mm^2 and the frequency tuning range was as wide as FTR = 84%.

ACKNOWLEDGMENTS

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