論文 / 著書情報
Article / Book Information

論題(和文)	
Title(English)	Wide-band, high linear low noise amplifier design in 0.18um CMOS
著者(和文)	ﾑｰｻ ｵﾄﾏﾝ, 天川 修平, 石原 昇, 益 一哉
Authors(English)	Mousa M. Othman, Shuhei Amakawa, Noboru Ishihara, Kazuya Masu
出典(和文)	, Vol. 7, No. 11, pp. 759-764
Citation(English)	IEICE Electronics Express, Vol. 7, No. 11, pp. 759-764
発行日 / Pub. date	2010, 6
URL	http://search.ieice.org/
権利情報 / Copyright	本著作物の著作権は電子情報通信学会に帰属します。 Copyright (c) 2010 Institute of Electronics, Information and Communication Engineers.

IEICE Electronics Express, Vol.7, No.11, 759–764

Wide-band, high linear low noise amplifier design in 0.18 um CMOS technology

Mousa M. Othman, Shuhei Amakawa, Noboru Ishihara, and Kazuya Masu[a)]

Integrated Research Institute, Tokyo Institute of Technology

4259-R2-17 Nagatsuta, Midori-ku, Yokohama 226–8503, Japan

a) *paper@lsi.pi.titech.ac.jp*

Abstract: This paper describes a technique to improve the linearity of low noise amplifier (LNA) that is implemented by the shunt-shunt feedback (SSFB) topology. By employing a parallel positive/negative feedback a suppression of the 2nd order harmonic distortion (OHD) in the feedback loop can be achieved which will result in minimization of the IM3 that is produced by mixing of this 2nd OHD with the input signal leading to an improvement of the LNA IIP3. Two LNA were fabricated using 180 nm CMOS technology one adopting the conventional SSFB that was described in [1] and another one using our proposed linearization technique where an average improvement of +8 dBm of IIP3 is achieved while maintaining quite similar minimum noise figure of 2.8 dB, 3-dB bandwidth of 3.7 GHz. Each of the fabricated LNAs consumes a current of 7.8 mA from 1.8 V power supply and occupies 0.007 mm^2.

Keywords: low noise amplifier (LNA), harmonic distortion, IIP3, IM3, shunt-shunt feedback

Classification: Integrated circuits

References

[1] J. Borremans, et al., "Low-area active-feedback low-noise amplifier design in scaled digital CMOS," *IEEE J. Solid-State Circuits*, vol. 43, no. 11, pp. 2422–2433, Nov. 2008.

[2] D. Manstretta, "A broadband low-noise single-ended input differential output amplifier with IM2 cancelling," *Radio Frequency Integrated Circuits Symposium*, pp. 79–82, June 2008.

[3] B. Razavi, *Design of analog CMOS integrated circuits*, McGraw-Hill, 2001.

[4] N. Kim, et al., "A highly linear SAW-less CMOS receiver using a mixer with embedded Tx filtering for CDMA," *IEEE J. Solid-State Circuits*, vol. 44, no. 8, pp. 2126–2137, Aug. 2009.

[5] Z. Ru, et al., "A software-defined radio receiver architecture robust to out-of-band interference," *International Solid-State Circuits Conference*, pp. 230–231, Feb. 2009.

DOI: 10.1587/elex.7.759
Received April 06, 2010
Accepted April 30, 2010
Published June 10, 2010

IEICE Electronics Express, Vol.7, No.11, 759–764

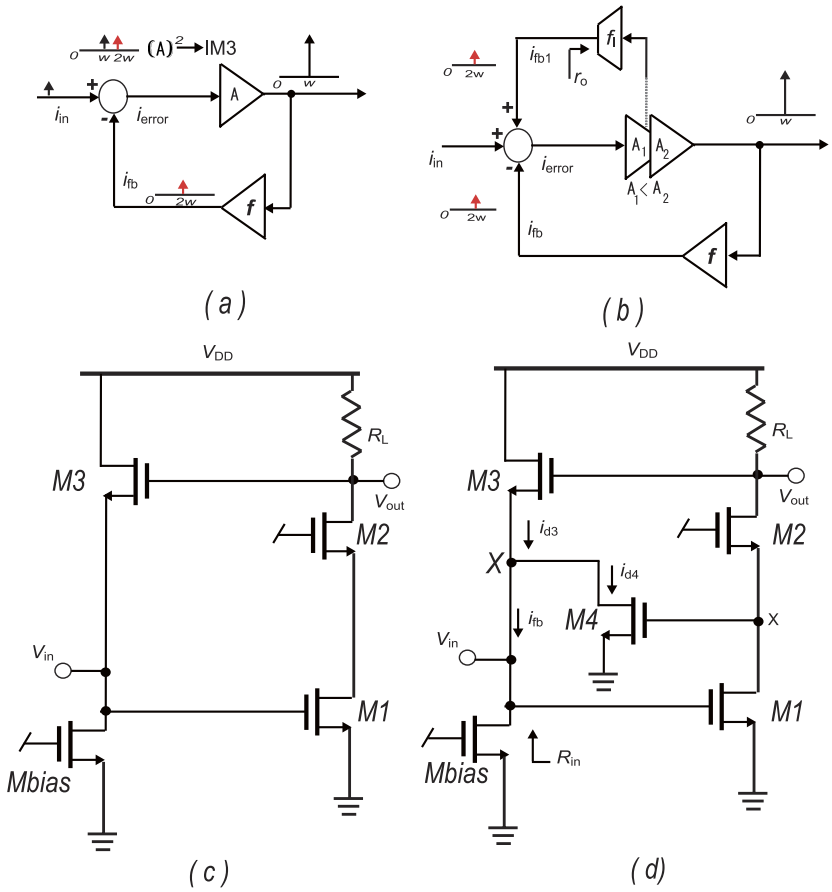

Fig. 1. (a) Conventional SSFB. (b) Parallel negative/positive feedback. (c) Circuit implementation of a. (d) Circuit implementation of b.

1 Introduction

One of the most attractive RF front-end architectures to implement the upcoming multi-standard/software-defined radios is the Zero-IF architecture due to lower cost and bill-of-material. But the required linearity that should be fulfilled in order to avoid the down conversion of the out of band IM3 products that may overlap on the wanted signal [2, 4, 5] forms a technical challenge in its realization. Using multi center-frequency SAW filter between the output of LNA and the input of mixer to suppress the out of band IM3 products that are produced by the LNA seems to be a non-practical solution since the SAW filter is a bulky, expensive and off chip, even in narrow-band applications avoiding SAW filter is of a big interest [4].On the another hand enhancing the linearity performance of the RF front-end by means of modifying the system itself can be achieved on the cost of complexity, power and area [4, 5]. So a compromised design is required in which the realization of wide-band, high linear LNA with low NF is essential to relax the needed system modifications to avoid the usage of SAW filter in order to achieve the required wide-band RF front-end linearity.

SSFB topology with active feedback network is an attractive to implement a wide band LNA [1] where bandwidth expanding can be achieved along with

DOI: 10.1587/elex.7.759
Received April 06, 2010
Accepted April 30, 2010
Published June 10, 2010

sufficient input matching while using small chip area, but with poor linearity performance and this is due to the fact that the 2nd OHD of the active feedback (source follower SF) will mix with the input signal and generate 3rd order cross modulation products (IM3) at the output of the LNA that will degrade its IIP3. By applying a parallel positive/negative feedback a reduction in the 2nd OHD current in the feedback loop can be achieved resulting in an enhancement of the obtained IIP3.

2 Concept of Distortion Cancellation

Fig. 1 (a) shows general SSFB block diagram with feedback (f) that is active (SF in the implemented circuit), the 2nd OHD current of f will mix with v_{in} and squared by the nonlinearity of main amplifier (A) resulting in an IM3 product that will degrade the overall IIP3 performance [1]. One way to reduce the 2nd OHD current in the feedback loop is by applying a parallel positive feedback (f_1) as shown in Fig. 1 (b) by this a subtraction of the 2nd OHD current will occur at the input leading to a considerable reduction of the IM3 at the output. Since the SSFB will be employed to implement LNA, the input matching is of an interest for this reason the positive feedback should have as minimum effect on the input impedance as possible, for this purpose f_1 is chosen to have high output impedance r_o (common source CS in the implemented circuit). Moreover, the net feedback current (fundamental harmonic) should be negative to avoid oscillation and this can be guaranteed by making $i_{fb} > i_{fb1}$. These issues will be discussed extensively in the next section in terms of the implemented circuit parameters.

3 Circuit Implementation

Fig. 1 (c) shows a possible implementation of the general feedback block diagram that is shown in Fig. 1 (a) [1] where M2 (cascode) is used to reduce the miller multiplication effect of c_{gd1} on the input node [3], Fig. 1 (d) shows the modified circuit using the linearization technique that was described in (Fig. 1 (b)), here M4 is playing the role of positive feedback. For small signal operation, the nonlinear transconductance of MOS transistors i_{d} is represented by the power series $\frac{1}{(n+1)!}\sum_{\mathrm{n=0}}^{2}\frac{\partial^n(g_{\mathrm{m}})}{\partial(V_{\mathrm{GS}})^n}v_{\mathrm{gs}}^{n+1}$, considering that at frequencies well below f_T the voltage gain $\frac{v_{out}}{v_{in}}$ can be expressed as $\frac{v_{out}}{v_{in}} \approx -g_{m1}R_L$, 2nd OHD cancellation in the feedback loop can be achieved when $\frac{1}{2}g_{m3}{}'v_{gs3}^2 = \frac{1}{2}g_{m4}{}'v_{gs4}^2$ where $v_{gs3} = -\left(1+g_{m1}R_L\right)v_{in}$ and $v_{gs4} = -\frac{g_{m1}}{g_{m2}}v_{in}$ i.e.:

$$\frac{g_{m3}{}'}{g_{m4}{}'} = \left(\frac{g_{m1}g_{m2}^{-1}}{1+g_{m1}R_L}\right)^2 \tag{1}$$

to minimize the Miller multiplication effect of c_{gd1} and c_{gd4} on the input node the numerator of the right hand side of (1) must be as small as possible [3], using the square law model of MOS transistor (1) can be rewritten as follows :

$$\frac{(W/L)_3}{(W/L)_4} = \frac{\left(g_{m1}g_{m2}^{-1}\right)^2}{\left(1+g_{m1}R_L\right)^2} \tag{2}$$

DOI: 10.1587/elex.7.759
Received April 06, 2010
Accepted April 30, 2010
Published June 10, 2010

to have a sufficient input matching R_{in} in (Fig. 1 (d)) must equal to R_S (50 Ω) i.e. $R_S = \frac{g_{m3}^{-1}//r_{o4}}{1+g_{m1}R_L}$, taking this into account and using the transconductance expression that is given by $g_m = \sqrt{(2C_{ox}\mu I_D\,(W/L))}$, M4 aspect ratio to meet (2) can be derived in terms of g_{m3}, R_S and the dimensions of M1-M3 as following:

$$(W/L)_4 = \frac{(W/L)_2\,(W/L)_3}{(W/L)_1\,(g_{m3}R_S)^2} \tag{3}$$

to minimize the thermal noise contribution of M4 its channel is set to its maximum available length to achieve higher channel area (in case of TSMC CMOS 180 nm it is 0.5 um) where the penalty of the added parasitic capacitance will have a negligible effect on the bandwidth.

To guarantee that the net feedback in the circuit shown in Fig. 1 (d) is negative one (i.e. not oscillator), i_{fb} must be larger than i_{d4} this can be expressed in terms of the circuit parameters as following :

$$\frac{g_{m3}}{g_{m4}} > \frac{g_{m1}g_{m2}^{-1}}{1+g_{m1}R_L} \tag{4}$$

by substituting (2) into (4), the condition to maintain negative feedback is by keeping $I_{D3} > I_{D4}$ (biasing currents).

4 Measurement Results

To verify the effectiveness of the proposed linearization technique, the two LNAs that are shown in Fig. 1 were fabricated using 180 nm CMOS technology with standard V_{th}. The active area of each of them is $50 \times 80\,\mu\text{m}^2$ and the chip microphotograph is shown in Fig. 2 (a). The measured frequency response is shown in Fig. 2 (b) where a gain of 11.3 dB is obtained over a 3 dB BW of 3.5 GHz while keeping $S_{11} < -10$ dB and isolation coefficient $S_{12} < -20$ dB in the entire achieved bandwidth of both LNAs, basically the similar S-Parameter performance is due to the fact that M4 in Fig. 1 (d) has a relatively small dimensions so that its parasitic capacitance c_{gd4} has a negligible effect on input node, moreover c_{gs4} effect at node x (Fig. 1 (d)) will be also negligible since (g_{m2}^{-1}) is small.

NF was measured by NF meter and minimum NF of 2.7 dB is achieved while having $NF < 3$ dB in the range of [1–3.5] GHz as shown in Fig. 2 (c).

To examine the linearity enhancement of the proposed technique two-tones spaced by 150 MHz with a swept center frequency was applied to both LNAs that are shown in Fig. 1. Fig. 2 (d) shows the measured IIP3 of both LNA where an average improvement of 9 dBm is achieved. It was found that the harmonic cancellation method will hold to a blockers level up to -18 dBm.

5 Conclusion

An efficient linearization technique for the SSFB topology was presented where by using parallel negative/positive feedback a suppression of the 2nd OHD in the feedback loop can be achieved leading to a minimization of the

DOI: 10.1587/elex.7.759
Received April 06, 2010
Accepted April 30, 2010
Published June 10, 2010

Table I. Comparison between Conventional and Modified LNA.

	Conventional LNA	Modified LNA
Gain [dB]	11.3	11.2
S_{11} [dB]	≤ -10	≤ -10
BW [GHz]	3.5	3.5
min. NF [dB]	2.7	2.8
Power [mW]	14.1	14
IIP3 [dBm]	-9	1

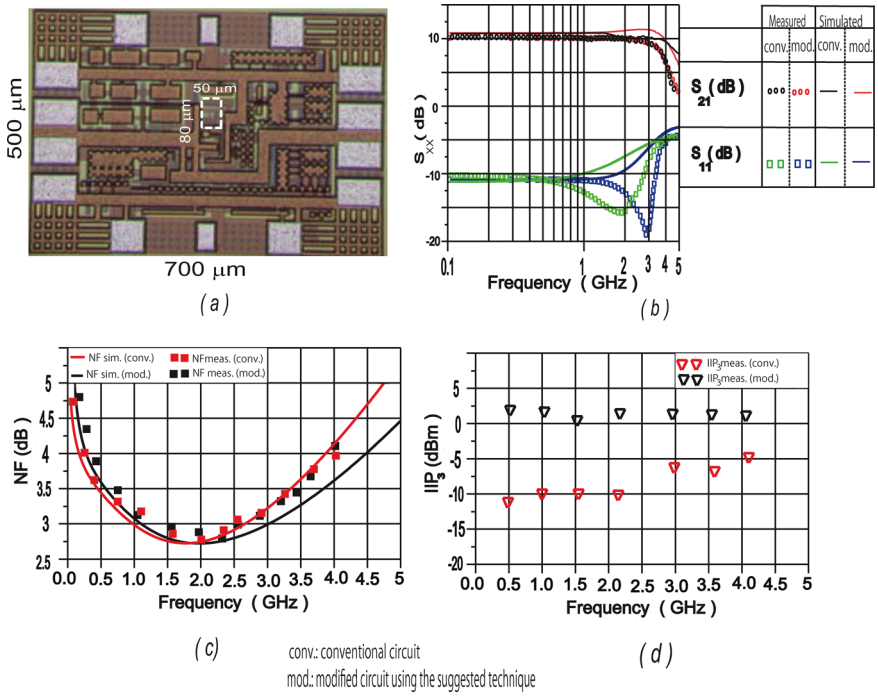

Fig. 2. (a) Chip microphotograph. (b) S-Parameters. (c) Noise figure. (d) IIP3 obtained from applying two-tones spaced by 150 MHz.

IM3 that is produced from mixing between this 2nd OHD and the input signal by the main amplifier non-linearities resulting in an overall IIP3 enhancement. Two LNA were fabricated using 180 nm CMOS technology one adopting the conventional SSFB and another using the proposed linearization technique where IIP3 enhancement of +8 dBm obtained while maintaining a minimum noise figure of 2.8 dB, 3-dB bandwidth of 3.7 GHz and power gain of 11.3 dB. Each of the fabricated LNAs consumes a current of 7.8 mA drawn from 1.8 V power supply and occupies 0.007 mm^2.

Acknowledgment

This work was partially supported by STARC, MIC.SCOPE, JSPS.KAKENHI, MEXT.KAKENHI, NEDO, Special Coordination Funds for Promoting Science and Technology, and VDEC in collaboration with Cadence Design

DOI: 10.1587/elex.7.759
Received April 06, 2010
Accepted April 30, 2010
Published June 10, 2010

Systems, Inc., Agilent Technologies Japan, Ltd., Mentor Graphics, Inc. The authors would like to thank Prof. A. Matsuzawa for discussions, T. Nakajima and M. Oturu for help in measurements, and T. Maekawa for technical assistance. M.M.O. thanks MONBUKAGAKUSHO for scholarship.

DOI: 10.1587/elex.7.759
Received April 06, 2010
Accepted April 30, 2010
Published June 10, 2010