Low-Phase-Noise Wide-Frequency-Range Differential Ring-VCO with Non-Integral Subharmonic Locking in 0.18 μm CMOS

Sang_yeop Lee #1, Shuhei Amakawa #2, Noboru Ishihara #3, Kazuya Masu #4

Integrated Research Institute, Tokyo Institute of Technology
4259-R2-17 Nagatsuta, Midori-ku, Yokohama 226-8503, Japan
1 lee.s.af@m.titech.ac.jp
2 amakawa.s.aa@m.titech.ac.jp
3 ishihara.n.aa@m.titech.ac.jp
4 masu.k.aa@m.titech.ac.jp

***Abstract*—A low-phase-noise ring voltage-controlled oscillator (VCO) with subharmonic injection locking is presented. The ring VCO topology is designed to obtain not only an acceptable spurious level but also satisfactory phase-noise characteristics by enabling the use of short-pulse-width injection signals (83.3 ps). We also present the measurement results in the case of non-integral subharmonic locking such as quarter-integral subharmonic locking and half-integral subharmonic locking.**

The proposed VCO has a wide frequency tuning range, namely, 0.62–1.5 GHz. This range is realized by combining pMOS resistive loads and a circuit for shifting the bias level. Thus, rail-to-rail voltages can be used for control. The 1-MHz-offset phase noise of the VCO is -126 dBc/Hz at an output frequency of 1.35 GHz ($= 13.5 \times 100$ MHz) and a spurious level of -48 dBc. At a spurious level of -40 dBc, the phase noise of the VCO at the same frequency ($= 6.75 \times 200$ MHz) is -126 dBc/Hz. At a VCO output frequency of 1.35 GHz, the power consumption from a 1.8 V power supply is 41 mW. The VCO was fabricated by 0.18 μm CMOS technology and occupies an area of 0.014 mm^2.

***Index Terms*—Ring-VCO, injection-locked oscillator, subharmonic locking, low phase noise, CMOS**

I. Introduction

Conventional multistandard wireless mobile terminals contain multiple RF front-end chips. To reduce production costs, one-chip RF LSI systems are needed. A great effort is being made to develop wideband and/or multiband RF solutions by adopting highly scaled advanced CMOS processes. The use of such processes will improve the performance of A/D and D/A converters and digital baseband circuits. However, it is very difficult to reduce the size of RF/analog circuits, especially power amplifiers and oscillator circuits that include voltage-controlled oscillators (VCOs) and phase-locked loops (PLLs), because of the presence of inductors that do not scale with advances in technology.

Ring-oscillator-based VCOs are attractive since they occupy a small area and have a wide frequency tuning range. Unfortunately, a ring-oscillator-based VCO cannot be used in cellular phones or WLANs that require high frequency resolution; this is because its phase-noise characteristics are inferior compared to the characteristics desired at its levels of power consumption.

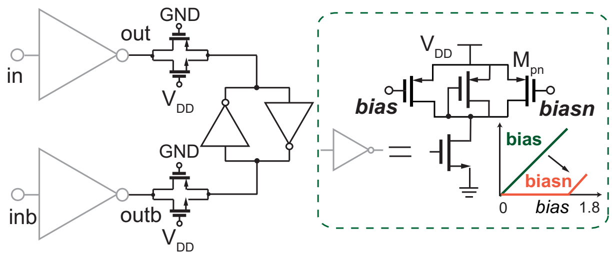

Fig. 1. Proposed differential delay cell.

Nevertheless, a low-phase-noise ring VCO can be obtained if a noise-suppression mechanism can be included in the VCO. Injection locking is one such mechanism. A paper on half-integral subharmonic injection locking based on the use of a ring VCO has been presented; this type of locking serves as a powerful means of realizing low-phase-noise high-resolution ring VCOs [1].

This paper is organized as follows. In Section II, the proposed circuit topology for decreasing the phase noise characteristic is presented. In Section III, non-integral subharmonic injection locking due to the topology of the proposed ring VCO is described. In Section IV, the measurement results for a VCO implemented by adopting a 0.18 μm CMOS process are presented. The conclusions of this work are presented in Section V.

II. Design of the Differential Injection-Locked Ring VCO

Fig. 1 shows the topology of the proposed delay cell. The delay cell of the proposed ring VCO contains a latch that generates a delay variation by positive feedback in order to satisfy the oscillation condition [2].

CMOS inverters have been used in the latch in order to simplify the design and achieve a rail-to-rail output voltage swing. The rail-to-rail output swing is expected to result in lower phase noise. Because the single-sideband phase-noise spectrum decreases as the charge swing $q_{\max}$ increases in

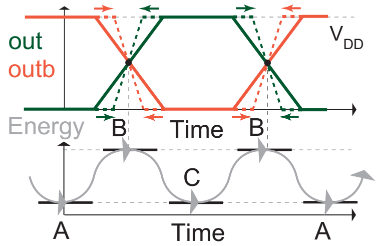

Fig. 2. Voltage waveforms and potential energy versus time.

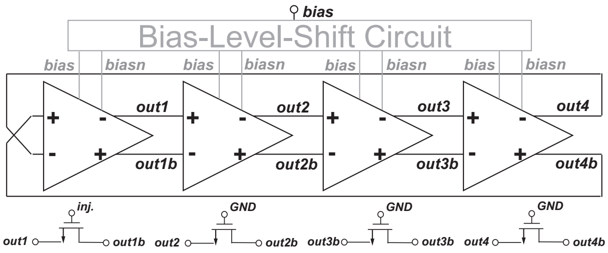

Fig. 3. Four-stage direct-injection-locked differential ring VCO.

eq. (1).

$$L\{\Delta f\} = \frac{\Gamma_{\rm rms}^2}{8\pi^2 \Delta f^2} \cdot \frac{\overline{i_{\rm n}^2}/\Delta f}{q_{\rm max}^2}. \quad (1)$$

In eq. (1), $\Gamma_{\rm rms}$ is the rms value of the impulse sensitivity function (ISF) [3]. The characteristics of the latch also affect $\Gamma_{\rm rms}$.

Fig. 2 shows the approximate voltage waveforms as well as how the potential energy evolves with time in an oscillation cycle [4]. When the output voltage is at point A or C, the latch resists perturbation and tries to maintain the HI or LO output voltage. But once the time has passed a point B in Fig. 2, the latch enters a positive feedback phase and quickly descends to a stable point A or C. Altogether, the latch works to elongate the flat parts of the voltage waveforms and to make switching faster. Thus, $\Gamma_{\rm rms}$ in eq. (1) should decrease.

The pMOS resistive loads are used for tuning the output frequency. Biasn, the bias level shifted by 1 V from the main control voltage is applied to a pMOS, $M_{\rm pn}$, in order to ensure that the total equivalent resistance of the two pMOS resistive loads is linear with respect to the main control voltage, bias. Therefore, tuning the oscillation frequency while maintaining the $K_{\rm VCO}$ across the tuning range of the VCO can be achieved.

The proposed ring VCO is shown in Fig. 3. It is based on a four-stage differential ring oscillator. To achieve subharmonic injection locking, four nMOS switches are connected at the nodes between which there is a phase difference of 540 deg. To achieve injection locking, rail-to-rail pulses are injected into one of switches.

III. Non-Integral Subharmonic Injection Locking

For simplicity, let us consider integral and half-integral subharmonic locking, namely $f_{\rm o} = 2f_{\rm inj}$ and $f_{\rm o} = 1.5f_{\rm inj}$ (Figs. 4 (a), (b)). The two output nodes are shorted when the injection signal is inputted into the nMOS switches. Phase

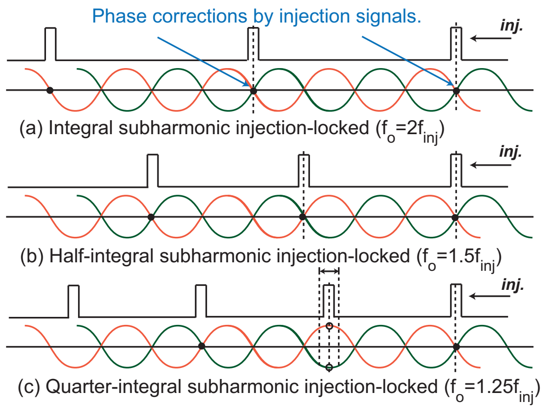

Fig. 4. Voltage waveforms of signals at output nodes and injection signals versus time.

corrections may occur at the time, and the jitter reduced. Generally, there are two points of time during the period of the output signal when two output nodes can be shorted because of topological symmetry. Consequently, the VCO is capable of both integral and also half-integral subharmonic locking [1].

Fig. 4 (c) shows waveforms in the case of quarter-integral subharmonic injection locking. In this case, we see that quarter-integral subharmonic injection locking can be attained only when phase shifts due to the pulse that is injected into a peak point of the output swing are almost zero. This locking phenomenon resembles that in the case of half-integral subharmonic injection locking, i.e., $f_{\rm o} = 2.5f_{\rm inj}$. Let us consider Fig. 2 one more time. Suppose that the difference between maximum and minimum potential energies is sufficiently large and the pulse width is sufficiently short. The pulse injected at the unstable point B could result in the phase shift easily even though the pulse width is short, because the potential energy at the unstable point is much higher than that at the stable point. In contrast, the pulse injected at the stable point A or C could not result in the phase shift easily because the external injection energy produced by the injection pulse was relatively lower than that at the unstable point. The characteristics of the proposed VCO, such as the rail-to-rail output voltage swing and fast rise and fall times of the waveforms, are attributed to the effect of inverter latches. Consequently, quarter-integral as well as half-integral subharmonic locking can be easily realized using a short-pulse-width injection signal in the proposed topology.

IV. Measurement Results

Fig. 5 (a) shows a chip micrograph of the proposed ring-VCO. The VCO was fabricated by a 0.18 μm CMOS process. The area of the ring-VCO core is $80 \times 180\,\mu{\rm m}^2$, including the circuit for shifting the bias level. Fig. 5 (b) shows the frequency tuning range of the proposed ring VCO. The range was measured for a 1.8 V power supply. The frequency tuning range in the free-running condition of the VCO was 0.62–1.5 GHz. At an oscillation frequency of f_0=1.35 GHz, the power consumption of the VCO core was 41 mW.

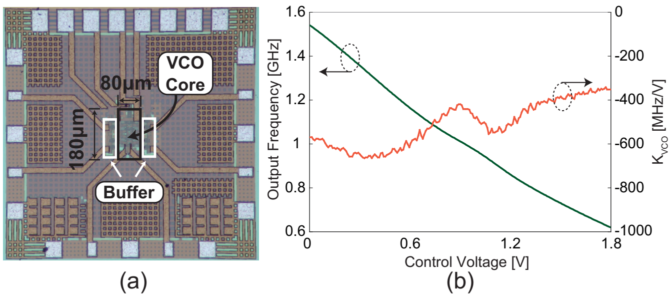

Fig. 5. (a) A micrograph of the proposed ring VCO, (b) measured output frequency and K_{VCO}.

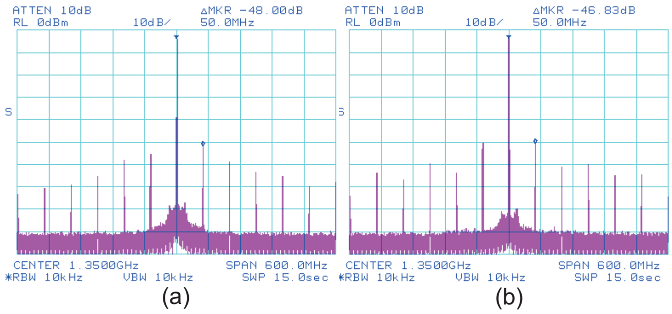

Fig. 6. Measured output frequency spectrum of the VCO output at f_0=1.35 GHz, with a reference input of (a) f_{inj}=50 MHz and (b) f_{inj}=100 MHz.

Reference input pulses with a width of 83.3 ps were generated by an Anritsu MP1761B pulse pattern generator. Fig. 6 shows a frequency spectrum of VCO outputs at f_0=1.35 GHz for a reference input of f_{inj}=50 MHz and f_{inj}=100 MHz under injection locking. The measured spurious levels for the reference inputs of 50 MHz and 100 MHz were -48 dBc and -47 dBc, respectively as measured by an Agilent Technologies 8563EC spectrum analyzer.

Fig. 7 shows the phase-noise characteristics at f_0=1.35 GHz in the free-running condition and under injection locking, with a reference input of f_{inj}=50 MHz and f_{inj}=100 MHz. The 1-MHz-offset phase noise of the VCO was -101 dBc/Hz in the former condition. The 1-MHz-offset phase noise of the VCO in the case of integral subharmonic injection locking (=27×50 MHz) was -120 dBc/Hz and that in the case of half-integral subharmonic injection locking (=13.5×100 MHz) was -126 dBc/Hz. These values were measured using an Agilent Technologies E5052B signal source analyzer.

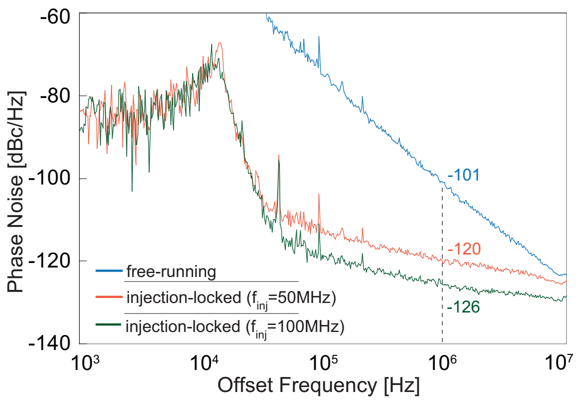

Fig. 7. Measured phase noise at f_0=1.35 GHz for a reference input of f_{inj}=50 MHz and f_{inj}=100 MHz.

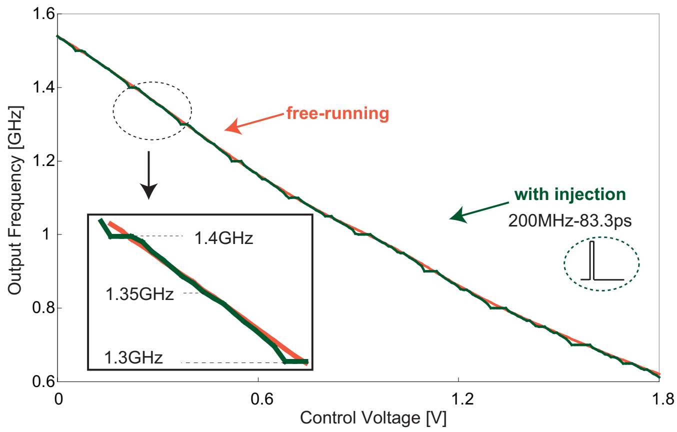

Fig. 8. Frequency tuning range for a reference input of f_{inj}=200 MHz.

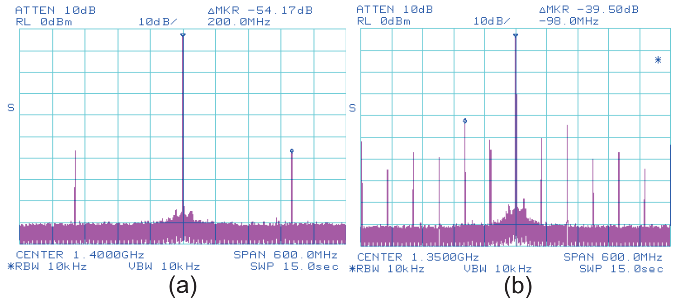

Fig. 9. Measured output frequency spectrum of the VCO output (f_{inj} = 200 MHz) (a) N=7, (b) N=6.75 ($N = f_{\mathrm{out}}/f_{\mathrm{inj}}$).

Fig. 8 shows VCO responses with and without a reference input of f_{ref} = 200 MHz. As the control voltage was swept, the VCO successfully locked to the integral and half-integral subharmonics. The figure also shows that the non-integral subharmonic injection locking occurs at significantly lower frequencies than the VCO output frequency of 1.2 GHz, e.g., quarter-integral subharmonic injection locking at f_{inj}=200 MHz.

Fig. 9 and Fig. 10 shows frequency spectra and phase-noise characteristics for a reference input of f_{inj}=200 MHz. In the case of quarter-integral subharmonic injection locking at f_0=1.35 GHz (=6.75×200 MHz), the measured spurious level was -40 dBc and the 1-MHz-offset phase noise was -126 dBc/Hz. We can observe that the phase-noise characteristic at f_0=1.35 GHz for a reference input of f_{inj}=200 MHz is almost identical to that for a reference input of f_{inj}=100 MHz.

Fig. 11 shows the jitter characteristic at $f_0 = 1.35$ GHz, as measured by an Agilent Technologies 86100C digital communication analyzer. For a reference input of f_{inj}=200 MHz, the overall rms jitter was measured to be 1.5 ps.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON OF PLLS.

Ref.	Technology	f_o [GHz]	f_o/f_{ref}	FTR* [%]	Phase Noise [dBc/Hz]	Offset [MHz]	Power [mW]	Spur. [dBc]	Area [mm^2]	Method
This work	0.18 μm	1.35	27	85	**−120**	1	41	−48	0.014	Injection locking
	·	·	13.5	·	**−126**	·	·	−47	·	·
	·	·	6.75	·	**−126**	·	·	−40	·	·
[1]	0.18 μm	1.92	24	75	−126	1	55**	N/A	0.031	Injection locking
	·	1.88	23.5	·	−122	1	·	−20	·	·
[5]	0.18 μm	2.0	10	N/A	−108	1	0.2	−39	0.0001	Injection locking
[6]	90 nm	2.0	23	70	−120	0.2	13	−39	0.008	Phase alignment†
[7]	90 nm	0.8	8	143	−122	0.2	15	−48	0.048	PLL +MDLL

*Frequency Tuning Ratio: Tuning Range/Center Frequency **Includes current in the LDO. † Based on injection locking.

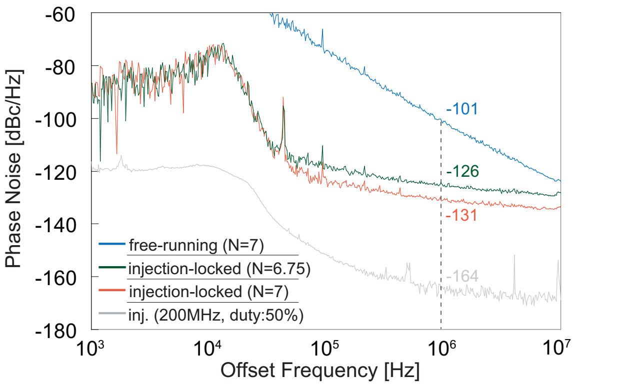

Fig. 10. Measured phase noise of the VCO (f_{inj} = 200 MHz, N = f_{out}/f_{inj}).

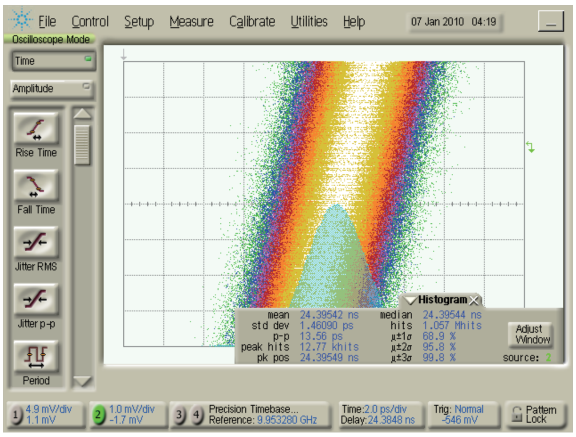

Fig. 11. Measured jitter characteristics at f_0=1.35 GHz for f_{inj}=200 MHz.

A summary of the performance of the proposed ring VCO and a comparison of the proposed ring VCO with other VCOs and PLLs that were designed using various kinds of phase-locking methods are given in Table I. The proposed circuit has low phase noise value and a wide frequency tuning range. Also its area is small and comparable to that of other circuits.

V. CONCLUSION

We proposed a ring-VCO topology for (1) achieving low-phase-noise characteristics with non-integral subharmonic locking and (2) reducing the spurious level by enabling the use of a short-pulse-width signal. Non-integral subharmonic locking enables the use of higher frequency of reference signals with the same frequency resolution. The characteristics of the VCO are attributed to the rail-to-rail output signal of the VCO and the positive feedback of inverter latches. It also implies that the VCO has characteristics that are intermediate between those of frequency multipliers and dividers.

The VCO was fabricated by 0.18 μm CMOS technology. In the case of half-integral subharmonic injection locking ($= 13.5 \times 100$ MHz) and quarter-integral subharmonic injection locking ($= 6.75 \times 200$ MHz), the 1-MHz-offset phase noise of the VCO was −126 dBc/Hz at an output frequency of 1.35 GHz; the VCO also has a wide tuning range and a comparable small area of 0.014 mm^2.

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