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PAPER Special Section on Analog Circuit Techniques and Related Topics

Capacitance Reduction Technique for Switched-Capacitor Circuits Based on Charge Distribution and Partial Charge Transfer

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SUMMARY This paper proposes a technique to reduce the capacitance spread in switched-capacitor (SC) filters. The proposed technique is based on a simple charge distribution and partial charge transfer which is applicable to various integrator topologies. An implementation example on an existing integrator topology and a design example of a 2nd-order SC low-pass filter are given to demonstrate the performance of the proposed technique. A design example of an SC filter show that the filter designed using the proposed technique has an approximately 23% less total capacitance than the one of SC low-pass filter with conventional capacitance spread reduction technique.

key words: *switched capacitor, filter, capacitance spread*

1. Introduction

Filters have been one of the important analog circuit blocks in signal processing. There are various filter implementations such as passive RC filters, active RC filters [1]–[4], Gm-C filters [5]–[14], and SC filters [15]–[20]. Among those well known filter topologies, switched-capacitor filters have been noticed for its low sensitivity to parameter deviation. However, in practical implementations, SC filters need continous-time (CT) filters at their input and output (Fig. 1) to prevent aliasing and to reduce undesired spectrum due to switching operation at the output of the filters.

The order of the CT filters will be proportional to the ratio of SC filter's cutoff frequency and clock frequency, which is also known as over sampling ratio (*OSR*) where

$$OSR = \frac{\text{sampling frequency}(f_s)}{\text{cutoff frequency}(f_0)}. \quad (1)$$

When the over sampling ratio is small, i.e. the sampling frequency is closer to the cutoff frequency, higher order CT filters are required. The higher the order is, the bigger the size of CT filters will be. In particular, for low frequency applications, the size of CT filters will become more significant. Therefore, choosing higher *OSR* will be an alternative to reduce the size of CT filters. However, this approach is not preferable when the size of SC filters, which is mostly determined by total capacitance, are considered. Since one of the important properties of SC filters is that the filter characteristic depends on capacitance ratios, ideally there will be no limitation on the value of smallest capacitance. However, in practical implementation, fabrication precision and noise requirement of the filters will determine the smallest capacitance, which also called unit capacitance. As a result, the total capacitance of SC filters will be proportional to *OSR* and there will be a trade-off between the size of CT filters and SC filter as the function of over sampling ratio. In order to reduce the total capacitance, some papers have proposed techniques to reduce capacitance spread [17], [19], [20], however, for some scaling factors, the conventional techniques require larger capacitor area [17].

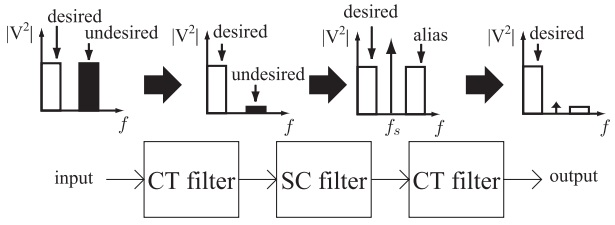

Fig. 1 Practical implementation of SC filters.

This paper proposes a technique to minimize the capacitance spread as well as total capacitance in switched-capacitor filters. Section 2 will give a brief explanation on the conventional capacitance spread reduction techniques [17], [20]. The principle of the proposed technique will be explained in Sect. 3, followed by an example of integrator implementation with analysis on minimum total capacitance and effect of parasitic capacitances. Finally, the validity of the proposed technique is confirmed using simulation results in Sect. 4.

2. Conventional Capacitance Reduction Methods

Figure 2 shows a variant of a Fleischer-Laker low-pass SC filter. This circuit uses a non-overlaping two-phase clock where the symbols 1 and 2 represent switches that turned on at phase-1 and phase-2 of the clock respectively. This filter is a 2nd-order low-pass filter and the transfer function is given by

$$H(z) = \frac{DI + (AG - 2DI)z^{-1} + DIz^{-2}}{BD + (AC + AE - 2BD)z^{-1} + (BD - AE)z^{-2}}. \quad (2)$$

As an example, assume that a 2nd-order continuous-time filter transfer function of

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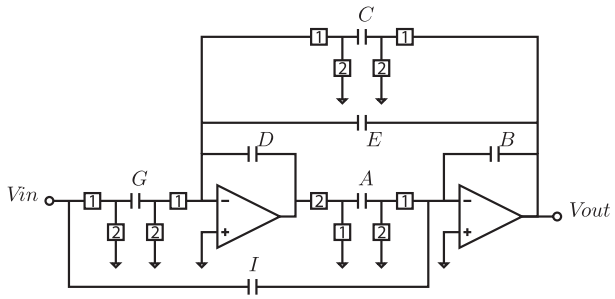

Fig. 2 Fleischer-Laker low-pass filter.

Table 1 Normalized capacitances.

Name	Value	Name	Value	Name	Value
A	1	D	1	I	$\frac{K}{\lambda}\left(\frac{2\pi}{OSR}\right)^2$
B	1	E	$\frac{4}{\lambda Q}\frac{2\pi}{OSR}$		
C	$\frac{4}{\lambda}\left(\frac{2\pi}{OSR}\right)^2$	G	$\frac{4K}{\lambda}\left(\frac{2\pi}{OSR}\right)^2$		

$$H(s) = \frac{K\omega_0^2}{s^2 + \frac{\omega_0}{Q}s + \omega_0^2} \tag{3}$$

is going to be implemented using the SC filter in Fig. 2. The transfer function of SC filter can be obtained by applying bilinear z-transformation to Eq. (3). As a result, the normalized capacitances are given in Table 1 where

$$\lambda = 4 + \frac{2}{Q}\frac{2\pi}{OSR} + \left(\frac{2\pi}{OSR}\right)^2. \tag{4}$$

Table 1 shows that the normalized values of C, E, G, and I depend on filter's gain K, quality factor Q and over sampling ratio OSR. When the quality factor is bigger than over sampling ratio (i.e. $Q > OSR$) then E will be the smallest capacitance. Otherwise, according to filter gain K, either C or I will be the smallest one. However since the case of $Q > OSR$ is rare in practical implementation, it will not be discussed in this paper. Here cut-set scaling technique might be used to reduce the total capacitance. Assume that A is scaled down to $A/\alpha(\alpha > 1)$, then D should be also scaled down to D/α to keep the transfer function unchanged. As a result, the total capacitance normalized by unit capacitance will be given by

$$C_T = \begin{cases} \dfrac{C_{T0}}{\alpha KQ} & \text{if } K \le 4 \\ \dfrac{C_{T0}}{4\alpha Q} & \text{if } K > 4 \end{cases} \tag{5}$$

where

$$C_{T0} = 4(2+\alpha)Q\left(\frac{OSR}{2\pi}\right)^2 + (4+6\alpha)\frac{OSR}{2\pi} + 5\alpha KQ + (2+5\alpha)Q. \tag{6}$$

Assumes that the over sampling ratio (OSR) is sufficiently large, i.e. in the order of hundreds or more and $OSR \gg K, Q$, then

$$C_{T0} \approx 4(2+\alpha)Q\left(\frac{OSR}{2\pi}\right)^2. \tag{7}$$

Furthermore, since the scaled capacitances A and D should not be smaller than the smallest capacitance, then the total capacitance will be approximately given by

$$C_T \approx \begin{cases} \dfrac{4}{K}\left(\dfrac{OSR}{2\pi}\right)^2 & \text{if } K \le 4 \\ \left(\dfrac{OSR}{2\pi}\right)^2 & \text{if } K > 4 \end{cases} \tag{8}$$

Equation (8) shows that when $K \le 4$, the total capacitance will be reduced with the increasing of filter gain because the smallest capacitance I increases with the gain. However, it will reach the minimum value at $K = 4$ because at that point C will replace I as the minimum capacitance. Further filter's gain increment will not change the value of total capacitance since capacitance C does not depend on filter gain K and the increment of I and G is negligible.

This means for high over sampling ratios, the total capacitance of a Fleischer-Laker low-pass filter shown in Fig. 2 is proportional to OSR^2 and its minimum value is given by $(OSR/2\pi)^2$ at $K \ge 4$. Next, define the capacitance spread β as

$$\beta = \frac{\text{largest capacitance}}{\text{smallest capacitance}}. \tag{9}$$

Since B is the largest capacitance while C or I are the smallest ones, the capacitance spread of the circuit in Fig. 2 will be approximately given by

$$\beta \approx \begin{cases} \dfrac{4}{K}\left(\dfrac{OSR}{2\pi}\right)^2 & \text{if } K \le 4 \\ \left(\dfrac{OSR}{2\pi}\right)^2 & \text{if } K > 4 \end{cases} \tag{10}$$

and it is clear that the capacitance spread also proportional to the square of over sampling ratio.

In order to furthermore reduce the total capacitance, a capacitance spread reduction technique using a unique integrator topology has been proposed [20]. The circuit is shown in Fig. 3 and the transfer function of the filter is given by

$$H(z) = \frac{\frac{A_1 G_1}{4} z^{-1}(1+z^{-1})^2}{BD + (A_1 C + A_1 E - 2DB)z^{-1} + (BD - A_1 E)z^{-2}}. \tag{11}$$

Assume that $A_1 = A$ and $G_1 = G$ such that the denominator

of Eq. (11) is exactly the same to the denominator of Eq. (2). The differences appear on the numerator of the transfer function in Eq. (11). The coefficients of the numerator are now determined by $AG/4$ and an additional delay (z^{-1}) is added. This additional delay, however, will not affect the gain characteristic of the filter and only add a constant delay of one clock period.

Since I is removed from the configuration, now C or G (if $K < 1$) will be the smallest capacitance. Assume that A_1 is scaled down from A to $A/\alpha(\alpha > 1)$ such that the transfer function in Eq. (11) becomes

$$H(z) = \frac{\frac{AG}{4\alpha} z^{-1}(1+z^{-1})^2}{BD + (\frac{AC}{\alpha} + \frac{AE}{\alpha} - 2DB)z^{-1} + (BD - \frac{AE}{\alpha})z^{-2}}. \quad (12)$$

Here, if either the product of BD or capacitances C, E, and G are scaled down by the same factor α, then the transfer function will be unchanged. Here, let B and D are scaled down by $\sqrt{\alpha}$, then the total capacitance will be given by

$$C_T = \begin{cases} \dfrac{C_{T0}}{2\alpha KQ} & \text{if } K < 1 \\ \dfrac{C_{T0}}{2\alpha Q} & \text{if } K \geq 1 \end{cases} \quad (13)$$

where

$$C_{T0} = 4(1+\sqrt{\alpha})Q\left(\frac{OSR}{2\pi}\right)^2 + 2(\alpha + \sqrt{\alpha} + 1)\frac{OSR}{2\pi} + 2\alpha KQ + (2\alpha + \sqrt{\alpha} + 1)Q. \quad (14)$$

Since the over sampling ratio is assumed to be relatively high and A should not be smaller than C or G, then the total capacitance will be approximately

$$C_T \approx \begin{cases} \left(\dfrac{2}{\sqrt{K}} + \dfrac{1}{KQ}\right)\left(\dfrac{OSR}{2\pi}\right) & \text{if } K < 1 \\ \left(2 + \dfrac{1}{Q}\right)\left(\dfrac{OSR}{2\pi}\right) & \text{if } K \geq 1 \end{cases} \quad (15)$$

This result shows that the total capacitance of circuit in Fig. 3 are proportional to OSR.

3. Capacitance Spread Reduction Technique Using Charge Distribution and Partial Charge Transfer

This section will explain a technique of capacitance reduction which is based on two simple steps to furthermore reduce the total capacitance of SC filters. Implementation example on an existing integrator topology as well as analysis on total capacitance and effect of parasitic capacitances will be given to clarify the properties of the proposed technique.

3.1 Basic Principle

The proposed capacitance spread reduction technique is based on two basic steps. The first step is a charge distribution and the second one is a partial charge transfer. This technique takes an advantage on the fact that signals in SC filters are transferred as electric charges. Considering series connected capacitances C_1 and C_2 in Fig. 4, the electric charges stored in both capacitors will be given by

$$Q_1 = Q_2 = \frac{C_1 C_2}{C_1 + C_2} V_{in}. \quad (16)$$

Note that the electric charges stored in both capacitors are always equal regardless of the capacitances. If C_2 is made of shunt connected two capacitors C_{2a} and C_{2b} (Fig. 5), then the electric charge in C_{2b} is

$$Q_{2b} = \frac{C_{2b}}{C_{2a} + C_{2b}} Q_2 = \frac{C_{2b}}{C_2}\frac{C_1 C_2}{C_1 + C_2} V_{in} = \frac{C_1 C_{2b}}{C_1 + C_2} V_{in} = \frac{C_1 C_{2b}}{C_1 + C_{2a} + C_{2b}} V_{in}. \quad (17)$$

Equation (17) reveals that if only Q_{2b} is transferred, the equivalent capacitance C_{eq} is given by

$$C_{eq} = \frac{Q_{2b}}{V_{in}} = \frac{C_1 C_{2b}}{C_1 + C_{2a} + C_{2b}} \quad (18)$$

which in fact is a capacitance scaling effect similar to the T-cell integrator in [17]. The difference is, this technique requires a delay to complete the two steps explained above.

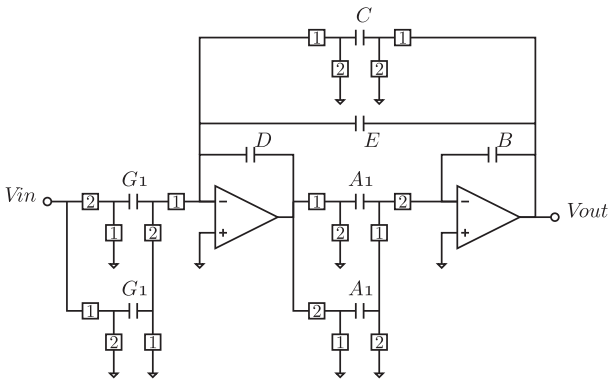

Fig. 3 2nd-order low-pass filter with reduced capacitance spread.

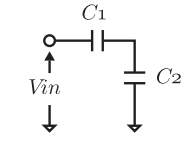

Fig. 4 Charge distribution.

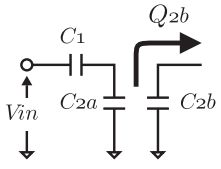

Fig. 5 Partial charge transfer.

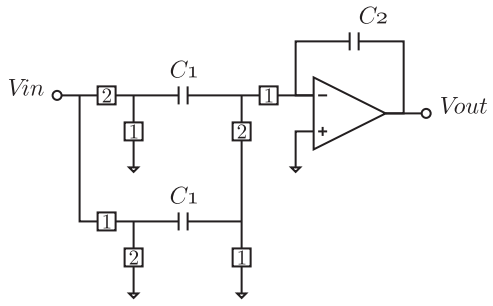

Fig. 6 Basic integrator topology.

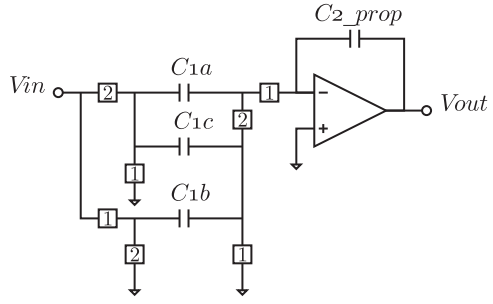

Fig. 7 Integrator with the proposed capacitance spread reduction technique.

3.2 Implementation Example

As is described in the previous sub-section, the proposed technique is applicable to any SC integrator topology as long as signal delay is allowed. For example, the integrator cell shown in Fig. 6 has an output voltage of

$$V_{out} = \frac{C_1(z^{-1}V_{in}^{(1)} + z^{-1/2}V_{in}^{(2)})}{2C_2(1-z^{-1})} \tag{19}$$

where $V_{in}^{(1)}$ and $V_{in}^{(2)}$ are the input voltages at phase-1 and phase-2 respectively. Here both input capacitances are set to a same calue C_1 since it will give the smallest total capacitance. When the input voltage at phase-2 is held such that $V_{in}^{(1)} = z^{-1/2}V_{in}^{(2)}$, then the transfer function can be rewritten into

$$H_1(z) = \frac{V_{out}}{V_{in}^{(2)}} = \frac{C_1 z^{-1/2}(z^{-1}+1)}{2C_2(1-z^{-1})}. \tag{20}$$

Since there is a delay in the transfer function, the proposed technique can be applied to this integrator topology. Integrator topology with the proposed technique is shown in Fig. 7. The transfer function of the proposed integrator is given as

$$H_2(z) = \frac{C_{1a}C_{1b}}{C_{1a}+C_{1b}+C_{1c}} \frac{z^{-1/2}(z^{-1}+1)}{C_{2\_prop}(1-z^{-1})}. \tag{21}$$

Comparing Eqs. (20) and (21), both transfer functions will be equal when the capacitances satisfy

$$\frac{C_{1a}C_{1b}}{C_{1a}+C_{1b}+C_{1c}} \frac{1}{C_{2\_prop}} = \frac{C_1}{2C_2}. \tag{22}$$

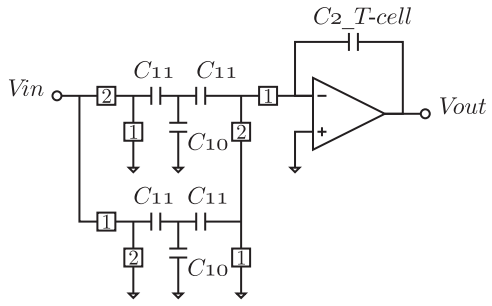

Fig. 8 Integrator with T-cell topology.

Since C_{1a} determines the amount of electrical charge transfered to C_{2_prop}, it should be set to the smallest capacitance (unit capacitance) to make the transfered charge minimum. Solving Eq. (22) for C_{2_prop} gives

$$C_{2\_prop} = \frac{2C_{1b}}{C_1 + C_{1b} + C_{1c}} C_2 \tag{23}$$

where C_1 is assumed as the smallest capacitance. As a result, the total capacitance of the proposed integrator in term of the number of unit capacitance (C_1) will be given by

$$C_{TP} = 1 + \alpha_1 + \alpha_2 + \frac{2\alpha_1\beta}{1+\alpha_1+\alpha_2} \tag{24}$$

where $\alpha_1 = C_{1b}/C_1, \alpha_2 = C_{1c}/C_1$, and $\beta = C_2/C_1$. Equation (24) has a minimum value when $1+\alpha_1+\alpha_2 = \sqrt{2\alpha_1\beta}$, which results in $C_{T\_min} = 2\sqrt{2\alpha_1\beta}$. Since β is the original capacitance spread, the smallest total capacitance is obtained when $\alpha_1 = 1$, which means $C_{1b} = C_{1a} = C_1$ and therefore

$$C_{TP} = 2\sqrt{2\beta}. \tag{25}$$

Furthermore, C_{1c} and C_{2_prop} will be given by

$$C_{1c} = C_1(\sqrt{2\beta} - 2) \tag{26}$$

$$C_{2\_prop} = C_1\sqrt{2\beta}. \tag{27}$$

Since the total capacitance of integrator in Fig. 6 is given by $(2+\beta)C_1$, Eq. (25) shows that the proposed integrator will have smaller total capacitance when $\beta > 2$. However, since C_{1c} should not be smaller than C_1, regarding Eq. (26), the minimum β will be 4.5. As a result the minimum total capacitance of the proposed circuit is $6C_1$.

On the other hand, for a comparison, consider an integrator with T-cell topology as shown in Fig. 8. The transfer functions of the T-cell integrators is given by

$$H_3(z) = \frac{C_{11}^2}{2C_{11}+C_{10}} \frac{z^{-1/2}(z^{-1}+1)}{2C_{2\_T-cell}(1-z^{-1})}. \tag{28}$$

In order to obtain the same transfer function as Eq. (20), the capacitances of T-cell integrator should satisfy

$$\frac{C_{11}^2}{C_{10}+2C_{11}} = C_1 \tag{29}$$

$$V_{out} = \frac{z^{-1/2}(C_{1a}C_{1b} + C_{1a}C_{1bp} + C_{1a}C_{1cp} - C_{1c}C_{1ap})V_{in}^{(2)} + z^{-1}C_{1b}(C_{1a} + C_{1ap})V_{in}^{(1)}}{(C_{1a} + C_{1ap} + C_{1b} + C_{1bp} + C_{1c} + C_{1cp})C_{2\_prop}(1 - z^{-1})} \tag{35}$$

$$\begin{aligned} V_{out} &= \frac{z^{-1/2}(C_{1a}C_{1b} + C_{1a}\delta C_{1b} + C_{1a}\delta C_{1c} - C_{1c}\delta C_{1a})V_{in}^{(2)} + z^{-1}C_{1a}C_{1b}(1+\delta)V_{in}^{(1)}}{(C_{1a} + C_{1b} + C_{1c})(1+\delta)C_{2\_prop}(1 - z^{-1})} \\ &= \frac{z^{-1/2}C_{1a}C_{1b}(1+\delta)V_{in}^{(2)} + z^{-1}C_{1a}C_{1b}(1+\delta)V_{in}^{(1)}}{(C_{1a} + C_{1b} + C_{1c})(1+\delta)C_{2\_prop}(1 - z^{-1})} = \frac{C_{1a}C_{1b}(z^{-1/2}V_{in}^{(2)} + z^{-1}V_{in}^{(1)})}{(C_{1a} + C_{1b} + C_{1c})C_{2\_prop}(1 - z^{-1})} \end{aligned} \tag{37}$$

Table 2 Comparison summary.

Topology	Total capacitances	Capacitance spread	Scaling range
original	$2+\beta$	β	—
T-cell	$2\sqrt{2\beta}$	$\sqrt{\beta}$	$\beta \geq 9$
proposed	$2\sqrt{2\beta}$	$\sqrt{2\beta}$	$\beta \geq 4.5$

and therefore

$$C_{11} = C_1\left(1 + \sqrt{1 + \frac{C_{10}}{C_1}}\right). \tag{30}$$

With an assumption that $C_{11} = C_1$ and $C_{10} > 0$, the transfer function will be unchanged when

$$C_{2\_T-cell} = \frac{C_1}{2C_1 + C_{10}}C_2. \tag{31}$$

As a result, the total capacitance of T-cell integrator (normalized by C_1) will be given by

$$\begin{aligned} C_{TTn} &= 4 + \frac{2C_{10}}{C_1} + \frac{C_1}{2C_1 + C_{10}}\frac{C_2}{C_1} \\ &= 4 + 2\gamma + \frac{1}{2+\gamma}\beta, \end{aligned} \tag{32}$$

where $\gamma = C_{10}/C_1$. Equation (32) has a minimum value at

$$\gamma = \sqrt{\beta} - 2, \tag{33}$$

which is given by

$$C_{TTn} = 2\sqrt{2\beta}. \tag{34}$$

It is exactly equal to the total capacitance of the proposed integrator given in Eq. (25). However, since C_{10} should not be smaller than C_1, γ should be greater or equal to 1 to keep C_1 as the smallest capacitance. As a result, according to Eq. (33), $\beta = 9$ will be the minimum original capacitance spread for T-cell integrator to obtain less total capacitances than the original integrator. The relation between normalized total capacitance, capacitance spread and scaling range is summarized in Table 2.

3.3 Effect of Parasitic Capacitances

One of the commonly known problems in switched-capacitor filters is the effect of parasitic capacitances. Consider the proposed integrator with parasitic capacitances in Fig. 9. Here C_{1ap}, C_{1bp}, and C_{1cp} are the parasitic capacitances of C_{1a}, C_{1b}, and C_{1c} respectively. Only these three parasitic capacitances need to be considered since other parasitic capacitances do not have any effect on integrator transfer function. The output voltage of the proposed integrator V_{out} will be given by Eq. (35). Since all capacitors are made of unit capacitor connected in parallel, then it is assume that the relation between capacitance and parasitic capacitance of a capacitor satisfies

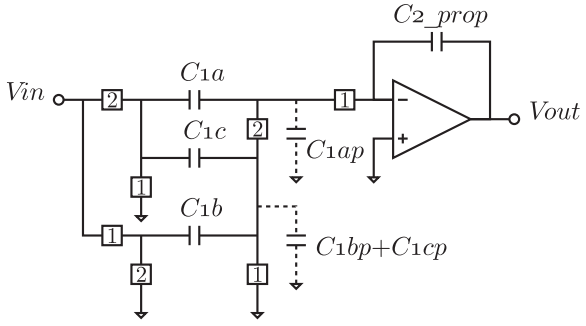

Fig. 9 Proposed integrator with parasitic capacitances.

$$\frac{C_{1ap}}{C_{1a}} = \frac{C_{1bp}}{C_{1b}} = \frac{C_{1cp}}{C_{1c}} = \delta \tag{36}$$

where δ is the ratio of parasitic capacitance to the capacitance of unit capacitor. As a result, substituting Eq. (36) into Eq. (35) will give Eq. (37). Equation (37) shows that the proposed integrator is not affected by parasitic capacitances while the T-cell integrator is sensitive to parasitic capacitances.

4. Design Example and Simulation Results

In this section, a design example to obtain a minimum total capacitance is demonstrated. Referring Table 1 and considering the 2nd-order LPF in Fig. 3, C will be the smallest capacitance as long as $K \geq 1$ holds. Assume that A are scaled down to A/α, B and D are scaled down to $B/\sqrt{\alpha}$ and $D/\sqrt{\alpha}$ such that the transfer function is unchanged. Here, the ratio of A and B will become $\beta_{AB} = B/A = \sqrt{\alpha}$. When $\sqrt{\alpha} > 4.5$, then the proposed technique can be applied to the second integrator. Since the ratio of C and G determines the gain of

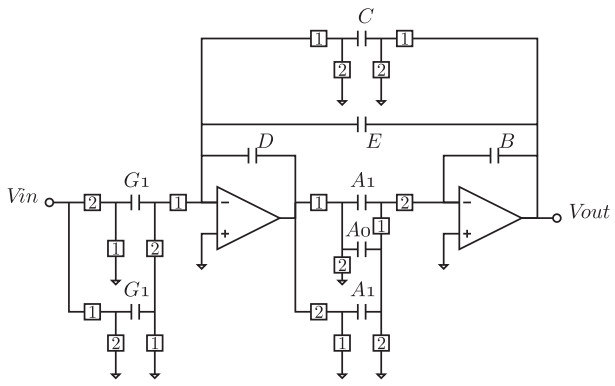

Fig. 10 2nd-order SC LPF with the proposed technique.

Table 3 Capacitance scaling.

Capacitance		Scaled Value
A1	→	$\frac{A}{\alpha}$
A0	→	$(\sqrt{2\beta_{AB}}-2)\frac{A}{\alpha}$
B	→	$\sqrt{\frac{2}{\beta_{AB}}}\frac{B}{\sqrt{\alpha}}$
C	→	C
D	→	$\frac{D}{\sqrt{\alpha}}$
E	→	E
G	→	G

the filter, they have to be scaled by a same factor to keep the ratio constant. For this reason, the first integrator will be left unchanged. The proposed circuit is shown in Fig. 10.

The transfer function of the filter can be found as

$$H(z)=\frac{\frac{A'G}{2}(1+z^{-1})^2}{BD+2(A'C+A'E-BD)z^{-1}+(BD-2A'E)z^{-2}},$$

where $A_1 = A/\alpha$ and

$$A' = \frac{A_1^2}{2A_1 + A_0}. \tag{38}$$

Assume that the proposed technique is applied such that B is scaled down to $B' = \beta'_{AB}B$. According to analysis results in Sect. 3.2, total capacitance of the integrators will be minimum when

$$\beta'_{AB} = \sqrt{\frac{2}{\beta_{AB}}} = \sqrt{\frac{2}{\sqrt{\alpha}}}. \tag{39}$$

The scaling of capacitances is summarized in Table 3. The total capacitance will be given by

$$C_{Tn}=\begin{cases}\dfrac{C_{T0}}{4\alpha KQ} & \text{if } K<1\\[2ex] \dfrac{C_{TO}}{4\alpha Q} & \text{if } K\geq 1\end{cases} \tag{40}$$

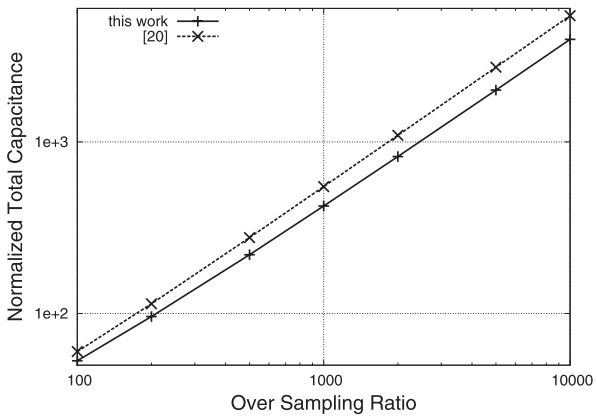

Fig. 11 Normalized total capacitance.

where

$$C_{T0} = 4\beta Q\left(\frac{OSR}{2\pi}\right)^2 + (2\beta + 4\alpha)\left(\frac{OSR}{2\pi}\right) + (4\alpha + \beta)Q + 4\alpha KQ \tag{41}$$

$$\beta = 2\sqrt{2\sqrt{\alpha}} + \sqrt{\alpha}. \tag{42}$$

With an assumption that $OSR \gg 1$ and A should not be smaller than C or G, the minimum total capacitance will be approximately given by

$$C_{Tn}\approx\begin{cases}\left(\dfrac{1}{\sqrt{K}}+\dfrac{1}{KQ}\right)\left(\dfrac{OSR}{2\pi}\right) & \text{if } K<1\\[2ex] \left(1+\dfrac{1}{Q}\right)\left(\dfrac{OSR}{2\pi}\right) & \text{if } K\geq 1\end{cases} \tag{43}$$

Comparing Eqs. (15) and (43), for a relatively large OSR, the proposed circuit will have a smaller total capacitance than the circuit of Fig. 3.

The comparison of total capacitance between original SC filter with reduced capacitance spread [20] and the proposed circuit is shown in Fig. 11. Here the proposed circuit has the smallest total capacitance compared to the other two topologies. This figure also shows that the total capacitance of the original SC filter is proportional to OSR^2 while the total capacacitance of SC filter in [20] is proportional to OSR as has been predicted in Eqs. (5) and (8). It should be noticed that the the proposed filter and filter of Fig. 3 are scaled with the same factor to make the comparison more reasonable.

Finally, the performance of the proposed filter will be demonstrated using simulation with filter parameters of $K = 1, Q = 1/\sqrt{2}, f_s = 1\,\text{MHz}, f_0(\omega_0/2\pi) = 1\,\text{kHz}, OSR = 1000$. The normalized capacitances of original Fleischer-Laker SC filter, SC filter with reduced capacitance spread [20] and SC filter utilizing proposed method are shown in Table 4. The values are rounded to the nearest integer. Here the SC filter implemented using the proposed technique has the smallest total capacitance. The total capacitance is approximately 0.4% of the total capacitance of original Fleischer-Laker SC filter and 77% of the SC filter using capacitance spread reduction technique introduced

Table 4 Normalized capacitances.

Capacitance	Normalized value		
	original	[20]	this work
A	1	1	—
A_1	—	—	1
A_0	—	—	16
B	101770	160	18
C	4	1	1
D	1	160	160
E	900	225	225
G	4	1	1
I	1	—	—
Total	102681	550	424

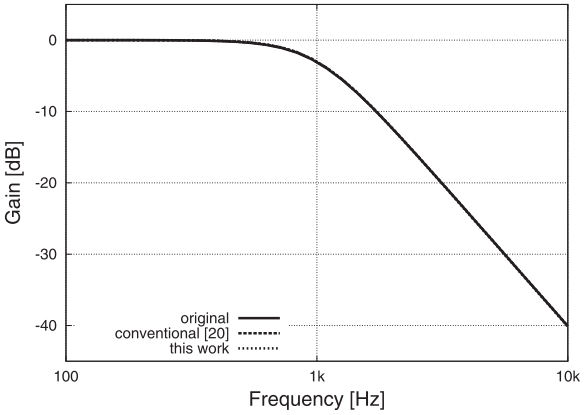

Fig. 12 Frequency characteristic.

in [20]. However, it should be remarked that this example only emphasizes the total capacitance of the filter. In more practical design, characteristics such as dynamic range and noise should be considered since capacitances scaling will affect these performances. Finally, the simulated frequency characteristics of the original Fleischer-Laker SC filter, SC filter with reduced capacitance spread [20] and the SC filter implemented with the proposed technique are shown in Fig. 12. The circuits are simulated using periodical steady state (PSS) analysis of Spectre. Switches are modeled by voltage controlled resistors and operational amplifiers are modeled using voltage controlled voltage sources where the gain of each amplifier is 100 dB. Under the given simulation conditions, even if the total capacitance is greatly reduced, the gain characteristic of the proposed SC filter is equal to the other implementations.

5. Conclusions

A capacitance spread reduction technique based on charge distribution and partial charge transfer is proposed. The proposed technique is applied to the existing integrator topology to demonstrate its effectiveness in reducing total capacitance. Analysis results show that the implemented integrator is also insensitive to parasitic capacitances.

A design technique to obtain a minimum total capacitance on a 2nd-order SC LPF is also given. A design example with OSR=1000 shows that the proposed technique can reduce the total capacitances of the filter by 23% of the one with conventional capacitance spread reduction technique (Fig. 3). However, the demonstrated design technique only consider the total capacitance of the filter. Since the other aspect of filter characteristics should be considered for practical implementation, a design optimization method with consideration on those characteristics is under investigation.

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