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Nano-Grating Channel MOSFETs for Improved Current Drivability

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Drivability-improved MOSFETs were successfully fabricated using nano-grating silicon wafers. Effective channel widths were universally increased with the wafers. This required almost no additional process change for device fabrication when the grating height was less than or comparable to the conventional macroscopic wafer surface roughness. The fabricated MOSFET with the grating height of 25nm showed 22% improvement in current drivability compared to the conventional structure.

Introduction

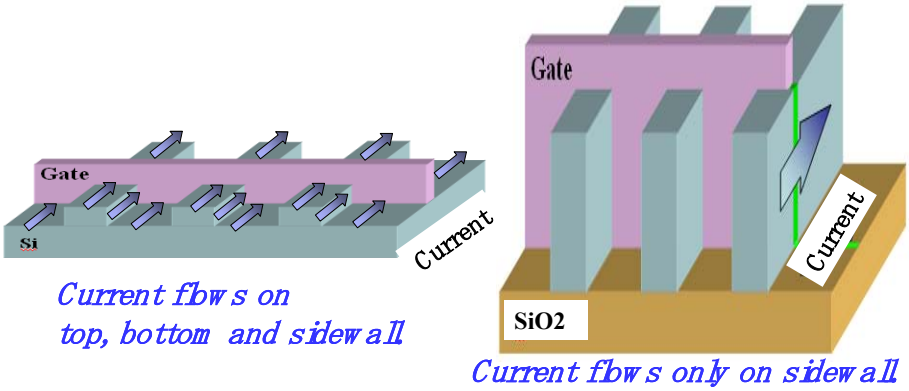
Electronics systems require higher and higher performances for CMOS-LSIs which are achieved with high drivability of scaled CMOS transistors. Continuous scaling of CMOS transistors, however, soon will meet their physical limits as well as the economical limits. The non-scaled approaches such as 3D-structures[1][2] and strained-channels of CMOS transistors [3] are widely studied. This paper reports a new approach for improving drivability of MOS transistors without almost any changing fundamental fabrication process steps. Special feature is that we need not to employ complicated 3D processes such as Fin-FETs for drivability improvement. It is much advantageous compared to 3D or strain devices. Nano-gratings, or nanometer level trenches, are periodically formed on bare silicon wafers. It has become possible that MOSFETs are fabricated on the nano-grating wafers with the conventional processes because the nano-gratings are shallow enough compared to the macroscopic roughness of conventional wafer surfaces (thickness variation). Wafers can be universally used if transistor channels are aligned to direction of gratings.

Feature of Nano-Grating Channel MOSFETs

The multi-channels are consisted of nano-gratings formed with nanometer-level line & space trenches. Trenches are periodically–formed over an original wafer and are shallow enough compared to site flatness of a wafer. The universal nano-grating wafers are applicable to various kinds of LSI production if transistor channels are aligned to direction of gratings.

The drivability of a MOSFET is shown as follows: $\alpha \cdot g_m/(\alpha \cdot C_g + C_l)$, where g_m and C_g are transconductance and gate capacitance, respectively. C_l is load capacitance. Generally, $\alpha=1$, $\alpha \cdot C_g << C_l$. The purpose of this proposal is to increase α ; ($\alpha > 1$) and then to increase its drivability $(\sim \alpha \cdot g_m / C_l)$.

Figure 1 shows comparison of structures and current flows between a nano-grating channel MOSFET and a conventional multi-fin MOSFET. The conventional multi-fin type structure is 3-dimensional and requires complicated processes for fabrication such as pattering, etching, channel ion implantation et al. Current flows only on vertical sidewalls of the multi-fins. The structure has area loss on plain area. For a multi-channel MOSFET by nano-gratings, current flows along three kinds of surfaces of silicon on the top, bottom and sidewall of each grating. There is a great difference in pitch size between the nano-grating and the multi-fin. The greater area-advantage on silicon wafer is obtained. We need not any additional transistor process without grating formation for the first stage. There are several types of gratings; triangular, square, and trapezoid. We may prepare wafers as universal ones with nano-gratings for many kinds of LSI applications.



(a) (b)

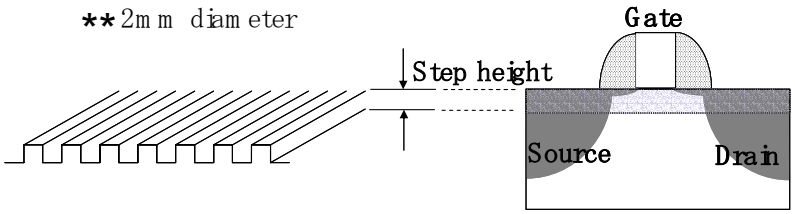
Fig. 1 Comparison of structures and current flows between a nano-grating channel MOSFET where current flows on top, bottom and sidewall(a) and a conventional multi-fin MOSFET where current flows only on sidewall(b).

Table 1 shows requirements for wafer flatness and doping cited from International Technology Roadmap for Semiconductors (2005 ITRS)[4]. The nanotopography is already less than 18nm in 2006. However, the site flatness is now 70nm and is expected 35nm in 2012 and junction depth is now 30nm and 15nm in 2012 for high performance LSIs. If the step height of nano-gratings as shown under the table is much smaller than these values, we need not to care about surface roughness or deviation which is caused by the nano-gratings for device fabrication process, especially for lithography. If the height of nano-gratings is higher than those values, the design of nano-grating channel MOSFETs may be modified to suppress short-channel effects and so on.

Table 2 ITRS requirements[4] for wafer flatnesses and source-drain doping depths of MOSTETs in each technology node. The step height defined under the table is comparable or less than each critical value.

Year	2006	2008	2010	2012
Site flatness(nm)*	<70	<57	<45	<35
Nanotopography(nm)**	<18	<14	<11	<9
Junction depth(nm)	30.8	25.3	19.8	15.4
Drain extension(nm)	9	7.5	6.5	4.5

* SFQR 26mm×8mm
** 2mm diameter



Fabrication Process of Nano-Grating MOSFETs

Figure 3 shows the process flow of a nano-Grating MOSFET. Firstly, lines & steps of photo resist patterns were formed on a conventional p-type (100) Si wafer. EB direct lithography technology was employed to experimentally realize nano-level patterns. Other lithographic technologies may be used for higher throughput. The pattern pitch on the resist was 75nm. After dry etching the Si wafer, nano-gratings with square shape were formed. Two kinds of step height of 15nm and 25nm were used. The grating density with line & space was approximately 13000 per mm of channel width. The wafer with nano-gratings was chemically cleaned and subjected to the conventional MOSFET fabrication process; trench-isolation with silicon dioxide, p-well ion implantation with boron ions of 2×10^{13} cm^{-2} and an energy of 180keV, channel ion-implantation of boron ions of 2×10^{12} cm^{-2} and an energy of 10keV, gate dielectric growth of SiON with thickness of 2nm by thermal oxidation and nitridation, and gate poly Si deposition & doping with arsenic atoms, annealing, aluminum deposition and metallization.

Figure 4(a) and (b) are SEM pictures of bird's view and cross-section after resist removal, respectively. The Si wafer was patterned with nano-gratings of step height of 25nm and pitch of 75nm. The etched surface seemed not as smooth as the top surface of the grating which was the surface of the original Si wafer. Optimization of the grating etching process may improve the flatness. The influence of the Si surface roughness will be discussed later.

Figure 5 is a picture of a multi-channel MOSFET fabricated with nano-gratings. The gate length L and width W in plain are 80nm and 1μm, respectively.

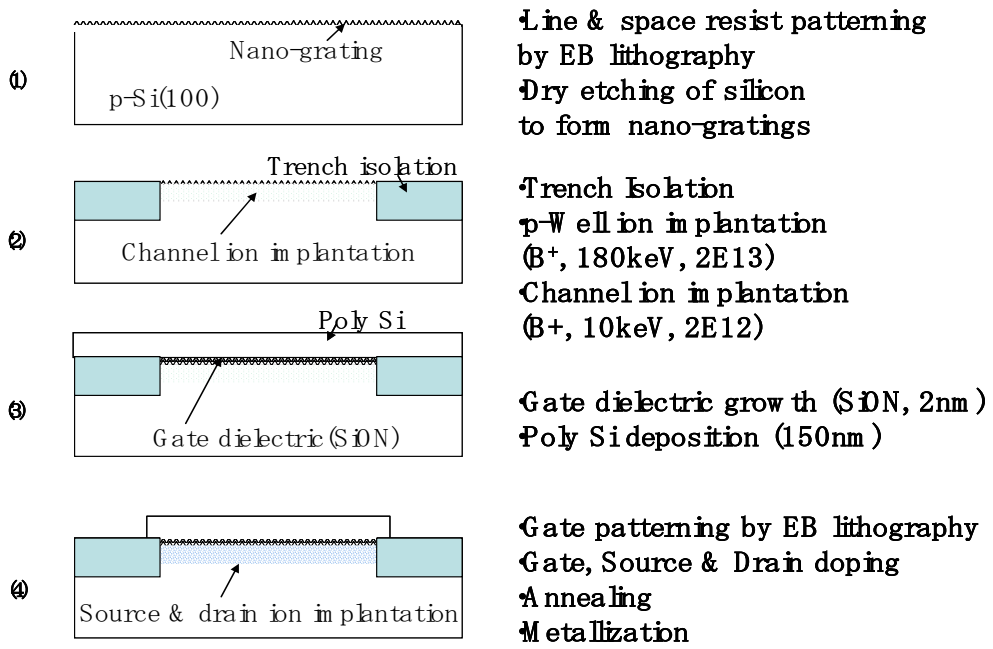


Fig. 3 Fabrication process flow of a nano-Grating n-channel MOSFET on conventional p(100) Si surface.

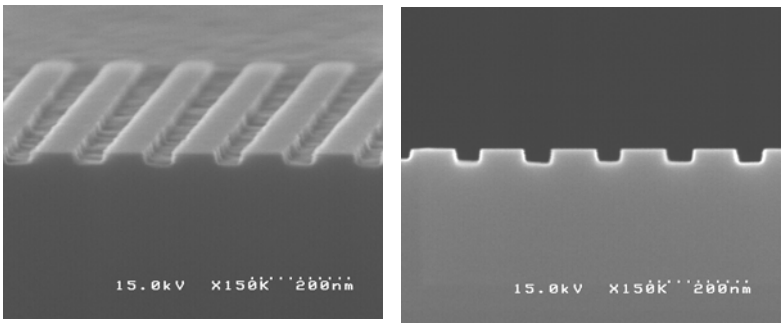


Fig. 4 SEM pictures of a bird's view (a) and a cross-section (b) after resist removal. The step height and pitch of line & space are 25nm and 75nm, respectively. The grating density was approximately 13000 /mm in channel width.

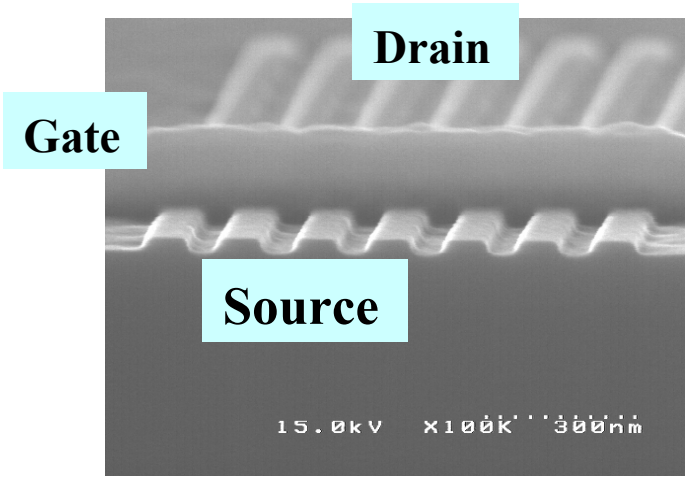


Fig. 5 SEM picture of a multi-channel MOSFET fabricated with nano-gratings. The gate poly Si length L and width W in plain are 80nm and 1μm, respectively. The step height and pitch of line space were 25nm and 75nm, respectively.

Characteristics of Nano-Grating MOSFETs

Figure 6 is a relation between drain current I_{on} and grating step height of the fabricated nano-grating MOSFETs. The characteristics are compared with calculation of I_{on} by using grating heights and pitches. The experimental I_{on} increases with the grating step height. For the grating step height of 25 nm, the drivability enhancement was about 22 %. We observe the experimental values which are a little lower than the calculated ones for all cases. This may be due to decrease in carrier mobility caused by the previously-mentioned surface roughness by Si dry etching. This will be improved by Si etching process optimization in future.

The increase in off-current I_{off} is one of concerns of MOSFETs fabricated on nano-grating wafers because current crowding may occur due to increase in localized electric field. . Electric field may increase at the grating corners of top and bottom along channels. Figure 7 shows sub-threshold current of fabricated MOSFETs corresponding to those in Fig.6. Although the very short gate length of 80 nm was examined, we measured no degradation in off-current I_{off} compared to the reference, slight decrease in I_{off} was observed due to process deviation.

Figure 8 shows dependence of sub-threshold slope S on the grating step height. The S values were almost constant and as small as those of the conventional MOSFETs.

These results show there was no critical problem in characteristics of MOSFETs fabricated on nano-grating silicon wafers.

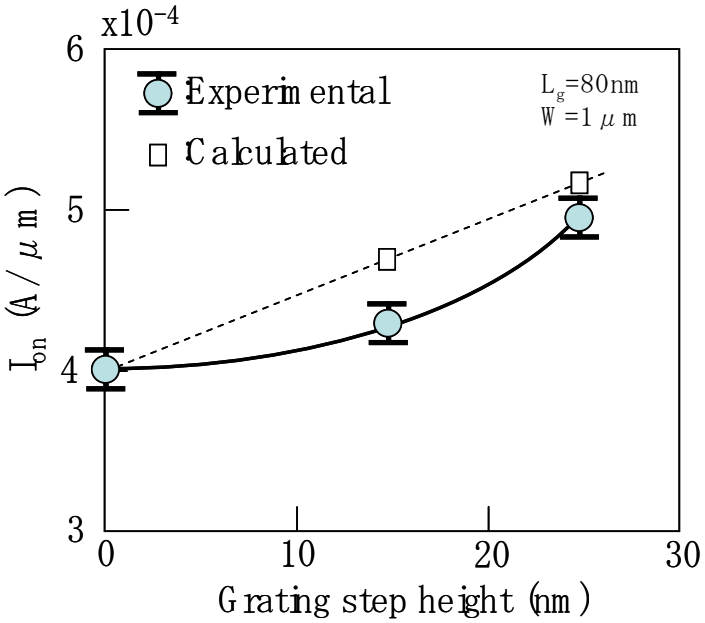


Fig. 6 Relation between drain current I_{on} and grating step height of the fabricated nano-grating MOSFETs. The characteristics are compared with calculation of I_{on} by using grating heights and pitches.

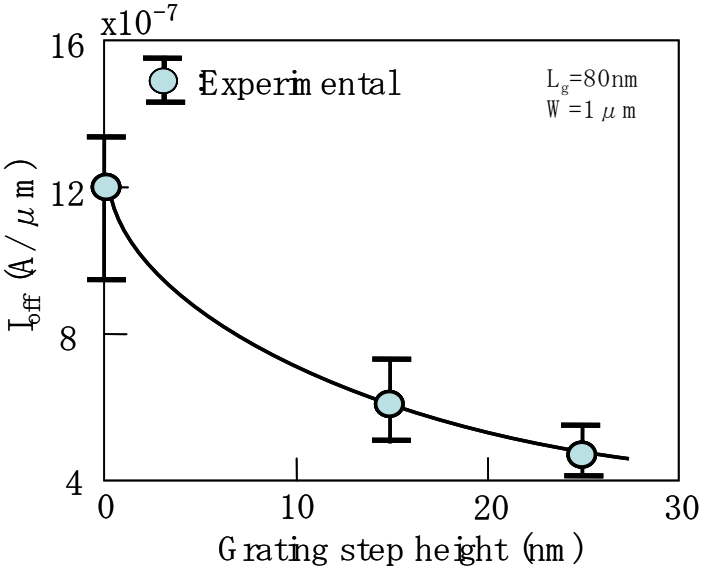


Fig. 7 Sub-threshold drain off-current of the fabricated nano-grating MOSFETs corresponding to those in Fig.6.

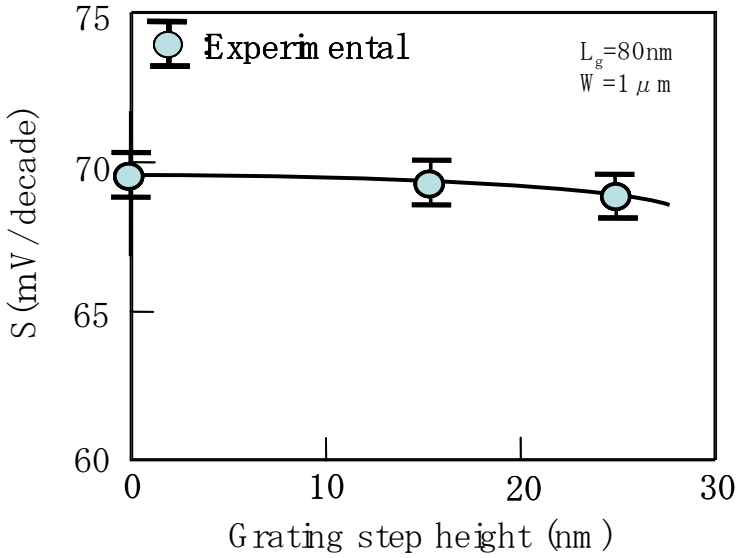


Figure 8 Dependence of sub-threshold slope S on grating step height

Conclusion

Drivability-improved n-channel MOSFETs were successfully fabricated using nano-grating silicon wafers. Effective channel widths were universally increased. Almost no additional process change was needed for device fabrication when the grating height was less than or comparable to the conventional macroscopic wafer surface roughness. The fabricated MOSFET showed 22 % improvement in drain current compare to the conventional device when the grating height was 25nm. As far as the fundamental characteristics obtained with the experimental devices, there was no critical problem of MOSFETs fabricated on nano-grating silicon wafers. The technology provides great advantages for drivability improvement without paying much tradeoff of process cost. This proposal will be useful to CMOS-LSIs with high performance in general.

Acknowledgment

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