

論文 / 著書情報
Article / Book Information

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Authors	Xiaoli ZHU, Shin-Ichiro KUROKI, Koji KOTANI, Hideharu SHIDO, Masatoshi FUKUDA, Yasuyoshi MISHIMA, Takashi ITO
出典 / Citation	IEICE Transactions on Electronics, Vol. E90-C, No. 9, pp. 1830-1836
発行日 / Pub. date	2007, 9
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PAPER

Characteristics of Nano-Grating N-Channel MOSFETs for Improved Current Drivability

Xiaoli ZHU^{†a)}, Shin-Ichiro KUROKI[†], Nonmembers, Koji KOTANI[†], Member, Hideharu SHIDO^{††}, Masatoshi FUKUDA^{††}, Yasuyoshi MISHIMA^{††}, Nonmembers, and Takashi ITO[†], Member

SUMMARY Drivability-improved MOSFETs were successfully fabricated by using nano-grating silicon wafers. There was almost no additional process change in device fabrication when the height of the gratings was less than the conventional macroscopic wafer surface roughness. The MOSFETs with the grating height of 35 nm showed 21% improvement in current drivability compared to the conventional one with the same device occupancy area. And the roll-off characteristic of threshold voltage of nano-grating device held the line of conventional one in despite of the 3-D channel structure. The technology provides great advantages for drivability improvement without paying much tradeoff of process cost. This proposal will be useful to CMOS-LSIs with high performance in general.

key words: nano-grating, transconductance, effective mobility, current-drivability

1. Introduction

Higher drivability of transistors is necessary to meet the requirements of electronic systems. Up to now, the improvements in the performance of MOSFETs were mostly achieved by scaling of gate length (L) and the gate dielectric thickness. However when scaling the device size into deep submicron regions, there are some problems caused by the short channel effects as well as increased process cost. So the non-scaled approaches such as fin-channel-structures [1]–[6] and strained-channel transistors [7], [8] are widely studied to sustain Moore's law. But these methods are so complicated that it is too costly. Multi-wall p-channel MOSFETs were reported to have 45% increase in hole mobility [9]. The improvement was mainly caused by p-channel strains. In this paper nano-grating n-channel MOSFETs are reported. The gratings, or nanometer level trenches, were periodically formed on bare silicon wafers, and then MOSFETs were fabricated on the nano-grating wafers with conventional process. The special feature is that no complicated process is needed and the process is almost compatible with the conventional one.

2. Feature of Nano-Grating Channel MOSFETs

The multi-channels consist of nano-gratings formed with

Manuscript received March 12, 2007.

Manuscript revised May 21, 2007.

[†]The authors are with Graduate School of Engineering, Tohoku University, Sendai-shi, 980-8579 Japan.

^{††}The authors are with Fujitsu Laboratories Ltd., Atsugi-shi, 243-0197 Japan.

a) E-mail: gaozxl@ecei.tohoku.ac.jp

DOI: 10.1093/ietele/e90-c.9.1830

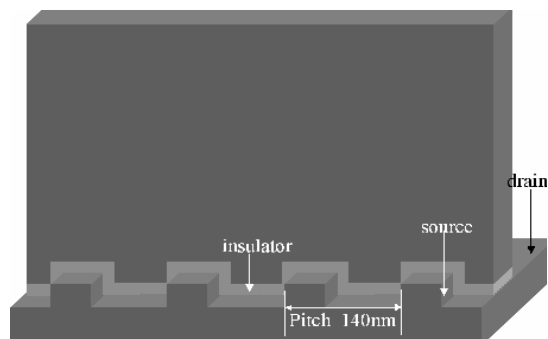


Fig. 1 Structure of a nano-grating MOSFET. The current flows along three kinds of surface of the wafer: the top, sidewalls and bottom with a larger total effective channel width.

nanometer level line and space trenches. The trenches are periodically formed over an original wafer and are shallow enough compared to the site flatness of a wafer. The universal nano-grating wafers are applicable to various kinds of LSI production if transistor channels are aligned to the directions of gratings.

The drivability of a MOSFET is shown as $\frac{\alpha \cdot g_m}{\alpha \cdot C_g + C_l}$, where g_m and C_g are transconductance and gate capacitance, respectively. C_l is the load capacitance. Generally, $\alpha = 1$, $\alpha \cdot C_g \ll C_l$. The purpose of this proposal is to increase α and then to increase the drivability.

As shown in Fig. 1, in a multi-channel MOSFET by nano-gratings, current flows along three kinds of surfaces of silicon on the top, bottom and sidewall of each grating, different from the conventional multi-fin type structure in which current flows only on vertical sidewalls of the multi-fins, is 3-dimensional and requires complicated processes for fabrication such as patterning, etching, channel ion implantation and so on. By nano-grating channel, the greater area-advantage on silicon wafer can be obtained. Any additional transistor process is unnecessary except the grating formation for the first stage. Universal wafers with nano-gratings in triangular, square, or trapezoidal can be prepared for many kinds of LSI applications.

Table 1 shows the requirements for wafer flatness and doping cited from the 2005 International Technology Roadmap for Semiconductors (2005 ITRS) [10]. The nanotopography was already less than 18 nm in 2006. However, the site flatness was close to 70 nm and is expected to be less than 35 nm in 2012. The junction depth is now about

Table 1 ITRS requirements [10] for wafer flatness and source-drain doping depths of MOSFETs in each technology node.

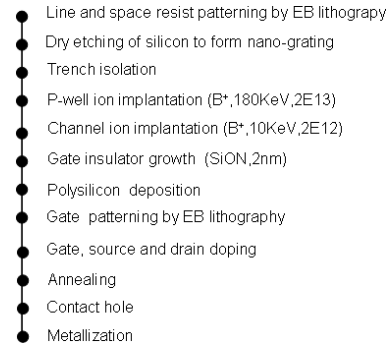
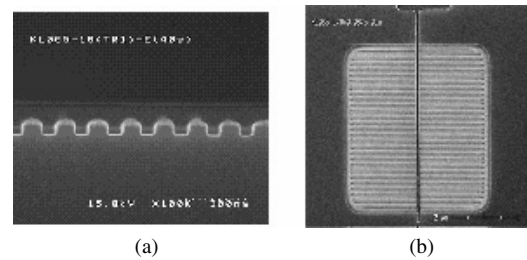
Year	2006	2008	2010	2012
Site flatness (nm)*	<70	<57	<45	<35
Nanotopography(nm)**	<18	<14	<11	<9
Junction depth(nm)	30.8	25.3	19.8	15.4
Drain extension(nm)	9	7.5	6.5	4.5

30 nm and to be 15 nm in 2012 for high performance LSIs. If the step height of nano-gratings is much smaller than these values, we need not to care about surface roughness or deviation caused by the nano-gratings during the fabrication process. On the contrary, if the height of nano-gratings is higher than those values, the design of nano-grating channel MOSFETs must be modified to suppress short-channel effect and so on.

3. Experiments

Both the nano-grating channel MOSFET and the conventional one are employed for this experiment, and the structure of a nano-grating channel MOSFET is shown in Fig. 1. The device has conducting channels on three kinds of surface: the top, bottom and sidewalls of silicon wafer with a total effective channel width larger than the conventional ones.

Key fabrication processes of nano-grating device are listed in Fig. 2. The process started with a conventional p-type (100) Si wafer. The lines and spaces were patterned using EB direct lithography technology. Dry etching was used to etch the surface of the wafer to form nano-grating steps. The pitch of lines and the step height was 140 nm and 35 nm, respectively, which is much smaller than the values required in site-flatness in ITRS [10], so it is unnecessary to care about surface roughness or deviation caused by nano-gratings. The wafer with nano-gratings was chemically cleaned and was followed by the conventional MOSFET fabrication process, the isolation is formed by shallow trenches followed with p-well ion implantation at a dose of $2 \times 10^{13} \text{ cm}^{-2}$ with an energy of 180 keV. The channel ion implantation was carried out at a dose of $2 \times 10^{12} \text{ cm}^{-2}$ with an energy of 10 keV. The gate insulator of SiON film with thickness of 2 nm was grown by thermal oxidation and nitridation. The poly Si gate electrode was deposited and followed by patterning, ion implantation and annealing. The standard contact metallization steps completed the device fabrication. Figure 3 shows the cross-section SEM image of nano-grating and the plain-view SEM image of a nano-grating MOSFET. By measuring the effective width shown in Fig. 3(a), in ideal situation, the drain current of nano-grating device is expected to be 1.5 times to that of the conventional one under the same bias conditions.

**Fig. 2** The process flow of a nano-grating n-channel MOSFET on P(100) silicon surface.**Fig. 3** The SEM pictures of nano-grating (a) and nano-grating MOSFET (b).

4. Results

4.1 Drain Current-Voltage Characteristics

Figures 4(a) and (b) shows the drain current-voltage characteristics (I_d - V_d) for nano-grating and conventional n-MOSFETs with the same occupancy channel width of $5 \mu\text{m}$ and length of $0.25 \mu\text{m}$, respectively. The drain bias is from 0 to 2 V with one step of 10 mV and the gate bias is from 0 to 1 V with a step of 0.2 V. According to the drain saturation current equation

$$I_d = \frac{1}{2} \frac{W}{L} \mu_{eff} \frac{\epsilon_i \epsilon_{ox}}{t_{ox}} (V_g - V_{th})^2,$$

the enhancement of drain current may result from the change of W , V_{th} and (or) μ_{eff} . To make sure how the channel width W has changed, the gate capacitances of both the nano-grating device and the conventional one with the same gate area are measured.

Figure 5 shows the relation between the gate-channel capacitance and the gate area of both the nano-grating device and the conventional one. As a result, the former is 1.35 times of that of the latter. The improvement percentage is smaller than the expected value of 50%, and the reason will be discussed in Sect. 5.

4.2 Drain Current-Gate Voltage Characteristics

Figure 6 shows the drain current-gate voltage (I_d - V_g) characteristics of both the nano-grating device and conventional

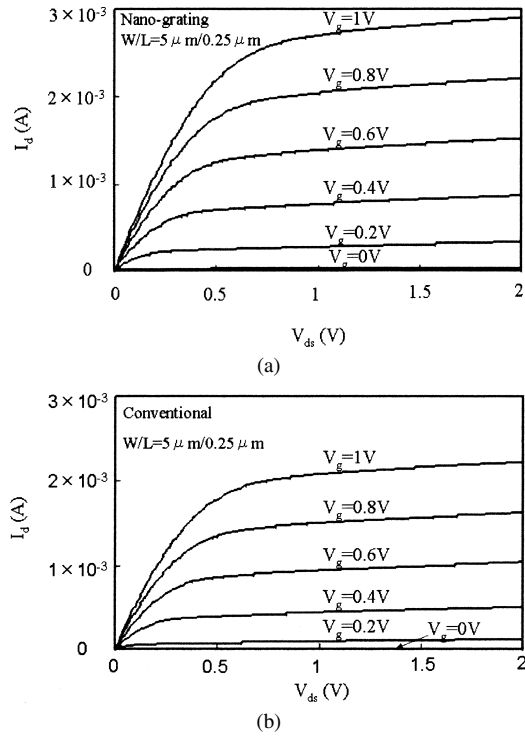


Fig. 4 Drain current-voltage characteristics of the nano-grating device (a) and the conventional one (b). The channel length L and width W in plane are $0.25 \mu\text{m}$ and $5 \mu\text{m}$, respectively.

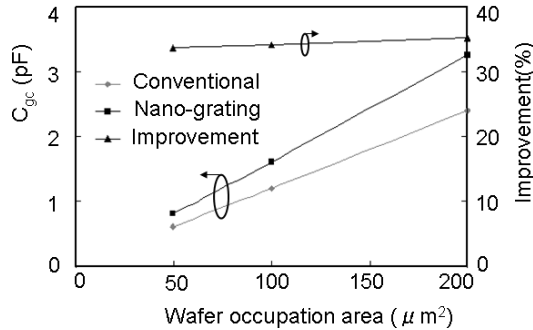


Fig. 5 Gate area dependence of gate-channel capacitance of the nano-grating device and the conventional one.

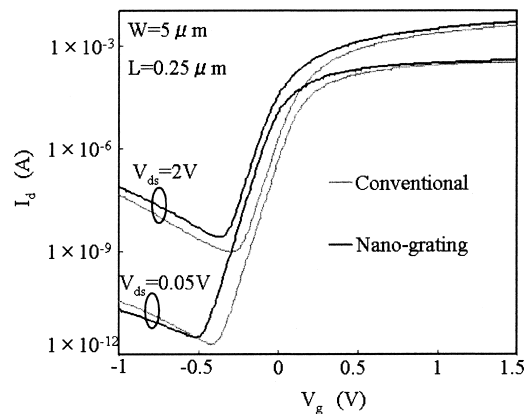


Fig. 6 The I_d - V_g characteristics of the nano-grating device and the conventional one with the same plane channel width and length of $5 \mu\text{m}$ and $0.25 \mu\text{m}$, respectively.

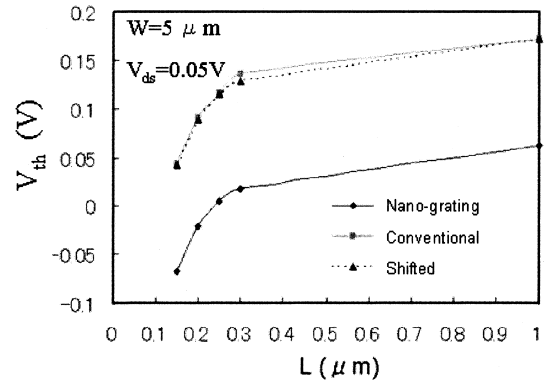


Fig. 7 The channel length L dependence of threshold voltage of the nano-grating device and the conventional one.

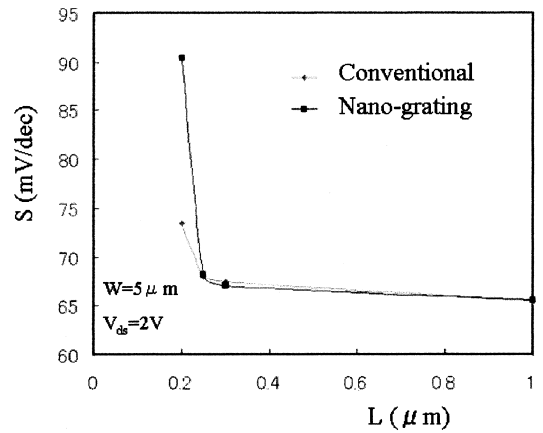


Fig. 8 The channel length L dependence of sub-threshold slope S of the nano-grating device and the conventional one.

one with the same plane channel width and length of $5 \mu\text{m}$ and $0.25 \mu\text{m}$, respectively. The threshold voltage is extracted from the linear region I_d - V_g characteristics with small V_d . Figure 7 shows the threshold voltages of the devices. Compared to the conventional plane device with the same plane device size, the threshold voltages of nano-grating device is smaller. The reason will be discussed later in Sect. 5 in detail. In Fig. 7, the threshold voltage curve of the nano-grating devices with different channel length was shifted to compare the short channel effect between the two kinds of devices. The shifted curve almost matched to the curve of the conventional device. It can be concluded that the nano-grating device has almost the same short channel effect. So it is possible to scale the nano-grating devices down in spite of the 3-D structure of the channel. Figure 8 shows the dependence of sub-threshold slope S on the channel length. The S values of nano-grating devices were almost as small as those of conventional ones until the channel length becomes smaller than $0.25 \mu\text{m}$.

4.3 Transconductance Characteristics

Figure 9 shows the transconductance G_m as the function of the plane channel width and length. The values of G_m of

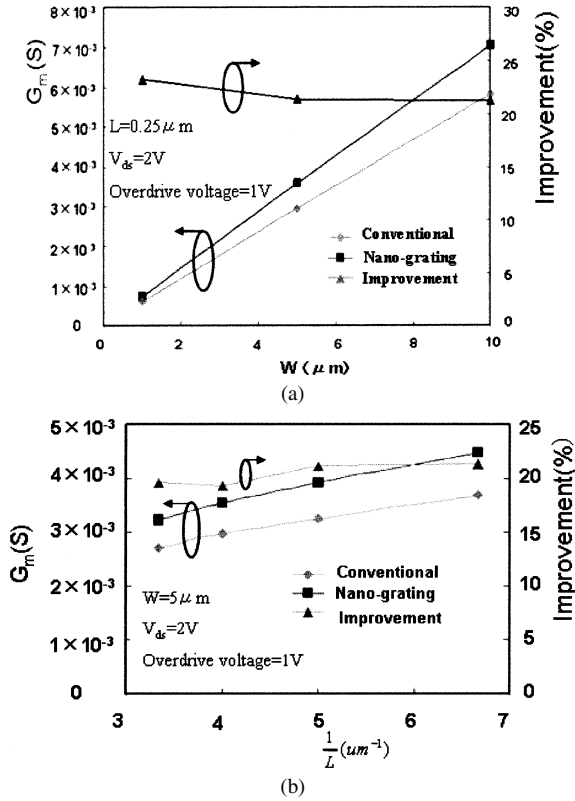


Fig. 9 The channel width and length dependence of the transconductance in the nano-grating device and the conventional one.

both the nano-grating device and the conventional one with several kinds of occupied area, measured with the same condition, were compared. And it is obvious that with the same plane area, the current drivability of nano-grating device is about 21% larger than that of the conventional one, independent of the plane channel width or the plane channel length.

4.4 Effective Channel Mobilities

The effective channel mobility in the inversion layer, μ_{eff} was determined from the drain conductance g_d in the linear region.

$$\mu_{eff} = \frac{L}{W} \frac{g_d(V_g)}{qN_S(V_g)}$$

The nano-grating device and the conventional one with the same plane size was studied. g_d was measured at the drain voltage V_d of 10 mV. The channel width W of the nano-grating device was considered as 1.35 times of that of the conventional one from the measurement of $C_{gc}(V_g)$. The surface carrier concentration $N_S(V_g)$ was determined directly through gate-channel capacitance $C_{gc}(V_g)$ measurement [11]–[13],

$$qN_S(V_g) = \int_{-\infty}^{V_g} C_{gc}(V_g) dV_g.$$

Figure 10 shows the effective mobility in both kinds

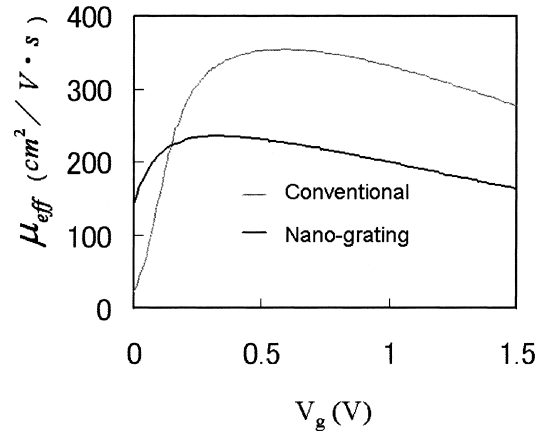


Fig. 10 Gate voltage dependence of effective mobility of the nano-grating device and the conventional one.

of devices. It can be seen clearly that in lower voltage region, the mobility in nano-grating device is larger than that in conventional one, which is considered to be induced by the lower impurity concentration in nano-grating device. In higher voltage region, mobility is smaller than that in conventional one due to the roughness surface in nano-grating device.

5. Discussion

5.1 Decrease of Nano-Grating Devices' Threshold Voltage

To make the reason why nano-grating device' threshold voltage is smaller than that of conventional one clear, the body effect of the two kinds of device with planar channel width of $10 \mu m$ and length of $10 \mu m$ was studied. The dependence of threshold voltage on back bias voltage was shown in Fig. 11. It can be obviously seen that nano-grating channel device has a smaller back-gate effect parameter γ [14] than the conventional one. From the function about $\gamma \left(\gamma = \frac{\sqrt{2\epsilon_S q N_A}}{C_{ox}} \right)$, the average doping concentrations of the substrate were calculated. As a result, the doping concentration of nano-grating wafer and conventional wafer is $4.24 \times 10^{16} cm^{-3}$, $1.57 \times 10^{17} cm^{-3}$ respectively. From the function about threshold voltage

$$V_{th} = V_{FB} + 2\phi_B + \frac{\sqrt{2\epsilon_S q N_A (2\phi_B)}}{C_{ox}}$$

with the same condition, the lower the substrate doping concentration is, the lower the threshold voltage will be, which is consistent with the result.

The process simulation was also carried out about the impurity profiles after well and channel ion implantation. Redistribution of those impurities after the activation annealing were ignored because of its short time ($1000^\circ C$, 3 s). The result is shown in Fig. 12 and it proved the supposition of less concentration of the impurities in the nano-grating

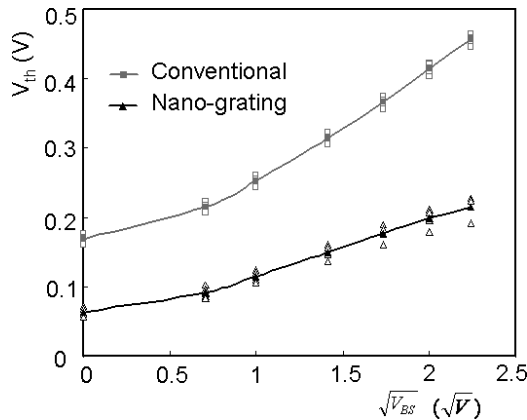
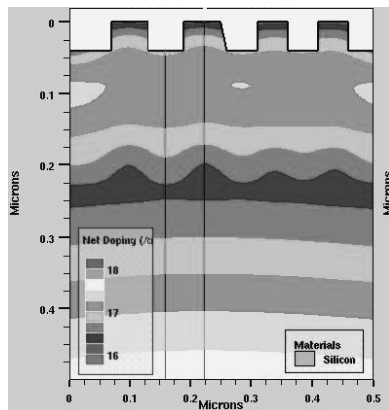
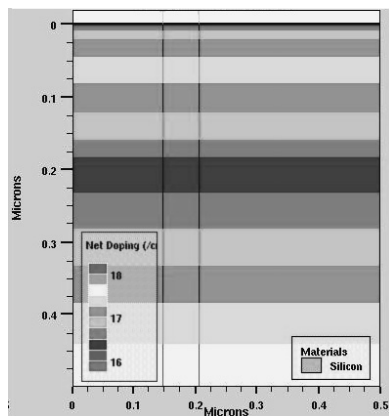


Fig. 11 The dependence on back bias voltage of the nano-grating device and the conventional one both with the planar width and length of $10\ \mu\text{m}$.



(a) Nano-grating device



(b) Conventional device

Fig. 12 The simulation result of impurity profiles. The p-well implantation was done with boron ions of $2 \times 10^{13}\ \text{cm}^{-2}$ and energy of 180 keV and the channel ion implantation with boron ions of $2 \times 10^{12}\ \text{cm}^{-2}$ and energy of 10 keV.

channel region.

The effective channel mobility was also influenced by the channel impurity profile as can be seen in Fig. 10. It is also the evidence that the channel doping concentration of nano-grating device is lower than the conventional one. In lower voltage region where it is limited by Coulomb scat-

tering, the effective mobility in nano-grating device is larger than that in the conventional one although it is smaller than that in the conventional one due to roughness scattering at the nano-grating surface. The strain effect for the n-channel MOSFET may remain as the other reason to decrease the effective mobility [15].

5.2 Improvement of Transconductance

With the formation of nano-grating shown in Fig. 3(a), it is expected the improvement of the gate-channel capacitance and the current drivability to be 50%. But the roughness of the etched sides in Fig. 3(a) may cause the nonuniform thickness of the gate dielectric which will result in the decrease of the improvement. So the improvement rate of the capacitance was 35%. Due to the deterioration of effective mobility in nano-grating device shown in Fig. 10 which may be induced by the roughness of etched silicon surface of nano-gratings, the improvement of transconductance became 21%, smaller than the improvement of gate-channel capacitance of 35%. But with the optimization of the etching process, larger improvement can be achieved in future.

6. Conclusion

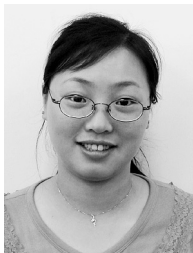
A drivability enhanced n-channel MOSFET with nano-grating channel is reported. By using nano-grating wafer, the effective channel width can be increased universally without any additional process change. The nano-grating device showed about 21% improvement in drain current compared to the conventional one with the same occupied area. With the optimization of fabrication process in the future, more improvement can be enhanced. The roll-off characteristics of threshold voltage of nano-grating device held the level of the conventional one in spite of the 3-D channel structure. The technology provides great advantages for drivability improvement without paying much tradeoff in process cost. This proposal will be useful to CMOS-LSIs with high performance in general.

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Xiaoli Zhu received the M.Eng. degree in microelectronics and solid state electronics from Hunan University, China, in 2003. She is currently pursuing the Ph.D. degree in electronic engineering from Tohoku University, Sendai, Japan. Her main research interest is the investigation of semiconductor devices with high performance and new structure.



Shin-Ichiro Kuroki was born in Miyazaki, Japan, in 1975. He received the B.S. degree in Department of Physics from Yamaguchi University, in 1997, the M.S. and Ph.D. degrees in Department of Physics from Hiroshima University, Japan, in 1999 and 2002, respectively. From 2002 to 2005, he worked for Research Center for Nanodevices and Systems of Hiroshima University as a Researcher for Industry-University-Government cooperation, where he was engaged in the process and the reliability technologies for Cu/Low-k multilevel interconnection of LSIs. In 2005, he joined the Graduate School of Engineering, Tohoku University as an Assistant Professor. His research interests are in the areas of device and process technologies in silicon integrated circuit, at present concerned with silicon thin film transistor.



Koji Kotani received the B.Eng., M.Eng. and Dr. Eng. degrees all in electronic engineering from Tohoku University, Sendai, Japan, in 1988, 1990 and 1993, respectively. He joined the Department of Electronic Engineering, Tohoku University as a research associate in 1993. From 1997 to 1998, he belonged to the VLSI Design and Education Center (VDEC) of the University of Tokyo as a visiting associate professor. He is currently an associate professor at Department of Electronic Engineering, Tohoku University. He is engaged in the research and development of low power and high performance silicon devices/circuit technologies, especially studying about high performance TFT devices for 3D integration, advanced MIS devices using novel materials, functional MOS devices and circuits (floating-gate MOS), and dynamic reconfigurable processors. Dr. Kotani is a member of the IEEE Electron Devices Society and Solid-State Circuits Society.



Hideharu Shido joined Fujitsu laboratories Ltd., Atsugi, Japan, in 1985, developing semiconductor processes for bipolar Tr. His currently workings are high-speed CMOS devices and advanced CMOS processes. Mr. Shido is a member of the Japan Society of Applied Physics.



Masatoshi Fukuda received the B.E. and M.E. degrees in electronic engineering from Hiroshima University, Hiroshima, Japan, in 1993 and 1995, respectively. In 1998, he joined Fujitsu laboratories Ltd., studying scaled DRAM and Flash Memories. His currently workings are low-power and high-speed CMOS devices. Mr. Fukuda is a member of the Japan Society of Applied Physics.



Yasuyoshi Mishima received his Ph.D. degree in 1984 from Hiroshima University, Japan. He joined Fujitsu Laboratories Ltd. in 1984, studying solar cells, imaging devices, TFT-LCDs, and OLEDs. His current research interests are advanced CMOS technologies. He has published over 70 papers in these fields. He is a member of the Japan Society of Applied Physics.



Takashi Ito received the B.S., M.S. and Ph.D. degrees in Electronics Engineering from Tokyo Institute of Technologies, Tokyo, Japan in 1969 and 1971, and 1974, respectively. He joined Fujitsu Laboratories Ltd., in 1974 and has been engaged in research and development of semiconductor technologies for high-performance LSIs. He was assigned as Head of Silicon Technology Laboratory, Fujitsu Laboratories Ltd. in 2001 and Chief Scientist & Director of Akiruno Technology Center, Fujitsu Ltd.

in 2003. He moved to Tohoku University as Professor of Graduate School of Engineering in 2004. Dr. Ito is a member of Japan Society of Applied Physics, IEEE and the Electrochemical Society. He received the Teshima Award, Watanabe Award, Ohm Technology Award, Ohkouchi Award, and Yamazaki Award in 1975, 1981, 1999, 2000, 2006, respectively.