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PAPER

Self-Vth-Cancellation High-Efficiency CMOS Rectifier Circuit for UHF RFIDs

Koji KOTANI[†a)] ***and*** **Takashi ITO**[†]**,** ***Members***

SUMMARY A high-efficiency CMOS rectifier circuit for UHF RFID applications was developed. The rectifier utilizes a self-Vth-cancellation (SVC) scheme in which the threshold voltage of MOSFETs is cancelled by applying gate bias voltage generated from the output voltage of the rectifier itself. A very simple circuit configuration and zero power dissipation characteristics in biasing enable excellent power conversion efficiency (PCE), especially under small RF input power conditions. At higher RF input power conditions, the PCE of the rectifier automatically decreases. This is the built-in self-power-regulation function. The proposed SVC CMOS rectifier was fabricated with a 0.35-μm CMOS process and the measured performance was compared with those of conventional nMOS, pMOS, and CMOS rectifiers and other types of Vth cancellation rectifiers as well. The SVC CMOS rectifier achieves 32% of PCE at the −10 dBm RF input power condition. This PCE is larger than rectifiers reported to date under this condition.

key words: *radio frequency identification (RFID), ultra-high frequency (UHF), rectifier, self-Vth-cancellation, power conversion efficiency (PCE)*

1. Introduction

The application of a passive-type radio-frequency identification (RFID) tag is rapidly expanding in various fields, including supply chain management, logistics, access control, etc. [1]. Passive RFID tags have no battery and must be powered by an RF signal radiated from a reader/writer (R/W). There are several types of passive RFIDs in terms of frequency bands. High-frequency (HF) RFIDs use near-field magnetic coupling for power/data transfer, resulting in a communication distance of less than 1 m. RFIDs using Ultra-High-Frequency (UHF) or higher frequency bands utilize far-field electromagnetic wave transmission and can achieve a longer communication distance. However, since free space receivable power using appropriate antenna is proportional to λ^2 and electromagnetic waves are easily absorbed by materials at higher frequency, the communication distance of the μ-wave RFID using the 2.45 GHz band, for instance, is limited to less than 1 m [2]. From such considerations, the UHF band (860–960 MHz) is the best choice to realize the longest communication distance. Recently, UHF RFIDs having communication distances of 7 m have been reported [3].

The available power at the tag antenna P_{AVAIL} can be theoretically calculated by the following equation:

$$P_{AVAIL} = \left(\frac{\lambda}{4\pi R}\right)^2 P_{EIRP} G_{tag},$$

where λ is the wavelength of the EM wave, R is the distance between R/W and the tag, P_{EIRP} is the effective isotropic radiation power of R/W, and G_{tag} is the tag antenna gain. Note that perfect impedance matching between the tag antenna and the tag circuit as well as perfect matching of polarization planes of the R/W antenna and the tag antenna are assumed. P_{EIRP} is determined by regional regulations (4 W for US and Japan), and G_{tag} is mainly determined by the allowable antenna area (1.64 for $\lambda/2$ dipole antenna).

Under the conditions where the frequency is 953 MHz, P_{EIRP} is 4 W, and G_{tag} is 1.64, the available power P_{AVAIL} is resultantly as small as 114 μW (−9.4 dBm), assuming that the distance R is 6 m. Input RF power is then converted into DC power by a rectifier circuit and supplied to the tag circuits. Since the power dissipation of the tag circuit P_{tag} is roughly determined by the functions implemented in the tag (varies from 10 to 100 μW according to the tag functions), PCE of the rectifier circuit which is defined by P_{tag}/P_{AVAIL} should be as large as possible in order to achieve larger R. When P_{tag} is 30 μW, a PCE of larger than 26% is required at the very low input power condition of −9.4 dBm in order to achieve a communication distance R of 6 m. This is very challenging since it is very difficult to achieve a higher PCE under very low input power conditions.

The PCE of the rectifier circuit is affected by circuit topology, diode parameters, and input RF signal amplitude. Since the input RF signal voltage of RFIDs at the far-end position in the range of communication distance is quite small, as described above, a small turn-on voltage of the diode device is the most important factor. A Schottky diode having a turn-on voltage of 200–300 mV can be utilized with a charge pump configuration [3], [4], but at greater processing cost. A diode-connected MOSFET is compatible with the CMOS process, but the PCE is generally worse than in the case of the Schottky diode due to the large threshold voltage (Vth). However, when Vth-cancellation techniques are utilized, the PCE can be increased dramatically. A semi-passive tag utilizing a switched-capacitor external-Vth-cancellation (EVC) scheme has been proposed [5], [6]. However, since the operation of a switched-capacitor circuit requires an external power supply and clocking, this scheme cannot be applied to passive RFIDs. A passive tag utilizing the internal-Vth-cancellation (IVC) circuit composed of a current-mirror bias circuit has also been reported [7], [8].

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This scheme can work effectively under large input power conditions but not in small input power conditions since Vth-cancellation bias voltage is created by dividing the output voltage, which is very small when input power is small.

We have developed a high-efficiency CMOS rectifier circuit based on the self-Vth-cancellation (SVC) scheme [9]. The circuit requires no power dissipation to cancel Vth and realizes large PCE at very small input RF power conditions. In addition, the circuit has a self-power-regulation function, where the PCE is automatically degraded at input power conditions higher than optimal operating conditions to regulate output DC voltage.

In this paper, the performance of the SVC CMOS rectifier circuit is compared with those of conventional rectifier circuits as well as previously proposed Vth-cancellation rectifier circuits. In addition, the circuit operation depending on the frequency and output loading condition is evaluated.

The paper is organized as follows. Section 2 describes qualitative analysis of the conventional rectifier circuit. Section 3 gives a circuit configuration of the newly-developed self-Vth-cancellation rectifier circuit. Section 4 describes measurement setups for a fabricated test circuit. Measurement results and discussion are found in Sect. 5, which is followed by a conclusion in Sect. 6.

2. Conventional Rectifier Circuits

Figure 1 shows a conventional rectifier circuit for RFIDs, which has a multi-stage voltage multiplier configuration based on the Dickson charge pump [10]. Input RF voltage is applied through coupling capacitor C_c and rectified DC voltage is smoothed and stored in storage capacitor C_s. A multistage configuration, in which diodes are connected in series and coupled parallel to the RF input, is utilized to generate an appropriate DC output voltage from a small RF input voltage.

In order to reveal the factors limiting the PCE of the rectifier circuit, simple analysis is carried out. Figure 2 shows I-V characteristics of a diode. In order to simplify the analysis, the diode I-V characteristics are assumed to be ideal except that they have non-zero turn-on voltage V_{TO}. RF input signal voltage is applied through a coupling capacitor C_c, its waveform being shown in the figure as $v_D(t)$. Due to the ideal rectification characteristics of the rectifier, the highest voltage of $v_D(t)$ is clipped at V_{TO}. Therefore, DC offset voltage V_{DC} is generated. As a result, the following simple equation is possible.

$$V_{RF} = V_{DC} + V_{TO}$$
$$\therefore V_{DC} = V_{RF} - V_{TO},$$

where V_{RF} is the peak voltage amplitude of the applied RF signal. DC output voltage of the rectifier circuit can be given by

$$V_{OUT} = N \cdot V_{DC} = N\left(V_{RF} - V_{TO}\right),$$

where N is the number of diode stages. It can be concluded that the smaller the V_{TO}, the larger the V_{OUT} becomes.

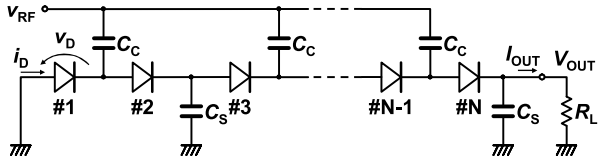

Fig. 1 Conventional rectifier circuit for RFIDs.

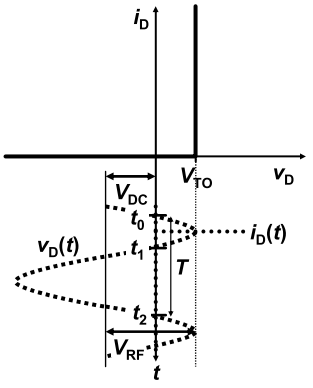

Fig. 2 Simplified diode I-V characteristics and schematic representations for applied voltage and current waveforms.

PCE of the rectifier is defined by the output power P_{OUT} divided by the input power P_{IN}. The input power can be written as the sum of the output power and the loss of the rectifier. Therefore, PCE can be written as

$$PCE \equiv \frac{P_{OUT}}{P_{IN}} = \frac{P_{OUT}}{P_{OUT} + P_{LOSS}} = \frac{P_{OUT}}{P_{OUT} + N \cdot P_{DIODE}},$$

where P_{DIODE} is the power loss of each diode. Diode loss originates from the resistive loss when current flows through the diode. In the simplified model shown in Fig. 2, current only flows when the applied voltage is equal to V_{TO} and the time-averaged current is equal to the DC output current. Therefore, P_{DIODE} can be written as

$$\begin{aligned} P_{DIODE} &= \frac{1}{T}\int_{t_0}^{t_2} v_D(t) \cdot i_D(t)\, dt \\ &= V_{TO} \cdot \frac{1}{T}\int_{t_0}^{t_2} i_D(t)\, dt = V_{TO} \cdot I_{OUT}, \end{aligned}$$

where I_{OUT} is the output current. Meanwhile, P_{OUT} can be written as

$$P_{OUT} = V_{OUT} \cdot I_{OUT} = N \cdot V_{DC} \cdot I_{OUT}.$$

Finally, we obtain the PCE formula as follows:

$$\begin{aligned} PCE &= \frac{N \cdot V_{DC} \cdot I_{OUT}}{N \cdot V_{DC} \cdot I_{OUT} + N \cdot V_{TO} \cdot I_{OUT}} \\ &= \frac{V_{DC}}{V_{DC} + V_{TO}} = \frac{V_{RF} - V_{TO}}{V_{RF}} \end{aligned}$$

Again, the smaller the V_{TO}, the larger the PCE becomes. It can be said that the small V_{TO} is essential in order to achieve large PCE of a rectifier.

In actual rectifier circuit operations, there are some non-ideal effects. The diode has a finite on-resistance and non-zero reverse leakage current resulting in an increase in diode energy loss. Also, the circuit has some residual resistances in wiring and contacts resulting in an increase in energy loss. Input RF signal voltage is divided by the coupling capacitor with parallel connected diode capacitance and substrate parasitic capacitance and applied to the diode, resulting in a small increase in energy loss. Capacitance itself does not cause energy loss, but substrate capacitance has a resistive loss component caused by the conductive substrate. Furthermore, the increase in capacitance increases the reactive current, resulting in a small increase in energy loss due to residual resistance of the circuit. Therefore, we cannot calculate actual PCE accurately by the previously shown equation, but can obtain a general guideline for increasing PCE.

As described above, a small V_{TO} is essential in order to achieve a large PCE. For this purpose, a Schottky diode is utilized in rectifiers [3], [4]. It has a relatively small V_{TO} of around 200–300 mV. The rectifier circuit using the Schottky diode achieves a large PCE, but it is not compatible with the conventional CMOS technology and requires costly fabrication processing. Instead, a diode-connected MOS transistor is widely used. The effective V_{TO} of the diode-connected MOS transistor is almost equal to the threshold voltage of the MOS transistor, which is slightly larger than a Schottky diode but smaller than a pn-junction diode. Figures 3(a), (b) and (c) show nMOS, pMOS and CMOS rectifier circuits, respectively. A unit doubler circuit composed of two-stage diodes is shown for purposes of simplicity. The nMOS transistor has a larger transconductance than the pMOS transistor, resulting in smaller on-resistance and larger PCE. The pMOS is superior to nMOS in some cases since the increase in threshold voltage due to the back-bias effect can be eliminated by individual well biasing when using an n-well process. The CMOS configuration has characteristics in between those of nMOS and pMOS.

While the PCE for rectifiers using a simple diode-connected MOS transistor is not so large, it can be drastically increased when an appropriate Vth-cancellation mechanism is applied. Figure 4(a) schematically shows the external-Vth-cancellation (EVC) scheme [5], [6] utilized in a semi-passive tag. nMOS gate bias voltage is generated with a switched-capacitor (SC) circuit. Since the operation of the SC circuits requires an external power supply and clocking, this scheme cannot be applied to passive-type RFIDs.

Figure 4(b) shows the internal-Vth-cancellation (IVC) scheme [7], [8]. Gate bias voltage is generated internally from the output DC voltage by a bias generation circuit. This circuit works very well in large input power conditions, but not under small input power conditions since gate bias voltages are generated by the voltage division mechanism. In addition, the bias generation circuit dissipates some amount of power due to the DC pass current, resulting in slight degradation in PCE. In this IVC scheme, the CMOS configuration has been applied. The CMOS configuration is effective, especially for the Vth-cancellation scheme, where gate bias voltages are DC and bias circuits can be isolated from the nodes at which an RF signal is applied.

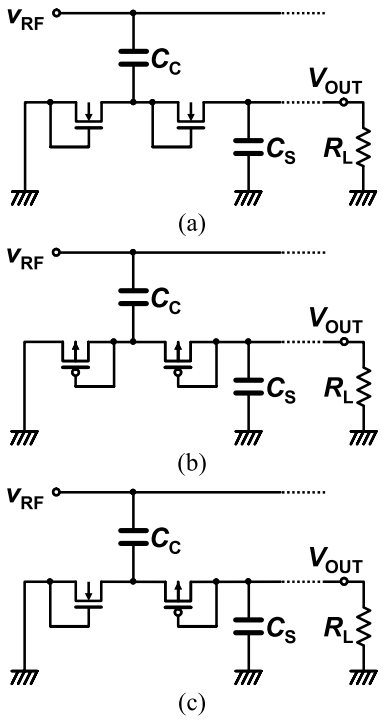

Fig. 3 (a) nMOS rectifier circuit, (b) pMOS rectifier circuit and (c) CMOS rectifier circuit.

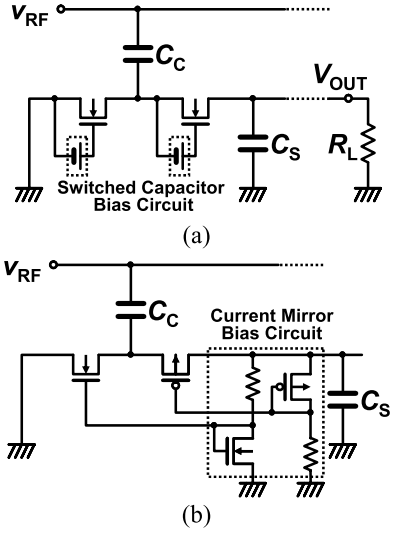

Fig. 4 (a) External-Vth-cancellation (EVC) [5], [6] and (b) Internal-Vth-cancellation (IVC) [7], [8] rectifier circuits.

3. Self-Vth-Cancellation Rectifier Circuit

Figure 5 shows the developed self-Vth-cancellation (SVC) CMOS rectifier circuit. It is the same as the conventional CMOS rectifier circuit described in the previous section ex-

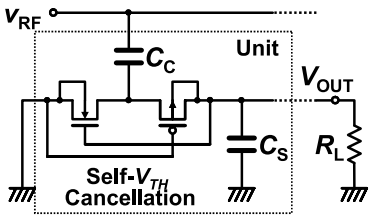

Fig. 5 Proposed self-Vth-cancellation (SVC) rectifier circuit.

cept that gate electrodes of the n-MOS transistor and the p-MOS transistor are connected to the output terminal and ground terminal, respectively. This connection boosts gate-source voltages of the n-MOS and p-MOS transistors as much as possible. In other words, threshold voltages of the MOS transistors are equivalently decreased by the same amount as the output DC voltage.

Compared with the EVC scheme using the switched-capacitor mechanism [5], [6] and the IVC scheme [7], [8], this SVC scheme is much simpler and requires no additional power, possibly resulting in better PCE. In addition, the SVC scheme can obtain the best Vth cancellation efficiency at lower DC output voltage conditions, and hence at the lower RF input power and voltage conditions, as compared with the IVC scheme in which gate bias voltage is generated by dividing the DC output voltage by the IVC circuit. This is quite important, especially in UHF RFID applications where input RF signal voltage is quite small.

In diode-connected MOSFET with Vth cancellation, excess gate bias voltage results in effective Vth which is too small. In this condition, reverse leakage current, which is ignored in the previous simplified analysis, increases dramatically, resulting in increased diode loss under conditions of large gate bias. In the SVC scheme, since gate bias voltage is directly supplied from output DC voltage, PCE decreases under conditions of large DC voltage output. As a result, PCE of the SVC rectifier circuit will first increase with the increase in input power, but then decrease with the further increase in input power, exhibiting some peak value in between.

4. Experimental

A test circuit for the SVC CMOS rectifier was designed and fabricated with 0.35 μm CMOS 2P3M technology. A single unit stage composed of one nMOS and one pMOS transistor was designed. Drawn gate length and width of the MOS transistors are 0.4 μm and 40 μm for n-MOS and 0.4 μm and 120 μm for p-MOS, respectively. MOS transistors have a multi-finger structure where each finger has a length of 5 μm. Measurement of threshold voltages of n-MOS and p-MOS showed them to be 0.585 V and −0.828 V, respectively. An input coupling capacitor C_C and an output smoothing capacitor C_S were fabricated with a polysilicon-polysilicon capacitor structure and designed to have capacitances of 3.4 pF and 7.6 pF, respectively. Figure 6 shows a photomicrograph of the fabricated SVC CMOS rectifier circuit. A conventional CMOS rectifier, an n-MOS-only rectifier, and a p-MOS-only rectifier with the same device sizes and parameters as those in the SVC CMOS rectifier were also designed for performance comparison.

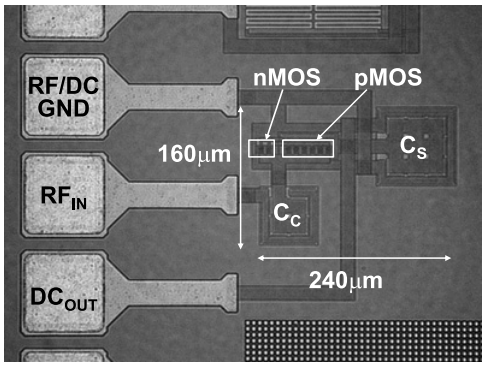

Fig. 6 Photomicrograph of the fabricated SVC CMOS rectifier test circuit.

Measurement conditions were as follows unless otherwise specified. RF frequency was 953 MHz, which is the center frequency of the licensed frequency band for UHF RFIDs in Japan. To emulate the power dissipation of functional circuits in RFIDs as a load of a rectifier, a 10 kΩ resistor was connected to the DC output terminal of the rectifier.

Impedance of the test chip was measured with a Vector Network Analyzer (VNA), N5242A. The test chip was probed with a 125 μm-pitch *Infinity* GS Probe. Open, short, and load calibrations were done at the probe tip using an Impedance Standard Substrate (ISS).

Due to the process technology specifications, we could not use low-loss RF probing pads and MIM capacitors with shielded structures. Instead, conventional pads and poly-poly capacitors were used. Therefore, there was significant energy loss associated with the lossy Si substrate due to pad-to-substrate and capacitor bottom plate-to-substrate coupling. De-embedding processes were conducted to extract the true input impedance and input power applied to the rectifier. Figure 7 shows an equivalent circuit representation of the rectifier circuit on a die. We modeled a pad, a coupling capacitor bottom plate and a rectifier circuit with an output load as individual parallel-connected RC networks. Three-step measurements using dummy structures were carried out to extract all component parameters and de-embed them. First, only the pad (dummy pad) was probed and parallel resistance and capacitance were measured as R1 and C1, respectively. Next, the pad with a coupling capacitor bottom plate was probed and parallel resistance and capacitance were measured as R2 and C2, respectively. We constructed this dummy structure by a Focused Ion Beam (FIB) system, where the interconnect between the top plate of the coupling capacitor and internal node of the rectifier was cut off. Third, the whole rectifier circuit with pad and input coupling capacitor was probed, and parallel resistance and capacitance were measured as R3 and C3, respectively, with various source power settings. Component parameters in

the equivalent circuit can be calculated from measured resistances and capacitances as follows:

$$
\begin{aligned}
R_{PAD} &= R1 \\
C_{PAD} &= C1 \\
R_{BP} &= 1/\left(1/R2 - 1/R1\right) = 1/\left(1/R2 - 1/R_{PAD}\right) \\
C_{BP} &= C2 - C1 = C2 - C_{PAD} \\
R_{RECT} &= 1/\left(1/R3 - 1/R2\right) \\
&= 1/\left(1/R3 - 1/R_{PAD} - 1/R_{BP}\right) \\
C_{INT} &= C3 - C2 = C3 - C_{PAD} - C_{BP}
\end{aligned}
$$

RF input power to the rectifier P_{IN} can be calculated by the following equation:

$$
P_{IN} = P_S\left(1 - |S|^2\right)\frac{\dfrac{1}{R_{RECT}}}{\dfrac{1}{R_{PAD}} + \dfrac{1}{R_{BP}} + \dfrac{1}{R_{RECT}}},
$$

where P_S is the source power supplied from VNA in the forward direction. S is a measured 1-port s-parameter (reflection coefficient). The power injected into the chip at the pad was calculated by $P_S(1 - |S|^2)$. This compensates the impedance mismatch effect between the VNA (50 Ω) and the chip. We eliminated the impedance-matching-related problems such as the power reflection caused by impedance mismatch and losses in the matching circuit from the following PCE analyses since they depend on the antenna and matching circuit designs, which are beyond the scope of this paper. The actual input power to the rectifier can then be calculated by resistive division with parasitic resistances. By these calculations, we can evaluate the intrinsic performance of the rectifiers.

PCE can be calculated by

$$
PCE = \frac{P_{OUT}}{P_{IN}} = \frac{V_{OUT}\cdot I_{OUT}}{P_{IN}} = \frac{\dfrac{V_{OUT}^2}{R_L}}{P_{IN}}.
$$

Output DC voltage V_{OUT} was measured by an auxiliary ADC of the VNA. Input impedance Z_{RECT} of the rectifier without pad and lossy substrate coupling can be estimated by

$$
\begin{aligned}
Z_{RECT} &= 1/\left(1/R_{RECT} + j\omega C_{RECT}\right) \\
&= 1/\left\{1/R_{RECT} + j\omega\left(C_{INT} + C_{BP}\right)\right\},
\end{aligned}
$$

where equivalent input capacitance of the rectifier C_{RECT} is taken as a parallel connection of C_{INT} and C_{BP}. This is not so accurate since the parallel RC model of the substrate coupling of the input capacitor bottom plate is not so accurate but gives an appropriate approximation.

Note that since R_{PAD}, C_{PAD}, R_{BP} and C_{BP} are essentially linear components in the first-order approximation, these dummy structures were measured once for each measurement frequency at a source power level of 0 dBm. Extracted parameters were used for measurements at various power levels. At 953 MHz, R_{PAD}, C_{PAD}, R_{BP}, and C_{BP} were determined to be 1.03 KΩ, 301 fF, 1.18 KΩ and 320 fF, respectively.

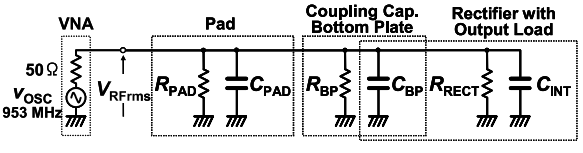

Fig. 7 Equivalent circuit representation of the fabricated rectifier circuit with parasitic components.

5. Measurement Results and Discussions

Figure 8 shows measured PCE as a function of RF input power P_{IN}. The SVC CMOS rectifier developed in this study was compared with conventional nMOS, pMOS and CMOS rectifiers under the same design parameters and measurement conditions. Although PCEs for conventional rectifiers monotonically increase in input power P_{IN}, PCE of the SVC CMOS rectifier first increases and then decreases with the further increase in P_{IN} as expected. PCE of the SVC CMOS rectifier exhibits a peak PCE of 32% at a P_{IN} of −10 dBm. At this condition, the SVC CMOS rectifier has a larger PCE than conventional nMOS, pMOS and CMOS rectifiers. In addition, it is superior to the EVC nMOS rectifier [5], [6] and the IVC CMOS rectifier [7], [8], although the design parameters and measurement conditions of the latter two are different from those of the SVC CMOS rectifier.

The conventional nMOS rectifier is superior to the SVC CMOS rectifier in the small input power range below −14 dBm. This is because under extremely small input power conditions the SVC mechanism cannot work well and the SVC CMOS rectifier operates just like a conventional CMOS rectifier. The CMOS rectifier contains a pMOS diode which has a larger turn-on voltage than an nMOS diode, resulting in degraded PCE. However, since PCE obtained by the nMOS rectifier under the extremely small input power conditions is too small to be applied practically, this inferiority of the SVC CMOS under these conditions is not

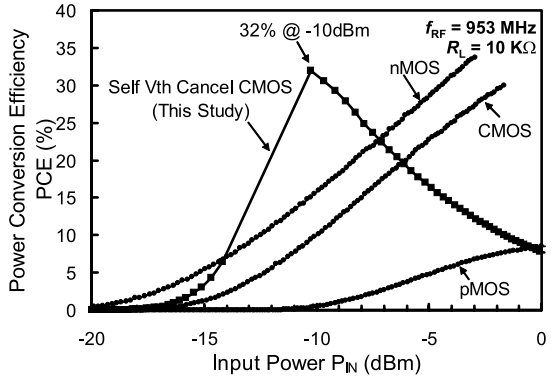

Fig. 8 Measured PCE as a function of RF input power P_{IN}. The SVC CMOS rectifier developed in this study is compared with conventional nMOS, pMOS and CMOS rectifiers.

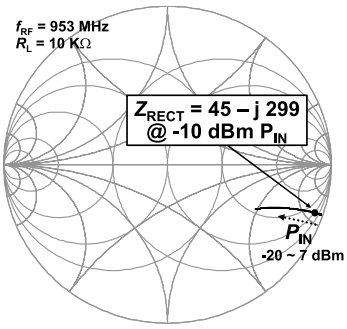

Fig. 9 Measured input impedance Z_{RECT} of the rectifier.

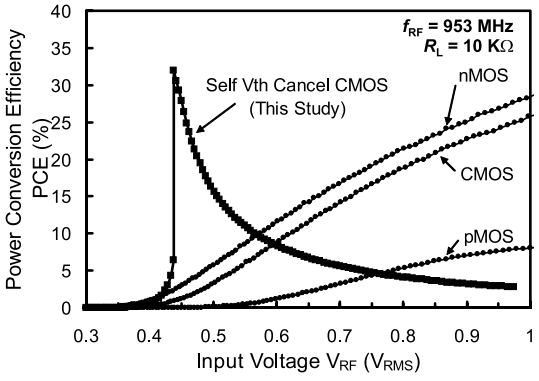

Fig. 10 *PCE*s as a function of RF input voltage V_{RF}.

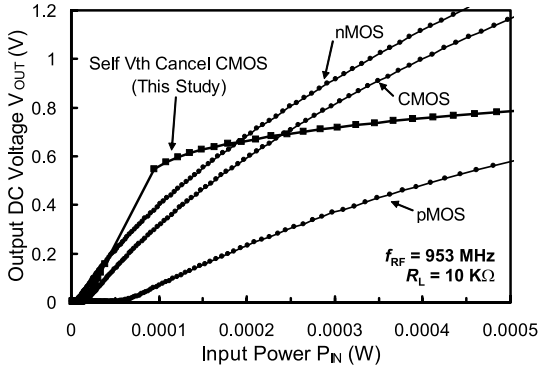

Fig. 11 DC output voltage V_{OUT} as a function of RF input power P_{IN}.

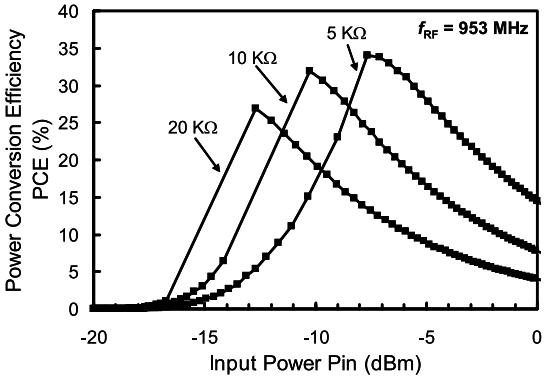

Fig. 12 Output load resistance R_L dependency on *PCE*s.

disadvantageous at all.

In addition, PCE of the SVC CMOS rectifier is inferior to the conventional nMOS rectifier when input power becomes larger than −7 dBm. This is also no problem since the larger PCE under the small input power condition is the only requirement and large PCE at large input power condition is not helpful for achieving longer communication distance of RFIDs.

Figure 9 shows measured input impedance of the rectifier as a function of input power. When PCE had a maximum at the input power level of −10 dBm, input impedance Z_{RECT} of the SVC CMOS rectifier was measured to be 45 − j299 Ω, which corresponds to the equivalent parallel resistance R_{RECT} and capacitance C_{RECT} of 2.03 kΩ and 547 fF, respectively. With regard to the impedance matching with an antenna, a matching circuit should be designed so as to match this impedance in order to achieve the largest total efficiency.

PCEs are re-plotted as a function of RF input voltage and shown in Fig. 10. PCE of SVC rises sharply at an RF input voltage of 440 mVrms. This is the threshold for triggering the positive feedback mechanism. When RF input voltage reaches this point, loop gain exceeds unity and DC output voltage, which is increased by the increase in PCE, further increases PCE. Meanwhile, DC output voltage excessively increases, effective threshold voltage of diode-connected MOS transistors decreases due to the SVC mechanism and leakage current increases, resulting in the suppression of the increase in PCE. Then the operation reaches steady-state, where loop gain falls to unity and positive feedback ends. At this point the maximum PCE can be obtained.

Figure 11 shows DC output voltage V_{OUT} as a function of RF input power P_{IN}. DC output voltage of the SVC CMOS rectifier monotonically increases with the increase of input power. Therefore, there is no problem in the operation stability, even though PCE has peaking characteristics as shown previously. DC output voltage V_{OUT} reaches 500–600 mV at an RF input power of 100 μW(−10 dBm). When RF input power further increases, however, DC output voltage does not increase so rapidly, exhibiting saturation characteristics. This is a kind of self-voltage-regulation function and is one of the interesting features of the SVC CMOS rectifier. The requirement for a following-stage precise voltage regulator can be relaxed. This function cannot be obtained by static Vth-cancellation schemes such as zero-threshold MOS (native MOS) rectifiers.

When DC output load changes, PCE characteristics are altered, as shown in Fig. 12. When DC output load resistance R_L increases, the PCE curve shifts to the smaller input power region. Peak PCE can be obtained with a smaller input power condition. This is because peak PCE is obtained at a fixed DC output voltage of about 0.55 V, regardless of output load resistance, as shown in Fig. 13. PCE has a maximum when DC output voltage, which is the gate bias voltage in the SVC CMOS rectifier, reaches a value around V_{TH}.

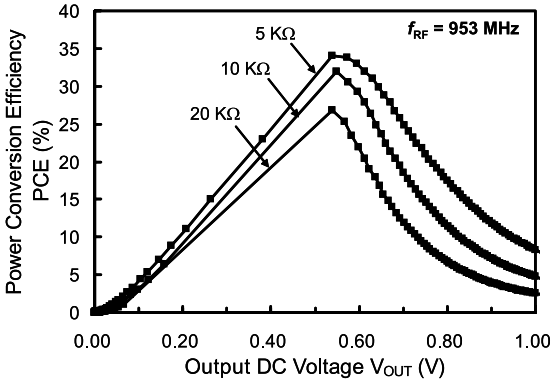

Fig. 13 *PCE*s as a function of DC output voltage V_{OUT}. Output load resistance R_L was set at 5 KΩ, 10 KΩ and 20 KΩ.

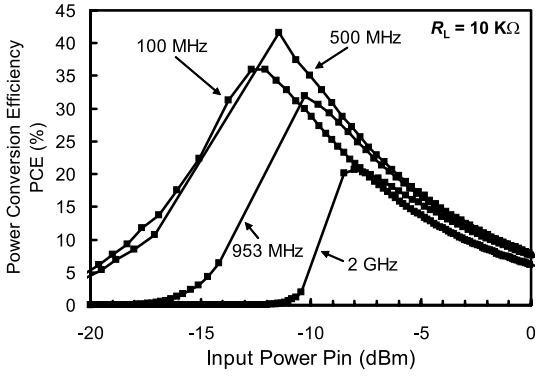

Fig. 14 Operation frequency dependence on *PCE*s.

Values of peak PCE, however, slightly decrease with the increase in R_L. This phenomenon can be interpreted as follows: Increasing the output load R_L results in a decrease of not only the power dissipation in R_L but also forward diode loss due to the smaller forward current. The reverse leakage current and resultant loss, however, are maintained at the same level since the gate bias voltage of the diode-connected MOSFETs under peak PCE conditions are almost the same regardless of R_L, as shown in Fig. 13. Therefore, the ratio of the diode loss, which is composed of the sum of the forward and reverse diode losses, to the total power dissipation increases, resulting in a slight decrease in PCE.

Figure 14 shows the effect of the operation frequency. When the operation frequency increases, PCE decreases. This is because energy loss increases with the increase in the high frequency current flowing in the circuit due to the increase in the reactance component. PCE increases with the decrease in operation frequency down to 500 MHz. When the operation frequency decreases down to 100 MHz, however, PCE decreases to less than that of 500 MHz. This is because admittance of the coupling capacitor C_C is not sufficient at low operation frequency to apply an RF signal to the diode effectively, resulting in a degraded PCE.

Incidentally, 500–600 mV of DC output voltage shown in Fig. 11 is insufficient as V_{DD} supply for logic circuits in RFID tags. Static logic circuits generally require at least 2 × Vth or 3 × Vth for stable operation. For achieving 2 × Vth or 3 × Vth for DC output voltage, stacking of the unit SVC CMOS rectifier circuit shown in Fig. 5 is effective. By stacking, we can design a rectifier circuit which can provide appropriate DC output voltage at the optimal operating point where the maximum PCE can be obtained. For example, when two unit SVC rectifier circuits are stacked and a 20 kΩ resister is connected to the DC output terminal as an output load, each stage works just the same as a single stage rectifier having an output load of 10 kΩ. Therefore, doubled output DC voltage (0.55 × 2 = 1.1 V) can be obtained with the same peak PCE (32%) as that of the single stage case. The peak PCE, however, is obtained at the 3 dB larger input power condition (−7 dBm) since two unit rectifier circuits are connected in parallel to the RF input terminal and two times larger input power is required.

6. Conclusions

We developed a high-efficiency CMOS rectifier circuit utilizing the self-Vth-cancellation scheme for UHF RFID applications. The rectifier creates V_{GS}-boosting bias voltage from the DC output voltage itself. The circuit is quite simple and requires no additional power dissipation, resulting in large PCE, especially under very small RF input power conditions. The rectifier is equipped with a self-regulation function, which can ease the requirement for a following-stage precise voltage regulator. The 31% PCE achieved at −10 dBm of RF input power enables the operation of an RFID chip dissipating power of 30 μW at a 6.5 m range under the UHF RFID regulations (4 W_{EIRP}).

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