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# High-Frequency Half-Integral Subharmonic Locked Ring-VCO-Based Scalable PLL in 90 nm CMOS

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***Abstract*—A wide-frequency-range ring-VCO-based PLL with half-integral subharmonic locking was realized (PLL area: 0.11 mm$^2$) by adopting 90 nm CMOS technology. The proposed circuit is configured with two cascaded PLLs; one of them is a reference PLL (frequency tuning range: 1.2–2.4 GHz) that generates reference signals to the other one from low-frequency external reference signals. The other is a main PLL (frequency tuning range: 6.1–10.4 GHz) that generates high-frequency output signals. A high-frequency half-integral subharmonic locking technique was used to decrease the phase noise characteristics.**

**For a 46 MHz input reference signal, the 1-MHz-offset phase noise of the PLL was −89 dBc/Hz without injection locking (PLL output frequency: 6.62 GHz = 4.5 × 32 × 46 MHz); with half-integral subharmonic locking at the same output frequency, the 1-MHz-offset phase noise was −99 dBc/Hz (power consumption from a 1.0 V power supply: 23 mW).**

***Index Terms*—Phase-locked loops, injection locked oscillators, ring VCO, phase noise, CMOS integrated circuits**

## I. Introduction

Conventional multistandard wireless mobile terminals contain multiple RFICs. To reduce manufacturing costs, one-chip RF LSI systems are needed. A great effort is being made to develop wideband and/or multiband RF solutions using highly scaled advanced CMOS processes. The use of such processes is beneficial to A/D and D/A converters and digital baseband circuits. However, it is very difficult to reduce the size of RF/analog circuits, especially power amplifiers and oscillator circuits that include voltage-controlled oscillators (VCOs) and phase-locked loops (PLLs), because of the presence of passive devices such as inductors that do not scale with advancements in technology.

This paper describes a study on a ring-VCO-based PLL for a wide-band system as a potential solution to realize scalable high-performance PLLs. In order to improve its phase-noise performance, the proposed PLL is augmented with high-frequency half-integral subharmonic locking.

## II. Subharmonically injection-locked PLL

Fig. 1 (a) shows a conventional charge pump PLL. The closed-loop transfer function of this kind of PLLs, $H(s)$, is proportional to $K_{\rm VCO}$ [1]. The loop bandwidth of a PLL can be expressed as

$$\omega_{-3\,\rm dB} = \frac{K_{\rm VCO} I_{\rm P} R}{2\pi N}, (\zeta > 1), \qquad (1)$$

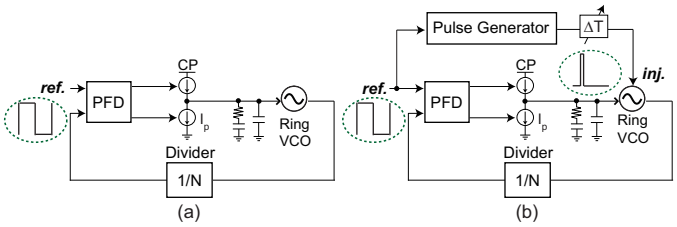


Fig. 1. (a) Configuration of a conventional CP-PLL and (b) an injection-locked PLL.

where $I_{\rm P}$ is the charge pump (CP) current, $R$ is the filter resistance, $N$ is the division ratio of the feedback loop, and $\zeta$ is the damping factor of a PLL. PLLs that use ring type VCOs for the scalability are required to have a wide loop bandwidth for lowering their poor phase noise characteristics. However, there is a trade-off between the loop bandwidth and the stability of PLLs. In general the loop bandwidth must be smaller than $2\pi f_{\rm ref}/10$, where $f_{\rm ref}$ is the reference-signal frequency. Consequently, there is a limitation on lowering the phase noise in ring-VCO-based CP PLLs.

Subharmonic injection techniques have been introduced to suppress the phase noise of PLLs [2], [3]. Fig. 1 (b) shows an injection-locked PLL that has two phase locking mechanisms, respectively, a phase-locked loop and injection locking. Fig. 2 (d) shows the reason why injection-locked PLLs can reduce the jitter, namely phase noise characteristics. When a VCO is in the free-running condition (Fig. 2 (a)), the jitter will be spread randomly over time. When a pulse signal is injected to the VCO at $T_{\rm inj}$ (Fig. 2 (b)), the phase of a VCO output aligns with that of an injected pulse. In this case, the phase correction occurs at $T_{\rm inj}$ and the jitter will be reduced because the clean edge of the injected pulse may exchange the flicking edge of a VCO output as shown in Fig. 2 (b). Fig. 2 (c) shows that the maximum jitter can be maintained by using the feedback operation of PLLs [4]. Consequently, injection-locked PLLs may have the intermediate characteristics between injection-locked VCOs and conventional PLLs (Fig. 2 (d)).

Let us consider trade-offs between two phase noise mechanisms in injection-locked PLLs. The locking range of injection locking is proportional to the power and the frequency of the

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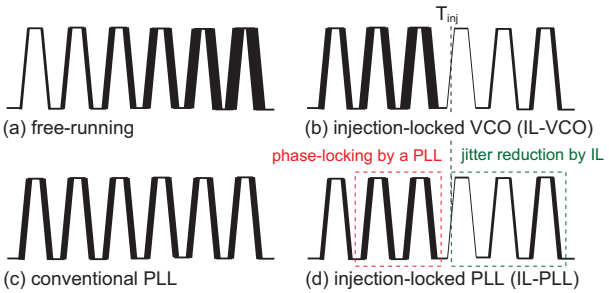


Fig. 2. Conceptual phase evolution over time in an injection-locked PLL.

injected signal and can be expressed as

$$\omega_{\mathrm{L}} \approx \frac{\omega_{\mathrm{o}}}{2Q} \cdot \frac{I_{\mathrm{inj}}}{I_{\mathrm{OSC}}} \cdot \frac{1}{N}, \tag{2}$$

where $\omega_0$ is the output frequency of the PLL, $I_{\mathrm{OSC}}$ is the tail current of the VCO, and $I_{\mathrm{inj}}$ is the current injected into the VCO [5]. When the locking range of injection locking is much wider than the loop bandwidth of a PLL ($\omega_{-3\,\mathrm{dB}}$ : $constant$), the PLL acts like an injection-locked VCO because the maximum jitter of each edge may be much smaller than that by phase locking of a conventional PLL. Conversely, when the locking range of injection locking is narrow enough, the PLL acts like a conventional PLL because the maximum jitter of each edge could not be larger by phase-locking as a conventional PLL and it may show phase evolutions across a period of an injected signal as shown in a conventional PLL. Therefore, it is required to have a wide locking range of injection locking than the loop bandwidth of a PLL for improving phase noise characteristics and we will see that an injection-locked PLL with a ring VCO has a wide locking range because its topology has a low quality factor as shown in eq. 2.

## III. High-Frequency Half-Integral Subharmonic Locking Topology for Noise Reduction

A paper on half-integral subharmonic injection locking based on the use of a ring VCO has been presented [6]. A differential ring VCO can be easily designed to lock to half-integral subharmonics by giving its necessary symmetry properties. Suppose that a ring VCO consists of differential delay cells and has a certain symmetry (Fig. 5). Fig. 3 (a) shows differential waveforms of the VCO in the case of both integral and half-integral subharmonic locking. The two output nodes are shorted when the injection signal is inputted into the nMOS switches. Phase corrections may occur at the time and the jitter reduced.Generally, there are two points of time during the period of the output signal when two output nodes can be shorted because of topological symmetry as shown in Fig. 3 (a). Consequently, the VCO is capable of both integral and also half-integral subharmonic locking.

One advantage of using half-integral subharmonic locking is to be able to use high-frequency reference signal and can make the locking range of injection locking, $\omega_{\mathrm{L}}$ wide as shown in eq. 2. Fig. 3 (b) shows that the phase noise of

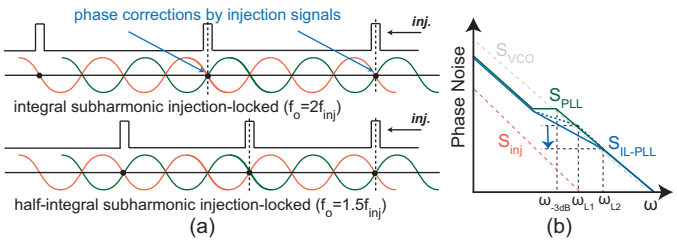


Fig. 3. (a) Voltage waveforms of output nodes and injection signals versus time, (b) phase noise shaping with injection locking when $\omega_{\mathrm{n}} < \omega_{\mathrm{L1}}, \omega_{\mathrm{L2}}$.

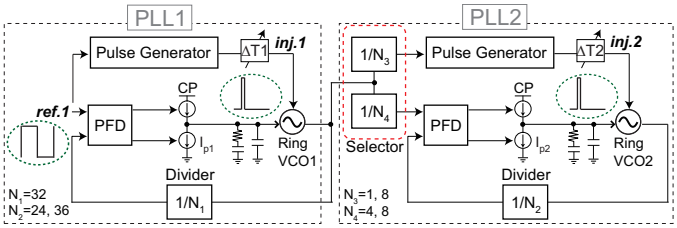


Fig. 4. Configuration of the proposed PLL.

the reference signal mainly affects the output phase noise at low offset frequencies and that the phase noise of the PLL becomes dominant as the offset frequency approaches the edge of the locking range [2]. Therefore, it will improve phase noise characteristics to the edge of the locking range to use high-frequency reference signals.

Fig. 4 shows the configuration of the proposed PLL that enables the use of half-integral subharmonic locking. The proposed PLL consists of two injection-locked PLLs. A reference PLL, namely, PLL1 generates reference signals to a main PLL, namely, PLL2 from low-frequency external reference signals. In this topology, when we choose divider ratios respectively as $N_2 = 36$, $N_3 = 1$ and $N_4 = 8$, the ratio between the reference signal to PLL2 and the output frequency of PLL2 may be $4.5$ and we can apply half-integral subharmonic locking. Time delay cells $\Delta T1$, $\Delta T2$ are implemented to control the time when injection signals are inputted because phase corrections can occur easily when differential output nodes are shorted in the direct injection locking scheme (Fig. 3 (a)) .

The topologies of ring VCOs are shown in Fig. 5. They are based on a four-stage (Fig. 5 (a)) and a two-stage (Fig. 5 (b)) differential ring oscillators. Fig. 6 shows the topology of the proposed delay cell. The delay cell of the proposed ring VCO contains a latch that generates delay variation by positive feedback in order to satisfy the oscillation condition [1].

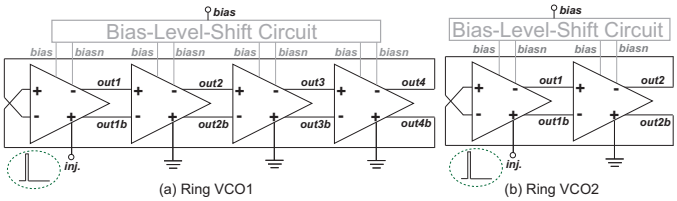


Fig. 5. (a) Ring VCO1 (b) Ring VCO2.

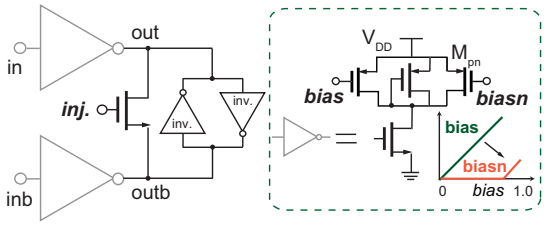


Fig. 6. Proposed differential delay cell.

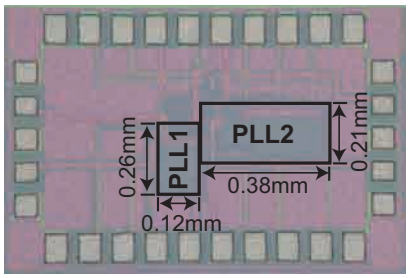


Fig. 7. A micrograph of the proposed PLL.

In order to achieve subharmonic injection locking, nMOS switches are connected at the nodes between differential output nodes, and rail-to-rail pulses are injected into one of switches.

Moreover, the pMOS resistive loads are used for tuning the output frequency. Biasn, the bias level shifted by 0.6V from the main control voltage is applied to a pMOS $M_{\rm pn}$ in order to ensure that the total equivalent resistance of the two pMOS resistive loads is linear with respect to the main control voltage, bias. Therefore, tuning the oscillation frequency while maintaining the $K_{\rm VCO}$ across the tuning range of the VCO can be achieved. [3].

## IV. Measurement Results

Fig. 7 shows a chip micrograph of the proposed PLL. The PLL was fabricated by a 90 nm CMOS process. The proposed PLL that includes both PLL1 and PLL2 occupies an area of 0.11 $\rm mm^2$. It was measured with 1.8V power supply. The frequency tuning range of PLL1 was 1.2–2.4 GHz when PLL1 was locked to reference signals of 38–75 MHz which were generated by an Anritsu MP1761B pulse pattern generator. That of a main PLL, namely, PLL2 was 6.1–10.4 GHz under phase locking by a PLL. At an output frequency of $f_{02} = 6.62$ GHz, the power consumption of the PLL was 23 mW.

Fig. 8 shows frequency spectra of PLL1 at $f_{01} = 1.47$ GHz($= 32 \times 46$ MHz) with an external reference signal of $f_{\rm ref} = 46$ MHz. It shows that the spurious levels without and with injection locking are, respectively, $-43$ dBc and $-40$ dBc. They were measured using an Agilent Technologies

TABLE I
Measurement Parameters.

| $V_{\rm DD}$ [V] | $f_{\rm ref}$ [MHz] | $I_{\rm P1}$ [$\mu A$] | $I_{\rm P2}$ [$\mu A$] | $N_2$ | $N_3$ | $N_4$ |
|---|---|---|---|---|---|---|
| 1.0 | 46 | 110 | 20 | 36 | 1, 8 | 8 |

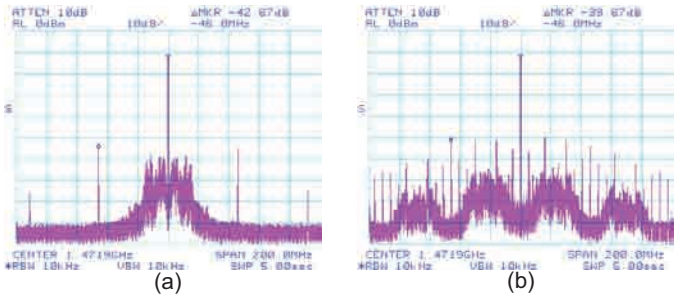


Fig. 8. Measured output frequency spectra of the PLL1 at $f_{01} = 1.47$ GHz(=32 × 46 MHz) (a) without and (b) with injection locking.

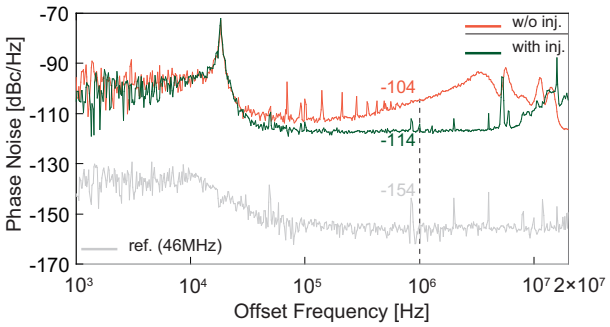


Fig. 9. Phase noise measured at $f_{01} = 1.47$ GHz (=32 × 46 MHz).

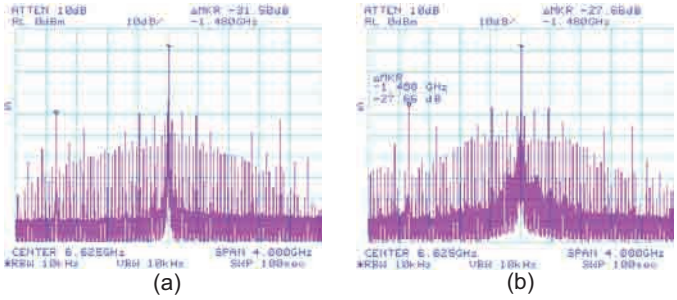


Fig. 10. Measured output frequency spectra of the proposed PLL at $f_{02} = 6.62$ GHz (a) without and (b) with injection locking ($f_{\rm inj} = f_{\rm o1}$).

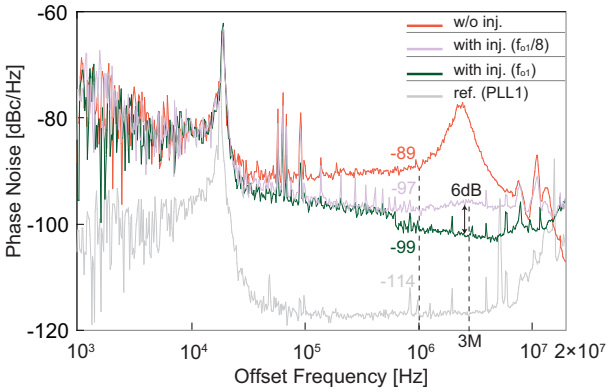


Fig. 11. Phase noise measured at $f_{02} = 6.62$ GHz.

TABLE II
PERFORMANCE SUMMARY AND COMPARISON OF PLLS.

| Ref. | CMOS Technology | $f_{\rm o}$ [GHz] | N=$f_{\rm o}/f_{\rm ref}$ | FTR* [%] | $L_{\rm in-bnad}$ [dBc/Hz] | Offset [MHz] | $L_{\rm norm}$** [dBc/Hz$^2$] | Power [mW] | Area [mm$^2$] | VCO |
|---|---|---|---|---|---|---|---|---|---|---|
| This work | 90 nm | 1.47 | 32 | 65 | $\mathbf{-114}$ | 1 | $\mathbf{-221}$ | 10 (sim.) | 0.031 | Ring |
| | · | 6.62 | 144 | 51 | $\mathbf{-99}$ | 1 | $\mathbf{-219}$ | 23 | 0.11 | · |
| [3] | 0.18 $\mu$m | 1.44 | 16 | 84 | $-122$ | 0.2 | $-226$ | 39 | 0.1 | Ring |
| [8] | 90 nm | 2.46 | 61.5 | 29 | $-105$ | 0.3 | $-217$ | 10 | 0.37 | LC |
| [9] | 90 nm | 9.24 | 35 | 33 | $-97$ | 1 | $-212$ | 56 | 0.09 | Ring |
| [10] | 0.18 $\mu$m | 8.98 | 17 | 38 | $-110$ | 1 | $-222$ | 58 | 0.77 | LC |
| [11] | 0.18 $\mu$m | 8.45 | 32 | 108 | $-98$ | 1 | $-212$ | 117 | 5.5 | LC |

*(Frequency tuning ratio) = (Tuning range)/(Center frequency). **Normalized in-band phase noise = $L_{\rm in-band} - 20\log N - 10\log f_{\rm ref}$

8563EC spectrum analyzer. Fig. 9 shows the phase noise characteristics at $f_{01} = 1.47\,\text{GHz}$ ($= 32 \times 46\,\text{MHz}$), as measured by an Agilent Technologies E5052A signal source analyzer. Without injection locking, a 1-MHz-offset phase noise of $-104\,\text{dBc/Hz}$ was generated in PLL1. With injection locking, the measured phase noise was $-114\,\text{dBc/Hz}$ at an offset of 1 MHz. A 1-MHz-offset phase noise of an external reference signal of $f_{\rm ref} = 46\,\text{MHz}$ was $-154\,\text{dBc/Hz}$.

Fig. 10 shows frequency spectra of PLL2 at $f_{02} = 6.62\,\text{GHz}$ ($= 144 \times 46\,\text{MHz}$) with PLL1 outputs of $f_{01} = 1.47\,\text{GHz}$ ($N_3$=1). It shows that the spurious levels without and with half-integral subharmonic locking ($f_{\rm o2} = 4.5 \times f_{\rm o1}$) are, respectively, $-32\,\text{dBc}$ and $-28\,\text{dBc}$. The poor spurious levels were caused by the poor matching of current switching charge pump. Fig. 11 shows the phase noise characteristics at $f_{02} = 6.62\,\text{GHz}$ ($= 144 \times 46\,\text{MHz}$). Without injection locking, a 1-MHz-offset phase noise of $-89\,\text{dBc/Hz}$ was generated in the proposed PLL. With half-integral subharmonic injection locking, the measured phase noise was $-99\,\text{dBc/Hz}$ at an offset of 1 MHz. With half-integral subharmonic locking ($f_{\rm o2} = 4.5 \times f_{\rm o1}$), we successfully achieved 6 dB lower phase noise at 3MHz offset than the case with integral subharmonic locking ($f_{\rm o2} = 32 \times f_{\rm o1}/8$).

A summary of the performance of the proposed PLL and a comparison of the PLL with other PLLs that were designed using various kinds of phase-locking methods are given in Table II. To make a fair in-band phase noise comparison between in various kinds of PLL designs, the dependency of in-band phase noise on $f_{\rm ref}$ and N should be normalized out [7]. Therefore, normalized in-band phase noise $L_{\rm norm}$ was applied for comparison. The proposed PLL shows a relatively good $L_{\rm norm}$ value. Also its area is small and comparable to that of other circuits.

## V. CONCLUSION

We proposed a scalable injection-locked PLL based on a wide-frequency-range ring VCO. The proposed PLL that consists of two PLLs was designed in order to generate high-frequency output signals with low-frequency external reference signals. We used subharmonic injection locking for improving the phase noise characteristics of a ring-VCO-based PLL. Moreover, we verified the usefulness of half-integral subharmonic locking that could make a powerful means of realizing a low-phase-noise high-resolution PLL.

The injection-locked PLL was fabricated by adopting 90 nm CMOS technology. The reference PLL generates low-phase-noise output signals with injection locking. A 1-MHz-offset phase noise of $-99\,\text{dBc/Hz}$ was achieved at an output frequency of 6.62 GHz by using the output of the reference PLL. The area of the PLL was as small as $0.11\,\text{mm}^2$ and the total power consumption was as small as 23 mW.

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