論文 / 著書情報
Article / Book Information

論題(和文)	
Title(English)	CMOS Inverter-based Wideband LNA in 65nm Technology
著者(和文)	DAYANG NUR SALMI D, 大鶴 基格, 中島 智也, 田野井 聡, 天川 修平, 石原 昇, 益 一哉
Authors(English)	Dayang Nur Salmi Dharmiza, Mototada Oturu, Tomoya Nakajima, Satoru Tanoi, Shuhei Amakawa, Noboru Ishihara, Kazuya Masu
出典(和文)	, , , C-12-37
Citation(English)	2010 年電子情報通信学会エレクトロニクスソサイエティ大会, , , C-12-37
発行日 / Pub. date	2010, 9
URL	http://search.ieice.org/
権利情報 / Copyright	本著作物の著作権は電子情報通信学会に帰属します。 Copyright (c) 2010 Institute of Electronics, Information and Communication Engineers.

CMOS Inverter-based Wideband LNA in 65nm Technology

Dayang Nur Salmi Dharmiza, Mototada Oturu, Tomoya Nakajima, Satoru Tanoi, Shuhei Amakawa, Noboru Ishihara, and Kazuya Masu

Solution Science Research Laboratory, Tokyo Institute of Technology

1 Introduction

Small-sized, low power consumption and wide-band low noise amplifier (LNA) in RF circuits have been immensely developed in recent years. Today, electronic devices contain multiple RF front-end circuits for various kind of wireless communications. We believe all wireless communications standard below 10GHz can be covered by a single chip. Since passive devices such as inductors and capacitances consume large area despite of the developing scaling technology, we proposed a CMOS inverter-based LNA.

2 Wideband LNA Design

Figure 1 shows schematic of LNA circuit and fabricated micrograph. For this design, we proposed two methods to enhance LNA bandwidth. First, by cascading inverters with adaptation of Cherry Hooper topology to the CMOS amplifier, Miller effect is reduced and this results in wider bandwidth. The effective input capacitance for the first stage is

$$C_{\text{in}} = C_{\text{gs1}} + C_{\text{gs2}} + (C_{\text{gd1}} + C_{\text{gd2}})[1 + (g_{\text{m1}} + g_{\text{m2}})Z_{\text{x}}], \quad (1)$$

where Z_{x} is the input impedance of the second inverter stage and is given approximately by

$$Z_{\text{x}} \simeq \frac{1}{g_{\text{m3}} + g_{\text{m4}}}. \quad (2)$$

Second method for bandwidth enhancement is by implementing inverter feedback to the cascaded inverters. Usually, capacitance or inductive peaking technique is proposed for broadening the bandwidth, but since inductance and capacitance size is not suitable for circuit area scalability, we introduced an active peaking technique using scalable CMOS inverter. With feedback inverter, the feedback is negative at low frequency, and as the frequency becomes higher, the feedback changes to positive.

In the end of combination of proposed design, an additional low-resistance feedback amplifier is added to provide high load impedance to the voltage amplifier and better 50 Ω output matching.

3 Fabrication Results

The circuit was fabricated by using 65 nm CMOS process. Without the output buffer, our LNA only occupies 0.0016 mm^2 of area with power consumption 18.2 mW from 1.2 V voltage supply.

Simulation and measured results for S-parameters and noise figure are shown in Fig 2. and Fig. 3. Based on our S21 characteristics, our LNA gain was about 15 dB with frequency range from 100 MHz to 7.5 GHz. The measured noise figure was 4.8-8.8 dB, while the input third-order intercept point (IIP3) was -15 dBm.

4 Conclusion

In this work, we proposed scalable LNA architecture with smaller chip size and wider bandwidth. Our circuit has successfully achieved wide bandwidth and considerably low noise. For future work, we are going to investigate methods on how to improve circuit linearity and noise figure for our designed LNA.

Acknowledgments

This work was partially supported by STARC, MIC.SCOPE, KAKENHI, NEDO, and VDEC in collaboration with Agilent Technologies, Cadence Design Systems, Inc., and Mentor Graphics, Inc.

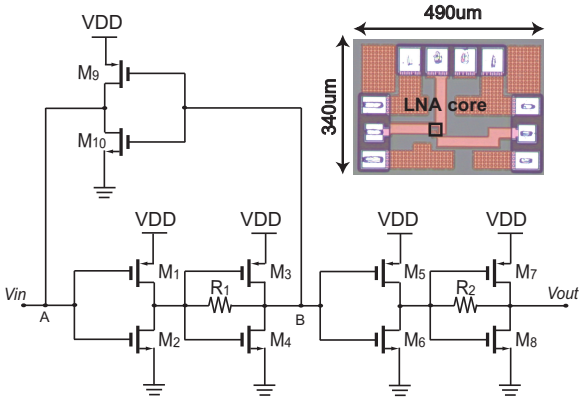

Fig. 1 LNA schematic and chip micrograph

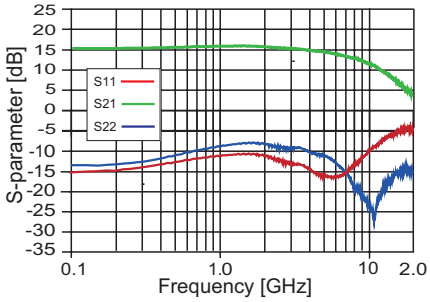

Fig. 2 S-parameter characteristics.

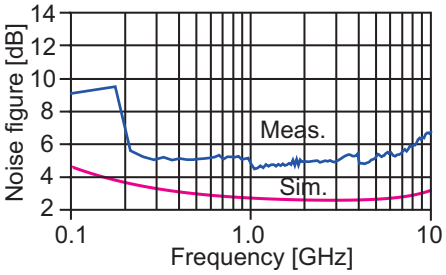

Fig. 3 Noise figure characteristics.