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Category(English)	Doctoral Thesis
種別(和文)	論文要旨
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（博士課程）
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論 文 要 旨

THESIS SUMMARY

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要旨（英文 800 語程度）
Thesis Summary (approx.800 English Words)

This thesis analyzes a working principle of the rotary traveling wave oscillator (RTWO) and proposes a low phase noise all-digital phase locked loop (ADPLL).

Chapter 1 discusses general issues of voltage controlled oscillators (VCOs) and PLLs. In order to meet the market demand for realizing high speed wireless communications, it is required for the PLLs to achieve low phase noise and high operation frequency while consuming less power with high level of integration. Even though analog charge-pump PLLs have been the standard choice, ADPLLs have gained recent interest to overcome the performance degradations of analog circuits due to CMOS process scaling. In the ADPLL, a time-to-digital converter (TDC) converts the analog phase information into the digital domain. However, the TDC generates quantization noise which degrades the phase noise of the PLL. Moreover, the phase noise contribution due to the TDC increases as the carrier frequency becomes higher. To overcome these problems, this thesis proposes an ADPLL that can achieve excellent phase noise even for higher carrier frequencies. By using the RTWO, the analog-to-digital conversion is merged into the oscillator core, breaking the existing tradeoff between power consumption, quantization noise and operation frequency. This is made possible by an innovative ADPLL architecture combined with detailed analysis of the working principles of the RTWO.

Chapter 2 presents the phase error calibration technique. By introducing non-uniform distributed capacitors in the resonator, the phase relationships among multiphase outputs available from the RTWO are adjusted to compensate for physical asymmetries. To have a better understanding of the proposed method, a new model, in which the RTWO is described as injection locked multiple standing wave oscillators (SWOs), is developed. The proposed model reveals possible modes of oscillation, their stability, and provides better design insights. The prototype is fabricated in a 110 nm RF-CMOS process, demonstrating more than 10° phase control range at the vicinity of 3 GHz oscillation frequency.

Chapter 3 analyzes phase noise in the RTWO. By treating the RTWO as a superposition of multiple SWOs, a phase noise formula for the SWO is first derived, and then it is extended to the RTWO. The phase noise expression is verified by simulation and measurements. The physically based approach and simple resulting expressions make it possible for circuit designers to optimize the RTWO for a given phase noise without lengthy simulations.

Chapter 4 presents a low noise RTWO based ADPLL. By using multiphase signals available from the RTWO, the analog phase information is directly converted into the digital domain. Unlike the conventional TDC based ADPLL, the proposed ADPLL eliminates power hungry inverter delay chains as well as real-time period normalization. The proposed approach significantly simplifies the ADPLL architecture while maintaining excellent phase noise. The PLL is implemented in a 65 nm CMOS process. The 32-phase embedded phase-to-digital converter (PDC) achieves only 4.7 ps effective time resolution in the fractional phase detection. The measured in-band phase noise is -108 dBc/Hz at 4 GHz with a 78 MHz reference.

Chapter 5 compares performance of the RTWO with other VCO topologies and also discusses the pros and cons of the RTWO. In order to make fair comparison, the FoM of the RTWO is theoretically derived and it is confirmed that under the sinusoidal assumption the best FoM of the RTWO can be the same as the one for the *LC*-VCO. However, the measurement shows that the phase noise of the RTWO is not good as the state-of-the-art VCOs. It is expected to introduce the low phase noise techniques to further improve the phase noise performance. The chapter also discusses the performance of the PLL in terms of the PLL FoM (jitter performance normalized by power consumption). Thanks to the fine resolution PDC, the proposed ADPLL gives the excellent FoM of -232.1 dB, showing the effectiveness of the proposed approach.

Chapter 6 summarizes the achievements of this work and concludes the thesis. Unlike the conventional TDC approach, the proposed RTWO based ADPLL has a unique property of maintaining the same in-band phase noise regardless of the operation frequency. Thus, it is suitable for future high carrier frequency systems such as millimeter wave and beyond. The remaining work is further study to improve the RTWO core performance and to minimize its required area. The former will be solved by introducing the low phase noise topologies such as class-C mode and the latter will be alleviated by investigating the compact ring structure and employing higher carrier frequency.

備考 ： 論文要旨は、和文 2000 字と英文 300 語を 1 部ずつ提出するか、もしくは英文 800 語を 2 部提出してください。
Note : Thesis Summary should be submitted in either a copy of 2000 Japanese Characters and 300 Words (English) or 2 copies of 800 Words (English).