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Doctoral Thesis

A Study on Metal Gate Electrodes with Nano-Sized Grains for Scalable La-silicate Gate Dielectrics

A Dissertation Submitted to the Department of

Electronics and Applied Physics

Interdisciplinary Graduate School of Science and Engineering

Tokyo Institute of Technology

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Abstract

Downscaling of the MOSFET has been the driving force for circuit evolution. Feature size of MOSFET becomes smaller and smaller, billions of CMOS transistors are integrated on a single chip. However, power consumption caused by leakage current increased to unacceptable level. Therefore, new materials and new structures in MOSFET have been introduced to solve these issues. High-k gate dielectrics have enabled continuous scaling in CMOS devices by increasing the capacitive coupling of gate electrode to the channel which eventually suppresses the short channel effects, while reducing the gate leakage current. Considering further equivalent oxide thickness (EOT) scaling down to 0.45 nm, which is required in the year of 2026 from ITRS roadmap, high-k materials should be directly in contact with Si channels. Some of attempts to achieve direct contact of high-k on Si channels have been proposed so far; those include precise oxygen partial pressure controlled process and a thermal process to reduce the interfacial layer by incorporating additional elements in the metal gates. In addition to these processes, La-silicate can be in direct contact with Si channels by means of silicate reactions between La_2O_3 layer and Si channel. The prominent features of La-silicate are that the structure is amorphous and the silicate reaction does not show any channel surface orientation dependency, which are advantageous for scaled devices with three dimensional channels. Issues in La-silicate/Si interfaces include D_{it} in the order of high 10^{11} cm^{-2}/eV, and interface roughness presented at both metal/La-silicate and La-silicate/Si interfaces, which results in channel mobility degradation due to La-silicate thickness variation. An experimental work has shown that metal gate materials affect the interface properties, so the impact of metal gate should be clarified. According to reports, the crystal structure and grain size of metal gates strongly impact

on electrical properties of MOS devices, in terms of threshold voltage variability, metal gates with grain less than 5nm or amorphous are preferable. Therefore, in this study, metal gate electrodes with nano-sized grains for scalable La-silicate gate dielectrics were experimentally investigated.

Novel sputtering processes have been introduced to form nano-sized metal gate. Multi-stacking of carbon and metal thin films with subsequent annealing process to reactively form metal carbides (TiC, TaC and W_2C) has been presented. Grain sizes of the carbides are as small as 3.9, 3.2, and 1.9 nm for TiC, TaC and W_2C, respectively. Work functions of TiC, TaC and W_2C layers have been extracted as 4.3, 4.7, and 4.9 eV, respectively, relatively high values owing to oriented growth. W_2C layer formed by the presented process gives high potential to gate electrode application in terms of grian size and oriented growth for scaled devices.

Electrical properties of La-silicate MOS devices and nMOSFET with nano-sized tungsten carbide (W_2C) gate electrode has been experimentally investigated. Interface state density (D_{it}) was suppressed by W_2C gate electrodes. Atomically flat metal/high-k and high-k/Si interfaces can be achieved by W_2C gate electrodes, where the interface roughness extracted from TEM is 0.26 and 0.12nm, respectively. Origin of interface state density is due to La-silicate/Si interface roughness due to grains in metal gate electrode. Electron μ_{eff} showed improvements in both low and high E_{eff}, especially 163 cm^2/Vs (E_{eff}=1MV) at an EOT of 0.63 nm was achieved, owing to lower D_{it} and reduced roughness scatterings.

Reliability of La-silicate with different gate electrodes, such as tungsten carbide and tungsten, was measured by TDDB and PBTI. Better reliability was obtained by nano sized W_2C gate electrode owing to atomically flat high-k/Si interface.

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Chapter 1 Introduction

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1.1 MOSFET downscaling

High-technology electronic products such as smart phones, laptops and digital cameras have already been a part of our life. The main device used for these products is Complementary Metal Oxide Semiconductor (CMOS) Field Effect Transistor. Since the first integrated circuits in 1971, the performance of CMOS devices has continued to improve over a forty year times by scaling rule. The scaling rule is called as Moore`s law [1.1]. According to this rule, the device voltages, device dimensions, current, capacitance and circuit delay time should be reduced by the same factor k, and main while, power dissipation per circuit is reduced by k^2. It shows that CMOS technology continues to advance generations every two years, and the device feature size decreases each year. However, power consumption caused by leakage current increased to unacceptable level [1.2], as shown in figure 1.1.

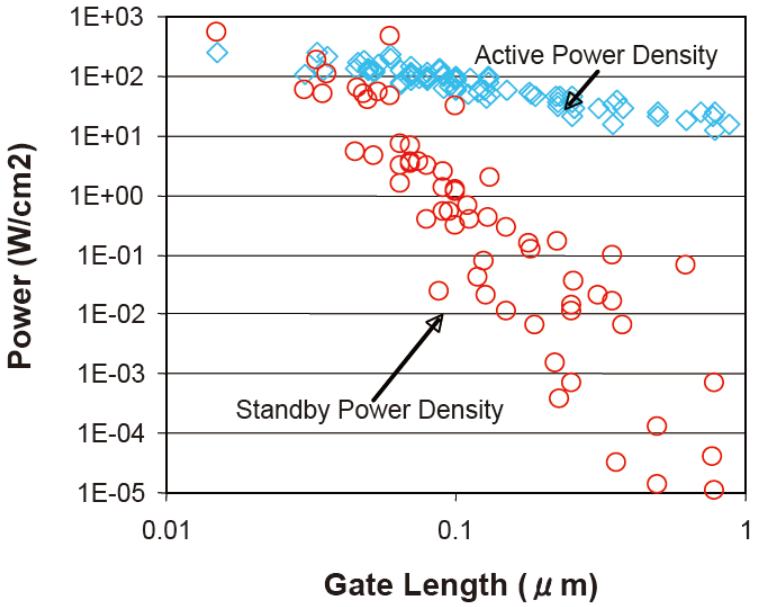

Figure 1.1 Power consumption trend with gate length scaling [1.2]

Simple scaling is no longer an option for improve MOSFET performance, therefore, for further scaling, new technologies such as strained channel, high-k/metal

gate stack, and multi-gate transistor (FinFET) is extensively studied, as shown in figure 1.2 [1.3]. Among these technologies, high-k/gate stack (combination of gate dielectrics and gate electrode) is quite important for planner and advanced type of MOSFETs.

Until recently, the most common used CMOS structure was doped poly-silicon on SiO_2, SiO_2 is utilized as gate insulator, and poly-Si is used as gate electrode, shown in figure 1.3. SiO_2 has been used as ideal gate dielectrics for forty years due to nice interface properties and good thermal stability [1.4]. However, with down-scaling, this system has faced the scaling limit due to the excess leakage current caused by short channel effects [1.5]. As a result, power consumption increases unacceptable level [1.6]. This physical limitation imposed by SiO_2 has led the research into the study of novel material of a physically thicker layer of oxide with high dielectric constant (high-k materials) and new structure advanced type of MOSFETs, such as FinFET and Nanowire structures.

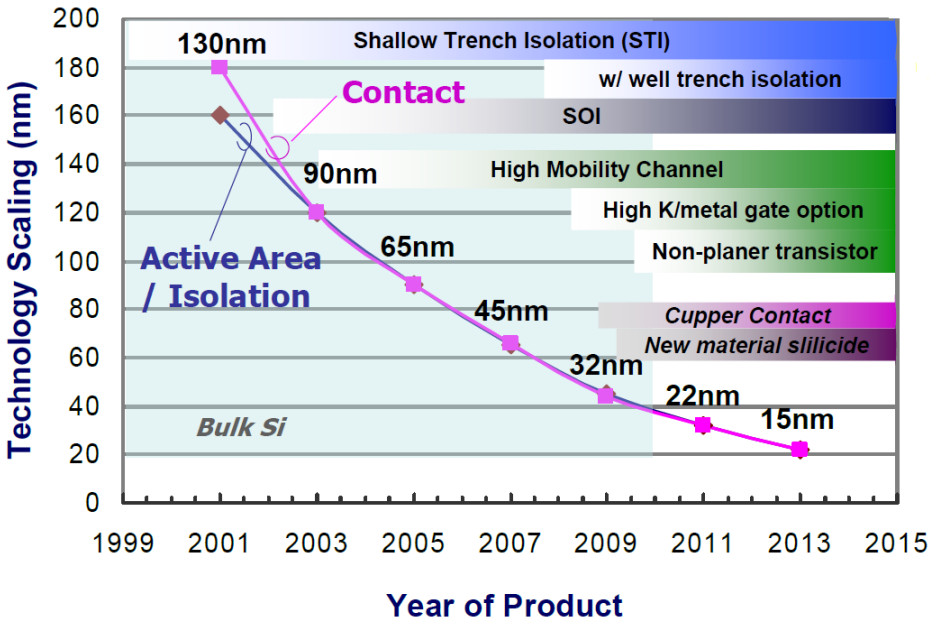

Figure 1.2 Device scaling roadmap [1.3]

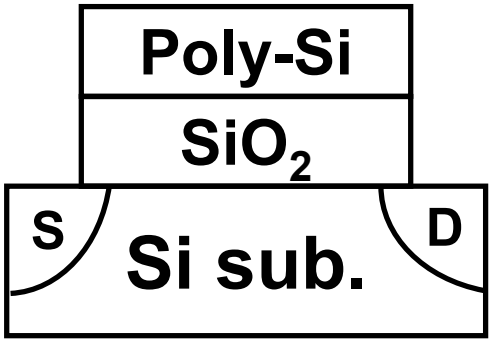

Figure 1.3 Schematic illustration of MOSFET

1.2 Innovative solutions for improving MOSFET performance

1.2.1 High-k/metal gate stack

As complementary metal oxide semiconductor (CMOS) technology continues to scale down duo to suppress leakage current and further scale, high-k gate dielectrics have been studied as alternative gate dielectrics to replace conventional SiO_2, There are many challenges reported in literature in replacing SiO_2 with high-k for high-performance CMOS [1.7, 1.8], and meanwhile metal thin layers have become the primary gate materials together with high-k gate dielectrics for scaled devices to eliminate the problems associated with poly-Si electrodes, as shown in Figure 1.4. In 2007, Intel introduced high-k/metal gate stack into their 45nm node devices, the figure 1.5 shows that the introduction of high-k dielectric and metal gate has caused the gate leakage current to be decreased by more than 10 times and the further EOT scaling can be possible [1.9].

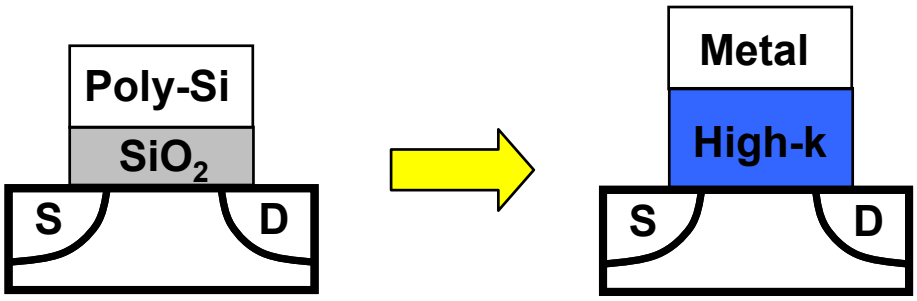

Figure 1.4 High-k gate dielectrics for further scaling

High-k materials make it possible to thicken physical thickness with the same equivalent oxide thickness (EOT), which means physical thickness can be thickened with the same gate capacitance. The capacitance and EOT can be written as,

$$C_{ox} = \frac{\varepsilon_{ox}\varepsilon_o}{t_{ox}} A, EOT = \frac{\varepsilon_{SiO_2}}{\varepsilon_{high-k}} t_{phys}$$

Where, ε_{SiO2} and $\varepsilon_{high\text{-}k}$ are the permittivity of SiO_2 (=3.9) and that of high-k materials, respectively.

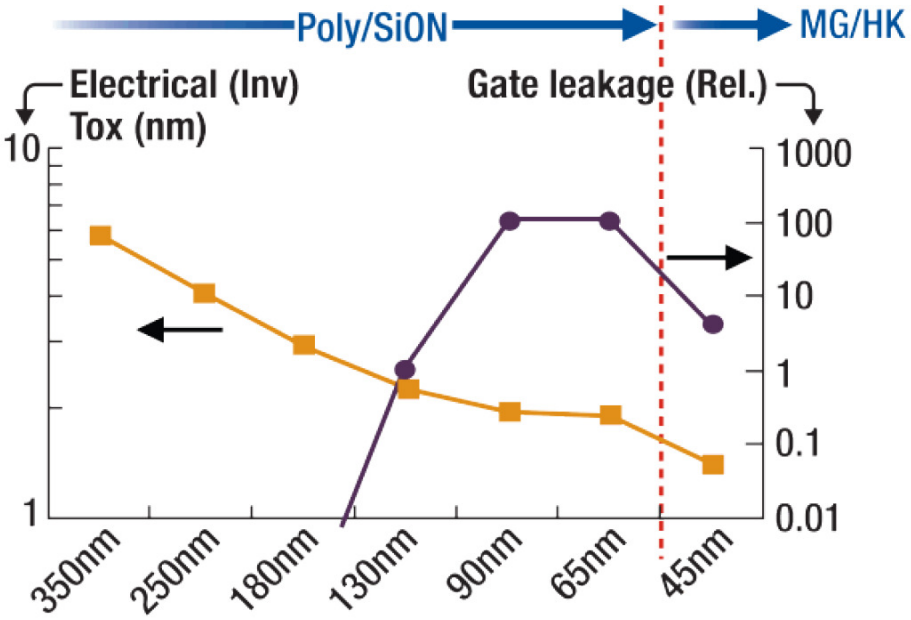

Figure 1.5 Gate leakage as a function of oxide thickness

at various technology nodes [1.9]

1.2.2 Multi gate FET

Downscaling of the conventional planar MOSFETs has required continuing efforts to suppress short channel effects. Recently, multi-gate and nanowire field-effect-transistors (FETs) with three-dimensional (3D) channels have drawing much interest duo to the excellent short-channel-effect immunity. Therefore, the metal oxide semiconductor (MOS) transistor with 3D channels has been considered as one of the promising candidates to overcome the scaling issues in planar FETs , as shown in figure 1.6 [1.10].

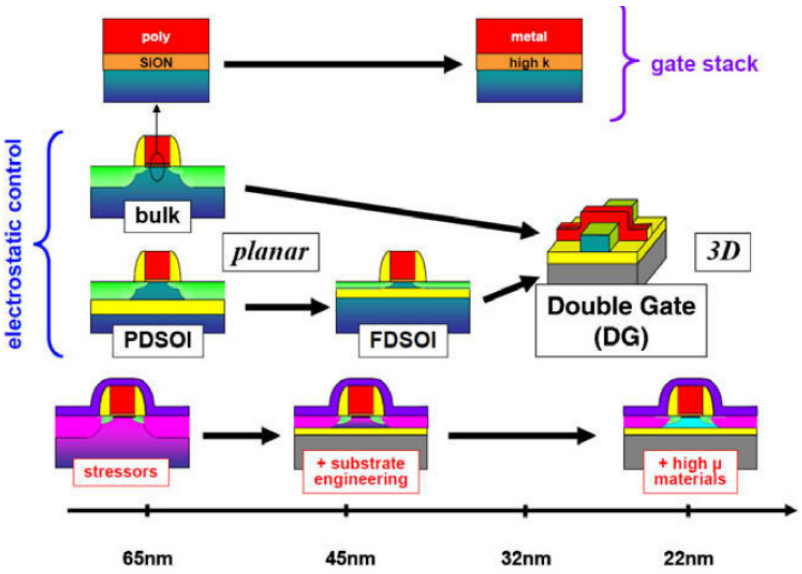

Figure 1.6 Technology node [1.10]

1.3 Introduction of high-k gate dielectrics

1.2.1 Requirements for high-k gate dielectrics

Selection of high-k materials is very important. In the past years, many companies, universities and research organizations spent major efforts investigating a wide range of high-k materials candidates for continue scaling of MOSFET. The main criteria for

selecting high-k materials were manufacturability, integration capabilities, and transistor performance. There are some requirements for selection of high-k materials, such as high dielectric constant, wide band gap, band offsets with Si, thermal stability, a good electrical interface, amorphous phase and direct contact with silicon substrate [1.11]. It is known that high-k dielectrics have one advantage than silicon oxide, it is a high dielectric constant. Figure 1.7 shows the relationship of static dielectric constant and band gap for candidate gate oxide [1.11]. There are a lot of materials are researched to accommodate new gate insulator for MOSFET, especially metal oxide like Al_2O_3, ZrO_3, HfO_2 and rare earth oxides have been expected to be the gate insulator for nest generation. Among them, Hf-based and La-based high-k materials have attracted much attention to replace SiO_2 gate dielectrics in advanced CMOS applications [1.12, 1.13].

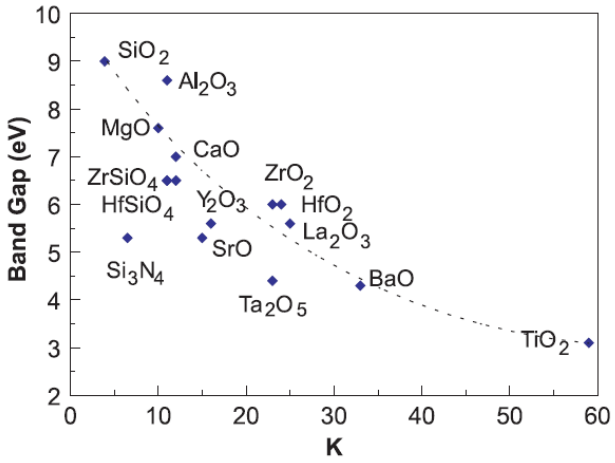

Figure 1.7 Relationship of static dielectric constant and band gap for candidate gate oxide

Due to further scaling of equivalent oxide thickness (EOT), direct contact of high-k/Si structure is indispensable [1.14, 1.15]. According to reports, a thin layer of SiO_2 is typically formed as interfacial layer to suppress the increase in interface state density or inversion carrier mobility degradation, as shown in figure 1.8 [1.16]. But the interfacial

layer between high-k dielectric and Si substrate, have limited further EOT scaling. Based on ITRS roadmap of planar bulk MOSFET, as shown in figure 1.9 [1.18], it can be seen that EOT of 0.5nm or beyond is required in near future. The removal of SiO_2 interfacial layer is an essential problem in high-k/metal gate stacks for further EOT scaling because of a low dielectric constant of SiO_2, although the interfacial layer is prepared for recovery from the degradation of effective mobility duo to the interfacial properties of high-k and Si interface. Therefore, for further scaling of EOT, direct contact of high-k dielectric and Si substrate is indispensable, as shown in figure 1.10.

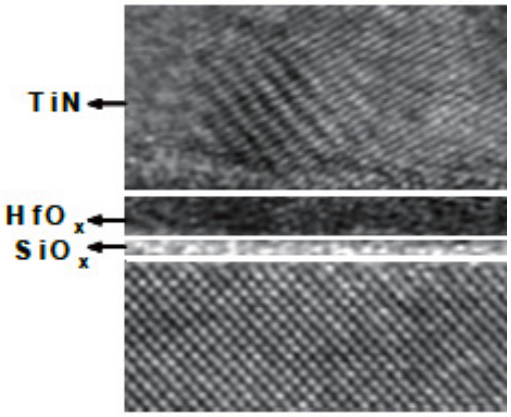

Figure 1.8 SiOx-interfacial layer growth at HfOx/Si interface [1.16]

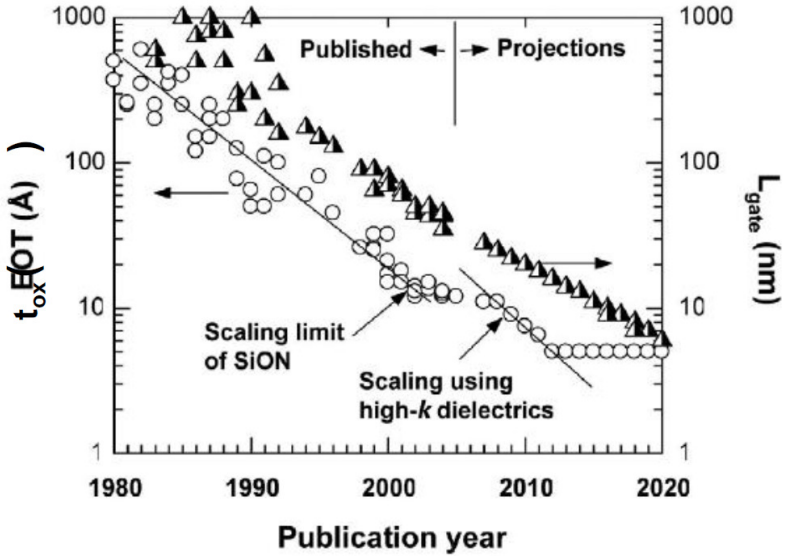

Figure 1.9 Scaling roadmap of planar bulk MOSFET [1.18]

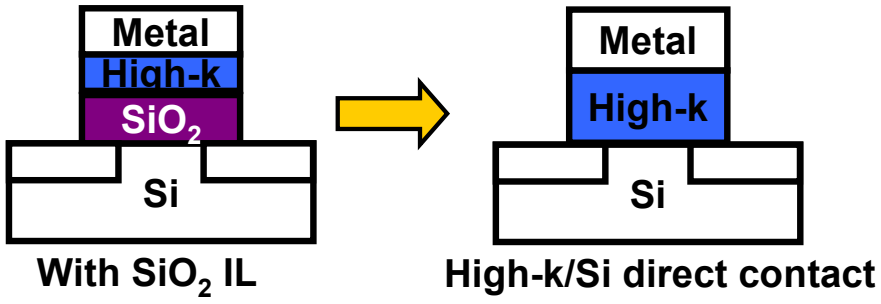

Figure 1.10 High-k/Si direct contact for scaled EOT beyond 0.5nm

The reported results show that, as shown in figure 1.11, the direct contact of high-k/Si structure can be achieved with Hf-based high-k materials to by SiO_2 interfacial layer scavenging technique [1.15], control of O_2 partial pressure is the key technology to achieve a direct contact of HfO_2/Si structure. But the issue is with deceasing of interface layer, same time the mobility is decreased, as shown in figure 1.12 [1.17].

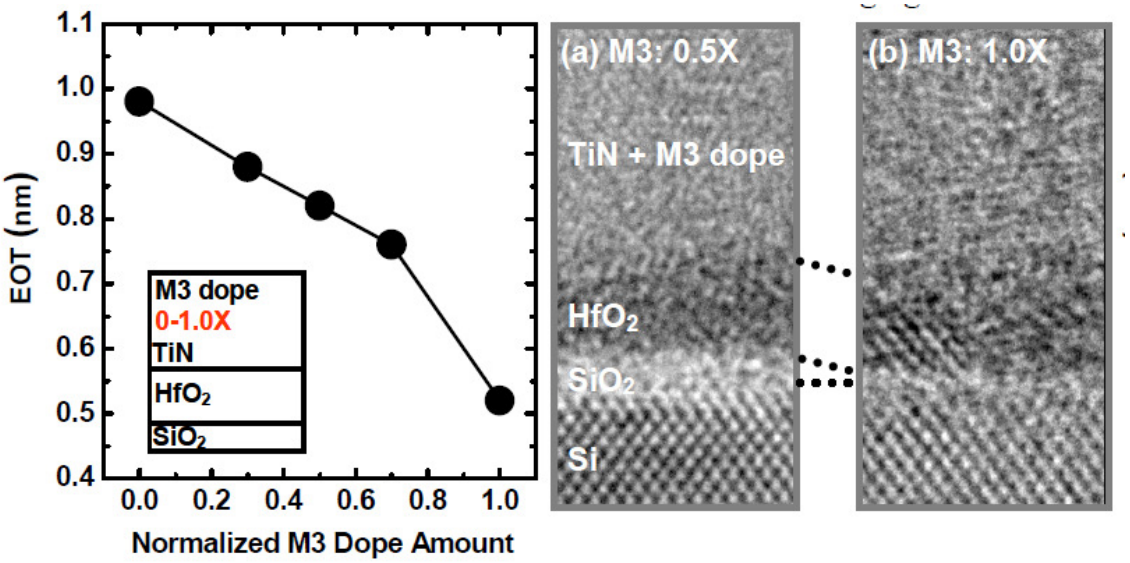

Figure 1.11 Reports on direct high-k/Si [1.15]

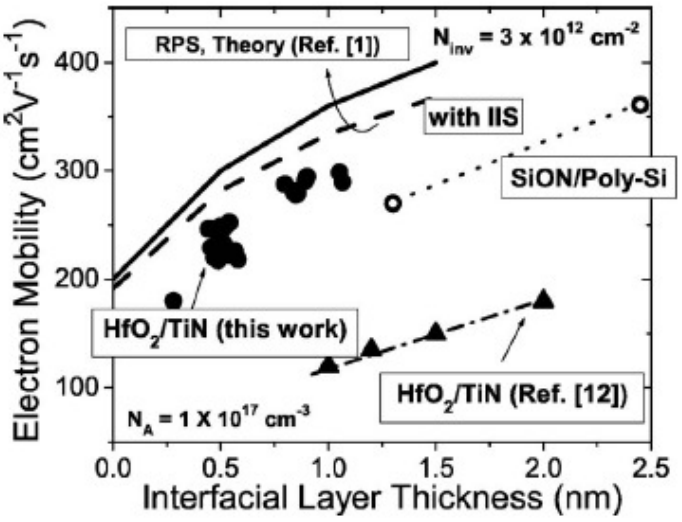

Figure 1.12 Relationship of interfacial layer thickness and mobility [1.17]

Crystallization becomes big issue of Hf-based oxide for gate dielectric application [1.11]. HfO_2 is phase separator materials [1.19]. Grain boundaries in a poly-crystalline oxide act as easy diffusion paths for dopants, same time increase leakage current. Unlike SiO_2, high-k oxides usually have low crystalline temperature and can easily crystallize at thermal treating process [1.22]. It was reported [1.23], as shown in figure 1.14, a relation between mobility and crystallinity. For both HfON and HfSiON lack clear crystallinity in regions of high mobility (>220 cm2/Vs). Conversely, crystallinity is observed in the region of low mobility (<200cm2/Vs), in this case, strained or broken bonds present along crystalline grain boundaries may negatively impact device mobility. Therefore, using an amorphous oxide has many advantages over a poly-crystalline oxide, it is important to select amorphous gate oxide for gate dielectric application.

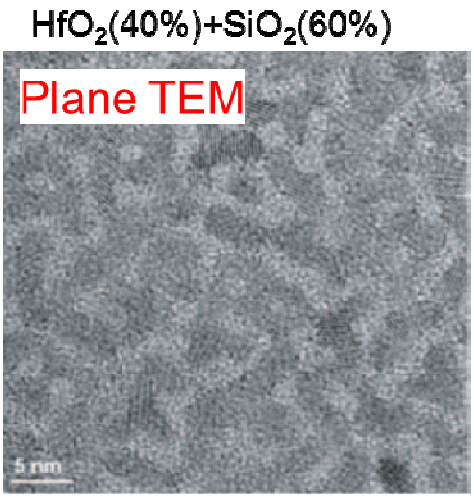

Table II: Classification of Unary Oxides

Silicate Formers	Phase Separators
Y_2O_3	ZrO_2
La_2O_3	HfO_2
Gd_2O_3	ThO_2
Al_2O_3	BeO
Dy_2O_3	NiO
	UO_2

Figure 1.13 Hf-based oxide suffer from crystallization [1.11, 1.19]

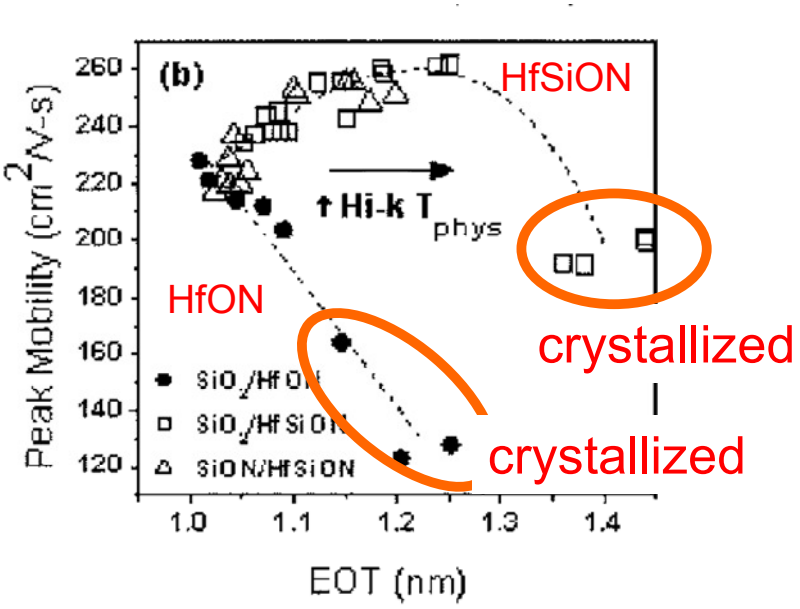

Figure 1.14 Mobility and EOT relationship [1.23]

1.2.2 La-silicate for gate dielectric application

Among high-*k* materials, La-silicate gate dielectrics are regarded as promising candidates for gate dielectric materials for further EOT scaling, owing to high dielectric constant (*k*~20), wide band-gap, amorphous structure and fairly nice interface properties [1.20]. An EOT of 0.62 nm accompanied by superior interfacial properties has been reported with a direct contact La-silicate/Si interface structure and an effective electron mobility of 155 cm2/V s has been demonstrated [1.21]. An advantage for La-silicate gate dielectrics is that the direct contact of high-k/Si structure can be easily achieved by simply depositing La_2O_3 on Si substrate owing to the reactively formation of La-silicate by the reaction between La_2O_3 and Si during annealing process, as shown in figure 1.15 [1.20]. $La_2O_3+nSi+mO_2 \sim La(SiO4)_n$ [1.24], dielectric constant of La-silicate dependent to supply of oxygen atoms, excess supply of oxygen atom increase dielectric constant due to formation of Si-rich La-silicate [1.20]. Thus, control of oxygen partial pressure is

the key for processing.

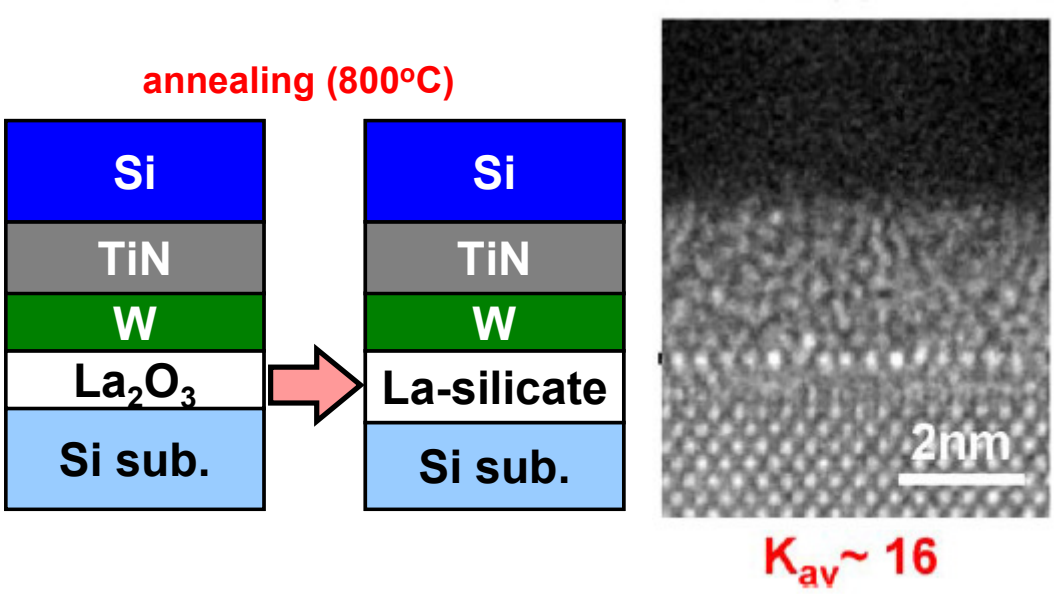

Figure 1.15 La-silicate for gate dielectrics [1.20]

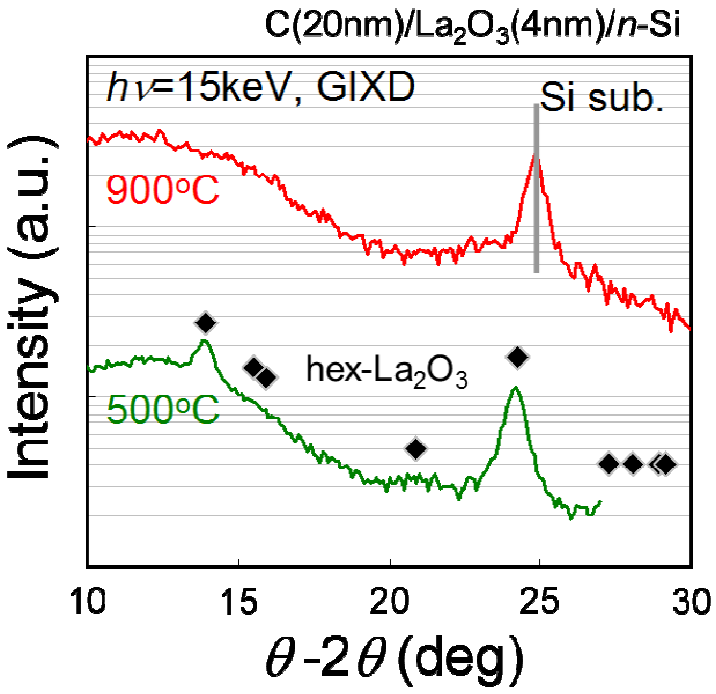

Figure 1.16 Amorphous La-silicate for gate dielectrics

La-silicate is amorphous, as shown in figure 1.16. it is good advantage for gate dielectric application, and meanwhile La-silicate with Si substrate has fairly nice interface properties. It has been reported that the interface state density at the La-silicate/Si interface is reduced by increasing annealing temperature [1.21, 1.25], as shown in figure 1.17, with high temperature annealing interface state density can be as low as 10^{11} cm^{-2}/eV. Thanks to a fairly nice interface property of La-based dielectrics, a peak effective mobility of over $300cm^2/Vs$ has obtained [1.26].

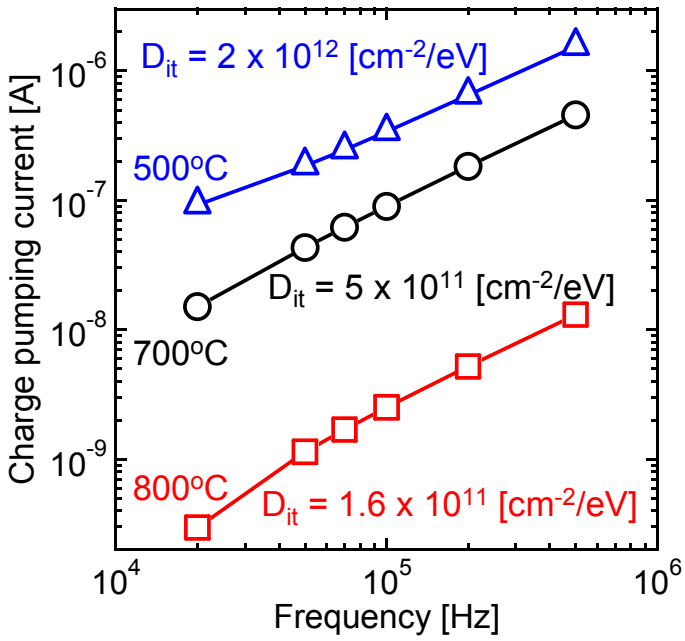

Figure 1.17 Interface state density and annealing temperature relationship [1.20]

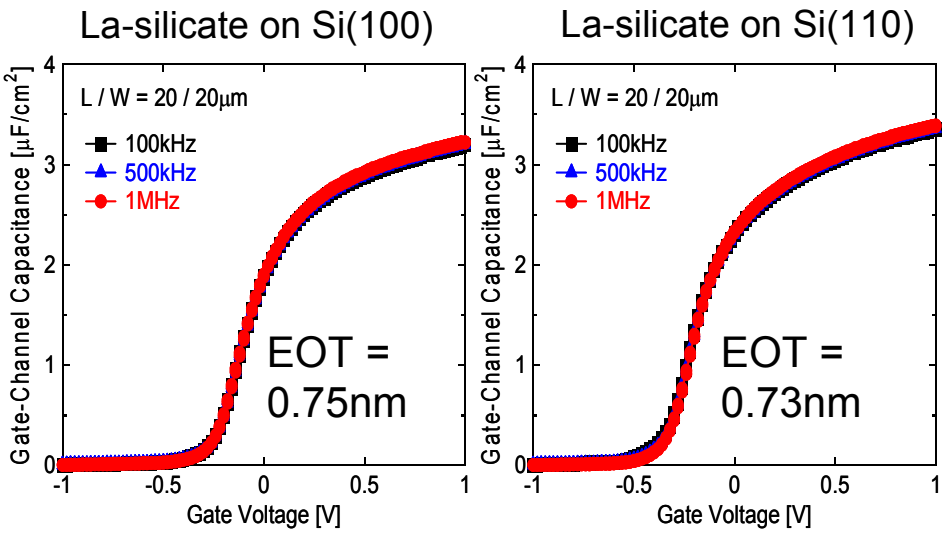

Figure 1.18 comparison of gate channel capacitance for (100) and (110) oriented nMOSFETs with deposited Si layer [1.27]

La-silicate gate dielectrics have advantage for 3D channel device application duo to no orientation dependent EOT change [1.27]. Figure 1.18 shows that duo to reactively-formed La-silicate gate dielectrics, no significant difference relating to the EOT between (100) and (110) orientation. Therefore La-silicate regarded potential candidate for gate dielectric application.

1.4 Scaling issues for La-silicate gate dielectrics

La-silicate gate dielectrics are regarded as promising candidates for gate dielectric materials for further EOT scaling. However, serious problem are still remained to be solved. One of the serious issues in high-k/metal gate stacks is degradation of effective mobility trend with EOT scaling, as shown in Figure 1.19. For both Hf-based and La-based high-k dielectric device, further thinning of the oxide thickness or EOT induced degradation of effective mobility [1.20, 1.28].

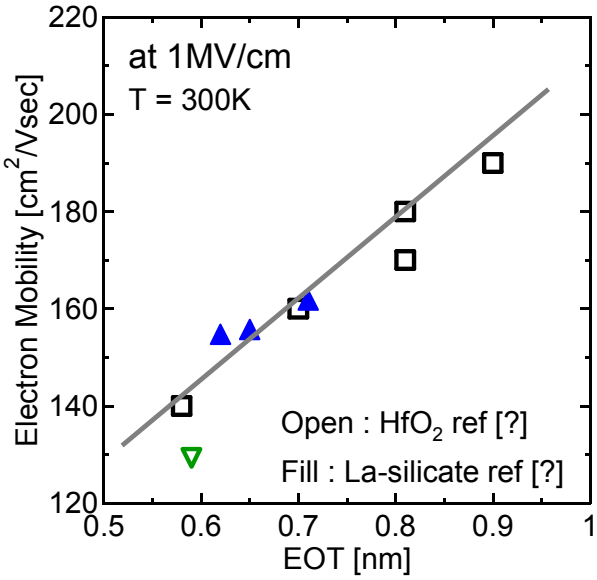

Figure 1.19 A benchmark of high-field electron mobility at 1MV/cm [1.28]

It was reported that several sources have been responsible for mobility reduction, as shown in figure 1.20. 1. Mobility is limited by Columbic scattering by metal induced defects, metal atom diffusion and oxygen vacancy formation, therefore suppression of the formation of metal induced defects in the high-k layer is important. 2. It is limited by roughness scattering by metal/high-k and high-k/Si roughness [1.10]. The interface of metal/high-k and high-k/Si is played important role in CMOS devices, in terms of roughness of metal/high-k and high-k/Si interfaces, and the absence of interface defects, or interface state density [1.20, 1.29].

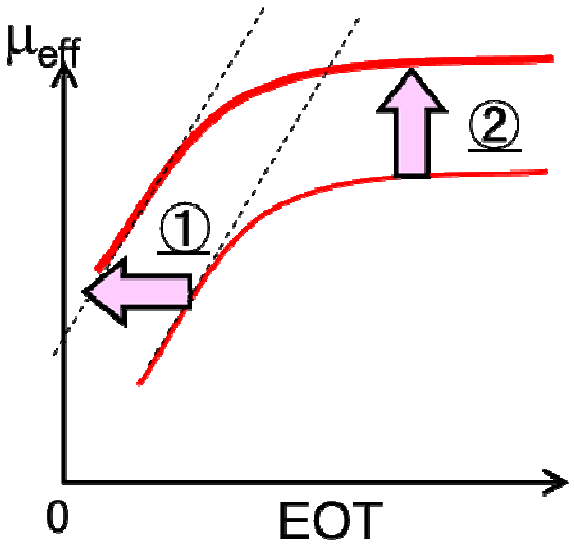

Figure 1.20 mobility reduction trend with EOT scaling

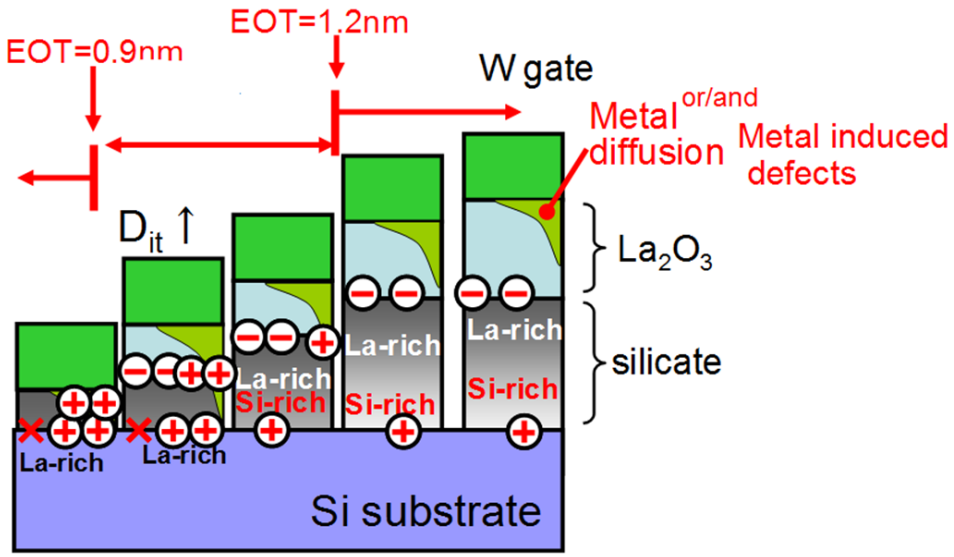

Figure 1.21 Scaling issues for La-silicate duo to interface properties

Figure 1.21 shows scaling issues for La-silicate duo to interface properties, at relatively large EOT, the interface density was determined by La-silicate/Si interface, as mentioned above, the interface roughness of La-silicate/Si is one of the sources for degradation of effective mobility, the interface roughness as modeling in Figure 1.22. At

scaled EOT, EOT< 1 nm, interface mixing at metal/high-k interface influences the interface state density, thus it is necessary to minimize the both interfaces for EOT scaling.

There is onther issue on direct contact of high-k/Si, strain in the Si substrate. As shown in 1.22 stress applied below high-k layer, and not under SiO2 layer. The possible reasons are thermal expansion difference, less viscous flow of high-k dielectric and stress form high-k or/and metal gate.

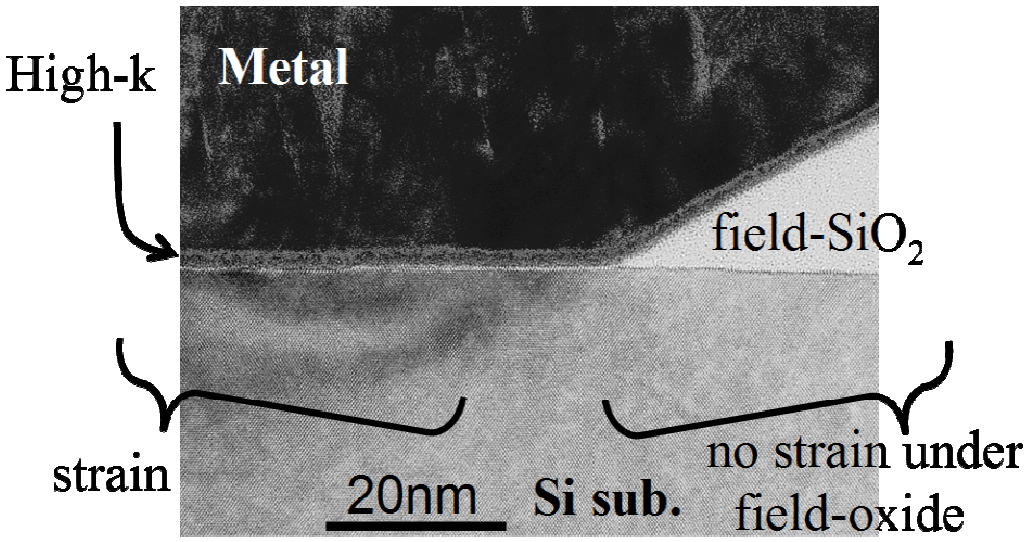

Figure 1.22 issues on direct contact of high-k/Si

Another most serious issue in high-k/metal gate stacks is reliability. Aggressive scaling of gate oxide thickness in CMOS transistors has caused the reliability of ultrathin dielectrics. It is therefore important to investigate the reliability of La-silicate gate dielectrics.

1.5 Introduction of metal gate

1.5.1 General requirements for metal gate materials

Doped poly-Silicon has been used as a gate electrode for CMOS devices for past few decades. However, with continued down-scaling of MOSFET, this system started to exhibit some serious problems, such as the poly-depletion effect at the poly-Si/Silicon oxide interface, the boron penetration, especially for ultra-thin SiO_2, the boron would diffuse from the gate and into the channel region causing unwanted doping, resulting in the degradation of mobility and reliability, the high gate resistance, and poor compatibility with high-k gate dielectrics [1.31-1.34], therefore, the research focus is shifted to metal gate electrodes. It is realized that high-k gate dielectrics must be implemented in conjunction with metal gate electrodes to get sufficient potential for CMOS continuous scaling. In order to improve transistor performance, the gate electrode material must to have some good properties, such as thermal stability against agglomeration, stability against phase separation, small resistivity, proper work function for n-FETs and p-FETs, small grain size less than 5 nm, and less orientation dependent on work function variability [1.36]. Along with EOT scalability, these requirements should be satisfied at the same time, but it is difficult to find metals satisfying all of these requirements.

Commonly nitrides (TiN, TaN, etc) with midgap work function used for gate electrodes. According to reports these nitrides suffer from orientation induced work function variability, shown in table 1.1 [1.38].

Table 1.1 Reported orientation dependent work function [1.38]

Material	Orientation	Probability	Workfunction (eV)	Grain size (nm)
TiN	(100)	60%	4.6	22
	(111)	40%	4.4	
TaN	(100)	50%	4.0	7
	(200)	30%	4.2	
	(220)	20%	4.8	
WN	(111)	65%	4.5	10
	(200)	15%	4.6	
	(220)	15%	5.3	
	(311)	5%	4.2	

The one of serious problem is threshold voltage variability. This is due to the polycrystalline nature of the current metal gates, as Figure 1.23. With decreasing of gate length, the gate length becomes comparable to the gate metal grain size, the grain orientation distribution and hence work function distribution no longer averages out. This causes the threshold voltage to vary from device to device since the threshold voltage is directly related to the gate work function. Thus, metal gates with grain size less than 5 nm or amorphous are preferable [1.37], as in Figure 1.24.

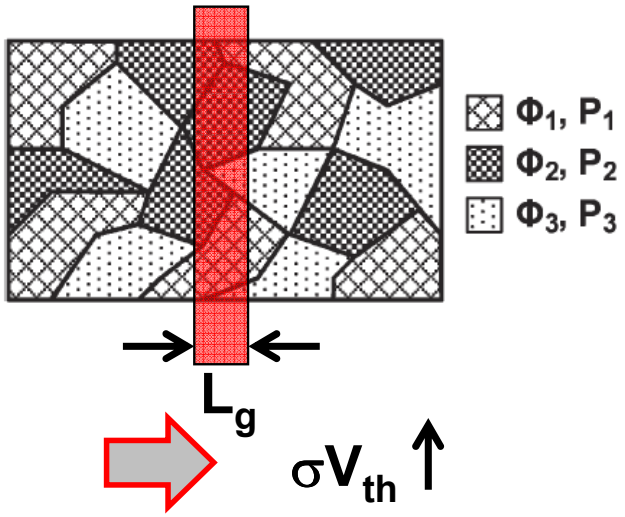

Figure 1.23 Polycrystalline metal

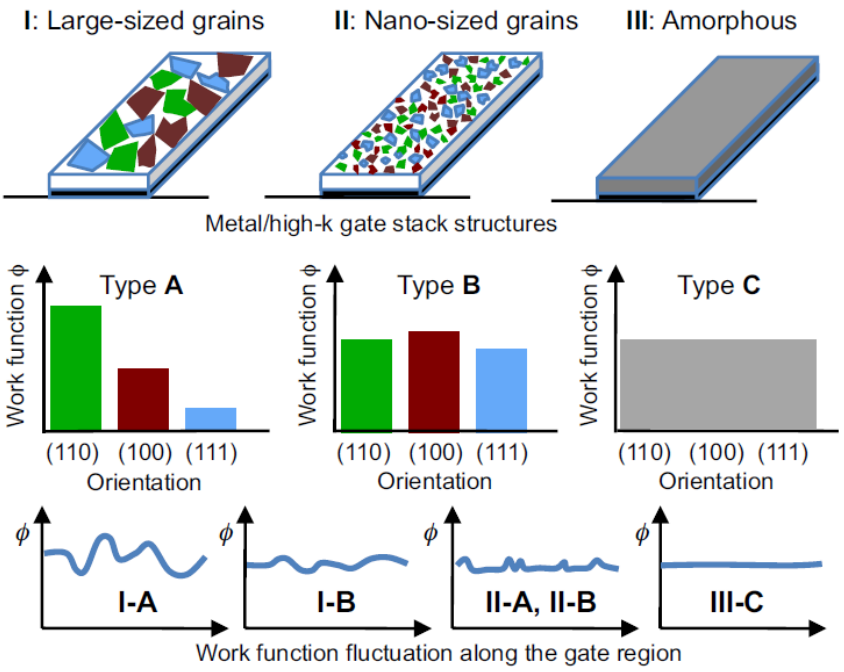

Figure 1.24 Polycrystalline granular structure influence of σ_{Vth} [1.35]

Polycrystalline granular structure of metal electrodes has been found to be dominant in σ_{Vth}, as shown in Figure 1.24, when the gate dimensions become comparable to the grain size of metal electrodes, due to work function variability of

different crystallographic orientation in the metal grains. Recent modeling studies have revealed that the amount of work function variability to σ_{Vth} cannot be reduced when only one grain covers the entire gate surface area. An intuitive approach to solve the work function variability is to use nano-sized grains or amorphous metals, which average out the work functions. Indeed, carbon doped TiN gates with nano-sized grains have shown reduced σ_{Vth} with small transistors [1.36], as shown in figure 1.25. Furthermore, formation of an amorphous metal alloy with $Ta_{40}W_{40}Si_{10}C_{10}$ has been demonstrated with thermal stability up to 1100 ^{o}C, thus expected to solve the problem [1.36]. Although compositional control in the alloy is still necessary, an easy process to form metal layers with nano-sized grains or amorphous is necessary for reducing the σ_{Vth} for extremely scaled devices,

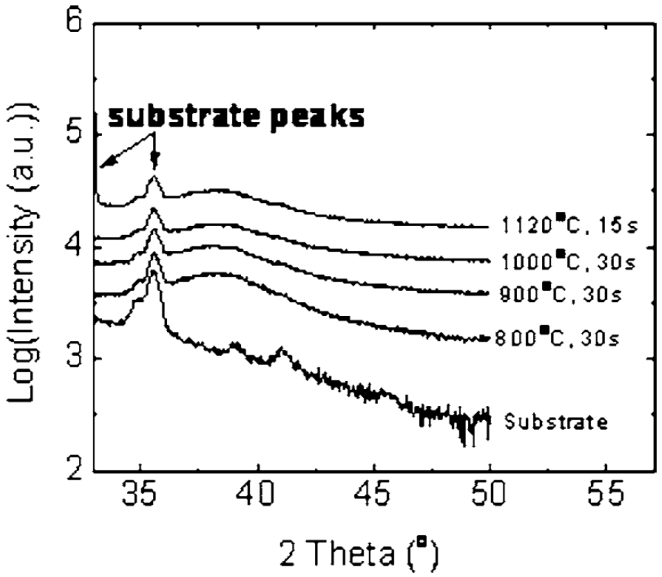

Figure 1.25 amorphous metal [1.36]

Table 1.2 shows structure of metal gates on σ_{Vth} and its effective work function. Nano-grains and amorphous gates present average work function duo to various facets and different bonding angles at metal/high-k interface, giving less controllability to WF,

shown in Figure 1.26. As shown in figure 1.27, highly growth of CVD-TiN effective for suppresss threshold voltage variability [1.39].

Table 1.2 Structure of metal gates on σ_{Vth} and its effective work function.

Metal structure	Inhomogeneous strain induction	Metal/high-k roughness & ΔT_{ox}	WF	σV_{th}	Example
Large-grains (~100nm)	High	Large	Facet dependent	Large	Pure metal
Nano-grains (~10nm)	Low	Small	Average	Large	TiN
Amorphous	N/A (might be high)	Small	Average	Small	TaSiN

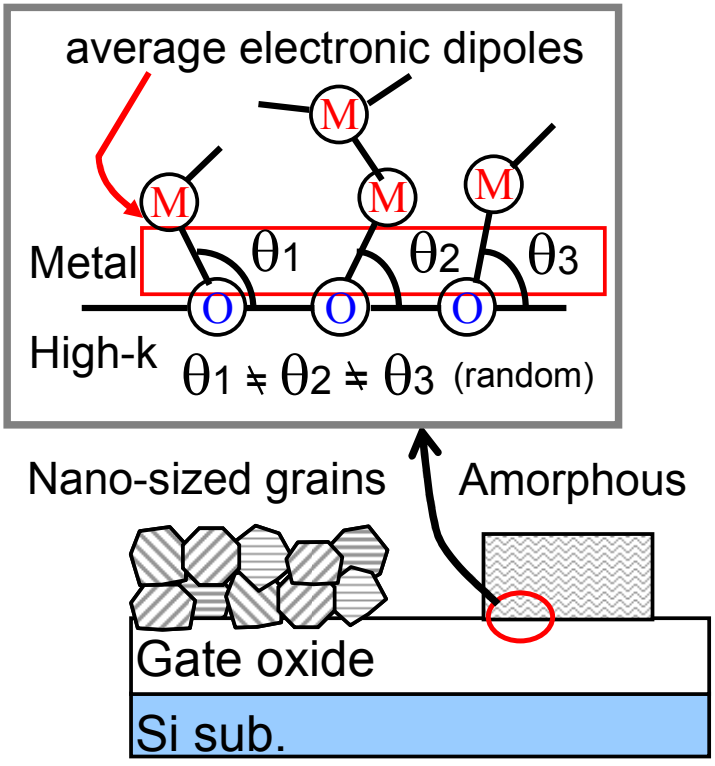

Figure 1.26 Different bonding angles at metal/high-k interface

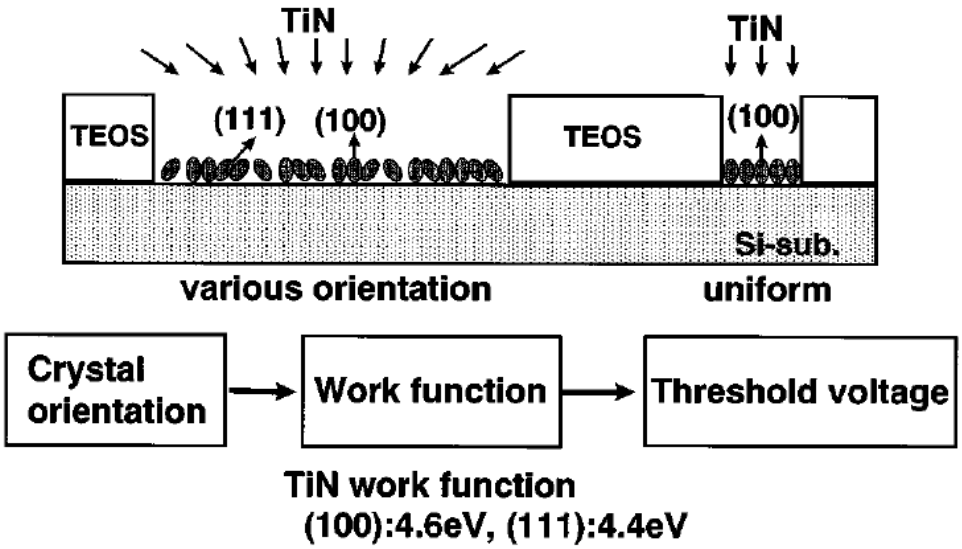

Figure 1.27 Schematic diagram for the work function deviation metal (crystal orientation deviation model) [1.39]

1.5.2 Metal material candidates for La-silicate gate dielectrics

La-silicate formed by reaction of La_2O_3 and Si substrate during annealing process, as shown in figure 1.29. $La_2O_3+nSi+mO_2 \sim La\ (SiO4)_n$ [1.20], dielectric constant of La-silicate dependent to supply of oxygen atoms, thus proper oxygen atom supply is needed. Excess supply of oxygen atom increase dielectric constant due to formation of Si-rich La-silicate [1.20]. Less supply of oxygen atoms let remain residual La_2O_3 layer. So, oxygen atoms should be released after annealing process. Therefore, metal layer should contain proper oxygen atoms for silicate reaction. TiN, TaN do not contain oxygen, they react to form TiOx, TaOx, instead. In all metals, tungsten (W) and molybdenum (Mo) are considerate metal gate candidates for La-silicate due to the nature of oxygen contain materials, but, same time they must to satisfy the general requirements mentioned above, such as small grain size. Grain size should be less than

5 nm due to suppress work function variability. Following nitrides, carbides, and borides of W and Mo will be considerate for metal material candidates for La-silicate gate dielectrics.

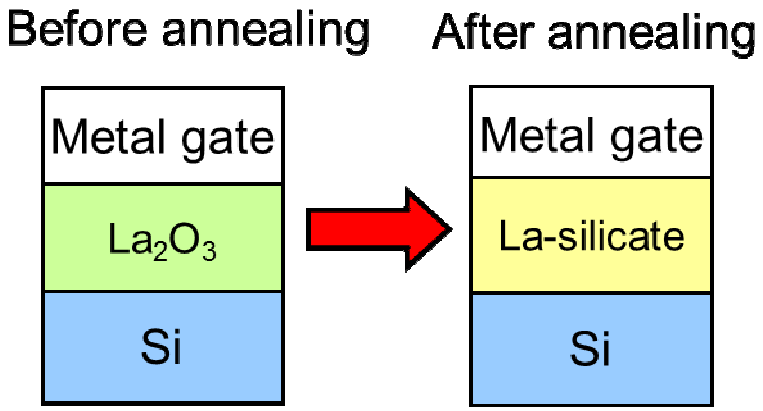

Figure 1.28 La-silicate formation

Table 1.3 tungsten nitrides [1.40]

TABLE I. Φ_m, correlation coefficient (r), 2θ position of the main diffraction peak, and resistivity for W and WN_x films. The Φ_m is extracted from the plot of V_{FB} vs SiO_2 thickness, r is obtained by linear fitting of the V_{FB} vs oxide thickness line, and mean grain size is estimated according to Scherrer's formula.

Film	Φ_m (V)	Correlation coefficient (r)	Main peak and its 2θ position (deg)	Mean grain size (nm)	Resistivity ($\mu\Omega$ cm)
W	4.67	0.96	W(110): 39.92	13.9	35
$WN_{0.4}$	4.39	0.99	W(110): 39.82	8.4	116
$WN_{0.6}$	4.50	0.97	W(110): 39.40	2.6	174
			W_2N (111): 37.50	8.1	
$WN_{0.8}$	5.01	0.92	W_2N (111): 37.09	17.1	326
$WN_{1.5}$	4.49	0.95	W_2N (111): 36.53	6.9	483

According to reports, grain size of 2.6 nm can be obtain by changing of N contents, as shown in table 1.3 [1.40], but the issue is properties of WNx films are sensitive to N atom contents, it is difficult to control N content, because N is introduces as gas like N_2 or NH_3. The issue of borides as gate metal application for La-silicate gate dielectrics is mixture of phase, for example, WB, WB_2, Mo_2B, MoB, Mo_2B_5, MoB_4. Therefore the most potential candidate for gate metal application for La-silicate is carbides, tungsten

carbides (W_2C, WC) and molybdenum carbides (MoC, Mo_2C), as shown in figure 1.29 and 1.30, but question is how we can obtain carbides at low temperature, and same time small grain sized carbide? A novel process is needed to solve this problems,

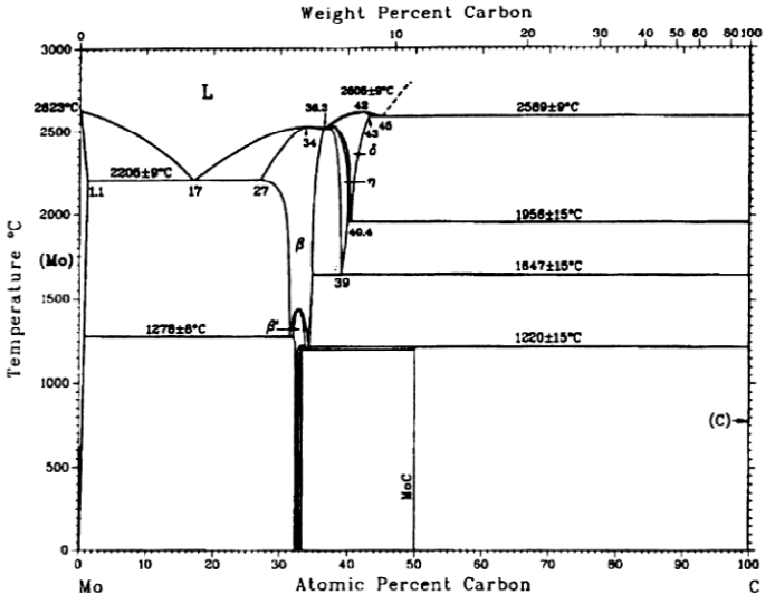

Figure 1.29 molybdenum carbides phase diagram [1.41]

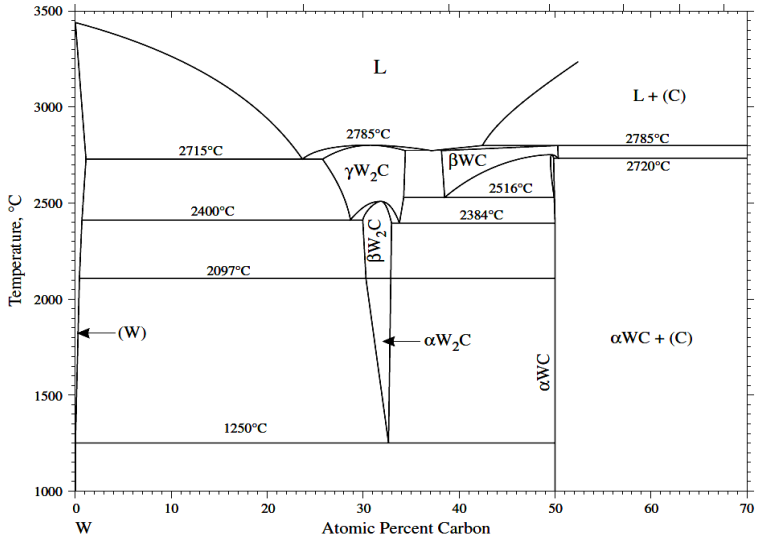

Figure 1.30 tungsten carbides phase diagram [1.42]

1.6 Purpose of this work

The purpose of the thesis is proper metal gate selection for scalable La-silicate gate dielectrics.

1. A process for metal gate formation with nano-sized grains
2. Interface property improvement
3. Reliability improvement

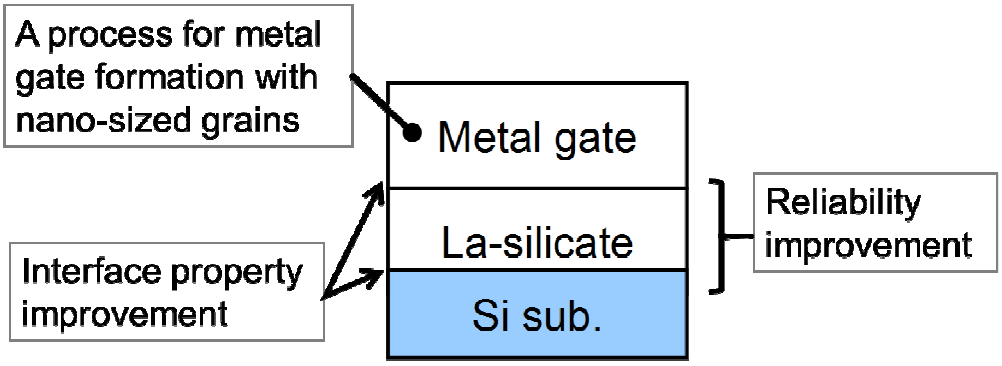

Figure 1.31 Purpose of this study

This thesis is consisted of 6 chapters. Figure1. 32 shows the contents of this thesis.

In chapter 3, a novel process, multi-stacking of carbon and metal thin films with subsequent annealing process to reactively form metal carbides has been investigated. Nano sized TiC, TaC and W_2C has been introduced for gate electrode application.

In chapter 4, electrical characteristics of La-silicate MOS and MOSFET devices with nano-sized tungsten carbide gate electrode has been experimentally investigated. Atomically flat MF/HK and HK/Si interface can be achieved.

In the chapter 5, reliability of La-silicate gate dielectrics have been investigated with different metal electrodes, by TDDB and PBTI.

Finally, chapter 6 summarizes of this study and future work.

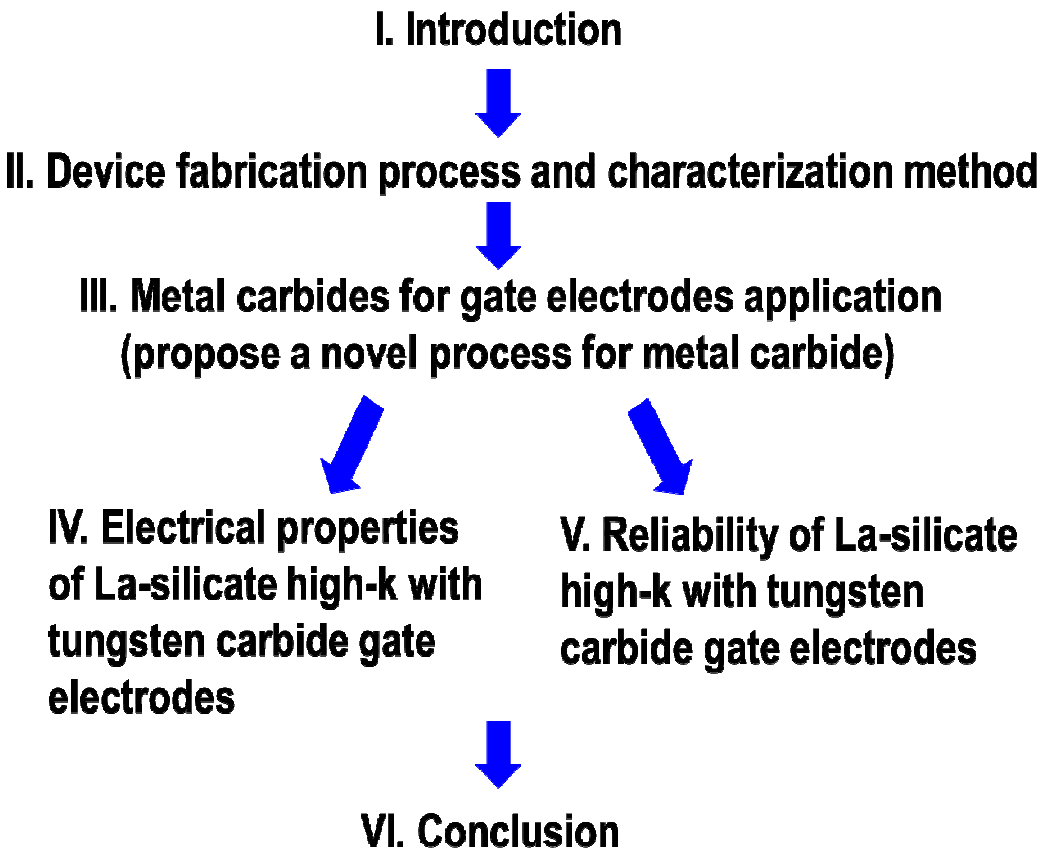

Figure 1.32 thesis structure

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Chapter 2 Fabrication and Characterization

2.1 Fabrication Procedure

2.1.1 MOS Capacitor and MOS Transistor Process Flow

2.1.2 Substrate cleaning: SPM Cleaning and HF Treatment

2.1.3 Electron-Beam Evaporation for La_2O_3 deposition

2.1.4 RF Magnetron Sputtering

2.1.5 Photolithography

2.1.6 Dry Etching by reactive ion etching (RIE)

2.1.7 Vacuum Evaporation for Al Deposition

2.2 Characterization method

2.2.1 Interface state density by conductance method

2.2.2 Mobility measurement method based on split *C-V*

2.3 References

2.1 Fabrication Procedure

The purpose of this chapter is to introduce the fabrication procedure and characterization for both of MOS capacitor and MOS transistor. The process fabrication involves the steps of surface cleaning of substrate, gate dielectrics and gate electrode deposition, patterning, thermal treatment and contacting of electrodes.

2.1.1 MOS Capacitor and MOS Transistor Process Flow

In this study, MOS capacitors were fabricated on *n*-Si (100) substrates with doping of 3×10^{15} cm^{-3} (3×10^{16} cm^{-3} for MOSFET). nMOSFETs were fabricated by a gate-last process using source and drain preformed p-Si (100) substrates with a substrate impurity concentration of 3×10^{16} cm^{-3}. Figure 2.1 and 2.2 shows the device fabrication process flows for MOS capacitor and MOSFETs, respectively. After performing SPM and HF chemical cleanings with H_2SO_4/H_2O_2 mixture at 130^oC for 5 minutes, thin La_2O_3 gate dielectric films were deposited by e-beam evaporation at a substrate temperature of 300 ^oC. Metal gate were deposited by radio frequency (RF) magnetron sputtering without breaking the ultra-high vacuum. Then, TiN (10nm) and Si (100nm) capping layers were deposited on W/C metal also by RF sputtering to control the silicate reaction [2.1, 2.2]. The gate electrode was patterned by lithography and formed by reactive-ion etching (RIE). The samples were then annealed at 800^oC in forming gas (N_2:H_2=97:3) ambient. Backside contacts were formed by Al evaporation. Finally, the sample was annealed in forming gas (N_2:H_2=97:3) ambient at 420 ^oC for 30 minutes.

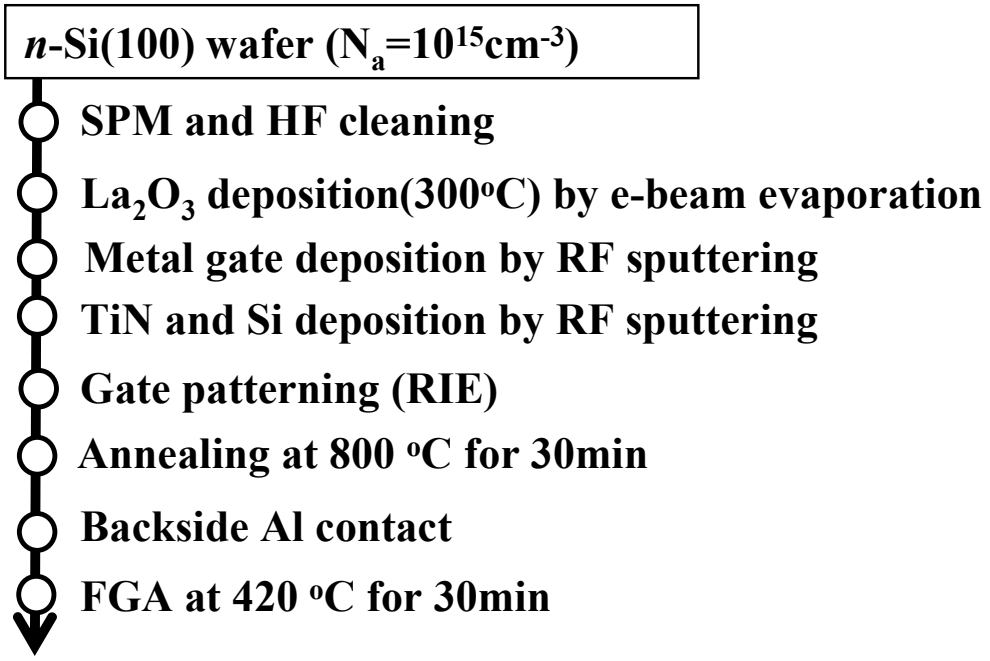


Fig. 2.1 Fabrication procedure for MOS devices

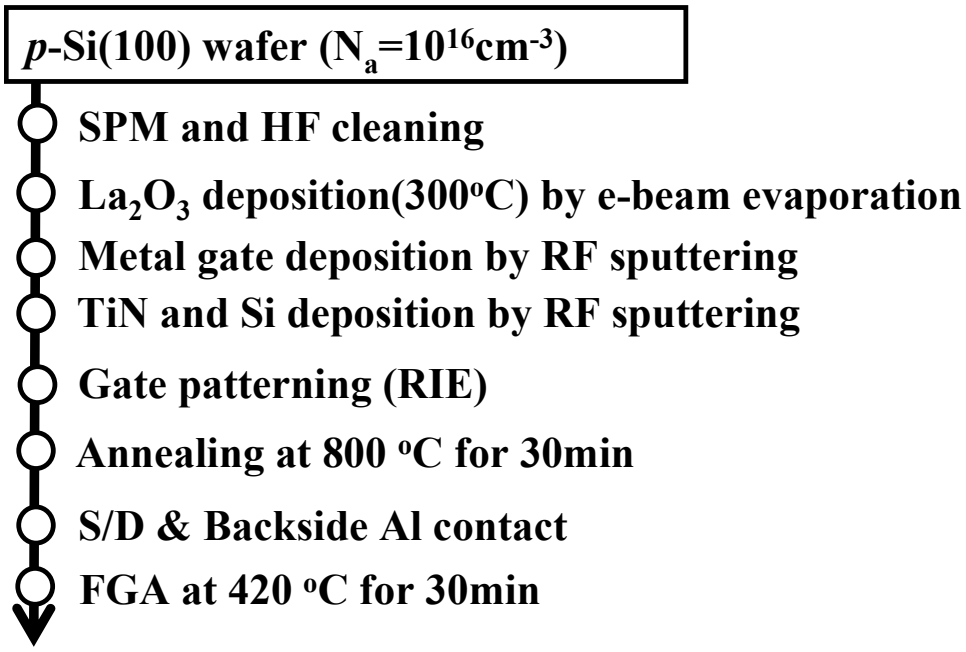


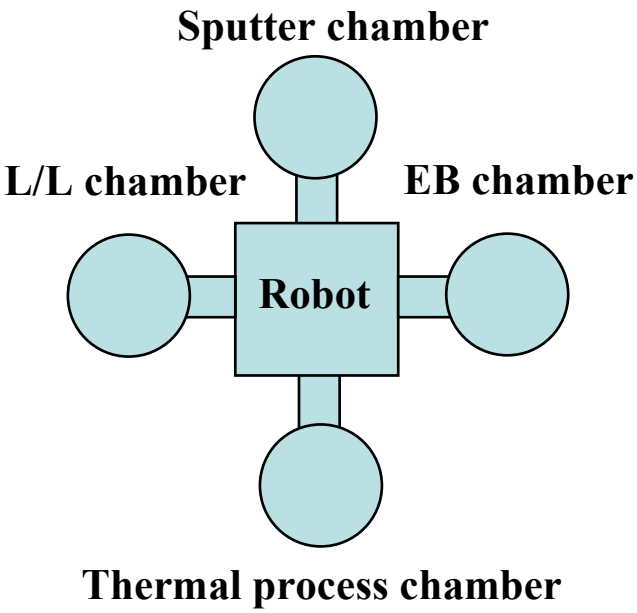
Fig. 2.2 Fabrication procedure for MOS devices

2.1.2 Substrate cleaning: SPM cleaning and HF treatment

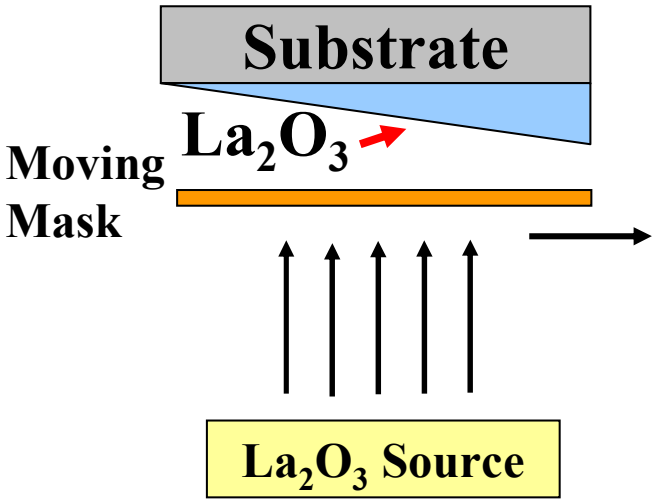
Careful process techniques are important to high performance of MOSFET. Thus, the first step of fabrication process is cleaning of substrate. There are many method of cleaning substrates. In this study, we used wet cleaning by chemical liquid. Before start to deposit gate dielectrics and gate electrodes, the wafers were cleaned by a mixture of H_2SO_4 and H_2O_2 (H_2SO_4/ H_2O_2=4/1) called SPM cleaning to remove the particles and organic substance at the surface of Si substrate. Then, the surface of Si substrate was treated by 1% HF to remove the native or chemical oxide.

2.1.3 Electron-beam evaporation of La_2O_3 deposition

After performed the SPM and HF treatment, the substrates were transferred into an ultra-high vacuum cluster tool system, as shown figure 2.3. A process system equipped with an electron beam deposition chamber, a sputter chamber and a thermal processing chamber. Electron-beam evaporation is one of the physical vapor depositions (PVD). The high-k materials were evaporated by E-beam in ultra high vacuum, in this study, the vacuum was about 10^{-6} Pa. The Si-substrate was heated at 300oC during La_2O_3 deposition. The physical thickness of the deposited La_2O_3 thin films was controlled by mask, as shown in figure 2.4, the graded thickness of La_2O_3 was from 1 nm to 4 nm.



2.2 Schematics of the developed cluster tool system.



2.3 Schematic illustration of the concept of high-k deposition with graded thickness using a linear moving mask

2.1.4 RF magnetron sputtering

After La_2O_3 layer deposition, the samples were transported to sputter chamber without breaking the ultra-high vacuum. Gate metals were deposited by radio frequency (RF) magnetron sputtering on the La_2O_3 layer. W/C, Ti/C, Ta/C multi stack are deposited by RF with Ar gas ambient, gas follow is 10sccm, RF power is 60w for W, Ti and Ta, 200w for C. TiN layer is deposited from Ti source with Ar and N_2 gas ambient, the ratio of Ar and N_2 is 9:1. The thickness of the sputtered metal layer was controlled by deposition time.

2.1.5 Photolithography

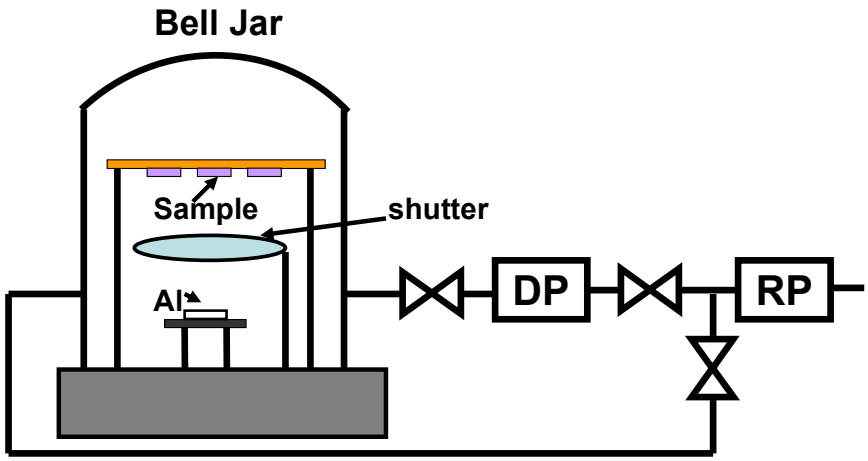
Photoresist layer of S1805 was coated on the sample by spin coater system. Then samples were baked at 115 ^oC for 5 minutes. The spin-coated photoresist layer was aligned and exposed by ultraviolet (UV) light. After that, exposed wafers were developed using the specified developer called NMD-3. Post-baking at 130 °C for 3 minutes is necessity to harden the developed photoresist pattern before metal gate etching.

2.1.6 Dry etching by reactive ion etching (RIE)

Reactive ion etching (RIE) is one of the pattering methods by plasma. The metal gate Si/TiN/W, Si/TiN/C/W…. C/W, Si/TiN/C/Ti…. C/Ti and Si/TiN/C/Ta…. C/Ta was patterned by RIE with SF_6 gas chemistry to form gate electrode. SF_6 gas flow rate and RF power is 30 sccm and 30 W, respectively. La_2O_3 layer was patterned by Ar gas. After the gate metal etching, photoresist layer on top of metal gate was removed by O_2-based ashing method inside the same RIE system.

2.1.7 Vacuum evaporation for Al deposition

Aluminum (Al) evaporation in this study was deposited by using bell-jar type thermal evaporation for wiring and backside contact, as shown in figure 2.2. in the figure, DP is diffusion pump, RP is rotary pump. Al for deposition is put on tungsten boat and heated up tp boiling point of Al by joule heating. Backside Al thickness for all samples is 50nm.



2.4 Schematics of the Al evaporator

2.2 Characterization method

Electrical characterization of MOS capacitors was mainly performed by using capacitance-voltage (C-V) characteristics, gate leakage current density-voltage (Jg-V) characteristics and interface-trap density (D_{it}) calculated by conductance method. Split C-V method for effective mobility evaluation was used to examine the MOSFET characteristics.

2.2.1 Interface state density by conductance method

In this study, interface state density (D_{it}) was determined by conductance method. The conductance method was proposed by Nicoliian and Goetzberger in 1967 [2.3].

Conductance method is an approach which we replace the measurement circuit of MOS capacitor with equivalent circuit models and calculate D_{it}. Figure 2.5 (a) shows an equivalent circuit model of MOS capacitor, where C_{ox} is the oxide capacitance per unit area, C_s is the silicon capacitance per unit area, R_{it} and C_{it} are the resistance and capacitance components per unit area related to interface trap, and G_t is tunnel conductance per unit area related to leakage current. On the other hand, the measurement circuit is shown in figure 2.5 (b), where C_m and G_m are the measured capacitance and conductance per unit area. The circuit figure 2.5 (a) can be simplified by the circuit of figure (c). The equivalent parallel circuit is shown in figure 2.5 (c), where C_p and G_p are the equivalent parallel capacitance and conductance per unit area.

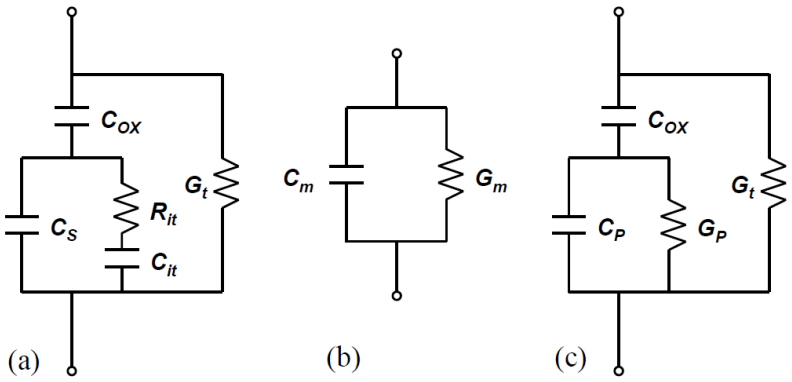


Figure 2.5 Equivalent circuit of MOS capacitor, (a) an equivalent circuit model of MOS capacitor; (b) the measurement circuit; (c) the simplified circuit of (a)

C_P and G_P are given by

$$C_p = C_s + \frac{qD_{it}}{1+(\omega\tau_{it})^2} \qquad (2.1)$$

$$\frac{G_p}{\omega} = \frac{q\omega\tau_{it}D_{it}}{1+(\omega\tau_{it})^2} \qquad (2.2)$$

Where, $C_{it} = qD_{it}$, and $\tau_{it} = C_{it}R_{it}$. D_{it} is interface state density and τ_{it} is interface trap time constant. These two equations are for interface traps with a single energy level in the band gap. On the other hand, the capacitance and conductance are measured from the circuit in figure 2.5 (b). By using equivalent circuit in figure 2.5 (c) GP/ω can be calculated as:

$$\frac{Gp}{\omega} = \frac{\omega(G_m - G_t)C_{ox}^{\ 2}}{(G_m - G_t)^2 + \omega^2(C_{ox} - C_m)^2} \qquad (2.3)$$

2.2.2 Mobility measurement method based on split *C-V*

MOSFET drain current is due to drift and diffusion of the mobile carriers in the inverted Si channel. The drain current I_d can be written as,

$$I_d = \frac{W\mu_{eff}Q_{inv}V_{ds}}{L} - W\mu_{eff}\frac{kT}{q}\frac{dQ_{inv}}{dx} \qquad (2.4)$$

Where, L is gate length, W is gate width, Q_{inv} is the carrier channel charge density and μ_{eff} is the effective mobility. At low V_{ds}, one can assume that channel charge to be fairly distribute and uniform from the source to drain, allowing the diffusive second term in eq. (2.4) to be dropped. Solving eq. (2.4) then gives,

$$\mu_{eff} = \frac{g_d L}{WQ_{inv}} \qquad (2.5)$$

where the drain conductance g_d is defined as,

$$g_d = \frac{\partial I_d}{\partial V_{ds}} \qquad (2.6)$$

to accurately determine the Q_{inv}, direct measurement of Q_{inv} from 100 kHz high frequency capacitance measurement, with mobile channel density or inverted charge density determined from the gate-to-channel capacitance/unit area (Cgc) according to the following equation.

$$Qinv = \int_{V_{fb}}^{V_g} C_{gc} dV_g \qquad (2.7)$$

Where, V_{fb} and V_g are the flatband voltage and gate voltage, respectively. The C_{gc} is measured by using the connection of figure 2.6 (a). The capacitance meter is connected between the gate and the source-drain connected together with substrate grounded. Setup in figure 2.6 (b) is used to measure the gate to substrate capacitance/unit area (C_{gb}). The connected source-drain is grounded during C_{gb} measurement. C_{gb} is used to calculated bulk charge density (Q_b) according to the following equation,

$$Qb = \int_{V_{fb}}^{V_g} C_{gb} dV_g \qquad (2.8)$$

both Q_{inv} and Q_b are then used to calculate the effective vertical electric field (E_{eff}) according to

$$E_{eff} = \frac{Q_b + \eta Q_{inv}}{\varepsilon_{Si}} \qquad (2.9)$$

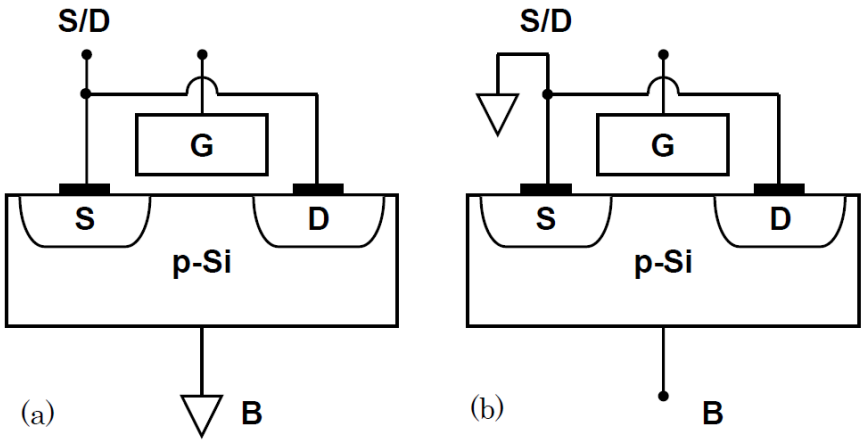


Figure 2.6 Schematic configurations for (a) gate to channel, and (b) gate to body capacitances measurements for nMOSFETs [2.4]

Where, η is the inversion layer charge accounts for averaging of the electric field over the electron distribution in the inversion layer. The parameter η=1/2 for the electron mobility and η=1/3 for the hole mobility. ε_{Si} is silicon permittivity. In this study, C_{gc} is

measured at 100 kHz. The μ_{eff} and g_d are extracted from the area of C_{gc}-V_g characteristic and the slope of the I_{ds}-V_{ds} characteristic, respectively.

2.3 References

[2.1] C. Choi, T. Ando, E. Cartier, M. M. Frank, R. Iijima, and V. Narayanan, "Quasi-damascene metal gate/high-k CMOS using oxygenation through gate electrodes", Microelectron. Eng., Vol. 86, pp. 1737–1739, 2009.

[2.2] T. Kawanato, Y. Lee, K. Kakushima, P. Parhat, K. Tsutsui, A. Nishiyama, N. Sugii, K. Natori, T. Hattori, and H. Iwai, "EOT of 0.62nm and high electron mobility in La-silicate/Si structure based nMOSFETs achieven by utilizing metal-inserted poly-Si stacks and annealing at high temperature", IEEE TED, Vol. 59, pp: 269-276, 2012.

[2.3] E.H. Nicollian, and A. Goetzberger, "The Si-SiO_2 interface-electrical properties as determined by the metal-insulator-silicon conductance technique", Bell Syst. Tech. J., Vol.46, pp:1055-1133, 1967.

[2.4] D. K. Schroder, "Semiconductor material and device characterization", John Willey & Sons, New York, pp: 489-500, 2006.

Chapter 3 Metal Carbides for Metal Gate Electrode Applications

3.1 Introduction

3.2 Process for carbide formation

3.3 Titanium Carbide Formation and characteristics

3.4 Tantalum Carbide Formation and characteristics

3.5 Tungsten Carbide Formation and characteristics

3.6 Conclusions

3.7 References

3.1 Introduction

Metal thin layers have become the primary gate electrode materials together with high-k gate dielectrics for scaled devices to eliminate the problems associated with poly-Si electrodes; poly-depletion effects, high gate resistance, boron penetrations and poor compatibility with high-k dielectrics [3.1-3.4]. Therefore, select of proper metal gate materials is important to improve device performance. As mentioned in chapter 1, according to resent reports, in terms of σVth, metal gates with grain size less than 5 nm or amorphous are preferable [3.5, 3.6]. Ohmori *et al.* have also shown that threshold voltage variability is reduced with respect to polycrystalline TiN gates when 5 at. % carbon is added to the gate during deposition in order to stabilize a nano crystalline phase where the average grain size is 5 nm.

Recently, metal carbides have been studied as a candidate for gate electrode duo to improved thermal stability originated from the properties of metal carbides [3.7]. However, the deposition methods of metal carbide caused some problems, such as carbon deficiency formation, interface reaction and growth of grains during annealing process [3.8]. Therefore, it is necessary to find a novel process to solve this problem. Another concerning issue is metal carbide formation temperature, metal carbide are known as high temperature, high pressure materials, there is a question about how we can obtain a metal carbide at low temperature (~800^{o}C).

In this chapter, we have developed thin carbide electrodes (TiC, TaC and W_2C,) with nano-sized grain of several nm, using multi-stacked sputtering process, for metal gate applications. Moreover, the work functions of formed carbides are extracted through electrical measurements.

3.2 Process for carbide formation

A set of carbon and metal layers which corresponds to atomic ratio, was cyclically stacked for 18 times, as shown in Figure 3.1, resulting in a total thickness of 20 nm, metal carbide was formed after annealing process. Advantage of this kind process, first, excess growth of grain size was suppressed by layered reaction. Second, carbon content can be controlled. Third, metal carbide can be formed at low temperature. Here, the density and number of carbon atoms in sputter deposited carbon film was evaluated to be 2.05 g/cm^3 and 7.8×10^{17} /cm^3, respectively, by x-ray reflectivity, as shown in Figure 3.2.

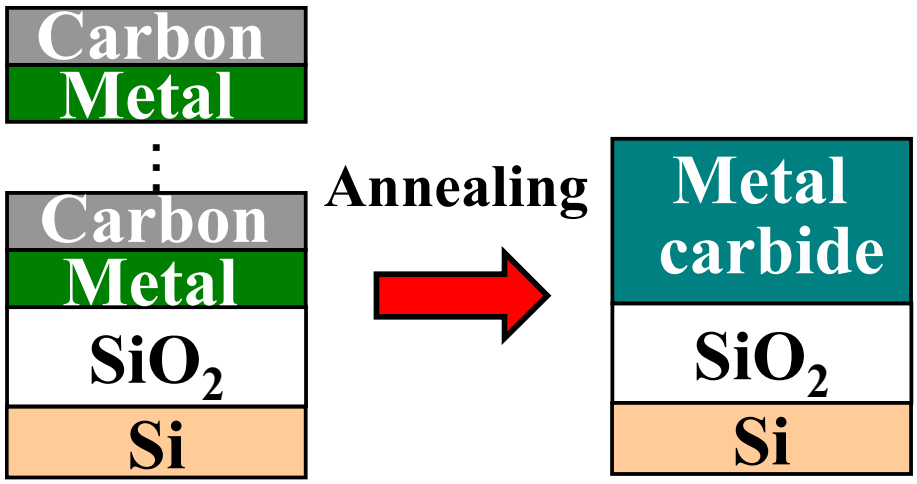


Figure 3.1 Formation of metal carbide

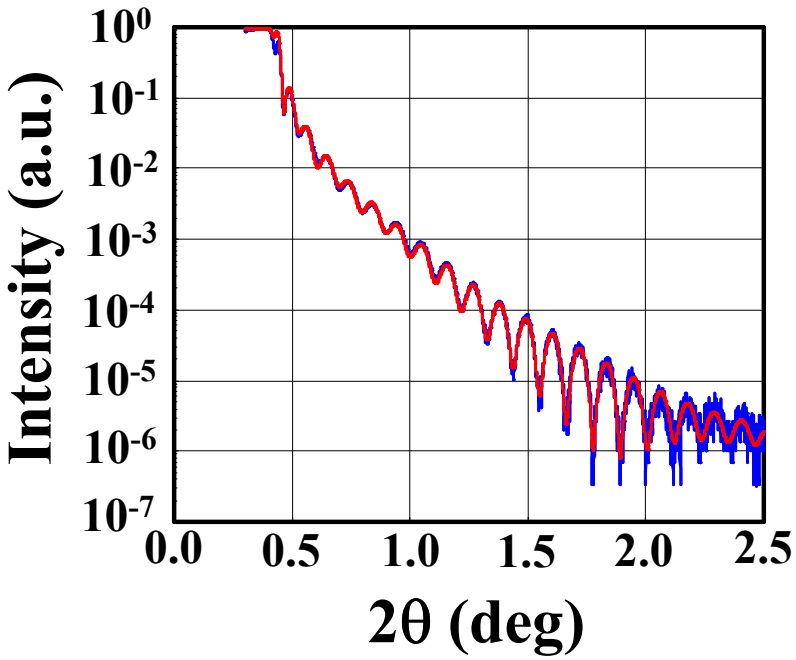


Figure 3.2 x-ray reflectivity

3.3 Titanium Carbide Formation

A set of carbon (0.45 nm) and Titanium (0.80 nm) layers which corresponds to an atomic ratio of 1:1, was cyclically stacked for 18 times on thermally oxidized Si wafers by magnetron sputtering using Ar gas, as shown in Figure 3.3. The total thickness is 20nm. The films were subjected to annealing at various temperatures in N_2 ambient to induce reaction between carbon and metal layers. Figure 3.4 shows sheet resistance (ρ_{sh}) change of the films on annealing temperature. Ti/C stacked films showed a slight increase in ρ_{sh} at 400 ºC, and then showed gradual increase over 600 ºC annealing. In-plane x-ray diffraction (XRD) of the film annealed at 500 ºC, shown in Figure 3.5, revealed weak peaks related to cubic TiC, indicating the presence of nano-sized TiC grains in the layer. When annealed over 600 ºC, the color of the films start to change

due to surface oxidation by residual oxygen gas in the annealing ambient. Capping metals against oxidation such as TiN layer might be useful to improve the thermal resistivity for gate metal application. The ρ_{sh} of 318 Ω/sq., which corresponds to a resistivity of 636 μΩcm appears to be high compared to reported bulk TiC of 80 μΩcm [3.9]. Generally, with a thickness as thin as 20 nm, the effect of grain size to the mean free path of electrons plays a dominant role for the resistivity, so that the observed resistivity increase is reasonable. Here, the average grain size of the TiC film can be extracted as 3.9 nm using Scherrer's equation, which is still longer than calculated electron mean free path of 1.2 nm for TiC [3.10]. Therefore, the increase in the resistivity can be attributed to residual amorphous Ti-C bondings in the layer [3.11, 3.12]. Indeed, the weak signal-to-background ratio in the diffraction patterns is a characteristic of an amorphous-rich film.

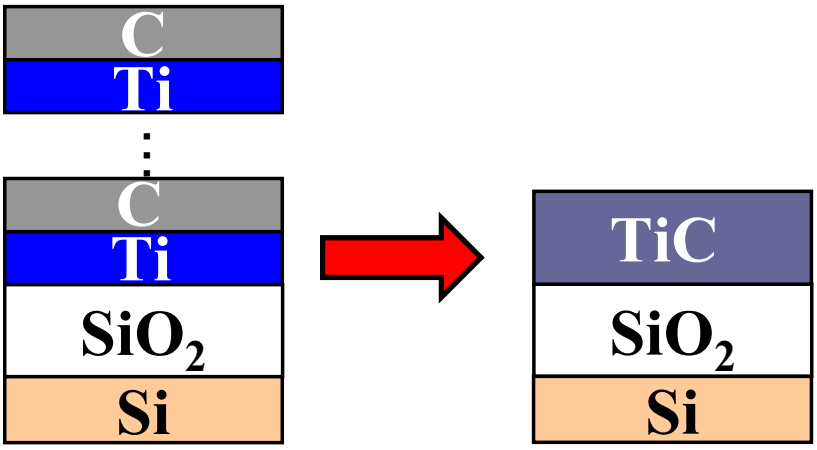


Figure 3.3 Formation of TiC

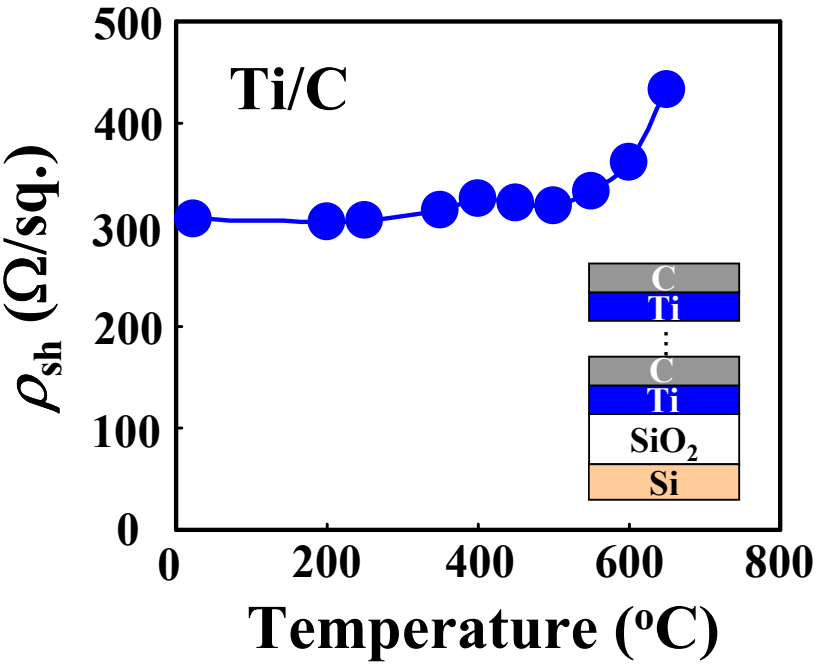


Figure 3.4 Sheet resistance of multi-stacked Ti/C layers

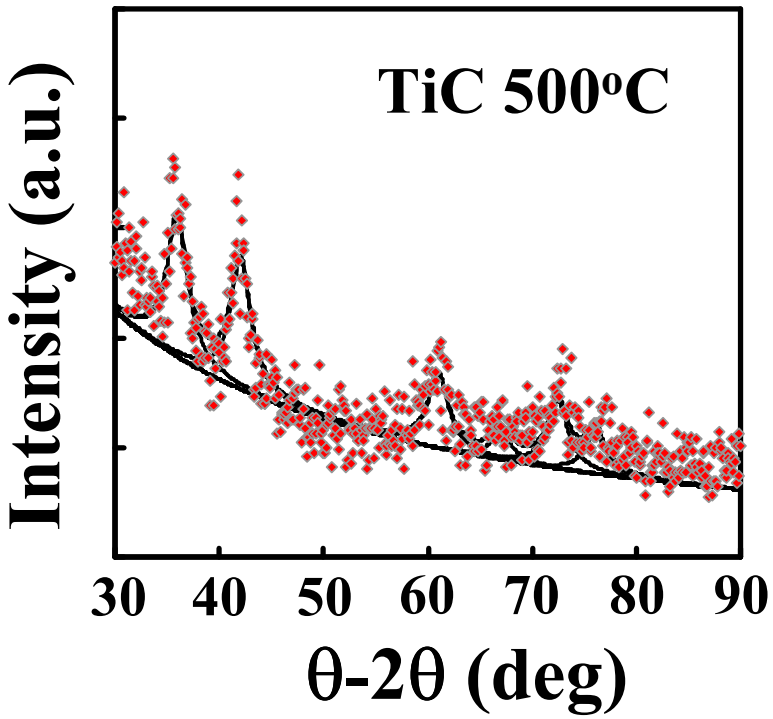


Figure 3.5 XRD measurement of multi-stacked Ti/C layers

Work functions of TiC electrodes formed by stacked sputtering process were extracted through fabrication of metal-oxide-semiconductor (MOS) capacitors using (100)-oriented *n*-Si substrates (N_d=3×10^{15} cm^{-3}) and measurements of flatband voltage (V_{fb}) on different SiO_2 thickness. To exclude the effect of interface states, annealing in forming gas (H_2:N_2=3%:97%) at 420 ºC for 30 min was performed for all the samples. The work function was extracted form thermally-grown TiC/SiO2 MOS capacitor. Figure 3.6 shows the measured V_{fb} on SiO_2 thickness. From the intercept to vertical axis, work function values of 4.3 eV were extracted for TiC. Generally, low work functions around 3.9 are reported for bulk TiC [3.13, 3.14, 3.15], through electron emission study, however, nanometer-thick TiC layer tends to exhibit higher work functions as 4.6 eV, which is comparable to our extracted value. The reason might be due to oriented growth of carbide layers, where preferred surface orientation with high work function could be in contact to the SiO_2 layer as the same phenomenon is observed for chemical-vapored deposited TiN electrodes [3.13]. To confirm the oriented growth, normalized intensities of each diffraction plane of carbides are summarized in table 3.1. By comparing those ratios with powder diffraction database [3.16], where a random orientation is assumed, preferred orientation of (220) and (311) planes can be confirmed for both TiC layers.

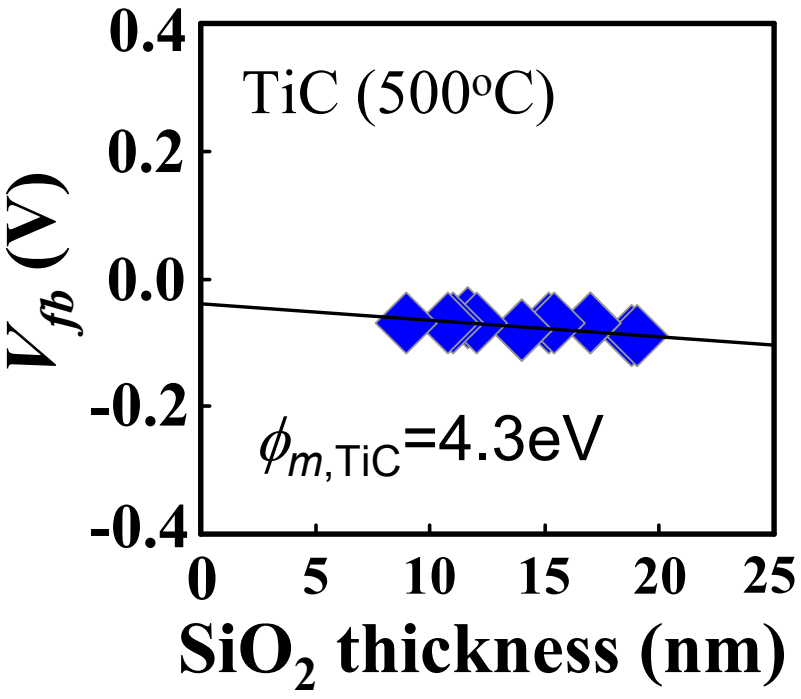


Figure 3.6 Work function of TiC

TABLE 3.1. Normalized intensities of in-plane XRD measurements and powder diffraction patterns of TiC ([a]JC-PDS 00-032-1383)

(hkl) of cubic TiC	(111)	(200)	(220)	(311)
Ti/C stacked film annealed at 500 °C	79	100	71	39
Powder diffraction pattern of cubic TiC[a]	94	100	46	22

3.4 Tantalium Carbide Formation

A set of carbon (0.45 nm) and Tantalium (0.82 nm) layers which corresponds to an atomic ratio of 1:1, was cyclically stacked for 18 times on thermally oxidized Si wafers by magnetron sputtering using Ar gas, resulting in a total thickness of 20 nm, as shown in Figure 3.7. The films were subjected to annealing at various temperatures in N_2 ambient to induce reaction between carbon and tantalium. Figure 3.8 shows sheet resistance (ρ_{sh}) change of the films on annealing temperature. Ta/C stacked film showed constant ρ_{sh} up to 800 ^{o}C. Again above 800^{o}C, the ρ_{sh} start to increase with color change in the film surfaces due to surface oxidation. In-plane XRD patterns of the films annealed at 500 and 750 ^{o}C. shown in Figure 3.9, revealed the formation of cubic TaC. A grain size of 3.2 nm, smaller than TiC case, was extracted for both cases. The ρ_{sh} of 150 Ω/sq., which corresponds to resistivity of 300 μΩcm, is again higher than 170 μΩcm of bulk TaC [3.8]. As the mean free path of TaC is 0.6 nm, so that amorphous structure in the film might be the reason for increased resistivity.

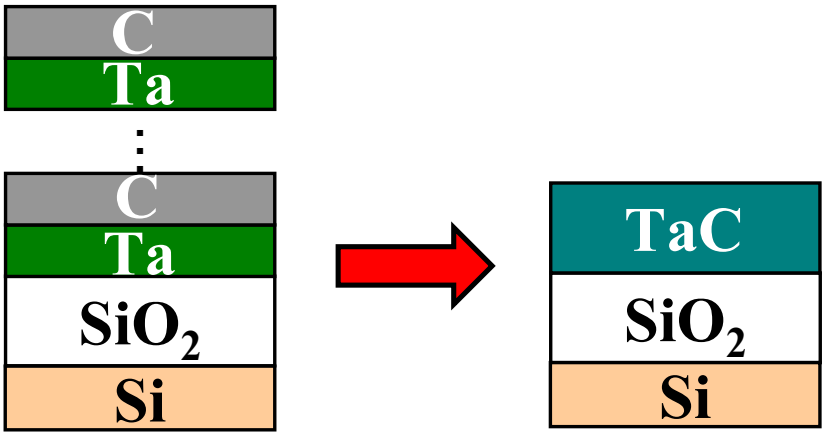


Figure 3.7 Formation of TaC

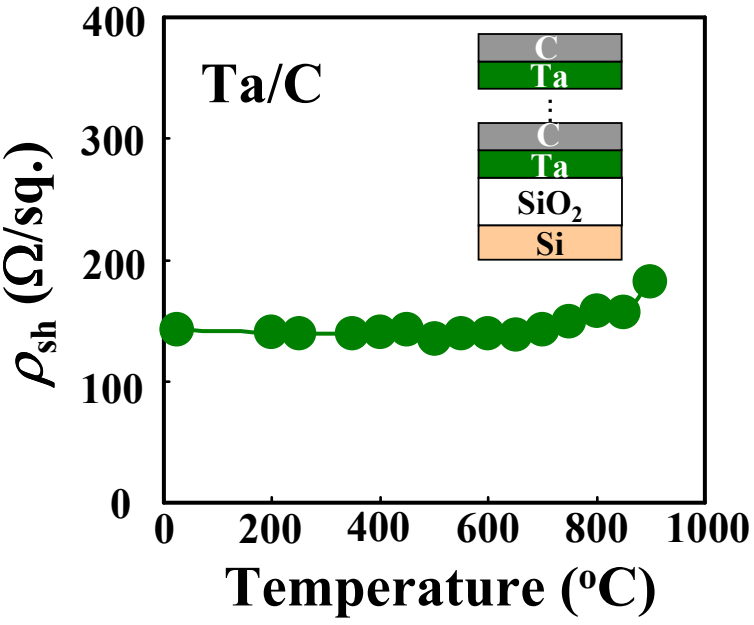


Figure 3.8 Sheet resistance of multi-stacked Ta/C layers

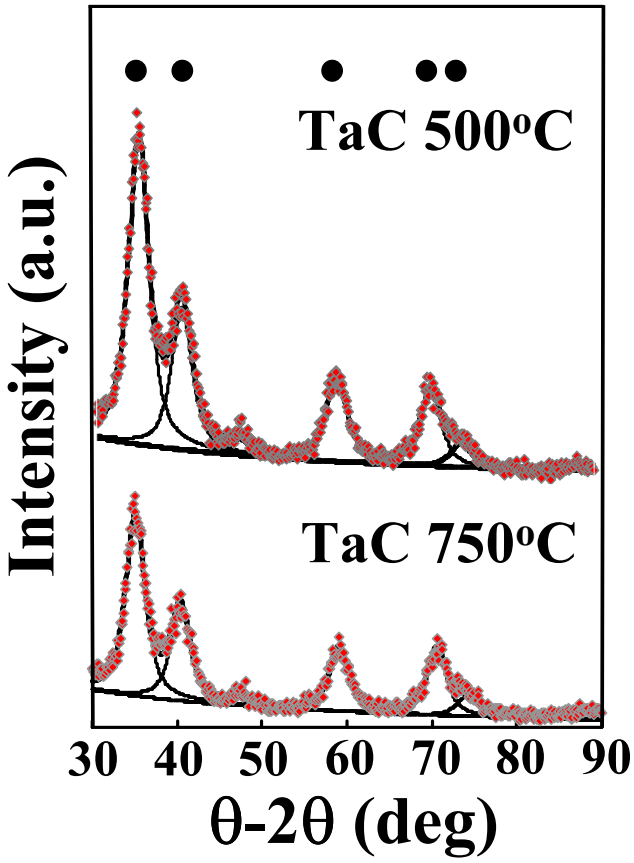


Figure 3.9 XRD measurement of multi-stacked Ta/C layers

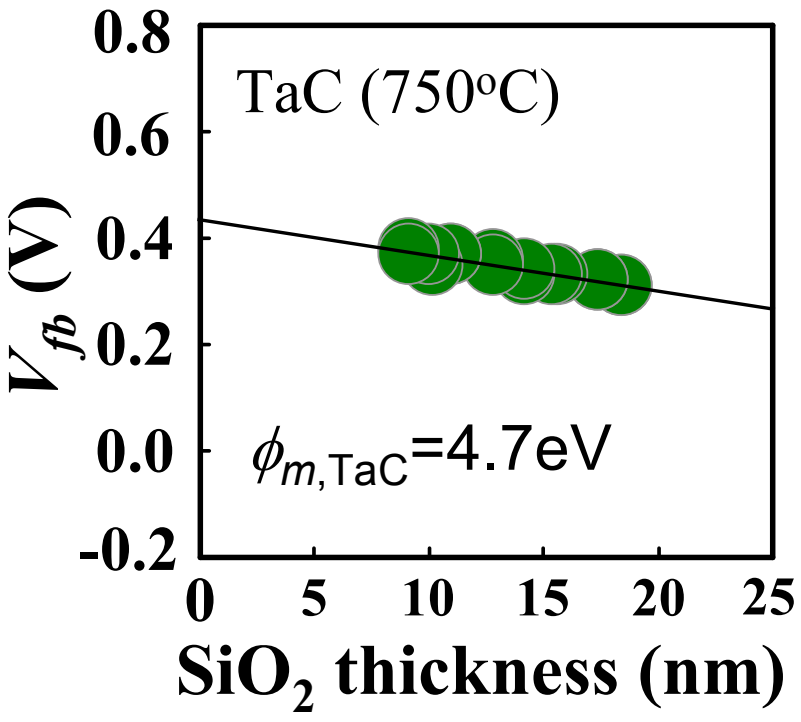


Figure 3.10 Work function of TiC

Work functions of TaC electrodes formed by stacked sputtering process were extracted through fabrication of metal-oxide-semiconductor (MOS) capacitors using (100)-oriented *n*-Si substrates and measurements of flatband voltage (V_{fb}) on different SiO_2 thickness same as TiC. Figure 3.10 shows the measured V_{fb} on SiO_2 thickness. work function values of 4.7 were extracted for TaC. Generally, low work functions around 4.2 eV are reported for bulk TaC [3.10, 3.11, 3.12], The reason might be due to oriented growth of carbide layers, where preferred surface orientation with high work function could be in contact to the SiO_2 layer as the same phenomenon is observed for chemical-vapored deposited TiN electrodes[3.13]. To confirm the oriented growth, normalized intensities of each diffraction plane of carbides are summarized in table 3.2. By comparing those ratios with powder diffraction database[3.14], where a random orientation is assumed, preferred orientation of (220) and (311) planes can be confirmed

for TaC layers.

TABLE 3.2. Normalized intensities of in-plane XRD measurements and powder diffraction patterns of TaC. (JC-PDS 00-035-0801)

(hkl) of cubic TaC	(111)	(200)	(220)	(311)
Ta/C stacked film annealed at 750 ºC	100	60	39	40
Powder diffraction pattern of cubic TaC	100	59	31	25

3.5 Tungsten Carbide Formation

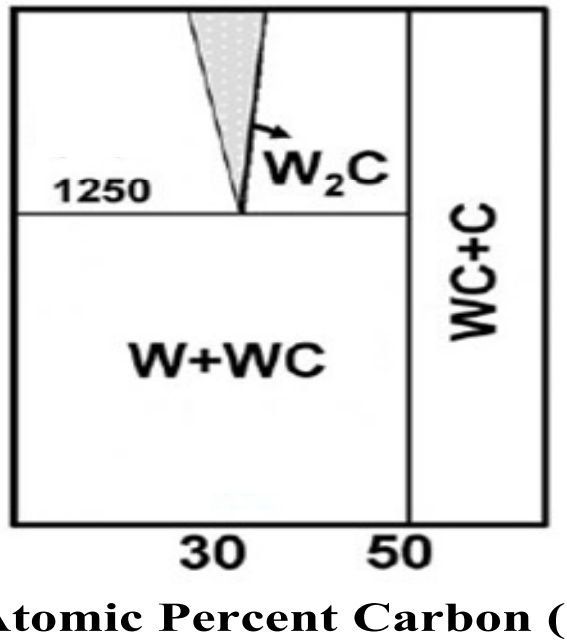


Figure 3.11 Carbon-Tungsten phase diagram [10]

As tungsten carbides take several stable compositions such as WC or W_2C in W-C phase diagram [3.15], as shown in Figure 3.11 , the thickness of each C layers in the

stacked sputtering process, were varied from 0.22 to 0.45 nm, while the thickness of the W layer is kept constant as 0.7 nm, as shown in Figure 3.12. The varied thickness corresponds to an atomic concentration from 1:0.5 to 1:1. Figure 3.13 shows the ρ_{sh} change on annealing temperature for four kinds of C concentrations. First decrease in ρ_{sh} was observed at 700 ^{o}C, and second one at 825 ^{o}C, irrespective to the C thicknesses, indicates drastic phase change in the films, which is contrast to the Ti or Ta cases. Figure 3.14 shows the in-plane XRD spectra of W/C with 1:0.5 and 1:1, annealed at 750 ^{o}C. With W/C of 1:0.5, weak diffraction peaks suggest the mixture of hexagonal W_2C and hexagonal WC phases in the film with grain size of 18 and 19 nm, respectively. On the other hand, for the film with W/C of 1:1, only hexagonal W_2C with grain size of 1.9 nm, was detected. The cross-sectional transmission electron microscope (TEM) image, shown in figure 3.15, revealed a column-like shape metal layer with grain size of 2 nm, which is in good agreement with the value extracted by XRD peaks. The ρ_{sh} of 94 Ω/sq., 188 μΩcm in resistivity, is only a double compared to that of bulk W_2C [3.14]. As the electron mean free path of W_2C is 1.8 nm, the main scattering mechanism can be attributed to grain boundary and not by the thickness of the film. Metal gates with nano-sized grains and short mean free path is advantageous for future narrow gate length as the effect of structure rarely influence the resistivity. An in-plane XRD measurement of W/C of 1:1 annealed at 900 ^{o}C, showed strong signals related to cubic W with grain size of 20 nm. The corresponding TEM image of the sample, shown in figure 3.15, revealed the formation of W grains on SiO_2 layer, where the grain size of 20 nm in width and 12 nm in height is in good agreement with the size extracted by XRD pattern. As the interface between W and SiO_2 layers becomes rough with the presence of a weak contrast at the interface, we can consider that interface reaction took place upon

annealing. The formation of pure W can be understood by decomposition of W_2C crystals to reduce the underlying SiO_2 layer with carbon atoms as $SiO_2(s)+3C(s)\rightarrow SiC(s)+CO(g)$ [3.17].

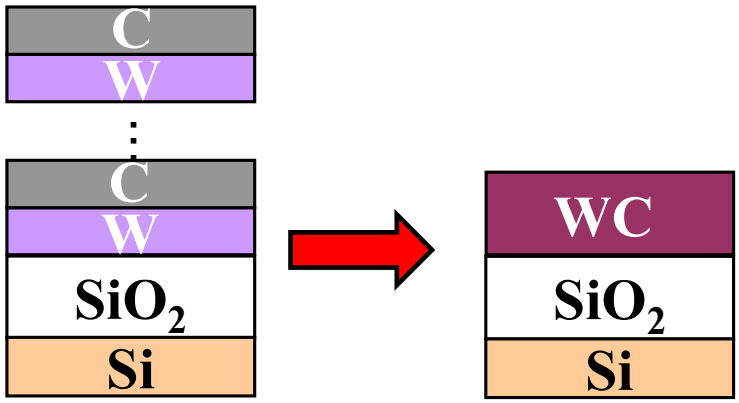
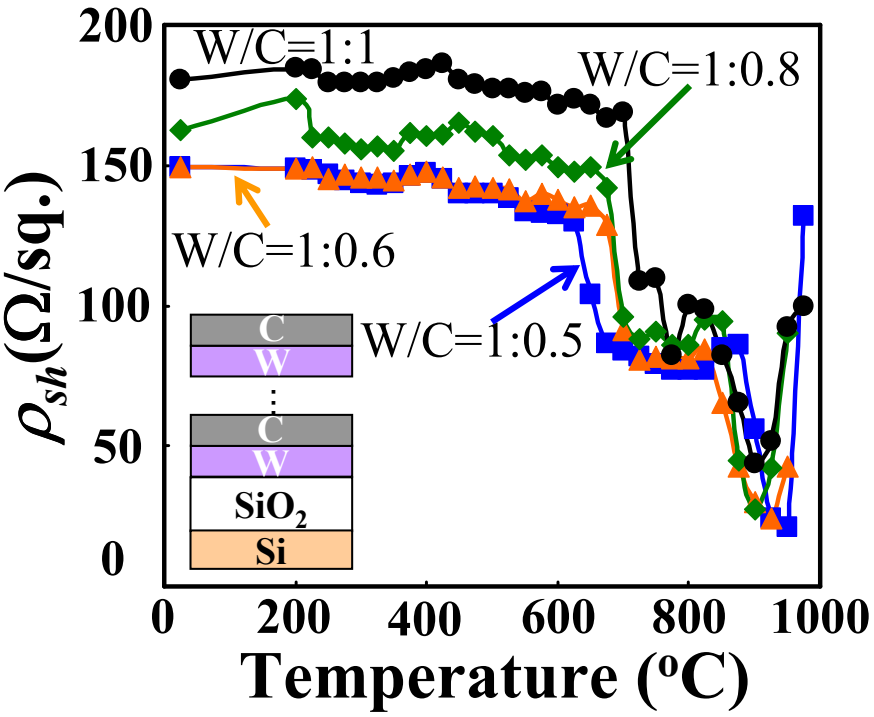


Figure 3.12 Formation of tungsten carbide



igure 3.13 Sheet resistance of multi-stacked W/C layers

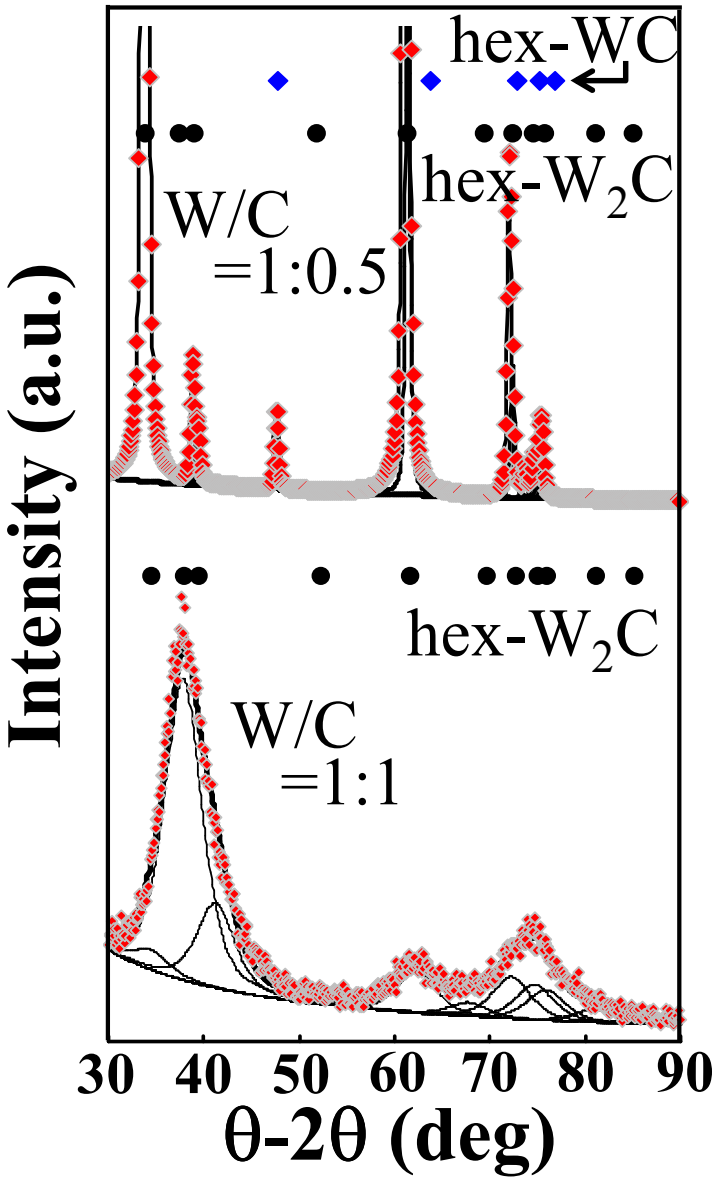


Figure 3.14 XRD measurement of multi-stacked W/C layers

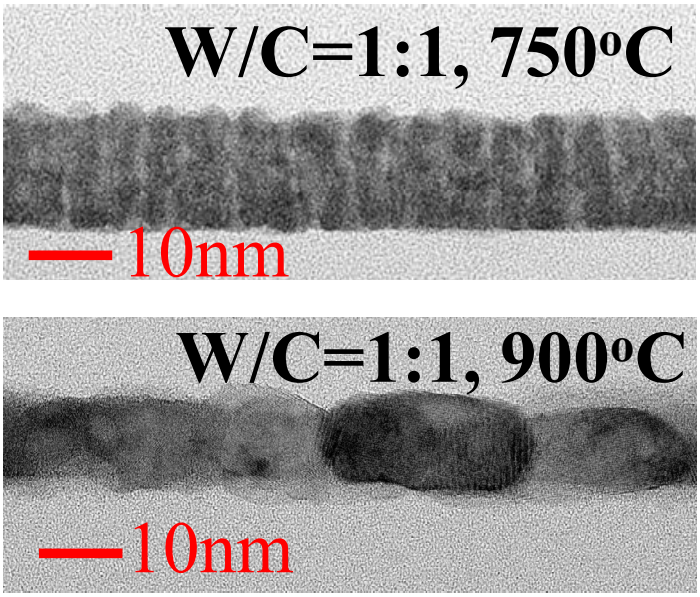


Figure 3.15 TEM of multi-stacked W/C layers

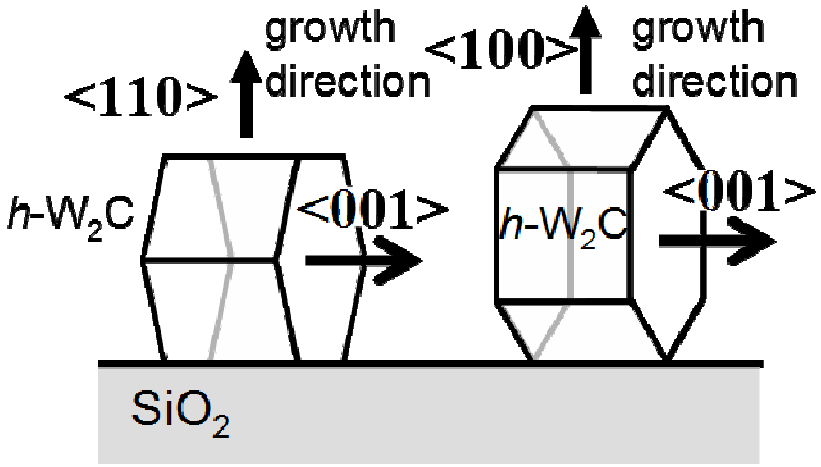


Figure 3.16 highly oriented tungsten carbide formation

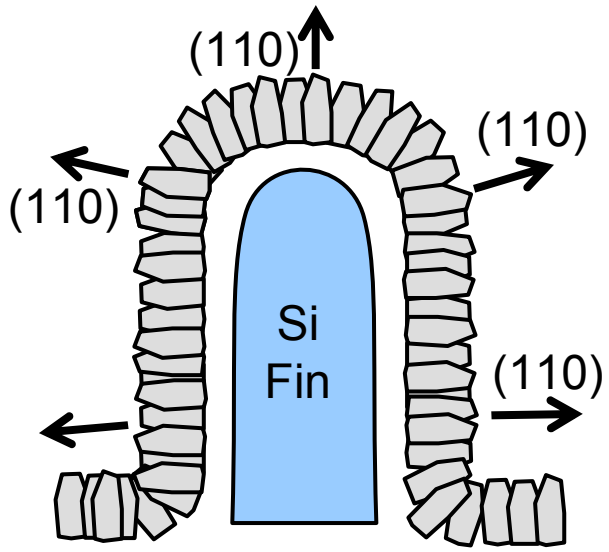


Figure 3.17 Prospective for 3D channel application

Work functions of W_2C electrodes formed by stacked sputtering process were extracted through fabrication of metal-oxide-semiconductor (MOS) capacitors using (100)-oriented *n*-Si substrates (N_d=3×10^{15} cm^{-3}) and measurements of flatband voltage (V_{fb}) on different SiO_2 thickness. Here, W/C of 1:1 is used to form W_2C electrode. To exclude the effect of interface states, annealing in forming gas (H_2:N_2=3%:97%) at 420 ^oC for 30 min was performed for all the samples. Figure 3.16 shows the measured V_{fb} on SiO_2 thickness. Work function values of 4.9 eV were extracted W_2C. To confirm the oriented growth, normalized intensities of each diffraction plane of carbides are summarized in table 1. W_2C layer showed strong preferred orientation with (002) plane, which indicates that c-axis of W_2C crystals is in parallel to the surface of SiO_2. A high work function of W_2C is in good agreement with reported values. Moreover, a high work function of 4.9 eV with W_2C is suitable for *p*-ch MOS devices.

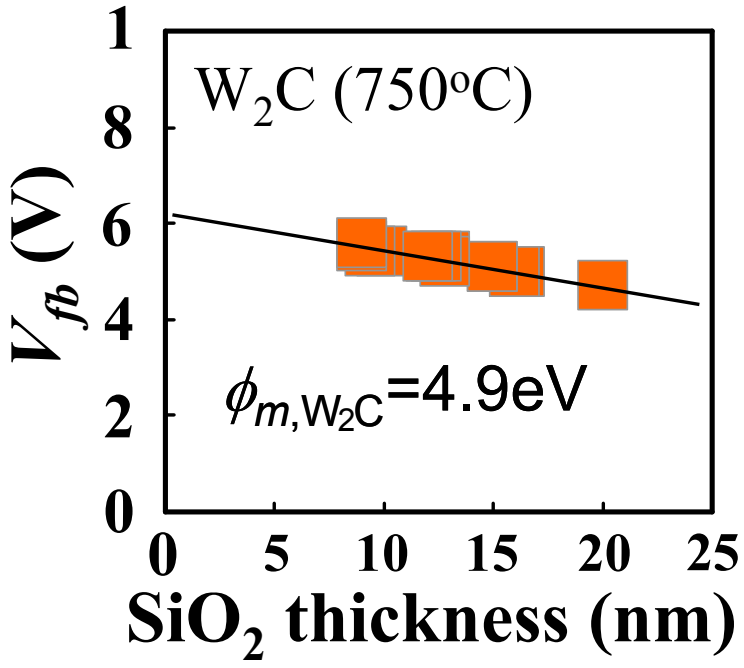


Figure 3.18 Work function of WC annealing at 750°C

TABLE 3.3. Normalized intensities of in-plane XRD measurements and powder diffraction patterns of W_2C. (JC-PDS 00-035-0776)

(hkl) of hexagonal W_2C	(100)	(002)	(101)	(102)
W/C stacked film annealed at 750 °C	23	355	100	1
Powder diffraction pattern of hexagonal W_2C[c]	23	24	100	14

3.6 Conclusions

A sputtering process using multi-stacking of carbon and metal thin films with subsequent annealing process to reactively form metal carbides (TiC, TaC and W_2C) has been presented. Grain sizes of the carbides are as small as 3.9, 3.2, and 1.9 nm for TiC, TaC and W_2C, respectively. Work functions of TiC, TaC and W_2C layers have been extracted as 4.3, 4.7, and 4.9 eV, respectively, relatively high values owing to oriented growth, as shown in Figure 3.16. W_2C layer formed by the presented process gives high potential to form carbides with nano-sized grain and high work function for gate electrode application for planner and 3D FET, as shown in Figure 3.17.

Table 3.4 Summary of grain size and orientation of nitrides and carbides with nano sized grains.

Metal gate	Grain size	Process	Oriented growth	Ref.
TiN	22 nm	Sput.	No	Re.
		CVD	Yes; <100>⊥sub.	
TaN	9.2 nm	CVD	No	Re.
TiC	3.9 nm	Sput.+Reaction	No	this work
TaC	3.2 nm	Sput.+Reaction	No	this work
W_2C	1.9 nm	Sput.+Reaction	Yes; <001>//sub.	this work

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Chapter 4 Electrical Properties of La-silicate High-k with Tungsten Carbide

4.1 Introduction

4.2 Interface properties of La-silicate with tungsten carbide gate electrode

4.3 MOSFET characteristics with tungsten carbide gate electrode

4.4 Conclusions

4.5 References

4.1 Introduction

High-k gate dielectrics have enabled continuous scaling in complementary metal-oxide semiconductor (CMOS) devices by increasing the capacitive coupling of gate electrode to the channel which eventually suppresses the short channel effects, while reducing the gate leakage current [4.1-4.3]. Considering further equivalent oxide thickness (EOT) scaling down to 0.45 nm, which is required in the year of 2026 from ITRS roadmap [4.4], high-k materials should be directly in contact with Si channels [4.5]. Some of attempts to achieve direct contact of high-k on Si channels have been proposed so far; those include precise oxygen partial pressure controlled process [4.6] and a thermal process to reduce the interfacial layer by incorporating additional elements in the metal gates [4.7, 4.8]. In addition to these processes, La-silicate can be in direct contact with Si channels by means of silicate reactions between La_2O_3 layer and Si channel [4.9, 4.10]. The prominent features of La-silicate are that the structure is amorphous and the silicate reaction does not show any channel surface orientation dependency, which are advantageous for scaled devices with three dimensional channels [4.11]. Issues in La-silicate/Si interfaces include D_{it} in the order of high 10^{11} cm^{-2}/eV, and interface roughness presented at both metal/La-silicate and La-silicate/Si interfaces, which results in channel effective mobility degradation due to La-silicate thickness variation [4.12]. An experimental work has shown that the effect of metal gate material affect the interface properties, so the impact of metal gate should be clarified [4.13]. As mentioned in chapter 3, highly-oriented tungsten carbide (W_2C) gate electrode with 1.9-nm-sized grains are proposed using multi-stacked W/C layers for gate electrode application for MOSFET. Therefore, in this chapter, the electrical properties of La-silicate MOS capacitors have been investigated and focused on the

effect of grain size in metal gate electrode on La-silicate/Si interface properties including roughness using W_2C gate electrodes. The all sample annealed at 800ºC, it has been reported that the interface state density at La-silicate/Si interface can be reduced by increasing of annealing temperature [4.15], meantime, with high temperature annealing, interface state density can be as low as 10^{11} cm^{-2}/eV [4.10], thus the choice of 800ºC for annealing temperature is reasonable, and it is in W_2C formation temperature period, as mentioned in Figure 3.13 of chapter 3. The main fabricated process shown in figure 4.1.

MOS capacitors were fabricated on *n*-Si (100) substrates with doping of 3×10^{15} cm^{-3}, as shown in figure 4.1. After performing sulfuric peroxide mixture cleaning followed by HF dip cleanings, thin La_2O_3 gate dielectric films ranging from 2 to 4 nm were deposited by e-beam evaporation at a substrate temperature of 300 ºC in ultra-high vacuum (10^{-6} Pa). A set of W and C layers with thickness of 0.70 and 0.45 nm, respectively, were cyclically deposited for 18 times onto La_2O_3 films by RF magnetron sputtering without exposing the wafers to air, so that any moisture or carbon-related contamination can be eliminated. Samples with a pure W layer were also fabricated as counterparts. Then, TiN and Si capping layers with thicknesses of 10 and 100 nm, respectively, were deposited on W/C multi-stacked metal and W also by RF sputtering. Samples were subjected to annealing at 800 ºC in forming gas (N_2:H_2=97%:3%) ambient for 30 minutes to form an amorphous La-silicate layer by reaction of La_2O_3 and Si substrates. The capping layers of Si and TiN are used to inhibit oxygen atom diffusion from ambient to La_2O_3 layer during the annealing, which allows precise control of interface reaction between La_2O_3 and Si substrates [4.10]. The annealing process also induces reactions at W and C layers to form W carbides at this temperature

[4.14]. After removing the capped Si layers and forming backside Al contacts, samples were subjected to annealing at 420 ^{o}C in forming gas ambient for 30 minutes.

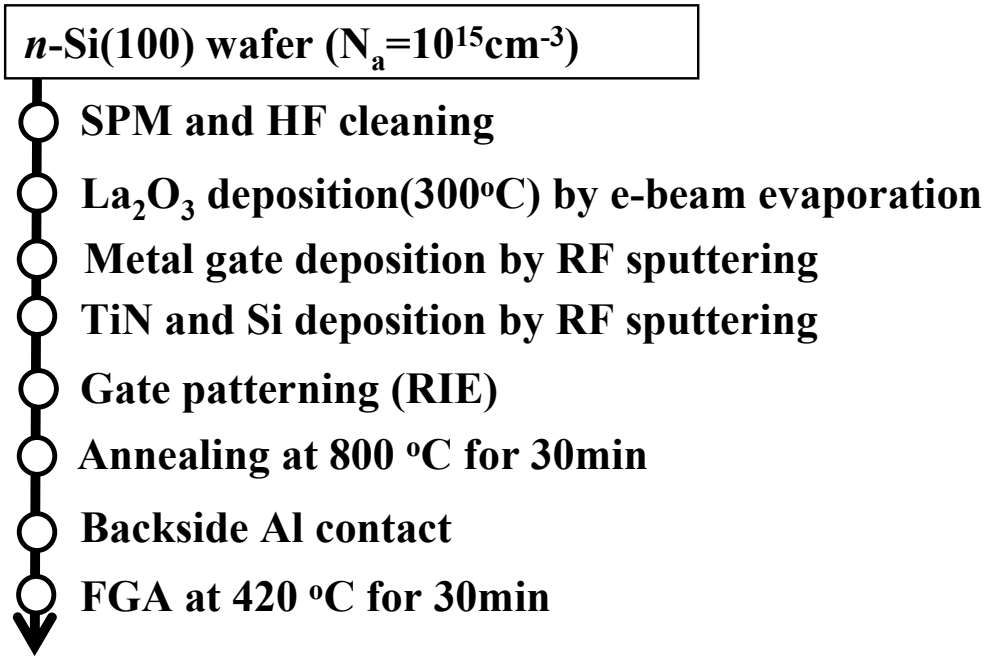


Figure 4.1 Fabrication procedure for MOS devices

4.2 Interface properties of La-silicate with tungsten carbide gate electrode

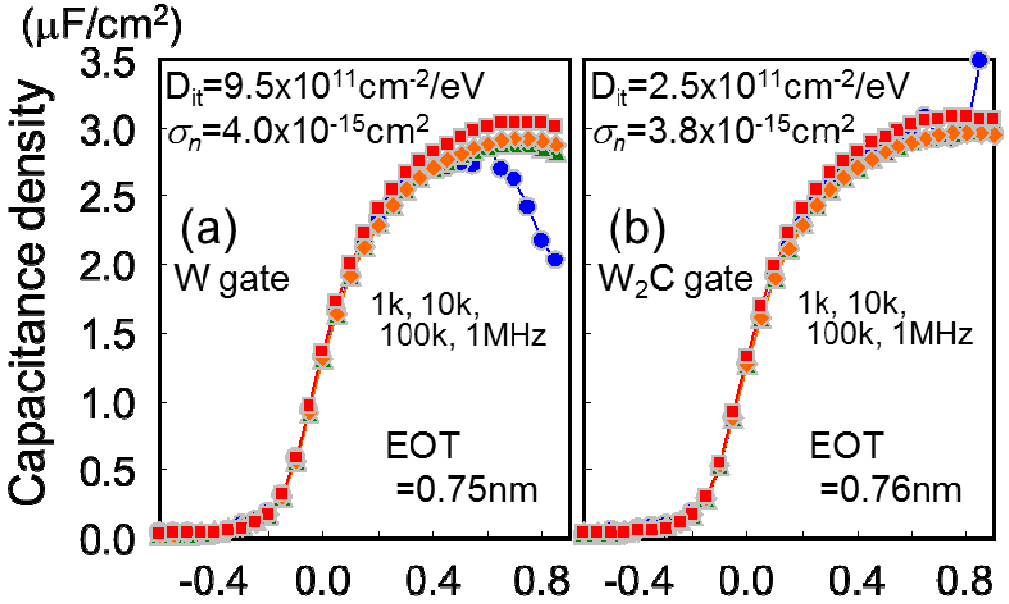
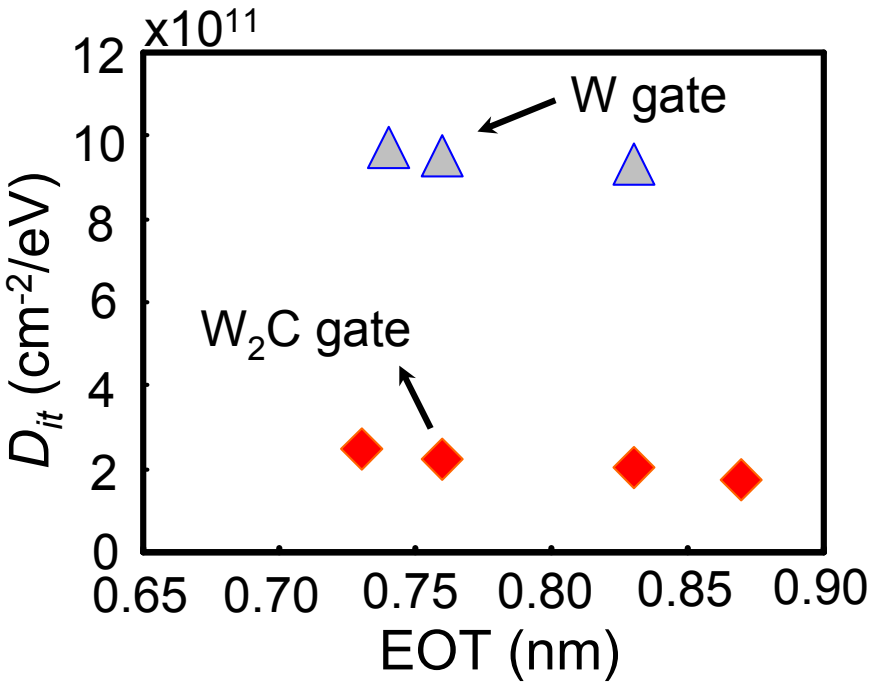


Figure 4.2 C-V characteristics of TiN/W_2C/La-silicate/Si and TiN/W/La-silicate/Si

Capacitance-voltage (CV) characteristics of La-silicate capacitors with pure W or nano-sized grain W_2C metal gates are shown in figure 4.2 (a) and (b), respectively. Similar EOT of 0.75 nm were obtained for both samples, suggesting there is no difference in interface silicate reaction rate between the gate electrode materials. Also similar flatband voltage (V_{fb}) was measured, indicating that there is little change in the influence of metal gate electrodes to interface charges. Humps in depletion region, which is typically observed for high-k/Si direct contact capacitors, were sufficiently suppressed for both samples, indicating fairly nice interface properties. Conductance

method, taking the surface potential fluctuation of 80 meV into account [4.17], revealed D_{it} of 9.5×10^{11} and 2.5×10^{11} cm^{-2}/eV for W and W_2C metal gate electrodes, respectively, indicating large reduction by one-third for the capacitor with W_2C gate electrode. From the trap time constant dependency on surface potential, identical capture cross sections of 3×10^{-15} cm^2 were extracted among the samples, which is comparable to those reported on thermal SiO_2 on Si(100) surface [4.18]. Therefore, the physical nature of the D_{it} can be thought to be the same, and only the amounts of the trap states are different. D_{it} dependency on EOT, in figure 4.3, shows that D_{it} can be reduced in all the studied EOT range with W_2C gate electrode. A slight degradation in D_{it} observed with smaller EOT, which is in good agreement with previous reports [4.19], will be discussed in the following text. And constant V_{fb} on different EOT, indicating low Q_{fix} ($10^{10}/cm^2$) in La-silicate with W_2C gate electrode.



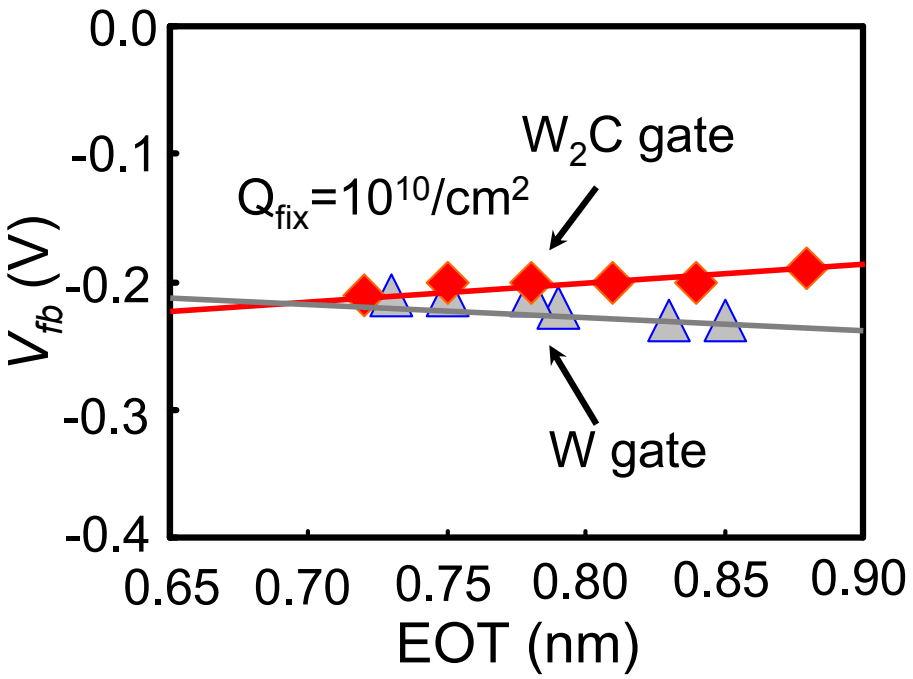
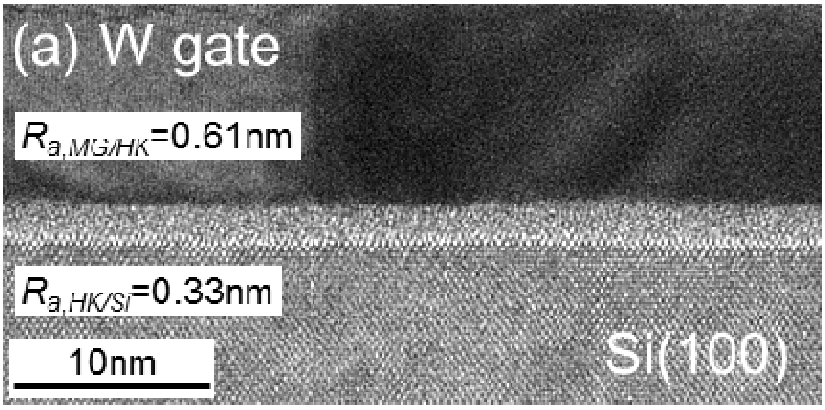
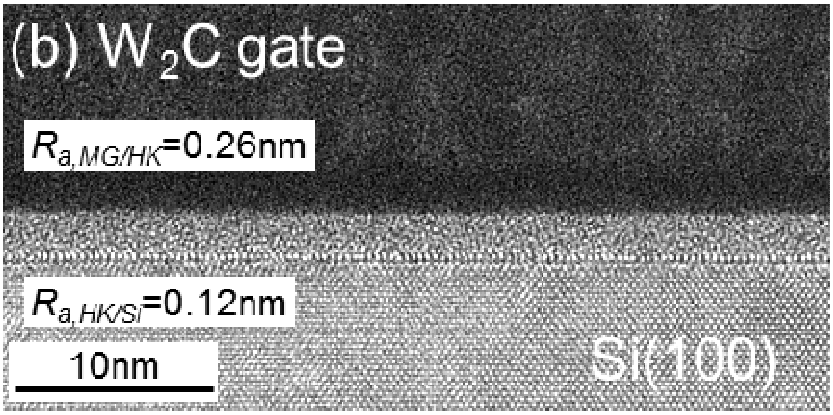


Figure 4.3 Dependency of interface state density (D_{it}) on EOT and Flat band voltage as a function of EOT

Cross-sectional transmission electron microscope (TEM) images of the electrically measured capacitors with W and W_2C gate electrodes are shown in figure 4.4 (a) and (b), respectively. One can find rough metal/high-k and high-k/Si interfaces with the W gated capacitor. Interface height position analysis showed root-mean-square (RMS) roughness of metal/high-k ($R_{a,MG/HK}$) and high-k/Si ($R_{a,HK/Si}$) interfaces to be 0.61 nm and 0.33 nm, respectively. On the other hand, the TEM image of the capacitor with W_2C gate electrode showed an atomically flat metal/high-k and high-k/Si interfaces; $R_{a,MG/HK}$ of 0.26 nm and $R_{a,HK/Si}$ of 0.12 nm. An RMS roughness of 0.12 nm is comparable to those of thermal SiO_2 on Si(100) substrates formed at high temperature with enough thickness [4.20], and is far smaller than reported high-k dielectrics directly in contact to Si

substrates [4.7].





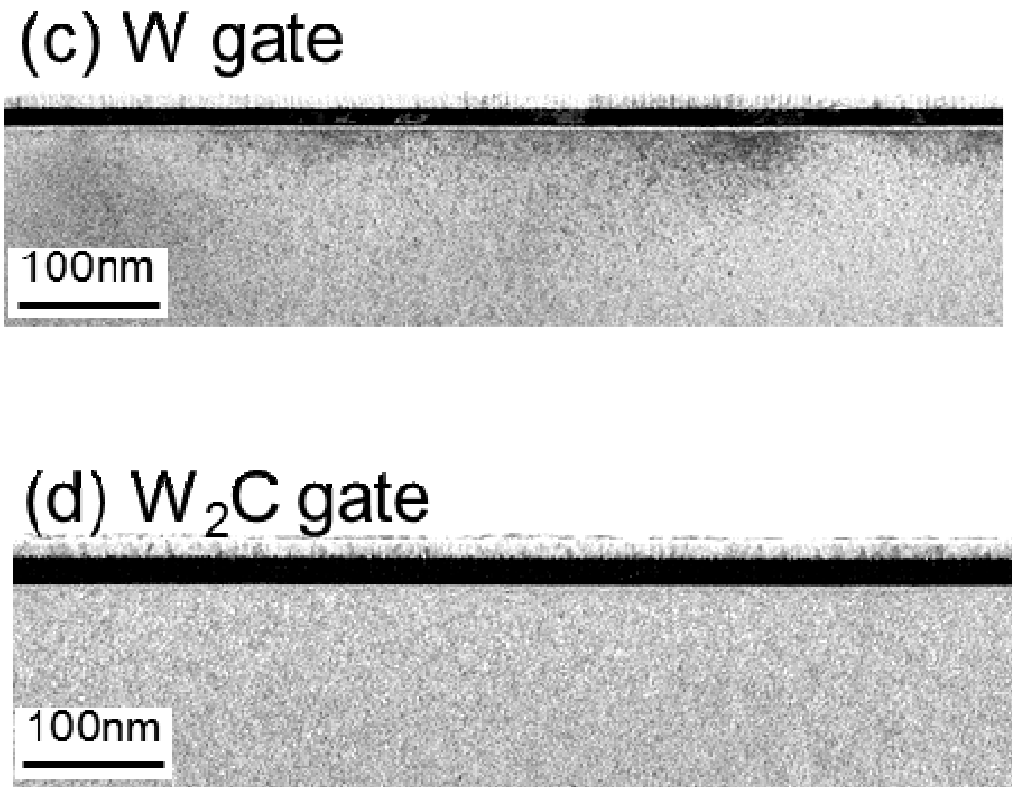
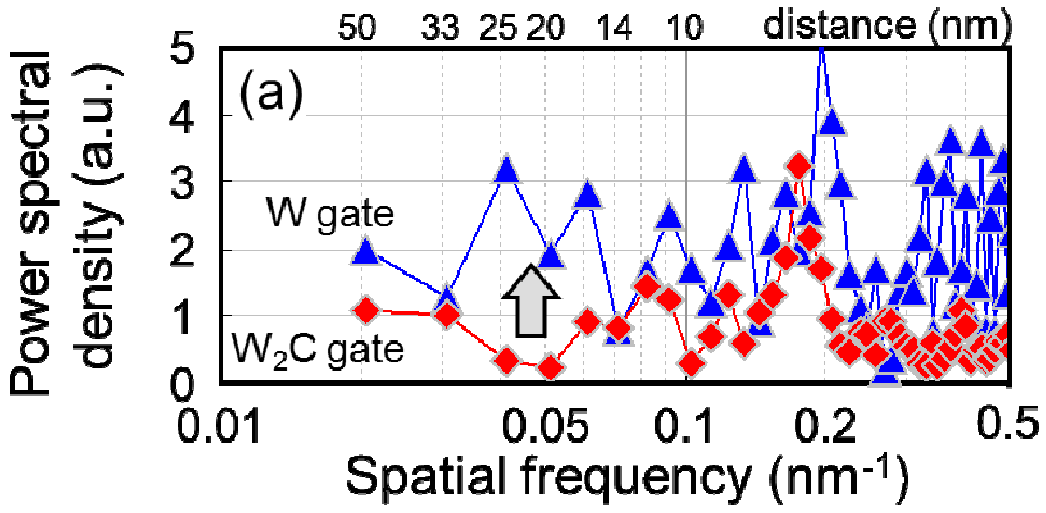


Figure 4.4 Cross sectional TEM images of the La-silicate capacitor with (a) W gate electrode [magnified view in (c)] and those of W_2C gate electrode [magnified view in (d)].

An intuitive explanation of the reduction in D_{it} with W_2C gate electrode can be drawn from the improvement in flatness at La-silicate/Si interface. Generally, edge sites in the step atoms at SiO_2/Si(100) interface are responsible for D_{it}, so that higher atom steps at the interface which constitute a stronger distortion at the step edge increase the D_{it} [4.21]. The appearance of edge steps at the interface is commonly observed when Si(100) substrates are oxidized below a temperature where the viscous flow is hardly presented. The interface roughness is reported to arise due to inhomogeneous local

stress effects, and to be more prominent when surface irregularities increases [4.21]. In addition to the interface roughness difference between the samples, a dark contrast in the Si substrate can be observed in the TEM image of the capacitor with W gate electrode, which is not presented in that with W_2C gate electrode. Dark contrasts in TEM image in single crystalline silicon can result from poor crystallinity or by strain due to change in the lattice constant [4.21]. Here, both TEM specimens were prepared through identical focus-ion beam (FIB) sampling technology, so that preparation-induced damage to worsen the crystallinity can be eliminated. Thus, one can consider that a strong inhomogeneous residual stress exists in the Si substrate near the surface, which extends down to several hundred nanometers deep in Si substrate.



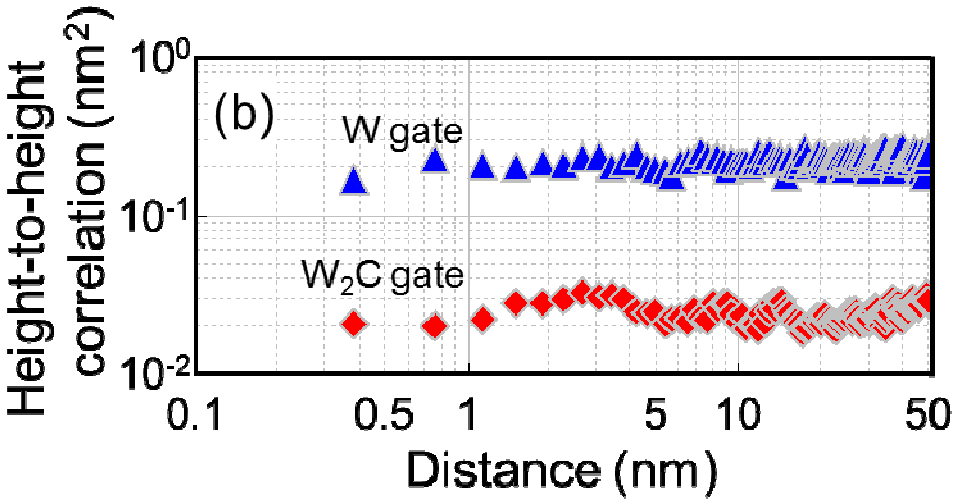


Figure 4.5 (a) Power spectral density of La-silicate/Si interface height position obtained from FFT analysis and (b) height-to-height correlation of the interface for both W and W_2C gate electrodes.

Fast Fourier transform (FFT) analysis of the roughness taken from TEM images are shown in figure 4.5 (a). By comparing the power spectral density of both interfaces, higher values from 0.04 to 0.06 nm^{-1} in spatial frequency, which corresponds to interface roughness period of 17 to 25 nm, can be confirmed with W gate electrode. These values are comparable to the average grain size of 20 nm in W gate electrode which is obtained from x-ray diffraction measurements [4.14]. Therefore, a strong correlation exists between the grain size of the metal gate electrode and the interface roughness. The starting materials were both the same for W and W_2C gate electrodes, the appearance of interface roughness should arise during the reaction to form La-silicate layers between La_2O_3 and Si substrate. Generally, surface reaction rate can be anisotropic depending on crystal planes due to difference in surface energy and

elastic constants [4.23]. Moreover, the reaction can be inhomogeneous due to defects or impurities at the surface [4.24]. In this study, however, the starting materials are the same and are processed through identical wet cleaning, deposition and annealing processes so that the effects contaminants on the formation of interface roughness can be negligible. As the only difference is the metal gate material, the effect of stress induced from the metal layer can be the origin to change the interface roughness. Base upon the reports on amorphous-to-crystalline transformation in silicon, the crystallization rate is affected by the stress applied in the plane of interface; higher rate with tensile stress and lower rate with compressive stress, where the effect of stress is interpreted as the change in the activation energy of reaction [4.25]. For our case, crystal grains accompanied by grain boundaries in W gate electrode may induce non-uniform stress to the Si surface to change the rate of silicate reaction, which results in roughening the interface. As a result of small average grain size of 1.9 nm with W_2C gate electrode, the stress accompanied during reaction can be evened out, so that the initial surface flatness can be hardly infected. The increase in D_{it} with smaller EOT might be understood from increase in stress due to thinner La-silicate film thickness. Height-to-height correlations of both La-silicate/Si interfaces are shown in figure 4.5 (b). Both interfaces did not show any scaling dependency, which suggests that presented interfaces are not self-affine structures, and follows random Gaussian distribution from atomic scale [4.26]. This is not the case for thermal SiO_2/Si interface case where a balance between local stress to roughen and viscous flow to smoothen the interface is presented within a specific scale length [4.25]. Therefore, one can conclude that metal gate electrodes with nano-sized grains or even amorphous structures are effective for obtaining atomically flat La-silicate/Si interfaces by removing inhomogeneous local

stress. Also, a flat metal/La-silicate interface can be obtained with nano-sized grain metal, which is effective in suppressing gate oxide thickness variability. Incidentally, we would like to note that metal gates with nano-sized grains are mandatory in terms of threshold voltage variability suppression, which holds the right direction for metal gate material selection for scaled devices. Besides, when comparing the D_{it} with SiO_2/Si cases, La-silicate capacitors with W_2C gate electrode still present higher D_{it} by one order of magnitude even with atomically flat interface. The difference between SiO_2 and La-silicate is that La atoms are presented at the interface. It is reported that D_{it} can also be degraded due to the presence of other elements at the interface. For example, a trace amount of Al atoms at the interface are reported to increase the D_{it}, whereas Zn atoms slightly increase the D_{it} when the amount exceeds a certain level [4.28, 4.29]. On the other hand, Ca or Cr atoms do not degrade the D_{it} [4.30]. Although the mechanism is not clarified yet, formation of Al or Zn compounds at the interface is speculated to be the source. For La-silicate case, the contribution of La atoms presented at the interface to D_{it} is not known yet, however, it can be speculated that La atoms may slightly increase the D_{it}.

According to the reports [4.31], shown in figure 4.6, the solid-phase epitaxial-growth rate of crystalline Si from the amorphous Si on the tensile side is greater than on the compressive side of elastically bent wafers. Tensile stress to increase the reaction, compressive stress to decrease the reaction. Reaction rate change due to applied stress can be interpreted as change in activation energy. Thus, in our case, there are high possibility that silicate reaction rate can be modified under applied stress. The possible mechanism shown in figure 4.7. Nano-sized grains help elimination of inhomogeneous stress applied to the interface to form uniform La-silicate gate

dielectrics.

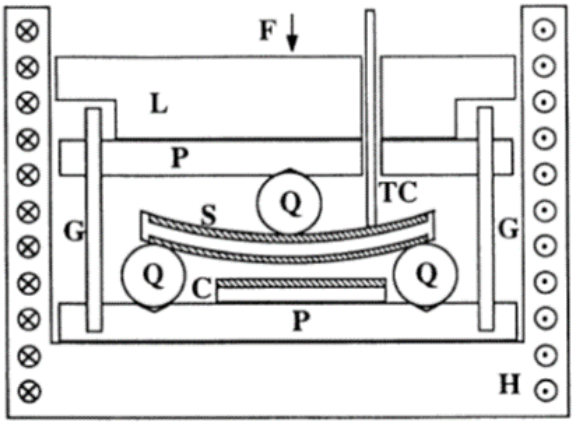


FIG. 1. Schematic cross section of three-point bending apparatus for annealing wafers under nonhydrostatic stress. S: sample, cross-hatched areas correspond to amorphous Si; C: calibration sample; Q: fused quartz support rods; P: brass plate; G: guide posts; TC: thermocouple; H: heating element; F: weights; L: lid.

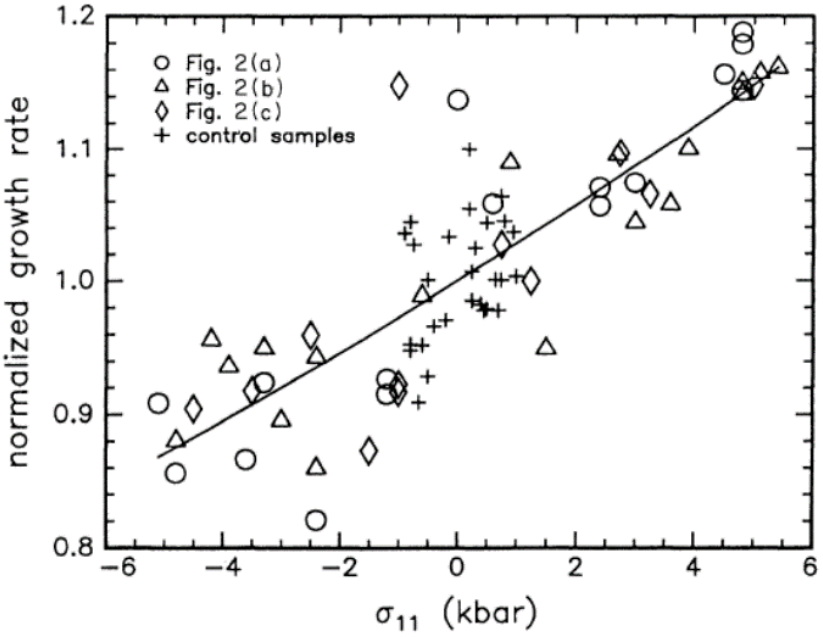


Figure 4.6 Reports on stress induced reaction [4.31]

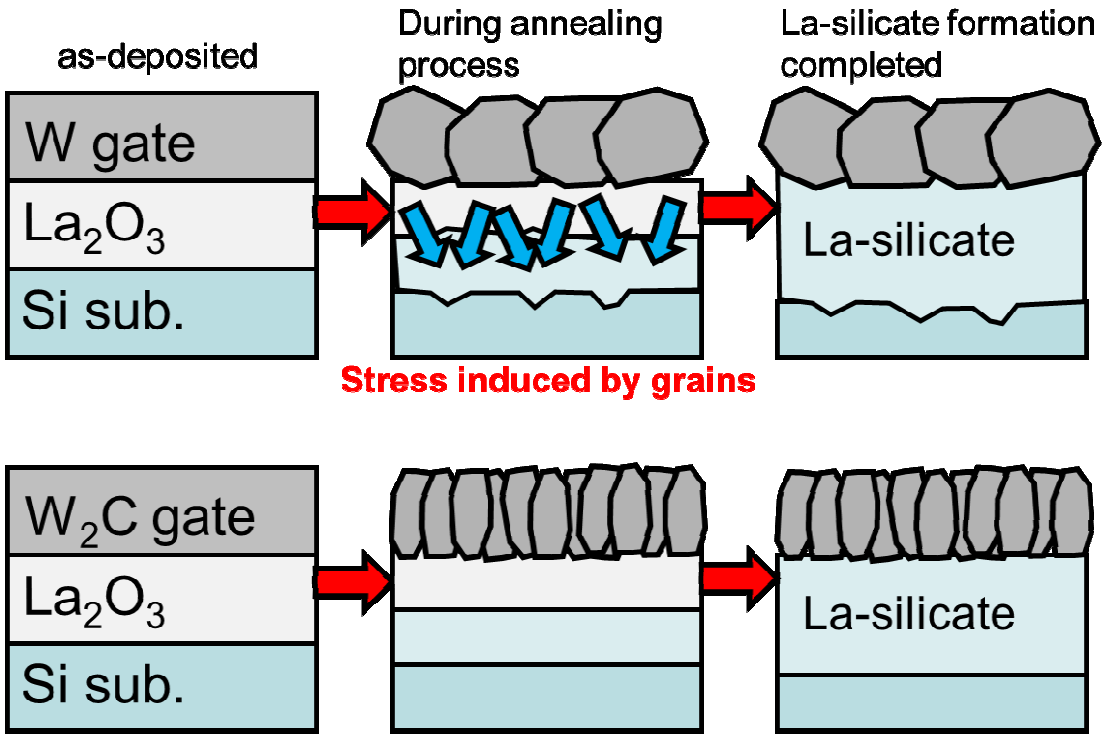


Figure 4.7 A schematic model to explain atomically flat interface of high-k/Si

In summary, the interface properties of reactively formed La-silicate gate dielectrics on Si substrates with W or nano-sized grain W_2C gate electrodes have been investigated. An interface with periodic roughness comparable to the average grain size of W gate electrode has been observed, where an atomically flat La-silicate/Si interface has been obtained with nano-sized grain W_2C gate electrode. The origin of smooth interface roughness may be attributed to the elimination of inhomogeneous stress induced by metal grains during the formation of silicate at the interface.

4.3 Experimental results of MOSFETs

In this study, nMOSFETs were fabricated by a gate-last process using source and drain preformed p-Si (100) substrates with a substrate impurity concentration of 3×10^{16} cm^{-3}. Figure 4.8 shows the device fabrication process flows. After performing SPM and HF chemical cleanings with H_2SO_4/H_2O_2 mixture at 130°C for 5 minutes, thin La_2O_3 gate dielectric films were deposited by e-beam evaporation at a substrate temperature of 300 °C. Metal gate were deposited by radio frequency (RF) magnetron sputtering without breaking the ultra-high vacuum. Then, TiN (10nm) and Si (100nm) capping layers were deposited on W/C metal also by RF sputtering to control the silicate reaction. The gate electrode was patterned by lithography and formed by reactive-ion etching (RIE). The samples were then annealed at 800°C in forming gas (N_2:H_2=97:3) ambient. Source/Drain and backside contacts were formed by Al evaporation. Finally, the sample was annealed in forming gas (N_2:H_2=97:3) ambient at 420 °C for 30 minutes.

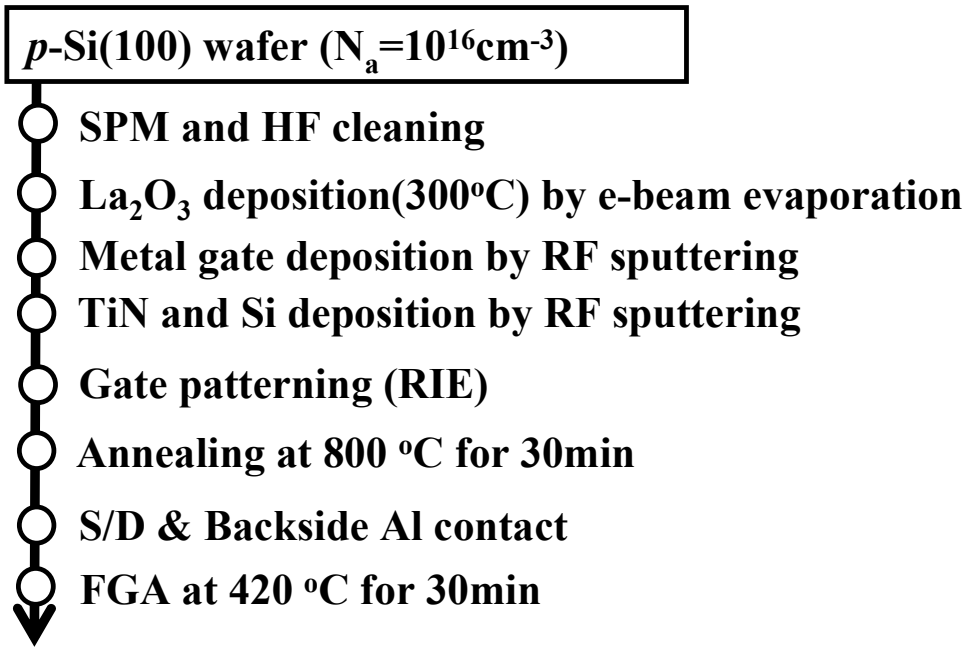


Figure 4.8 Fabrication procedure for MOSFETs

Figure 4.9 shows impact of carbon atoms on D_{it}, smaller *Dit* were obtained with tungsten carbide gate electrodes especially with a ratio of 1 to 1. The La-silicate MOSFETs with W_2C (W:C=1:1) have been prepared, where the MOSFET with tungsten carbide with a ratio of 1 to 0.5 for reference, as shown in figure 4.10. Higher effective mobility of 163 cm^2/Vs (E_{eff}=1MV) at an EOT of 0.63 nm was achieved by W_2C gate electrode, owing to lower D_{it} and reduced roughness scatterings. Benchmarking of μ_{eff} at high E_{eff} , as shown in figure 4.11, W_2C gate with La-silicate gate stack exhibit μ_{eff} improvements beyond μ_{eff} -EOT trends line.

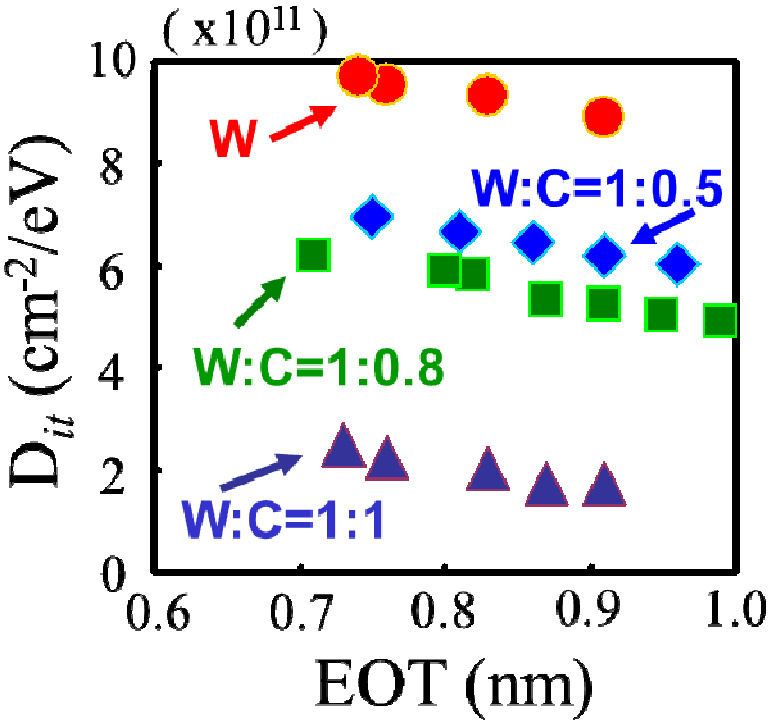
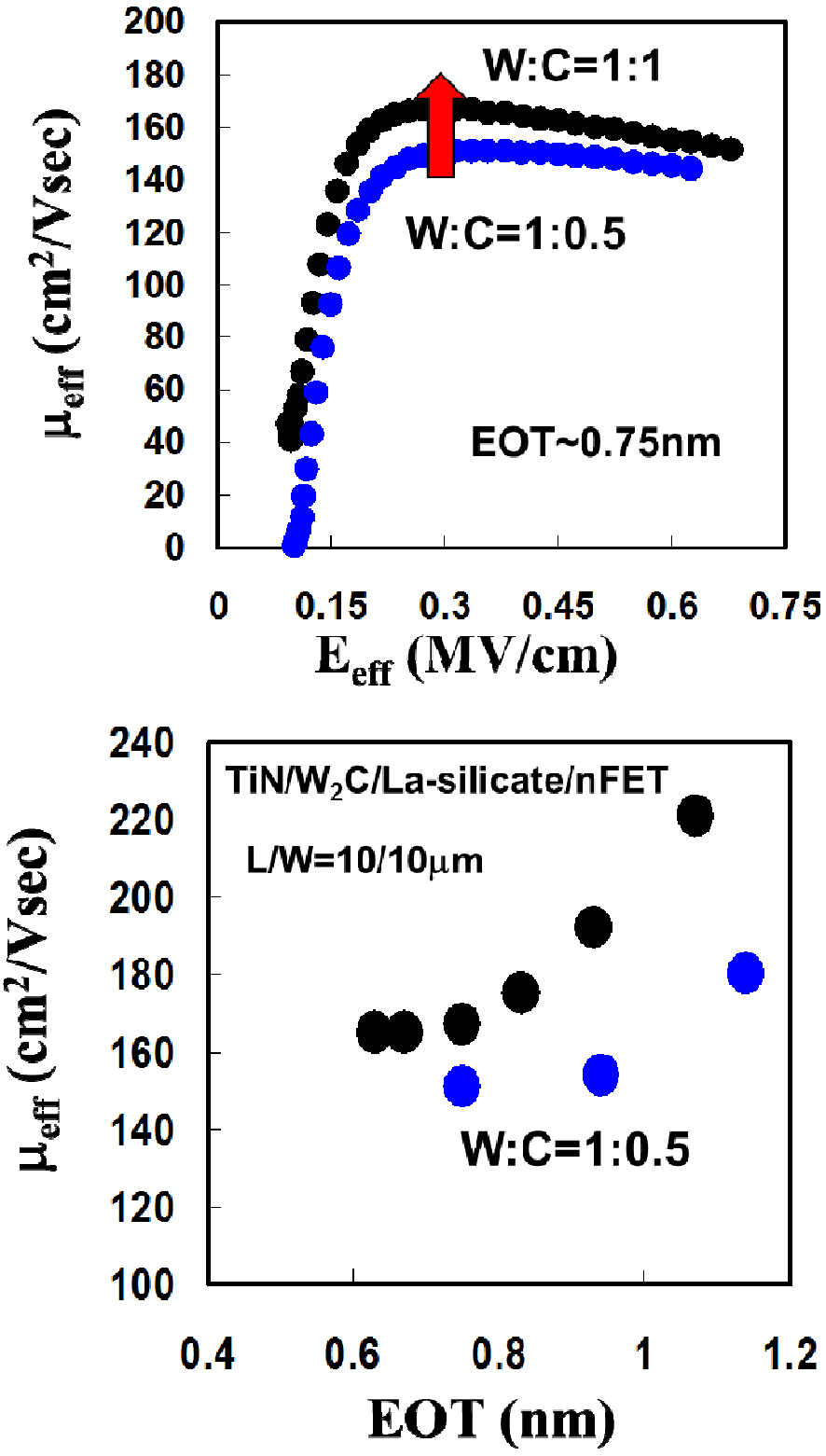
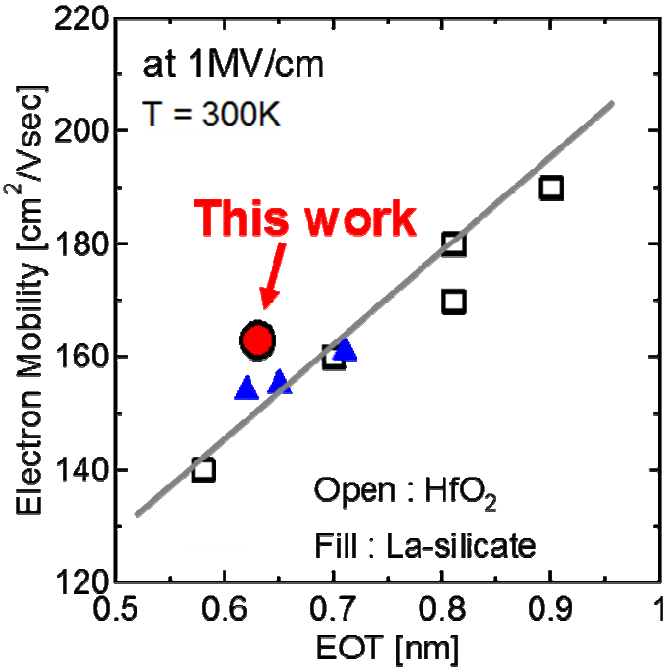


Figure 4.9 Relationship of D_{it} and EOT



4.10 Electron mobility of W_2C gate La-silicate nMOSFET



4.11 A benchmark of high-field electron mobility at 1MV/cm [4.12]

4.4 Conclusions

Electrical properties of La-silicate MOS devices and nMOSFET with nano-sized tungsten carbide (W_2C) gate electrode has been experimentally investigated. Interface state density (D_{it}) was suppressed by W_2C gate electrodes. Atomically flat metal/high-k and high-k/Si interfaces can be achieved by W_2C gate electrodes, where the interface roughness extracted from TEM is 0.26 and 0.12nm, respectively. Origin of interface state density is due to La-silicate/Si interface roughness due to grains in metal gate electrode. Electron μ_{eff} showed improvements in both low and high E_{eff}, especially 163 cm^2/Vs (E_{eff}=1MV) at an EOT of 0.63 nm was achieved, owing to lower D_{it} and reduced roughness scatterings.

Table 4.1 Comparison of reported processes for direct high-k/Si structures.

Process for direct high-k/Si	EOT	Mobility at 1MV/cm	Metal/high-k interface roughness	High-k/Si interface roughness	Ref.
Oxygen controled deposition (HfO_2)	0.59 nm	130 cm^2/Vs	0.46 nm	0.50 nm	[10]
IL scavenging by metal incorporation (TaN/cap/HfO_2)	0.55 nm	140 cm^2/Vs	0.66 nm	0.54 nm	[11]
Oxygen controled reacitve formation (W/La-silicate)	0.62 nm	155 cm^2/Vs	0.61 nm	0.36 nm	[7]
Oxygen controled reacitve formation with oriented nano-sized W_2C grains (W_2C/La-silicate)	**0.63 nm**	**163 cm^2/Vs**	**0.26 nm**	**0.12 nm**	**This work**

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Chapter 5 Reliability of La-silicate High-k with Tungsten Carbide Gate Electrode

5.1 Introduction

5.2 Time Dependent Dielectric Breakdown (TDDB)

5.3 Positive Bias Temperature Instability (PBTI)

5.4 Conclusions

5.5 References

5.1 Introduction

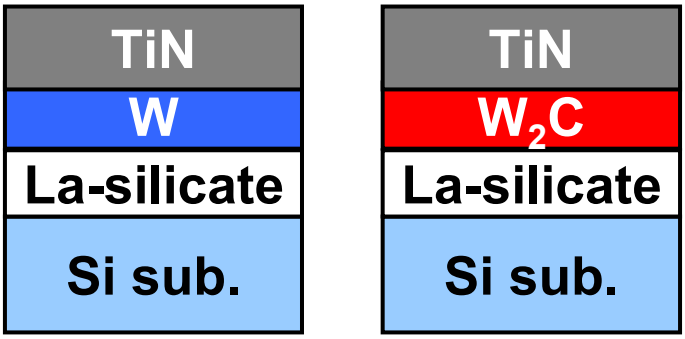
With the scaling of the CMOS technology and the associated gate oxide thickness, the reliability of the gate oxide has become a major barrier for reliable circuit design in nano-scaled devices. As shown in Table 5.1 [5.1], the average oxide electric field increases with each new technology node. All of these phenomena can have a large impact on the reliability of a circuit, right after production or during its operational lifetime. Therefore, a good understanding of gate oxide reliability is mandatory.

Table 5.1, Evolution of nanometer CMOS characteristics [5.1]

Year	L_g (nm)	V_{DD} (V)	V_{TH} (V)	EOT (nm)	E_{ox} (MV/cm)
1995	350	3.3	0.58–0.70	10.0–12.0	2.17–2.72
1998	250	1.8–2.5	0.47–0.52	6.0–7.0	1.83–3.38
2003	180	1.8	0.39–0.43	4.5–5.5	2.49–3.13
2001	130	1.2	0.35–0.40	3.5–4.0	2.00–2.43
2004	90	1.0–1.2	0.25–0.40	1.6–3.0	2.00–5.93
2007	65	1.0–1.2	0.20–0.35	1.5–2.0	3.25–6.66
2009	45	1.0–1.1	0.20–0.35	1.0–1.4	4.64–9.00
2011	32	0.9–1.0	0.20–0.35	0.8–1.1	5.00–10.0

(Iwai 1999; Bult 2000; Bravaix et al. 2009; Wu et al. 2009; Europractice 2012; International technology roadmap for semiconductors 2011)

La-silicate gate dielectrics are regarded as promising candidates for gate dielectric materials for further EOT scaling, owing to high dielectric constant (k~20), wide band-gap, and fairly nice interface properties [5.2. 5.3]. However, reliability characteristics are not well understood. In this chapter, the reliability of La-silicate gate dielectrics has been investigated by PBTI and TBBD. Figure 5.1 shows the device structure.



5.1 device structure

5.2 Time Dependent Dielectric Breakdown (TBBD)

Each dielectric material has a maximum electric field it can sustain. When a larger electric filed is applied, this leads to hard breakdown. At lower electric fields, the insulator can wearout after some time and finally break down completely. This is called time dependent dielectric breakdown (TDDB), prior oxide TDDB, a degradation process of the dielectric takes place that initiates the generation of traps in random positions inside oxide and at the interface [5.1]. Figure 5.2 shows relationship between stress time and interface state density at different stress voltage.

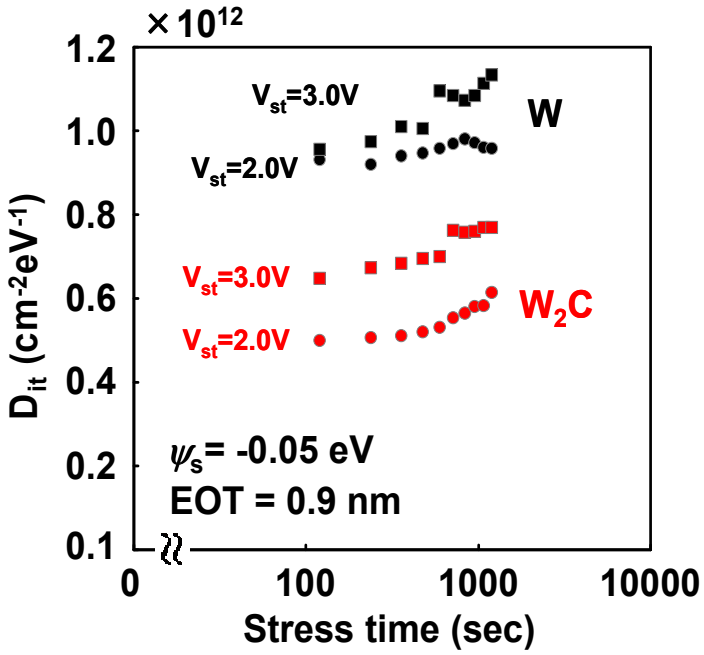
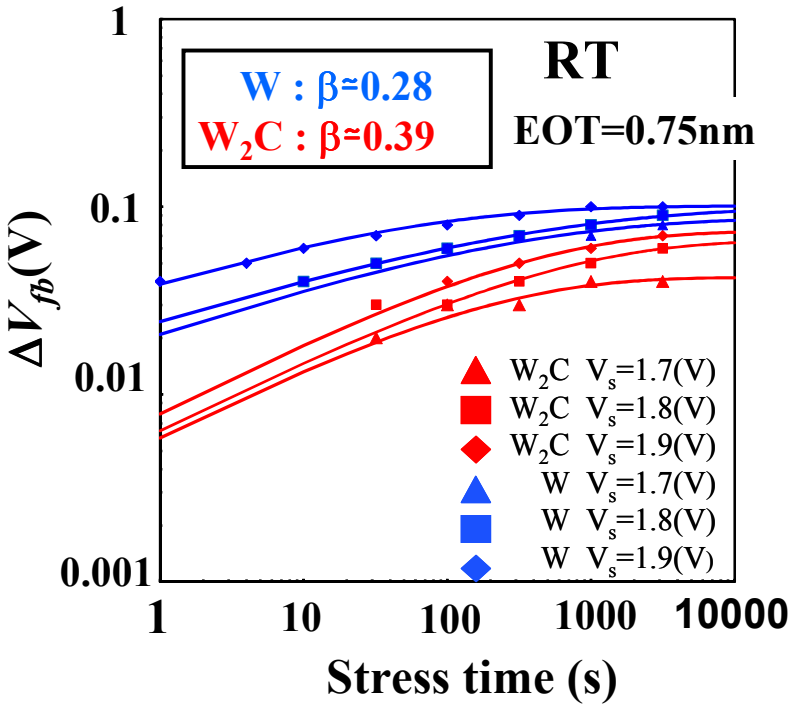


Figure 5.2 shows relationship between stress time and interface state density.

The interfacial state density (D_{it}) can be estimated using conductance method from C-V and current density-voltage measurements. The samples for TDDB measurement were utilized the MOS capacitors with EOT=0.9nm. W2C and W were adopted for gate electrode. Interface state density increased with increasing of stress voltage for both case, indicating electron trapped state generated La-silicate dielectrics, but W_2C gate electrode effectively suppress the interface state density.

5.3 Positive Bias Temperature Instability (PBTI)

BTI is typically observed as a V_{th} or V_{fb} shift after a bias voltage has been applied to a MOS gate at elevated temperature. In this study, Reliability of La-silicate gate dielectric was estimated by positive bias temperature instability (PBTI).



5.3 Dependence of flat band voltage shift (V_{fb}) on total stress time

Figure 5.3 shows dependence of flat band voltage shift (V_{fb}) on total stress time at various stress voltage, EOT=0.75nm. The sample measured at room temperature. V_{fb} was shift on total stress time at each stress bias for both cases. Comparing W gated capacitor, V_{fb} shift was suppressed by W_2C gate electrodes, indicating the capacitor with W_2C has better reliability than capacitor with W electrode. The model calculates ΔV_{fb} as function of stressing time and injected charge density using three fitting parameters [5.4]. The model equation is given by.

$$\Delta V_{fb} = \Delta V_{max} (1-\exp[-(t/\tau_0)^{\beta}]) \qquad (5.1)$$

Where, ΔV_{max}, τ_0 and β is fitting parameters. As in table 5.2, for SiO_2 gate dielectric, β is 1. Compacaing reported results on Hf-based dielectrics, La-silicate with W_2C gate dielectrics shows getter reliability.

TABLE 5.2. Comparison of model parameter β

Structure	β	Ref.
SiO_2/Si	1	[5.4]
TiN/HfO_2/SiON/n-Si	0.16~1.19	[5.5]
W/La-silicate/n-Si	0.27	This work
W_2C/La-silicate/n-Si	0.49	This work

5.4 Conclusions

Reliability of La-silicate gate dielectrics with tungsten carbide and tungsten gate electrode have been investigated by TDDB and PBTI with constant stress voltage. During constant voltage stress of the MOS capacitors, La-silicate MOS capacitors with tungsten carbide gate electrodes show better reliability due to the nice interface properties.

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Chapter 6 Summary and Conclusions

In this thesis, nano sized metal gate introduced for La-silicate for further EOT scaling. The purpose of the thesis is proper metal gate selection for scalable La-silicate gate dielectrics.

In chapter 3, a sputtering process using multi-stacking of carbon and metal thin films with subsequent annealing process to reactively form metal carbides (TiC, TaC and W_2C) has been presented. Grain sizes of the carbides are as small as 3.9, 3.2, and 1.9 nm for TiC, TaC and W_2C, respectively. Work functions of TiC, TaC and W_2C layers have been extracted as 4.3, 4.7, and 4.9 eV, respectively, relatively high values owing to oriented growth. W_2C layer formed by the presented process gives high potential to form carbides with nano-sized grain and high work function for gate electrode application.

In chapter 4, Electrical properties of La-silicate MOS devices and nMOSFET with nano-sized tungsten carbide (W_2C) gate electrode has been experimentally investigated. Interface state density (D_{it}) was suppressed by W_2C gate electrodes. Atomically flat metal/high-k and high-k/Si interfaces can be achieved by W_2C gate electrodes, where

the interface roughness extracted from TEM is 0.26 and 0.12nm, respectively. Origin of interface state density is due to La-silicate/Si interface roughness due to grains in metal gate electrode. Electron μ_{eff} showed improvements in both low and high E_{eff}, especially 163 cm^2/Vs (E_{eff}=1MV) at an EOT of 0.63 nm was achieved, owing to lower D_{it} and reduced roughness scatterings.

In chapter 5, Reliability of La-silicate with different gate electrodes, such as tungsten carbide and tungsten, was measured first time by TDDB and PBTI. Better reliability was obtained by nano sized W_2C gate electrode, presumably duo to nice interface properties.

Publications and Presentations

Publications (first author):

[1] K. Tuokedaerhan, R. Tan, K. Kakushima, P. Ahmet, Y. Kataoka, A. Nishiyama, N. Sugii, H. Wakabayashi, K. Tsutsui, K. Natori, T. Hattori, H. Iwai, Stacked sputtering process for Ti, Ta, and W carbide formation for gate metal application, Appl. Phys. Lett., Vol. 103, pp: 111908, 2013.

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Presentation at international conference and symposium (first author):

[1] K. Tuokedaerhan, T. Kaneda, M. Mamatrishat, K. Kakushima, P. Ahmet, K. Tsutsui, A. Nishiyama, N. Sugii, K. Natori, T. Hattori, H. Iwai. Impact of annealing ambient for La_2O_3/Si capacitor. G-COE PICE international symposium and IEEE EDS mini colloquium on Advanced Hybrid Nano Devices: Prospects by World's Leading Scientists. Tokyo Institute of Technology, Japan, October 4-5, 2011.

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Presentation at domestic conference (first author):

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