論文 / 著書情報
Article / Book Information

題目(和文)	La-silicateゲート絶縁膜の薄膜化を可能とする微結晶金属ゲート電極の研究
Title(English)	A Study on Metal Gate Electrodes with Nano-Sized Grains for Scalable La-silicate Gate Dielectrics
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論 文 要 旨

THESIS SUMMARY

専攻： Department of	物理電子システム創造　専攻	申請学位（専攻分野）： Academic Degree Requested	博士 Doctor of　（　工学　）
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要旨（英文 800 語程度）
Thesis Summary（approx.800 English Words ）

Downscaling of the MOSFET has been the driving force for circuit evolution. Feature size of MOSFET becomes smaller and smaller, billions of CMOS transistors are integrated on a single chip. However, power consumption caused by leakage current increased to unacceptable level. Therefore, new materials and new structures in MOSFET have been introduced to solve these issues. High-k gate dielectrics have enabled continuous scaling in CMOS devices by increasing the capacitive coupling of gate electrode to the channel which eventually suppresses the short channel effects, while reducing the gate leakage current. Considering further equivalent oxide thickness (EOT) scaling down to 0.45 nm, which is required in the year of 2026 from ITRS roadmap, high-k materials should be directly in contact with Si channels. Some of attempts to achieve direct contact of high-k on Si channels have been proposed so far; those include precise oxygen partial pressure controlled process and a thermal process to reduce the interfacial layer by incorporating additional elements in the metal gates. In addition to these processes, La-silicate can be in direct contact with Si channels by means of silicate reactions between La_2O_3 layer and Si channel. The prominent features of La-silicate are that the structure is amorphous and the silicate reaction does not show any channel surface orientation dependency, which are advantageous for scaled devices with three dimensional channels. Issues in La-silicate/Si interfaces include D_{it} in the order of high 10^{11} cm^{-2}/eV, and interface roughness presented at both metal/La-silicate and La-silicate/Si interfaces, which results in channel mobility degradation due to La-silicate thickness variation. An experimental work has shown that metal gate materials affect the interface properties, so the impact of metal gate should be clarified. According to reports, the crystal structure and grain size of metal gates strongly impact on electrical properties of MOS devices, in terms of threshold voltage variability, metal gates with grain less than 5nm or amorphous are preferable. Therefore, in this study, metal gate electrodes with nano-sized grains for scalable La-silicate gate dielectrics were experimentally investigated.

Novel sputtering processes have been introduced to form nano-sized metal gate. Multi-stacking of carbon and metal thin films with subsequent annealing process to reactively form metal carbides (TiC, TaC and W_2C) has been presented. Grain sizes of the carbides are as small as 3.9, 3.2, and 1.9 nm for TiC, TaC and W_2C, respectively. Work functions of TiC, TaC and W_2C layers have been extracted as 4.3, 4.7, and 4.9 eV, respectively, relatively high values owing to oriented growth. W_2C layer formed by the presented process gives high potential to gate electrode application in terms of grain size and oriented growth for scaled devices.

Electrical properties of La-silicate MOS devices and nMOSFET with nano-sized tungsten carbide (W_2C) gate electrode has been experimentally investigated. Interface state density (D_{it}) was suppressed by W_2C gate electrodes. Atomically flat metal/high-k and high-k/Si interfaces can be achieved by W_2C gate electrodes, where the interface roughness extracted from TEM is 0.26 and 0.12nm, respectively. Origin of interface state density is due to La-silicate/Si interface roughness due to grains in metal gate electrode. Electron μ_{eff} showed improvements in both low and high E_{eff}, especially 163 cm^2/Vs (E_{eff}=1MV) at an EOT of 0.63 nm was achieved, owing to lower D_{it} and reduced roughness scatterings.

Reliability of La-silicate with different gate electrodes, such as tungsten carbide and tungsten, was measured by TDDB and PBTI. Better reliability was obtained by nano sized W_2C gate electrode owing to atomically flat high-k/Si interface.

備考 ： 論文要旨は、和文 2000 字と英文 300 語を 1 部ずつ提出するか、もしくは英文 800 語を 2 部提出してください。
Note : Thesis Summary should be submitted in either a copy of 2000 Japanese Characters and 300 Words (English) or 2 copies of 800 Words (English).