

論文 / 著書情報
Article / Book Information

題目(和文)	誘電体/半導体と半導体ヘテロ接合界面における界面トラップおよび界面近傍のバルクトラップに関する研究
Title(English)	A study on interface traps and near interfacial bulk traps at the interfaces of dielectric/semiconductor and semiconductor heterojunction
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出典(和文)	学位:博士(工学), 学位授与機関:東京工業大学, 報告番号:甲第9533号, 授与年月日:2014年3月26日, 学位の種別:課程博士, 審査員:岩井 洋,名取 研二,片岡 好則,筒井 一生,若林 整,杉井 信之,西山 彰,角嶋 邦之,Yi Shi,Liu Ming
Citation(English)	Degree:Doctor (Engineering), Conferring organization: Tokyo Institute of Technology, Report number:甲第9533号, Conferred date:2014/3/26, Degree Type:Course doctor, Examiner:,,,,,,,,,
学位種別(和文)	博士論文
Type(English)	Doctoral Thesis

Doctoral Thesis

A study on interface traps and near interfacial bulk traps at the interfaces of dielectric/semiconductor and semiconductor heterojunction

誘電体/半導体と半導体ヘテロ接合界面における界面トラップおよび界面近傍のバルクトラップに関する研究

by

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A dissertation submitted to

Department of Electronics and Applied Physics,

Interdisciplinary Graduate School of Science and Engineering,

Tokyo Institute of Technology

for the degree of doctor of engineering

Spring, 2014

Acknowledgements

First and foremost, I would like to express deepest gratitude to my advisor Prof. Hiroshi Iwai from Tokyo Institute of Technology (TIT) for all of his dedicated guidance and attentive support on my studies and life. He also provides me many invaluable chances for participating research program in world-leading universities/institutes outside TIT, which greatly broaden my horizon and deepen my interest on my research field.

I am also deeply indebted to Associate Prof. Kuniyuki Kakushima of TIT, who intelligently and patiently guides me to overcome many crucial challenges in my laboratory studies and daily life through my Ph.D. journey.

Likewise, I am very grateful to Prof. Takeo Hattori, Prof. Kenji Natori, Prof. Kazuo Tsutsui, Prof. Hiroshi Wakabayashi, Prof. Nobuyuki Sugii, Prof. Akira Nishiyama, Prof. Yoshinori Kataoka, and Prof. Parhat Ahmet from TIT for their tireless mentoring and valuable advices.

Besides, I sincerely acknowledge Prof. Keisaku Yamada, Prof. Kenji Ohmori, Prof. Masaaki Niwa, and Dr. Wei Feng from Tsukuba University for their strong guidance on fabrication and characterization multi-gate MOSFETs devices after I joined the Tsukuba Nanotechnology Human Resource Development Program (honors graduate program), Tsukuba University.

Additionally, I would like to express my appreciation to Prof. Guido Groeseneken, Dr. Aaron Thean, Dr. Dennis Lin from IMEC and Prof. Yuan Taur from University of California, San Diego, for their cordial guidance on characterizing the oxide traps in III-V MOS capacitors during my intern at IMEC. I also indebted to many members of the LDD team of IMEC for many fruitful discussions and kind assistance.

I also significantly benefited from the kindest help from Ms. Akiko Matsumoto and Ms.

Masako Nishizawa from Iwai/Kakushima laboratories, Prof. Yogaku Iwamoto, and Ms. Yumiko Yuzawa from the Innovative Platform for Education and Research (IPER) of TIT, Prof. Kikuo Yamabe, Prof. Kiyoshi Asakawa, Prof. Yasuhiro Horiike, Ms. Namiko Suzuki, Ms. Midori Hirano, and Mr. Masaya Oouchi from the honors graduate program of Tsukuba University. Due to their kind arrangements, I could conduct my studies smoothly at TIT and Tsukuba University, and also participate in an intern at IMEC. I would also like to thank Dr. Daniel Berrar from IPER of TIT for proofreading my journal publications.

I would also like to express my deep gratitude to all of other research staff and student members in Iwai/Kakushima Lab for their help from many aspects, and I will always recall my time at Japan with fondness.

I would also like to gratefully appreciate Prof. Ming Liu (The Institute of Microelectronics of Chinese Academy of Sciences), Prof. Yi Shi (Nanjing University), Prof. Zhenchao Dong (University of Science and Technology of China), Prof. Hei Wong (City University of Hong Kong), for evaluating the qualification of this thesis and their valuable advices.

Lastly, many thanks to my parents and all of my family members for their constant support and firm encouragement.

Abstract

In order to avoid CMOS down-scaling limit due to the short-channel effect, multi-gate structure, such as fin-FETs or Tri-gate has been introduced. In addition, MOSFETs with new channel materials such as InGaAs (III-V) and Ge are studied for low power application under low voltage. Also, HEMT (High Electron Mobility Transistor) devices using AlGaIn/GaN hetero-junction for the channel are being developed for power and high-frequency applications.

For the development of these emerging device technologies, it is important to accurately evaluate the distribution of interface and near-interface traps at the gate dielectrics/semiconductor interfaces and the semiconductor hetero-junction interfaces and thus, to understand the behavior of those traps. In this thesis, the results of the systematic studies for the distribution of interface and near-nterface traps at SiO₂/Si interfaces with fin structure, high-*k*/InGaAs interfaces, and AlGaIn/GaN hetero-interfaces are described. We have proposed methodologies for trap characterization and revealed in-depth understanding of the distributions, origins, species, and trapping mechanisms. These methodologies and discoveries can be also easily extended for studying other dielectric/semiconductor interfaces and semiconductor hetero-interfaces, and thus provide a guideline for trap characterization for future development of advanced FETs.

In particular, following characterizing methodologies were proposed: (1) extraction of trap densities in the different regions of fin surface by the measurement of trap densities with different fin width, (2) extraction of near-interface traps (or border traps) for high-*k*/III-V MOS structures, from the *C-V* characteristics measured at different temperatures, and (3) extraction of the distribution and species of the interface traps by comparative study on conductance spectra of AlGaIn/GaN hetero-junctions with different electrodes.

The major results are listed as follows; At the SiO₂/Si interface with fin structure, a high concentration of interface traps tend to locate at the corners. In high-*k*/III-V MOS systems, there are a large amount of electrically active oxide border traps, whose concentration is likely to increase with increasing energy level and distance from the interface into the oxide. These traps seem to be caused by accumulated defectives during high-*k* material growth. Besides, the trapping process of oxide border traps is found to be caused by thermal activation. At last, for AlGaIn/GaN hetero-interfaces, it is confirmed that there are no distributed bulk traps in the near interfacial region of the hetero-interface. Besides, the different properties of deep trap levels and shallow trap levels at the hetero-interface are also presented.

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Symbols and Abbreviation

A

ALD, atomic layer deposition

AC, alternating current

B

BT, border traps or near interfacial bulk traps

C

CMOS, complementary metal-oxide-semiconductor

CP method, charge-pumping method

C , capacitance

C_b , barrier layer capacitance

C_m , measured capacitance

C_s , substrate capacitance

C_{ox} , oxide capacitance

C_{it} , interface traps induced capacitance

C_{tot} , total capacitance

C_g , gate capacitance

D or Δ

DIBL, drain induced barrier lowering

D.O.S., density of states

D_{it} , density of interface states

$D_{it,top}$, density of interface states at the top wall of the fin structure

$D_{it,side}$, density of interface states at the sidewall of the fin structure

$D_{it,corner}$, density of interface states at the corner of the fin structure

ΔC_{bt} , incremental oxide border traps capacitance

ΔG_{bt} , incremental oxide border traps conductance

E

E_C , conduction band edge

E_V , valence band edge

E_f , Fermi energy level

E_T , Trap energy level

F

FET, field-effect transistor

f , frequency

G

G , conductance

G_m , measured conductance

G_p , parallel conductance

H or \hbar

High- k , high dielectric constant

H_{fin} , height of the fin structure

H.F., high frequency

\hbar , reduced plank constant

I

I_{ON} , on-state current

I_{OFF} , off-state current

I_{leak} , leakage current

I_{CP} , charge-pumping current

K

k , Boltzmann constant

κ , tunneling decay factor

L

L.T., low temperature

L.F., low frequency

M

MOS, metal-oxide-semiconductor

MOSFET, metal-oxide-semiconductor field-effect transistor

N

N_C , density of state in the conduction band

N_V , density of state in the valence band

N_d , donor impurity density

N_a , acceptor impurity density

n_s , carrier density at the semiconductor surface

N_{bt} , volume density of oxide border traps

P

$P_{dynamic}$, dynamic power consumption

P_{static} , static power consumption

P_{SP} , spontaneous polarization

P_{PE} , piezo-electric polarization

Q

q , element charge

S or σ

S.S., subthreshold slope

SCE, short channel effect

SOI, silicon-on-insulator

$\sigma_{n,p}$, capture cross-section of electrons/holes

σ_s , surface potential parameters

T or τ

T , temperature

t_{ox} , oxide thickness

τ_{it} or τ_0 , the time constant of the interface trap

τ_{bt} , the time constant of the border trap

V

V , voltage

V_{dd} , supply voltage

V_g , gate voltage

V_{th} , threshold voltage

v_{th} , thermal velocity

W or w

W_{fin} , width of the fin structure

W , angular frequency

X

X_P , probing depth

$X_{P, \max/\min}$, maximum or minimum probing depth

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Besides, the vertical dash-dot lines in (d) show the evaluated maximum probing depth, $X_{P,max}$ at different temperatures using Eq. (3) with $\kappa = \kappa(E) = 5.09 \text{ nm}^{-1}$, $f = 100 \text{ Hz}$ and the τ_0 shown in (c), and the horizontal dash lines in (d) shown the N_{bt} extracted at different temperatures by assuming uniform N_{bt} spatial distribution. Additionally, except the influence of border traps, that of series resistance is also considered in the distributed model by using the parameters of $R_s = 6.6 \times 10^{-3} \Omega \cdot \text{cm}^2$ and $G_{Ln} = 1.2 \times 10^{-4} \text{ S/cm}^2$.

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Chapter 5:

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Chapter 1: Introduction

In order to avoid CMOS down-scaling limit due to the short-channel effect, multi-gate structure, such as fin-FETs or Tri-gate has been introduced. In addition, MOSFETs with new channel materials such as InGaAs (III-V) and Ge are studied for low power application under low voltage. Also, HEMT (High Electron Mobility Transistor) devices using AlGaIn/GaN hetero-junction for the channel are being developed for power and high-frequency applications. However, the distribution of interface and near-interface traps at the gate dielectrics/semiconductor interfaces and the semiconductor hetero-junction interfaces in these emerging devices are still lack of investigation.

In this thesis, in order to provide a guideline for trap characterization for future development of advanced FET, we have proposed methodologies for trap characterization and revealed in-depth understanding of the distributions, origins, species, and trapping mechanisms gate dielectrics/semiconductor interfaces and the semiconductor hetero-junction interfaces.

1.1 Moore's law and Dennard Scaling

1.1.1 Moore's law – history and current status

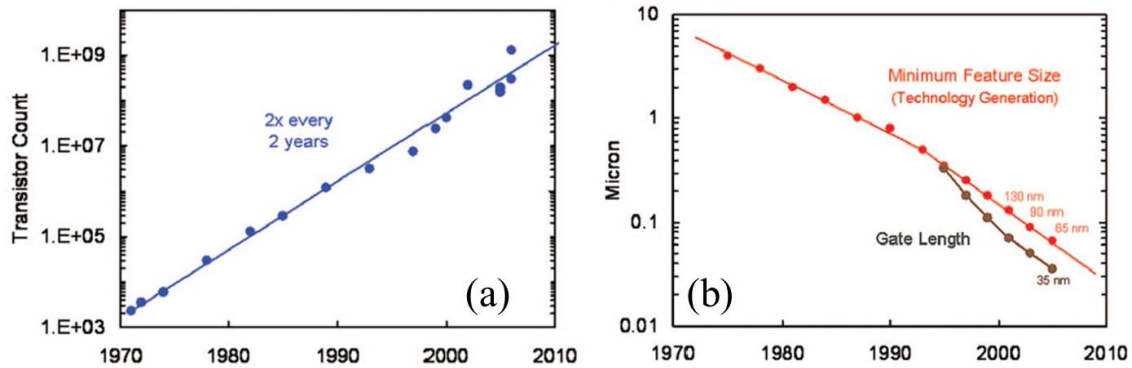


Fig. 1.1 The evolution of total transistor count on a chip (a) and the feature size of logic technology (b) of Intel microprocessors [1.4]

The relentless development of Si-based large-scale-integrated circuits (LSIs), in the past four decades has revolutionized the information technology, and contributed to far-reaching impacts on the modern society [1.1, 1.2]. This tremendous progress is achieved on the scaling of LSIs' technology driven by Moore's law, which predicted that the transistor density would double every 24 months [1.3]. For instance, **Figure 1.1(a)** shows the evolution of total transistor count on a chip of Intel microprocessors released from 1970 to 2010 [1.5]. The transistor count on a chip has approximately increased by a factor of two every two years in the past four decades, which also allows dramatic improvement on operating frequency of the microprocessors. This is mainly achieved by scaling the transistors which keeping the transistor lateral-to-vertical aspect ratio according to the scaling rule proposed by Robert Dennard et al. [1.5] as described in the following section. **Figure 1.1(b)** shows the aggressive scaling of the feature size for logic application in Intel [1.5]. The scaling trend of transistors still persists till today and the schedule in which the transistor density increases by 2X every 24 months is still generally recognized by the roadmap made by the industry. Nowadays, the 22 nm generation technology has already been ramped into mass production [1.6].

1.1.2 Dennard scaling law and its challenges

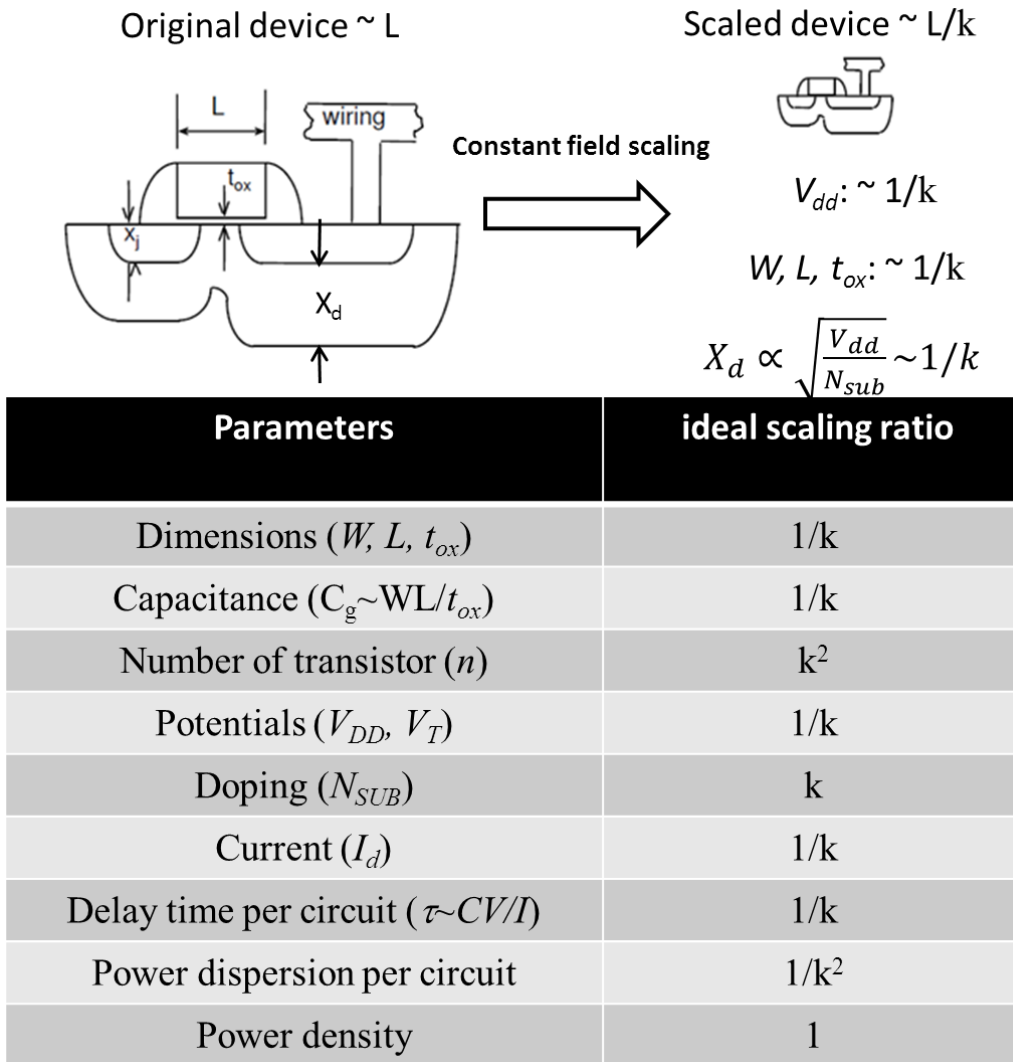


Fig.1.2 Illustration of the constant-field scaling theory of MOSFET proposed by Dennard et al. in 1974 [1.5]

The ideal scaling of metal-oxide-semiconductor field-effect transistors (MOSFETs), which results in smaller device size and improved device performance, can be achieved by the constant-field scaling theory proposed by Dennard et al. [1.5], as shown in **Fig.1.2**.

According to this method, in order to keep constant electric field in the channel, all of the dimensional parameters, including gate length (L), channel width (W), thickness of the gate oxide (t_{ox}), and the junction depth (X_j), are scaled by a factor of k . The supply voltage (V_{dd}) and threshold voltage (V_{th}) are also scaled by a factor of k . Besides, to simultaneously scale the depletion depth (X_d) by same ratio, the doping concentration (N_{sub}) in the channel is increased by a factor of k . Besides, the drain current I_d , which can be from Eq. 1.1.1 as below [1.6], is also scaled by a fact of k .

$$I_d = \mu C_{ox} \frac{W}{L} (V_{gs} - V_{th} - \frac{V_{ds}}{2}) V_{ds} \dots \dots \text{Eq.(1.1.1)}$$

Here, μ is the mobility, C_{ox} ($\sim 1/t_{ox}$) is the oxide capacitance, V_{gs} and V_{ds} are the gate-to-source and the drain-to-source voltage, respectively.

As a result, the delay time τ ($\sim CV/I$) is scaled to $1/\alpha$, which indicates that the whole circuit can be operated at faster speed or higher frequency. More importantly, if the ideal constant-field scaling can be achieved, the power for switching the transistor can be scaled to $1/k^2$. Because the transistor density is increased to k^2 due to the laterally scaling of the transistor dimensions, the power density can be kept constant after scaling. Therefore, it can be seen that high operational speed can be achieved without increasing the power density in the ideal case.

However, it should be noticed that the Dennard scaling rules are based on following assumptions. First, it ignored the impact of transistor sub-threshold leakage on overall power consumption. Secondly, it assumed that the oxide thickness can be continually scaled. Lastly, it assumed that the channel doping concentration can be continually increased.

In the early days of MOSFET scaling around 1970's, the dimensions and the operational voltages of MOSFETs were relatively large and the ideal Dennard scaling rules could be well achieved. However, after about 40 years' aggressive scaling, dimensions of advanced MOSFETs have shrunk to the deep sub-micrometer region and the aforementioned

assumptions are not valid any more. The limitations of the traditional scaling rules are discussed in details as below.

(a) Power-constrained supply voltage scaling

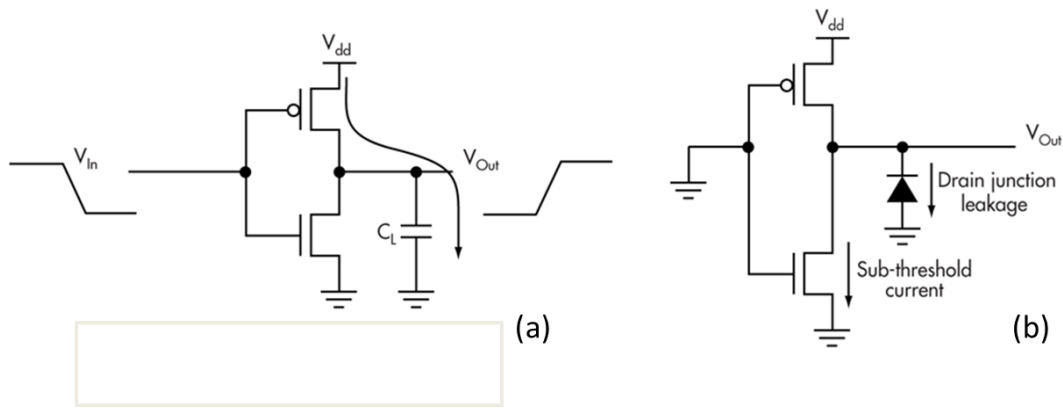


Fig. 1.3 Illustration of the main origin of the dynamic power (a) and the static power (b) of a CMOS inverter.

The CMOS inverter is one of the fundamental components for constructing LSIs, in which both of n-type and p-type MOSFETs are complementarily used. The power consumption of a CMOS inverter can be divided into two types, dynamic and static, as illustrated in **Fig. 1.3**. As shown by **Fig. 1.3 (a)**, the dynamic power mainly originates from the energy that is used to charge and discharge the load capacitance. It can be derived that the energy per transition for charging or discharging can be given by:

$$Energy / transition = C_L \times V_{dd}^2, \text{ Eq. (1.1.2)}$$

Therefore, the dynamic power can be given by:

$$P_{dynamic} = Energy / transition \times frequency = C_L \times V_{dd}^2 \times f, \text{ Eq. (1.1,3)}$$

On the other hand, the static power is mainly associated with the leakage current, such as sub-threshold leakage and drain junction leakage, as shown in **Fig. 1.3 (b)**. It can be given

by:

$$P_{static} = V_{dd} \times I_{leak}, \text{ Eq. (1.1.4)}$$

Thereby, the total power consumption can be given by:

$$P = P_{dynamic} + P_{static} = C_L \times V_{dd}^2 \times f + V_{dd} \times I_{leak} \text{ Eq. (1.1.5)}$$

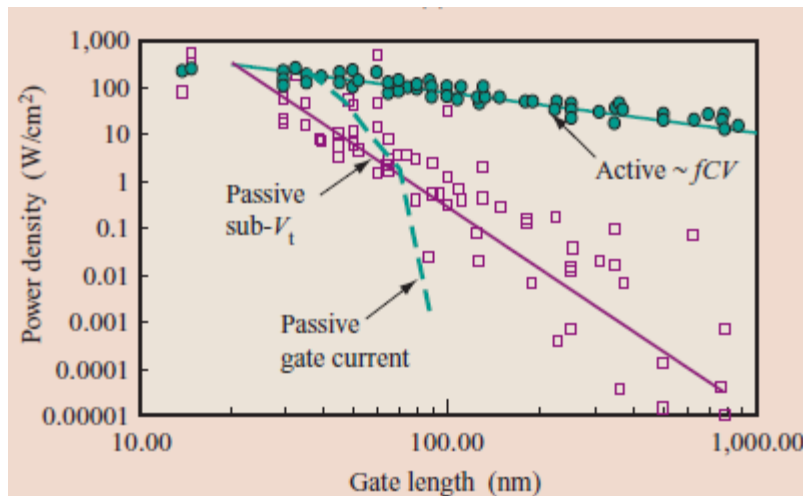


Fig. 1.4 Evolution of the power density of CMOS circuits as a function of gate length [1.7]

Ideally, the static power of the CMOS inverter should be very low, which is also widely recognized as one of the most important advantages of the CMOS technology, because n-MOSFET and p-MOSFET always do not switch on or off at the same time in this type of circuit. Thus the static power should be ignorable compared to the dynamic power. This is generally true for the technology generation with relatively long gate length ($\sim 1\mu\text{m}$). However, as shown by **Figure 1.4**, as the gate length scaled to the $< 100\text{ nm}$ region, it can be seen that the static power significantly increases with decreasing gate length. It is also noteworthy that the static power even may even surpasses the dynamic power when the gate length scaled to around 10 nm . Considering the extremely high transistor density, the increased static power of the LSIs constructed by highly scaled transistors may result in huge power consumption. In addition, the huge power consumption also considerably rises

the temperature of the chip, which may leads to several failure mechanisms and degrade the reliability of the circuit [1.8]. In short, to continually the CMOS scaling trend, suppressing the power consumption, especially the static power consumption, is of significant importance.

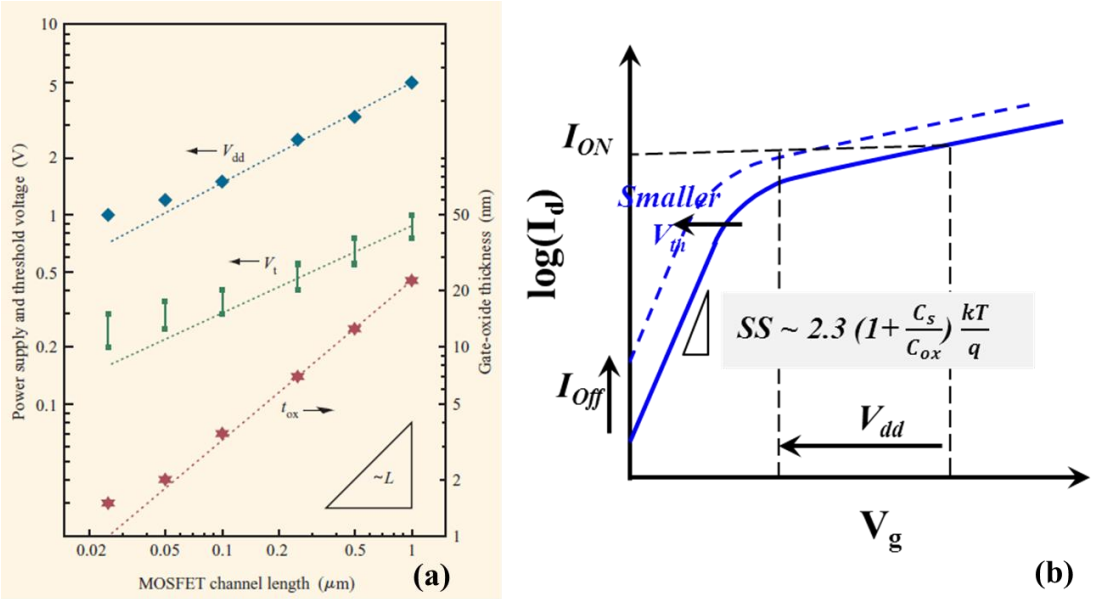


Fig. 1.5 (a) Power-supply voltage (V_{dd}), threshold voltage (V_{th}) and gate-oxide thickness (t_{ox}) as a function of channel length for CMOS logic technologies [1.9], and (b) schematic drain current-gate voltage (I_d - V_g) relationships with different V_{dd} and V_{th} with illustration of the increased off-state current (I_{off}) after V_{dd} or V_{th} scaling.

Figure 1.5 (a) shows the history and trends of the power-supply voltage, threshold voltage as a function of channel length for CMOS logic technologies, adopted from Ref. [1.9]. It can be seen that when the channel length was scaled from $\sim 1\mu\text{m}$ to $\sim 0.1\mu\text{m}$, the V_{dd} was scaled with a smaller rate compared to that of the scaling of the channel length. Besides, V_{th} was scaled even slower that of the scaling of V_{dd} . Furthermore, as the channel length was scaled to sub-100 nm region, the scaling of V_{dd} and V_{th} almost got saturated. The underlying mechanism that hinders the scaling of V_{dd} and V_{th} is shown in **Fig. 1.5 (b)**. In order to scale V_{dd} without sacrificing on-state current, I_{ON} , V_{th} also has to be scaled at the same time.

However, it can be seen that the off-state current, I_{OFF} , increases logarithmically with decreasing V_{th} . At the early stage of CMOS scaling, the sub-threshold leakage was relatively low and its contribution to the chip total power consumption was ignorable. Considering relatively high sub-threshold leakage current and transistor density nowadays, it is very difficult to further continually scale the V_{th} and V_{dd} . To overcome this impediment, novel devices with new operational principle allowing ultra-steep sub-threshold slope, or novel channel design having enhanced carrier's transportation, are under development.

(b) The limitation of scaling the thickness of gate dielectrics

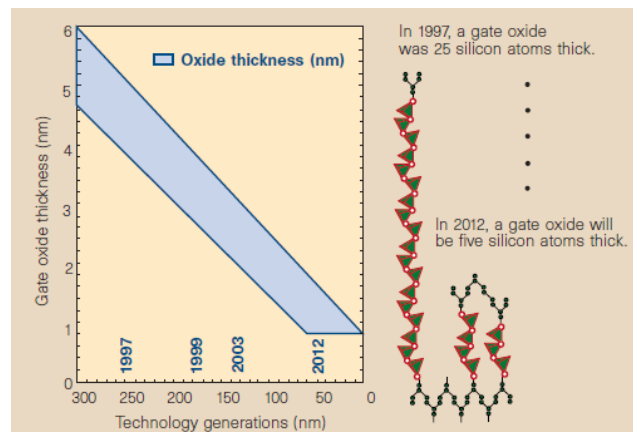


Fig. 1.6 (a) The road map for scaling of the gate oxide predicted by the semiconductor Industry Association (SIA), USA, in 1997 [1.10], and (b) Schematic of the evolution of the SiO₂ gate oxide [1.11].

The SiO₂ gate insulator is considered as one of key points that contribute to the unprecedented success of the Si MOSFETs as the workhorse for modern microelectronic industry. It owns high resistance and high breakdown voltage. Besides, it can be easily grown on Si substrate by thermal oxidation process with abrupt interface and few amounts of active interface traps. However, **Fig. 1.6 (a)** the roadmap predicted by SIA in 1997 (note that the actual scaling trend is more aggressive than this), the technology nodes below 50

nm require that the thickness of SiO₂ should be scaled to 1.3 nm. As shown by the schematic image of the atomic structure of the SiO₂ layer in **Fig. 1.6 (b)**, a 1.3-nm-thick SiO₂ layer contains only five layers of atomic. While the top and bottom layers are used to connect the Poly-Si gate and the Si channel, only three atomic layers serve as the insulating layer, which is considering the minimum requirement for effective suppression of the tunneling current between gate and substrate. It means that the thickness scaling of the SiO₂ gate oxide had already been reached now. To tackle this challenge, the SiO₂/poly-Si gate stack has to be replaced by the high-*k*/metal-gate configuration, as introduced in the later sections.

(c) The limitation of increasing the channel doping concentration

In Dennard's law, another very important enabling factor for continuing the constant-field scaling is that continual increasing the channel doping concentration. However, the channel doping concentration cannot be too high mainly because of two reasons: (1) the carrier mobility can be severely degraded due to increased impurity scattering, and (2) the drain junction leakage may considerably increases due to direct band-to-band tunneling.

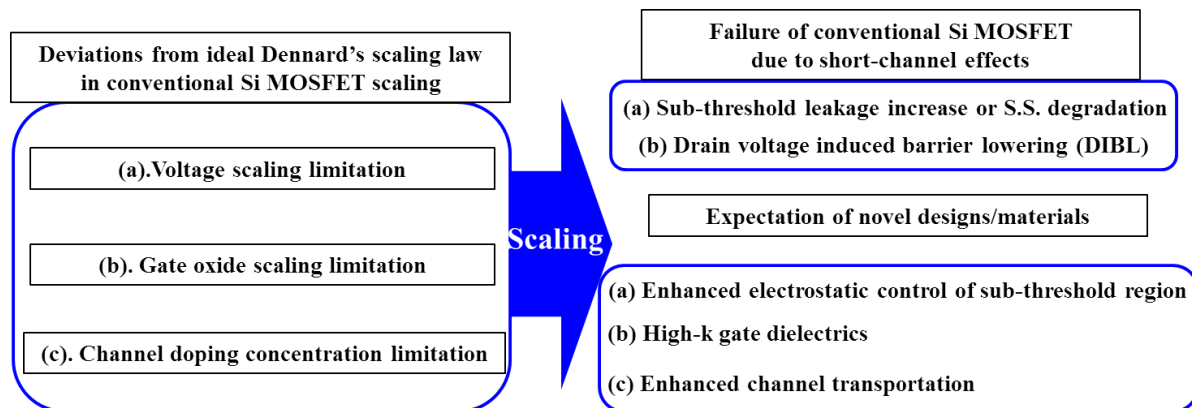


Fig. 1.7 Illustration of the deviations from ideal Dennard’s scaling law in scaling the conventional Si MOSFETs and their influences: conventional Si MOSFET will finally fail as scaling continues due to the short channel effects and novel design/materials are expected.

Here, we summarized the aforementioned limitations that deviate the scaling of conventional Si MOSFET from the ideal scaling rules: (a) the limitation of voltage scaling due to the power concern, (b) the limitation of scaling the thickness of SiO₂ gate oxides, and (c) the limitation of increasing the channel doping concentration, as shown in the left-hand side in **Fig. 1.7**. In the extremely scaled devices, these limitations lead to (a) the horizontal electric field from source to drain is increased, (b) the electrostatic control of channel by gate is weakened, and (c) the space charge region cannot be sufficiently scaled as the same ratio of the scaling of the dimensions of the devices. These effects due to the deviations from the ideal scaling rules induce so-called “short-channel effects”, including the increase of the sub-threshold leakage, or the S.S. degradation, and the drain induced barrier lowering (DIBL), as shown by the upper part of the right-hand side in **Fig. 1.7**.

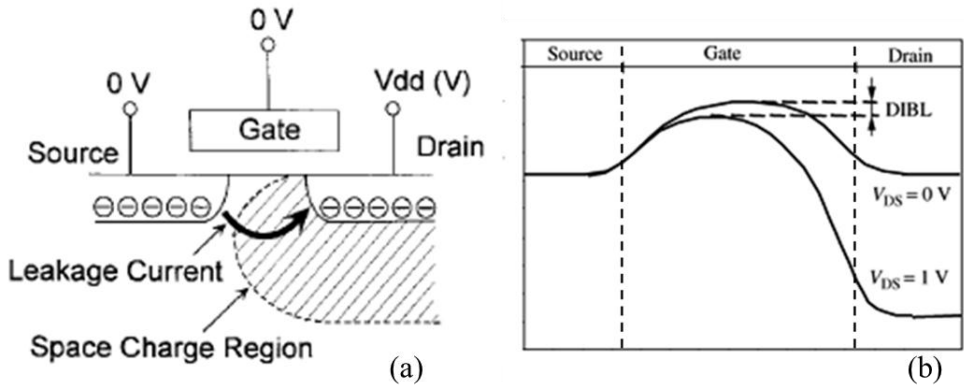


Fig.1.8 Short channel effects in n-MOSFETs: (a) Schematics of the leakage current in sub-threshold region, [1.1] and (b) the band diagram of source/channel/drain with illustration of the drain induced barrier lowering (DIBL) effect.

Figure 1.8 shows two key device degradation mechanisms as channel length decreases known as short channel effects: (a) increasing in sub-threshold leakage, or degradation of S.S., and (b) DIBL effects, as described in details as follows. In generally, the short channel effects are caused by two facts that violated the constant-field rule: (1) the horizontal electric field from source to drain substantially increased and thus drain electric-field may penetrate to the source side, and (2) the vertical electric field is weakened as thus the gate-to-channel control degrades. Simply put, the drain take over the control of the channel from the gate as channel length decreases.

The underlying mechanism of increased sub-threshold leakage in short-channel devices is schematically shown in **Fig. 1.8 (a)**. It is mainly caused by the fact that the space charge region cannot be scaled as the same ratio as that of scaling of the device dimensions. As a result, if the large space charge region in the drain junction caused by the reverse drain bias sufficiently approaches the source, the carriers in source can directly inject from source to drain and thus a leakage path beneath the surface channel is created. This effect contributes to additional sub-threshold leakage current and can significantly degrade the S.S. characteristic.

The other short channel effect known as DIBL is mainly caused by penetration of the drain electric-field to the source sides, as shown by **Fig. 1.8 (b)**. Ideally, in long channel devices, the barrier between the source and the channel should be completely controlled by the gate electrode. However, in extremely scaling devices, the barrier can be lowered by drain electric-field. This effect leads to (1) increasing sub-threshold leakage, and (2) drain voltage dependent V_{th} that can further increase the sub-threshold leakage.

The short channel effects caused by the deviation from the ideal scaling rule finally cause the failure of convention Si MOSFET to continue the aggressive CMOS scaling trends. As a result, novel designs/materials have to be implanted to overcome these challenges, as summarized in the lower part of the right-hand side in **Fig. 1.7**. To continually enhance the

gate-to-channel control, multi-gate structure or high-k gate dielectrics can be adopted. To further reduce the supply voltage, one of possible solutions is adopting high-mobility channel to boost the drivability. In addition, another emerging trend to improve the performance of IC is innovatively integrated the semiconductor devices for digital applications, which need to be scaled for increasing performance, and those for non-digital applications, which do not need to be scaled at the same ratio with those for digital application. From this perspective, high performance field-effect transistors for non-digital application are also of particular importance. In the following sections, the strategy and the emerging device technologies for overcoming the current challenges faced on continuing Moore's law are discussed in details.

1.2 Overcoming the challenges faced by CMOS scaling

1.2.1 “More Moore” and “More than Moore”

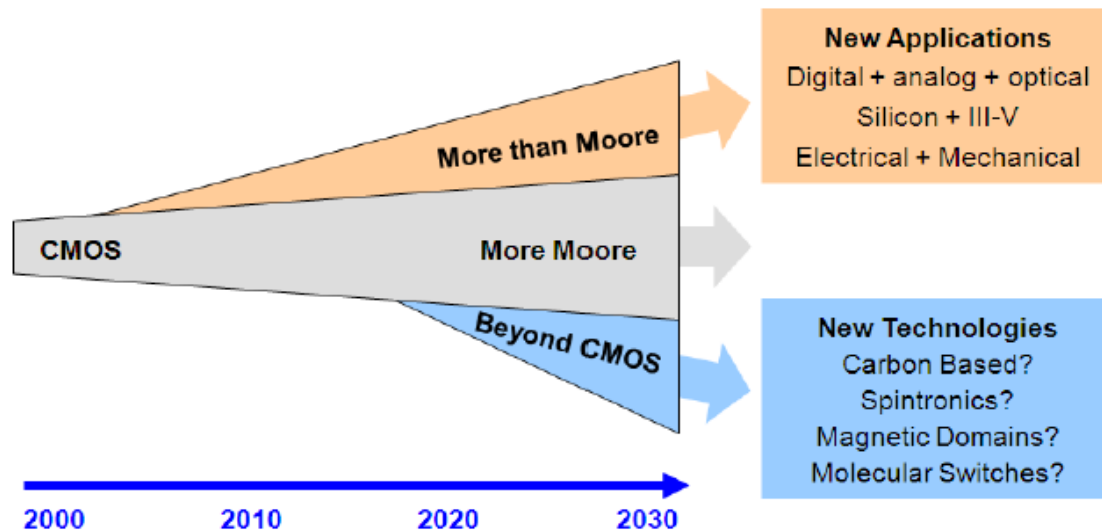


Fig. 1.9 Future technology directions, including “More Moore”, “More than Moore”, and “Beyond CMOS”, to further improve the performance of LSIs. [1.12]

As discussed in the previous sections, CMOS scaling is facing critical challenges in deep sub-micrometer region. To further improve the IC’s performance, there are three main directions, including “More Moore”, “More than Moore”, and “Beyond CMOS”, as illustrated by **Fig. 1.9**. In further, CMOS scaling is still the mainstream driven by Moore’s law, namely “More Moore”. To continue the progress in this direction, novel structures/materials, such as multi-gate configuration, high- k /metal gate, and high-mobility channel, have to be integrated into conventional bulk planar MOSFET. The second trend is so called “More than Moore”. It is characterized by functional diversification of semiconductor-based devices, and innovative integration of the non-digital functionalities that do not necessarily scale at the same rate as the one required by the digital circuits. To develop this technology trend, novel semiconductor devices for analog/RF, high power electronics, sensors and etc., such as III-nitride based HEMT, are expected. The last trend is the

“Beyond CMOS”, which emphasize on developing electronic systems based on revolutionary concept that is completely different with that of conventional CMOS technology. Examples includes carbon-based electronics, spintronics, molecular switching devices and etc.

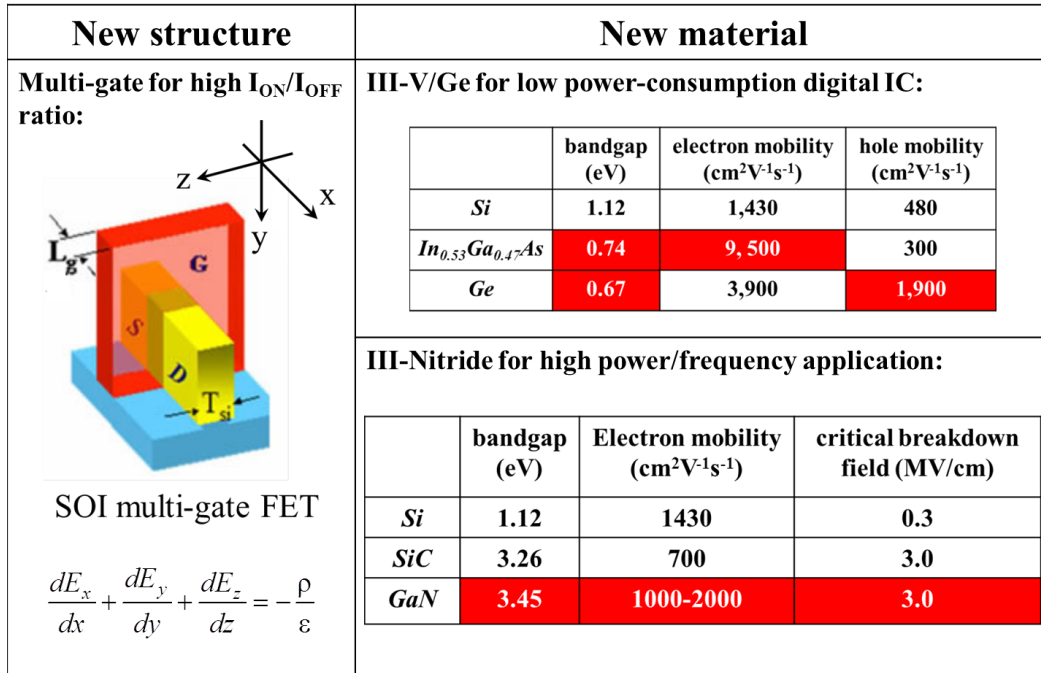


Fig. 1.10 Representative new structure/material technology for novel field-effect transistors to continue CMOS scaling and diversify functionality.

Our study mainly focuses on the new structure/material technology for novel FETs to continue CMOS scaling and diversify functionality for “More Moore” and “More than Moore”. Specifically, as shown by **Fig. 1.10**, from structure prospective, multi-gate structure can be adopted to enhance the electrostatic control of the channel. From material perspective, compared to conventional Si channel, semiconductors with relatively small bandgap and high mobility, such as III-V and Ge, can be integrated for low power-consumption digital IC. On the other hand, semiconductors with relatively large bandgap and high mobility, such as III-nitride, are attractive for high-power and high-frequency application. The principles and features of these technologies are detailed as follows.

1.2.2 Multi-gate FETs for gate-to-channel electrostatic control

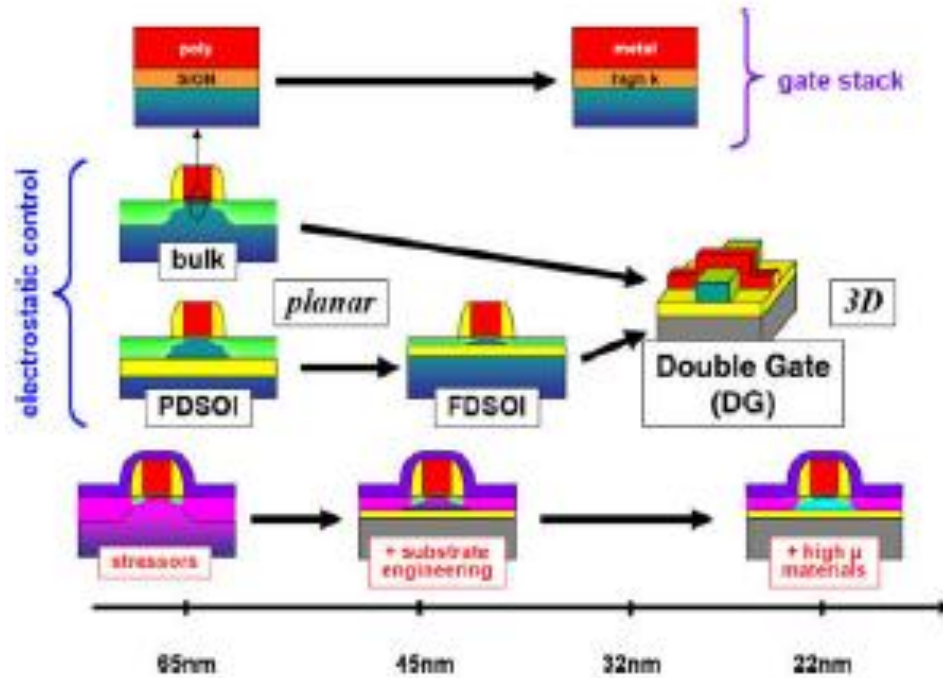


Fig. 1.11 Structure and technology innovation for MOSFET, adopted from H. Iwai [1.2].

Figure 1.11 [1.2] shows the structure innovation for MOSFET to address SCEs by increasing electrostatic control. The three-dimension (3D) channel with gate-all-around (GAA) structure is considered to be the ideal structure for ultimate scaling because it's excellent gate-to-channel electrostatic control [1.14, 1.15]

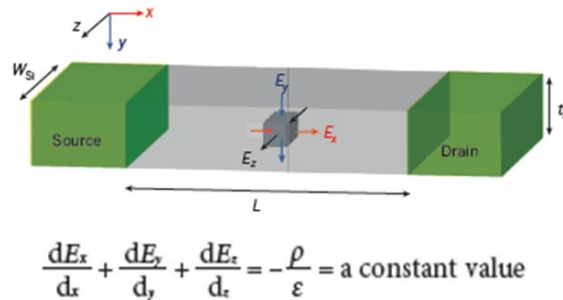


Fig. 1.12 Enhanced electrostatic gate control of the channel can be achieved by adopting 3-D channel with multi-gate structure. After I. Ferain, et al [1.14]

Figure 1.12 illustrates the principle for enhanced electrostatic control by using the 3D channel. Considering the Poisson equation in the channel of the MOSFET in conventional planar devices, the electric field in the channel comes from (1) the horizontal electric field from the drain to source (x-direction) and (2) the vertical electric field from the gate to the channel (y-direction). Therefore, the Poisson equation in the channel can be given by:

$$\frac{dE_x}{dx} + \frac{dE_y}{dy} = -\frac{\rho}{\epsilon} \quad (1.2.1)$$

On the other hand, in a MOSFET with 3D channel as shown in **Fig. 1.11**, the vertical electric field from the gate to the channel is not only one dimensional but surrounding the channel. For a 3D channel with rectangular-like cross-sectional shape, the Poisson equation in the channel can be given by:

$$\frac{dE_x}{dx} + \frac{dE_y}{dy} + \frac{dE_z}{dz} = -\frac{\rho}{\epsilon} \quad (1.2.2)$$

By comparing Eq. (1.2.1) and Eq. (1.2.2), we see that the electrostatic control in the 3D channel is more effective than that in conventional planar devices.

Furthermore, based on the Poisson equation shown in Eq. (1.2.2) with a few assumptions, a parameter called the natural length (λ), which reflects the penetration of the drain electric field from the drain side to the source side, can be calculated, and the minimum gate length (L_g) is about seven times of λ [1.14]. Particularly, λ can be given by [1.9]:

$$\lambda = \sqrt{\frac{\epsilon_{ch}}{N\epsilon_{ox}}} t_{ox} t_{ch} \quad (1.2.3)$$

Here, ϵ_{ch} and ϵ_{ox} are the relative dielectric constants of the channel material and the oxide materials. t_{ox} and t_{ch} represent the thickness of the gate oxide and the channel. N is the number of the “effective gate number” (Planar: N=1, Double-Gate: N=2, Tri-Gate: N=3, GAA: N=4). From the Eq. (1.2.3), the penetration of the electric field from the drain to the

source can be effectively suppressed by (1) using the 3D structure channel, (2) shrinking the thickness of the channel and (3) the gate stack with ultra-thin high- k dielectric. The later issue will be further discussed in the coming section.

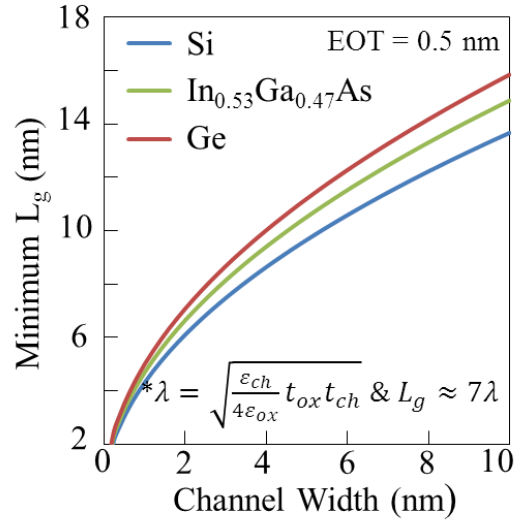


Fig. 1.13 Evaluated minimum gate length as a function of channel width for a gate-all-around MOSFET with Si, $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$, Ge channel.

In 3D MOSFET with fully-depleted channels, shrinking the dimensions of the cross-section is also a big challenge. It not only relies on the development of advanced process, but also may arouse new transportation mechanism. Here, we also estimated the minimum gate length as a function of the channel width according to Eq. (1.2.3) of a GAA MOSFET with the equivalent oxide thickness (EOT) of 0.5 nm, as shown in **Fig.1.13**. It can be seen that scaling the gate length requires aggressive scaling of the channel width. Specifically, gate length below 10 nm requires Si channel width below 6 nm. Furthermore, introduction of new channel materials, such as $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ and Ge, requires even smaller dimension because of their relatively low dielectric constants.

In addition, it is also noteworthy that in 3D channel structure, the scaling of channel width is of significant importance to realize 1D ballistic transportation [1.16]. In case of ballistic transportation, the carriers are expected to be directly injected from the source to the drain

without experiencing any scattering. Therefore, achieving 1D ballistic transportation in extremely scaled 3D MOSFET devices is highly expected for superior drivability.

1.2.3 High- k /Metal gate for EOT scaling

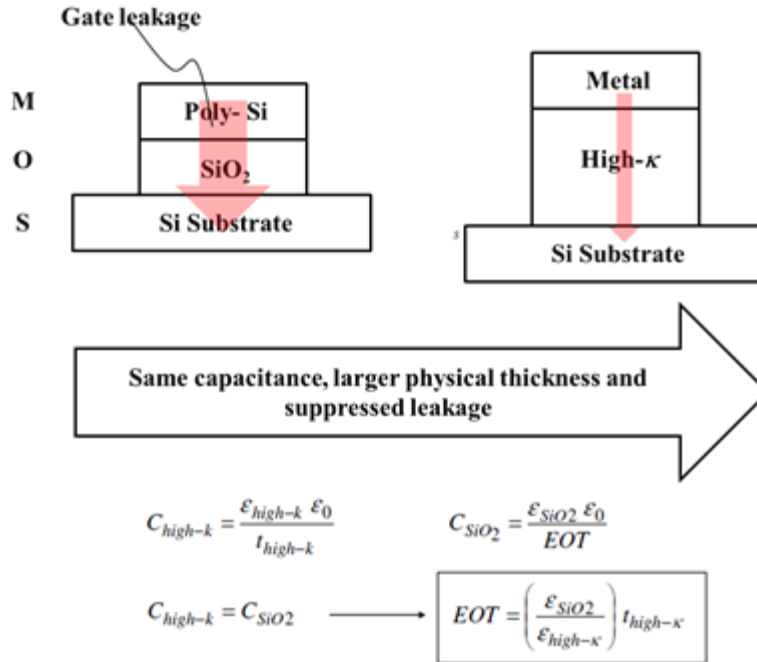


Fig. 1.14 Illustration of (1) replacement of SiO₂/poly-Si gate stack with high- k /metal electrode to achieve same capacitance with suppressed gate leakage, and (2) the concept of the equivalent oxide thickness (EOT) of the high- k dielectrics. Here, C_{high-k} and C_{SiO_2} are the capacitance values of the high- k and SiO₂ MOS capacitors, respectively. t_{high-k} is the physical thickness of the high- k . ϵ_{high-k} and ϵ_{SiO_2} are the relative permittivity, and ϵ_0 is the vacuum permittivity.

Replacement of the SiO₂/poly-Si gate stack by that consisting high- k /metal electrode can address this problem by achieving same capacitance with suppressed gate leakage. As shown in **Fig. 1.14**, since the larger dielectrics constant of high- k materials compared to that of SiO₂, same capacitance can be achieved by high- k dielectrics with thicker physical oxide thickness. Therefore, the gate leakage in the high- k based MOS device can be effectively suppressed. In addition, the equivalent oxide thickness (EOT) of high- k can be

defined by calculating the thickness of SiO₂ that gives same capacitance.

Furthermore, the deployment of metal electrodes is also an indispensable element to realize the high-*k* technology. Poly-Si/high-*k* gate stack have following problems. (1) weak depletion of the poly-Si electrode degrades the EOT [1.6], (2) the fermi-level is pinning at the poly-Si/high-*k* interface due to the large amount of traps at the surface [1.17] and thus we cannot adjust the threshold voltage by change the doping in the poly-Si electrode, and (3) poly-Si/high-*k* gate stack shows strong remote phonon scattering phenomenon and considerably degrades the channel mobility [1.18]. These issues can be solved by using high-*k*/metal gate structure [1.19].

1.2.4 III-V/Ge based FETs for mobility boosting

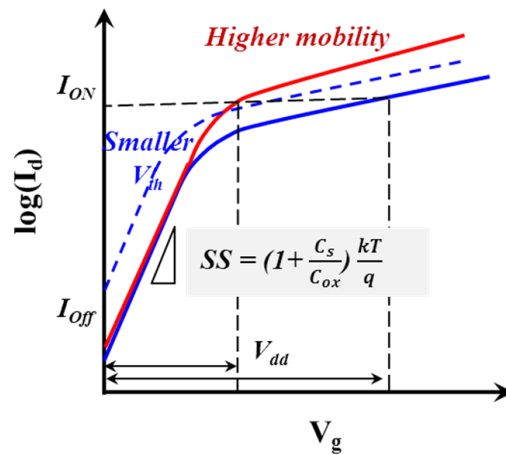


Fig. 1.15 Schematic illustration of the necessity of adopting the high mobility channel for lowering the supply voltage without degrading the requirement for on- and off-current (I_{ON} and I_{OFF}). The blue line shows typical I_d - V_g of an MOSFET, the dash line shows the one of the device with decreased V_{th} and the red line shows the one of the device with high mobility in the channel.

As previously discussed, the supply voltage cannot be scaled due to the power consumption considerations. One solution of this problem, as illustrated in **Fig. 1.15**, is adopting the channel with enhancement transportation, such as strained Si, Ge, and III-V compound semiconductor. It can results in larger on-current and thus allow reducing V_{dd} without sacrificing the requirements on I_{on} and I_{off} .

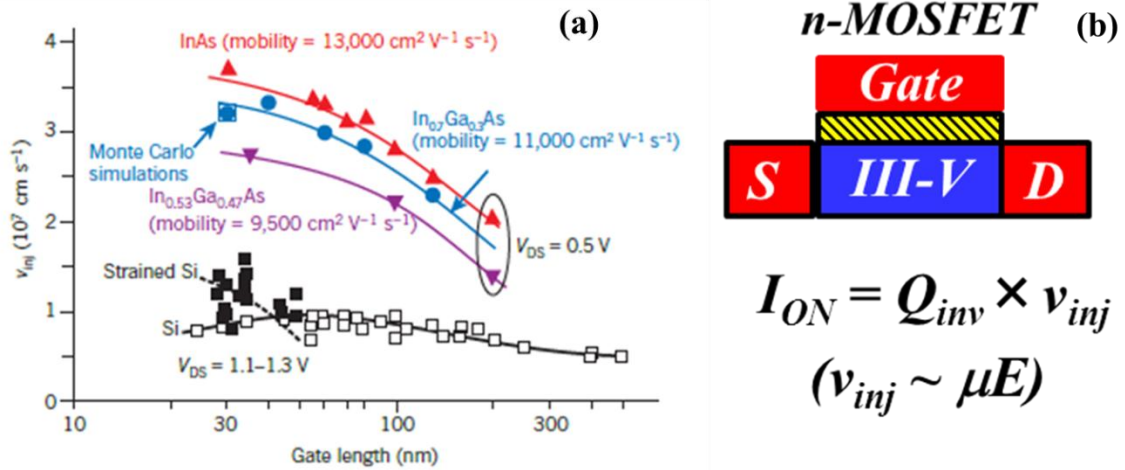


Fig. 1.16 (a) Comparison of the electron injection velocity (v_{inj}) at different gate lengths in Si channel and III-V channel. After J.A.del Alamo, et al. [1.20], and (b) schematic image of the III-V based MOSFET with illustration the relationship between on I_{on} and v_{inj} .

In particular, III-V compound semiconductors, such as $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ and InAs, are extensively studied as alternative channel materials of n-type metal-oxide-semiconductor field effect transistors (n-MOSFETs) for future high-speed, low-power logic applications due to their intrinsic high electron mobility [1.20, 1.21]. As shown in **Fig. 1.16(a)** [1.20], compared to conventional Si or Strained Si channels with large V_{dd} (1.1-1.3 V), the III-V channels with small V_{dd} (0.5 V) show much larger injection velocity, especially at short gate length case ($L_g \sim 30 \text{ nm}$), and thus potentially show better drivability (**Fig. 1.16(b)**).

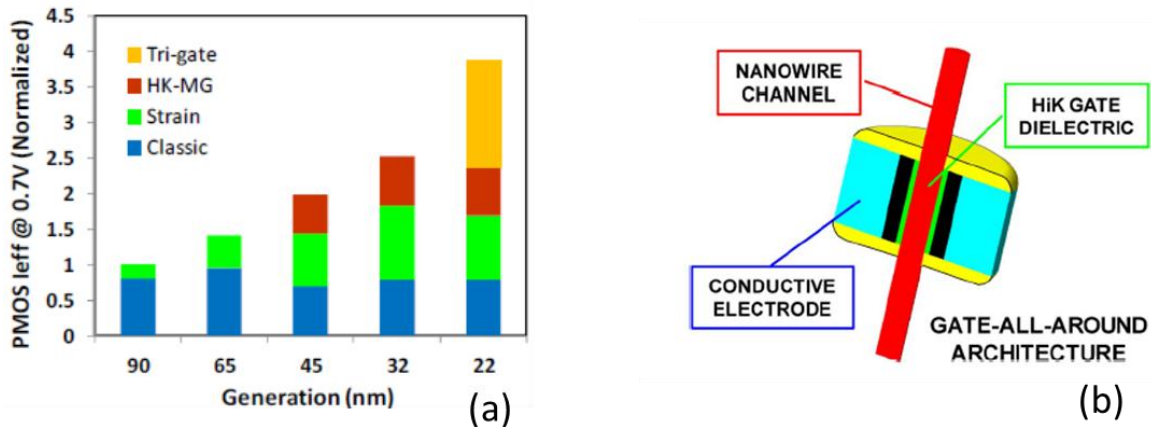


Fig. 1.17 (a)The improved performance of the p-MOSFET as the generation of the technology node evolves is achieved by implementation of new materials and architecture in past technology node.[1.22] and (b) the component of the ultimate CMOS device.[1.22]

In summary, to extend the Moore’s law and take the advantage of improving the performance while lowering the cost by scaling, new structures and materials have to be developed. **Fig. 17 (a)** shows the utilizing of new structures and materials has become the key to boost the performance in recent technology nodes, e.g., the high- k /metal gate replaced SiO_2 based gate insulator in 45 nm generation to overcome the scaling limit of the gate oxide, the tri-gate structure was introduced in 22 nm, in which the fully-depleted Si Fin channel was surround by the top/side gate electrodes and the electrostatic control was substantially increased. **Fig. 17 (b)** schematically shows the component for the ultimate scaling [1.22]. The three key ingredients are: (1) the nanowire channel with GAA architecture, (2) enhanced transportation in the channel, and (3) the high- κ gate dielectrics. In the following section, we will discuss the role of interface and near-interface bulk traps in the realization of this “the ultimate component”.

1.2.5 AlGaIn/GaN based HEMT for high-frequency, high-power application

High-Electron mobility Transistor (HEMT), using GaAs and AlGaAs based heterojunctions, was invented by Prof. Mimura around 1980 [1.23-1.25], which has already become one of the mainstream technology for high-frequency electronics. The first experimental demonstration of HEMT [1.24] is based on the heterojunction structure based on alternative thin layers of n-type AlGaAs and undoped GaAs, as shown in **Fig. 1.18 (a)**. At the interface of n-type AlGaAs and GaAs, due to the higher electron affinity of GaAs, the electrons in the n-type AlGaAs layer can move into the GaAs potential wells. As a result, the near interfacial layer of the AlGaAs layer is depleted and quasi two-dimensional (2D) electron gas is formed at the interface of GaAs, as schematically shown by the band diagram in **Fig. 1.18 (b)**. This 2D electron gas (2DEG) has very high mobility for two reasons: (1) III-V compound semiconductor has the internal property of high electron mobility, and (2) compared to conventional MOSFET, because the mobile electrons is physically separated from the space charge in the depletion region in HEMT, the 2DEG in HEMT is less suffered from the coulomb scattering than that in MOSFET devices.

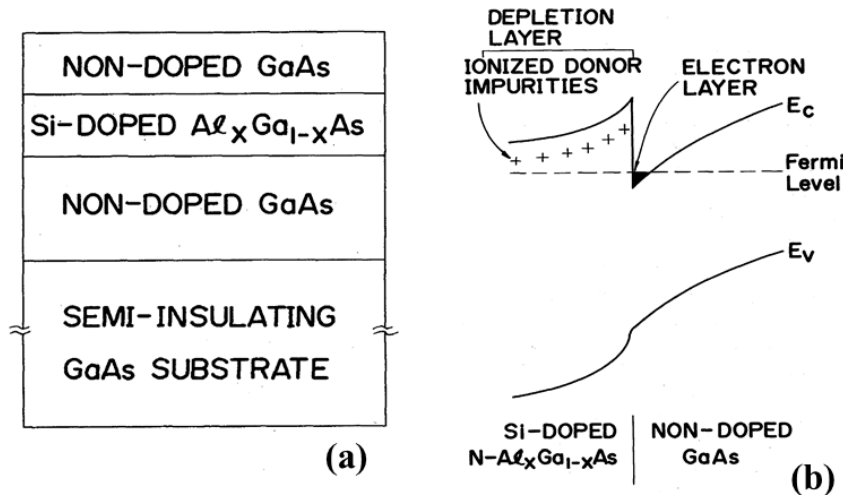


Fig. 1.18 (a) The structure of the heterojunction structure used to constitute the field-effect transistor, and (b) The schematic band diagram of the GaAs/n- $Al_xGa_{1-x}As$ heterojunction

with the illustration of the formation of the tow-dimensional electron gas, adopted from [1.24]

		Si	SiC	AlGaAs/ InGaAs	InAlAs/ InGaAs	AlGaN/ GaN
Characteristic	Unit					
Bandgap	eV	1.1	3.26	1.42	1.35	3.45
Mobility	cm ² /V•s	1500	700	8500	5400	1000- 2000
Saturated velocity	10 ⁷ cm/s	1.0	2.0	1.3	1.0	1.3
Critical Breakdown field	MV/cm	0.3	3.0	0.4	0.5	3.0
Thermal conductivity	W/cm•K	1.5	4.5	0.5	0.7	>1.5
ϵ_r	--	11.8	10.0	12.8	12.5	9.0

Table 1.1 Comparison on critical properties for high-frequency and high-power applications between several semiconductor materials.

Although AlGaN/GaN heterojunction based HEMT is still in its fancy before piratical application, it has already aroused extensive attention due to its outstanding properties for high power and high frequency application [1.26]. As shown by **Table 1.1**, the AlGaN/GaN heterojunction structure shows unique combination of large band-gap, high break-down field, high mobility and saturation velocity, and good thermal conductivity. All of these properties of AlGaN/GaN heterojunction make it as an extremely promising candidate for high power and high frequency electronics.

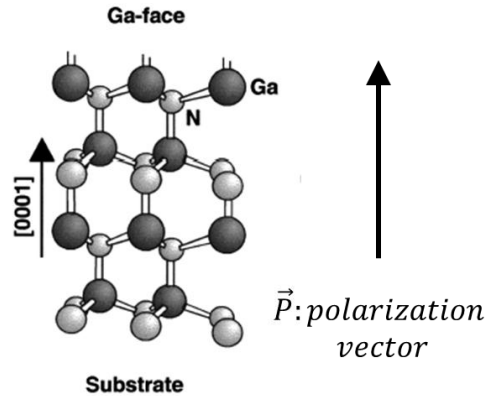


Fig. 1.19. Schematic drawing of the crystal structure of Ga-face GaN. [1.27]

Unlike AlGaAs/GaAs HEMT that requiring intentional doping to form charge, 2DEG in AlGaN/GaN HEMT are induced by the polar nature of AlGaN and GaN, including both of spontaneous and piezoelectric polarization (P_{SP} and P_{PE}), and thus no intentional doping is needed. Normally, the high-quality GaN epitaxy layers have the crystal structure with Ga-polarity, or Ga-face, as shown in **Fig. 1.19** [1.27, 1.28]. Due to strong non-centrosymmetric crystal structure of the GaN, GaN based compounds show strong spontaneous polarization. Besides, the external strain can also modify the crystal structure of GaN and thus change its polarization. Therefore, GaN based compounds also shows strong piezoelectric polarization.

In $\text{Al}_x\text{Ga}_{1-x}\text{N}/\text{GaN}$ heterojunction structure, due to the lattice mismatch between the $\text{Al}_x\text{Ga}_{1-x}\text{N}$ and GaN (**Fig.1.20(a)**), tensile strain is applied to the AlGaN layer after the formation of the heterojunction. As a result, due to the internal spontaneous polarization and the external piezoelectric polarization caused by the strain stored in the heterojunction, a large amount of the polarization charge appears at the interfaces (**Fig.1.20(b)**). This interfacial polarization charges result in the formation of a high concentration of 2DEG in the interface of the heterojunction (**Fig.1.20(c)**). Therefore, the 2DEG can be formed in the AlGaN/GaN heterojunction without intentional doping. Besides, comparing the schematic band diagram of n-type AlGaAs/GaAs (**Fig.1.18(b)**) and AlGaN/GaN (**Fig.1.20(c)**), it can be seen that due to the 2DEG is caused by depletion of the

donors in the n-type AlGaAs in the previous one and that in the later one is caused by the polarization induced charge-sheet, stronger conduction band discontinuity, or “sharper” quantum well, can be found at the interface of AlGaN/GaN heterojunction. This means the distribution of electron gas in the AlGaN/GaN is closer to the ideally two-dimensional distribution, which suggests that higher mobility could be achieved.

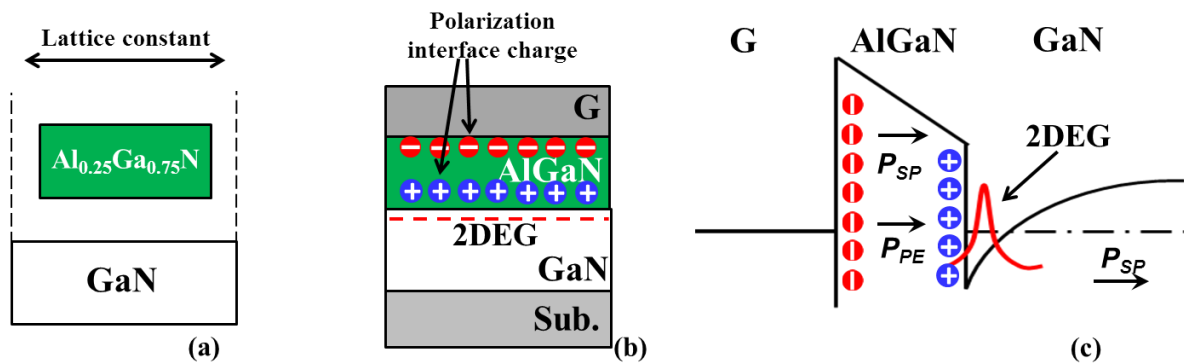


Fig. 1.20. (a) Schematic illustration of the lattice mismatch between AlGaN and GaN, (b) Schematic drawing of the polarization interface charge and the 2DEG in AlGaN/GaN heterojunction, and (c) band diagram of the AlGaN/GaN heterostructure with the illustration of polarization interface charge induced by spontaneous and piezoelectric polarization and the 2DEG formed in the quantum well at the interface between AlGaN and GaN.

1.3 Interface traps and near interfacial bulk traps: origin, properties and influences.

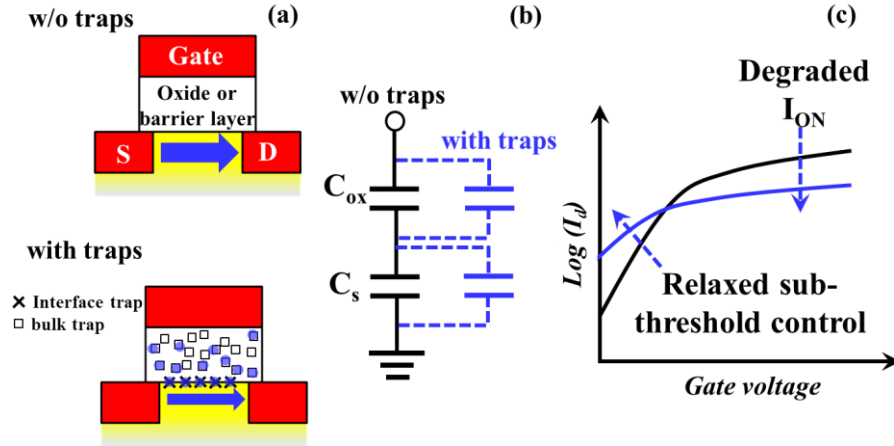


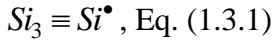
Fig. 1.21 (a) Illustration of the spatial distribution of interface traps and near interfacial bulk traps in MOSFETs, (b) Extremely simplified equivalent circuit to clarify the influence of interface traps and near interfacial bulk traps, and (c) Schematic comparison between the I_d - V_g characteristics of the MOSFETs with and without traps in the gate stacks.

To realize novel FETs with new structures/materials, proper understanding, accurate profiling and effective suppressing the interface and near interface traps in the gate stack, as schematically shown in **Fig. 1.21(a)**, is of crucial importance. In order to clarify the influence of the traps in the gate stack, we plotted extremely simplified equivalent circuits of the gate stacks with and without traps in **Fig. 1.21(b)**. It can be seen that both of interface and near interface traps can contribute to additional capacitance by trapping mobile carriers, and this effect results in screening the gate-to-channel control. In other word, the gate electric field cannot effective control the fermi-level in the semiconductor. As a results, the subthreshold control is weakened because the channel cannot be effectively depleted; the on-state current is also degraded because sufficient amounts of mobile carriers cannot be formed at the surface, as depicted by the schematic I_d - V_g characteristics shown in **Fig. 1.21 (c)**.

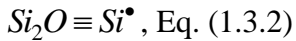
1.3.1 Interface traps at dielectric/semiconductor interface

In this section, we mainly introduced the origin and properties of the interface traps at the Si/SiO₂ interface. Although the cases in novel 3D or high-*k*/high-mobility substrate gate stacks are much more complex, the basic principle for understanding the origin and properties of the interface traps should be similar. After that, we will discuss the influence of interface traps in dielectric/semiconductor interface from a more general prospective.

Most of interface traps are most likely to come from the dangling bands of the semiconductor at the interface due to the interruption of the periodic lattice structure at the surface of a crystal [1.29]. In the Si/SiO₂ interface, the defects can be formed by an unpaired valence electron of a silicon atom back-bonded to three silicon atoms [1.30]:



or an unpaired valence electron of a silicon atom back-bonded to two silicon atoms and one oxygen atom[1.30]:



As shown in **Fig. 1.22**, depending on the specific atomic configuration and surface orientation, three types of electrically active type can be divided and recognized as P_b centers, P_{b0} centers and P_{b1} centers, respectively. Here, P_b centers and P_{b0} centers have similar electrical properties and both of them belong to the type (1.3.1). P_{b1} centers belong to the type (1.3.2).

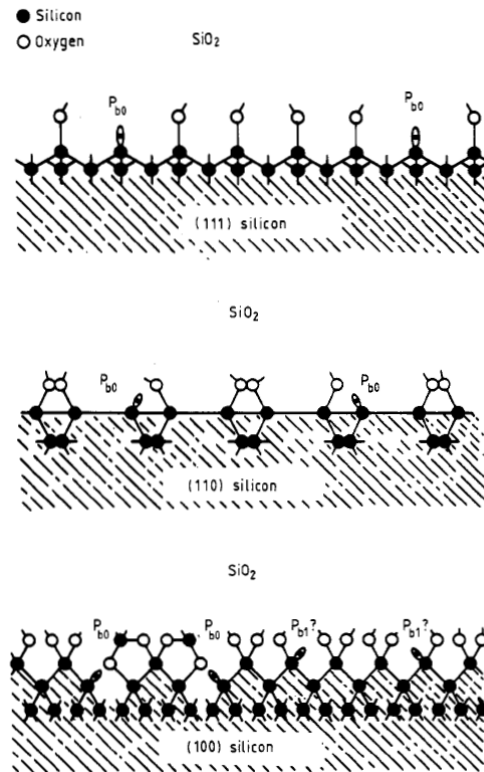


Fig. 1.22 Structure of P_b centers on Si wafers of three major orientations. [1.30, 1.31]

As for the energy distribution of these traps, most of interface traps tend to distribute inside the conduction band. This can be understood by considering that in the tight binding formalism, the conduction band and valence bands are formed as bonding and antibonding combination of the atomic sp^3 hybrids [1.29]. Besides, all of aforementioned types of interface traps are of amphoteric nature: the donor-like traps and the acceptor-like traps. **Figure 1.23** schematically shows the charge properties of the donor-like and the acceptor-like traps. The acceptor-like traps tend to locate at the upper half part of the band-gap. They are electrically neutral when empty and negatively charged when occupied by an electron. On the other hand, the donor-like traps tend to locate at the lower half part of the band-gap. They are positively charged when empty and electrically neutral when occupied by an electron.

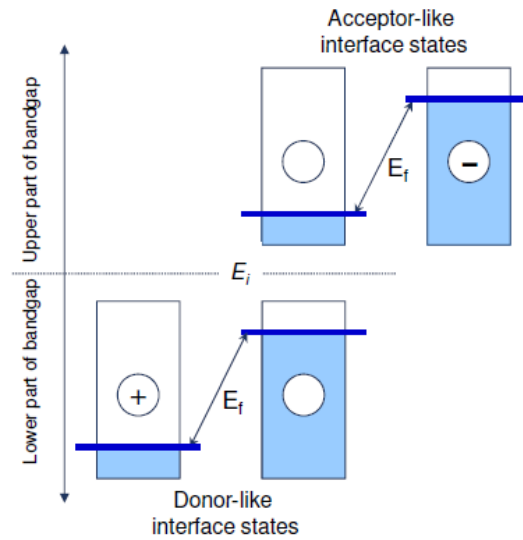


Fig. 1.23 The charge states of the donor-like interface states and the acceptor-like interface states below and above the Fermi-level.

On basis of the amphoteric nature of the interface traps, a very important concept to illustrate the influence of the interface traps is the charge neutrality level (CNL). The concept of CNL is clarified in Fig. 1.24. When the Fermi-level is biased at the CNL, the total trapped charge at the interface traps is electrically neutral.

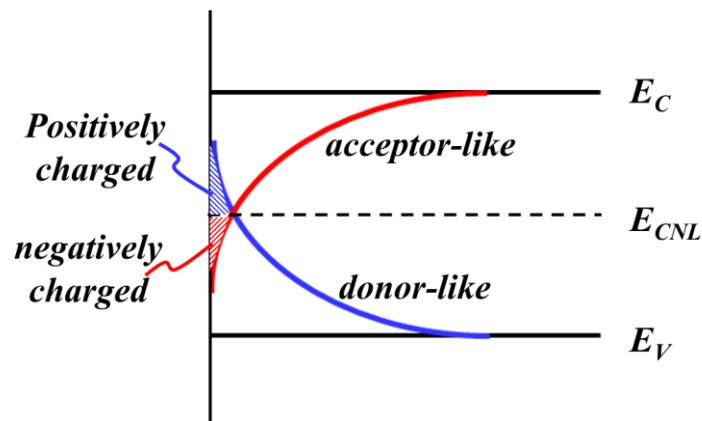


Fig. 1.24 Illustration of the charge neutrality level (CNL). The amount of the donor-like traps above the CNL is equal to the amount of the acceptor-like traps below the CNL.

An empirical method to explain the dominant role of the interface traps based on the CNL is the unified disorder induced gap state model [1. 32, 1.33]. When the fermi-level moves from the CNL to the conduction band edge, the net negative interface charge will form by occupation of the acceptor-like traps and thus prevent the formation of mobile electrons in the conduction band. On the other hand, when the fermi-level moves from the CNL to the valence band edge, the positive interface charge will form by occupation of the donor-like traps and thus prevent the formation of mobile holes in the valence band. Therefore, in case that there is a large amount of the interface traps, the fermi-level tends to be pinned near the CNL. In other words, the gate will lose its control on the fermi-level in the semiconductors.

(a) Interface traps issues to realize MOSFET with 3D channel

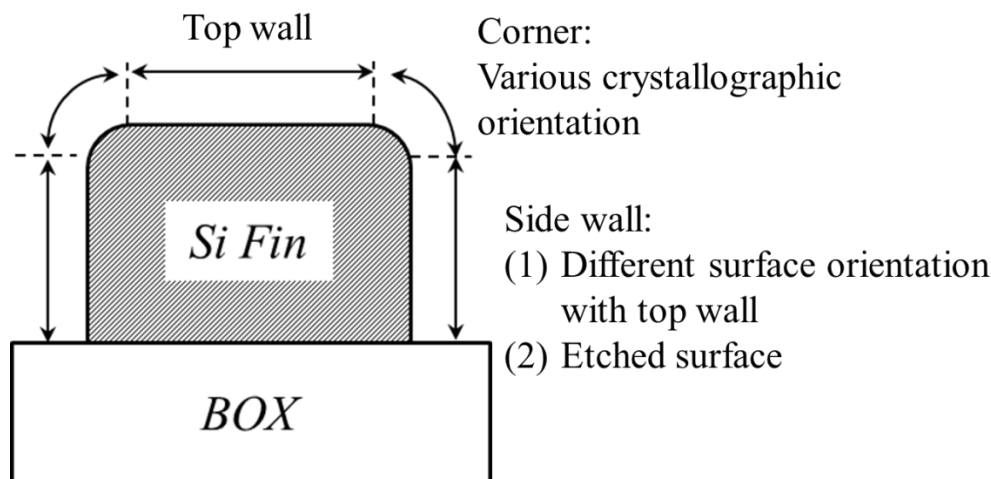


Fig. 1.25 Schematic cross-sectional view of a Tri-gate Si MOSFET with rectangular-like cross-section shape formed. The possible origins of additional D_{it} compared the 3D surface to conventional planar ones are also listed.

Although the conventional Si/SiO₂ gate stack with (100)-oriented Si surface experienced proper surface treatment have D_{it} as low as $10^{10} \text{ cm}^{-2}\text{eV}^{-1}$, the introduction of 3D structure probably lead to high D_{it} , which can eventually hinders the practical application of this type of device. **Figure 1.25** shows a schematic image of the cross-sectional view of a Tri-gate Si MOSFET with rectangular-like cross-section shape. In this device, it is obvious that the

spatial distribution of the D_{it} around the surface is not uniform. Particularly, the top wall and the side wall may have different D_{it} because their different surface orientation. Besides, in commonly used top-down approach for formation of Si fins, the side wall usually experienced etched process. More importantly, the corner part may also show large D_{it} because the crystallographic orientation continually changes at the corner region. In addition, considering the scaling of MOSFET requires aggressive scaling of the channel width, the corner part will play a significant role in the extremely scaled devices.

In published works, some studies have been carried out on separately qualifying the D_{it} at the top and sidewall in the MOSFET with 3D channels [1.34, 1.35]. And some work also qualitatively clarifies the high D_{it} at the corner region [1.35], the quantitative studying of the D_{it} values at the corner part is still not sufficient.

(b) Interface traps issues to realize MOSFET with high mobility channel

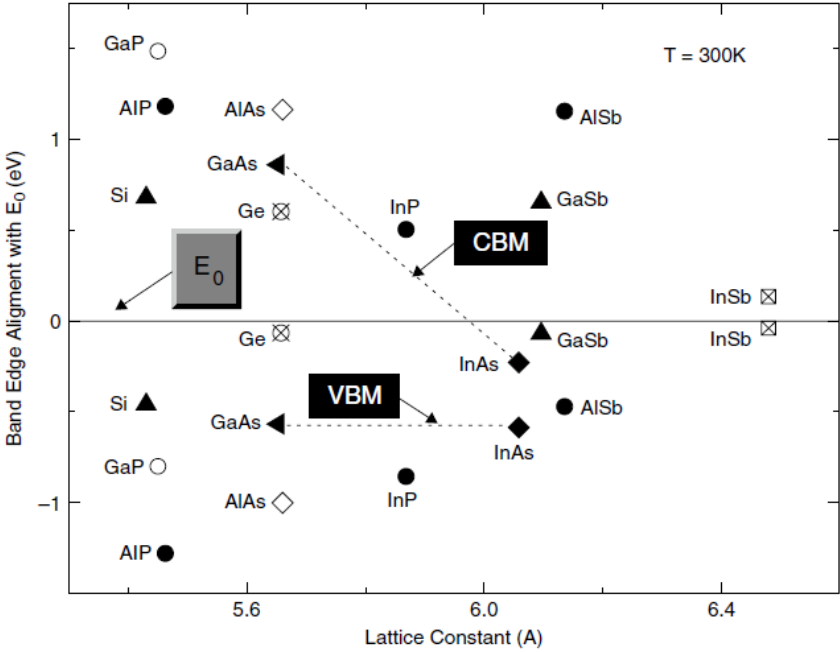


Fig. 1.26 The energy alignment of the CNL with the band edges of the representative semiconductors at MOS interfaces.[1.36]

In the studies of realization of MOSFETs with high mobility channels for practical application, enormous research effort is focusing on the passivation of the interface traps on the channel surface. Generally, the interface properties of the high mobility substrate is much worse than that of Si, and thus the CNL is an important parameter to understand the material properties. **Fig. 1.26** shows the energy alignment of the CNL with the band edges for some representative semiconductors [1.36]. Because Ge has CNL near the valence band edge and high hole mobility, it is considered as a promising candidate for high-mobility p-type MOSFET. On the other hand, the In-rich InGaAs has CNL near the conduction band edge and high electron mobility, it is extensively studied to realized high-mobility n-MOSFET.

1.3.2 Near interfacial oxide traps: emerging issues in MOS device with high mobility substrate

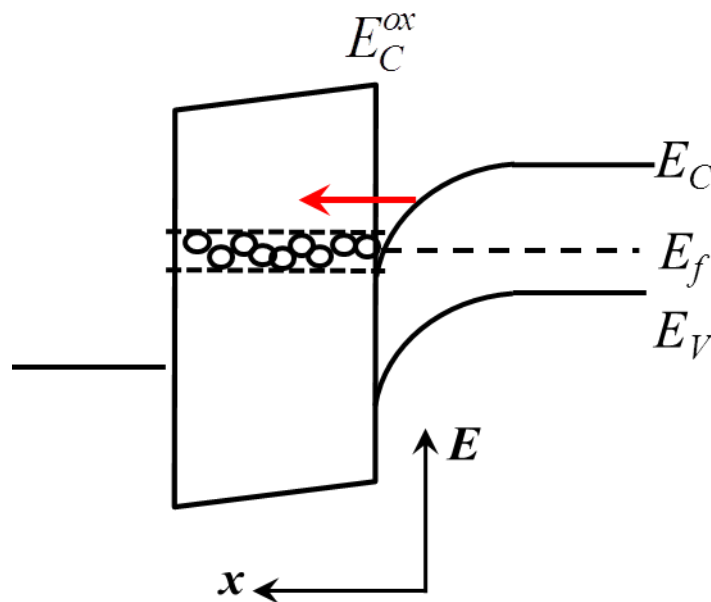


Fig. 1.27 The charging of oxide traps in the on state of a n-MOSFET

Figure 1.27 shows the oxide traps charging effect in the on state of a n-MOSFET. The mobile carriers in the conduction band can directly charge the oxide traps by tunneling effect. The oxide traps is usually caused by the oxygen vacancies or the H Bridge [1. 37].

The near interfacial oxide traps have much more pronounced influences in the MOS system based on the high-mobility substrates and the Si substrates in the following ways: (Here, we mainly discuss on InGaAs as an example.)

(1) The thermodynamically stable interfacial oxide layer with good quality, as that in the SiO₂/Si systems, is still lack in the high mobility substrates based systems.

(2) The band-offset between the conduction band edge of the oxide and substrate in the MOS systems based on high mobility substrates is lower than that in SiO₂/Si. In particular, the band-offset of Al₂O₃/In_{0.53}Ga_{0.47}As is about 2.0 eV, and that SiO₂/Si is about 2.6 eV.

(3) Due to the low effective mass nature, III-V materials have superior electron mobility. However, the low effective mass also leads to low density of states (N_{DOS}) in the conduction band. In particular, the N_{DOS} of InGaAs is about two magnitudes of orders smaller than that in Si. As a result, to form sufficient carriers concentration in the channel, the Fermi-level has to travel deeply into the conduction band. Otherwise, the III-V MOSFET will not benefit from the high mobility on the on-current. However, once the fermi-level E_f has been biased into the conduction band edge, the tunneling barrier decided by $E_C^{ox}-E_f$ becomes even more smaller and thus the oxide trap charging process caused by tunneling also becomes more pronounced.

	effective mass of electron, m^*/m_0	electron mobility, μ ($\text{cm}^2\text{V}^{-1}\text{s}^{-1}$)	density of states in conduction band, N_C (cm^{-3})
<i>Si</i>	$m_i:0.98/m_i:0.19$	1,430	3.2×10^{19}
<i>GaAs</i>	0.067	8,500	4.7×10^{17}
<i>InAs</i>	0.023	13,000	8.7×10^{16}
<i>In_{0.53}Ga_{0.47}As</i>	0.041	9,500	2.1×10^{17}
<i>InP</i>	0.077	4,600	5.7×10^{17}

$$I_{ON} = Q_{inv} \times v_{inj} \quad \text{where} \quad v_{inj} \sim \mu E \quad \text{and} \quad Q_{inv} \sim \int_{E_C}^{\infty} N_C f_D(E) dE$$

Table. 1.2 Comparison on the effective mass, the electron mobility and the density of states (DOS) in the conduction band in Si and representative III-V compound semiconductors. The underlying equations show how the mobility and the DOS influence the on-current of MOSFET devices.

Furthermore, the existence of electrically active oxide traps in the MOS systems with high mobility substrates is further confirmed by following experimental results.

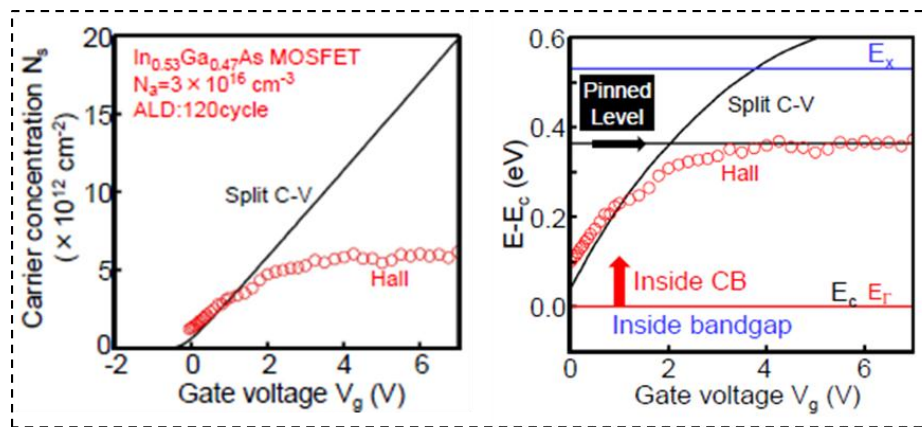


Fig. 1.28 Comparison on the results of (a) the carrier concentration and (b) the Fermi-level position at the ON state of InGaAs n-MOSFET evaluated by the split C-V measurement and Hall measurement [1. 38].

(1) The hall measurement carried out by N. Taoka, et al. [1.38] reveals that in the InGaAs n-MOSFET, Fermi-level tends to pin at about 0.4 eV about the conduction band edge, as shown in **Fig. 1.28**. The discrepancy between the results given by hall measurement and the split *C-V* measurement indicates that there is a large amount of electrically active traps above the conduction band edge.

(2) The pulsed *I-V* measurement, which is commonly used to characterize the transient oxide charging process in MOSFET devices, demonstrates the existence of the traps with very widespread time constants [1. 39]. It is mostly likely to be caused by the oxide traps distributed though the thickness of the oxide.

In summary, large amount of electrically active near interfacial oxide traps exist in the MOS systems with high mobility substrates due to the lack of thermodynamically stable interfacial oxide layer with good quality and large band-offset in these systems. These oxide traps have strong influence on the on-state of the MOSFET with high mobility channel. In particular, these traps potentially prevent the formation of sufficient carriers concentration in the channel by pinning the Fermi-level, degrade the mobility by remote coulomb scattering, and also lead to the threshold voltage instability in the III-V based n-MOSFETs [1.40]. Consequently, it is of significant importance to (1) strengthen the understanding of the trapping/de-trapping process of the oxide traps and (2) establish a readily way to profile the distribution of oxide traps inside the conduction/valence bands of the high-mobility substrates for gate dielectrics optimization.

1.3.3 Interface and near interface traps in semiconductor hetero-junction

In semiconductor hetero-junctions, the interface and near interface traps are likely to be formed at the hetero-interfaces. Particularly, in AlGa_N/Ga_N heterojunction, a considerable amount of elastic strain is stored in the hetero-interface due to the lattice mismatch between AlGa_N and Ga_N [1.40]. Although the stored strain can contribute to the formation of the 2DEG with high density due to the piezoelectric polarization effects, it also leads to

dislocation at the hetero-interface and thus eventually results in interface and near interface traps in the heterojunctions. Additionally, it also has been reported that nitrogen deficiency is likely to be formed in bulk of AlGa_N barrier layer depending on device processing [1.41]. These traps may lead to gate leakage current and performance instabilities in AlGa_N/Ga_N based HEMT devices [1.40, 1.43]. Besides, these traps also play a critical role on the reliability of the devices, as shown in Fig. 1.29 [1.42]. According to published results, the density of interface traps at the hetero-interface is between 10^{12} to 10^{13} cm⁻²eV⁻¹ [1.44, 1.45]. Besides, J. Yang et al. [1.46] also demonstrated the existence of electrically active bulk traps in the AlGa_N barrier layer. However, the origin, distribution, and species of these traps, including the traps at the hetero-interface and the bulk traps in the AlGa_N barrier layer, are still lack of in-depth investigation.

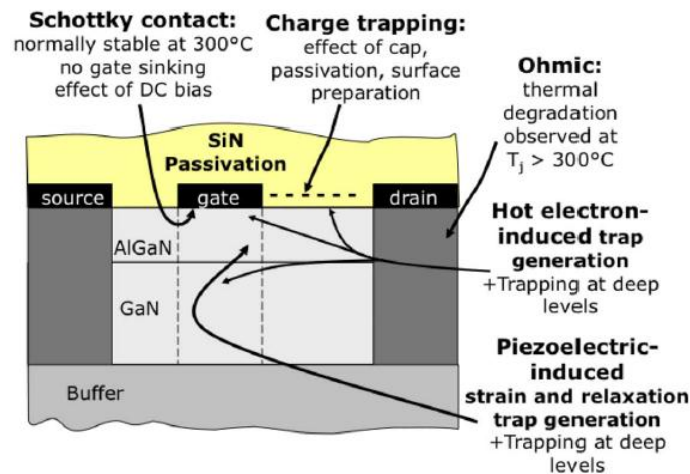


Fig. 1.29 Schematic cross-section on an AlGa_N/Ga_N HEMT, identifying critical areas which can be subjected to degradation. [1.42]

1.4 Purpose and Organization of this study

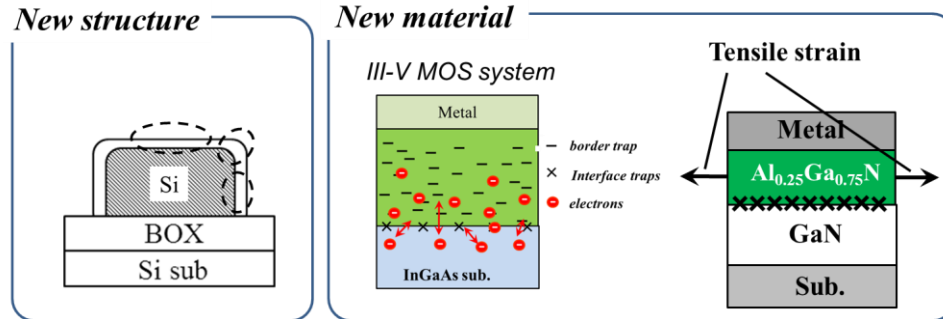


Fig. 1.30 Summary of the interface issues of novel dielectric/semiconductor and semiconductor systems investigated in this study: (1) the spatial distribution of interface traps on the fin structure, (2) the oxide trapping in high- k /III-V MOS systems due to the lack of high-quality interfacial oxide layer with large band-offset, and (3) the interface traps distribution at the AlGaIn/GaN hetero-interfaces.

As previously discussed, to continually extend Moore's law, novel field-effect transistors based on new structure and material have to be developed. However, to achieve these novel devices, there are many unexpected issues about the interface traps and the near interfacial bulk traps at the dielectrics/semiconductor interface and the semiconductor hetero-interfaces requiring further investigation. In this thesis, by studying representative interfacial issues caused by introducing new structure/material (**Fig. 1.30**), i.e., (1) the spatial distribution of interface traps on the fin structure, (2) the oxide trapping in high- k /III-V MOS systems due to the lack of high-quality interfacial oxide layer with large band-offset, and (3) the interface traps distribution at the AlGaIn/GaN hetero-interfaces, we aim to propose methodologies for trap characterization of dielectric/semiconductor interfaces and semiconductor hetero-interfaces based on new structure/materials, reveal in-depth understanding of the distributions, origins, species, and trapping mechanisms of these traps, and thus provide a guideline for trap characterization for future development of advanced FETs.

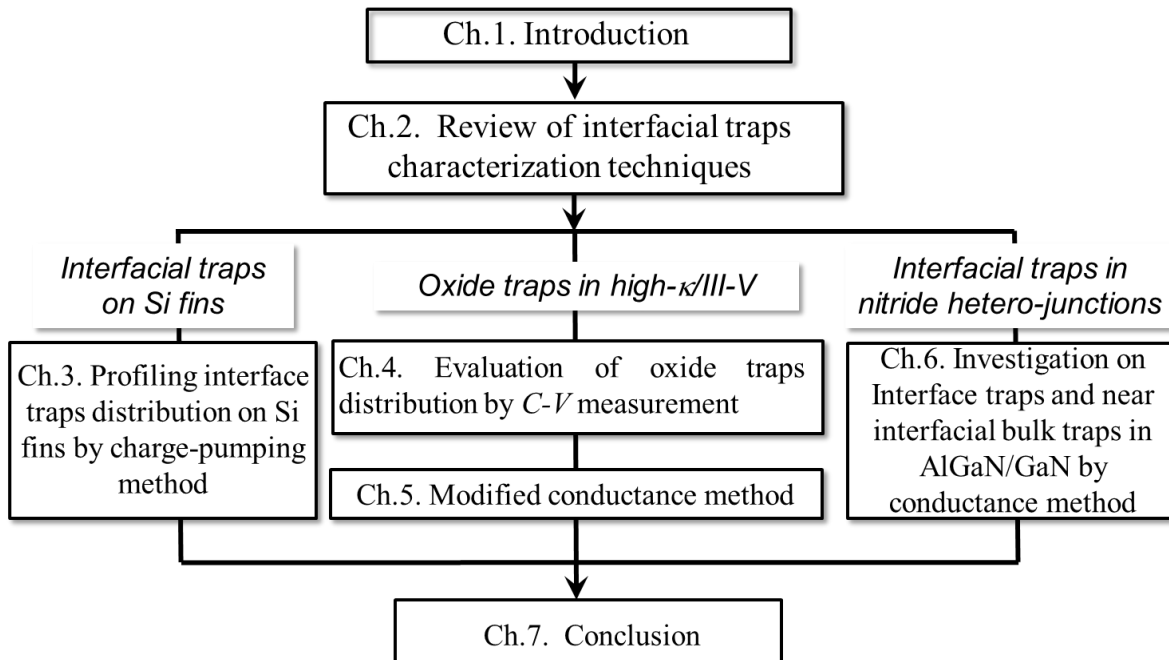


Fig. 1.29 The flow chart of this thesis, which consists of 7 chapters.

This thesis consists of seven chapters. The flow-chart of the thesis is shown in **Fig. 1. 29**. The contents of each chapter are briefly described as follows.

In chapter 1, the necessities for realizing novel field-effect transistors (FETs), including multiple-gate FET, III-V/Ge FET, and AlGaIn/GaN high-electron-mobility transistor (HEMT), and their technological advantages over their conventional counterparts are firstly explained. Then we detail the peculiar interfacial issues of dielectric/semiconductor interfaces and semiconductor hetero-interfaces in these devices and interpret the importance of developing proper trap characterization techniques. Lastly, the motivation and the organization of this thesis are presented. Particularly, by investigating the interfaces of SiO₂/Si with fin structure, high-k/InGaAs, and AlGaIn/GaN, we aim to propose methodologies for electrical characterization of the interface and near interface traps in these systems, reveal in-depth understanding of their distributions, origins, species, and trapping mechanisms, and thus provide a guideline for trap characterization for future

development of advanced FETs.

In chapter 2, a review of commonly used techniques for characterizing interfacial traps is carried out. Especially, capacitance-voltage ($C-V$) based methods, including high- and low-frequency $C-V$ techniques, and charge-pumping method are compared in details. Their applicable scopes and problems for electrically charactering advanced dielectric/semiconductor interface and semiconductor hetero-interface are also discussed.

In chapter 3, the distribution of interface traps on the surface of Si fins is systemically studied by carrying out charge-pumping method on the gated p-i-n diode configuration. The optimal forming gas annealing temperature is extracted and a new methodology to profile the local D_{it} at different regions (i.e., top/side walls and corners) on the 3D surface is proposed. The highest local D_{it} is found at the corners, which is likely to be caused by continually varying crystallographic orientations at the corners.

In Chapters 4 and 5, the interface traps and the oxide border traps in high- k /III-V MOS capacitors are studied by analyzing the admittance characteristics, including capacitance and conductance characteristics, measured at various temperatures. In chapter 4, we propose an empirical way to model frequency- and temperature-dependent responses of oxide border traps in $C-V$ measurement. Particularly, thermally activated trapping process of oxide border traps is demonstrated. On this bias, a methodology to extract the spatial and energy distribution of oxide border traps from the frequency- and temperature-dependent $C-V$ characteristics in accumulation region is developed. The results reveal that there are a large amount of electrically active oxide border traps, whose concentration is likely to increase with increasing energy level and distance from the interface into the oxide. These traps seem to be caused by accumulated defectives during high- k material growth. On the other hand, in chapter 5, the standard conductance method is modified to be applicable for high- k /III-V MOS capacitors by considering both of the influences of interface traps and oxide border traps. The densities of interface traps and oxide border traps are successfully separated by using the different conductance behaviors caused by the responses of interface

traps and oxide border traps. It is found that for the parallel conductance curve with strong low-frequency responses, ignoring the oxide border traps would result in a severe misunderstanding of interfacial trap distribution.

In chapter 6, by adopting the conductance method, the interface and near interface traps at the AlGaIn/GaN hetero-interfaces are studied. It is confirmed that there are no distributed bulk traps in the near interfacial region of the hetero-interface. Besides, the different properties of deep trap levels and shallow trap levels at the hetero-interface are also presented.

Lastly, in chapter 7, we summarize the achievements of this thesis, and also discuss the future works that are worthy for further investigation.

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Chapter 2: Review of the techniques for characterizing interface and near interface traps

In this chapter, commonly used electrical characterization techniques for profiling the interface and near interface traps in MOS systems are reviewed. We mainly focused on the admittance analysis methods, including high- and low-frequency $C-V$ method and conductance method, and the charge-pumping method. Their advantages, disadvantages, and applicable scopes are also analyzed. In addition, the limitations of using these techniques to analyze novel dielectric/semiconductors interfaces and semiconductor heterointerfaces are also pointed out.

2.1 Admittance analysis for interfacial traps characterization

2.1.1 Low-frequency capacitance method

(i) Determination of the D_{it} values

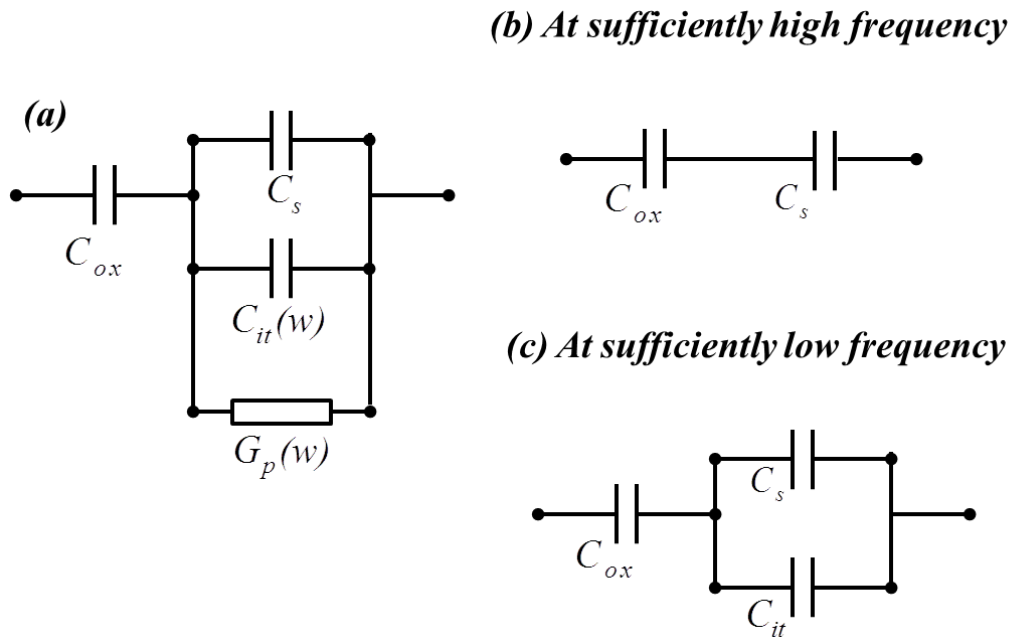


Fig. 2.1 (a) The equivalent circuit for MOS capacitors with interface traps under ac small signal measurement, (b) the equivalent circuit at sufficiently high frequency that the influence of interface traps can be completely screened, and (c) the equivalent circuit at sufficiently low frequency that all of interface traps can follow the ac signal.

In low frequency C - V method (Castagne-Vapaille method) [2.1], D_{it} can be roughly evaluated by comparing the high-and-low C - V characteristics. **Figure 2.1(a)** shows the general equivalent circuit of the MOS structure with interface traps, and thus the total capacitance, C_{tot} , at a given angular frequency, ω , can be given by:

$$\frac{1}{C_{tot}(w)} = \frac{1}{C_{ox}} + \frac{1}{C_{it}(w) + C_S} \quad \text{Eq. (2.1.1)}$$

At sufficiently low frequency C - V measurement, or quasi-static C - V measurement, as shown in **Fig. 2.1(c)**, all of the interface traps are supposed to be able to change their occupation according to the change of gate voltage and thus arouse interface traps induced capacitance C_{it} , which is given by:

$$C_{it}(w \rightarrow 0) = qD_{it} \quad \text{Eq. (2.1.2)}$$

Therefore, from Eq. (2.1.1) and Eq. (2.1.2), it can be derived that:

$$D_{it} = \frac{1}{q} \left(\frac{C_{ox} C_{tot}^{lf}}{C_{ox} - C_{tot}^{lf}} - C_S \right) \quad \text{Eq. (2.1.3)}$$

On the other hand, when the frequency of the small ac signal in C - V measurement is very high, the interface traps cannot change their occupation according to the ac signal, as shown in **Fig. 2.1(b)**. As a result, there is:

$$C_{it}(w \rightarrow \infty) = 0 \quad \text{Eq. (2.1.4)}$$

Consequently, the substrate capacitance C_S can be derived from high-frequency C - V by using Eq. (2.1.1) and Eq. (2.1.3):

$$\frac{1}{C_S} = \frac{1}{C_{tot}^{hf}} - \frac{1}{C_{ox}} \quad \text{Eq. (2.1.5)}$$

Finally, by substituting Eq. (2.1.5) into the Eq. (2.1.3), the D_{it} can be evaluated from the high-frequency and low frequency C - V characteristics as:

$$D_{it} = \frac{C_{ox}}{q} \left(\frac{C_{ox} C_{tot}^{lf}}{C_{ox} - C_{tot}^{lf}} - \frac{C_{ox} C_{tot}^{hf}}{C_{ox} - C_{tot}^{hf}} \right) \quad \text{Eq. (2.1.6)}$$

(ii) Extraction of the voltage-energy relationship

In order to position the evaluated D_{it} in energy, voltage-energy relationship has to be extracted. The voltage-energy relationship can be estimated from low-frequency C - V by using Berglund integral [2.2]:

$$\Psi_s = \Psi_s^0 + \int_{V_g^0}^{V_g} \left(1 - \frac{C_{tot}^{lf}(V_g)}{C_{ox}}\right) dV_g, \quad \text{Eq. (2.1.7)}$$

where Ψ_s is the surface potential and Ψ_s^0 is the surface potential at V_g^0 . It is noteworthy that in order to properly evaluate the V_g - Ψ_s relationship, we have to choose a gate voltage V_g^0 that near the V_g^0 , Ψ_s not strongly depends on gate bias V_g . In case of Si MOS capacitor, V_g^0 can be chosen in accumulation region.

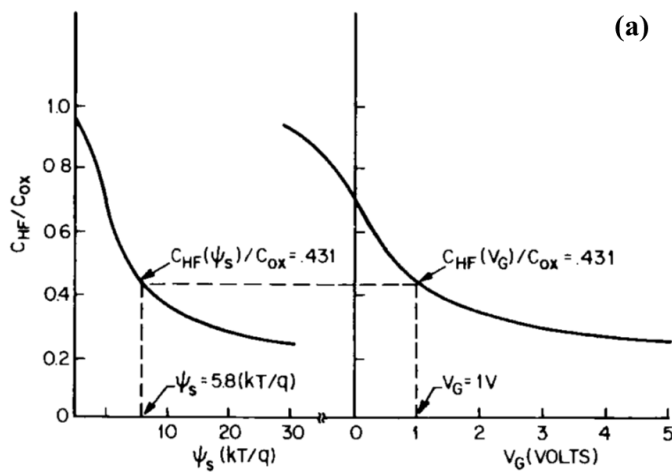
However, one problem of low-frequency capacitance method is how low the frequency should be. If the frequency is not low enough, we cannot assure that all the traps can response to the small signal. On the other hand, if the frequency is too slow, some slow traps, such as oxide border traps, may also contribution to low-frequency capacitance and thus D_{it} may be overestimated. In Chapter 5, we will further discuss this issue.

2.1.2 High-frequency capacitance method

The method of determining D_{it} from high frequency capacitance is also known as Terman method [2.4]. In this method, C - V characteristics are measured with a frequency that high enough so that all the interface traps cannot follow the ac small signal. Therefore, measured capacitance should be equal to the ideal capacitance of the MOS capacitors without interface traps, which can be theoretically calculated according to the oxide capacitance and substrate doping concentration of the under test sample. However, all the interface traps do not influence the measured high-frequency capacitance. They can lead to the “stretch-out” of the C - V curve compared to the ideal C - V curve because these traps can change their occupation during the gate voltage sweeps from inversion to accumulation with relatively

slow sweeping rate. Note that the “stretch-out” effect in high-frequency $C-V$ caused by interface traps is essentially different from the horizontal shift of the $C-V$ curves caused by the oxide fixed charges or the gate work-function.

Therefore, the D_{it} can be estimated from the “stretch-out” effect caused by interface traps. **Figure 2.2** shows extraction of gate voltage-surface potential ($V_g-\Psi_s$) relationship by comparing the theoretically ideal $C_{HF}-\Psi_s$ relationship and $C_{HF}-V_g$ data with the influence of the interface traps. Since D_{it} just lead to the horizontal “stretch-out” of the $C_{HF}-V_g$ curves, the Ψ_s for a given V_g can be extracted by connecting the Ψ_s and V_g that give same C_{HF} in Ψ_s-C_{HF} and V_g-C_{HF} relationships.



(a)

Fig. 2.2(a) Extraction of $V_g-\Psi_s$ relationship from high-frequency capacitance C_{HF} . The LHS diagram shows the theoretical C_{HF} versus Ψ_s without the influence of interface traps. The RHS shows the hypothetical C_{HF} versus V_g .

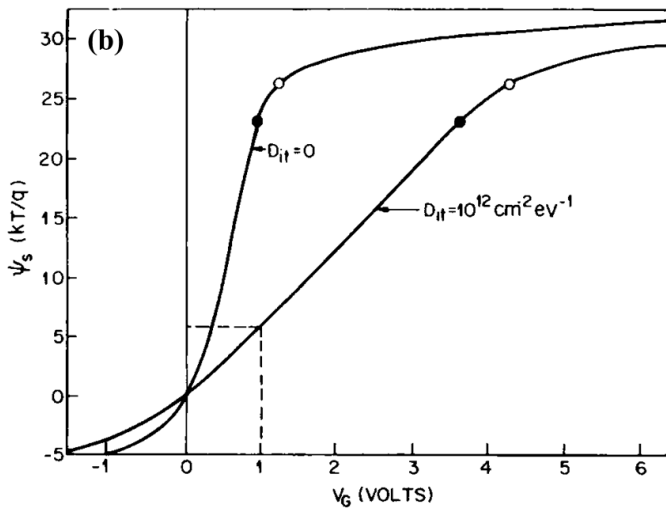


Fig. 2.2(b) Comparison between the theoretical $V_g-\Psi_s$ with $D_{it} = 0$ and $D_{it} = 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$ for the example shown in Fig. 2.2(a).

After Ref [2.3] Nicollican and Brews, Fig. 8.4 and 8.5, pp. 328

The D_{it} can be extracted from extracted V_g - Ψ_s relationship by considering the capacitance of the MOS capacitors [2.5] :

$$C_g = \frac{dQ_s}{dV_g} \quad \text{Eq. (2.1.8)}$$

Here, C_g is the total gate capacitance and Q_s is the total carrier concentration in the semiconductor. Particularly, with considering D_{it} induced capacitance C_{it} , C_g can be given by:

$$\frac{1}{C_g} = \frac{1}{C_{ox}} + \frac{1}{C_{ox} + C_{it}} \quad \text{Eq. (2.1.9)}$$

where $C_{it} = qD_{it}$ in case that V_g change slowly during gate voltage sweeping.

On the other hand, considering Q_s and Ψ_s relationship, there is:

$$C_s + C_{it} = \frac{dQ_s}{d\Psi_s} \quad \text{Eq. (2.1.10)}$$

Therefore, from Eq. (2.1.8), (2.1.9) and (2.1.10), the C_{it} can be estimated by:

$$C_{it}(\Psi_s) = C_{ox} \left[\left(\frac{d\Psi_s}{dV_g} \right) - 1 \right] - C_s(\Psi_s) \quad \text{Eq. (2.1.11)}$$

And thus D_{it} can be given by:

$$D_{it}(\Psi_s) = \frac{C_{ox}}{q} \left[\left(\frac{d\Psi_s}{dV_g} \right) - 1 \right] - C_s(\Psi_s) \quad \text{Eq. (2.1.12)}$$

However, some uncertainties also remain in high-frequency capacitance method. The problems is how to positioning the C_{HF} - Ψ_s relationship, which is influenced by flat-band voltage, V_{fb} . Although V_{fb} can be determined by positioning ideal C - V and experimental

high-frequency C - V . But when the D_{it} is substantially large, such as the case for III-V based MOS capacitance, there is no straightforward method to positioning ideal C - V with experimental ones. Besides, since the slow traps also can contribute to the “stretch-out” effect, the influence of slow traps and fast traps also cannot be distinguished in this method. Some discussion about this issues will also be covered in Chapter 5.

2.1.3 Conductance method

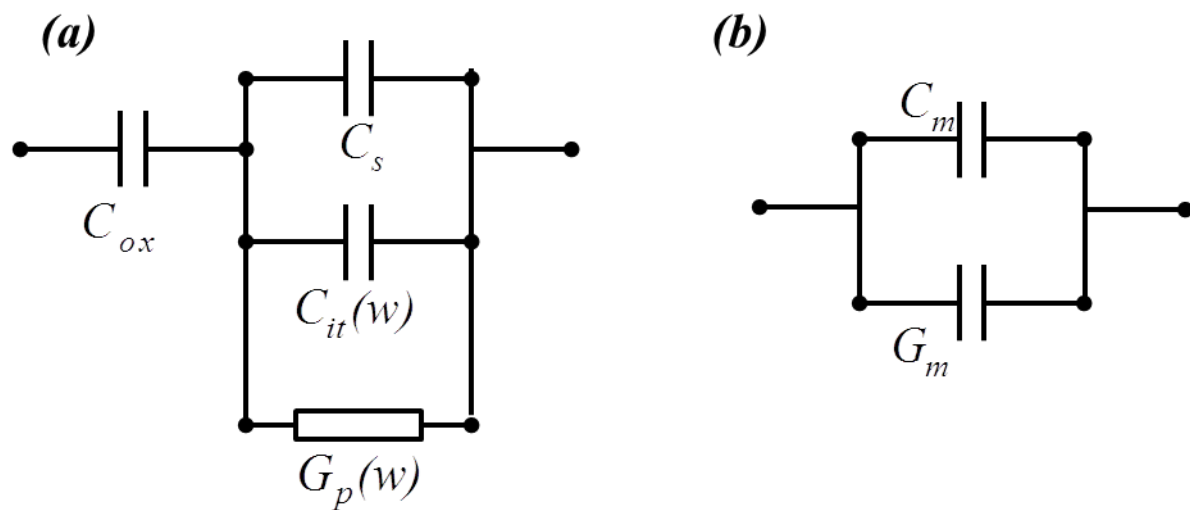


Fig. 2.3 (a) The equivalent circuit for MOS capacitor in depletion with interface traps. Here, C_{ox} is the oxide capacitance, C_s is the semiconductor capacitance, C_{it} is parallel interface traps capacitance, G_p is the parallel interface traps conductance, and (b) The equivalent circuit for an impedance analyzer with parallel connect capacitance-conductance model. C_m and G_m are measured capacitance and conductance.

The conductance method for determination of the interface trap density is developed by E. Nicollian and A. Goetzberger [2.3, 2.6]. **Figure 2.3(a)** shows the equivalent circuit for an MOS capacitor with interface traps biased in depletion without minority carriers responses. **Figure 2.3(b)** shows the parallel C-G model for the measurement by an impedance analyzer. The G_p can be derived from C_m and G_m by:

$$G_p = \frac{w^2 C_{ox}^2 G_m}{G_m^2 + w^2 (C_{ox} - C_m)^2} \quad \text{Eq. (2.1.13)}$$

Furthermore, it can be demonstrated that:

$$\frac{G_p}{w} \sim \frac{w\tau}{1 + w^2\tau^2} \quad \text{Eq. (2.1.14)}$$

Here, w is the angular frequency of the small ac signal and τ is the time constant of the interface trap, which physically represents the average time the trap need to wait before it capture mobile carriers.

From Eq. (2.1.14), it can be seen that when $w\tau \ll 1$, or $\tau \ll 1/w$, G_p/w approximately equals to 0. It means that the interface traps can immediately change their occupation according to the ac signal and there is no energy loss in this case. When $w\tau \gg 1$, or $\tau \gg 1/w$, G_p/w also tends to become 0. It indicates that the interface traps almost cannot response to the ac signal and thus there is no energy loss, too. However, when $w\tau \sim 1$, or $\tau \sim 1/w$, G_p/w shows its maximum value. In this case, because the time constant of the traps is comparable to the period of the ac signal, they change their occupation with a lag behind the ac signal, which leads to considerable energy loss of the MOS systems. As a result, the peak value of the G_p/w versus w plot actually reflects the D_{it} value. It can be estimated by:

$$D_{it} = \frac{2.5}{Aq} \left(\frac{G_p}{w} \right)_{max} \quad \text{Eq. (2.1.15)}$$

Here, A is total active area of the devices and q is the elementary charge.

Furthermore, the time constant τ is given by Shockley-Read-Hall statistics of capture and emission rates: [2.6-2.9]

$$\tau = \frac{1}{n_s v_{th} \sigma} \quad \text{Eq. (2.1.16)}$$

where n_s is the carriers concentration at the semiconductor surface, v_{th} is thermal velocity and σ is the capture cross-section.

Particular, for the interface traps inside the band-gap, n_s can be approximately estimated by:

$$n_s = N_{DOS} \exp(-\Delta E / kT), \quad \text{Eq. (2.1.17)}$$

Where N_{DOS} is density of states in conduction band or valence band, ΔE is a positive value that represents the different between the trap energy and the band edge, k is the Boltzmann constant, and T is the absolute temperature. Therefore, Eq. (2.1.16) can be rewritten as follows by substitute Eq. (2.1.17):

$$\tau = \frac{\exp(\Delta E / kT)}{N_{DOS} v_{th} \sigma}, \quad \text{Eq. (2.1.18)}$$

From Eq. (2.1.18), it can be seen that the time constant of the interface traps is exponentially depends on temperature. Specifically, τ tends to be enlarged with decreasing temperature and be shrined with increasing temperature.

The characteristic frequency of certain interface traps with time constant of τ can be defined by using $\omega\tau = 1$ condition:

$$f = \frac{1}{2\pi\tau} \quad \text{Eq. (2.1.19)}$$

Thereby, by using the commonly acceptable parameters, including N_{DOS} , v_{th} , and σ for a given materials, the characteristic frequency of a certain material as a function of energy with a parameter of temperature can be estimated by using Eq. (2.1.18) and (2.1.19).

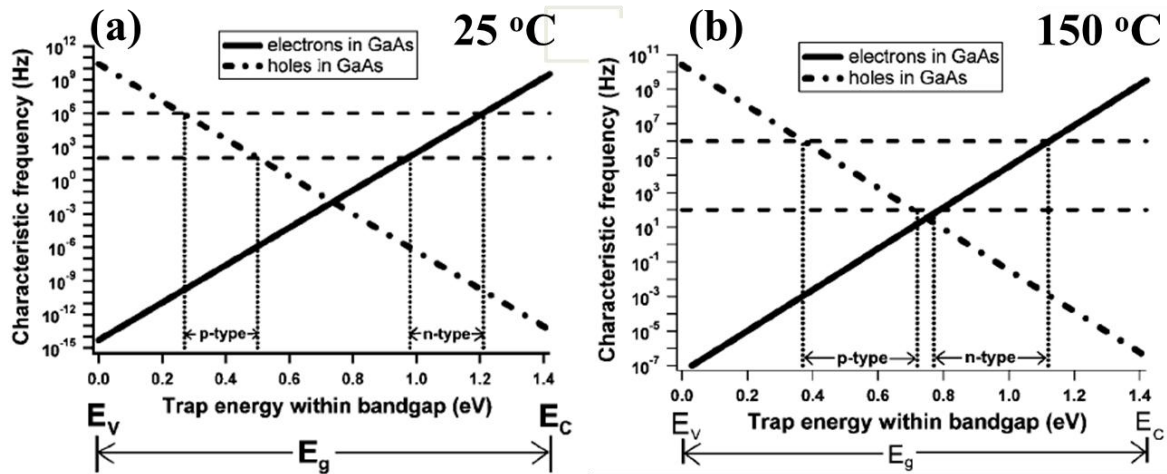


Fig. 2.4 The characteristic frequency for electron trapping (solid line) and hole trapping (dash-dot line) as a function of energy along the band gap of GaAs at 25 °C (a) and 150 °C (b). The dash lines label commonly used frequency window of 100 Hz to 1 MHz. The dot lines depict the detectable energy range for the frequency window. After G. Brammertz et al. [2.7]

Figure 2.4 shows the characteristic trapping frequency of electrons and hole in GaAs [2.7], the III-V compound with relatively large band-gap about 1.43 eV. We see that at room temperature, only a partial of region of the upper and lower halves of the band-gap can be measured due to the time constant near the mid-gap is too slow for our measurement window from 100 Hz to 1 MHz. However, the mid-gap region can be measured at same frequency range by shortening the time constants though heating the sample to about 150 °C.

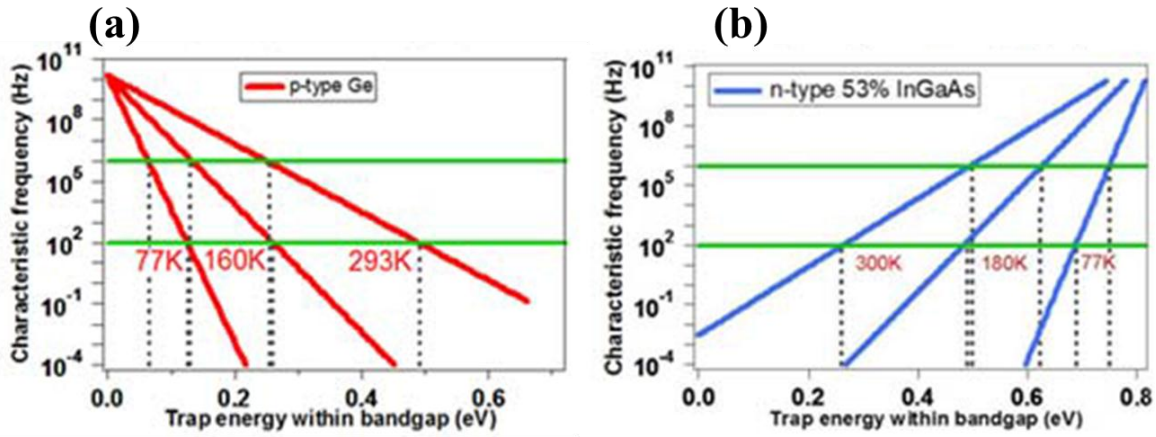


Fig. 2.5 (a) The characteristic frequency of hole trapping in Ge at 293K, 160K, and 77 K, and (b) the characteristic frequency of electron trapping in InGaAs at 300 K, 180 K and 77 K. The green lines label the normal measurement frequency window from 100 Hz to 1 MHz. The dot lines label the detectable energy range at different temperatures.

Figure 2.5 shows the characteristic frequency of hole trapping in Ge and that of electron trapping in InGaAs. Ge and InGaAs are high-mobility substrates with relatively small band-gap (Ge: 0.67 eV, InGaAs: 0.74 eV). It can be seen that in these materials, the detectable energy range in the band-gap at room temperature is near mid-gap. By lowering the temperature, we can measure the energy range near the band-gap.

In summary, the conductance method provides an accurate way to evaluate the D_{it} in the energy-gap from the parallel interface trap conductance. In addition, changing temperature can help us to extend the detectable energy range. Particularly, high-temperature measurement may help to probe the mid-gap D_{it} for semiconductors with relatively large band-gaps. On the other hand, low-temperature measurement may help to probe the near band edge D_{it} for the semiconductors with relatively small band-gaps.

2.2 Charge-pumping (CP) method for interfacial traps characterization

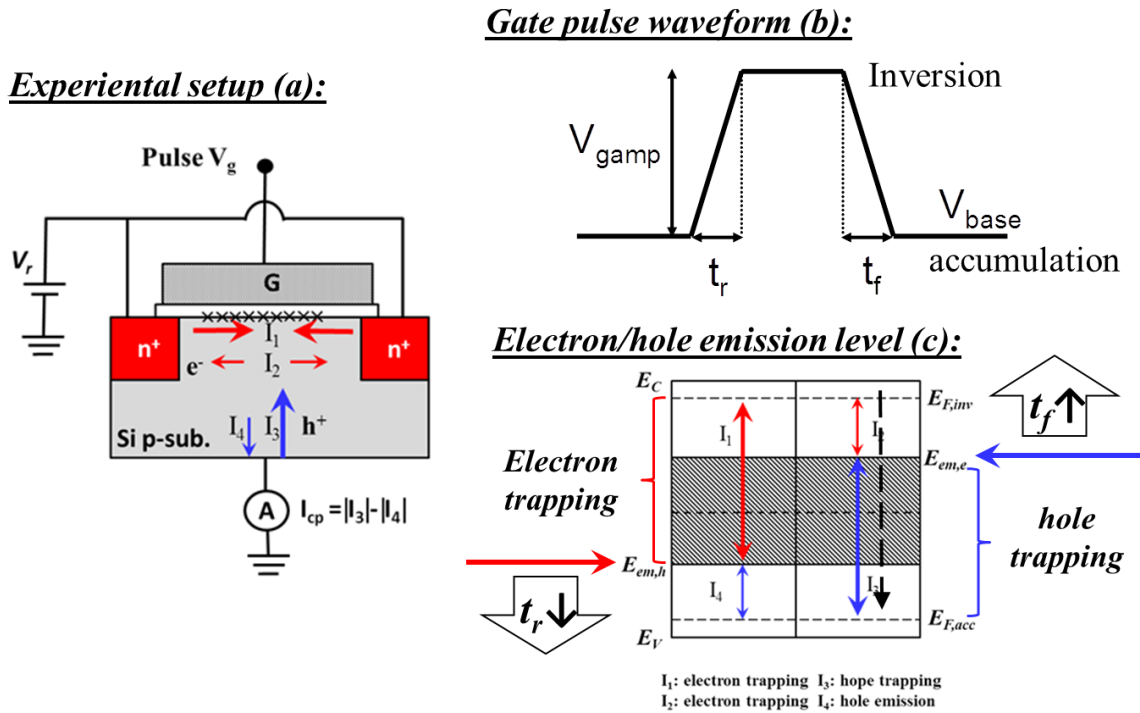


Fig. 2.6 Schematic illustration of charge-pumping method for n-MOSFET: (a) experimental setup, (b) gate pulse waveform, and (c) description of the electron/hole emission level as a function of rising/falling time of the gate pulse.

The CP technique is a reliable technique for the study of the interface traps in MOS transistors [2.10-2.13]. It is able to directly measure the electron-hole recombination current at the trap sites and thus accurately profile the interface trap density. The CP technique for an n-MOSFET is described in **Fig. 2.6**. Figure 2.6 (a) shows the experimental setups. While positive voltage is applied to source/drain to reversely bias the junction, pulse voltage is applied to the gate electrode. The waveform of the gate pulse is shown in Fig. 2.6 (b). As gate pulse rises from base to top, the fermi-level in the channel is swept from VB edge to CB edge and thus the trap levels in the bandgap also change their occupancy by either emitting holes or trapping electrons. The energy level that the trap levels begin to trapping

electrons is dependent on the rising time of the gate pulse. Specifically, if the rising time of the gate pulse is infinite fast, then most of traps in the bandgap do not have enough time to emit holes to VB but direct trap electrons from source or drain. If the rising time the gate pulse is relative slow, then the hole emission level move to the intrinsic fermi-level position of the semiconductor. Reversely, during gate pulse is falling and the fermi-level is sweeping from CB to VB, the trap levels in the bandgap change their occupancy by emitting electrons or trapping holes for the substrate. The electron emission level is also decided by the falling time of the gate pulse. Particularly, the hole emission level, $E_{em,h}$, and the electron emission level, $E_{em,e}$, can be given by [2.11]:

$$E_{em,h} = E_i + k_B T \ln \left(v_{th} n_i \sigma_p \frac{|V_{th} - V_{fb}|}{V_{amp}} t_r \right), \text{ and} \quad \text{Eq. (2.2.1)}$$

$$E_{em,e} = E_i - k_B T \ln \left(v_{th} n_i \sigma_n \frac{|V_{th} - V_{fb}|}{V_{amp}} t_f \right) \quad \text{Eq. (2.2.2)}$$

where E_i is the intrinsic Fermi-level, k_B is the Boltzmann constant, v_{th} is the thermal velocity, $\sigma_{n,p}$ is the capture cross-section of electrons or holes, $t_{r,f}$ is the rising or falling time of the gate pulse.

Therefore, as shown in **Fig. 2.6 (c)**, it can be seen that electrons and holes will recombine at the trap sites whose energy levels locate between $E_{em,h}$ and $E_{em,e}$. This recombination current is so-called CP current, I_{CP} , which is given by [2.11]:

$$I_{cp,max} = qfA \int_{E_{em,h}}^{E_{em,e}} D_{it}(E) dE \quad \text{Eq. (2.2.3)}$$

Here, q is the element charge, f is the frequency of the gate pulse, A is the gate area and the integration is over the energy between holes and electrons emission level.

Besides, since $E_{em,h}$ and $E_{em,e}$ are determined by t_r and t_f , respectively, varying t_r while fixing t_f , and reversely, allows to extract the D_{it} at $E_{em,h}$ and $E_{em,e}$ using [2.11]:

$$D_{it}(E_{em,h}) = -\frac{1}{qAfk_B T} \frac{dI_{cp,max}}{d \ln t_r}, \text{ and} \quad \text{Eq. (2.2.4)}$$

$$D_{it}(E_{em,e}) = -\frac{1}{qAfk_B T} \frac{dI_{cp,max}}{d \ln t_f} \quad \text{Eq. (2.2.5)}$$

Hereby, by change t_r or t_f , the D_{it} at the lower half or the upper half of the bandgap can be measured. In addition, it is also noteworthy that by carrying out frequency-dependent CP technique [2.13], the near interfacial oxide traps as a function of the distance from the interface into the oxide also can be evaluated.

2.3 Comparison between different interfacial traps characterization techniques

	Admittance analysis		Charge-pumping method
	C-V based-method	Conductance method	
Advantages	1. Common method for evaluate MOS capacitor	1. Sensitive to low D_{it} , and other information is available	Direct evaluation of D_{it} by measuring the electron-hole recombination current at the trap sites
	2. Convenient measurement for MOS capacitor		
Problems	1. Required theoretically ideal C-V model or equivalent circuit model		Requiring MOSFET or diode configuration
	2. Not applicable for MOS capacitors on SOI		
	3. Separate evaluation of interface traps and near interface bulk traps is lack of discussion		

Table 2.1. Comparison on the advantages and disadvantages of interfacial traps characterization techniques based on admittance analysis and CP methods.

Table 2.1 summarizes the advantages and disadvantages of the interfacial traps characterization techniques previously described. Admittance analysis based methods, including C-V based method and conductance method, are very convenient to be carried out with MOS capacitors. Especially, multi-frequency C-V measurement is one of the most important characteristics of the MOS capacitors. Besides, conductance method is very sensitive to low interface traps density and capable to provide many properties of the traps, such as their time constant and capture cross-section. However, admittance analysis methods are basically based on equivalent circuit models or theoretically ideal C-V models, which may lead to uncertainties in the extracted distribution profiles of the traps. Moreover, considering most of advanced devices are fabricated on silicon-on-insulator (SOI) wafers, then the admittance characteristics are no longer able to be easily measured by only using capacitor structures. Additionally, separate evaluation of interface and near interface traps is still lack of investigation in this type of method.

On the other hand, by using CP method, the electron-hole recombination current at the trap sites can be directly measured. One of problems of CP method is that relatively complex experimental setup is required. Also, to carry out CP method, well-functioned MOSFET devices are required.

In summary, considering both of advantages and disadvantages of these methods, admittance analysis methods are suitable to preliminarily evaluate the interface quality of MOS capacitors and can be used as a powerful tool during devices optimization. CP methods are capable to achieve an accurate profiling of interface traps distribution in the gate stacks of the MOSFET devices after proper optimization. Therefore, in this study, we used CP method to accurately study the interface traps density in the Si/SiO₂ interfaces with fin structures. For new materials that still required further optimization, such as high- κ /III-V interfaces and AlGaIn/GaN heterointerfaces, admittance analysis is carried out to reveal the distribution, species, trapping mechanisms of the interface and near interface traps in these structures, which is the basis for carrying out further optimization.

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Chapter 3: Study of Interface traps at the surfaces of Si fins by charge-pumping method

Adopting the gated p-i-n diode configuration, the interface state density (D_{it}) at the Si/SiO₂ interface of Si fin structures on Silicon-on-Insulator (SOI) wafers has been systematically studied using charge pumping method. The optimal forming gas annealing temperature for the three-dimensional ($3D$) surface is extracted. And a new methodology for separately quantifying the local D_{it} at different regions of the $3D$ surfaces (i.e., the top/side walls and the corners) is also derived by characterizing the fins with various widths and the planar counterparts. The results validate the necessity to independently consider the corner regions, at which substantially high local D_{it} situates, and further clarify the origin of high D_{it} at $3D$ surfaces.

3.1 Introduction

The 3D semiconductor structure is considered one of the significantly critical building blocks for nano-electronics, which not only enable the relentless scaling trend of complementary metal oxide semiconductor (CMOS) technology to be continued [3.1], but also have remarkable impacts on many interdisciplinary fields, such as photonics and the life sciences [3.2, 3.3]. Of particular interest is the interface state density (D_{it}) of the 3D nano-system, given its dominant role for the device functionality and the uncertainty caused by involvement of surfaces with various crystallographic orientations [3.4, 3.5].

In this study, we have systematically investigated the D_{it} distribution profile on the surfaces of Si fins with rectangular-like cross-sectional shape on Silicon-on-Insulator (SOI) wafers. By formation of gated p-i-n diodes configuration with three terminals, the charge pumping method, a reliable approach to qualify the D_{it} by the interface states induced recombination process [3.6-3.8], is applicable to directly measure the D_{it} situated at the 3D interface of the fin structure [3.9, 3.10]. The optimal annealing temperature of forming gas (F.G.), which is a mixture of N_2 and H_2 in a ratio of 97:3, for the interface states passivation is extracted. Furthermore, a new methodology for separately quantifying the local D_{it} situated at different regions along the cross-section, i.e., the top/side walls and the corners, is developed by characterizing the fins with different widths and the planar counterparts. The results reveal that independent consideration of the corner parts is necessary to obtain reasonable local D_{it} profile of the 3D surfaces. This technique can help to optimize the cross-sectional shape for further lowering the D_{it} of 3D surfaces by estimation of local D_{it} distribution profile.

3.2 Experiments

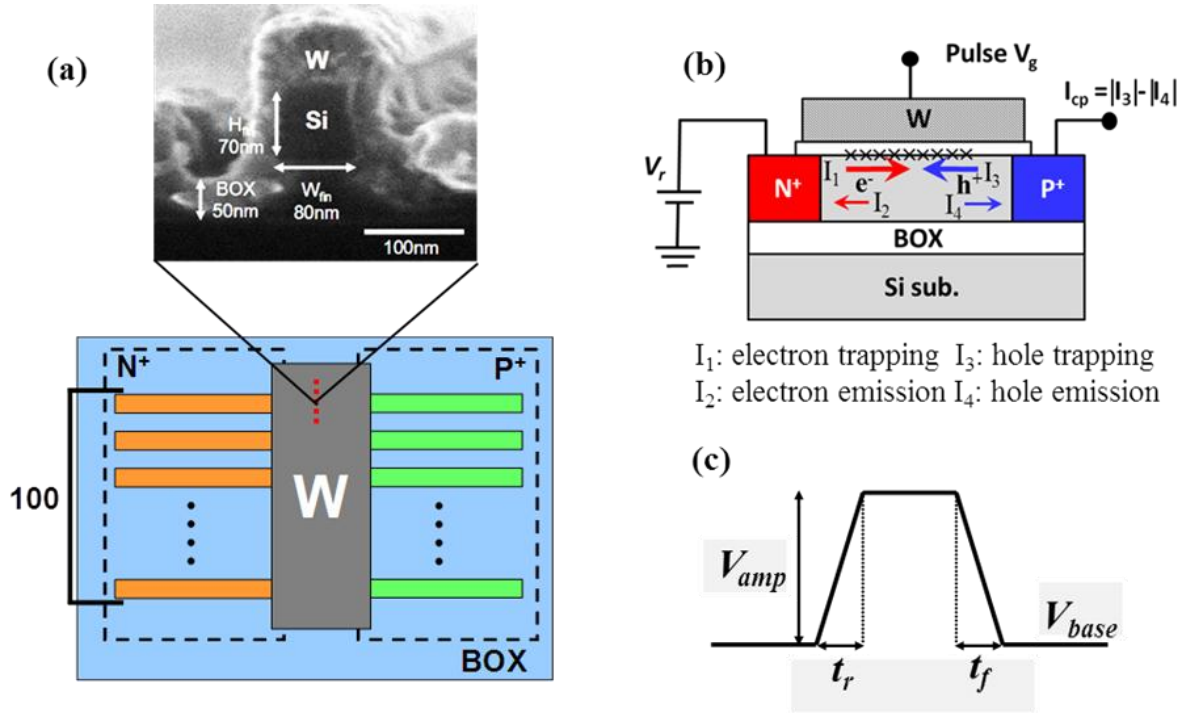


Fig. 3.1 (a) Schematics of the top view of the fabricated gated p-i-n diode device. The inset shows the SEM image of the cross-sectional view of a single fin, (b) experimental setup for the charge pumping measurement; the arrows represent four different current flows in one period of the gate pulse, and (c) the waveform of applied gate pulse.

The structure of the gated p-i-n diodes used in this study is schematically shown in **Fig. 3.1(a)**. Each device contains a large number of parallel-connected fins ($N = 100$) to produce measurable current and average out the process induced variation. The device fabrication starts from patterning $\langle 110 \rangle$ -directed Si fins on (100)-oriented SOI substrates with 70-nm-thick SOI layers and 50-nm-thick buried oxide layers. Patterned Si fins have rectangular-like cross-sectional shape with (100)-oriented top walls and (110)-oriented side walls, as shown by the SEM image in the inset of **Fig. 3.1(a)**. For the purposes of this study, Si fins with a height (H_{fin}) of 70 nm and various widths (W_{fin}) ranging from 80 to 110 nm

are patterned to assure that the top walls, the side walls and the corners can be clearly distinguished. The 14-nm-thick SiO₂ gate-oxide is formed by dry oxidation at 1000 °C for 10 min, and the tungsten gate electrode is deposited by sputtering. The n⁺ and p⁺ regions adjacent to the gate electrode are formed by implantation of P and BF₂ ions, respectively. After thermal activation of the dopants, F.G. annealing for interface states passivation from 300 to 600 °C for 30 min is carried out for different samples. Besides, the planar counterparts are fabricated on the same type of SOI substrates under identical process flow, except that the relatively large W_{fin} ranging from 46 to 78 μm are patterned to exclude the influences of the side walls at the channel edge. Indeed, it has been shown that when $W_{fin} \gg H_{fin}$, D_{it} depends only on the (100) top walls, as discussed later in **Fig. 3.4 (a) and (b)**.

The basic experimental setup for charge pumping measurement is shown in **Fig. 3.1(b)**. Here, the p⁺ region serves as the body contact of the Si fins to measure the charge pumping current (I_{cp}). The reverse voltage (V_r) at the n⁺ region is set to 0.05 V, which is sufficient to eliminate the “geometric component” [3.6] without excessive shortening the effective channel length. Repetitive trapezoidal pulse with frequency of 500 kHz is applied to the gate electrode and the waveform is shown in **Fig. 3.1(c)**. The base level of the gate pulse (V_{base}) is swept from -3 V to 1 V to vary the devices from accumulation to inversion. The amplitude of the gate pulse (V_{amp}) is held constant at 2 V. Note that V_{amp} should be larger than $|V_{th} - V_{fb}|$ as required by the charge-pumping method [3.7], where V_{th} is threshold voltage and V_{fb} is the flat band voltage. Consequently, the maximum charge pumping current ($I_{cp,max}$) can be given by [3.6, 3.7]:

$$I_{cp,max} = qfA \int_{E_{em,h}}^{E_{em,e}} D_{it}(E) dE \quad \text{Eq. (3.2.1)}$$

Here, q is the element charge, f is the frequency of the gate pulse, A is the gate area and the integration is over the energy between holes and electrons emission level given by [3.7, 3.8]:

$$E_{em,h} = E_i + k_B T \ln \left(v_{th} n_i \sigma_p \frac{|V_{th} - V_{fb}|}{V_{amp}} t_r \right), \text{ and} \quad \text{Eq. (3.2.2)}$$

$$E_{em,e} = E_i - k_B T \ln \left(v_{th} n_i \sigma_n \frac{|V_{th} - V_{fb}|}{V_{amp}} t_f \right) \quad \text{Eq. (3.2.3)}$$

where E_i is the intrinsic Fermi-level, k_B is the Boltzmann constant, v_{th} is the thermal velocity, $\sigma_{n,p}$ is the capture cross-section of electrons or holes, $t_{r,f}$ is the rising or falling time of the gate pulse (Fig. 1(c)). Since $E_{em,h}$ and $E_{em,e}$ are determined by t_r and t_f , respectively, varying t_r while fixing t_f , and reversely, allows to extract the D_{it} at $E_{em,h}$ and $E_{em,e}$ using [3.7, 3.8]:

$$D_{it}(E_{em,h}) = -\frac{1}{qAfk_B T} \frac{dI_{cp,max}}{d \ln t_r}, \text{ and} \quad \text{Eq. (3.2.4)}$$

$$D_{it}(E_{em,e}) = -\frac{1}{qAfk_B T} \frac{dI_{cp,max}}{d \ln t_f} \quad \text{Eq. (3.2.5)}$$

First, the effectiveness of the experimental setup is validated on a planar device. As shown in **Fig. 3.2(a)**, the I_{cp} versus V_{base} plot shows a typical ‘‘hat’’ shape, and the magnitude between the rising and falling edge is about 2 V in accordance with the V_{amp} . Besides, the I_{cp} decreases as t_f increases since more trapped electrons emit back to source rather than involve in the recombination process associated with interface states. Here, the $D_{it}(E_{em,e})$ can be extracted from $I_{cp,max}$ as a function of t_f , as shown in **Fig. 3.2(b)** according to Eq. (3.2.5), and the corresponding energy level can be estimated by Eq. (3.2.3).

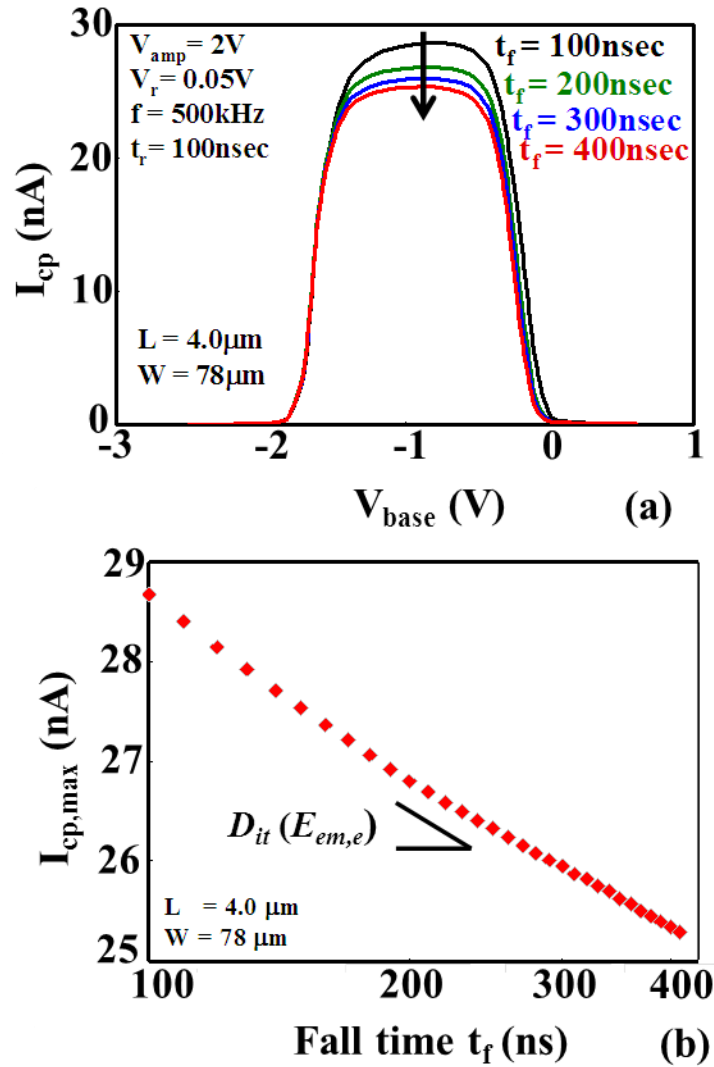


Fig. 3.2 Typical charge pumping characteristics of a planar SOI device: (a) charge pumping current (I_{cp}) versus base level voltage of the gate pulse (V_{base}), and (b) the maximum charge pumping current ($I_{cp,max}$) as a function of fall time (t_f), while the rising time (t_r) is held constant at 100 ns.

3.3 Results and Discussion

3.3.1 Extraction of the optimal forming gas annealing temperature

Before studying the local D_{it} distribution at different regions of the Si fins, we have investigated the optimal F.G. annealing temperature for passivation of the Si dangling bands at the 3D Si interfaces to achieve low average D_{it} over the whole surfaces. As shown in **Fig. 3.3** (a) to (d), the D_{it} values in the detectable energy range substantially decreased at the F.G. annealing temperature of 420°C. Although large D_{it} toward E_i appears in the as-fabricated device, the typical U-shaped distribution can be obtained after proper F.G. annealing. The dependency of the D_{it} profile on the F.G. annealing temperature is quite similar to that of the planar Si/SiO₂ interface [3.11, 3.12]: the D_{it} decreases as temperature increases from 300°C to around 450°C because of enhanced formation of Si-H band. On the other hand, when the temperature further increases, the D_{it} increases again because of the dissociation of the Si-H bond.

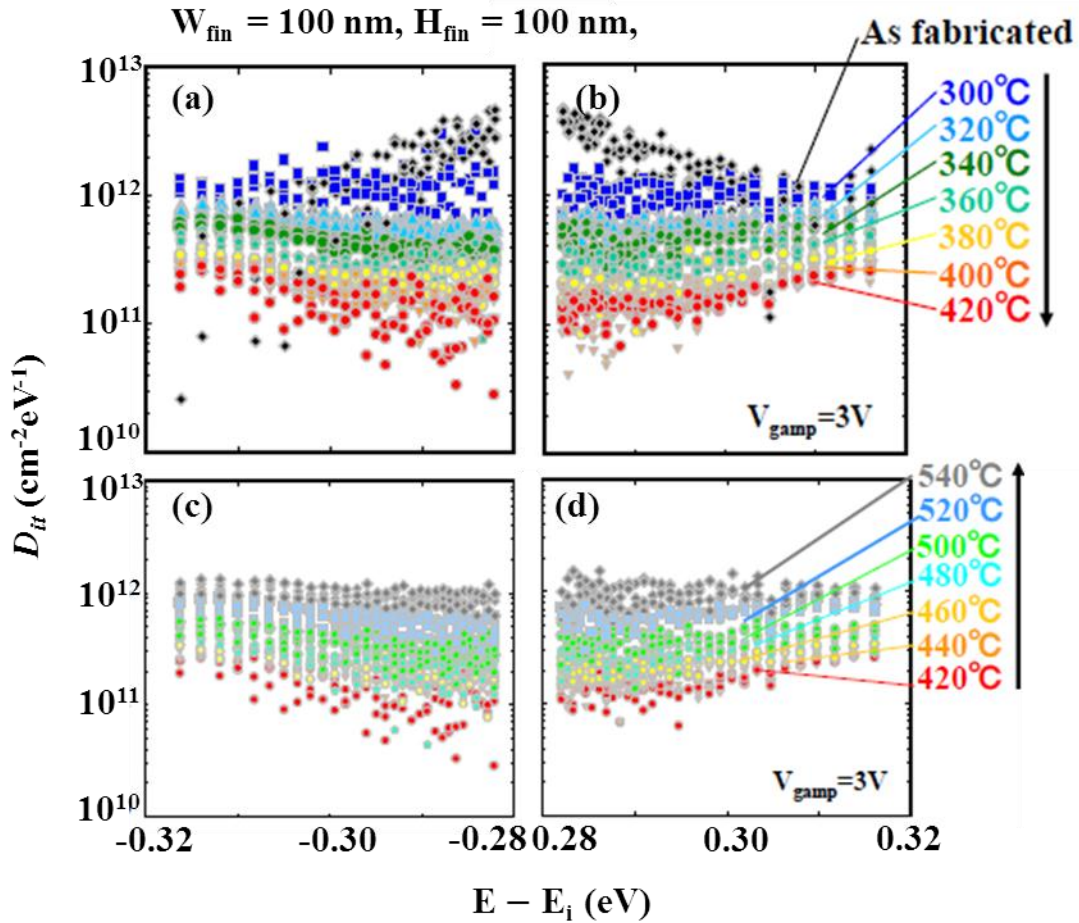


Fig. 3.3 Energy distribution of the D_{it} of Si fin devices with width of 100 nm and height of 70 nm under F.G. annealing for 30 min at various temperatures: (a) and (b) show the D_{it} profile at lower and upper halves of the band gap of the devices with annealing temperature ranging from 300°C to 420°C, (c) and (d) show that of devices with annealing temperature ranging from 420°C to 540°C. The as-fabricated case is also shown in (a) and (b).

3.3.2 Spatial distribution of the interface traps on the 3D surfaces of the Si fins

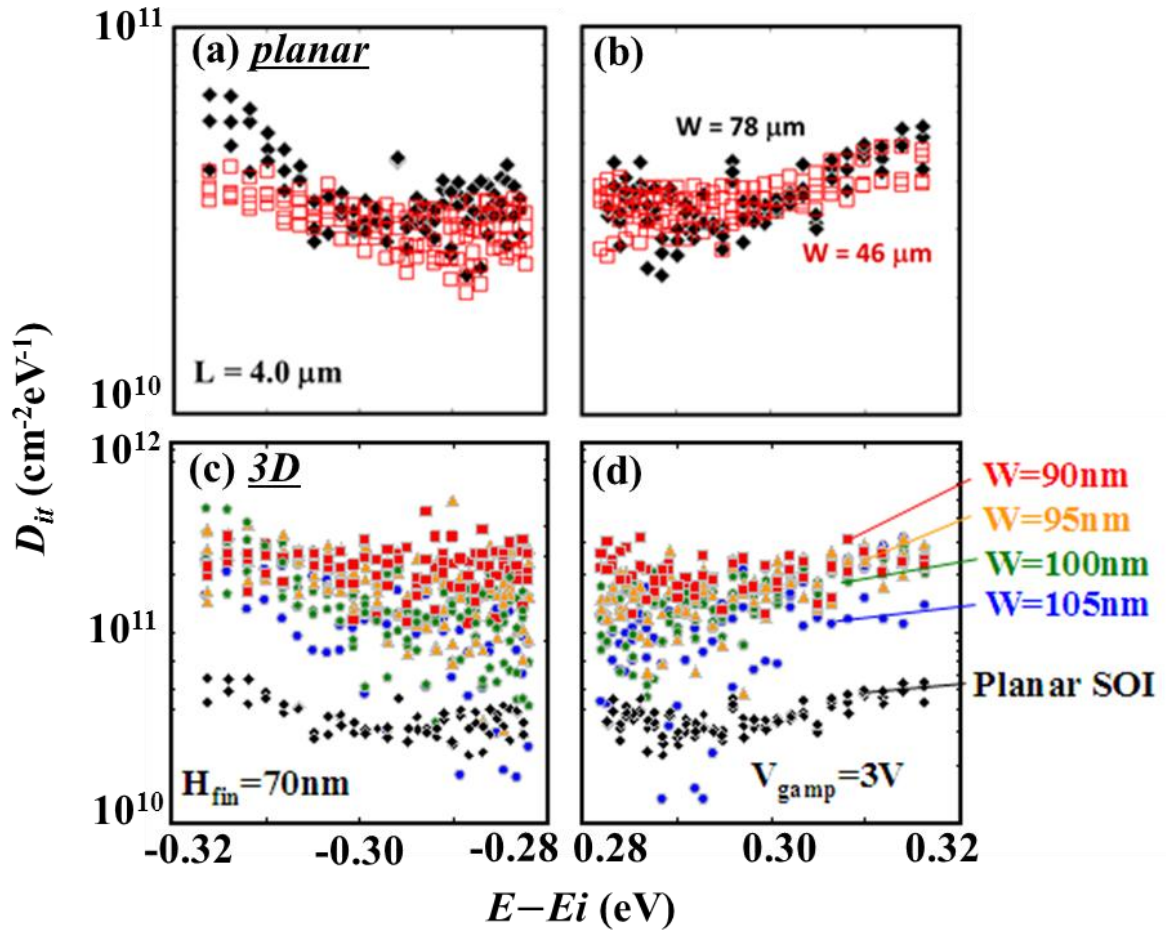


Fig. 3.4 (a) and (b) show the energy distribution of D_{it} of (100)-oriented planar SOI devices with different widths, (c) and (d) shows that of 3D Si fin device with width ranging from 90 to 105 nm. The case of planar is also depicted in (c) and (d) for comparison. All of the devices are annealed at 420°C under F.G. ambient for 30 min.

Figure 3.4 further depicts the energy distribution of D_{it} of the planar and the Si fin devices with different widths. All devices are annealed under the optimal F.G. annealing condition. **Figure 3.4** (a) and (b) shows the D_{it} profile of (100)-oriented planar SOI devices of the lower and upper half parts of the band-gap, respectively. The D_{it} in the detectable

energy range is between 10^{10} to 10^{11} $\text{cm}^{-2}\text{eV}^{-1}$ and almost independent of channel widths. On the other hand, as shown in **Fig. 3.4** (c) and (d), the D_{it} of the Si fin device is much larger than that of the planar ones, and it further increases as the channel width decreases, indicating the non-uniform spatial distribution of the D_{it} at the different parts of the 3D surfaces. Particularly, high local D_{it} may exist at the (110) side walls because (1) the Si (110) surface has higher D_{it} than the (100) surfaces in general [3.13] and (2) the side walls are formed by the dry etching process. More importantly, high local D_{it} also probably appears at the corner region containing various crystallographic orientations.

In order to separately evaluate the local D_{it} at different regions of the 3D surfaces, it is reasonable to divide the surfaces of the Si fins with rectangular-like cross-sectional shapes to three individual components, i.e., the top/side walls and the corners, as shown in **Fig. 3.5(a)**. Therefore, the average D_{it} over the peripheral length around the cross-section can be estimated by

$$D_{it} = \frac{(W_{fin} - 2\Delta) \times D_{it,top} + 2H_{fin} \times D_{it,side} + 2\Delta \times D_{it,corner}}{W_{fin} + 2H_{fin}}, \quad \text{Eq. (3.3.1)}$$

where Δ is the length of the corner parts, $D_{it,top}$, $D_{it,side}$ and $D_{it,corner}$ are the local interface state densities at the top, side walls and the corners. Two important extreme cases can be derived from Eq. (3.3.1):

$$D_{it}(W_{fin} \rightarrow \infty) = D_{it,top}, \text{ and} \quad \text{Eq. (3.3.2)}$$

$$D_{it}(W_{fin} = 2\Delta) = \frac{2H_{fin} \times D_{it,side} + 2\Delta \times D_{it,corner}}{2(\Delta + H_{fin})} \quad \text{Eq. (3.3.3)}$$

Here, Eq. (3.3.2) corresponds to the case that W_{fin} is much larger than H_{fin} and Δ , the average D_{it} approximately equals to $D_{it,top}$ as the ignorable contribution from side walls and corners. Eq. (3.3.3) signifies the case that when $W_{fin} = 2\Delta$, the average D_{it} is the weighted

average of the local D_{it} of the side walls and the corners because the influence of the top wall is ruled out. It is also noteworthy that if the contribution of the corner parts is ignored ($\Delta = 0$), the $D_{it}(W_{fin} = 0)$ is supposed to be equal to $D_{it,side}$, as shown in our previous work [3.14]. Thereby, by fitting the experimental D_{it} values extracted from Si fins with varying widths using Eq. (3.3.1), $D_{it,top}$, $D_{it,side}$ and $D_{it,corner}$ can be estimated by extrapolating the fitted curve to the extreme cases.

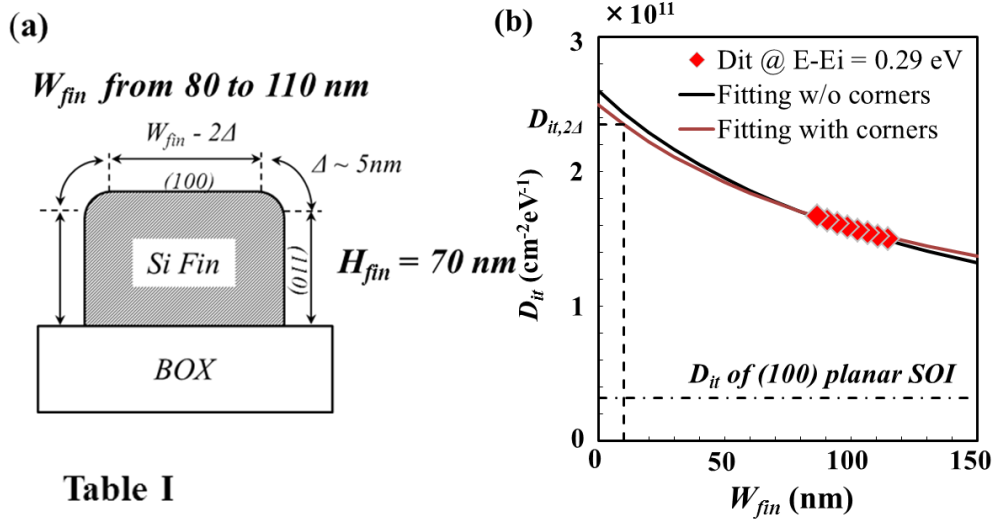


Table I

	$D_{it,top}$ (100)	$D_{it,side}$ (110)	$D_{it,corner}$
w/o corners	1.3×10^{10} $\text{cm}^{-2}\text{eV}^{-1}$	2.6×10^{11} $\text{cm}^{-2}\text{eV}^{-1}$	--
with corners	3.2×10^{10} $\text{cm}^{-2}\text{eV}^{-1}$	2.3×10^{11} $\text{cm}^{-2}\text{eV}^{-1}$	3.0×10^{11} $\text{cm}^{-2}\text{eV}^{-1}$

Fig. 3.5 (a) Schematics of the three different components, i.e., the top wall, the side walls, and the corners constituting the surface of the Si fin with rectangular-like cross-sectional shape, and (b) extraction of the D_{it} at different surface components by fitting with and without considering the corner component using Eq. (3.3.1). The D_{it} extracted from the planar SOI device is labeled by the dash-dot line, the position of $D_{it}(W_{fin} = 2\Delta)$ is depicted by the dash line. **Table 3.1** summarizes the extracted local D_{it} in both cases of with and without considering the corner regions.

Figure 3.5(b) shows the comparison between the measured D_{it} as a function of W_{fin} and the fitted curve given by Eq. (3.3.1) with and without considering the corner parts. The extracted local D_{it} values are summarized in **Table 3.1**. For the fitted curve that ignores the contribution of the corners (shown as the back line in **Fig. 3.5(b)**), the extracted $D_{it,top}$ and $D_{it,side}$ is $1.3 \times 10^{10} \text{ cm}^{-2}\text{eV}^{-1}$ and $2.6 \times 10^{11} \text{ cm}^{-2}\text{eV}^{-1}$, respectively, at 0.29 eV above the intrinsic Fermi-level. However, the (100)-oriented planar counterpart shows D_{it} of $3.2 \times 10^{10} \text{ cm}^{-2}\text{eV}^{-1}$ at the same energy level, which is larger than the extracted $D_{it,top}$ without considering the corner parts. This discrepancy indicates that the fitting without incorporating the influence of the corner parts may lead to an underestimation of the $D_{it,top}$. Therefore, the influence of the corner parts has to be taken into account for proper evaluation of the spatial distribution of D_{it} on the 3D surface. The red line in **Fig. 3.5(b)** shows the fitted curve with consideration of the corner parts. Here, the Δ is estimated as about 5 nm from the SEM image, and the $D_{it,top}$ is set to $3.2 \times 10^{10} \text{ cm}^{-2}\text{eV}^{-1}$ in accordance with that of the planar one. Then, $D_{it,side}$ and $D_{it,corner}$ are adjusted to modulate the value of $D_{it}(W_{fin} = 2\Delta)$ to fit the experimental data. Although uncertainties still remain between $D_{it,side}$ and $D_{it,corner}$, the value of $D_{it,corner}$ is controlled at around $3.0 \times 10^{11} \text{ cm}^{-2}\text{eV}^{-1}$ according to the published result on the D_{it} of the Si nanowire with circular cross-section characterized at the same energy level by the charge pumping method [3.15]. The results from the fitted curve give $D_{it,side}$ of $2.3 \times 10^{11} \text{ cm}^{-2}\text{eV}^{-1}$ and $D_{it,corner}$ of $3.0 \times 10^{11} \text{ cm}^{-2}\text{eV}^{-1}$ as tabulated in **Table 3.1**. We see that without considering the corner components, the local D_{it} of the (100)-orientated top wall tends to be underestimated because the overestimation of the local D_{it} of the etched (110)-oriented side walls. This result also reveals that in addition to the etched (110)-oriented side walls, the existence of the corner parts is also an important reason for the high D_{it} at the surfaces of Si fins, especially of those with highly scaled widths and heights.

3.4 Conclusion

In this study, the gated p-i-n diode is adapted to directly measure the D_{it} of 3D Si fins structure using the charge pumping method. We have verified the feasibility of low temperature F.G. annealing for passivation of Si dangling bonds at 3D surfaces with optimal temperature of 420 °C. Furthermore, a new methodology for quantitatively estimating the local D_{it} of different region of 3D structure has been proposed by characterizing fin structures with varying widths and the planar counterparts. Our results reveal that although the length of the corner parts only accounts for a small ratio of the total peripheral length, it still plays a crucial role for the distribution of the local interface states because substantially high D_{it} are situated at the corners. Particularly, without considering the high D_{it} at the corners, the D_{it} at etched side walls might be overestimated.

Future work on interface states of Si fins with different heights is needed. This future work could focus on the direct extraction of the D_{it} of the side walls with a similar method, and eventually lead to a more accurate local D_{it} profile at the 3D surfaces. Since the optimal curvature of the corner parts for lowering interface states is still questionable, this technique can help to extract the local D_{it} at the corners and thus provide guidelines for corner-shape optimization by additional processes, such as sacrificial oxidation [3.16] and hydrogen annealing [3.17].

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Chapter 4: Study of oxide border traps in high- k /InGaAs MOS capacitor by C - V measurement

In this chapter, we have systematically studied the frequency dispersion of the capacitance-voltage (C - V) characteristics of $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ metal-oxide-semiconductor (MOS) capacitors in accumulation region at various temperatures based on a distributed border traps model. An empirical method to evaluate the frequency and temperature dependent response of the border traps distributed along the depth from the interface into the oxide is established. While the frequency dependent response results from the dependence of the time constant of the border traps on their depths, the temperature dependent response is ascribed to the thermal activated capture cross-section of the border traps due to the phonon-related inelastic capturing process. Consequently, it is revealed that the frequency dispersion behaviors of the accumulation capacitance at different temperatures actually reflect the spatial distribution of the border traps. On this basis, we propose a methodology to extract the border trap distribution in energy and space with emphasis on analyzing the C - V characteristics measured from low to high temperatures in sequence.

4.1 Introduction

III-V compound semiconductors, such as $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$, are extensively studied as alternative channel materials of n-type metal-oxide-semiconductor field-effect transistors (n-MOSFETs) for future high-speed, low-power logic applications due to their intrinsic high electron mobility [4.1-4.5]. While a great deal of research effort still focuses on further passivation of the interface traps in high- κ /III-V gate stacks, another critical challenge arouses increasing attention comes from the oxide border traps, namely the near interfacial bulk traps that reside in the high- κ dielectrics [4.5-4.14]. Particularly, a high concentration of electrically active border traps may be located near and above the conduction band minima of the III-V substrates [4.5, 4.11]. Due to the relatively low density of states in the conduction band of the III-V semiconductors, the Fermi-level has to travel deeply into the conduction band to form sufficient amount of carriers at the surfaces [4.4]. Besides, because of the relatively small band-offset in high- κ /III-V interfaces compared to that of SiO_2/Si interfaces, the border traps in the high- κ dielectric can easily interact with the mobile carriers in the substrate when the Fermi-level is biased near or above conduction band minima[4.14].Therefore, oxide border traps charging may lead to severe on-state performance deterioration in the III-V based n-MOSFETs by pinning the Fermi-level inside the conduction band [4.4], degrades the mobility by remote coulomb scattering, and also leads to the threshold voltage instability[4.5, 4.14, 4.16]. Consequently, it is of significant importance to profile the distribution of border traps in energy and space near and above the conduction band edge of the III-V substrates in MOS devices.

In C - V characteristics of high- κ /III-V MOS capacitors with n-type substrates, the exchange of mobile carriers between the border traps and the conduction band states through tunneling process is considered responsible for the commonly existed frequency dispersion in accumulation region [4.6-4.12], as schematically shown in **Fig. 4.1**. Equivalent circuits for MOS capacitors with border traps distributed though the depth of the oxide have been developed [4.7-4.12], which successfully reproduces the frequency

dispersion of C - V and conductance-voltage (G - V) curves in accumulation observed in experiments. However, although the frequency dispersion induced by border traps is supposed to be independent on temperature because of the direct tunneling based trapping/de-trapping process of border traps [4.6], sometimes considerable temperature dependency of the frequency dispersion behavior can be observed as shown in this study (**Fig. 4.4(b)**) as well as in other published works [4.3, 4.17], which is still poorly understood. Besides, the spatial distribution of border traps through the depth of the oxide and its influences on the frequency dispersion behaviors are also lack of discussions.

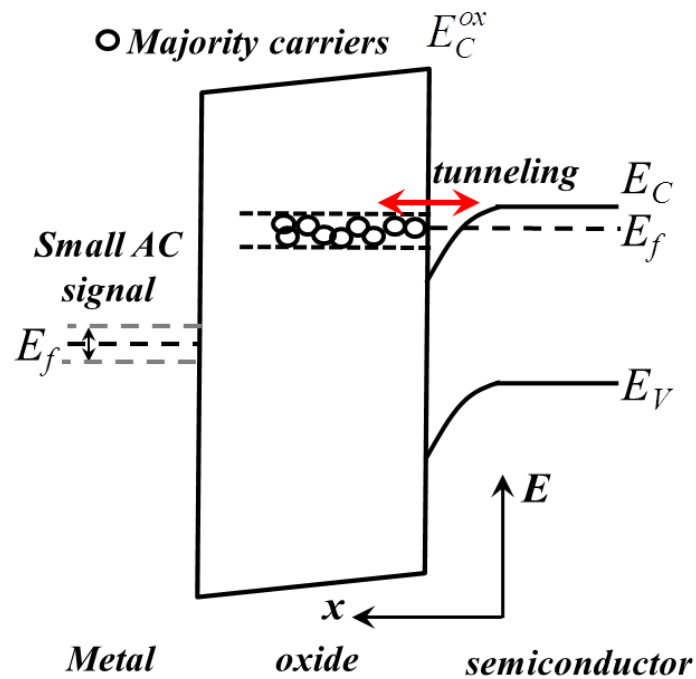


Fig. 4.1 Band diagram of an n-type InGaAs MOS capacitor biased in strong accumulation. When a small AC signal is applied to the metal electrode, as represented by the vertical arrow, the fermi-level in the semiconductor moves up and down and the mobile carriers can be exchanged between the border traps and the conduction band states through tunneling process.

In this study, by incorporating the consideration of the frequency and temperature dependent electrical response of border traps into a distributed border trap model [4.7-4.9], the frequency dispersion behaviors of C - V characteristics in accumulation of $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOS devices under a wide temperature range are investigated. We give deep insight into the trapping process of the border traps, and also develop a new methodology to extract the energy and spatial distribution of border traps near or above conduction band minimum. In section II, the samples preparation is described. In section III, the distributed border traps model for InGaAs MOS capacitors described in [4.6-4.8] is briefly introduced at first. Then an empirical method to evaluate the responses of border traps governed by the combined effect of frequency and temperature is presented. In section IV, we firstly validate the empirical method by analyzing the dependency on frequency and temperature of experimentally measured accumulation capacitance. On this basis, a three-step methodology for extracting the border traps distribution in energy and space directly from C - V characteristics at various temperatures is proposed. The extracted distribution profile of border traps is then discussed in details. Finally, the conclusion is made in the last section.

4.2 Sample preparation

The $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOS devices characterized in this study have a dual-layer gate insulator consisting of a 2-nm-thick GdAl_2O_3 layer and a 2-nm-thick HfO_2 layer. While the

GdAl₂O₃ layer is used to realize good interfacial properties with In_{0.53}Ga_{0.47}As, the HfO₂ layer is adopted for higher dielectric constant. The devices are fabricated on *n*-type ($5 \times 10^{16} \text{ cm}^{-3}$) In_{0.53}Ga_{0.47}As layer grown on *n*-type ($2 \times 10^{17} \text{ cm}^{-3}$) InP substrate. After carrying out sulfur-based wet-chemical treatment for surface passivation, the GdAl₂O₃ layer and the HfO₂ layer are successively formed by atomic layer deposition (ALD) at 300 °C. Then TiN metal dots with diameters of 50 nm are deposited through a lift off process by sputtering at room temperature. Finally, the full stacks are annealed in forming gas at 400 °C for 5 min. The *C-V* and *G-V* characteristics of the devices are measured by Agilent 4280A LCR meter with frequency ranging from 100 Hz to 1 MHz in a cryostat probe station equipped with liquid N₂ cooling. Note that the measured conductance is the equivalent parallel conductance of the device under test.

4.3 Model description

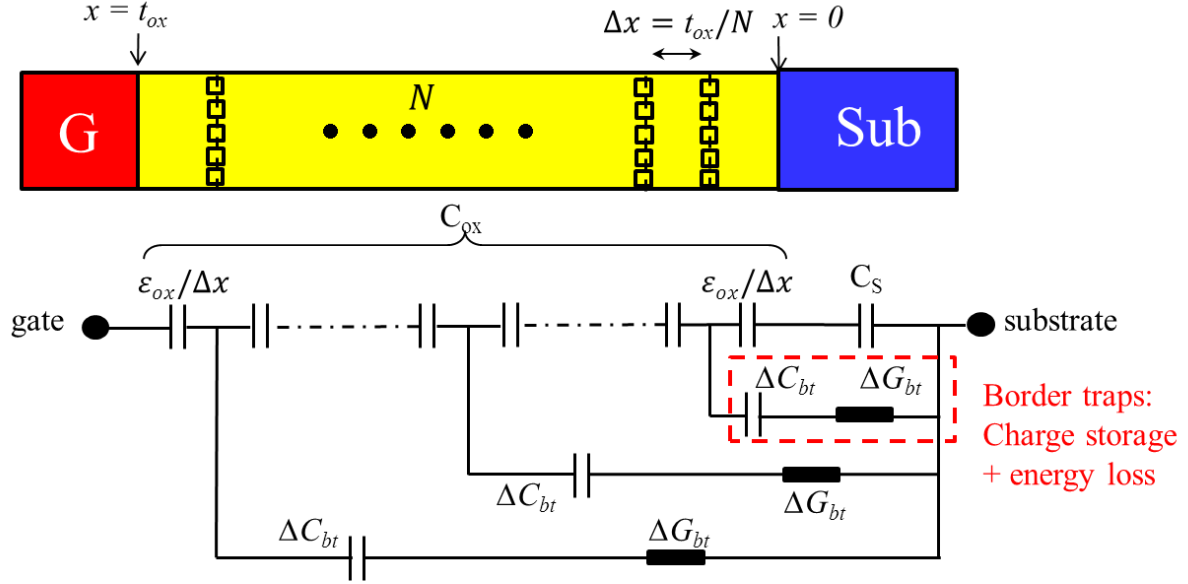


Fig. 4.2 The equivalent circuit for calculating the admittance characteristics in accumulation region for an MOS capacitor with border traps distributed through the thickness of the oxide [4.7, 4.8].

In order to quantitatively evaluate the distribution of border traps concentration, we adopted a distributed border traps model presented by Yuan *et al.* [4.7, 4.8] (**Fig. 4.2**) to calculate the admittance characteristics of an n-type MOS capacitor with border traps and compare them with experimental results. In this model, the gate oxide with thickness of t_{ox} is divided into a large number of pieces (N) with thickness of Δx for each one, and the influences of the border traps distributed in the oxide are represented by the series connected capacitor ΔC_{bt} and conductor ΔG_{bt} to model the border traps induced charge storage and energy loss. Here, for $t_{ox} = 4$ nm, N is set to 2000 to assure that $\Delta x = 2 \times 10^{-3}$ nm can be seen as an infinitesimal.

To numerically calculate the total admittance characteristics of the circuit at a given gate voltage (V_g), following key parameters are required: (1) E_f , which is the fermi-level position at the interface and also directly defines the energy level (E) of the detected border traps;

(2) C_{ox} and t_{ox} , which are the intrinsic oxide capacitance without the influence of border traps and the physical thickness of the gate oxide, respectively; (3) $C_s(E_f)$, which is the semiconductor capacitance depends on E_f ; (4) $N_{bt}(E, x)$, which is the volume density of the border traps at a distance of x from the interface into the oxide with energy level of E ; and (5) $\tau_{bt}(E, x)$, which is the time constant of the border traps located at x with energy level of E . In addition, B. Yu et al. [4.9] recently pointed out that although the existence of series resistance in real devices may be too small to influence measured capacitance, it plays a significant role on measured high-frequency conductance. Therefore, to successfully modeling the frequency dispersion of accumulation conductance, additional conductance component (G_{Ln}) represents the influence of dielectric tunneling leakage and series resistance (R_s) has to be taken into consideration [4.9]. In this study, we mainly focus on fitting the capacitance versus frequency data, $C(\omega)$. The fitting of conductance versus frequency data, $G(\omega)$, is also carried out to further validate the parameters extraction.

In this model, it is apparent that the strong dependence on frequency and temperature of the C - V in accumulation of the InGaAs MOS capacitors observed in our experiments (**Fig. 4.4(b)**) cannot be explained either by C_{ox} and $N_{bt}(E, x)$, which are the intrinsic properties of the oxide. It also cannot be ascribed to the C_s in accumulation because majority carriers can immediately response to the ac signal and once the E_f has been well biased above E_C , the occupation of the conduction band states is not sensitive to the variation of temperature. Therefore, the considerable temperature dependence of the frequency dispersion of the accumulation capacitance is most likely to result from the combined effects of frequency and temperature on the response of border traps controlled by τ_{bt} .

Particularly, τ_{bt} describes the average time that an empty trap needs to wait before it captures an electron [4.12], and it is exponentially proportional to the depth from the interface into the oxide of the trap, and can be given by [4.18]:

$$\tau_{bt}(E, x) = \tau_0(E) e^{2\kappa(E)x}, \text{ with } \kappa(E) = \sqrt{2m^*(E_C^{ox} - E)} / \hbar \quad \text{Eq. (4.3.1)}$$

Here, τ_0 is the time constant of the interface trap at the same energy level, κ is the attenuation coefficient in the electron wave function for tunneling process, which is determined by the effective electron mass (m^*) in the oxide, the tunneling barrier decided by the conduction band edges of the oxide (E_c^{ox}) and the trap energy (E), and the reduced plank constant (\hbar). Furthermore, τ_0 can be given by:

$$\tau_0 = (n_s \sigma v_{th})^{-1} \quad \text{Eq. (4.3.2)}$$

where n_s is the electron density at the semiconductor surface, σ is the electron capture cross-section of the border traps, and v_{th} is electron thermal velocity. In order to clearly illustrate the combined effects of frequency and temperature on the response of the border traps governed by τ_0 as discussed below, we used an extremely simplified approximation that assumes n_s is roughly equivalent to the density of states of the conduction band (N_C) of $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ when the MOS capacitor is biased in accumulation. Note that $n_s \approx N_C$ is a good approximation when E_f is biased near the conduction band edge (E_C), and when $E_f \gg E_c$ in strong accumulation, n_s can be several times larger than N_C . Therefore, although using $n_s \approx N_C$ condition can be used to be estimated the magnitude of τ_0 , the specific values of τ_0 need to be determined by fitting the $C(w)$ and $G(w)$ data. In addition, the $n_s \approx N_C$ approximation still can be used to evaluate the changing ratio of τ_0 or σ as a function of temperature as shown in the later section.

The frequency dependent electrical response of border traps can be simply estimated by considering the dependence of τ_{bt} on the depth from the interface into the oxide. When an ac small signal with angular frequency of w is applied, the border traps that reside deeply into the oxide with τ_{bt} larger than $1/w$ are not likely to response, and only those in the near interfacial region with τ_{bt} smaller than $1/w$ can change their occupancy according to the ac signal [4.13, 4.15]. Consequently, the probing depth, X_P , for border traps of a given measuring frequency (f) can be derived from the $w\tau_{bt} = 1$ condition together with Eq. (4.3.1):

$$X_P = \frac{I}{2\kappa} \ln \frac{I}{2\pi f \tau_0} \quad \text{Eq. (4.3.3)}$$

On the other hand, the temperature dependent response of border traps with energy level near or above conduction band minimum is inferred to be mainly caused by the temperature dependence of τ_0 due to the variation of the capture cross-section. As seen from Eq. (4.3.1), κ is a temperature independent value and thus the temperature dependence of τ_{bt} should come from $\tau_0 \approx (N_C \sigma v_{th})^{-1}$. Here, because N_C and v_{th} is also weakly temperature dependent ($N_C \sim T^{1.5}$, $v_{th} \sim T^{0.5}$, where T represents absolute temperature [4.19]), the pronounced temperature dependence of τ_0 is most likely to be caused by the thermal activated capture cross-section due to the energy relaxation associated with phonon-related process, such as multi-phonon emission, after trap ionization [4.20, 4.21]. In this case, the capture cross-section can be empirically expressed by [4.22]:

$$\sigma = \sigma_0 \exp\left(-\frac{E_b}{kT}\right) \quad \text{Eq. (4.3.4)}$$

where σ_0 is the pre-factor that equals to capture cross-section at infinitely high temperature, E_b is the thermal activation energy and k is Boltzmann constant. Usually, E_b is in orders of 10 to 10^2 meV [4.20, 4.21]. In consequence, the temperature dependence of τ_0 with consideration of the temperature dependence of N_C , v_{th} , and σ can be expressed as:

$$\tau_0(T) = \left\{ N_{C0} \left(\frac{T}{T_0}\right)^{1.5} v_{th0} \left(\frac{T}{T_0}\right)^{0.5} \sigma_0 \exp\left(-\frac{E_b}{kT}\right) \right\}^{-1} \quad \text{Eq. (4.3.5)}$$

where N_{C0} and v_{th0} denote the density of states in conduction band and the electron thermal velocity at a given temperature T_0 .

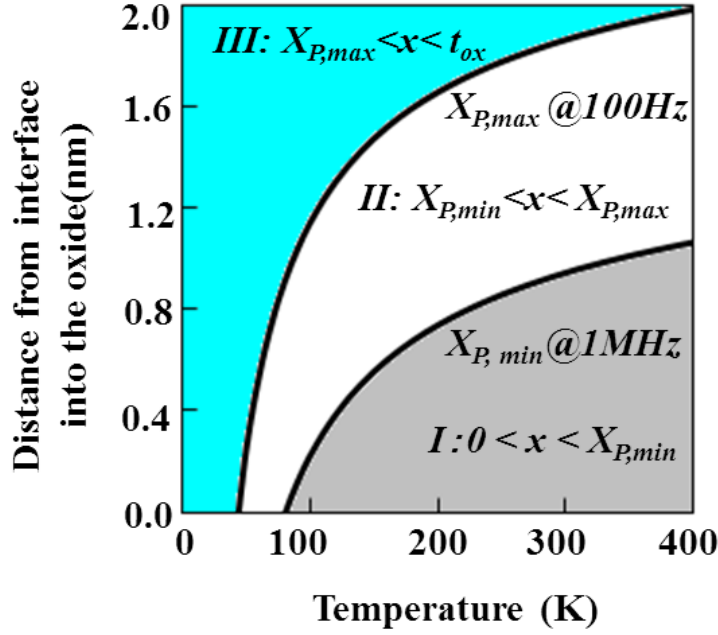


Fig. 4.3 Estimated probing depth of the 100 Hz and 1 MHz ac signal as a function of temperature by using Eq. (4.3.3) and Eq. (4.3.5). The parameters adopted here are applicable for an n-In_{0.53}Ga_{0.47}As MOS capacitor biased in accumulation. ($N_c = 2.2 \times 10^{17}$ cm⁻³, $v_{th} = 5.6 \times 10^7$ cm/s, $\sigma_n = 6 \times 10^{-15}$ cm² for In_{0.53}Ga_{0.47}As at 300 K [4.19], and $E_b = 65$ meV).

As a result, it can be clearly seen from Eq. (4.3.3) and Eq. (4.3.5), the response of border traps distributed through the thickness of the oxide is decided together by frequency and temperature. **Figure 4.3** shows the estimated probing depth of the 100 Hz and 1 MHz ac signals as a function of temperature by adopting the parameters that are applicable for an n-In_{0.53}Ga_{0.47}As MOS capacitor biased in accumulation. There are several observations listed as follows. Firstly, the probing depth decreases with increasing frequency or decreasing temperature. Secondly, in the multi-frequency *C-V* measurement between 100 Hz and 1 MHz, three regions along the depth of the oxide can be divided according to the influence of the border traps on measured capacitance: *Region I* is the region between the interface and the minimum probing depth ($X_{P,min}$) determined by the 1MHz signal. The trapping/de-

trapping processes of the border traps in this region are fast enough to contribute to the capacitance at all frequencies below 1 MHz and do not add to the dispersion; *Region II* is the region between the $X_{P,min}$ and the maximum probing depth ($X_{P,max}$) determined by 100Hz signal. The border traps in this region directly contribute to the observed frequency dispersion of the capacitance and thus decide the magnitude of the frequency dispersion; and *Region III* is the region between the $X_{P,max}$ to the total physical thickness of the oxide. The border traps in this region are not likely to respond and thus hardly exert influence on measured capacitance. Thirdly, as temperature decreases, the *Region II* effectively moves toward the interface, and thus the temperature dependent frequency dispersion of the $C-V$ curves may reflect the spatial distribution of border traps. Lastly, the probing depth can decrease to zero at sufficiently low temperature or high frequency. It means that in this case, all of the influences of border traps can be excluded, thus the intrinsic capacitance of the MOS system can be measured.

Thereby, an admittance model for the MOS capacitors with border traps distributed through the depth of the oxide, together with an empirical method to evaluate frequency and temperature dependent responses of border traps, has been established. In the following section, we firstly demonstrate this empirical method by analyzing the experimentally observed $C-V$ curves in accumulation at various temperatures. Then a three-step methodology is developed to extract the border trap distribution in energy and space for evaluating the oxide quality. Finally, the extracted distribution profile is discussed in details.

4.4 Results and discussion

4.4.1 Temperature and frequency dependence of C - V in accumulation region.

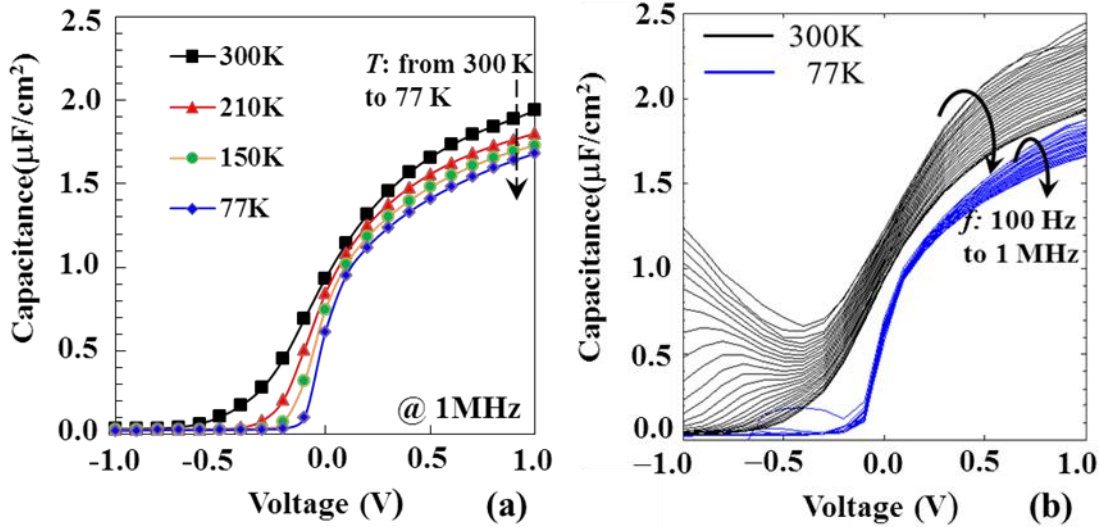


Fig. 4.4 The C - V characteristics of the fabricated n-type $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOS capacitor. (a) high-frequency (1 MHz) C - V at 300 K, 210 K, 150 K and 77 K, and (b) multi-frequency C - V at 300 K and 77 K with 26 characterizing frequencies that logarithmically varies from 100 Hz to 1 MHz. All of the C - V measurements in this study are carried out by sweeping V_g from -1 V to 1 V .

Figure 4.4(a) shows the 1 MHz C - V characteristics of our sample, which is an MOS capacitor on n-type $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$, measured at 300 K, 210 K, 150 K and 77 K, respectively. It can be seen that the accumulation capacitance decreases with decreasing temperature. In addition, there is no obvious flat-band voltage shift of the C - V curves as temperature changes from 300 K to 77 K, which indicates that the V_g - E_f relationship is not strongly temperature dependent and it is justifiable to compare the capacitance measured at same voltage but different temperatures. **Figure 4.4(b)** further shows the multi-frequency C - V curves (100 Hz to 1 MHz) of the sample at 300 K and 77 K. Strong frequency dispersion of the C - V curves can be observed from depletion region to accumulation region and the

dispersion magnitude substantially reduced at low temperature. While the C - V behaviors in depletion region can be attributed to the interface traps inside the band-gap [4.23, 4.24], that in accumulation can be interpreted from the viewpoint of the responses of the border traps. The decreased accumulation capacitance with increasing frequency or decreasing temperature can be explained by the dependence of the probing depth on $\omega\tau_0$, Eq. (4.3.3). When $\omega\tau_0 \sim 1$, the probing depth is near zero. No border traps can respond and the observed capacitance approaches the intrinsic (infinite frequency) value, $C_{ox}C_s/(C_{ox} + C_s)$. As $\omega\tau_0$ decreases, either because of lower frequency or because of shorter τ_0 at higher temperature, the probing depth increases thus adding more border trap contribution to the observed capacitance.

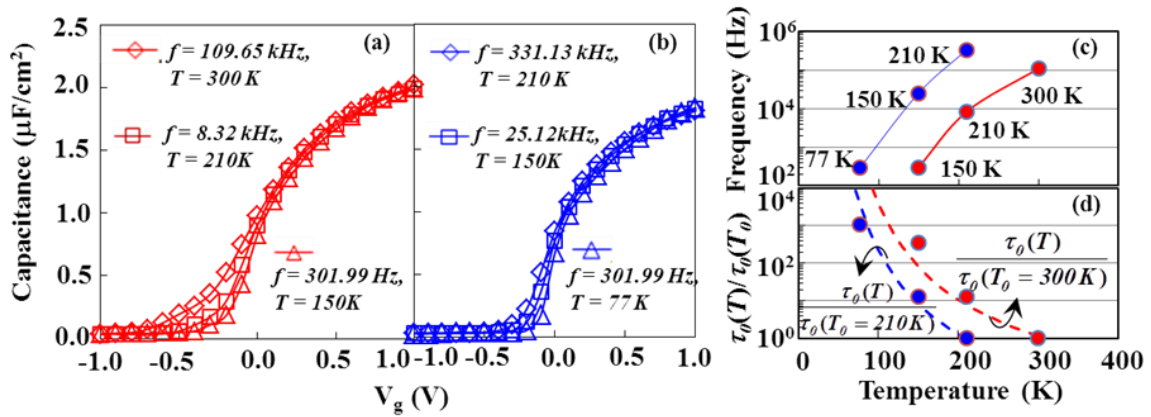


Fig. 4.5 The C - V curves with proper frequencies that have almost same capacitance in accumulation region measured at (a) 300 K, 210 K, and 150 K (red symbols), and (b) 210 K, 150 K, and 77 K (blue symbols). (c) The frequencies of the C - V curves used in (a) and (b) are plotted as a function of temperature by red and blue symbols, respectively. (d) The changing ratios of τ_0 as a function of temperature evaluated from the experiment (symbols) and the fitting curves (dash line) calculated by Eq. (6) using $E_b = 65$ meV as the temperature changes from 300 K, 210 K to 150 K (red) and from 210 K, 150 K, 77 K (blue).

Furthermore, as shown in **Fig. 4.3**, because the probing depth is determined by both of frequency and temperature, the same probing depth, or the similar responding behavior of border traps, is capable to be achieved by different combinations of frequency and temperature only if $w\tau_0(T)$ can be kept the same as shown by Eq. (3). Additionally, because the C_s in accumulation is not strongly temperature dependent, similar total accumulation capacitance, decided by C_s , C_{ox} , and the capacitance contributed by border traps, should be able to be approximately reproduced at different combinations of temperatures and frequencies that correspond to certain identical probing depth. The C - V curves measured under two sets of combinations of frequencies and temperatures that give similar accumulation capacitance of the sample are shown in **Figs. 4.5 (a) and (b)** with temperature changes from (a) 300 K, 210 K, to 150 K, and (b) 210 K, 150 K, to 77 K. It shows that by choosing proper frequencies, the C - V curves measured at different temperatures indeed can closely match with each other in accumulation region. It also shows that the C - V characteristics in the depletion region cannot be reproduced at the same time. It is caused by two effects due to the fact that the occupation probability of the conduction band states governed by the Fermi-Dirac distribution is a more sensitive function of temperature when E_f is biased near mid-gap compared to that when E_f is biased inside the conduction band. Firstly, the τ_0 of the traps near the mid-gap has stronger temperature dependence than that of the traps inside the conduction band [4.3, 4.24]. Secondly, C_s in depletion is also more sensitive to the variation of temperature compared to C_s in accumulation.

The characteristic frequencies that give similar accumulation capacitance as temperature changes from 300 K, 210 K, to 150 K and from 210 K, 150 K, and 77 K, as shown in **Figs.4.5 (a) and (b)**, are plotted in **Fig. 4.5 (c)** as a function of temperature. It can be seen that in order to achieve almost same accumulation capacitance with decreasing temperature, the characteristic frequency decreases almost exponentially. In addition, because each combination corresponds to the nearly same probing depth, namely the same $w\tau_0(T)$, the changing ratio of τ_0 as a function of temperature can be experimentally estimated from the

characteristic frequency that gives similar accumulation capacitance at different temperature by $\tau_0(T)/\tau_0(T_0) = f(T_0)/f(T)$. **Figure 4.5(d)** shows experimentally estimated $\tau_0(T)/\tau_0(T_0=300 \text{ K})$ (red symbols) and $\tau_0(T)/\tau_0(T_0=210 \text{ K})$ (blue symbols), which should also be able to be fitted by following relationship derived from Eq. (4.3.5):

$$\frac{\tau_0(T)}{\tau_0(T_0)} = \left(\frac{T_0}{T}\right)^2 \exp\left(\frac{E_b}{kT} - \frac{E_b}{kT_0}\right) \quad \text{Eq. (4.4.1)}$$

By setting $E_b = 65 \text{ meV}$, the changing ratios of τ_0 as a function of temperature can be well fitted as shown by the dash line in **Fig. 4.5(d)**. These results not only further demonstrate previously proposed model, but also provide a method to evaluate the change of τ_0 as a function of temperature. For this sample, it is evaluated that the τ_0 is enlarged by a factor about 10^3 mainly due to the shrinking of σ as temperature decreases from 300 K to 77 K.

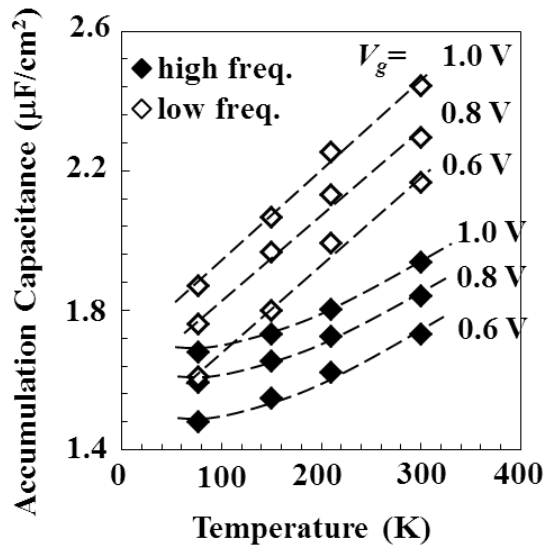


Fig. 4.6 The accumulation capacitance measured at $V_g = 1.0 \text{ V}$, 0.8 V , and 0.6 V by the high frequency signal of 1 MHz , (the solid symbols) and the low frequency signal of 100 Hz , (the open symbols) as a function of temperature, respectively

Since the τ_0 is about $10^{-9} \text{ s} \sim 10^{-10} \text{ s}$ for the border traps inside the conduction band of $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ at 300 K , it could be enlarged to 10^{-6} s to 10^{-7} s at 77 K according to previous

estimation. It is indicative that the $w\tau_0 \sim 1$ condition for measuring the intrinsic accumulation capacitance of the MOS systems without the influences of the border traps can be satisfied by using the 1 MHz signal at 77 K. **Figure 4.6** shows the accumulation capacitance measured by the 1 MHz (solid) and 100 Hz (open) signal as a function of temperature. It can be observed that while the accumulation capacitance measured by the 100 Hz signal continues to decrease as temperature decreases from 300 K to 77 K, the reduction of the accumulation capacitance measured by the 1 MHz signal tends to get saturated around 77 K. This observation is consistent with aforementioned analysis that the intrinsic capacitance can be sufficiently approached by the 1 MHz/77 K measurement.

4.4.2 Methodology for extracting the border traps distribution in energy and space

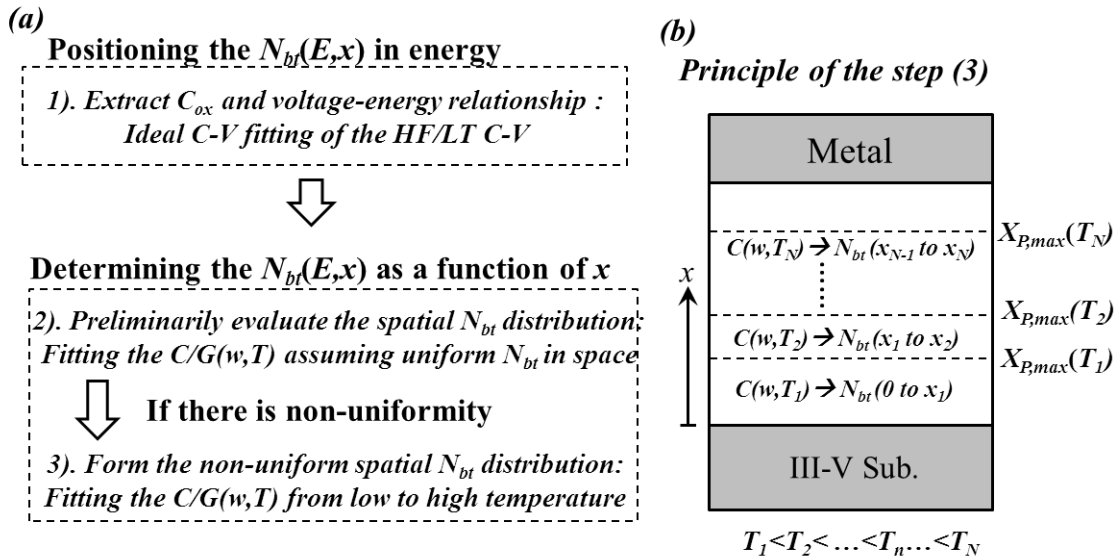


Fig. 4.7 (a) Proposed three-step methodology for extracting the border traps distribution in energy and space, and (b) The principle of the step 3. The N_{bt} from interface into the oxide can be gradually detected by analyzing the C - V characteristics measured from low to high temperatures with expanding the maximum probing depth, $X_{P,max}$.

Based on previous discussion, adopting the border traps model with considerations of the frequency and temperature dependent response of border traps, we propose a three-step methodology to extract the border traps distribution in energy and space. **Figure 4.7(a)** shows the flow chart of the methodology. Firstly, the C_{ox} and voltage-energy relationship are evaluated from high-frequency (H.F.) and low-temperature (L.T.) C - V . The extracted voltage-energy relationship is not only used to positioning the N_{bt} extracted later in energy, but also required to evaluate some of the input parameters of the border traps model, such as C_s and κ . Secondly, the $C/G(w)$ at different temperatures are preliminarily fitted by the border traps model with assuming uniformly distributed N_{bt} to judge if there is non-uniformly distributed N_{bt} spatial profile. Finally, if the previous step indicates non-uniform distribution of N_{bt} , the non-uniform spatial distribution of N_{bt} is gradually formed from the interface into the oxide by fitting $C/G(w)$ measured from low to high temperatures. The three main steps are discussed in details as follows.

(1) Extraction of C_{ox} and voltage-energy relationship

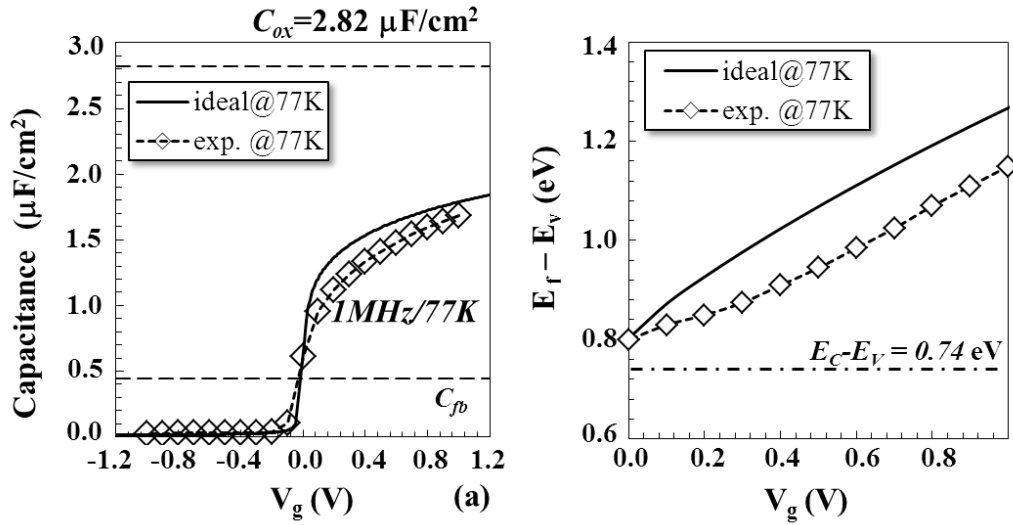


Fig. 4.8 (a) Comparison between the ideal C - V and the experimental 1MHz/77K C - V , and (b) the ideal voltage-energy relationship (solid line) and the extracted voltage-energy relationship (symbol) by using the Terman technique. The dash-dot line shows the position of the conduction band edge of $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$.

The considerable contribution of border traps on the accumulation capacitance in the C - V characteristics of InGaAs MOS capacitors leads to difficulties on correct evaluation of C_{ox} and comparison with the theoretically ideal C - V [4.4], which is crucial to extract the voltage-energy relationship and model the total admittance characteristics of the devices. Therefore, we firstly propose to extract the C_{ox} and the voltage-energy relationship by comparison the ideal C - V with the H.F./L.T. C - V that is able to thoroughly screen the contribution of border traps. A simple judgment to see if the influence of border traps has been sufficiently excluded is observing the reduction of high-frequency capacitance in accumulation with decreasing temperature. Once the reduction of the accumulation capacitance begins to saturate as temperature decreases to a certain degree, as shown by the 1 MHz data at 77 K in **Fig. 4.6**, it indicates the intrinsic capacitance of the MOS system has been sufficiently approached. **Figure 4.8(a)** shows the comparison between the 1 MHz/77 K C - V and the ideal C - V at 77 K, which gives $C_{ox} = 2.82 \mu\text{F}/\text{cm}^2$. The ideal C - V is calculated based on a Poisson solver presented by G.Brammertz et al.[4.25]. **Figure 4.8(b)** shows the extracted voltage-energy relationship in accumulation by the Terman technique [4.26]. The result also verifies that the E_f has indeed traveled far into the conduction band in InGaAs MOS capacitors in strong accumulation.

Besides, the extracted voltage-energy relationship at the low temperature is considered can be approximately used as that at increased temperatures due to following reasons. (1) For the sample under test, the flat-band voltage of the C - V curves almost show no obvious temperature dependence as shown in **Fig. 4.4(a)**; (2) C_s , or the band bending situation, in accumulation is not strongly temperature dependent; and (3) as can be observed from **Fig. 4.4(b)**, the magnitude of frequency dispersion is a much more sensitive function of temperature than a function of voltage. It indicates that the dependence of N_{bt} distribution on space is much stronger than that on energy. Therefore, the extracted voltage-energy relationship from H.F./L.T. C - V is supposed to be applicable to position the N_{bt} extracted from the frequency dispersion of C - V curves measured at increased temperatures.

(2) Preliminary evaluation of the spatial distribution of N_{bt}

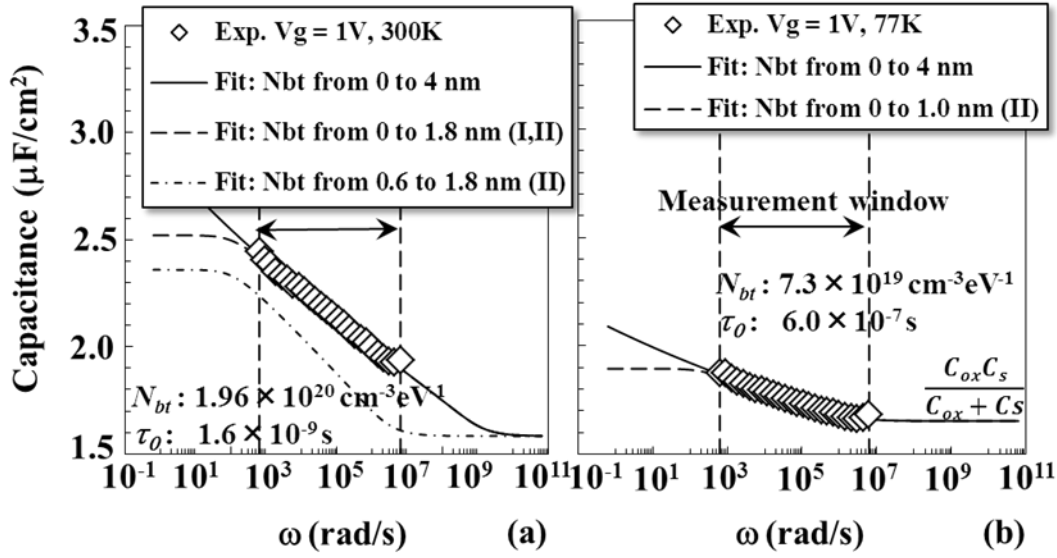


Fig. 4.9 Fitting of the $C(w)$ at $V_g = 1$ V at (a) 300 K and (b) 77 K, by the distributed border trap model with assuming uniform N_{bt} distributed in different regions. The fitting parameters are $C_s(E_f, T) = 3.61 \mu\text{F}/\text{cm}^2$, $\kappa(E) = 5.09 \text{ nm}^{-1}$, $N_{bt} = 1.96 \times 10^{20} \text{ cm}^{-3}$, $\tau_0 = 1.6 \times 10^{-9} \text{ s}$ for 300 K, and, $C_s(E_f, T) = 3.98 \mu\text{F}/\text{cm}^2$, $\kappa(E) = 4.95 \text{ nm}^{-1}$, $N_{bt} = 7.3 \times 10^{19} \text{ cm}^{-3}$, $\tau_0 = 6.0 \times 10^{-7} \text{ s}$ for 77 K. $E - E_V = 1.12 \text{ eV}$ and $C_{ox} = 2.82 \mu\text{F}/\text{cm}^2$ are used for both cases.

In order to preliminarily evaluate the spatial distribution of border traps, fitting of $C(w)$ in accumulation at different temperatures by the distributed border traps model with assuming uniformly distributed N_{bt} though the thickness of the whole oxide and different particular regions is carried out in this step. **Figure 4.9** shows the fitting results of the $C(w)$ with $V_g = 1$ V at (a) 300 K and (b) 77 K. For this fitting, E_f can be attained according the voltage-energy relationship evaluated in the previous step. Then the $\kappa(E)$ and $C_s(E_f, T)$ are calculated based on E_f by using Eq. (1) and the ideal C - V model. The N_{bt} and τ_0 are used as fitting parameters. As shown in **Fig. 4.9(a)**, measured $C(w)$ (symbols) can be well fitted by calculated $C(w)$ (solid line) using the model that assumes uniform spatial distribution N_{bt} . The extracted N_{bt} is $1.96 \times 10^{20} \text{ cm}^{-3}$ and τ_0 is $1.6 \times 10^{-9} \text{ s}$ at 300 K. Consequently, the range of *region II* is estimated to range from $x = 0.6 \text{ nm}$ to $x = 1.8 \text{ nm}$ according to extracted τ_0 .

The observed $C(w)$ also can be well fitted by only setting the N_{bt} in *Region I* and *II* (dash line), which verifies that the N_{bt} in *Region III* defined before has no influence in measurement frequency window. In addition, in case that N_{bt} is only set into *Region II*, the calculated $C(w)$ (dash-dot line) shifts downward and the magnitude of frequency dispersion almost keeps the same. It demonstrates that while the N_{bt} in *region I* contribution to additional capacitance, the N_{bt} in *region II* dominated the frequency dispersion magnitude. **Fig. 4.9(b)** shows fitting results of the $C(w)$ measured at the 77 K. Fairly nice fitting can be achieved by using $N_{bt} = 7.3 \times 10^{19} \text{ cm}^{-3}$ and $\tau_0 = 6.0 \times 10^{-7} \text{ s}$. In this case, the *region II* locates from $x = 0.0 \text{ nm}$ to $x = 1.0 \text{ nm}$ as temperature decreases to 77 K, and thus experimental data can be fitted by only setting N_{bt} in *region II*, as shown by the dash line in **Fig. 4.9(b)**.

However, there are two major discrepancies when we compare the fitting results at 300 K and 77 K. Firstly, although the *region II* at 300 K (0.6 ~ 1.8 nm) and that at 77 K (0 ~ 1.0 nm) overlap with each other, the N_{bt} extracted at 77 K is less than half of that extracted at 300 K. It indicates higher N_{bt} with increasing depth from the interface into the oxide. Secondly, the extracted τ_0 is enlarged by a factor about 3.7×10^2 as temperature decreases from 300 K to 77 K, which is smaller than the factor about 10^3 evaluated as shown in **Fig. 4.5(d)**. It also hints the existence of non-uniform spatial distribution of N_{bt} . In particular, since in the fitting of $C(w)$ at 300 K by assuming uniform N_{bt} , the N_{bt} in the near interfacial region tends to be overestimated, which may lead to the underestimation of the changing ratio of τ_0 as a function of temperature.

(3) Extraction of the non-uniform spatial distribution of N_{bt}

In this step, the $C(w)$ at $V_g = 1 \text{ V}$ is fitted again using the border traps model with non-uniform N_{bt} spatial distribution profile. The principle is schematically shown in **Fig. 4.7(b)**. The fitting starts from the $C(w)$ measured at low temperature (T_1) that the $X_{P,min}$ has sufficiently approached the interface, e.g. 77 K, and the N_{bt} profile from the interface ($X_{P,min} = 0 \text{ nm}$) to $X_{P,max}$ at T_1 is firstly formed. Then since the x_{max} can extend deeply into the oxide as temperature increases, the $C(w)$ measured at higher temperature of T_2 than T_1 can be fitted by adding the N_{bt} distribution profile from $X_{P,max}(T_1)$ to $X_{P,max}(T_2)$ while keeping

the same N_{bt} profile from the interface to $x_{max}(T_l)$. Thereby, by fitting the $C(w)$ and $G(w)$ measured at a series of temperatures from low to high in sequence, a continuous N_{bt} distribution profile can be gradually formed from the interface into the oxide using this method.

The fitting results extracted from $C(w)$ and $G(w)$ at 77 K, 150 K, 210 K and 300 K ($V_g = 1.0$ V) are shown in **Fig. 4.10**. **Figures 4.10(a) and (b)** show the comparison on frequency dispersion of capacitance (a) and conductance (b) at $V_g = 1$ V, measured at 77 K, 150 K, 210 K and 300 K, between experimental data (symbols) and fitted curves (lines) calculated by the distributed model using non-uniform distributed N_{bt} in space. **Figure 4.10(c)** shows the inputted τ_0 into the model (symbols) as a function of temperature, which is in accordance with our theoretical calculation using Eq. (4.3.5) (dash line). As measurement temperature decreases from 300 K to 77 K, τ_0 is estimated to be enlarged from 1.8×10^{-10} s to 6.0×10^{-7} s and σ approximately shrinks from 4.06×10^{-16} cm⁻² to 2.81×10^{-19} cm⁻² with thermal activation energy $E_b = 65$ meV. **Figure 4.10(d)** shows the inputted N_{bt} into the model (solid line) as a function of depth from the interface into the oxide. The vertical dash-dot lines in **Fig. 4.10(d)** show the $X_{P,max}$ at different temperatures estimated from the τ_0 shown in **Fig. 4.10(c)**. The horizontal dash lines in **Fig. 4.10(d)** show the extracted N_{bt} attained by fitting the $C(w)$ and $G(w)$ data assuming uniform distributed N_{bt} in space. Because the N_{bt} values attained by assuming uniform distribution indicate increasing N_{bt} from the interface into the oxide, linearly increased N_{bt} profiles as a function of the depth with different increasing rates are gradually filled into the interface to $X_{P,max}(77$ K), $X_{P,max}(77$ K) to $X_{P,max}(150$ K), $X_{P,max}(150$ K) to $X_{P,max}(210$ K), and $X_{P,max}(210$ K) to $X_{P,max}(300$ K) to fit the $C(w)$ and $G(w)$ at 77 K, 150 K, 210 K, and 300 K, respectively.

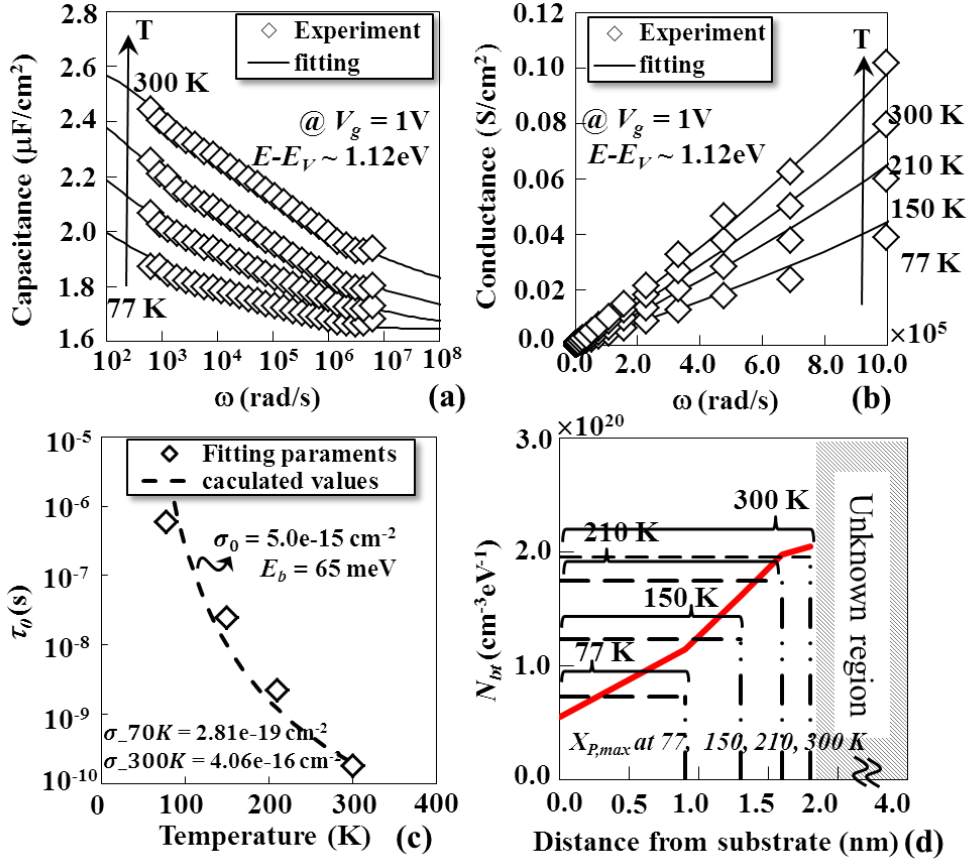


Fig. 4.10 Comparison on frequency dispersion of capacitance (a) and conductance (b) at $V_g = 1\text{V}$, measured at 77 K, 150 K, 210 K and 300K, between experimental data (symbols) and fitted curves calculated by the distributed model (lines). The inputted τ_0 (symbols) for the distributed model at different temperatures and the calculated curve (dash line) by using Eq. (5) with $N_c = 2.2 \times 10^{17} \text{cm}^{-3}$, $v_{th} = 5.6 \times 10^7 \text{cm/s}$, $\sigma_0 = 5 \times 10^{-15} \text{cm}^2$ and $E_b = 65 \text{meV}$ are shown in (c). The inputted N_{bt} profile (red line) for the distributed model is shown in (d). Besides, the vertical dash-dot lines in (d) show the evaluated maximum probing depth, $X_{P,max}$ at different temperatures using Eq. (3) with $\kappa = \kappa(E) = 5.09 \text{nm}^{-1}$, $f = 100 \text{Hz}$ and the τ_0 shown in (c), and the horizontal dash lines in (d) shown the N_{bt} extracted at different temperatures by assuming uniform N_{bt} spatial distribution. Additionally, except the influence of border traps, that of series resistance is also considered in the distributed model by using the parameters of $R_s = 6.6 \times 10^{-3} \Omega \cdot \text{cm}^2$ and $G_{Ln} = 1.2 \times 10^{-4} \text{S}/\text{cm}^2$.

4.4.3 Distribution profile of border traps in energy and space

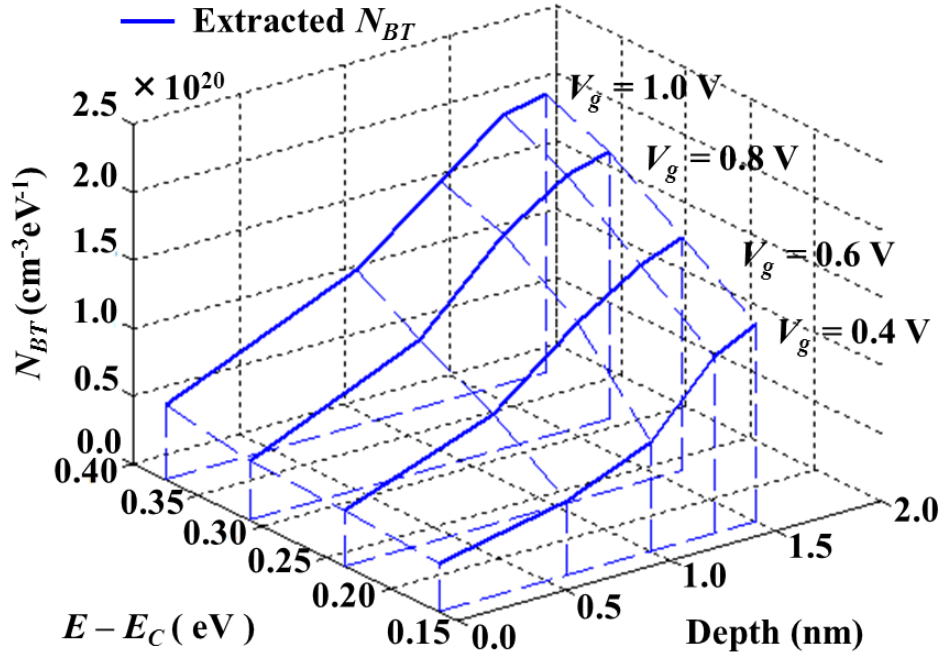


Fig. 4.11 The border traps distribution profile in energy and space extracted from the $C(w)$ and $G(w)$ dispersion data measured at 300 K, 210 K, 150 K, 77 K with $V_g = 0.4 \text{ V}$, 0.6 V , 0.8 V and 1.0 V .

Thereby, the distribution profile of border traps above the conduction band edge in energy and space can be evaluated by analyzing the capacitance- and conductance-frequency data at various V_g in accumulation measured from low to high temperatures using the methodology proposed above. The extracted distribution profile of border traps in the sample having TiN/HfO₂ (2 nm)/GdAl₂O₃(2 nm)/InGaAs structure is shown in **Fig. 4.11**. In the probing range of this measurement, high N_{bt} between 10^{19} cm^{-3} to 10^{20} cm^{-3} is found and it tends to increase with increasing energy or the depth into the oxide. The highest N_{bt} extracted in this study achieved $2.05 \times 10^{20} \text{ cm}^{-3}$ at about 0.37 eV above conduction band minima and 1.8 nm in the oxide from semiconductor interface. The increased N_{bt} with increasing depth into the oxide and relatively high N_{bt} in the sample is probably caused either by the accumulation of defects during oxide growth or the introduction of the gate

stack with dual-layer structure. Besides, the border traps distribution profile in III-V MOS devices extracted in this work is comparable to those extracted by using other techniques in III-V MOSFETs, such as AC transconductance [4.12-4.15] and low-frequency charge-pumping method [4.27]. Compared to those methods, this methodology provides a more convenient way to quickly evaluate the quality of the near interfacial oxide by from MOS capacitors. Additionally, it is noteworthy that high concentration of border traps on the order of 10^{20} cm^{-3} in high- κ dielectrics is not a peculiar feature of MOS devices with III-V substrates, similar results have also been reported in the HfO₂ layer in Si MOSFET with HfO₂/SiO₂ gate stack [4.28]. However, due to lack of high quality interfacial layer with large band-offset, such as the SiO₂ layer in the Si based MOS systems, the trapping/de-trapping of the border traps in high- κ dielectrics can play a more crucial role in the III-V MOS systems.

4.5 Conclusion

In summary, in order to profile the border traps distribution in energy and space in $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOS capacitors, an empirical method to evaluate the response of oxide border traps governed by the combined effect of frequency and temperature is established and incorporated into a distributed border traps model. While the frequency dependent response of border traps is attributed to the depth dependent τ_{bt} , the temperature dependence is inferred to result from the variation of τ_0 due to the thermal activated capture cross-section corresponding to phonon-related inelastic capturing process. A simple method to evaluate the change of τ_0 as a function of temperature from the characteristic frequencies that give very similar accumulation capacitance at different temperatures is also presented. Particularly, as temperature decreases from 300 K to 77 K, it is estimated that the τ_0 above the conduction band minimum of $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ increases from $10^{-9}\sim 10^{-10}\text{s}$ to $10^{-6}\sim 10^{-7}\text{s}$ mainly due to the shrinking of the capture cross-section. As for the methodology to extract the border traps distribution in energy and space, we propose to extract the voltage-energy relationship from the H.F./L.T. C - V and then gradually determining the spatial distribution of border traps from the interface into the oxide by analyzing the $C(w)$ and $G(w)$ measured from low to high temperatures in sequence. High concentration of border traps, which increases with increasing energy level and depth into the oxide, between 10^{19} cm^{-3} to 10^{20} cm^{-3} has been found in the sample with $\text{TiN}/\text{HfO}_2/\text{GdAl}_2\text{O}_3/\text{n-In}_{0.53}\text{Ga}_{0.47}\text{As}$ structure. These results reveal the significant necessity for further developing the high-quality gate dielectrics with low border traps concentration for boosting the performance of InGaAs MOSFETs. Besides, although this study focuses on InGaAs MOS capacitors, the methodology can be easily extended to other types of high-mobility substrates based MOS systems with electrically active oxide border traps and used as a convenient way to quantitatively evaluate the quality of the near interfacial oxide layer.

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Chapter 5: Study of oxide border traps and interface traps in high- k /InGaAs MOS capacitor by conductance method

In this chapter, we addressed with the influence of oxide border traps with energy level inside the band-gap on the admittance characteristics of the MOS capacitor biased in depletion region. In particular, for the MOS capacitors that are lack of interfacial layer with good quality and large band-offset, such as InGaAs based MOS systems, the parallel conductance curves probably show strong distortion and thus conventional conductance method that only takes account for the energy loss caused by interface traps may not be applicable and leads to considerable misunderstanding of the traps distribution. By analyzing the conductance curves measured at various temperatures with considerations on both of the interface traps and oxide traps, we have (1) confirm the oxide border traps response for the low-frequency signal by high temperatures measurement, (2) consistently fit the conductance curves at different temperatures and extract the D_{it} and N_{bt} values, and (3) propose a straight-forward way to decide the energy level of the near mid-gap traps.

5.1 Introduction

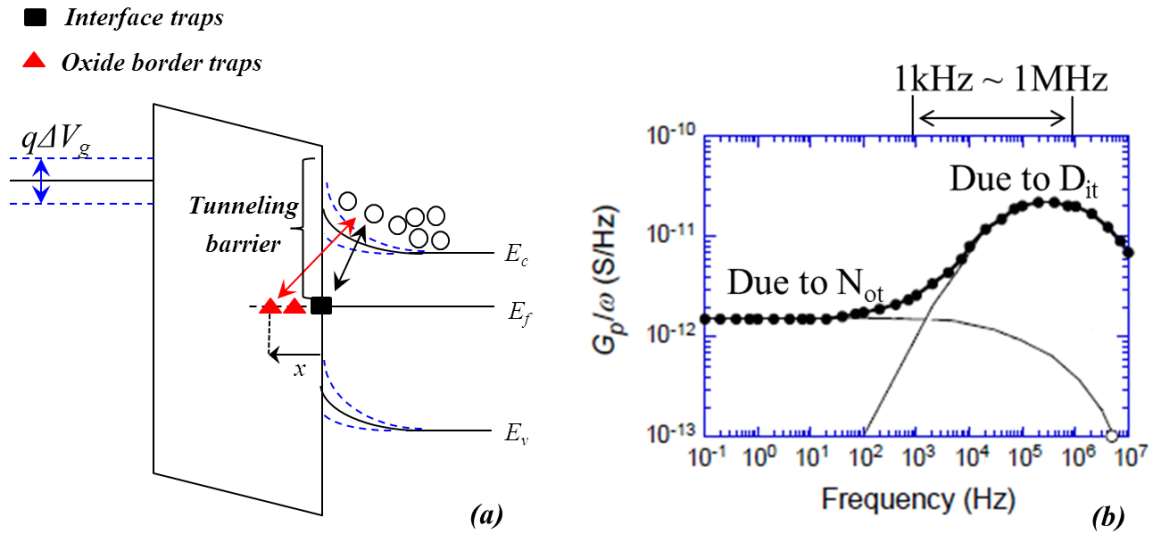


Fig. 5.1. (a) Band diagram of the MOS capacitor biased at the depletion condition with illustration of the trapping/de-trapping processes by interface and oxide traps under a small ac signal, and (b) typical parallel conductance versus frequency plot of a Al/SiO₂/Si MOS capacitor [5.3].

The conductance method proposed by Nicollian and Goetzberger [5.1, 5.2] is considered as one of the most accurate and sensitive way for charactering interface states distributed near mid-gap in the MOS devices. Theoretically, for an MOS capacitor biased in depletion subjected to an ac small signal, as shown in Fig. 5.1 (a), the majority carriers can be trapped or de-trapped by both of interface traps and oxide traps. Therefore, the energy loss caused by interface and oxide traps should be able to be observed in conductance measurement. However, since the relatively large tunneling barrier when fermi-level is biased inside the band-gap, the time constant of trapping by oxide traps is much longer than that caused by interface traps. Therefore, the oxide traps and interface traps are normally characterized in different measurement frequency window. Usually, in typical frequency window for conductance method ranges from 100 Hz to 1 MHz, interface traps are considered to dominate the conductance behavior. To investigate the influence of oxide trapping in the conductance measurement, M. J. Uren, et al. [5.3] carried out very low frequency

conductance measurement for an Al/SiO₂/Si MOS capacitor, as shown in Fig. 5.2 (b). It shows that in Si MOS capacitors, interface traps give rise to a peak in G_p/w versus w plot in the frequency range from 100 Hz to 10 MHz. On the other hand, oxide traps lead to a plateau in the low frequency range below 100 Hz.

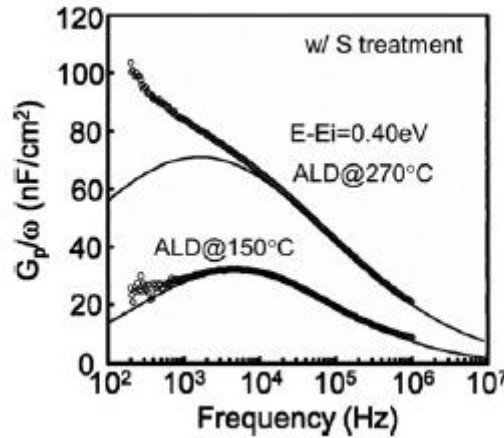


Fig. 5.2 The experimental (symbols) and fitted (lines) conductance curves of Al₂O₃/InP based MOS capacitors with same surface treatments and different gate dielectrics deposition parameters [5.4].

In case of InGaAs based MOS capacitor, considering the lack of thermal-dynamically stable interfacial layer with good quality and the relatively low band offset (SiO₂/Si: about 2.5 eV; Al₂O₃/In_{0.53}Ga_{0.47}As: about 2 eV), the oxide traps may play a more pronounced role in the parallel conductance behaviors and even exert influences on the frequency window that is overlapped with that of interface traps. Figure 5.4 shows the conductance curves of Al₂O₃/InP based MOS capacitors with same surface treatments and different gate dielectrics deposition parameters [5.4]. It can be seen that under certain gate dielectrics deposition condition, the G_p/w versus w plot distorted from typical the peak behaviors caused by interface traps and showed strong low frequency response, which is inferred to be caused by the responses of oxide traps [5.4]. Therefore, for III-V based MOS capacitors, due to the participation of a large amount of oxide traps, the conductance behaviors (G_p/w versus w)

in typical measurement frequency window ranges from 100 Hz to 1 MHz may show strong distortion and thus it is necessary to consider both of the influences of interface and oxide traps to precisely analyze the conductance behaviors.

5.2 Sample preparation

The $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOS devices characterized in this study are fabricated in Imec. It has a dual-layer gate insulator consisting of a 2-nm-thick GdAl_2O_3 layer and a 2-nm-thick HfO_2 layer. While the GdAl_2O_3 layer is used to realize good interfacial properties with $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$, the HfO_2 layer is adopted for higher dielectric constant. The devices are fabricated on n -type ($5 \times 10^{16} \text{ cm}^{-3}$) $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ layer grown on n -type ($2 \times 10^{17} \text{ cm}^{-3}$) InP substrate. After carrying out sulfur-based wet-chemical treatment for surface passivation, the GdAl_2O_3 layer and the HfO_2 layer are successively formed by atomic layer deposition (ALD). Finally, Pt metal dots with diameters of 50 μm are deposited through a lift off process. The admittance characteristics of the devices are measured by Agilent 4280A LCR meter.

For the under test $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOS devices with the n -type doping concentration of $5 \times 10^{16} \text{ cm}^{-3}$, the position of fermi-level can be easily estimated by:

$$E_C - E_f = kT \ln\left(\frac{N_C}{N_d}\right) \quad \text{Eq. (5.2.1)}$$

where N_d is the donor impurity density. By using $N_c = 2.1 \times 10^{17} \text{ cm}^{-3}$ for $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ and $N_d = 5.0 \times 10^{16} \text{ cm}^{-3}$, E_f is about 0.04 eV below the E_C .

5.3 Temperature dependent responses of interface and oxide traps

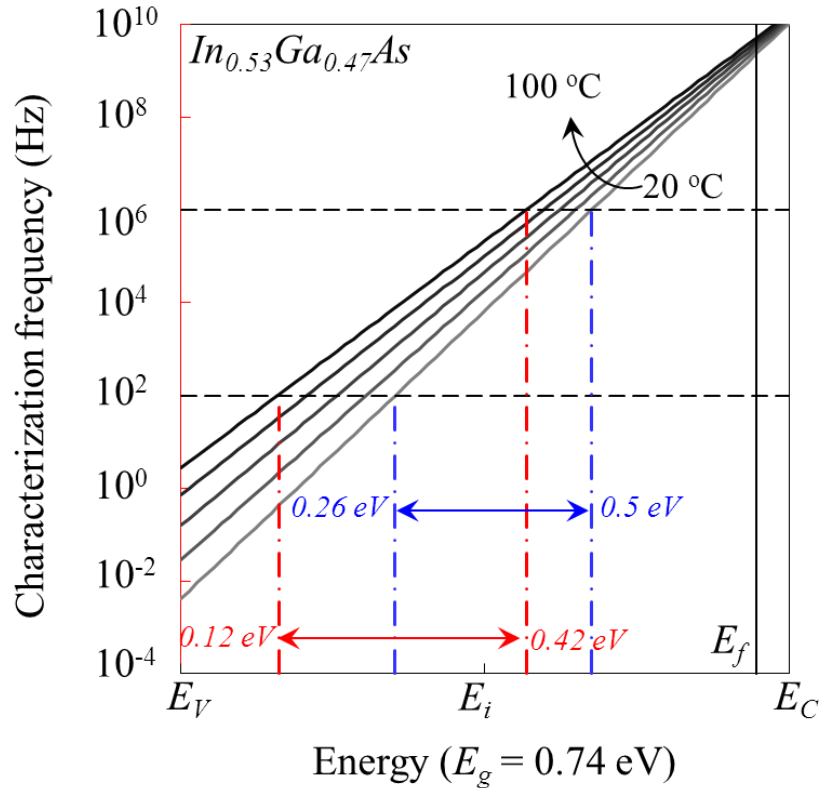


Fig. 5.3 Characteristic frequency of electron trapping by interface states as a function of the energy along the band-gap with temperature as a parameter in the InGaAs MOS capacitor. The commonly used measurement frequency window ranges from 100 Hz to 1 MHz is labeled by dash lines, and the corresponding energy ranges of the interface traps at 20 °C and 100 °C are also depicted by the blue and red dash-dot lines, respectively.

To confirm the responses of the oxide border traps for the low frequency ac signals, we propose to measure the AC admittance characteristics. The feature frequency of the interface traps with an energy level of E is defined as the frequency of the ac signal that the interface traps can change their occupancy in the corresponding period of the signal. In particular, the feature frequency of the electron trapping of the interface traps can be given by:

$$f = \frac{1}{2\pi\tau_{it}} = \frac{N_C v_{th} \sigma}{2\pi \exp(\Delta E/kT)} \quad \text{Eq. (5.3.1)}$$

Here, N_C is the density of states in the conductance band, v_{th} is the thermal velocity of electrons, σ is the electron capture cross-section of the interface traps, and ΔE is the different between the energy level of the interface traps and the conduction band edge ($\Delta E = E_C - E_T$). By using the commonly acceptable parameters of $N_C = 2.1 \times 10^{17} \text{ cm}^{-3}$, $v_{th} = 5.5 \times 10^7 \text{ cm/s}$, $\sigma = 6 \times 10^{-15} \text{ cm}^2$ for $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$, the feature frequency of the interface traps as a function of their energy level is evaluated as shown in Fig. 5.3 at T ranges from 20°C to 100°C . It can be seen that as temperature increases, the feature frequency increases exponentially. As a result, the measurable energy range for our measurement frequency window tends to move toward to the valence band. Particularly, for measurement frequency window from 100 Hz to 1 MHz, the measurable energy ranges from 0.26 eV to 0.5 eV at 20°C and from 0.12 eV to 0.42 eV at 100°C . Therefore, the interface traps located between 0.42 eV to 0.5 eV cannot be characterized at 100°C because their time constants are too short compared to the corresponding period of the 1 MHz signal. Here, we mainly discussed the change of the measurable energy range as a function of temperature at the upper half of the band gap, where the oxide border traps may also have pronounced influence due to the relatively low tunneling barrier.

On the other hand, the time constants of the oxide border traps are widespread due to the distributed nature of the oxide traps, and the feature frequency of the oxide border traps can be given by:

$$f = \frac{1}{2\pi\tau_{bt}} = \frac{N_C v_{th} \sigma}{2\pi \exp(\Delta E/kT) \exp(2\kappa x)} \quad \text{Eq. (5.3.2)}$$

Here, x is the depth of the border traps from the interface into the oxide, and κ is the tunneling decay factor. κ is given by:

$$\kappa = \frac{\sqrt{2m^*(E_c^{ox} - E)}}{\hbar} \quad \text{Eq. (5.3.3)}$$

Here, m^* is the electron effective mass in the dielectrics, E_c^{ox} is the conduction band edge of the dielectrics, E is the energy level of the traps, and \hbar is the reduced plank constant.

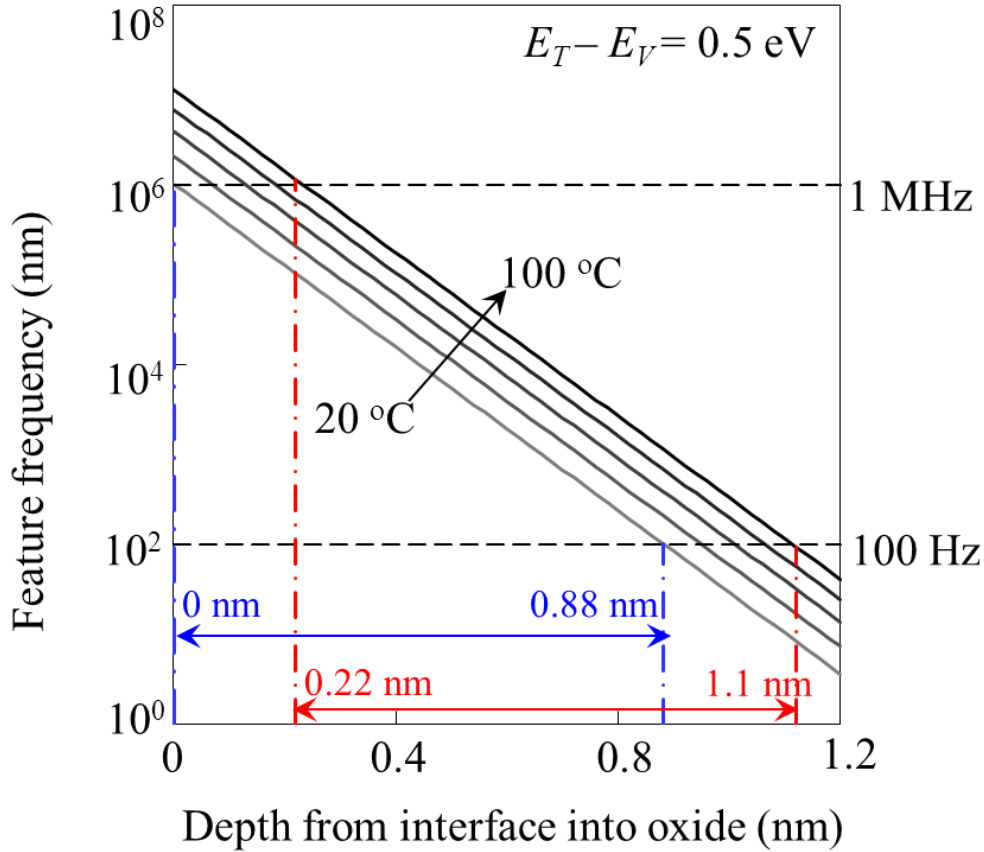


Fig. 5.4 Feature frequency as a function of the depth from interface into oxide of oxide border traps located at energy level of $E_T - E_V = 0.5$ eV. The normal used measurement frequency window range from 100 Hz to 1 MHz is labeled by the dash line.

Figure 5.4 shows the feature frequency of the oxide traps at 0.5 eV as a function of their depth from the interface into the oxide estimated by Eq. 5.3.2 & 5.3.3. In this estimation, same N_C , v_{th} , and σ previously used to estimate the τ_{it} are used here. The tunneling decay factor κ is estimated to be around 5.4 nm^{-1} by using $E_c^{ox} - E = 2.24 \text{ eV}$ and $m^* = 0.5m_0$, where m_0 is the free electron mass. It can be seen that as temperature increases, although the time constant of the interface traps can succeed the maximum frequency in the normally

used measurement window, i.e. 1 MHz, the oxide border traps at the same energy level still can response. Due to the border traps are distributed through the whole thickness of the oxide, the border traps with increasing depths can response at increased temperature. For example, in our estimation as shown in Fig. 5.4, the range of the depth of the border traps that can response for the 100 Hz to 1 MHz signals slightly change from 0 ~ 0.8 nm to 0.22 ~ 1.1 nm as temperature increases from 20 °C to 100°C. In other words, as temperature increases, while the influence of interface traps in normally used frequency window can be ruled out, oxide border traps can be mainly responsible for the observed frequency dispersion of the admittance characteristics. In consequence, the influence of the interface traps and the oxide border traps can be divided by carrying out high temperature AC admittance measurement.

5.4 Modified conductance method with consideration of oxide traps

5.4.1 High temperature capacitance and conductance behaviors

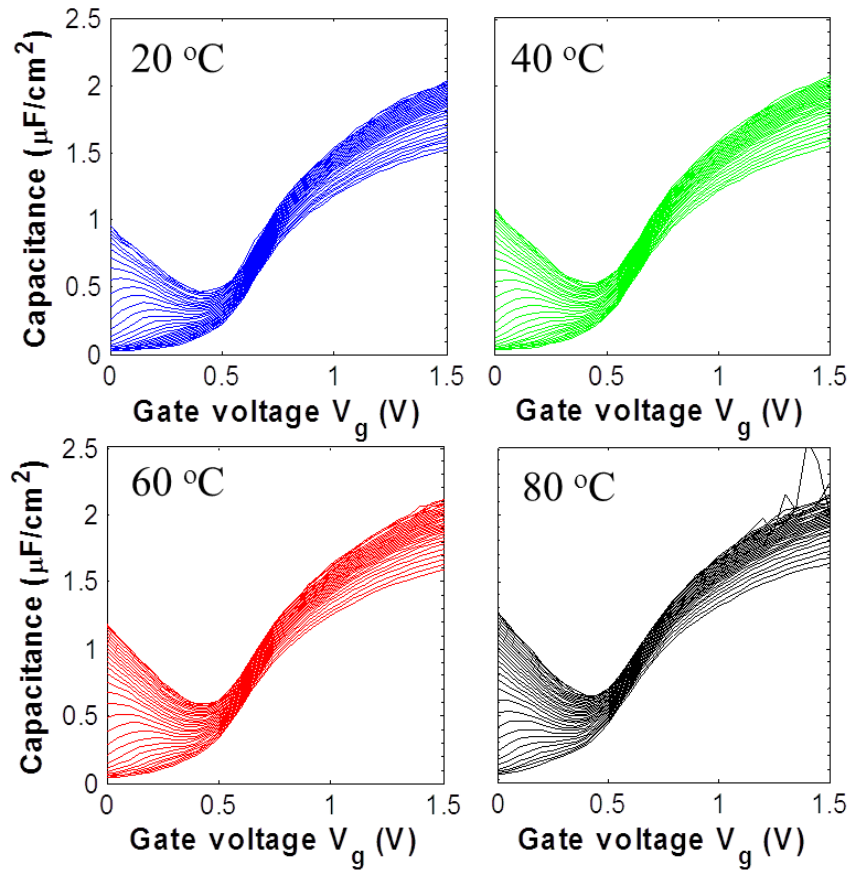


Fig. 5.5 Typical multi-frequency C - V characteristics of Pt/HfO₂/Al₂O₃/In_{0.53}Ga_{0.47}As from 100 Hz to 1 MHz at 20, 40, 60, and 80 °C.

Figure 5.5 shows the multi-frequency C - V characteristics of Pt/HfO₂/Al₂O₃/In_{0.53}Ga_{0.47}As from 100 Hz to 1 MHz at 20, 40, 60, and 80 °C. It can be seen that there is no strong distortion of the C - V curves or flat-band voltage shift as temperature increases from 20 °C to 80 °C.

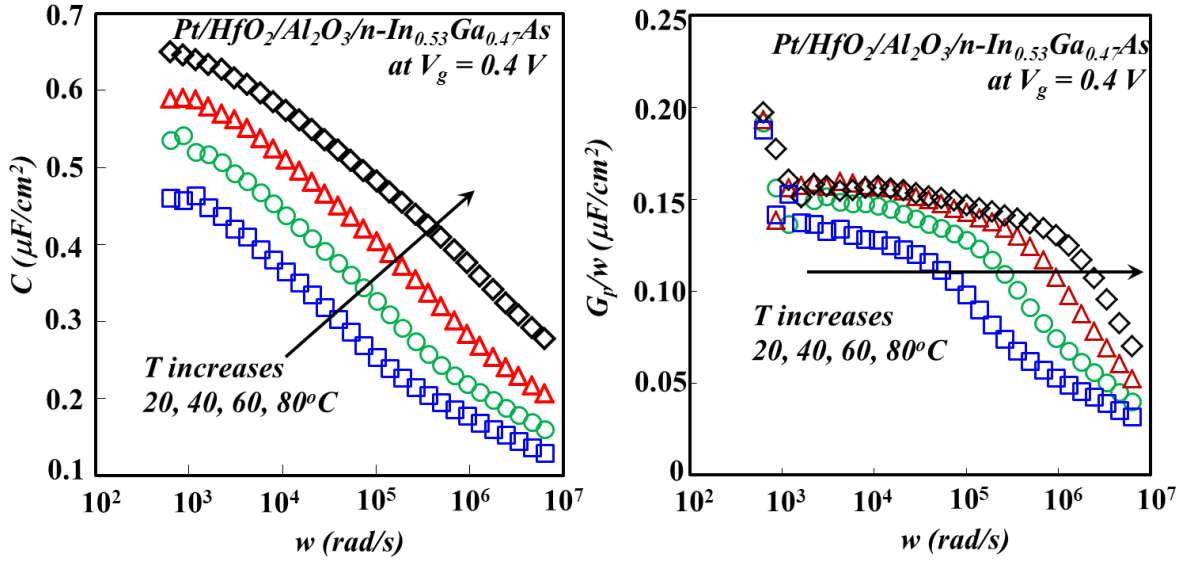


Fig. 5.6 (a) The Capacitance versus frequency and (b) the parallel conductance versus frequency plot of the under test sample at $V_g = 0.4$ V with measuring temperature of 20, 40, 60, 80 °C.

Figure 5.6 shows the frequency dispersion of the measured capacitance and parallel conductance of the under test sample at $V_g = 0.4$ V with measuring temperature of 20, 40, 60, 80 °C. From the C - V curves shown in Fig. 5.5, it is known that the device is in depletion region when biased in $V_g = 0.4$ V. As shown by the capacitance versus frequency plot in Fig. 5.6 (a), the frequency dispersion persists from 100 Hz to 1MHz at all measured temperatures. Besides, the measured capacitance increases with increasing temperature due to the decrease of τ_{it} . Figure 5.7 (b) shows the G_p/w versus w plot of the under test sample at $V_g = 0.4$ V. The conductance curves horizontally shift to the high frequency direction with increasing temperature, which indicates that the τ_{it} decreases as temperature increases. More importantly, there is a plateau of the conductance curve in the low frequency range. It is confirmed the responses of the distributed oxide traps, which corresponds to less frequency dependent energy loss in the low frequency region [5.3].

5.4.2 Extraction of D_{it} and N_{bt} from G_p/w versus w plot

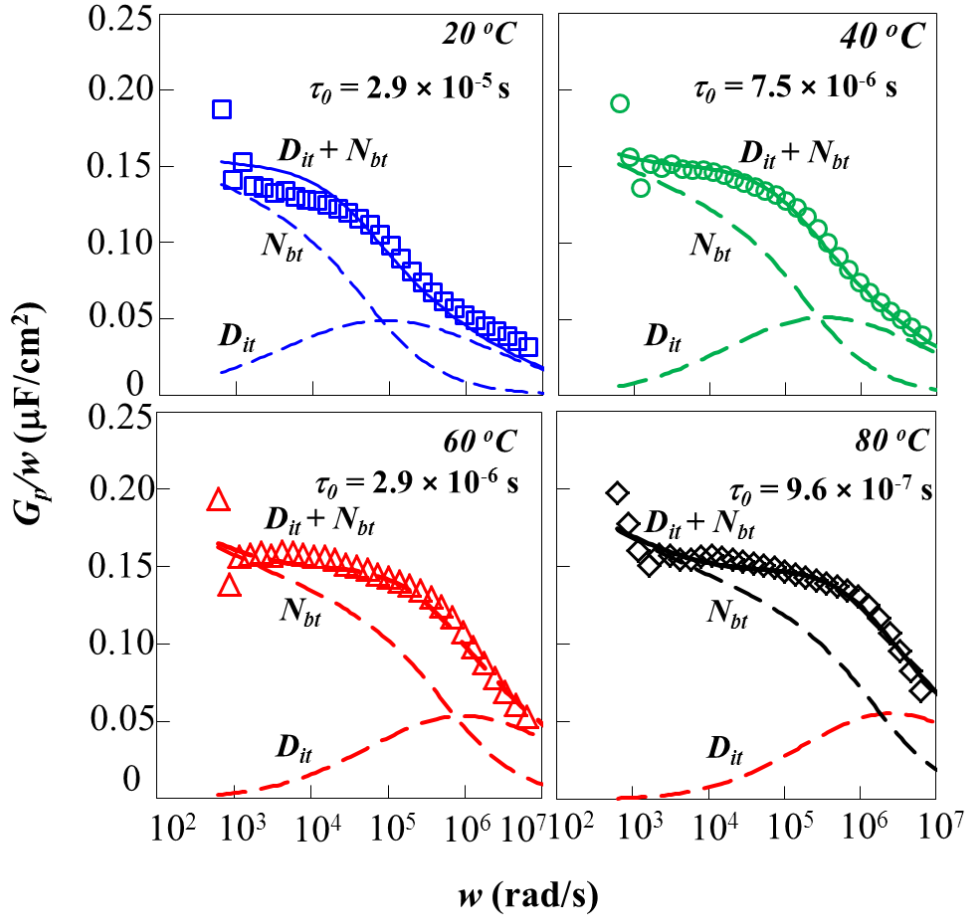


Fig. 5.7 Comparison between the experimental conductance curves (symbols) and the fitted curves (solid lines) with considering both of the responses of the interface traps and oxide border traps at 20, 40, 60, and 80 °C, respectively. The contribution of interface traps and oxide border traps on the fitted conductance curves is also plotted by dash lines.

Figure 5.7 shows the comparison between the experimental conductance curves and the fitted curves with considering both of the responses of interface traps and oxide border traps at 20, 40, 60, 80 °C, respectively. It can be seen that the experimental conductance characteristics can be well fitted. Here, the parallel conductance caused by D_{it} is calculated by using the standard conductance method with considerations of surface potential

fluctuation [5.1]. The parallel conductance caused by N_{bt} is calculated by using the distributed border traps model as described in the previous chapter. In particular, same parameters for interface traps and oxide border traps are used for fitting with the conductance curves at different temperatures except the time constant. The extracted D_{it} is $1.58 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$ with the surface potential fluctuation parameter σ_s of 60 meV. The tunneling decay factor is estimated to be about 5.4 nm^{-1} for the traps locate about 0.2 eV below the conduction band by using Eq. (5.3.3). (The estimation of the energy level of the traps is discussed in the following section.) Thus, for our measurement frequency and temperature window, the near interfacial oxide traps locate between $x = 0$ to $x = 1 \text{ nm}$ dominate the low frequency responses as shown in the conductance curves. It is also found that non-uniform spatial distribution profile with increasing N_{bt} from the interface into the oxide had to be used to fit the conductance curves. The spatial distribution profile of the N_{bt} is shown in Fig. 5.8, and the N_{bt} ranges from 3.0×10^{19} to $6.21 \times 10^{19} \text{ cm}^{-3}$ from interface into the oxide. Note that the increasing trend of N_{bt} from interface into the oxide extracted here is consistent with the spatial distribution profile extracted in the previous chapter for the oxide border traps above the conduction band. The τ_{it} for 20, 40, 60, 80 °C are $2.9 \times 10^{-5} \text{ s}$, $7.5 \times 10^{-6} \text{ s}$, $2.9 \times 10^{-6} \text{ s}$, and $9.6 \times 10^{-7} \text{ s}$.

According to previous discussion, it can be seen that for the MOS sample that is lack of thermal-dynamically stable interfacial layer with good quality, it is of particular importance to pay attention on influence of the oxide border traps on the conductance method, especially for the MOS samples show strong low frequency responses in the conductance characteristics. From Fig. 5.7, it can be seen that without considering the influence of the oxide traps, (1) it is very difficult to fit the conductance curve, and (2) the D_{it} may be severely overestimated and the origin of defects in the gate stack may be misunderstood.

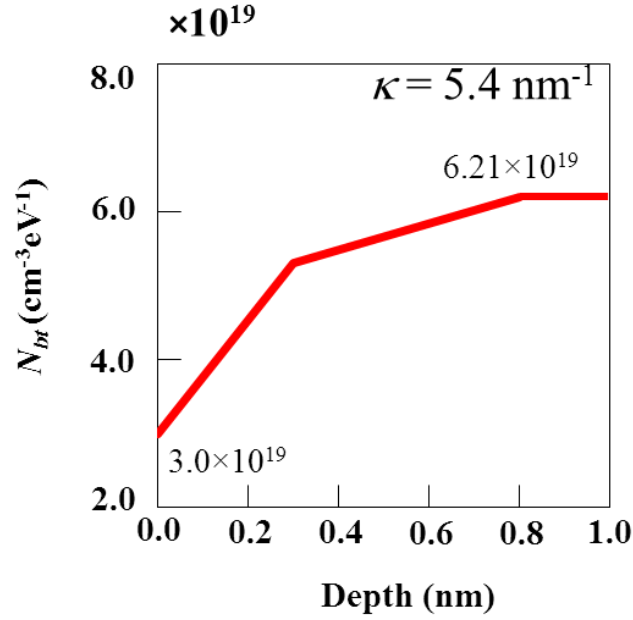


Fig. 5.8 The spatial distribution profile of N_{bt} used for fitting the conductance curves shown in Fig. 5.7.

5.4.3 Determination of the energy level

Due to the peculiarities of the III-V compounds, there are still many difficulties remain on accurate extraction of the V_g -energy relationship [5.10], and a straightforward method is still highly desired.

In the previous chapter, we propose extract the V_g -energy relationship when the fermi-level has been well biased into the conduction band by carrying out Terman technique on high-frequency/low-temperature C - V curves. Here, we propose extract V_g -energy relationship when the fermi-level is still biased inside the conduction band by evaluation of the change of the time constant of the interface traps as a function of temperature.

The essential difference between the temperature dependence of $\tau_{it} = (n_s v_{th} \sigma)^{-1}$ when the fermi-level is biased inside the band-gap and inside the conduction band is the temperature dependent of n_s . When fermi-level has been well biased inside the conduction band, the occupation rate of the conduction band states is not strongly temperature dependent. However, on the other hand, when the Fermi-level is biased inside the band-gap, the n_s is

strongly temperature dependent and τ_{it} is given by [5.5, 5.11]:

$$\tau_{it} = \frac{\exp(\Delta E/kT)}{N_C v_{th} \sigma} \text{ Eq. (5.4.1)}$$

From Eq. (5.4.1), it can be derived that:

$$\ln(\tau_{it}) + C = \frac{\Delta E}{kT} \text{ Eq. (5.4.2)}$$

where C represents a constant. From Eq. (5.4.1), it can be seen that $\ln(\tau_{it})$ should be a linear function of $1/kT$ and the slope is ΔE . Figure 5.9 shows the $\ln(\tau_{it})$ versus $1/kT$ plot. The τ_{it} used here is extracted from the conductance curves as shown in Fig. 5.7. Good linear relationship can be observed between $\ln(\tau_{it})$ and $1/kT$ and the ΔE is estimated to be around 0.22 eV. It is also noteworthy that the change of τ_{it} due to the temperature dependence of the σ , as discussed in the previous chapter, can be ignorable compared to that caused by the temperature dependence of n_s when $\Delta E \gg \Delta E_b$.

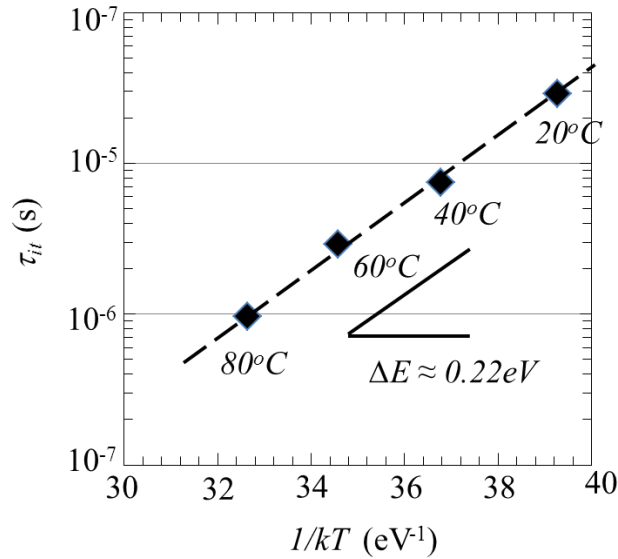


Fig. 5.9 The $\log(t_{it})$ versus $(1/kT)$ plot for extraction of the fermi-level energy. The t_{it} used here is extracted from the conductance curves as shown in Fig. 5.7.

5.5 Conclusion

In conclusion, this chapter addresses with the influence of oxide border traps with energy level inside the band-gap on the admittance characteristics of the MOS capacitor biased in depletion region. In particular, for the MOS capacitors that are lack of thermal-dynamically stable interfacial layer with good quality, such as InGaAs based MOS systems, the parallel conductance curves probably show strong distortion and thus conventional conductance method that only takes account for the energy loss caused by interface traps may not be applicable and leads to the misunderstanding of the traps distribution. By analyzing the conductance curves measured at various temperatures with considerations on both of the interface traps and oxide traps, we have (1) confirm the oxide border traps response for the low-frequency signal by high temperatures measurement, (2) consistently fit the conductance curves at different temperatures and extract the D_{it} and N_{bt} values, and (3) propose a straight-forward way to decide the energy level of the traps near mid-gap.

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Chapter 6: Study of interface traps and near interfacial bulk traps in AlGa_N/Ga_N heterojunction by conductance method

Conductance method is adopted to comparatively study the interface traps at the hetero-interface of AlGa_N/Ga_N based HEMT devices with different gate electrodes, including TiN and Ni. It is confirmed that there are no distributed bulk traps in the near interfacial region of the AlGa_N layer. Besides, it is found that the deep trap levels that are active in depletion region are likely to be caused by the crystallographic defects due to the stored strain near the heterointerface induced by the lattice mismatch between AlGa_N and Ga_N. The location of these trap sites may be influenced by the gate electrode due to the strain modulation in the AlGa_N layer. On the other side, the relatively shallow trap levels that are active in the inversion region is found to be independent on the gate electrodes, which is inferred to be caused by the nitrogen deficiency in the AlGa_N layer.

6.1 Introduction

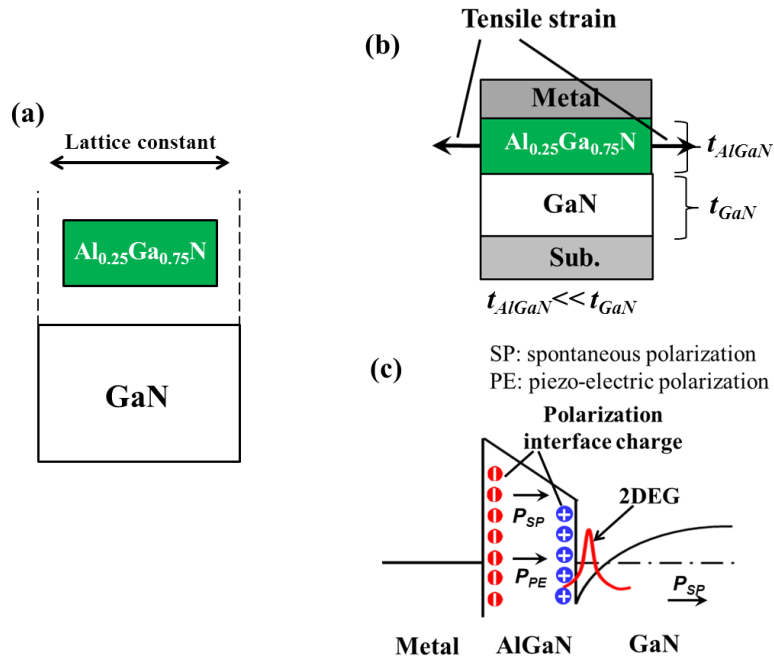


Fig. 6.1 Schematic illustration of (a) the lattice mismatch between AlGaN and GaN crystal structures, (b) the tensile strain endured by the thin AlGaN layer in the AlGaN/GaN heterojunction, and (c) the band diagram of the AlGaN/GaN heterojunction and the formation of polarization charges and two-dimensional electron gas (2DEG).

III-nitride compounds, such as GaN and AlGaN, shows unique combination of large band-gap, high break-down field, high mobility and saturation velocity, and good thermal conductivity. Due to these properties, AlGaN/GaN hetero-junction based high electron mobility transistors (HEMTs) are extremely attractive for high power and high frequency application and being extensively studied [6.1-6.4]. However, two crucial challenges still remain [6.4]. First, the gate leakage in AlGaN/GaN heterojunction is too high. Second, the AlGaN/GaN heterojunction exhibit current collapse with high drain voltage. Both of these problems can be attributed to the electrically active traps in the AlGaN/GaN heterojunction [6.3, 6.5]. Therefore, it is of significant importance to characterize the traps distribution in

GaN heterojunction.

In particular, considering the lattice mismatch between AlGaN and GaN (**Fig. 6.1 (a)**) and the relatively thin AlGaN barrier layer used in this type of devices, tensile strain is concentrated on the thin AlGaN layer in the heterojunction (**Fig. 6.1 (b)**). Although the tensile strain induced piezoelectric polarization substantially contributes to the formation of 2DEG (**Fig. 6.1 (c)**), it may also results in considerable amounts of interface traps in the hetero-interface and crystallographic defects in the bulk of AlGaN layer. Recently, many trap characterization techniques have already been adopted to profile the trap distribution in the AlGaN/GaN hetero-junction [6.6-6.9]. It is noteworthy that electron tunneling spectroscopy studies [6.8, 6.9] evidence that most of electrically active traps distributed at the hetero-interface and the near interface region instead of the region near the metal/AlGaN interface. In this study, we deploy standard conductance method, which is a very common and convenient trap characterization technique, to study the interface and the near interface traps at the hetero-interface of AlGaN and GaN. The heterojunctions with different metal electrodes, Ti and Ni, are also comparatively studied to clarify the properties of active traps and the influence of the electrodes.

6.2 Device structure

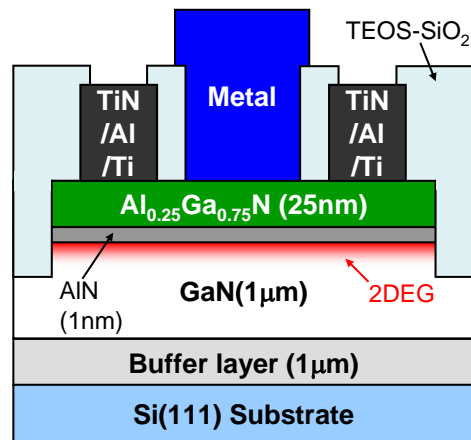


Fig. 6.2. Schematic structure of fabricated AlGaIn/GaN HEMTs [6.10, 6.11].

Figure 6.2 schematically shows the structure of the fabricated AlGaIn/GaN HEMTs. The devices were fabricated Al_{0.25}Ga_{0.75}N/GaN epitaxial wafer on Si (111) substrate with an AlN intermediate layer. The thickness of AlGaIn and AlN layer is 25 nm and 1 nm, respectively. Two types of devices, which prepared by same processes except that different metal gates are deposited, were studied here to investigate the potential influence of metal gates on the distribution of the interface traps. Details of the fabrication processes can be found in ref. [6.10, 6.11]. The admittance characteristics of the gate/AlGaIn/GaN heterojunction are measured between gate and source.

6.3 Results and Discussion

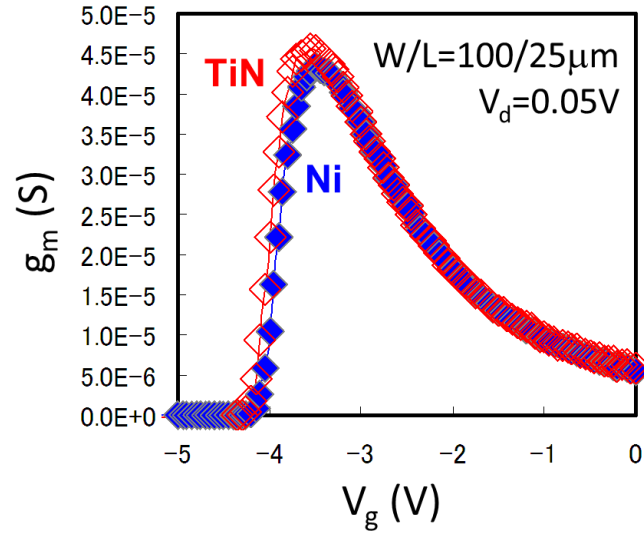


Fig. 6.3. Comparison on transconductance characteristics between AlGaIn/GaN based HEMTs with TiN and Ni gate electrodes.

Figure 6.3 shows the transconductance (g_m) characteristics of the AlGaIn/GaN based HEMTs with TiN and Ni gate electrodes. Generally, g_m is proportional to μC_g , where μ is the carrier mobility in the channel and C_g is the gate capacitance. The flat-band condition roughly locates at the gate bias that gives the maximum transconductance. When the heterojunction is biased below the flat-band condition, C_g is approximately given by $(1/C_b + 1/C_s)^{-1}$, where C_b is the capacitance of the barrier layer (the AlGaIn layer) and C_s is the capacitance of the substrate layer (the GaN layer). Therefore, the more the gate is biased below the flatband condition, the smaller the g_m is, because C_s decreases with increasing depletion width. On the other hand, when the heterojunction is biased above the flatband condition, C_g is roughly equal to the C_b , which is a constant. Here, the decreased g_m with increasing V_g can be mainly attributed to decreased μ due to increased roughness scattering with increasing transverse electric field in the channel. As a result, several points can be pointed out from fig. 6.3. Firstly, because the peaks of the g_m - V_g curves of these devices almost appear at same position, the gate electrodes, Ni and TiN, do not influence the flat-

band voltage of the devices. This is mainly due to the fermi-level pinning at the metal-gate/AlGa_N interfaces. Secondly, the low-field g_m of the TiN device is slightly higher than that of the Ni device. It indicates that the 2DEG in the TiN device may less suffer from coulomb scattering. Lastly, both of these devices show almost same high-field g_m , which suggests similar surface roughness scattering in these devices. In short, the comparison on the transconductance characteristics between the devices with TiN and Ni electrodes indicates that the metal electrode does not likely to influence the roughness but may have influence the distribution of interfaces traps of the AlGa_N/Ga_N hetero-interface. Therefore, we investigated the conductance spectra of the devices in details as follows.

6.3.1. Conductance analysis in depletion and inversion region

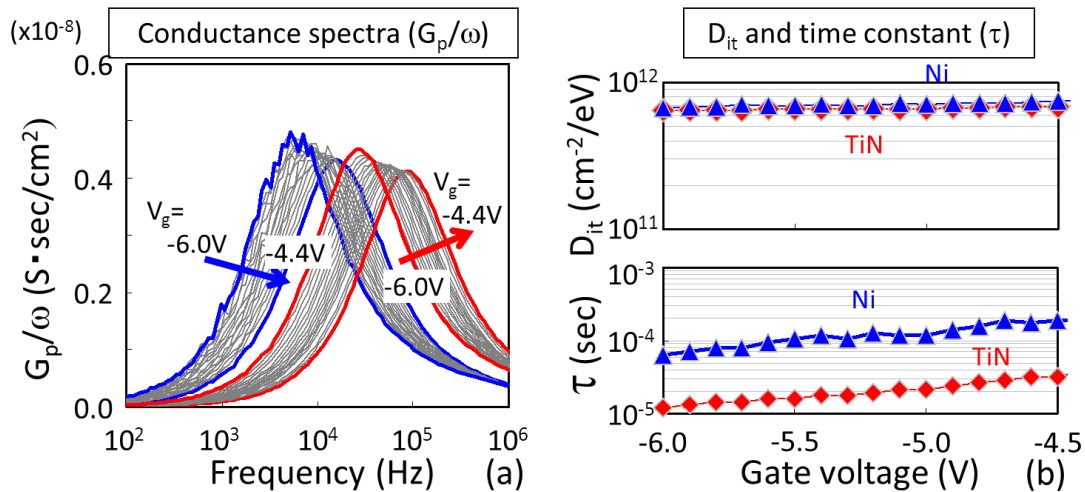


Fig. 6.4. Comparison on the (a) conductance spectra of the AlGa_N/Ga_N HEMTs with the Ni (blue) and TiN (red) electrodes biased in depletion region, and (b) extracted D_{it} and (c) time constant τ by using standard conduction method

Figure 6.4 shows (a) the conductance spectra of the AlGa_N/Ga_N HEMTs with the Ni (blue) and TiN (red) electrodes biased in depletion region and (b) extracted D_{it} and τ by using standard conduction method [6.12]. First of all, it can be seen that both devices shows typical peak behavior (**Fig. 6.4 (a)**), which represents the existence of interface traps.

Particularly, compared to the conductance curve of the MOS capacitor with large amounts of distributed border traps, as shown in **Fig. 5.6**, there is no obvious low frequency response and thus distributed border traps are not likely to exist in the AlGa_N layer. Secondly, as shown by **Fig. 6.4 (b)**, while the D_{it} in the Ni device is slightly higher than that in the TiN device, the τ of the traps in the Ni device is almost longer than that in the TiN device by an order of magnitude. The difference on the τ cannot be attributed to the different energy levels of the traps in different devices because the two devices have almost the same flat-band voltage as discussed before. Therefore, it may indicate that the interfacial traps are located at a deeper distance from the hetero-interface into the AlGa_N layer in the Ni device than the traps in the TiN devices.

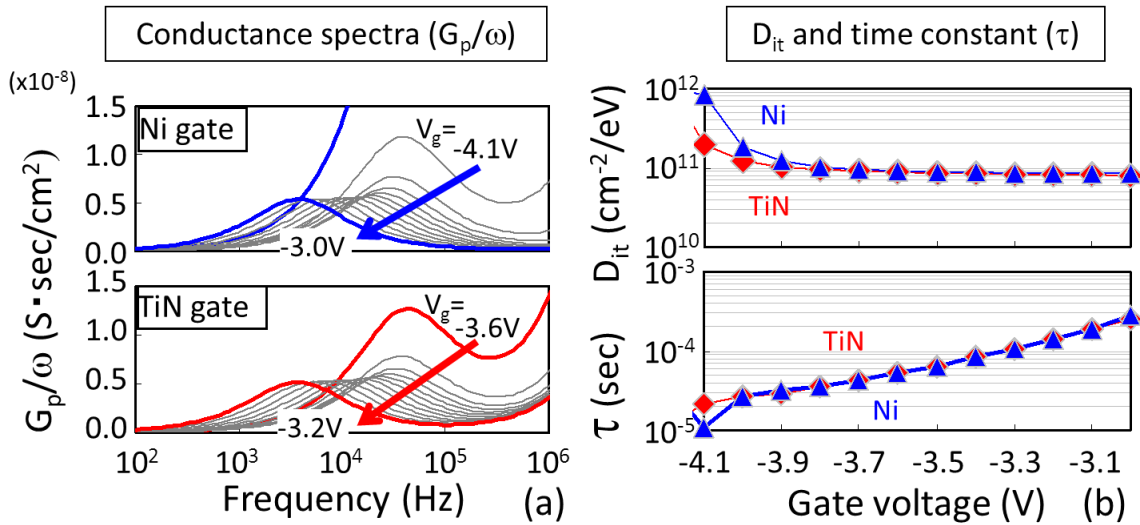


Fig. 6.5. Comparison on the (a) conductance spectroscopy, (b) extracted D_{it} and (c) time constant τ using standard conductance method of the AlGa_N/Ga_N heterostructures with the Ni (blue) and TiN (red) electrodes biased at inversion region.

Figure 6.5 shows (a) the conductance spectra of the AlGa_N/Ga_N HEMTs with the Ni (blue) and TiN (red) electrodes biased in depletion region and (b) extracted D_{it} and τ by using standard conductance method. As shown by **Fig. 6.5 (a)**, there is also no low frequency response in the conductance curves in the inversion region. Besides, **Fig. 6.5 (b)** further

shows that the D_{it} and τ are almost same in these two devices, indicating that same trap levels are responsible for the AC conductance responses in inversion region.

6.3.2. Model of traps distribution in AlGaN/GaN heterojunction

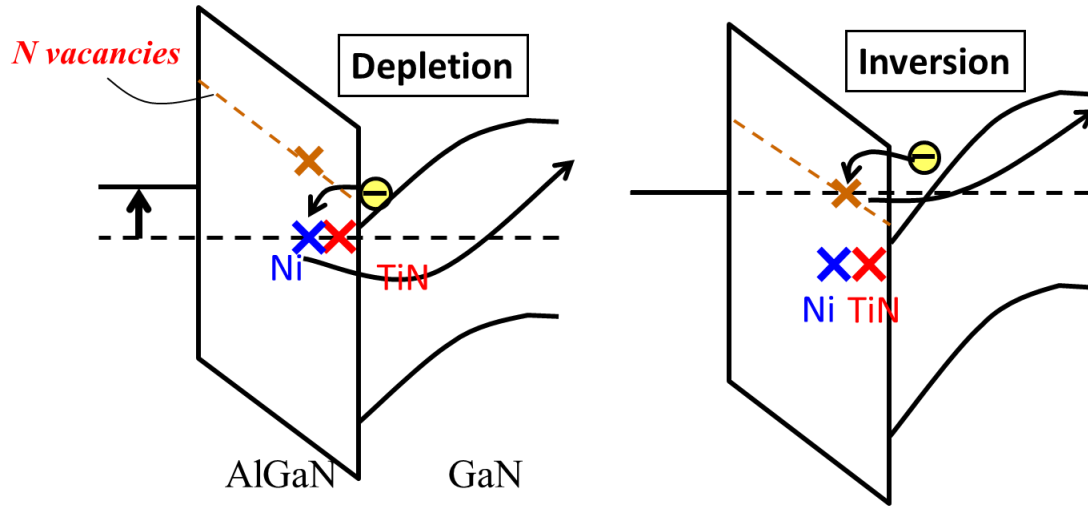


Fig. 6.6 Schematic band diagram of the AlGaN/GaN heterojunction in depletion and inversion with illustration of the distribution of the electrically active traps in the devices with TiN and Ni electrodes.

Based on previous observation, we proposed a model, as shown in Fig. 6.6 of the traps distribution in the AlGaN layer to explain the AC conductance behaviors of the devices with TiN and Ni electrodes. In depletion region, there are active trap sites whose spatial locations depend on metal electrodes. Especially, the Ni electrode may lead to the formation of active traps in a deeper distance from the hetero-interface into the AlGaN layer. On the other hand, in inversion region, the active trap sites are almost independent on the metal electrodes.

In particular, we infer that the deep trap levels that responsible for the conductance response in the depletion region may be related to the crystallographic defects caused by

the lattice mismatch in the heterojunction. As previously discussed, because of the lattice mismatch between the AlGa_N and Ga_N, the thin AlGa_N barrier layer is under tensile strain and thus crystallographic defects can be generated in the AlGa_N layer and result in deep trap levels. The metal gate may influence the distribution of these traps by modulating the strain in the AlGa_N layer. On the other hand, the relatively shallow trap levels that are responsible for the conductance response may result from the nitrogen deficiency in the AlGa_N layer. This has been reported that the nitrogen deficiency induced traps level locates near 0.5 eV below the conduction band of AlGa_N, which is just the fermi-level position when the device is biased into inversion region. Therefore, these relatively shallow trap levels are less influenced by the strain stored in the AlGa_N layer.

6.4. Conclusion

In conclusion, conductance method is adopted to comparatively study the interface traps at the hetero-interface of AlGa_N/Ga_N based HEMT devices with different gate electrodes, including TiN and Ni. It is confirmed that there are no distributed bulk traps in the near interfacial region of the AlGa_N layer. Besides, it is found that the deep trap levels that are active in depletion region are likely to be caused by the crystallographic defects due to the stored strain near the heterointerface induced by the lattice mismatch between AlGa_N and Ga_N. The location of these trap sites may be influenced by the gate electrode due to the strain modulation in the AlGa_N layer. On the other side, the relatively shallow trap levels that are active in the inversion region is found to be independent on the gate electrodes, which is inferred to be caused by the nitrogen deficiency in the AlGa_N layer.

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Chapter 7: Conclusion

7.1: Summary of this thesis

objects	New structures	New materials	
	Si fin structure	high- κ /III-V	AlGaIn/GaN
contribution			
method	Charge-pumping measurement of fins with different widths → Spatial distribution of D_{it} on the 3D surface	1. $C-V$ measurements from low-to-high temperatures → Spatial and energy distribution of N_{bt} 2. Conductance method considering contribution of oxide border traps → Separate evaluation of D_{it} and N_{bt}	Comparative studies on the conductance spectra of devices with different metal gates → D_{it} at the heterointerfaces and their species
discoveries	1. Optimal F.G.A temperature is around 420°C. 2. A high concentration of $D_{it} \sim 3 \times 10^{11} \text{cm}^{-2} \text{eV}^{-1}$ exists at corners	1. $N_{bt} \sim 10^{20} \text{cm}^{-3} \text{eV}^{-1}$ has been demonstrated, and N_{bt} tends to increase with increasing energy or depth 2. Trapping process of oxide border traps is thermally activated 3. In parallel conductance curves, interface traps contribute to “peak-like” behaviors and border traps contribute to “plateau-like” behaviors. 4. Proper interpretation of distorted conductance curves with strong low-frequency response require both consideration of D_{it} and N_{bt} .	1. No distributed border traps near the heterointerfaces 2. Deep traps levels may be related to crystallographic defects. 3. Shallow traps levels may be related to nitrogen deficiency

Table 7.1 Summary of the major contributions of this thesis

In summary, we have systemically studied the traps at or near the dielectrics/semiconductor interfaces and semiconductor heterointerfaces. The major contributions of this thesis, on both of trap characterization methodologies and the properties of the traps, are summarized in **Table 7.1**, as described as follows.

(A) About the SiO₂/Si interfaces with fin structure:

By carrying out CP measurement on gated diodes based on Si fins with different widths, a new methodology is proposed to extract the spatial distribution of D_{it} on the 3D surface. It is found that (1) for <110>-directed fins fabricated on (100)-orientated SOI wafers, the optimal forming gas annealing temperature is around 420 °C for passivation of the dangling bands on Si fin surfaces, (2) a high concentration of D_{it} ($\sim 3.0 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$) tends to locate at the corners, which is almost an order of magnitude higher than that at the (100)-oriented top wall ($\sim 3.0 \times 10^{10} \text{ cm}^{-2} \text{ eV}^{-1}$). This is attributed to the continually varying surface orientation at the corner region.

(B) About the high- κ /III-V interfaces:

We have established a methodology to extract the spatial and energy distribution of oxide border traps from the frequency- and temperature-dependent C - V and G - V characteristics. Besides, we also modified the standard conductance method by incorporating the influence of oxide border traps for analyzing the distorted parallel conductance curves with strong low-frequency response to properly characterize both of interface traps and oxide border traps. The major discoveries are listed as follows.

(1). A high concentration of oxide border traps, which increases with increasing energy level and depth into the oxide, between 10^{19} cm^{-3} to 10^{20} cm^{-3} has been found in the sample with TiN/HfO₂/GdAl₂O₃/n-In_{0.53}Ga_{0.47}As structure. These traps are likely to be caused by accumulated defects in the high- κ oxide layer during material growth depending on deposition techniques.

(2). Empirical model to evaluate frequency- and temperature-dependent responses of oxide border traps is proposed. Particularly, we have demonstrated that the trapping process of oxide border traps is thermally activated. As temperature decreases from 300 K to 77 K, the time constant of the border traps is estimated to be enlarged by a factor of 10^3 mainly due to the shrinking of the capture cross-section.

(3). We have confirmed the contribution of the responses of interface traps and oxide border traps on the parallel conductance characteristics. While the “peak-like” conductance curves indicates the response of interface traps, the “plateau-like” conductance curves in the low-frequency region suggests the response of distributed oxide border traps.

(4). The D_{it} and N_{bt} are separately extracted from the parallel conductance characteristics considering their different responding behaviors. It is found that for the conductance curves with strong low-frequency responses, applying standard conductance method without considering the existence of oxide border traps may result in considerable overestimation of D_{it} .

(C) About the AlGaN/GaN heterointerfaces:

Conductance method is adopted to comparatively study the interface traps at the heterointerface of AlGaN/GaN based HEMT devices with different gate electrodes, including TiN and Ni. It is confirmed that there are no distributed bulk traps in the near interfacial region of the AlGaN layer. Besides, it is found that the deep trap levels that are active in depletion region are likely to be caused by the crystallographic defects due to the stored strain near the heterointerface induced by the lattice mismatch between AlGaN and GaN. The location of these trap sites may be influenced by the gate electrode due to the strain modulation in the AlGaN layer. On the other side, the relatively shallow trap levels that are active in the inversion region is found to be independent on the gate electrodes, which is inferred to be caused by the nitrogen deficiency in the AlGaN layer.

7.2. Future work

In multi-gate FETs, considering that the dimensions of the cross-section shape of the 3D channel will continually decrease to enhance the electrostatic control of the channel, the corner regions will play a more and more important role on the performance of the devices. Therefore, it is important to further optimize the corner shape for lowering D_{it} . The corner shape can be adjusted by sacrificial oxidation and hydrogen annealing, and the local D_{it} at the corner can be evaluated by using the technique proposed in this study.

In high- k /III-V MOS systems, although the passivation of interface states is still the major concern, the oxide traps reside in the high- k dielectrics are worthy for more attention especially considering the lack of high-quality interfacial layer with large band-offset in high- κ /InGaAs MOS system. Additionally, several high- k materials, such as Al_2O_3 , HfO_2 , La_2O_3 , ZrO_2 , GdO_2 , have been demonstrated to be compatible with InGaAs substrates for achieving relatively low density of interface states (D_{it}). Therefore, comparing the concentration of electrically active oxide traps may be essential for materials selection and optimizing deposition techniques.

In AlGaIn/GaN heterojunctions, it is important to further clarify the species of the traps at and near the heterointerfaces by both of electrical and physical characterization. Furthermore, the influences of mechanical strain is worthy for further investigation. It can be achieved by characterizing the distribution of interfacial traps in the heterojunctions under different bending conditions. This study may lead to new HEMT devices optimizing strategies based on modulating the strain in the heterojunctions.

Appendix A: Anomalies in I - V characteristics of multiple Si nanowire FET under pulse measurement

A1 Introduction:

Tri-gate Si nanowire FET fabricated on Silicon-on-Insulator (SOI) substrate was an attractive component for future high speed logic circuits as its superior drivability, electrostatic control and fabrication feasibility [1]. However, the performance of multi-gate Si nanowire FET under pulse operation was still rarely reported. In this study, we report an anomalous IV characteristic of tri-gate multiple Si nanowires n-FET (tri-gate multiple n-SNWT) under pulse biases. The underlying mechanism was considered to be threshold voltage modulation because of accumulation of holes near the source sides because of strong impact ionization.

A2 Experiment:

Tri-gate multiple n-SNWT on SOI substrates were fabricated as described in Ref.[2]. Every device has 64 nanowires parallel connected from source to drain. Each nanowire has a rectangular-like cross section shape with size of $12 \times 18 \text{ nm}^2$ estimated by TEM images. The schematic image of the under test device is shown in Fig. A1.1. The waveforms of gate and drain pulses are shown in Fig. A1.2 (a), pulse V_g and V_d with rising time about 80ns [3] were applied to the devices. By fixing the averaging time and changing the delay time, the dynamic evolution of IV characteristics after applying pulse can be captured.

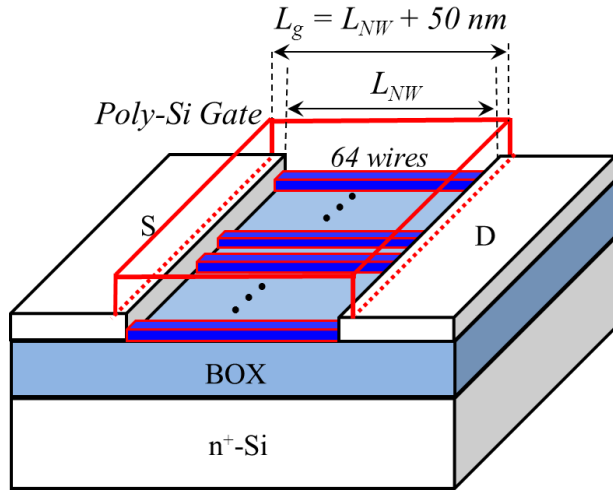


Fig.A1.1 Schematic structure of fabricated tri-gate multiple n-SNWTs. Gate overlapped structure with raised S/D was adopted to decrease series resistance. 64 wires were used as channels.

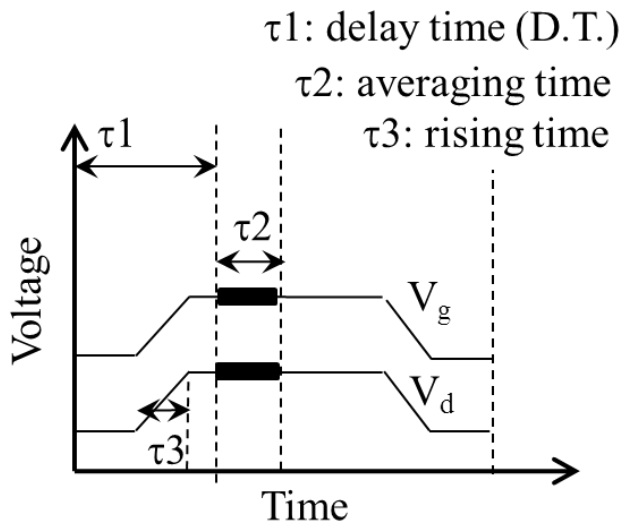


Fig. A1.2 Schematics of biasing and measuring event: I_d was measured after certain delay time (τ_1) by averaging the measured value during averaging time (τ_2). Both of gate voltage and drain voltage are pulses waveform with same rising time (τ_3).

A3 Results and discussion:

(a) Anomalies in pulsed I_d - V_d of short channel multiple channel SNWTs:

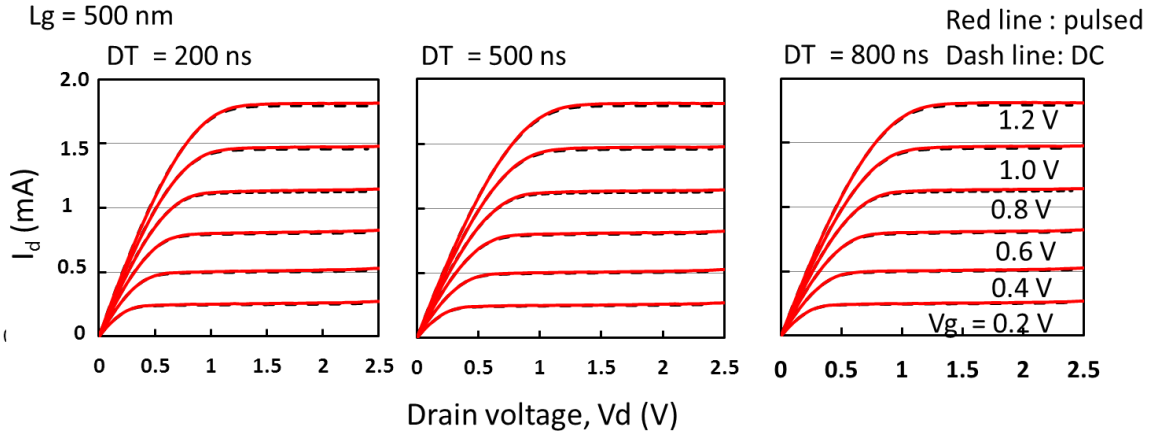


Fig. A1.3. The Pulsed I_d - V_d (red solid line) at different delay time (D.T.) and DC I_d - V_d (black dash line) of fabricated Tri-gate multi-nanowires Si NWFET with 64 nanowire channels and channel length of 500 nm. Gate overdrive ($V_g - V_{th}$) was ranging from 0.2 to 1.2 V with a step of 0.2 V.

Fig. A1.3 shows that pulsed and DC I_d - V_d of a n-SNWT device ($N = 64$) with gate length (L_g) of 500 nm almost overlapped with each other, demonstrating the correctness of measurement setting. Fig. A1.4 shows that in the device with shorter channel ($L_g = 200$ nm and $L_g = 160$ nm), although the pulsed I_d - V_d is very close to that of DC at beginning, it started to fluctuate as delay time (D.T.) increases, and finally evolves into an anomalous I_d - V_d with an negative differential conductivity (NDC) region. This phenomenon is considered to be caused by strong impact ionization in pinch-off region, as evidenced by following facts.

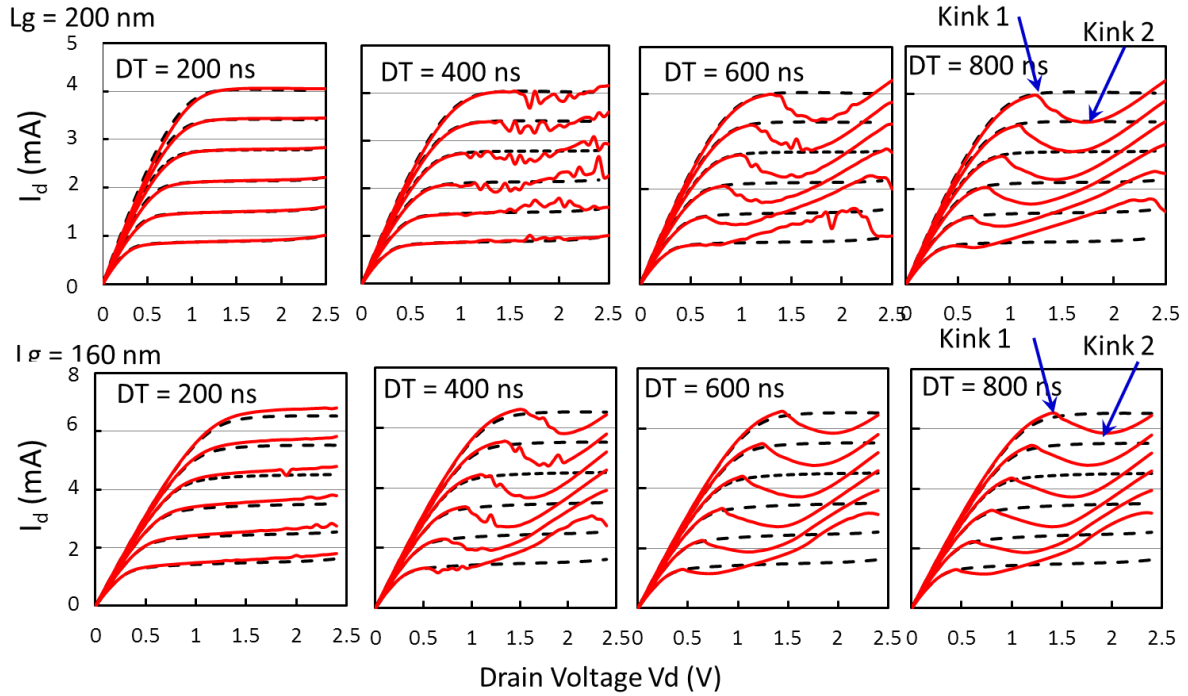
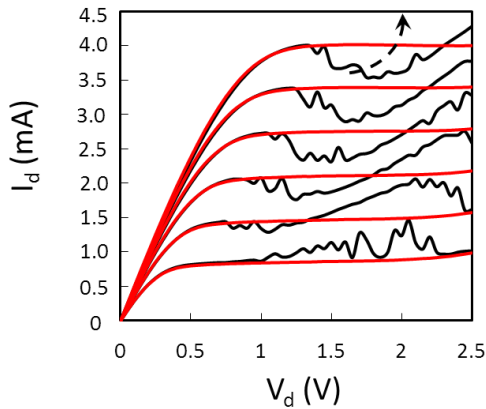


Fig. A1.4. The Pulsed I_d - V_d (red solid line) at different delay time (D.T.) and DC I_d - V_d (black dash line) of fabricated Tri-gate multi-nanowires Si NWFET with 64 nanowire channels and channel length of 200 nm and 160 nm. Gate overdrive ($V_g - V_{th}$) was ranging from 0.2 to 1.2 V with a step of 0.2 V.

(b) Dependence of the anomalies in pulsed I_d - V_d on the illumination condition

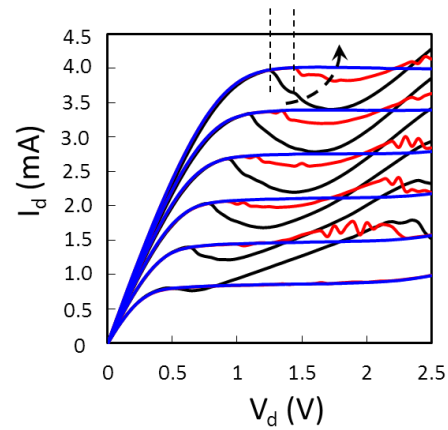
It was also well known that impact ionization induced floating body effects are sensitive to illumination [4], fig. A1.5 shows that as intensity of illumination increases, the anomalous curves vanished. It is worthy to note that the threshold voltage of the abnormality increased as light became stronger, which indicates that impact ionization was more difficult to be triggered because increased intrinsic carriers in the channel.

DT 500ns : weak holes accumulation



Black line: darkness
red line: light on (36%) (a)

DT 800ns : strong holes accumulation



Black line: darkness
red line: light on (36%)
blue line: light on (100%) (b)

Fig. A1.5. Pulsed I_d - V_d ((a) D.T. = 500 ns & (b) D.T. = 800 ns) characteristics of the multiple NWTs devices measured at different illumination condition, w/o light, 50W, and 150W, in the chamber of the probe station, which was equipped with 150W Halogen light source. As the power of light source increases, the abnormal I_d - V_d went back to the classical type.

(b) “History dependence” of the anomalies in pulsed I_d - V_d :

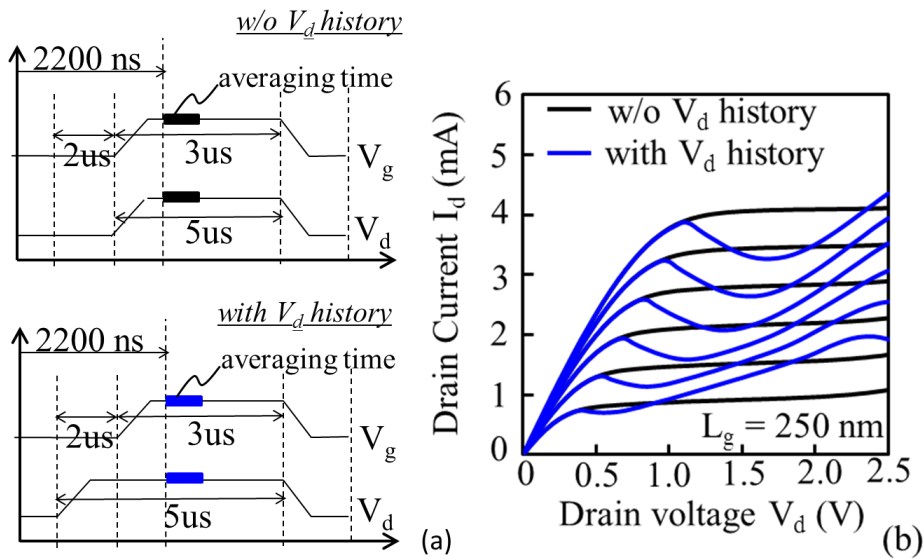


Fig. A1.6. (a) Schematics of biasing and measuring events. In case of with V_d biasing history, the V_d pulse raised 2ms earlier than V_g pulse, and (b) the dependency of pulsed I_d - V_d on the history of applying V_d . The gate overdrive was ranging from 0.2 to 1 V with a step of 0.2 V.

A4 Conclusion:

An anomalous I_d - V_d of tri-gate multiple n-SNWTs under pulse measurement are reported, which was attributed to the accumulation of holes in the body because of strong impact ionization triggered by pulse voltage. It likely to happen in multi-nanowire devices may because of lower series resistance of them and the NDC region was speculated to be a peculiar to multi-gate devices. Besides, p-SNWTs were supposed to less suffer from this phenomenon as its lower impact ionization rate with respect to that of n-type. These results reveals that suppressing impact ionization in pinch-off region of these devices is still crucial for high speed logic circuit application. It could be achieved by careful control of operation voltage or adopting novel structures, such as lightly doped drain structure. The underlying mechanisms still need further investigation.

Reference

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Appendix B: Modulation of the resistive switching behaviors of the CeO₂ based metal-insulator-metal (MIM) structure by interface engineering

B1 Introduction

Resistive switching random access memory (ReRAM) is an attractive component for future non-volatile memory technology owing to its simple structure, low operation voltage, compatibility with current CMOS processes and high scalability [B1]. Nanoionics-based resistive switching (RS) behavior, which is the basis of ReRAM, has been found in a wide variety of oxides [B2], such as NiO [B3], HfO₂ [B4], ZnO [B5], and CeO₂ [B8, B10]. The formation and rupture of conductive filaments (CFs) in the oxide film caused by electrical field induced ionic migration seems the most plausible mechanism in RS behaviors. However, several challenges are still faced by studies of ReRAM for practical application. One critical challenge is the elimination of the electrical forming process with high voltage, which is required by many fresh ReRAM devices to trigger the first time RS [B6]. Several solutions, such as doping metal ions [B7] and depositing nonstoichiometric oxides [B8], have been reported for eliminating forming process. The key of these methods is increasing the concentration of defects or vacancies in the bulk, which help CFs form more easily. On the other hand, another challenge might come from the suppression of tunneling current, especially in highly scaled devices. Recently, it has been reported that in a conductive bridge ReRAM device, although tunneling current between electrodes doesn't contribute to the RS process like ionic current, it plays the major portion of the operation current and directly leads to high power consumption [B9]. Therefore, in consideration of suppressing tunneling current through the materials, the concentration of defects and vacancies in the bulk of materials should be decreased as much as possible. As a result, elimination of

electrical forming by performing interface engineering, which doesn't fundamentally change the bulk properties or bring large amount of vacancies into the whole bulk, might be promising in future ReRAM technology from the viewpoint of suppression on tunneling current.

Cerium oxide has aroused strong attention for ReRAM application because of its features of solid electrolyte and high conductivity of oxygen ions [B10]. Besides, it has been reported that Ce-silicate with wide band gap and high dielectric constant could be formed at the interface between Si and Cerium oxide [B11], which enlightens the possibility for adjusting interface properties of CeO₂ by incorporating Si layer. In this study, ReRAM devices composed by 20-nm-thick CeO₂ resistive switching layer, 1-nm-thick Si buffer layer, W top electrode (TE) and TiN bottom electrode (BE) were fabricated. The improvement of memory performance by inserting Si buffer layer at the interface was confirmed. Effects of the Si buffer layer and its underlying mechanism were discussed based on CFs mechanism. Moreover, the gradual reset process under sweeping voltage of our devices, which is also important in other oxides based ReRAM devices [B5, B8], was investigated by employing parallel CFs model.

B2 Experiments

The W/CeO₂/Si/TiN devices were fabricated on highly doped n^+ -Si wafer ($<0.02 \Omega\text{cm}$). A 200-nm-thick SiO₂ layer was formed by thermal oxidation and patterned to open window to contact BE and the substrate. A 15-nm-thick TiN layer, and a 1-nm-thick Si buffer layer were successively deposited by RF sputtering. Then, a 20-nm-thick CeO₂ layer was deposited by electron beam evaporation in an ultrahigh vacuum chamber at a pressure of 10^{-7} Pa with a deposition rate of about 0.05 Å/s. The temperature of the substrate was set to be 300 °C during deposition. Subsequently, a 50-nm-thick W layer was in-situ deposited by RF sputtering without exposing the samples to the air in order to avoid any moisture absorption on the CeO₂. The W layer was then patterned to form square shaped top electrodes (TE) having sizes of $20 \times 20 \mu\text{m}^2$. Finally, Al was evaporated as a back contact

and rapid thermal annealing (RTA) was performed in N₂ ambient at 400 °C for 30 s. In addition, the device without Si buffer layer having W/CeO₂/TiN structure was also prepared as a reference. All electrical characteristics were measured by Agilent 4156C semiconductor parameter analyzer.

B3 Results and discussion

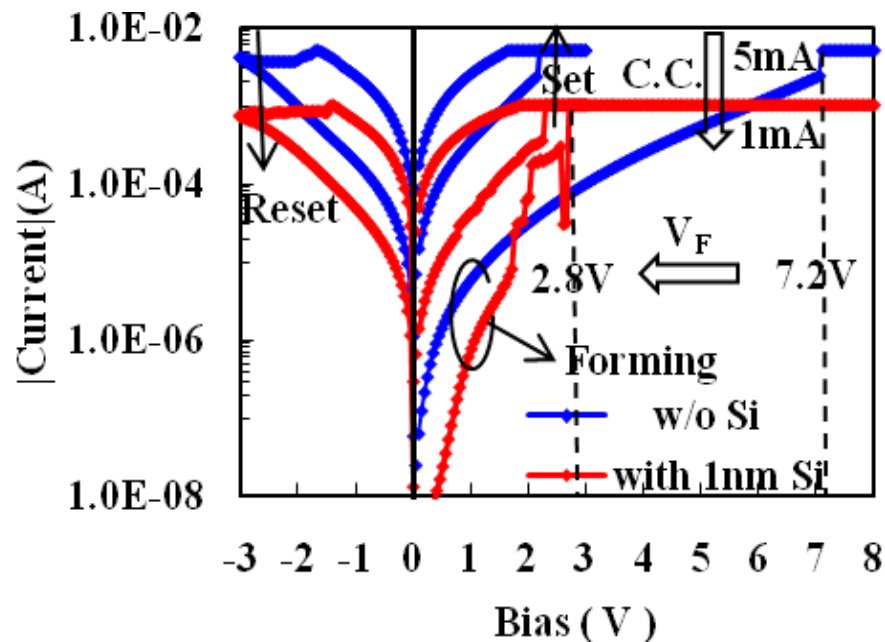


Fig. B1. Typical RS behaviors of the W/CeO₂ (20nm)/TiN device and the W/CeO₂ (20nm)/Si (1nm) /TiN. Both of the devices are operated at the same way, the voltage is in sequence swept from 0 → 10, 0→-3→0 and 0→3→0 V to realize forming, reset and set process, respectively. By inserting Si, the forming voltage (V_F) is decreased from 7.2 V to 2.8 V, and the C.C. is decreased from 5 mA to 1 mA.

The typical *I-V* characteristics of the W/CeO₂/Si/TiN and W/CeO₂/TiN devices are shown in **Fig. B1**. The TiN BE was grounded and sweeping voltage was applied to the W TE. In the initial stage both of devices with and without Si buffer layer required a positive forming process to reach low resistive states at the first time. Both of them exhibited similar

bipolar RS behaviors, in which positive for set and negative for reset. Although the Si buffer layer didn't change the RS polarity, the drastic decrease in forming voltage (V_F) was observed for the device incorporated with Si buffer layer. Moreover, due to the decreased V_F , the compliance current (C.C.) of the device with Si could be set to a lower value, which can improve RS characteristics according to the CF mechanisms [B2]. **Figure B2** depicts the enlarged window and improved endurance characteristics could be achieved by the device with Si buffer layer than that of device without Si. It also shows that high resistive state (HRS) and low resistive state (LRS) of the device with the Si layer were much larger than that without the Si layer, which indicates that the device with Si was protected from irreversible hard breakdown because of avoidance of the high voltage forming process. In summary, by inserting a Si buffer layer to the bottom interface of the W/CeO₂/TiN device, it was able to work under lower forming voltage and C.C. with larger window and better endurance characteristic.

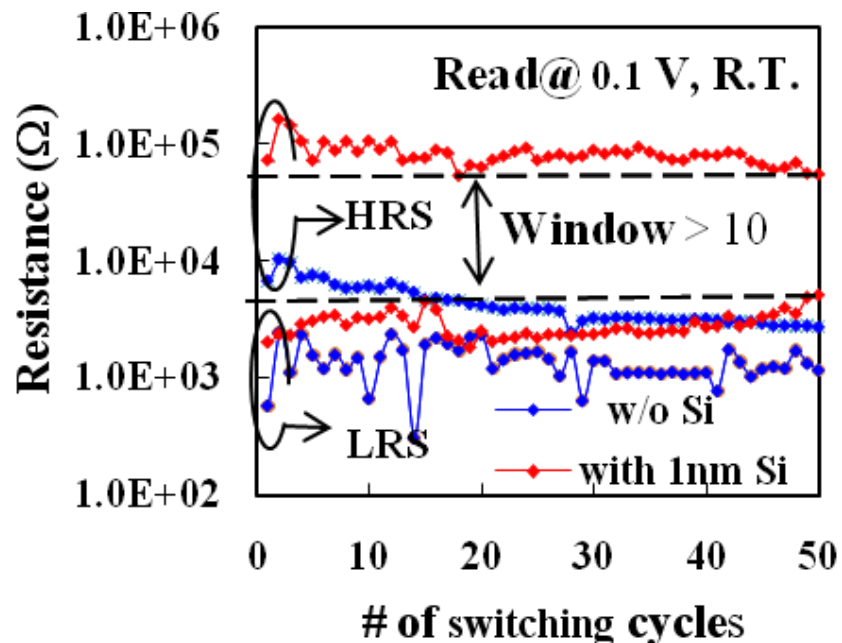


Fig. B2. HRS and LRS in 50 times cycles of the 20 nm CeO₂ based devices with and without 1 nm Si buffer layer. While the device without Si doesn't have stable window, the one with Si is able to keep a window large than 10 times in 50 cycles.

In consideration that the RS mechanism in cerium oxide is well explained by CFs based on oxygen vacancies [B8] and the reactivity between Si and CeO₂, we proposed following model to explain the underlying reason that how the Si buffer layer improved the device performance. **Figure B3(a)** shows the normal forming process based on CF mechanism of the device without the Si layer: In the forming process, oxygen vacancies were formed at anode and a large voltage was necessary for driving the vacancies to the cathode until the whole CFs were formed. Then, the device was able to be reset and set by annihilation and formation of partial CFs under small voltages. **Figure B3(b)** shows the RS behaviors of the device incorporated with Si buffer layer. After suitable thermal treatment, the Ce-silicate could be formed at the interfacial transition layer between CeO₂ and Si layers. During the formation of silicate, the oxygen ions at the surface of CeO₂ were involved in the oxidation process of Si and thus oxygen vacancies were left to the surface of CeO₂. Similar phenomenon that increased number of oxygen vacancies after formation of Ce-silicate was also reported by the studies of CeO₂ based MOS capacitors [B12]. Moreover, because oxygen vacancies in cerium oxide tend to rearrange into the line pattern [B13], the pre-existed partial CFs were probably formed in the bulk of fresh W/CeO₂/Si/TiN device. Once positive voltage is applied, the formation of the last part of the CFs was followed by the field enhancement effect at the peak of the partial CFs. Therefore, the forming voltage could be largely decreased because only parts of the filaments were needed to form in the devices with Si buffer layer. By formation of Ce-silicate and thus properly introduction of oxygen vacancies at the interface, the Si buffer layer made CFs were more easily to be form in the forming process.

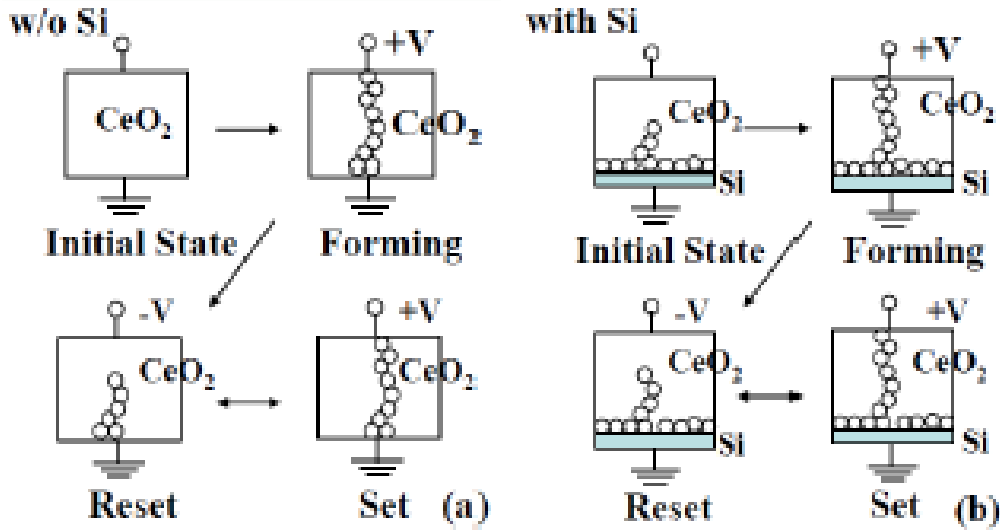


Fig. B3. Schematic illustration of RS behaviors of the W/CeO₂/Si/TiN device (a) and the W/CeO₂/Si/TiN device (b). The open circles represent for oxygen vacancies.

In addition, it is also shown in **Fig. B1** that the reset process of W/CeO₂/Si/TiN was a gradual process depending on the negative sweeping voltage (V_{stop}) applied to the TE. **Figure B4(a)** shows the different HRS and LRS of the device operated under different $|V_{\text{stop}}|$ ranging from 1.4 V to 3.2 V. As $|V_{\text{stop}}|$ increased, the LRS remained almost same while HRS stepwise increased and became unstable beyond $|V_{\text{stop}}|$ of 2.2 V. From the viewpoint of multiple CFs mechanism, it could be regarded that substantially same number of CFs were formed in LRS, while different numbers of CFs ruptured in reset process due to different $|V_{\text{stop}}|$. The instability of HRS at high $|V_{\text{stop}}|$ was probably caused by increased joule heat, which produced much more uncertainty to the rupture of CFs. In order to further clarify the dependence of CFs rupture on reset voltage, a simplified equivalent circuit, which is shown in the inset of **Fig. B4(b)**, is used to evaluate the resistance between TE and BE. The devices could be approximated as a parallel connection of insulator layers with several CFs with an identical resistance. Accordingly, the conductance of LRS (G_{ON}) can be expressed as:

$$G_{\text{ON}} = g_0 + N \times g_1 \approx N \times g_1 \quad (1)$$

where g_0 represents the original conductance of the CeO_2 thin film, and g_1 is the conductance of each CF, and N is the number of CFs that formed in LRS. Compared to g_1 , g_0 is very small and can be ignored because of its insulator characteristics. On the other hand, the conductance of HRS (G_{OFF}) can be expressed as:

$$G_{\text{OFF}} = g_0 + (N - n(V_{\text{stop}})) \times g_1 \approx (N - n(V_{\text{stop}})) \times g_1 \quad (2)$$

Here, $n(V_{\text{stop}})$ signifies the number of filaments that rupture in the reset process governed by V_{stop} and thus $N - n(V_{\text{stop}})$ represents the number of CFs that left in HRS. Using equations of (1) and (2), the ratio of ruptured filaments as a function of V_{stop} can be evaluated as follow:

$$n(V_{\text{stop}})/N = 1 - G_{\text{OFF}}/G_{\text{ON}} \quad (3)$$

The average values of G_{OFF} and G_{ON} in **Fig. B4(a)** were used to calculate the ratio of the ruptured CFs as shown in **Fig. B4(b)**. It shows that once the reset voltage exceeds 1.4 V, most of filaments would rupture in a short voltage range. For instance, 90 % of the CFs had been ruptured when $V_{\text{stop}} = 2.2$ V and V_{stop} larger than this actually contributed a little to the reset process. This result implies that by proper control of reset voltage, power consumption and instability of the device could be decreased without sacrificing too much window.

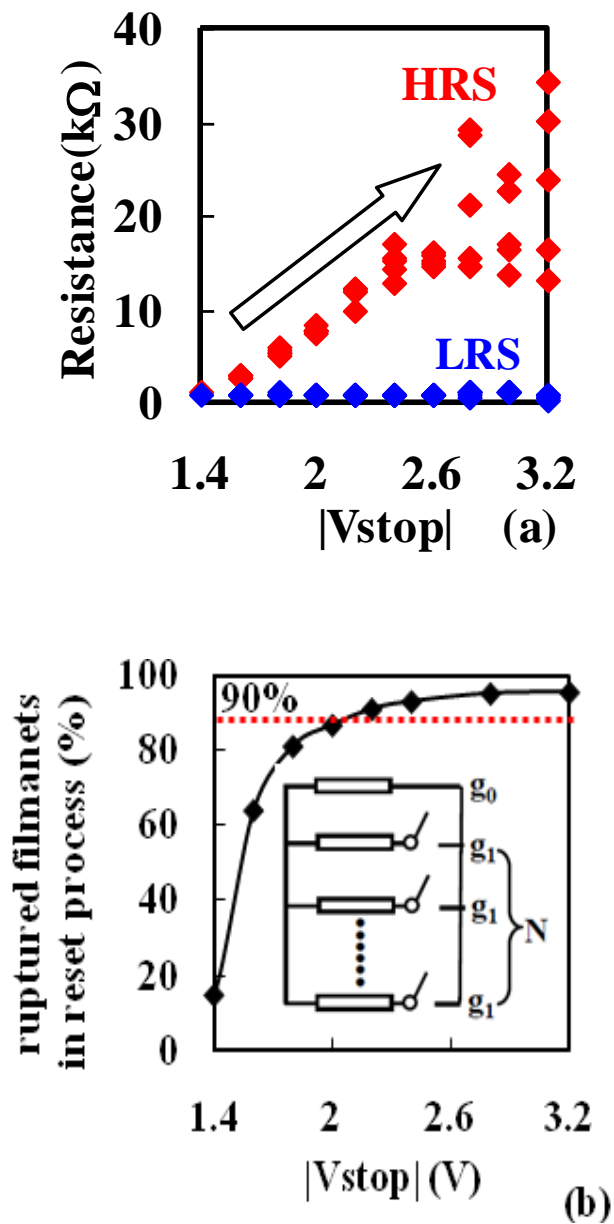


Fig. B4. (a) The HRS and LRS of the W/CeO₂(20nm)/Si(1nm)/TiN device as continually increase $|V_{stop}|$ every 5 times switching cycles from 1.4 to 3.2 V at a step of 0.2 V , and (b) The ratio of ruptured filaments in reset process on $|V_{stop}|$, and the inset shows equivalent circuit of the CFs dominated ReRAM device.

B4 Conclusion

In conclusion, thanks to incorporating a Si buffer layer at the bottom interface, the ReRAM cell having W/CeO₂/Si/TiN structure could be operated at lower forming voltage and C.C. with better window and endurance characteristics than that of the device without Si. This improvement was speculated to be caused by the formation of Ce-silicate at the interfaces, which properly introduced oxygen vacancies at the interface and thus made CFs form more easily in the forming process. Such result shed light on eliminating electrical forming in ReRAM device through interface engineering, which doesn't lead to fundamental change of bulk properties. Besides, by adopting the parallel CFs model, the process of successive rupture of the CFs as a function of reset voltage was quantitatively described, which not only provides a guideline of voltage control for optimizing device performance, but also provides an insight into the gradual reset process.

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About characterization of interface and near interface traps in dielectric/semiconductor structures:

- J1. **C. Dou**, D. Lin, A. Vais, T. Ivanov, H. -P. Chen, K. Martens, K. Kakushima, H. Iwai, Y. Taur, A. Thean, and G. Groeseneken, "[Determination of energy and spatial distribution of oxide border traps in InGaAs MOS capacitors from capacitance-voltage characteristics measured at various temperatures](#)", *Microelectronics Reliability* (2014), in press, <http://dx.doi.org/10.1016/j.microrel.2013.12.023>
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- J3. E. Miranda, S. Kano, **C. Dou**, J. Sune, K. Kakushima, H. Iwai, "[Effect of an ultrathin SiO₂ interfacial layer on the hysteretic current-voltage characteristics of CeO_x-based metal-insulator-metal structure](#)", *Thin Solid Films*, vol. 533, pp. 38-42 (2013)
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- J7. Y. Wu, **C. Dou**, W. Feng, K. Kakushima, K. Ohmori, P. Ahmet, T. Watanabe, K. Tsutsui, A. Nishiyama, N. Sugii, K. Natori, K. Yamada, Y. Kataoka, T. Hattori, and H. Iwai, "[Influence of structural parameters on electrical characteristics of schottky tunneling field-effect transistor and its scalability](#)", *Jpn. J. Appl. Phys.*, vol. 52, pp. 04CC28/1-5 (2013)

Conference publication: (first author)

International conference publication:

- C1.** W. Li, K. Nakajima, **C. Dou**, K. Kakushima, P. Ahmet, K. Tsutsui, A. Nishiyama, N. Sugii, K. Natori, T. Hattori, and H. Iwai, "[Evaluation of Interfacial State Density of MOS Capacitor with Three-Dimensional Channel by Conductance Method](#)", *ECS Trans.*, vol. 44, no. 1, pp. 1275-1279 (2012)
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