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種別(和文)	論文要旨
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（博士課程）
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論 文 要 旨

THESIS SUMMARY

専攻： Department of	Physical Electronics 専攻	申請学位（専攻分野）： Academic Degree Requested	博士 (Philosophy) Doctor of
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要旨（英文 800 語程度）
Thesis Summary（approx.800 English Words ）

This thesis presents a design strategy for ultra-low-voltage (ULV) high-speed analog-to-digital converters (ADCs). To address the challenges associated with supply voltage scaling, information from charge-, time-, and digital-domains are considered in addition to the conventional electrical voltage and current. Due to these additional dimensions, valuable information can be extracted to relax the design challenges of conventional analog circuit design in an ultra-low supply voltage environment.

Chapter 1 sets the background of this research. As the feature size of advance nanoscale CMOS technologies continues to scale, the maximum supply voltage is expected to be lowered to maintain the reliability of the devices, to avoid thermal issues, and to reduce power density. According to the International Technology Roadmap for Semiconductors (ITRS), the maximum supply voltage for CMOS technologies is expected to scale to around 0.5-to-0.6 V in the next decade or so. With such a scaled supply voltage, many conventional analog circuit design methodologies and techniques will be outdated. Therefore, new design strategies and techniques will be required for future electronics.

In Chapter 2, a design strategy for ULV high-speed ADCs is presented. Firstly, a new speed-conscious index, the figure-of-merit (FoM)-delay (FD) product, is proposed to provide a clear guideline between energy efficiency and conversion speed. Next, discrete-time charge-steering circuits are presented as an alternative to the conventional continuous-time current-steering circuits. This is followed by the concept of exploiting time-domain signal processing in addition to the traditional voltage-domain. Finally, the concept of digitally-assisted analog circuits is introduced to alleviate some of the design challenges with a scaled supply voltage.

In Chapter 3, an ULV charge-steering dynamic amplifier using a common-mode detection technique is proposed as an alternative to the conventional continuous-time current-steering amplifiers. The essential characteristics of an amplifier are analyzed, including gain, linearity, power consumption, and noise. To verify the idea, a prototype dynamic amplifier has been developed in 90 nm CMOS. In measurement, the proposed dynamic amplifier achieves a 13 dB gain with less than 1 dB drop over a differential output signal swing of 340 mV_{pp} with a supply voltage of 0.5 V. The attained maximum operating frequency is 700 MHz. With a slight increase of the supply voltage to 0.7 V, the gain increases to 16 dB with a signal swing of 700 mV_{pp}.

In Chapter 4, a 0.5 V high-speed 7-bit flash ADC using all-digital time-domain delay interpolation is presented. In this chapter, various ULV compensation techniques for latch-based comparators, or dynamic

comparators, are discussed and two suitable candidates are proposed. Furthermore, an all-digital time-domain interpolation is introduced to further enhance the resolution of a flash ADC. A 7-bit prototype flash ADC fabricated in 90 nm CMOS is measured to show the validity of these concepts. The measured results show that the prototype flash ADC achieves an ENOB of 5.5 bits while operating at 420 MS/s with two-channel interleaving. At this conversion rate, it consumes a total of 4.1 mW. The lowest measured FoM is 195 fJ/conversion-step during single-channel operation at 210 MS/s, which results in an extremely low FD product of 0.93 pJ×ns/conversion-step.

In Chapter 5, a 0.55 V 7-bit interpolated pipeline ADC using dynamic amplifiers is proposed. In this ADC, high-speed open-loop dynamic amplifiers with a common-mode detection technique are used as residue amplifiers to increase the ADC's speed, to enhance the robustness against supply voltage scaling, and to realize clock-scalable power consumption. To mitigate the absolute gain constraint of the residue amplifiers in a pipeline ADC, the interpolated pipeline architecture is employed to shift the gain requirement from absolute to relative accuracy. To show the new requirements of the residue amplifiers, the effects of gain mismatch and nonlinearity of the dynamic amplifiers are analyzed. The 7-bit prototype ADC fabricated in 90 nm CMOS demonstrates an ENOB of 6.0 bits at a conversion rate of 160 MS/s with an input close to the Nyquist frequency. At this conversion rate, it consumes 2.43 mW from a 0.55 V supply. The resulting FoM of the ADC is 240 fJ/conversion-step, which translates to a FD product of 1.5 pJ×ns/conversion-step.

In Chapter 6, a 0.5-to-1 V 9-bit digitally interpolated pipelined-SAR ADC using a dynamic amplifier is proposed. The proposed digital interpolation technique alleviates the inter-stage gain requirement of a pipelined-SAR ADC making this ADC insensitive to gain variation. With a relaxed gain requirement, a dynamic amplifier is employed as the residue amplifier making the proposed design clock-scalable and robust to supply voltage scaling. The prototype ADC fabricated in 65 nm CMOS demonstrates an ENOB of 7.88 bits up to 30 MS/s with an input close to the Nyquist frequency at 0.6 V. At this conversion rate, it consumes 0.48 mW resulting in a FoM of 68 fJ/conversion-step and a FD product of 2.3 pJ×ns/conversion-step.

Finally, the conclusion of this research is drawn in Chapter 7. The future prospects of ULV high-speed ADC design and the future works related to this research topic are discussed.