論文 / 著書情報
Article / Book Information

題目(和文)	物理的パターン形成による少数電子シリコン量子ドットの電気特性と電子スピン量子ビットへの応用に関する研究
Title(English)	Physically-defined few-electron silicon quantum dots for electron spin qubits
著者(和文)	堀部浩介
Author(English)	kosuke Horibe
出典(和文)	学位:博士（工学）, 学位授与機関:東京工業大学, 報告番号:甲第9784号, 授与年月日:2015年3月26日, 学位の種別:課程博士, 審査員:小田　俊理,波多野　睦子,宮本　恭幸,河野　行雄,小寺　哲夫,藤原　聡
Citation(English)	Degree:, Conferring organization: Tokyo Institute of Technology, Report number:甲第9784号, Conferred date:2015/3/26, Degree Type:Course doctor, Examiner:,,,,,
学位種別(和文)	博士論文
Type(English)	Doctoral Thesis

Physically-defined few-electron silicon quantum dots for electron spin qubits

Kosuke Horibe

12D14027

Supervised by Professor Shunri ODA and Associate Professor Tetsuo KODERA

Tokyo Institute of Technology

February 2015

Dissertation submitted to the Tokyo Institute of Technology

for the degree of Doctor of Engineering

Abstract

We fabricate physically-defined silicon quantum dot devices to investigate electron spin qubits for quantum information processing. Silicon is a promising material for electron spin qubits because of its several profitable properties and also we use a lithographical-defined structure which has a great advantage for integration of the qubits. In this thesis, we demonstrate charge sensing measurements of charge occupancy in silicon quantum dots using a charge sensor, observation of few-electron regime in silicon single and double quantum dots, measurements of the back-action generated from a charge sensor, and pulse measurements to investigate the jkPauli spin blockade in a double quantum dot. These topics are essential for achieving the electron spin qutits and we believe the study reported here give great developments for achieving electron spin qubit architecture in silicon devices.

Contents

Chapter 4 and chapter 6 include contents of the following paper (1) which is supposed to be published in Applied Physics Letters.

(1) Kosuke Horibe, Tetsuo Kodera, and Shunri Oda, **"Lithographically-defined few-electron silicon quantum dots based on a silicon-on-insulator substrate"**, (Accepted in Applid Physics Letters).

Chapter 5 and chapter 7 include contents of the following paper (2) and (3), respectively.

(2) Kosuke Horibe, Tetsuo Kodera, Tomohiro Kambara, Ken Uchida, and Shunri Oda, **"Key capacitive parameters for designing single-electron transistor charge sensors"**, Journal of Applied Physics, Vol. 111, pp. 093715 1-5 (2012).

(3) Kosuke Horibe, Tetsuo Kodera, and Shunri Oda, **"Back-action-induced excitation of electrons in a silicon quantum dot with a single-electron transistor charge sensor"**, Applid Physics Letters, Vol.106, pp. 053119 1-5 (2015).

Chapter 1

Introduction

1.1 Introduction

In this section, firstly we introduce overview about the quantum computing, quantum bit using spin of electrons, semiconductor quantum dots, silicon quantum dots and several issues for the electron spin quantum bits. Secondly we describe purpose of this work and outlines about each study.

1.2 Quantum computing

In recent years the semiconductor industry has achieved miniaturization of device elements and great development with increase in the operation speed, lower power consumption, and higher integration of the device elements on chips. These great progresses of the nanofabrication technology have enabled electrons to be confined in 0 dimensional structure of so-called ‘quantum dot (QD)’ and in rate years various properties of matter about electrons confined in QDs are investigated [1, 2]. In particular, studies for the ‘quantum computer’, which utilizes quantum mechanics of the spin or charge states of electrons confined in few-electron QDs, attracts attentions in both experimental and theoretical approaches [3].

Although first research for the quantum computing has been started since 1960’s, it was not obvious whether the quantum computer is superior in computation speed compared with any classic computer. Therefore only the theoretical approaches had been performed in those days.

However, in 1994 the quantum algorithm, which can solve the prime factorization with very small error probability and especially high speed, was supposed and shown by Peter W. Shor who is a researcher of the Bell Institute [4]. The difficulty of solving the prime factorization of

very large integer guarantees public key encryption such as RSA encryption; For example it is impossible to solve the prime factorization of large numbers with realistic computation time even if we use the super computer which has current best computation performance. However, if the quantum computer comes out and use the quantum algorithm shown by Shor, the prime factorization can be carried out significantly fast, which will give an extremely large social impact. Therefore experiment of the quantum computer in the real physics system has been accelerated since the discovery of the quantum algorithm.

1.3 Charge qubits and electron spin qubits based on semiconductor quantum dots

A bit in the quantum computer is called as ‘quantum bit’ (qubit) and constructed by superposition of two level quantum states. Quantum computing requires two well defined and controllable states as a qubit, which give the ability to construct a quantum logic gate. Therefore, if a physical system has two clear quantum states it could become a candidate of the qubit. However it is necessary to keep the ‘coherence’ of the quantum states during the qubit operation (coherent operation). So for, various two levels system for the qubits has been investigated theoretically and experimentally in the recent study, in such as nuclear magnetic resonance (NMR) on molecules in solution [5], trapped ions, and linear optical quantum computer [6]. However, these quantum systems are not suitable for the integration of many qubits because of its difficulty to extend construction experimentally. Therefore, for future integration, studies for qubits based on the solid-state quantum systems have been investigated recent years, in which especially charges or spins of electrons confined in semiconductor quantum dots (QDs) have attracted attentions as a qubit.

One example of the qubit using electric charges is the charge states of electrons confined in a tunnel coupled double QD, in which we use the superposition of probability of existence of the electron in each QD. So far, one or two charge qubit operation has been achieved experimentally using a two-dimensional electron gas in a compound semiconductor heterostructure (GaAs/AlGaAs) [7, 8]. However typical charge qubits have short coherence times (several nanoseconds order), which is not enough to perform the practical quantum calculations.

On the other hand, longer coherence times of several microseconds have been expected in the spin qubits using spins of electrons confined in semiconductor QDs [9, 10, 11], and various studies are performed in recent years. It has been shown that the basic quantum gates can be achieved by the two-qubit operations which consist of single spin manipulation and utilization of an interaction between two spins. Loss and DiVincenzo have shown XOR gate can be constructed by combining single-spin rotations with SWAP operations [9]. The experiments of solid-state spin qubits in semiconductor-based structures such as GaAs/AlGaAs heterostructures [12, 13, 14, 15, 16, 17, 18, 19], Si/SiGe heterostructures [20, 21, 22, 23], silicon metal-oxide-semiconductor (MOS) structures [24, 25, 26], nanowires [27], carbon nanotubes [28], and phosphorus donors in silicon [29, 30]. The electron spins confined in QDs can be manipulated by the exchange interaction between tunnel-coupled QDs [12, 13, 17, 20, 24] or the electron spin resonance (ESR) using the effective oscillating external magnetic field [15, 18, 19, 25, 27, 28]. The measurements of the spin states can be performed by spin-to charge conversion using the Pauli spin blockade [16, 31] or the energy selective spin readout [26, 40].

1.4 Silicon quantum dots

The primitive studies for the spin qubit using spins of electrons confined in QDs have been performed in the two dimensional electron gas (2DEG) systems based on compound semiconductors such as the GaAs/AlGaAs heterostructure because it has a relatively small effective mass of electrons ($m^* = 0.067m_0$ for GaAs, m_0 is a mass of a free electron). The small effective mass of electrons gives a remarkable quantum effect in the experiment at cryogenic temperature with the devices fabricated by using electron beam lithography (EBL), and therefore it is suitable for constructing clear quantum states and investigating its quantum properties. However, the progress of the study of the quantum operation has been clarified that the hyperfine interactions between electron spins and nuclear spins in the compound semiconductors destroy (decoherence) the coherence of the spin qubits [10]. Therefore in recent years the study using the group IV semiconductor, which has naturally less nuclear spins, has gathered attentions. For example, studies such as Si/SiGe heterostructures [20, 21, 22, 23, 32, 33, 34, 42, 44], silicon MOS structures [24, 25, 26, 35, 36, 37, 38, 39, 40, 41], silicon nanowires [45, 46, 47, 48, 49], Ge/Si core shell nanowires [43], phosphorus donors in silicon [29, 30], carbon

nanotube [28, 50, 51, 52, 53, 54] and graphenes [55, 56], have been performed experimentally. Particularly, Silicon is a promising material for spin qubits because it has extremely long coherence times [57, 58, 59, 60, 61] due to weak spin-orbit coupling [62, 63], the lack of piezoelectric electron-phonon coupling [64], and the capability of isotopic purification for the manufacture of nuclear spin-free silicon substrates to remove hyperfine coupling [65]. The additional advantages of silicon is that the fabrication process for silicon devices can be similar to conventional silicon device fabrication technologies such as the Complementary Metal-Oxide-Semiconductor (CMOS) process.

Significant progress has been achieved for electron spin qubits in silicon. Singlet-triplet qubit in a double QD based on Si/SiGe heterostructures has been achieved [20, 23]. Here manipulations of singlet-triplet qubit using exchange interaction between coupled QDs has been demonstrated with T_2* = 360 ns [20]. In another study T_1 = 10 ms on zero magnetic fields extends to T_1 = 3 s for triplet- states at B = 1T in singlet-triplet qubits [23]. Singlet-triplet qubit in a double QD based on the coupled phosphorus dimers in silicon has also been studied and T_1 = 4 ms has been observed [29]. Single-electron spin qubit in QDs based on Si/SiGe heterostructures [21] and Si MOS structures [25 ,26] or in phosphorus donors in silicon [30] have been reported. In Ref. 25, manipulation of single-electron spin qubits using electron spin resonance has been achieved with long coherence time T_2* = 63 ns compared to T_2* = 10 ns in GaAs QDs. Hybrid qubits in a double QD based on Si/SiGe heterostructures [30] and CNOT gate realized by two-qubit operation in a double QD based on an isotopically enriched Si MOS structures [24] have been also achieved in recent study.

1.5 Few-electron silicon quantum dots

To implement quantum logic gates based on electron spin, it is necessary to reduce the electron number in individual QDs to levels of a few-electrons or a single-electron to create spin states that are energetically well defined and separated from other states. However, it is difficult to form single-electron occupancy of QDs in silicon devices because of the relatively large effective mass m* of electrons (for the minor axis direction $m^* = 0.19m_0$ and for major axis direction $m^* = 0.916m_0$ respectively) and their small tunneling rates compared to those in compound semiconductor materials, such as in the GaAs/AlGaAs heterostructure. The

formation of a few-electron regime in silicon double QDs have been achieved in a Si/SiGe heterostructure [20, 21, 22, 23, 31, 33, 34, 42] and a silicon MOS structure [24, 25, 26]. The few-electron (or few-hole) regime in silicon single QDs has been achieved in a MOS structure [35, 36, 39, 40, 41] and a nanowire structure [45].

1.6 Valley-orbit states in silicon quantum dots

The conduction band structure in silicon has complication compared to GaAs because silicon has the valley degree of freedom for electrons in the conduction band [66, 67, 68, 69, 70]. In recent years valley physics in silicon has been studied both experimentally [21, 25, 26, 29, 32, 35, 41, 44, 78, 79, 80, 81, 81] and theoretically [71, 72, 73, 74, 75, 76, 77]. Bulk silicon has a sixfold degenerate conduction-band minimum (valley) in the Brillouin zone (Figure 1.1(a)). This degeneracy is lifted by strain or the presence of an interface. Confinement of electrons in the *z*-direction at the Si/SiO_2 interface lifts the sixfold valley degeneracy to four Δ valleys and twofold Γ valleys (Figure 1.1(b) and 1.1(c)). Here the four Δ valleys and two Γ valleys have a heavy effective mass $m^* = 0.916m_0$ and a light effective mass $m^* = 0.19m_0$ parallel to the interface. Therefore the four Δ valleys have an energy several 10 meV higher than the two Γ valleys. The sharp and flat $Si\text{-}SiO_2$ interface produces a potential step in the *z*-direction and lifts the degeneracy of the Γ valleys to the valley splitting E_v. Theoretically the valley splitting is predicted generally as the order 0.1 to 0.3 meV [71]. On the other hands, experimentally the valley splitting in a silicon inversion layer varies from 0.3 to 1.2 meV [78]. A very large valley splitting of 23 meV has also been observed in a similar structure and is explained in Ref. [79]. In silicon single QD based on a metal-oxide semiconductor structure the valley splitting of 0.3 to 0.8 meV has been observed by using magnetic spectroscopy or steep increase in relaxation of electrons (hot spot) [26]. In Si/SiGe QDs the valley splitting of 0.12 to 0.27 meV has been observed [32]. Hybridization between valleys and orbits is also predicted [75], leading it incongruous to define distinct orbital and valley quantum number. How the valley-orbit level behaves such as like valleys or like orbits depends on the degree of mixing.

The ‘valley blockade’ is also known as the blockade in transition of electrons or holes between different valley states. In a carbon nanotube-based QD the valley blockade has also been observed [28]. In silicon double QDs based on a metal-oxide semiconductor structure the valley

blockade has also been observed in spin-valley blockade configurations [25].

Typically larger valley splitting is desirable for electron spin qubits because the larger splitting prevent the different valleys from mixing each other and occurring the valley blockade. The valley physics described here such as valley splitting, valley-orbit states, and valley blockade require further more investigation to reveal how it influence to electron spin qubit operation.

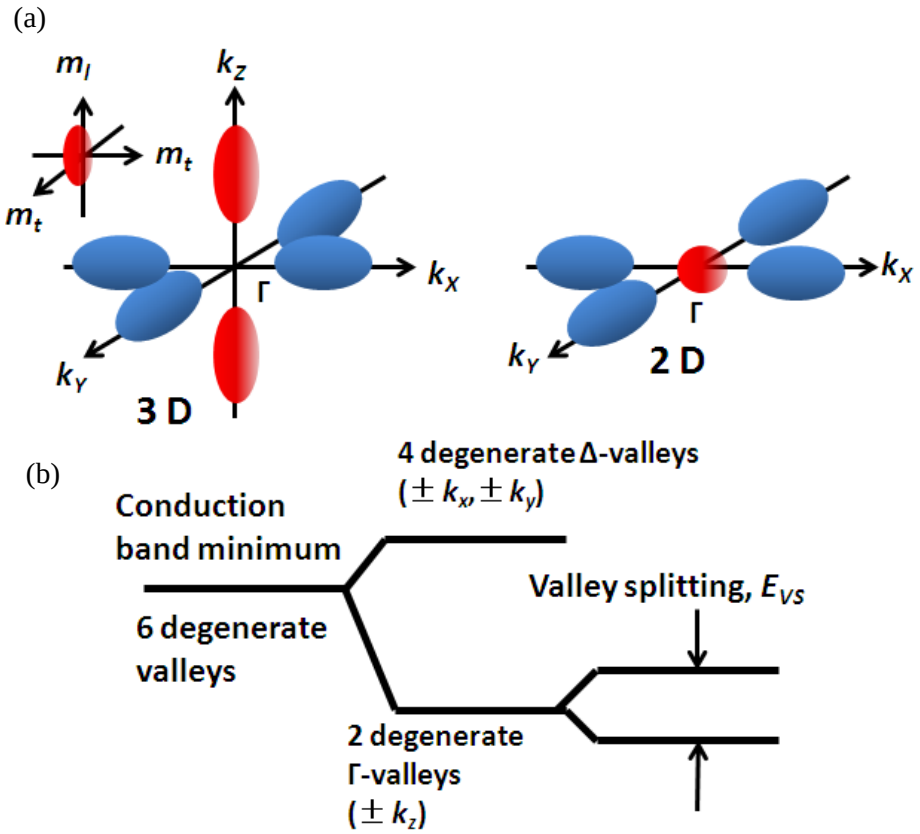


FIG. 1.1: (a) Schematic of conduction band minima (Valleys) in bulk silicon. Six ellipsoids of equal energy in the Brillouin zone are shown. Each ellipsoid has two light traverse masses (m_t) and a heavy longitudinal mass (m_l). (b) Schematic of valleys under z-direction confinement at the Si/SiO_2 interface. (b) Schematic of valley degeneracy in bulk silicon and the valley splitting under z-direction confinement.

1.7 Single electron transistors and charge sensors

Single electron transistors (SETs) are currently among the most widely studied nanoelectronic components. In particular, their strong charge sensitivity allows them to be used as charge

sensors for reading out spin or charge qubits contained in quantum dots (QDs), [82, 83, 84, 85, 86] and also as quantum point contact (QPC) charge sensors. In 2DEG systems such as GaAs/AlGaAs and Si/SiGe heterostructures, many experiments have been carried out on QD-QPC structures [12, 14, 15, 18, 19, 20] and some recent studies have focused on the use of QD-SET structures in order to improve the signal-to-noise ratio (SNR) during qubit readout. [17, 20]

1.8 Back-action of charge sensors

In qubit measurements, the so-called "spin-to-charge conversion" [17, 87] allows the spin state of electrons in QDs to be detected by sensing the electron occupancy states of the QDs using a nearby QPC or SET as a charge sensor. However, charge sensing using SETs and QPCs has an inevitable effect on the qubit states; this effect is known as the back-action [88, 89, 90]. Several prior studies of compound semiconductor devices such as GaAs/AlGaAs heterostructures show that the dissipated energy from a QPC via phonons or photons can be absorbed by electrons in QDs and excites the electrons either in the QDs themselves [90, 91, 92, 93, 94, 95] or in neighboring leads [96] to excited states as a result. Because this excitation and transportation indicate qubit relaxation and dephasing, efforts must be made to minimize this back-action effect while maintaining a desirable level of sensitivity.

1.9 Exchange interaction and exchange-only qubits

Exchange interaction between coupled QDs can evolve the single-triplet states in few-electron double QDs. Figure 1.2 shows the Schematic of energy diagram versus detuning energy ε (see section 2) in (1,1) singlet-triplet qubits. The exchange energy J is defined as energy splitting between (1,1) singlet stats and (1,1) triplet states. J can evolve the singlet and triplet states and manipulate the qubits. The 'exchange-only qubit' in a triple QD structure has been also proposed in recent years [97]. In this system, the three spin stats in the triple QD behave as single qubit and the two different exchange couplings between tunnel-coupled QDs are used for manipulating the spin states. The full single qubit operation can be achieved by using only the

two exchange couplings and does not require topical magnetic fields, which is great advantage for integration of qubits. The manipulation of the exchange-only qubit has been achieved in GaAs/AlGaAs heterostructures. [98, 99] However it has not been achieved in silicon devices because forming few-electron states of triple QDs is relatively difficult in silicon.

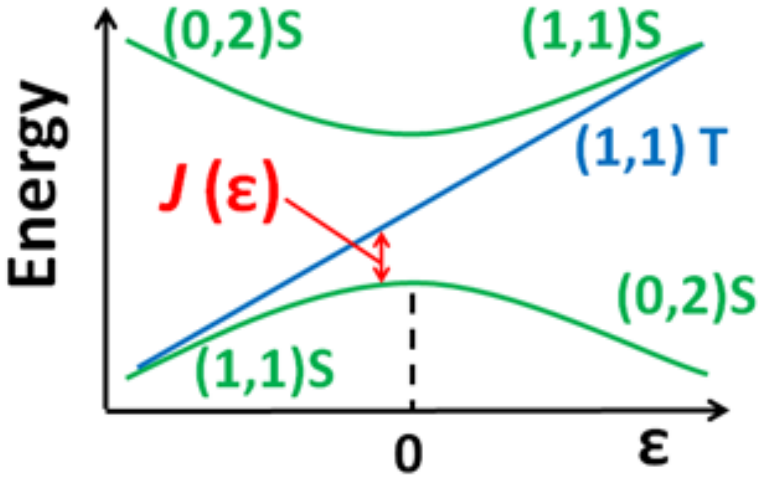


FIG. 1.2: (a) Schematic of energy diagram versus detuning energy ε (see section 2) in (1,1) singlet-triplet qubits. Exchange energy J can evolve the singlet and triplet states, which leads manipulation of the qubits.

1.10 Fabrication of lithographically-defined silicon quantum dots and research approach in this thesis work

We regard the exchange-only qubit system as the promising architecture for achieving the quantum computing. Our goal is to construct the exchange-only qubit in the silicon device which have long coherence time of electron spin states.

In this work we fabricate lithographically-defined silicon QDs, which are presented in capture 3 in detail. This device structure has great advantage for integration of QDs because the QDs formed by lithographically-defined physical shape of the structure and does not require gate contacts to create the confinement potential of the QD. Therefore it has high potential to possess complicated structures such as multiple QDs ant it has adaptability for the exchange-only qubit.

However this device structure has also many assignments to achieve and our purpose in this work is resolving these assignments.

The assignments tackled in this work in the lithographically-defined silicon QD device is ① charge sensing of the electron occupancy in QD using charge sensor, ②forming few-electron regime of the QDs, ③obtaining the strategy for designing the SET charge sensor to improve the SNR of charge sensing signal, ④control of the tunnel couplings between QDs for tuning the exchange coupling, ⑤investigation for the back-action generated from charge sensor, ⑥ observation of the spin blockade in the few-electron regime of the QDs using pulse voltage measurements.

In chapter 4 we present the experimental results of the charge sensing measurements and observation of few-electron regime in silicon single and double QDs. Silicon QD devices with a proximal SET charge sensor have been fabricated in a metal-oxide-semiconductor structure based on a silicon-on-insulator substrate. The charge state of the QDs could be clearly read out using the charge sensor via the SET current. The lithographically-defined small QDs enabled clear observation of the few-electron regime of a single QD and a double QD by charge sensing. To date, most of these silicon QD devices have gate-defined QD structures, in which QDs are formed by confinement of the electric fields from fine metal top-gates. However, the lithographically-defined silicon QD device reported in this thesis is technologically simple and does not require electrical gates to create QD confinement potentials, which is highly advantageous for the integration of qubits.

In chapter 5 we present measurements and calculation of the capacitive parameters of the charge sensor to obtain the ideal design to reduce the signal-to-noise ratio in the charge sensing. To investigate their capacitive parameters, which are related to the signal-to-noise ratio during qubit readout, twin silicon single QDs were fabricated using a lithographic process on a silicon-on-insulator substrate. Since the configuration and dimensions of the QDs could be determined by direct imaging, the theoretical capacitive parameters could be compared to the measured values. Good agreement was found between the calculated and measured values, which confirm the validity of the calculation method. The results indicated that decreasing the SET diameter reduces the capacitive coupling between qubits but increases the signal-to-noise ratio for both dc and radio frequency single-shot measurements.

In chapter 6 we introduce control of the tunnel coupling between coupled QDs. Electron spin

qubit architecture require to control the exchange coupling between tunnel coupled QDs and usually the exchange coupling energy *J* can be controlled by applying pulse voltage into the gate contact in which the stats on the charge stability diagram in the tunnel coupled QDs moves detuning direction. This method is valid in our device. However it is necessary to control the maximum value of *J* to allow flexible qubit operation. Tunnel coupling on tunnel barriers of the QDs can be controlled by tuning the top-gate voltages, which accommodates manipulation of the spin quantum bit using exchange interaction between tunnel-coupled QDs.

In chapter 7 we present back-action measurements. The back-action in the readout of quantum bits is an area that requires a great deal of attention in electron spin based-quantum bit architecture. We report here back-action measurements in a silicon device with quantum dots and a single-electron transistor charge sensor. We observe the back-action-induced excitation of electrons from the ground state to an excited state in a quantum dot. We also present fitting calculation to estimate the excitation rate of the electrons. We discuss about conditions which satisfy both suitable SET charge sensor sensitivity for qubit readout and low back-action-induced transition rates.

In chapter 8 we present pulse measurement of Pauli spin blockade in few-electron silicon double QDs. The Pauli spin blockade is greatly useful for measurements of electron spin qubits, in which the spin-to-charge conversion is used to probe the spin stats in double QD systems. In the qubit measurements, single-shot measurements (i.e. time-resolved measurements) of the spin states using pulse measurements required to achieve qubit manipulation. In our measurements, we observed the spin blockade (5,1)-(4,2) tunneling region of a DQD by applying pulse voltage to two side-gate. We also present of estimation of relaxation time of the singlet-triplet qubit from the pulse frequency.

Chapter 2

Theory for quantum dots and charge sensors

2.1 Introduction

In this chapter, we describe the theory of electric transportation which is necessary to analyze the characteristic of coupled QDs. Firstly the electrostatic energy in *N* conductors is introduced, and the Coulomb blockade in a single tunnel junction and the electric transportation in a single and double QD are described in turn [61, 100, 101]. Secondly we introduce theory for charge sensor such as signal-to-noise ratio, charge sensitivity, and RF-SET measurements [102, 103, 104].

2.2 Coulomb Blockade and transport of theory for quantum dots

2.2.1 Electrostatic energy in *N* conductors

We consider a system in which there are *N* conductors, and there are capacitive couplings between every conductors and ground. The total number of the capacitance in the system can be expressed as

$$N + \sum_{k=1}^{N} \frac{k-1}{2} = \frac{N(N+1)}{2} \quad . \tag{2.1}$$

Total charge Q_j in conductor j can be expressed as

$$Q_j = \sum_{k=1}^{N} q_{jk} = \sum_{k=0}^{N} c_{jk}(V_j - V_k)$$

$$= c_{j0}(V_j - V_0) + c_{j1}(V_j - V_1) + \cdots + c_{jN}(V_j - V_N)$$

$$= -c_{j0}V_0 - c_{j1}V_1 - \cdots - c_{j(j-1)}V_{j-1} + \sum_{k=0,k\neq j}^{N} c_{jk}V_j - c_{j(j+1)}V_{j+1} - \cdots - c_{jN}V_N \quad .$$

(2.2)

Here c_{jk} and q_{jk} are the capacitance and the electric charge between the conductor j and k, V_j is the electrostatic potential of the conductor j, and $V_0 = 0$ is the electrostatic potential of the ground. When we introduce

$$C_{jj} = \sum_{k=0,k\neq j}^{N} c_{jk}\,, \quad C_{jk} = C_{kj} = -c_{jk} \tag{2.3}$$

and

$$\vec{Q} = \begin{pmatrix} Q_0 \\ Q_1 \\ \vdots \\ Q_N \end{pmatrix}, \quad \vec{V} = \begin{pmatrix} V_0 \\ V_1 \\ \vdots \\ V_N \end{pmatrix}, \quad \mathbf{C} = \begin{pmatrix} C_{00} & C_{01} & \cdots & C_{0N} \\ C_{10} & C_{11} & \ldots & C_{1N} \\ C_{20} & \vdots & \ddots & \vdots \\ C_{N0} & C_{N1} & \cdots & C_{NN} \end{pmatrix} \tag{2.4}$$

, the equation (2.2) can be also expressed as

$$\vec{Q} = \mathbf{C}\vec{V} \tag{2.5}$$

using the capacitance matrix **C**.

The electrostatic energy U is the sum of energies charged in $N(N+1)/2$ of capacitances and can be expressed as

$$U = \frac{1}{2}\vec{V}\cdot\mathbf{C}\vec{V} = \frac{1}{2}\vec{V}\cdot\vec{Q} = \frac{1}{2}\vec{Q}\cdot\mathbf{C}^{-1}\vec{Q} \quad . \tag{2.6}$$

When a power supply is added as a node which has a capacitance C between ground and the power supply, then a sufficiently large electric charge Q is charged and the voltage of the power supply is $V = Q/C$. We define that the electric charge and voltage for the node of electric charge are Qc and Vc, and those for the node of the power supply are Qv and Vv, then we obtain

$$\begin{pmatrix}\vec{Q}_c\\ \vec{Q}_v\end{pmatrix} = \begin{pmatrix}\mathbf{C}_{CC} & \mathbf{C}_{CV}\\ \mathbf{C}_{VC} & \mathbf{C}_{VV}\end{pmatrix}\begin{pmatrix}\vec{V}_c\\ \vec{V}_v\end{pmatrix} \tag{2.7}$$

and

$$\vec{V}_c = \mathbf{C}_{CC}^{-1}(\vec{Q}_c - \mathbf{C}_{CV}\vec{V}_v)\,. \tag{2.8}$$

From these equations, we obtain the electrostatic energy

$$U = \frac{1}{2}\vec{V}_c\cdot\mathbf{C}_{CC}\vec{V}_c = \frac{1}{2}\vec{V}_c\cdot(\vec{Q}_c - \mathbf{C}_{CV}\vec{V}_v)\,. \tag{2.9}$$

2.2.2 Single electron tunneling and Coulomb blockade

We consider a potential barrier which has a capacitance C. Under the consideration of the classical physics electrons cannot tunnel the potential barrier and it behaves a capacitor. When a voltage V is applied to the capacitor, electric charge $Q = CV$ is charged and the electrostatic energy is $U = Q^2/2C$. When N electrons is charged ($Q = -Ne$ and $e = 1.6 \times 10^{-19}$) in the capacitor, the electrostatic energy $U(N)$ is given as

$$U(N) = \frac{(-Ne)^2}{2C} = N^2 \times \frac{e^2}{2C}. \tag{2.10}$$

On the other hand, under the consideration of quantum physics electrons can tunnel the potential barrier by tunnel probability Γ, which is called a tunnel junction. When an electron tunnels at the tunnel junction, the difference $\mu(N)$ in the electrostatic energy can be expressed as

$$\mu(N) = U(N) - U(N-1)$$

$$= (N^2 - (N-1)^2)\frac{e^2}{2C}$$

$$= (2N-1)\frac{e^2}{2C}. \tag{2.11}$$

$\mu(N)$ is called as the electrochemical potential which is corresponding to the energy to add an electron to the N-1 electron system. When the voltage V_{sd} of a power supply increase from 0 V, the current cannot flow through the tunnel junction on the case of $\mu_L < \mu(1)$, here $\mu_L = eV_{sd}$ is the electrochemical potential of the power supply which is connected the left-side electrode. Therefore we obtain the relationships

$$\mu_L < \mu(1) \quad \Leftrightarrow \quad |e|V_{sd} < \frac{e^2}{2C} \quad \Leftrightarrow \quad V_{sd} < \frac{e}{2C} \tag{2.12}$$

and the prohibition of the tunneling is called as Coulomb blockade.

On the other hand, when $V_{sd} > e/2C$ the tunneling through the tunnel junction occurs and currents can flow. Then we regard the tunnel junction as a resistance which has tunnel resistance value of RT. Figure 2.1 (a) shows the electrochemical potentials of the system. On the other hand, when $V_{sd} < 0$ we consider that power supply voltage $V'_{sd} = -V_{sd}$ is connected to the system (Fig. 2.1(b)). Then the condition to cause the Coulomb blockade is

$$\mu_R < \mu(1) \quad \Leftrightarrow \quad eV'_{sd} < \frac{e^2}{2C} \quad \Leftrightarrow \quad -eV_{sd} < \frac{e^2}{2C} \quad \Leftrightarrow \quad V_{sd} > -\frac{e}{2C} \quad .$$

(2.13)

Here μ_R is the electrochemical potential of the right-side electrode.
From equations (2.12) and (2.13), we obtain the condition of the Coulomb blockade as

$$-\frac{e}{2C} < V_{sd} < \frac{e}{2C} \quad . \tag{2.14}$$

The ideal characteristic of the Coulomb blockade is shown in figure 2.2(a). Here the width of the voltage between Coulomb peaks is called as the Coulomb gaps, and the tunnel junction and its equivalent circuit is shown in figure 2.2(b).
Here,

$$R(V) = \begin{cases} \infty & \left(|V_{sd}| < \frac{e}{2C} \right) \\ R_T & \left(|V_{sd}| \geq \frac{e}{2C} \right) \end{cases} \quad . \tag{2.15}$$

Observation of the Coulomb blockade in experiments required following conditions.

Fluctuation of the thermal energy
If the Fluctuation of the thermal energy k_BT (k_B : Boltzmann constant) is larger than the Coulomb gap $2\mu(1)$, the tunneling of electrons at the tunnel junction can occur even if the voltage between the source and drain is not applied, and then Coulomb blockade cannot be observed. Therefore the condition to observe the Coulomb blockade can be expressed as

$$2\mu(1) = \frac{e^2}{C} >> k_B T \quad . \tag{2.16}$$

At the room temperature (T = 300 K) the condition of capacitance C required for observation of

the Coulomb blockade is

$$C << \frac{e^2}{k_B T} \cong 6\,[aF] \quad . \tag{2.17}$$

To create the tiny capacitance a very fine construction of nanometer order is required. For example, in two parallel metallic plates which have distance of d = 1 nm between each plate, the area S of the plates require a condition

$$S << \frac{dC}{\varepsilon_0} \cong 25 \times 25[nm^2]\,. \tag{2.18}$$

Therefore to observe experimentally the Coulomb blockade fabrication of nanometer scale of construction and low temperature measurement techniques are essential.

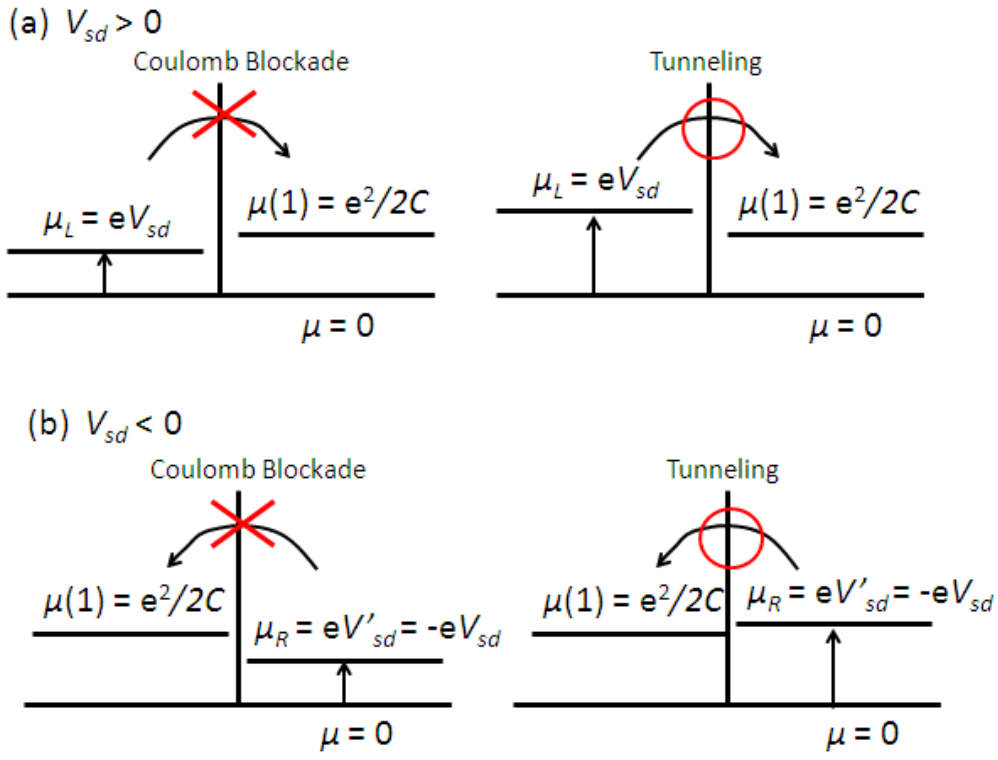


FIG. 2.1: Schematic of electrochemical potentials for the Coulomb blockade (a) $V_{sd} > 0$,(b) $V_{sd} < 0$, $Vsd = -V'sd$

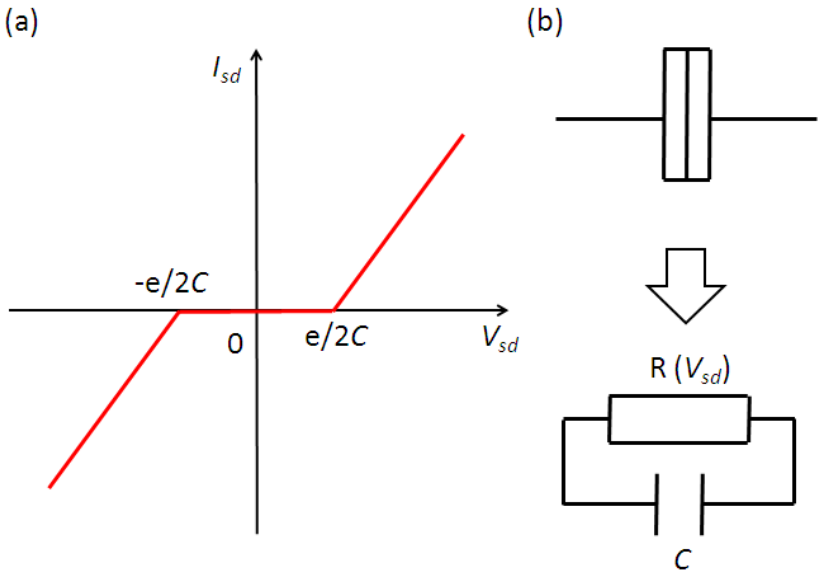


FIG. 2.2: (a) Ideal $I_{sd} - V_{sd}$ characteristic of the Coulomb blockade in a tunnel junction (b) Schematic of a tunnel junction and its equivalent circuit

Limitation for the tunnel resistance

For observation of the Coulomb blockade limitation for the tunnel resistance of the tunnel junction is

$$R_T >> R_K = \frac{h}{e^2} \cong 25.8[k\Omega] \tag{2.19}$$

R_K is called as the quantum resistance and it can be given from the uncertainty principle between energy and time, which is understood by following discussion: When a tunnel junction, which has capacitance C and tunnel resistance R_T, is expressed as a identical circuit, the time constant for relaxation by tunneling of electrons can be expressed as $\tau = CR_T$. Then the energy in the system has fluctuation of order of h/CR_T because of the uncertainty principle. In order to observe the Coulomb blockade the energy width of the Coulomb gap has to be much larger than the fluctuation;

$$\frac{h}{CR_T} << \frac{e^2}{C} \quad \Leftrightarrow \quad R_T >> \frac{h}{e^2} \tag{2.20}$$

Connection with the external environment

The tunnel junction has connection not only with the voltage power supply but also the external environment. We consider that an impedance of external environment is connected in series between the tunnel junction and the voltage power supply. From calculation of the current through the circuit by using the method of perturbation, we can understand that the relationship (2. 12) is valid only at low temperature and at which the impedance is much higher than the quantum resistance. Actually, achievement of these conditions is difficult in real experiment and it is difficult to observe expediently the Coulomb blockade in the single tunnel junction.

2.2.3 Single quantum dots

As discussed in preceding section, observation of the Coulomb blockade in the single tunnel junction because of the connection of the system with the external environment. However if we fabricate an island which is sandwiched by two tunnel junctions, the system has less connection with the external environment and then Coulomb blockade can be observed expediently. This system can be achieved by fabrication of a single quantum dot (QD) connected with a source and drain contact. The number of electrons confined in the single QD can be tuned by controlling the voltage of gate contact (Figure 2.3).

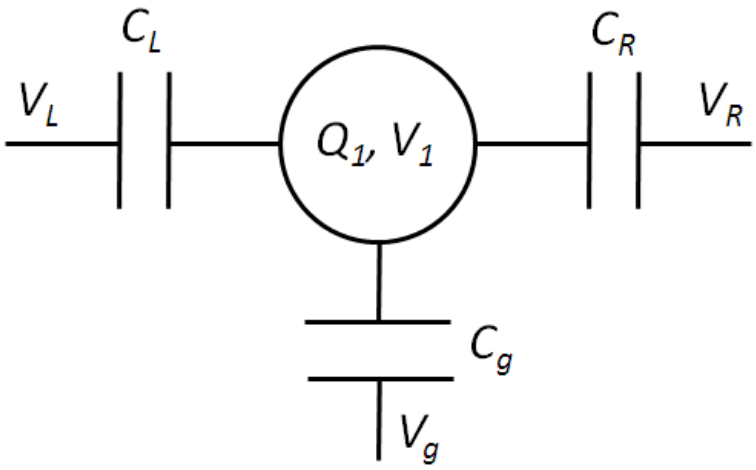


Fig. 2.3: Schematic diagram of a single quantum dot

The total charge of electrons confined in the single QD shown in figure 2.3 can be expressed as

$$Q_1 = C_L(V_1 - V_L) + C_R(V_1 - V_R) + C_g(V_1 - V_g) \quad \Leftrightarrow$$

$$Q_1 + C_L V_L + C_R V_R + C_g V_g = C_1 V_1 \tag{2.21}$$

Here $C_1 = C_L + C_R + C_g$ and $Q_1 = -(N_1 - N_0)e$ (N0 and N1 are the number of electrons in an initial state and a steady state, respectively). We define $E_{C1} = e^2/C_1$ and then the electrostatic energy $U(N_1)$ can be expressed as

$$U(N_1) = \frac{1}{2} V_1 \cdot C_1 V_1$$

$$= \frac{[-(N_1 - N_0)|e| + C_L V_L + C_R V_R + C_g V_g]^2}{2C_1}$$

$$= \frac{1}{2}(N_1 - N_0)^2 E_{C1}^2 - (N_1 - N_0)\left(\frac{C_L}{C_1} eV_L + \frac{C_R}{C_1} eV_R + \frac{C_g}{C_1} eV_g\right) + f(V_L, V_R, V_g)$$

(2.22)

Here,

$$f(V_L, V_R, V_g) = (C_L^2 V_L^2 + C_R^2 V_R^2 + C_g^2 V_g^2 + 2C_L C_R V_L V_R + 2C_L C_g V_L V_g + 2C_R C_g V_R V_g)/2C .$$

Then the electrochemical potential of the single QD $\mu(N_1)$ is given as

$$\mu(N_1) \equiv U(N_1) - U(N_1 - 1)$$

$$= \left(N_1 - N_0 - \frac{1}{2}\right) E_{C1} - \frac{C_L}{C_1} eV_L - \frac{C_R}{C_1} eV_R - \frac{C_g}{C_1} eV_g . \tag{2.23}$$

When V = $-V_{sd}$ and $V_R = 0$,

$$\mu(N_1) = \left(N_1 - N_0 - \frac{1}{2}\right) E_{C1} + \frac{C_L}{C_1} eV_{sd} - \frac{C_g}{C_1} eV_g . \tag{2.24}$$

The condition to occur the Coulomb blockade in the single QD can be given by comparing the electrochemical potential of the gate electrode and the single QD: Firstly we consider the case of $V_{sd} > 0$ in which the electrons tunnel from left to right side of the single QD. The condition to occur the Coulomb blockade at the left-side tunnel junction is given in the same way as discussed in preceding section,

$$\mu(N_1) > \mu_L \quad \Leftrightarrow$$

$$\left(N_1 - N_0 - \frac{1}{2}\right)E_{C1} + \frac{C_L}{C_1}eV_{sd} - \frac{C_g}{C_1}eV_g > eV_{sd} \quad \Leftrightarrow$$

$$V_{sd} < \frac{-C_g}{C_R + C_g}V_g + \left(N_1 - N_0 - \frac{1}{2}\right)\frac{e}{C_R + C_g} \tag{2.25}$$

Similarly, for the right-side tunnel junction, given as

$$\mu(N_1) < \mu_R \quad \Leftrightarrow$$

$$\left(N_1 - N_0 - \frac{1}{2}\right)E_{C1} + \frac{C_L}{C_1}eV_{sd} - \frac{C_g}{C_1}eV_g < 0 \quad \Leftrightarrow$$

$$V_{sd} < \frac{C_g}{C_L}V_g + \left(N_1 - N_0 - \frac{1}{2}\right)\frac{e}{C_L} \tag{2.26}$$

On the other hand, the condition of the coulomb blockade for $V_{sd} < 0$ can be given by inverting the sign of inequality in that for $V_{sd} > 0$. From the consideration of both cases of $V_{sd} > 0$ and $V_{sd} < 0$, schematic of the 'Coulomb diamond' is given, as shown in figure 2.4. The Coulomb blockade region with N electrons confined in the single QD is shown the region filled by grey color in figure 2.4. The conditions of the electrochemical potential for the regions represented from A to D in the schematic are also shown in figure 2.4.

For the case of $V_{sd} \approx 0$ the current through the QD has a characteristic of oscillation shown figure 2.5 and it is called as the 'Coulomb oscillation'. The conditions of the electrochemical potential for the Coulomb peaks and Coulomb blockade are also shown in figure 2.5. This single QD system is typically called as 'single electron transistor (SET)' because we can control the current by tuning a gate voltage by changing the number of electrons one by one. When we define the width of the gate voltage between Coulomb peaks for N_1 electron and $N_1 + 1$ electron as ΔV_g, the relationship with the electrochemical potentials is given as

$$\mu(N_1;V_g) = \mu(N_1+1;V_g+\Delta V_g) \quad \Leftrightarrow \quad \Delta V_g = \frac{e}{C_g} \tag{2.27}$$

The gate capacitance C_g can be estimated from the relationship (2. 27).

When both the source-drain voltage and the gate voltage are constant, the difference of electrochemical potentials for one electron can be given as

$$\mu(N_1+1) - \mu(N_1) = E_{C1} \tag{2.28}$$

E_{C1} and $\mu(N_1+1) - \mu(N_1)$ are called as the charging energy and addition energy respectively.

When there are two gate electrodes as shown in figure 2.6, $V_L = V_R \approx 0$, and $N_0 = 0$, the electrochemical potential $\mu(N_1)$ can be expressed as

$$\mu(N_1) = \left(N_1 - \frac{1}{2}\right)E_{C1} - \frac{C_{g1}}{C_1}eV_{g1} - \frac{C_{g2}}{C_1}eV_{g2}\,. \tag{2.29}$$

When $\mu(N_1) = 0$, the relationship between V_{g1} and V_{g2} can be given as

$$V_{g2} = -\frac{C_{g1}}{C_{g2}}V_{g1} + \left(N_1 - \frac{1}{2}\right)\frac{e}{C_{g2}}\,. \tag{2.30}$$

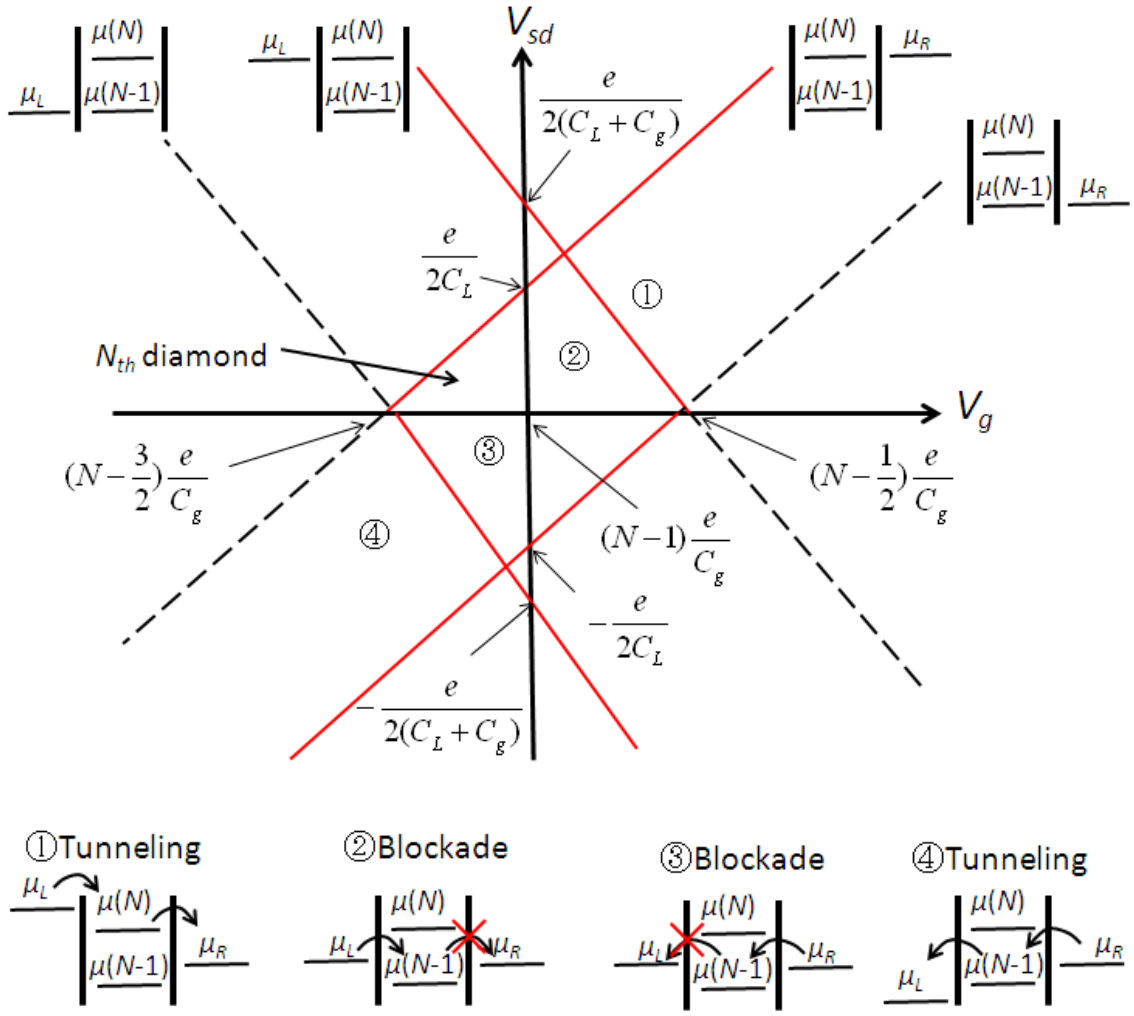


FIG. 2.4: Schematic diagram of the Coulomb diamond

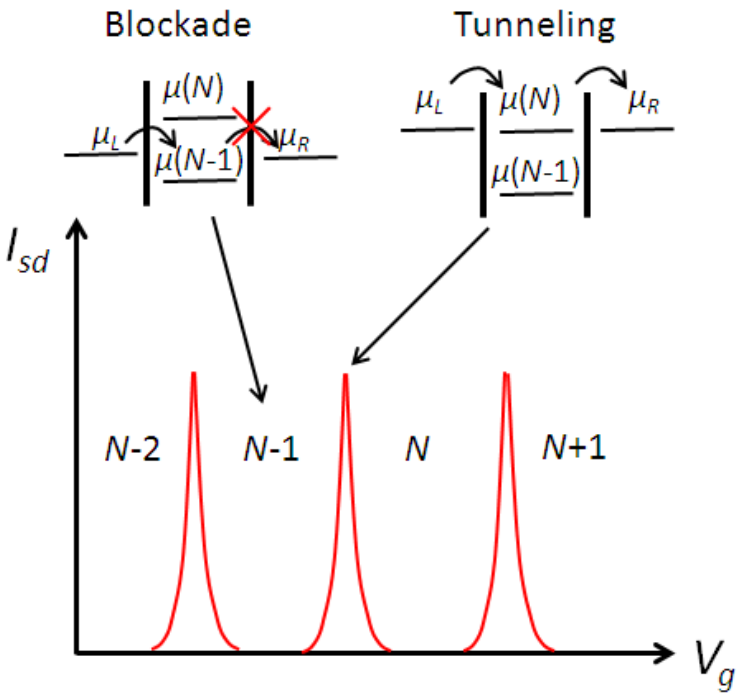


FIG. 2.5: Ideal characteristic of Coulomb oscillations

Figure 2.7 show the charge stability diagram for the single QD with two gate electrodes estimated from equation (2. 30). The integer values in the figure represent the number of electrons confined in the single QD and we can see that the charge stability diagram of the single QD have parallel Coulomb peaks. In the left-down region of the figure 2.7, there are no transitions of electrons through the QD, indicating the number of electrons in the QD is zero ($N = 0$). This low electron number region is called as few-electron regime of the QD.

Although we discussed above using the classical models, in the actual case the discretization of quantum energy states occurs in the nanometer order of the QD because the de Broglie wavelength is longer in semiconductors than in metals. By taking into account of the quantum energy states in the QD, the electrostatic energy $U(N_1)$ can be expressed as

$$U(N_1) = U^*(N_1) + \sum_{p=1}^{N_1} E_p \tag{2.31}$$

Here E_P is the energy of electrons to occupy quantum energy levels (For example, E_{N1} is the energy for the N_1-th electron) and $U^*(N_1)$ is the electrostatic energy given by using the classical

method.* Therefore the electrochemical potential $\mu(N_1)$ can be expressed as

*Here we use the one-body approximation for the confined electrons. In order to treat E_P and $U^*(N)$ more accurately, we have to take into account the many-body effect for it.

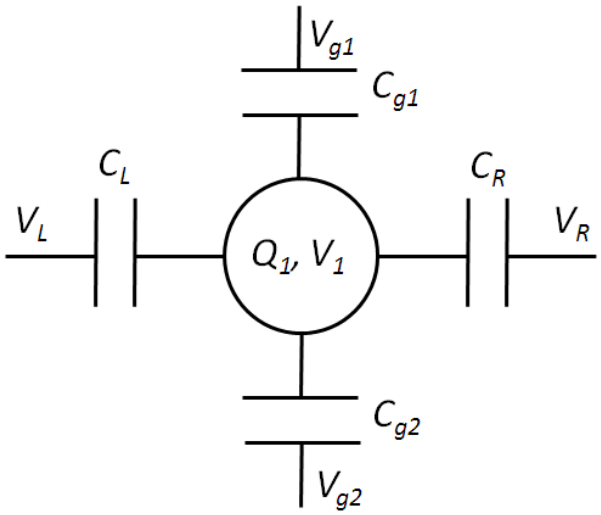


FIG. 2.6: Schematic diagram of a single quantum dot with two gate contacts

$$\begin{aligned}\mu(N_1) &= U(N_1) - U(N_1 - 1) \\ &= \mu(N_1) + E_{N_1}\end{aligned} \tag{2.32}$$

The addition energy is also given as

$$\begin{aligned}\mu(N_1 + 1) - \mu(N_1) &= E_{C1} + (E_{N_1+1} - E_{N_1}) \\ &= E_{C1} + \Delta E\end{aligned} \tag{2.33}$$

Here ΔE is the quantum energy level spacing. Then ΔV_g can be given from equations (2.23) and (2.32) as

$$\Delta V_g = \frac{e}{C_g} + \frac{C_1}{eC_g}\Delta E \tag{2.34}$$

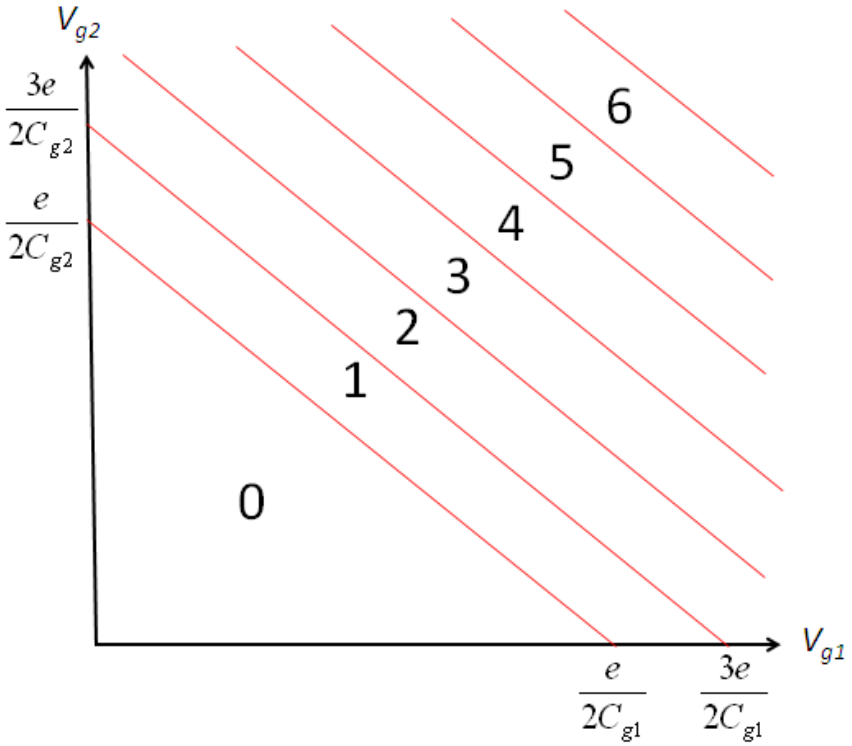


FIG. 2.7: Ideal charge stability diagram of a single quantum dot with two gate contacts. In the left-down region there are no electrons in the QD (N = 0).

If the thermal energy is sufficiently small ($k_BT << \Delta E$), the influence of the quantum energy levels appears obviously. Therefore then not only the ground states but also excited states can contribute to the current through the QD at the large source-drain voltage. Figure 2.8 depicts the Coulomb diamond by taking into account of the excited states. Figure 2.8(a) and 2.8(b) show the electrostatic energies and electrochemical potentials respectively in which we take account of the ground stats of GS(N) and GS($N+1$) ,and excited states of ES(N) and ES($N+1$). Here we consider the quantum level spacing between each state is not constant. When the current flows using the N+1-th electron, we consider the transitions of GS(N)↔GS(N+1), ES(N)↔GS(N+1), and GS(N)↔ES(N+1). Here we ignore the transition of ES(N)↔ES(N+1), which use two excited states, because that is relates tunnel rates at the tunnel junctions and relaxation times in the relaxation from the excited sates to the ground states and relatively complex.

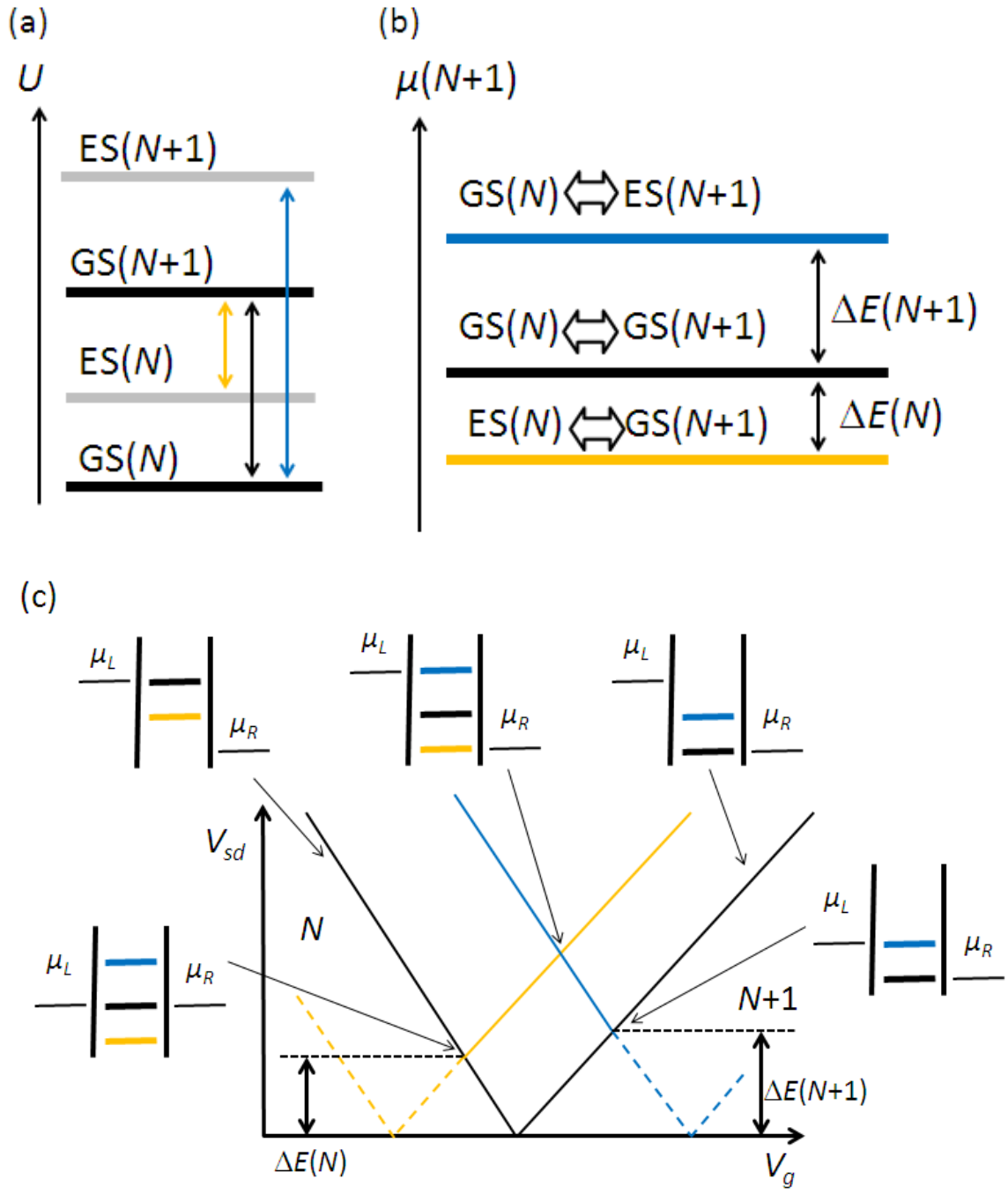


FIG. 2.8: Ideal characteristic of the Coulomb diamond with taking account of exited states

2.2.4 Double quantum dots

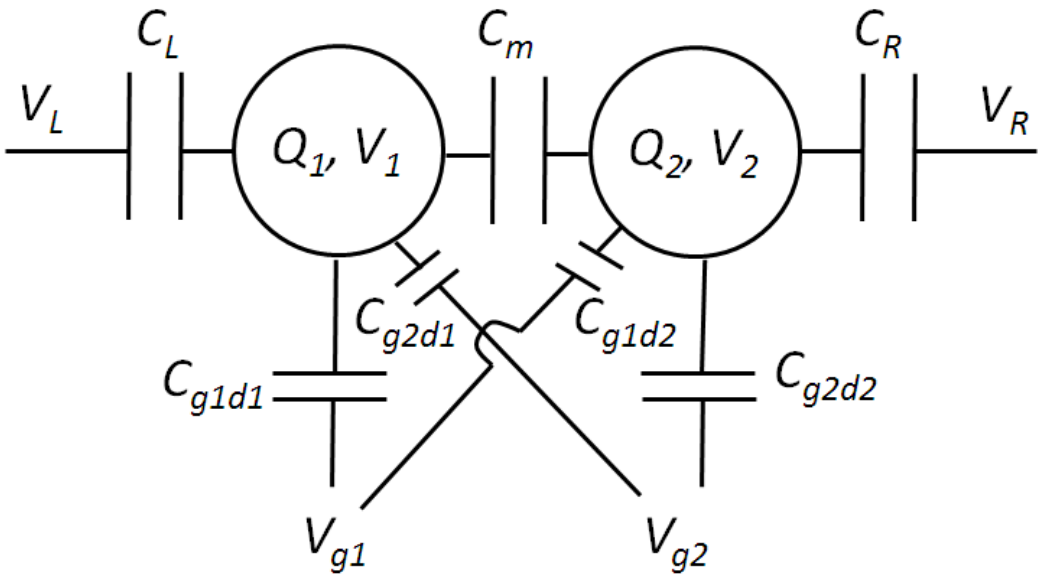


FIG. 2.9: Schematic diagram of a double quantum dot

In this section we discuss the electric transport property in a double QD connected in series with two gate electrodes (Figure 2.9). In this case we take account of the cross capacitive couplings (C_{g2d1} and C_{g1d2}) between the QDs and gate electrodes. The total charge of Q_1 and Q_2, which are accumulated in the right and left QD respectively, can be expressed as

$$Q_1 = C_L(V_1 - V_L) + C_m(V_1 - V_2) + C_{g1d1}(V_1 - V_{g1}) + C_{g2d1}(V_1 - V_{g2}) \qquad (2.35)$$

and

$$Q_2 = C_R(V_2 - V_R) + C_m(V_2 - V_1) + C_{g2d2}(V_2 - V_{g2}) + C_{g1d2}(V_2 - V_{g1}). \qquad (2.36)$$

When we define $C_1 = C_L + C_m + C_{g1d1} + C_{g2d1}$ and $C_2 = C_R + C_m + C_{g2d2} + C_{g1d2}$,

$$\begin{pmatrix} Q_1 + C_L V_L + C_{g1d1} V_{g1} + C_{g2d1} V_{g2} \\ Q_2 + C_R V_R + C_{g2d2} V_{g2} + C_{g1d2} V_{g1} \end{pmatrix} = \begin{pmatrix} C_1 & -C_m \\ -C_m & C_2 \end{pmatrix} \begin{pmatrix} V_1 \\ V_2 \end{pmatrix} \tag{2.37}$$

and

$$\begin{pmatrix} V_1 \\ V_2 \end{pmatrix} = \frac{1}{C_1 C_2 - C_m^2} \begin{pmatrix} C_1 & C_m \\ C_m & C_2 \end{pmatrix} \begin{pmatrix} Q_1 + C_L V_L + C_{g1d1} V_{g1} + C_{g2d1} V_{g2} \\ Q_2 + C_R V_R + C_{g2d2} V_{g2} + C_{g1d2} V_{g1} \end{pmatrix}$$

(2.38)

are given. Next we define $Q_{1(2)} = -N_{1(2)}e$ and calculate the electrostatic energy $U(N)$, then we can calculate the electrochemical potentials $\mu_{1(2)}(N_1,N_2)$ for the QD1(2) as

$$\begin{aligned} \mu_1(N_1, N_2) = &\left(N_1 - \frac{1}{2} \right) E_{C1} + N_2 E_{Cm} - \alpha \frac{C_L}{C_1} e V_L - \beta \frac{C_R}{C_m} e V_R \\ &- \left(\alpha \frac{C_{g1d1}}{C_1} + \beta \frac{C_{g1d2}}{C_m} \right) e V_{g1} - \left(\alpha \frac{C_{g2d1}}{C_1} + \beta \frac{C_{g2d2}}{C_m} \right) e V_{g2} \end{aligned} \tag{2.39}$$

and

$$\begin{aligned} \mu_2(N_1, N_2) = &\left(N_2 - \frac{1}{2} \right) E_{C2} + N_1 E_{Cm} - \alpha \frac{C_R}{C_2} e V_R - \beta \frac{C_L}{C_m} e V_L \\ &- \left(\alpha \frac{C_{g1d2}}{C_2} + \beta \frac{C_{g1d1}}{C_m} \right) e V_{g1} - \left(\alpha \frac{C_{g2d2}}{C_2} + \beta \frac{C_{g2d1}}{C_m} \right) e V_{g2} \end{aligned} \tag{2.40}$$

Here,

$$E_{C1} = \frac{e^2}{C_1} \left(\frac{1}{1 - \frac{C_m^2}{C_1 C_2}} \right) = \frac{e^2}{C_1} \alpha \,, \tag{2.41}$$

$$E_{C2} = \frac{e^2}{C_2}\left(\frac{1}{1-\frac{C_m^2}{C_1 C_2}}\right) = \frac{e^2}{C_2}\alpha \quad , \tag{2.42}$$

and

$$E_{Cm} = \frac{e^2}{C_m}\left(\frac{1}{\frac{C_1 C_2}{C_m^2}-1}\right) = \frac{e^2}{C_m}\beta = \frac{C_m}{C_1 C_2}e^2\alpha \tag{2.43}$$

$E_{C1(2)}$ is the charging energy for the QD1(2) and these equation have correction term α because of the capacitive coupling between the QD. E_{Cm} represents change in the electrochemical potential the QD when an electron is added in the other QD and $\mu_1(N_1,N_2+1) - \mu_1(N_1,N_2) = \mu_2(N_1+1,N_2) - \mu_2(N_1,N_2) = E_{Cm}$. The addition energy is $\mu_1(N_1+1,N_2) - \mu_1(N_1,N_2) = E_{C1}$ for the QD1, and $\mu_2(N_1,N_2+1) - \mu_2(N_1,N_2) = E_{C2}$ for the QD2.

Next we consider when $V_{L(R)} \approx 0$ and V_L is slightly larger than V_R. We define that $\mu_L = \mu_R = 0$ when no bias is applied to source and drain. Then the number of electrons confined in the QDs on the equilibrium state is natural numbers N_1 and N_2 in which $\mu_1(N_1,N_2) < 0$ and $\mu_2(N_1,N_2) < 0$ are fulfilled. Therefore the charge stability diagram of the double QD have on (V_{g1}, V_{g2}) plane honeycomb structure as shown in figure 2.10(b). Figure 2.10(a) depicts the charge stability diagram on the case of weak capacitive coupling limit ($C_m \rightarrow 0$). When the capacitive coupling between the QD becomes stronger, the vertex of the quadrangle becomes to be separated into two charge triple points (figure 2.10(b)). Figure 2.10(c) shows the charge stability diagram on the case of strong coupling limit ($C_m/C_{1(2)} \rightarrow 1$) , and then it behaves as same as a single QD which havs $N_1 + N_2$ electrons. The equations in the straight lines can be obtain from $\mu_1(N_1,N_2) = 0$ as

$$V_{g2} = \frac{\frac{C_2}{C_m}C_{g1d1} + C_{g1d2}}{C_{g2d2} + \frac{C_2}{C_m}C_{g2d1}}V_{g1} + \frac{\frac{C_2}{C_m}}{C_{g2d2} + \frac{C_2}{C_m}C_{g2d1}}\left(N_1 - \frac{1}{2}\right)e + \frac{1}{C_{g2d2} + \frac{C_2}{C_m}C_{g2d1}}N_2 e$$

(2.44)

and from $\mu_1(N_1,N_2) = 0$ as

$$V_{g2} = \frac{C_{g1d1} + \frac{C_1}{C_m} C_{g1d2}}{\frac{C_1}{C_m} C_{g2d2} + C_{g2d1}} V_{g1} + \frac{\frac{C_2}{C_m}}{\frac{C_1}{C_m} C_{g2d2} + C_{g2d1}} \left(N_2 - \frac{1}{2} \right) e + \frac{1}{\frac{C_1}{C_m} C_{g2d2} + C_{g2d1}} N_1 e \tag{2.45}$$

On the limit of $C_m \to 0$, the equations (2.44) and (2.45) can be expressed as

$$V_{g2} = -\frac{C_{g1d1}}{C_{g2d1}} V_{g1} + \frac{1}{C_{g2d1}} \left(N_1 - \frac{1}{2} \right) e \tag{2.46}$$

and

$$V_{g2} = -\frac{C_{g1d2}}{C_{g2d2}} V_{g1} + \frac{1}{C_{g2d2}} \left(N_2 - \frac{1}{2} \right) e \tag{2.47}$$

In this case the electrochemical potentials $\mu_{1(2)}(N_1,N_2)$ depend on the QD1(2) itself. On the other hand, on the limit of $C_m/C_{1(2)} \to 1$, the equations (2.44) and (2.45) can be expressed as

$$V_{g2} = -\frac{C_{g1d1} + C_{g1d2}}{C_{g2d2} + C_{g2d1}} V_{g1} + \frac{1}{C_{g2d2} + C_{g2d1}} \left(N_1 + N_2 - \frac{1}{2} \right) e \tag{2.48}$$

In this case we can regard the double QD as a single QD which has s $N_1 + N_2$ electrons (equation (2.30)).

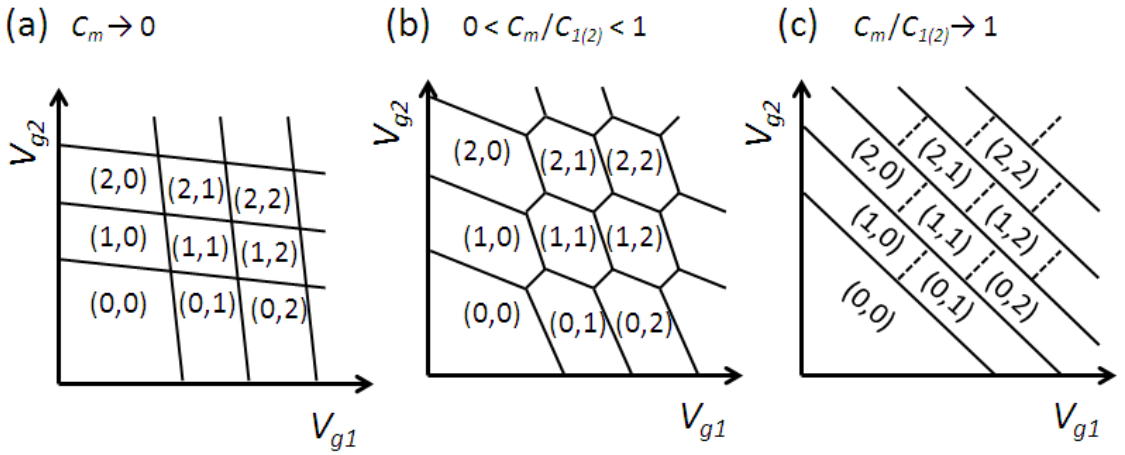


FIG. 2.10: Ideal charge stability diagram of a double quantum dot (a) Limit of capacitive coupling $C_m \to 0$ (Weak capacitive coupling) (b) Medium capacitive coupling (c) Limit of capacitive coupling $C_m / C_{1(2)} \to 1$ (Strong capacitive coupling)

Figure 2.11 depicts an enlarged view of the charge stability diagram in the medium capacitive coupling condition shown in figure 2.10(b). Typically the condition for generating current through the double QD is $\{\mu_L \geq \mu_1(N_1+1,N_2) \geq \mu_2(N_1,N_2+1) \geq \mu_R\}$, or $\{\mu_2(N_1,N_2+1) \geq \mu_R, \mu_L \geq \mu_1(N_1+1,N_2+1)$, and$\mu_1(N_1+1,N_2) \geq \mu_2(N_1,N_2+1)\}$. When $\mu_L = \mu_R = 0$, the current flows only under the condition in which the equality stands up. The black and white circle in figure 2.11 represent the triple points for $\{\mu_L = \mu_1(N_1+1,N_2) = \mu_2(N_1,N_2+1) = \mu_R\}$ and $\{\mu_2(N_1,N_2+1) = \mu_R, \mu_L = \mu_1(N_1+1,N_2+1)$, and $\mu_1(N_1+1,N_2) = \mu_2(N_1,N_2+1)\}$ respectively. On the case of the black circle, the charge states in the double QD transit in the order of (0, 0) →(1, 0)→(0, 1)→(0, 0) and electrons flow from the left-side electrode to the right-side electrode and we can interprets the transition as electron tunneling. On the other hand, on the case of the white circle, the charge states transit in the order of (1, 1)→(1, 0)→(0, 1)→(1, 1) and holes flow from the right-side electrode to the left-side electrode and we can interprets the transition as hole tunneling.

Next we calculate the coordinate points of the triple points to estimate capacitance parameters. From $\mu_1(N_1+1,N_2) = \mu_2(N_1,N_2+1)$, we obtain

$$V_{g1(2)}(N_1,N_2) = \frac{C_{g2(1)d2(1)}}{C_{g1d1}C_{g2d2} - C_{g1d2}C_{g2d1}} N_{1(2)}e - \frac{C_{g2(1)d1(2)}}{C_{g1d1}C_{g2d2} - C_{g1d2}C_{g2d1}} N_{2(1)}e + \frac{\left(1 - \frac{C_{2(1)}}{C_m}\right)C_{g2(1)d2(1)} - \frac{C_{2(1)}}{C_{1(2)}}\left(1 - \frac{C_{1(2)}}{C_m}\right)C_{g2(1)d1(2)}}{\left(\frac{C_m}{C_{1(2)}} - \frac{C_{2(1)}}{C_m}\right)(C_{g1d1}C_{g2d2} - C_{g1d2}C_{g2d1})} \frac{e}{2} \tag{2.49}$$

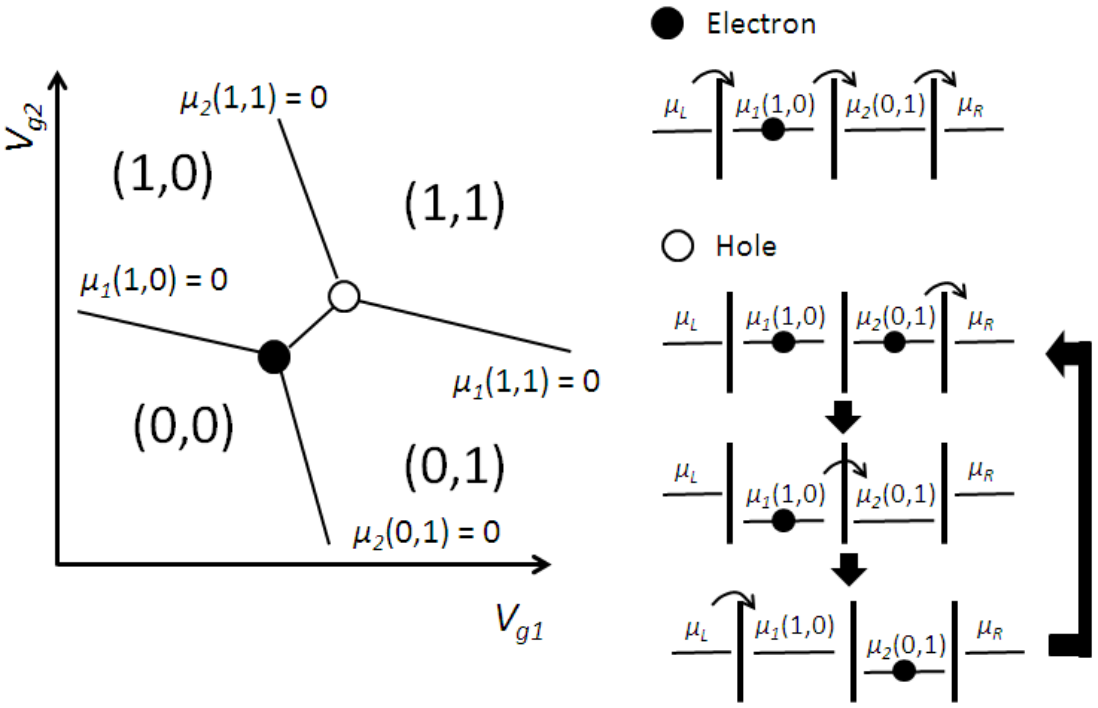


FIG. 2.11: Schematic diagram of transportation of electrons in the triple points

Here we define distance of the adjacent triple points as ΔV^d_{g1}, ΔV^g_{g1}, ΔV^d_{g2}, ΔV^g_{g2}, as shown in figure 2.12. We consider the typical condition $C_{g1(2)d1(2)} \geq C_{g1(2)d2(1)}$ and we use the equations

$$\Delta V^d_{g1} = V_{g1}(N_1+1, N_2) - V_{g1}(N_1, N_2), \tag{2.50}$$

$$\Delta V^g_{g1} = V_{g1}(N_1, N_2) - V_{g1}(N_1, N_2+1), \tag{2.51}$$

$$\Delta V^d_{g2} = V_{g2}(N_1, N_2+1) - V_{g1}(N_1, N_2), \tag{2.52}$$

and

$$\Delta V^g_{g2} = V_{g2}(N_1, N_2) - V_{g1}(N_1+1, N_2) \quad . \tag{2.53}$$

Then we obtain

$$C_{g1(2)d1(2)} = \frac{\Delta V^{d}_{g2(1)}}{\Delta V^{d}_{g1}\Delta V^{d}_{g2} - \Delta V^{g}_{g1}\Delta V^{g}_{g2}} \tag{2.54}$$

and

$$C_{g1(2)d2(1)} = \frac{\Delta V^{g}_{g2(1)}}{\Delta V^{d}_{g1}\Delta V^{d}_{g2} - \Delta V^{g}_{g1}\Delta V^{g}_{g2}} . \tag{2.55}$$

When ΔV^{m}_{g1} and ΔV^{m}_{g2} are used, we obtain

$$\mu_1(N_1, N_2; V_{g1}, V_{g2}) = \mu_1(N_1, N_2 + 1; V_{g1} + \Delta V^{m}_{g1}, V_{g2}) \tag{2.56}$$

and

$$\mu_1(N_1, N_2; V_{g1}, V_{g2}) = \mu_1(N_1 + 1, N_2; V_{g1}, V_{g2} + \Delta V^{m}_{g2}) \tag{2.57}$$

By solving these equations, we obrain

$$\frac{C_{1(2)}}{C_m} = \frac{e}{C_{g2(1)d2(1)}\Delta V^{m}_{g2(1)}} - \frac{C_{g2(1)d1(2)}}{C_{g2(1)d2(1)}} \tag{2.58}$$

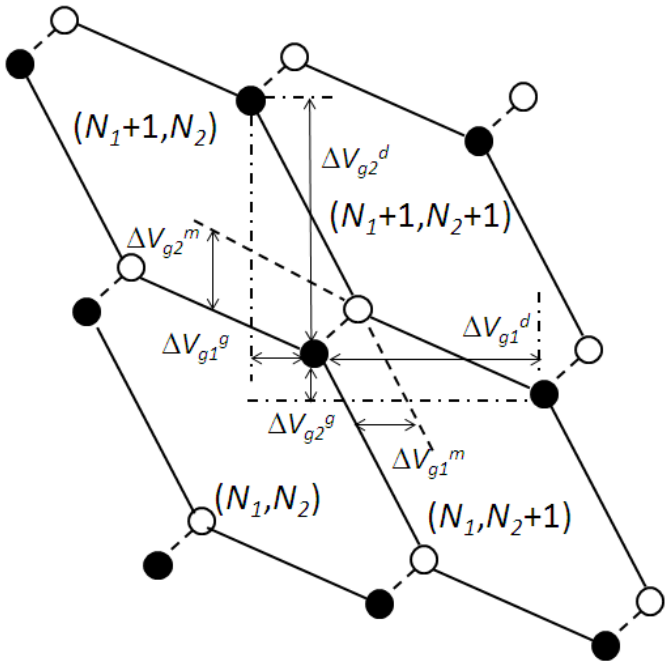


FIG. 2.12: Schematic of triple points in a charge stability diagram

Next we discuss the case of finite source-drain voltage. In this case the charge stability diagram is represented as shown in figure 2.13. Because V_{sd} is applied to the system, the aria of the region where the current can flow increase and the triple points become the triangle regions. From these triangles we can calculate the conversion factor to estimate the energy from the gate voltages. As shown in figure 2.13, the increase in the gate voltage $\delta V_{g1}(\delta V_{g2})$ for the triangle correspond to the energy for the source-drain bias. We define the conversion factor $\alpha_{1(2)}$, which convert the gate voltage to the energy, and then we obtain

$$\alpha_1 \delta V_{g1} = |eV| \tag{2.59}$$

and

$$\alpha_2 \delta V_{g2} = |eV| \tag{2.60}$$

By using the conversion factor we can estimate the charging energy or addition energy in the double QD from equations (2.39) and (2.40).

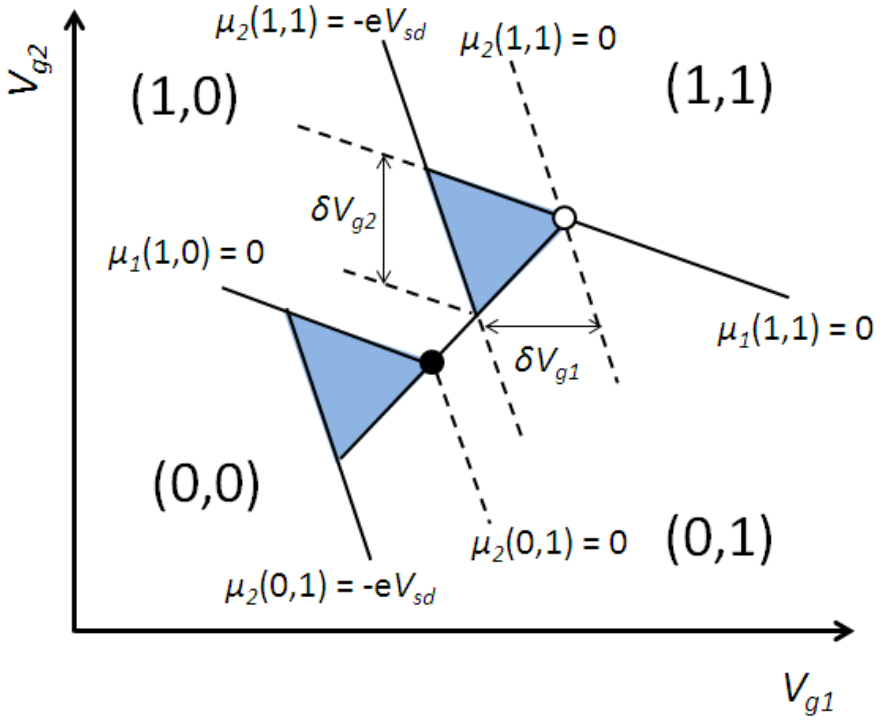


FIG. 2.13: Schematic of triple points on finite source-drain voltage

Next we discuss about tunnel coupling energy in a double QD system. Figure 2.14 shows schematic of triple points with finite tunnel coupling between QDs. The tunnel coupling between QDs generates anticrossing between the bonding and antibonding states in the energy versus detuning diagram. The tunnel coupling energy t_c can be estimated by bending of the charge transition lines reflected from the anticrossing in the double QD stability diagram. The voltage width, which is shown as by double-headed arrow indicated as t_c in figure 2.14, can be converted to energy by using conversion factor between energy and gate voltage mentioned above. Using the same methods the capacitive coupling energy E_m can be estimated by the separation between the two triple points as shown in figure 2.14. The askance axis in the figure called as ‘detuning’, which corresponds to the energy difference between ground states (GS) of each QD.

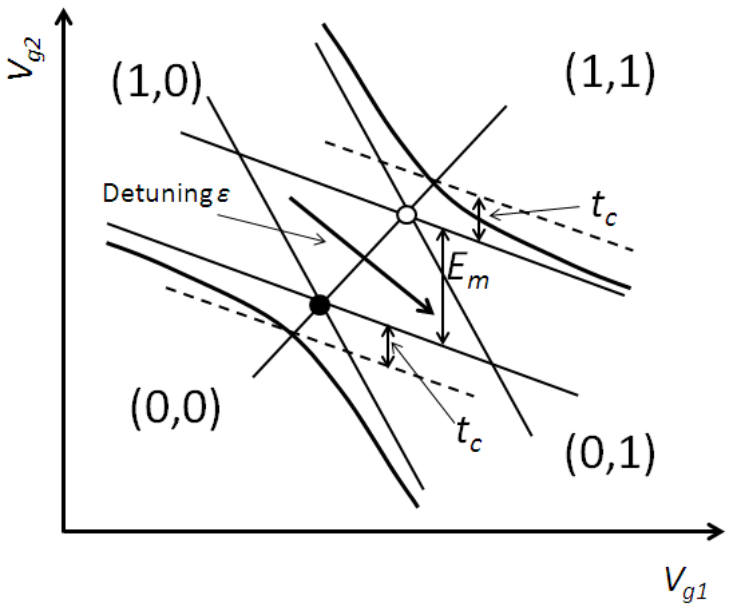


FIG. 2.14: Schematic of triple points with finite tunnel coupling between QDs

2.3 Theory for a single-electron transistor charge sensor

2.3.1 Signal-to-noise ratio

We consider periodic signals $V(t) = V(t + T)$. Here T is period of the signals. The amplitude of the signals, which can be obtained from Fourier transform of the time-dependent signal V(t), is in general a function of frequency. In addition to the amplitude, The root-mean square (rms) amplitude

$$V_{rms} = \sqrt{\frac{1}{T}\int_0^T V^2(t)dt} \tag{2.61}$$

is also used. Signals have the power P and $P = VI$ is valid for DC circuits. For the AC and RF circuits, the power P is expressed as

$$P = \frac{1}{T}\int_0^T V(t)I(t)dt. \tag{2.62}$$

We can compare two signal amplitudes. Alternatively we can also compare the signal and noise powers. The signal-to-noise ratio (SNR) can be expressed as

$$SNR = 20Log_{10}\frac{V_s}{V_n} = 10Log_{10}\frac{P_s}{P_n} \tag{2.63}$$

Here V_s and P_s are voltage and power for signals, and V_n and P_n are voltage and power for the noise. Because generally both signal and noise are dependent on the bandwidth ΔF of measurements, the SNR is also dependent on ΔF. The SNR for shot noise (here we chose Fano factor $\eta = 1$) can be expressed as

$$SNR = 10Log_{10}\frac{I_{rms}}{2e\Delta f} \tag{2.64}$$

Here I_{rms} is the rms current and the SNR becomes worse at lower currents. The smallest detectable signal can be obtained by the condition SNR $\geq$ 1 []. Shot noise configures the ultimate limit for the sensitivity of current driven sensors such as SETs.

2.3.2 Charge sensitivity of a single-electron transistor charge sensor

Using above-mentioned relationship, we define the charge sensitivity δq, which smaller limits of detectable charges by an SET charge sensor. The charge sensitivity δq can be expressed as

$$\delta q = \frac{\delta Q}{\sqrt{\Delta f}} = \sqrt{S_I}\left(\frac{\partial I}{\partial Q}\right)^{-1} \tag{2.65}$$

in units of $e/\sqrt{Hz}$. Here δQ is the rms noise amplitude in the system and S_I is the noise spectral density. The ultimate charge sensitivity of SETs can be estimated by assuming shot noise of the SET currents. $\partial I / \partial Q$ is the transconductance of SETs. Experimentally the charge sensitivity δq can be obtained from the measurement of SNR for an induced charge ΔQ according to

$$\delta q = \frac{\Delta Q}{\sqrt{B} \times 10^{SNR/20}} \tag{2.66}$$

and assuming white noise (shot noise).

2.3.3 Radio-frequency single electron transistor

The high sensitivity of SET charge sensors can be used to observe the signal near quantum-limitation. However the typical SET resistance of ≈100 kΩ and lead capacitance of ≈ 1 nF restrict the measurement bandwidth to a few kHz. This leads to a low operating speed and a 1/f noise can be influential. On the other hand measurements using the radio-frequency single electron transistor (RF-SET) has been realized high sensitivity of $0.9\times10^{-6}\ e/\sqrt{Hz}$ [112] and high measurement band width of more than 100 MHz [124]. In the RF-SET operation radio frequency waves are injected to the SET and reflected [124] and transmitted [114] wave are detected using LC-resonant circuit for impedance matching. Because of the remarkable advantages RF-SETs have been substituted to SETs in many measurements. Figure 2.15 shows the schematic of the reflection RF-SET measurement setups. The SET consists of two tunnel junctions with capacitances C_R and C_L and tunnel resistances R_R and R_L. The SET is coupled to a qubit confined in QDs with capacitance C_C. The RF carrier is injected to the SET through the coupled port of the directional coupler. The frequency of the charier is determined as resonant frequency of the RC-resonant circuit which consists of inductor L and parasitic capacitor C_S for the drain pad of the SET. The reflected signal from the SET passes through the through port of the directional coupler and is amplified by an amplifier.

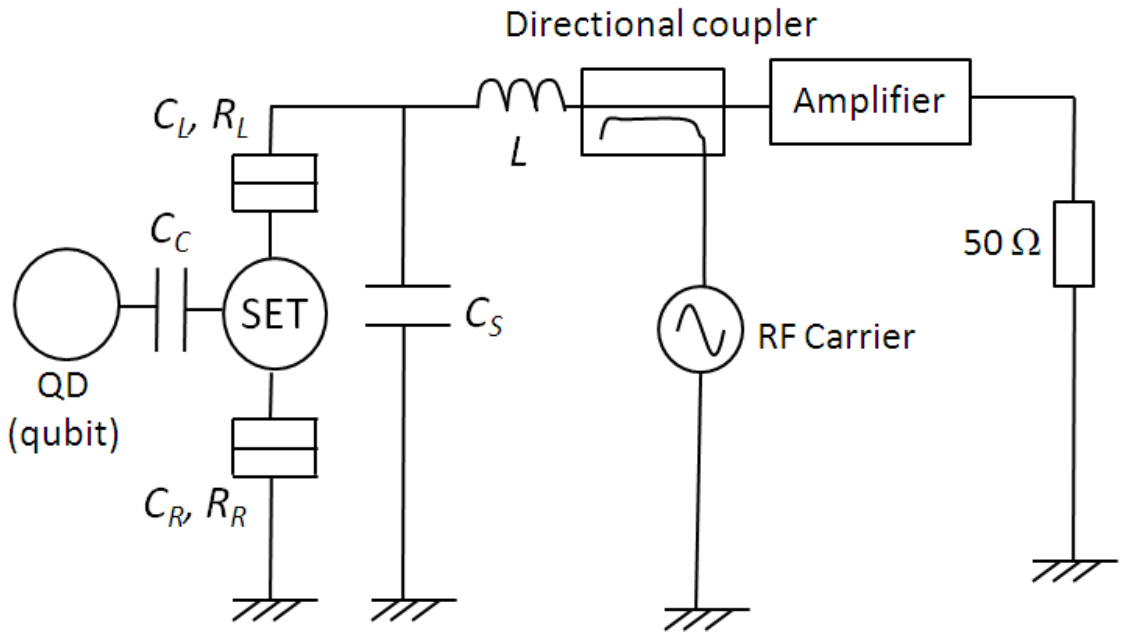


FIG. 2.15: Schematic of reflection RF-SET measurement setup

Chapter 3

Experimental Techniques

3.1 Introduction

In this chapter firstly we introduce our device structure and fabrication process. We use a silicon-on-insulator (SOI) substrate for fabricating device and we utilize metal-oxide-semiconductor substrate. The overall fabrication processes are same for all devices discussed in this work and fundamental fabrication processes are presented in this chapter. Fabrication of device has multi-step process. The major steps in silicon based device fabrication are oxidation, lithography, ion implantation and metallization.

3.2 Device structures

Figure 3.1(a) and 3.1(b) show a top-view scanning electron microscopy image of a single QD device and double QD device, and Fig. 3.2(c) shows a schematic cross section of the device structure. We use a silicon-on-insulator (SOI) wafer and QDs and side gates are formed in the SOI layer by using the electron beam lithography (EBL) and the reactive ion etching (RIE). The QDs and side gates are passivated by thermal oxidation and SiO_2 for a gate insulator is deposited by the low-pressure chemical viper deposition (LPCVD). The poly-Si top-gate, which is deposited by the LPCVD and formed by the plasma etching, is formed on the gate insulator. The device has a metal-oxide-semiconductor (MOS) structure and a two dimensional electron gas (2DEG) is induced near the SiO_2-Si interface by the electric field generated from the top-gate. The source and drain region is n-doped by using the ion implantation and the drive-in process. On the ion implantation the top-gate acts as a mask of the self-align process and therefore the QDs are in the non-doped region.

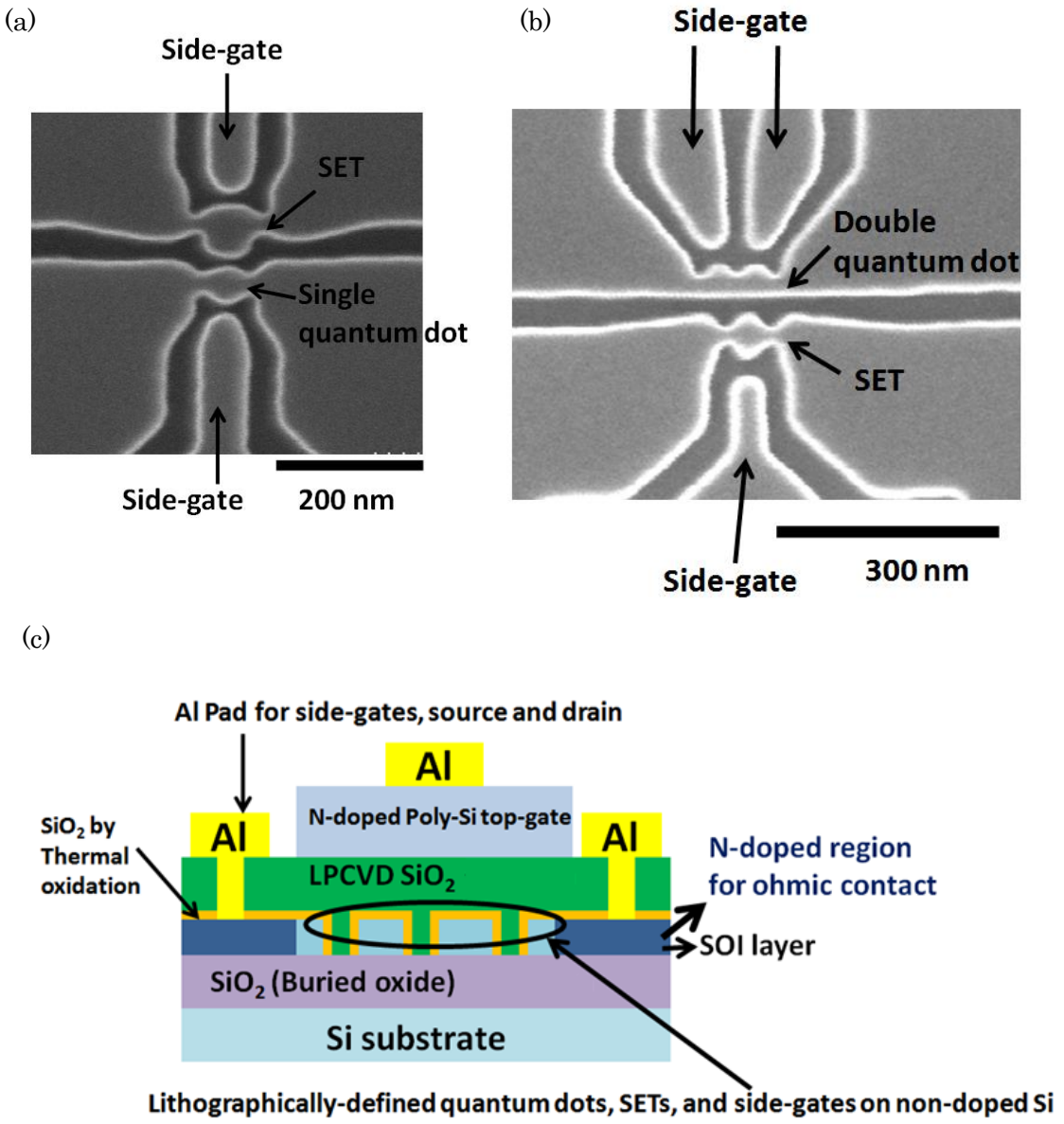


FIG. 3.1: (a) (b) Scanning micro scope image of (a) a single QD device and (b) a double QD device. (c) Schematic cross section of the device structure.

3.3 Fabrication process

Device is fabricated by thinning of the SOI layer, forming of the QDs and side gates using the EBL, passivation of the QDs, forming the top-gate contact, and forming the metal contact pads. In this section we introduce the details of the fabrication process.

- Wafer cleaning

On the fabrication process of the silicon device the cleanliness is extremely important. Therefore the wafer cleaning is performed after cutting the initial SOI wafer, and then the particle and impurities on the wafer is removed. The processes of the wafer cleaning are following.

① Cleaning with pure water using ultrasonic cleaner, 1 min
② Cleaning with SPM (H_2SO_4:H_2O_2 = 1:1), 100℃, 10 min (Removing the organic and metallic impurities)
③ Cleaning with pure water using ultrasonic cleaner, 1 min
④ Cleaning with 1.5% HF, 3 min (Removing the oxide and metal impurities)
⑤ Cleaning with pure water using ultrasonic cleaner, 1 min

- Thinning of the SOI layer

In order to observe the characteristic of the electric transportation and quantum effects, the substantial charging energy or the quantum orbital level spacing is required. Then the thinner SOI layer is advantageous because it has smaller total capacitance and stronger quantum confinement along the perpendicular direction. Another reason of the SOI thinning to for completely etch the SOI layer on the etching process of the SOI layer, because the etching resistance of the EB resist has limitation on the etching process.
In this work we use two types of SOI wafers; One is 100 nm of SOI layer and 200 nm of buried oxide (BOX) layer, and the other is 200 nm of SOI layer and 380 nm of BOX layer. In both cases the thickness of the SOI layer is adjusted to around 25～40 nm by repeating the thermal oxidation and HF etching. Before the thermal oxidation wafer cleaning is performed as the following process to reduce defects at the Si-SiO_2 interface.

1. Wafer cleaning
   ① Cleaning with pure water using ultrasonic cleaner, 1 min
   ② Cleaning with SPM (H_2SO_4:H_2O_2 = 1:1), 100℃, 10 min (Removing the organic and metallic impurities)
   ③ Cleaning with flowing pure water, 5 min
   ④ SC1（NH_3 : H_2O_2 : pure water＝1:5:25）150℃,10 min（Removing the organic impurities and silicon particles)
   ⑤ Cleaning with flowing pure water, 5 min
   ⑥ Cleaning with 1.5% HF, 3 min (Removing the oxide and metal impurities)
   ⑦ Cleaning with flowing pure water, 1 min
   ⑧ SC2（HCl : H_2O_2 : pure water=1:1:5）100℃,10min（(Removing the metal impurities）
   ⑨ Cleaning with flowing pure water, 5 min

2. Thermal oxidation for thinning the SOI layer

   - For the wafer with 100 nm SOI and 200 nm BOX

     ① Wafer cleaning
     ② Thermal oxidation 1100℃,35 min, about 82 nm of SiO_2 layer is formed
     ③ Removing the oxide by 1.5%HF, 30 min
     ④ Wafer cleaning
     ⑤ Thermal oxidation 1100℃,16～22 min, about 52～63 nm of SiO_2 layer is formed
     ⑥ Removing the oxide by 1.5%HF, 30 min, the SOI thickness is about 30～40 nm

   - For the wafer with 200 nm SOI and 380 nm BOX

     ① Wafer cleaning
     ② Thermal oxidation 1100℃,154 min, about 194 nm of SiO_2 layer is formed
     ③ Removing the oxide by 1.5%HF, 40 min
     ④ Wafer cleaning
     ⑤ Thermal oxidation 1100℃, 130 min, about 176 nm of SiO_2 layer is formed
     ⑥ Removing the oxide by 1.5%HF, 40 min, the SOI thickness is about 35～40 nm

- Forming the QD structure

The QDs, a proximal SET, and side gate structure are formed on the SOI layer by electron beam lithography (EBL) and reactive ion etching (RIE). The lithographically-defined constrictions in the silicon channel act as tunnel barriers for the QD and the SET, due to bandgap enlargement in the narrower regions26. The QD pattern shape and the distributions of topical exposure were optimized by adopting proximity-effect correction for the forward scattering in EBL to form smaller QDs. The exposures in the EBL are performed twice in which we use small current of 60 pA and large current of 7500 pA. The small current is used in the exposure of the fine pattern of nanometer scale and the large current is used in the exposure of large pattern such as device frames. Alignment on the between the two exposure is not performed because the misalignment is less than a few μm and does not have problem. On the device discussed in chapter 5 to 7, we add the thermal oxidation process prior to EBL to reduce electron-trapping defects at the Si/SiO_2 interface. After the SOI thinning the water is thermally oxidized at 900 °C for 5 min to create a 3 nm thick protective SiO_2 layer on the SOI surface before EBL. The thin SiO_2 layer protects the SOI surface from the EBL process and suppresses the formation of electron-trapping defects. We found this additional process results in the formation of clean Si/SiO_2 interfaces and consequently improves the properties of the QDs.

1. Thermal oxidation for forming protective SiO_2 layer on the SOI surface
   ① Wafer cleaning
   ② Thermal oxidation 900℃, 5 min, about 3 nm of SiO_2 layer is formed

2. Coating the EB resist on the wafer（ZEP520A:ZEP-A=1:3 with containing C^{60}）
   ① Drying the wafer by oven 170℃,10 min
   ② 1st spin coating 1000 rpm, 5 s
   ③ 2nd spin coating 3000rpm, 60 s
   ④ Pre-baking the EB resist by oven 170℃,10 min

3. Exposure in the EBL
   ① 1st（Fine patterns）: Current 60pA、accelerating voltage 50kV、exposure amount 400～600 $\mu C/cm^2$
   ② 2nd（Device frame patterns）: Current 4500pA、accelerating voltage 50kV、exposure amount 420 $\mu C/cm^2$

4. Development of the EB resist
   ① MIBK(Methyl IsoButyl Ketone)：IPA(IsoPropyl Alcohol) = 1 : 1（Development）1.5 min on resting state of the wafer
   ② IPA（Rinse）30 s on resting state

5. Reactive ion etching (Cl_2 etching or SF_6 etching)
   - Case of Cl_2 etching
     ① Cl_2 etching, 50 sccm (0.01 Torr), 50 W, 65 s
   - Case of SF_6 etching
     ② SF_6 etching, 10 sccm, 20 W, 75 s
     ③ O_2 aching, 20 sccm, 20 W, 10 s

6. Removing the EB resist
   ① H_2SO_4:H_2O_2=3:2, 10 min, with stirring the wafer
   ② H_2SO_4:H_2O_2=3:1, 10 min, with stirring the wafer
   ③ HF 1.5%, 20 s, removing the protective SiO_2 layer on the SOI surface

- Passivation of the QDs (at 900℃or 1000℃)
  - Case of 900℃
    ① Wafer cleaning
    ② Thermal oxidation 900℃, 5 min, about 3 nm of SiO_2 layer is formed
  - Case of 1000℃
    ① Wafer cleaning
    ② Thermal oxidation 1000℃, 5 min, about 11 nm of SiO_2 layer is formed

- Depositing SiO_2 for gate insulator by the low-pressure chemical viper deposition (LPCVD)

After the passivation process, the SiO_2 layer is deposited for the gate insulator by LPCVD. This gate insulator prevents the poly-Si top gate from sheltering the electric field between QDs and side gates.

① Cleaning with SPM (H_2SO_4:H_2O_2 = 1:1), 100℃, 10 min (Removing the organic and metallic impurities)
② Deposition of SiO2 by LPCVD 840℃, SiH_2Cl_2＋N_2O, about 50 nm of SiO_2 layer is deposited

- Forming the top gate (TG)

To forming the top gate, we deposit an amorphous-Si layer by the LPCVD. After the deposition top gate pattern is formed by using photolithography and plasma etching.

1. Deposition of the amorphous-Si layer by the LPCVD (Si_2H_6 0.3 sccm, PH_3 7 sccm, 500℃, 40min, the thickness is around 200 nm)

2. Coating the HMDS on the wafer
   ① Drying the wafer by oven 120℃,10 min
   ② 1st spin coating 1000 rpm, 5 s
   ③ 2nd spin coating 3000rpm, 60 s

3. Coating the S1818G (photo resist) on the wafer
   ① 1st spin coating 1000 rpm, 5 s
   ② 2nd spin coating 3000rpm, 60 s
   ③ Pre-baking of the photo resist by hot plate 110℃,1 min

4. Photolithography（exposure amount：130mJ）

5. Development of the photo resist
   ① MF320（Development）：90 s, with stirring the wafer
   ② Pure water（Rinse）：30 s, with stirring the wafer

7. Plasma etching (CF_4 100 sccm (max), O_2 10 sccm, 250 W, 2～3 min)

- Impurity doping

On low temperature measurements of devices, the ohmic contact is required to contact between the SOI layer and metal pads. To create the ohmic contact the impurity doping is performed on the SOI wafer by using ion implantation. Phosphine is used to implant the P+ ion to the wafer and then the SOI layer is n-doped. The depth of the injection of the ion is set to around the interface between Si and SiO_2, which is controlled by the accelerating voltage. The amorphous-Si top gate behaves as a mask to prevent the ion from injected to the QD region. After the ion implantation an annealing process (Drive-in process) is performed to revive the crustal lattice of the SOI layer and to inject the P+ ion the lattice point, which activate the conductivity of the SOI layer. This drive-in process behaves as the recrystallization of the amorphous-Si top gate.

① Ion implantation, phosphine, accelerating voltage 50 keV (Changed depending on the SiO_2 thickness)
② O_2 aching by plasma etcher, O_2 30 sccm, 250 W, 1 min
③ Removing the photo resist（Cleaning with SPM (H_2SO_4:H_2O_2 = 1:1), 100℃, 10 min）
④ Wafer cleaning
⑤ Drive-in, 1000℃, 30 min,

- Forming metal contact pads

On the low temperature measurement of devices the metal contact pad is required to create the ohmic contact (Figure 3.2(a) and 3.2(b)). The Al contact pads are formed by the photolithography, electron beam evaporator, and lift-off process

1. Coating the HMDS on the wafer
   ① Drying the wafer by oven 120℃,10 min
   ② 1st spin coating 1000 rpm, 5 s
   ③ 2nd spin coating 3000rpm, 60 s

2. Coating the S1818G (photo resist) on the wafer

① 1st spin coating 1000 rpm, 5 s
② 2nd spin coating 3000rpm, 60 s
③ Pre-baking of the photo resist by hot plate 110℃,1 min

3. Photolithography（exposure amount：130mJ）

4. Development of the photo resist
   ① Chlorobenzene (for curing the photo resist) : 2 min 15s, on resting state of the wafer
   ② MF320（Development）: 90 s, with stirring the wafer
   ③ Pure water（Rinse）: 30 s, with stirring the wafer
   ④ Post-baking of the photo resist by hot plate 120℃,3 min

5. Wet etching by Buffered Hydrogen Fluoride (BHF) to remove the SiO_2 on the region of contact pads, BHF 1 min 30 s

6. Deposition of Al by electron beam evaporator (Al 300 nm)

7. Lift-off : Acetone 24 hours, Acetone spray

8. Forming gas annealing (FGA) 10 min

- Device cutting and wire bonding

We fabricate 100 devices on a 2 cm×2 cm square wafer. Before measurement of the devices using cryostats, the wafer has to be cut to one by one device. We use two types of cryostats; One is Physical Property Measurement System (PPMS), which enable us to measure devices at base temperature of 4.2 K. This cryostat requires transfer of the liquid helium. The other is He^3 and He^4 cryostats, which enable us to measure devices at base temperature of 300 mK. This cryostat does not require the liquid helium transfer. To connect the device to these cryostats we put the sample on chip-carriers and perform wire bonding.

1. Coating PMMA (100 %) on the device surface to protect the device surface
   ① 1st spin coating 1000 rpm, 5 s
   ② 2nd spin coating 5000rpm, 30 s
   ③ Baking in oven by 120℃,1 hours

2. Scratching the device surface using a scriber

3. Cutting wafer with pushing the back side of the wafer by stweezers.

4. Forming gas annealing (FGA) 3 hours to reduce dangling bonds between Si/SiO_2 interface, which is discussed in chapter 4 in detail

5. Put the sample on chip-carrier by using silver paste (hot plate 120 ℃, 2 min)

6. Wire bonding between the contact pad of the device and contact pins of chip-carriers

7. Room temperature measurements for checking device

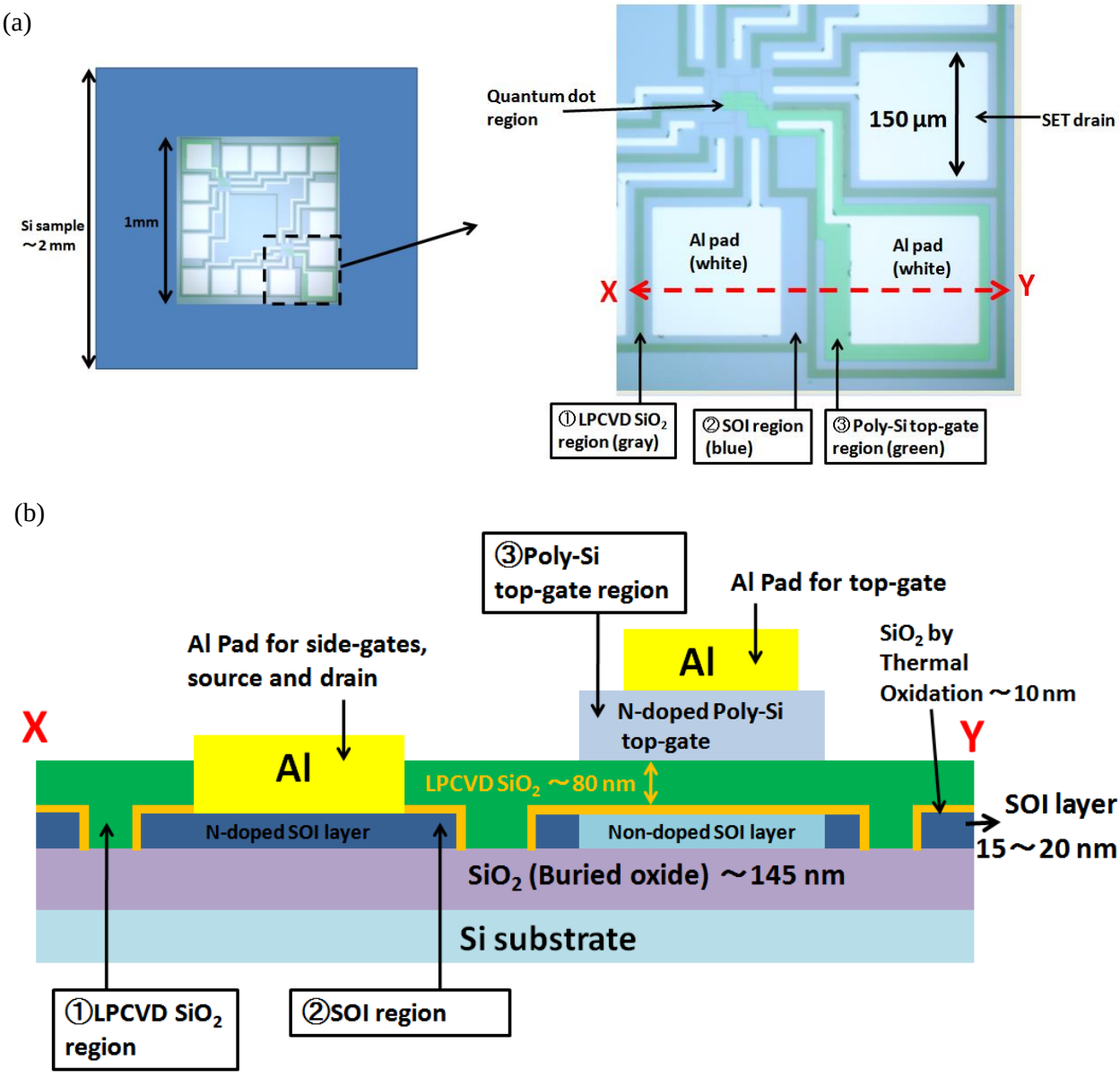


Fig. 3.2: (a)Schematic image of a sample and picture of a device (b)Schematic cross section of the device structure along the line XY in (a)

Chapter 4

Realization of charge sensing measurements and observation of few-electron silicon single and double quantum dots

4.1 Introduction

In this chapter we present realization of charge sensing measurements and observation of few-electron silicon and double QDs. As described in chapter 1, charge sensing measurement using a charge sensor is essential for achieving the measurements of spin states of electrons confined in QDs. Therefore to achieve the charge sensing measurements we fabricate silicon single QD device with an SET as a charge sensor. The electron occupancy of the single QD is clearly measured using charge sensing. This charge sensing measurements is achieved in lithographically-defined QD devices for the first time. We tried to observe few-electron regime of a single QD by using charge sensing. The 0, 1, and 2 electron occupancy of the single QD is clearly observed by the charge sensing measurement. We also succeed observation of few-electron regime in a double QD device in which such as (0,0), (1,0), (0,1), and (1,1) electron occupancy is clearly observed. The observation of few-electron regime in single and double QDs is also first time in our device structure. The electron occupancy in a single QD realized measured using an SET charge sensor and the few-electron regime in single and double

QDs is observed using charge sensing. The simplicity of the device structure reported here is a significant advantage for the integration of quantum logic gates and the fabrication process for this device is similar to conventional silicon device fabrication technologies such as the complimentary MOS (CMOS) process.

4.2 Device structure and measurements settings

Figure 4.1(a) shows a scanning electron microscopy (SEM) image of a single QD structure. The detail of the fabrication process is described in chapter 3. Therefore here we present only the entire flow of the device fabrication. We improved the device fabrication process reported in Refs. 37 and 38, by an additional thermal oxidation process prior to electron-beam lithography (EBL) to reduce electron-trapping defects at the Si/SiO_2 interface and for proximity-effect correction during EBL to produce smaller QD patterns. Figure 4.1(c) shows a schematic cross-section of the device structure. An SOI wafer with an SOI thickness of 30–40 nm, which is adjusted by thermal oxidation and HF etching, is also thermally oxidized at 900 °C for 5 min to create a 3 nm thick protective SiO_2 layer on the SOI surface before EBL. The thin SiO_2 layer protects the SOI surface from the EBL process and suppresses the formation of electron-trapping defects, which results in the formation of clean Si/SiO_2 interfaces and consequently improves the properties of the QDs. A single QD and a proximal SET were patterned on the SOI layer by EBL and reactive ion etching (RIE). The lithographically-defined constrictions in the silicon channel act as tunnel barriers for the QD and the SET, due to bandgap enlargement in the narrower regions [105]. The QD pattern shape and the distributions of topical exposure were optimized by adopting proximity-effect correction for the forward scattering in EBL to form smaller QDs. The SET is designed to be somewhat larger than the QD to prevent the SET being depleted at the few-electron regime of the QD. After RIE, the protective SiO_2 layer was removed by HF etching and thermal oxidation was performed at 1000 °C for 5 min to passivate the surface states of the SOI layer, which produced a final SOI thickness of 20–30 nm. To form a MOS structure, a SiO_2 gate insulator and an n-doped poly-Si layer were deposited by low-pressure chemical vapor deposition. The poly-Si layer is patterned to the TG shape and ion implantation is performed at the source-drain region of QDs using a self-alignment process. A two-dimensional electron gas (2DEG) is induced in the SOI layer near

the Si/SiO_2 interface by application of a positive voltage to the TG. Figure 4.1(b) shows an SEM image of a double QD (DQD) structure with an SET charge sensor. The DQD devices are fabricated in the same process with the single QD devices. In this chapter measurements for single QDs and double QDs are performed at base temperature of 4 K and 300 mK respectively. Current that flows through the QD (I_{QD}) and the SET (I_{SET}) are measured by connecting their drain contact to the source-measurement unit of a semiconductor device parameter analyzer. The side-gate voltages (V_{SG1} and V_{SG2}) are applied to control electrochemical potentials in the QD and the SET. The SET is used as a charge sensor to probe change in the number of electrons confined in the QD.

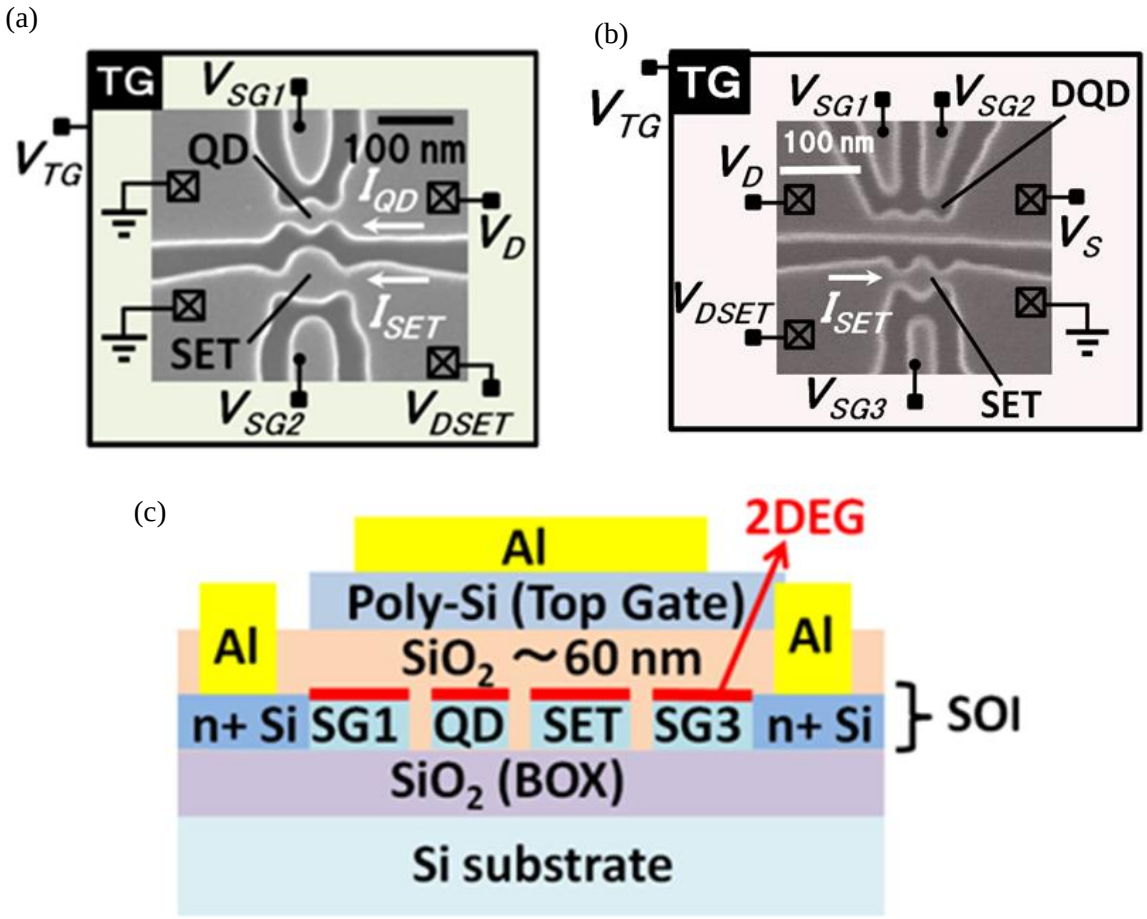


FIG. 4.1: (a) Scanning electron microscopy (SEM) image of a single QD device and and schematic measurement setups. (b) SEM image of a double QD (DQD) device and schematic measurement setups. DQD device is fabricated by the same process as that for the single QD device. Measurement of the single QD and DQD devices was performed at a base temperature of 4.2 K and 300 mK respectively. (c) Schematic cross section of the device structure.

4.3 Realization of charge sensing measurements

Figure 4.2(a) shows the current through the QD (IQD) and the SET (I_{SET}) as a function of the side-gate voltage V_{SG1}, which were measured simultaneously. Conventional periodic Coulomb peaks for the single QD system are observed in I_{QD} in which the electrochemical potential of the QD is varied by sweeping VSG1. The sharp Coulomb peaks are caused by resonance between the electrochemical potential of the QD and the Fermi energy in the source and drain contact of the QD. Sharp inflections are observed on the broad Coulomb oscillation of I_{SET} at the V_{SG1} position (indicated by red dashed lines in Fig. 4.2(a)) of the Coulomb peaks of IQD. This is because the stationary number of electrons (N) confined in the QD changes at the V_{SG1} position of the I_{QD} Coulomb peaks, which leads to a change in the electrochemical potential of the SET. Shifts of the Coulomb oscillation of I_{SET} on the V_{SG1} axis then occur, which results in the inflection observed for I_{SET} [65]. At the V_{SG1} position indicated by the green dashed lines in Fig. 5.2(a), although the tunnel rates in the tunnel barriers are so small that Coulomb peaks of IQD are not observed for such negative values of V_{SG1}, the charge transport can be observed from the sharp inflections in I_{SET}. This measurement showed the charge sensing for the transitions of N via the SET charge sensor.

4.4 Observation of few-electron regime in a silicon single quantum dot

In addition, observation of the few-electron occupancy in the QD was also achieved with application of a large negative V_{SG1}. Figures 4.2(b) and 4.2(c) show simultaneously measured plots of the QD current I_{QD}, and the SET transconductance dI_{SET}/dV_{SG1}, as functions of V_{SG1} and V_{SG2}, respectively, for another single QD sample. The clear lines in dI_{SET}/dV_{SG1} represent the change in the number of electrons confined in the QD and indicate no further transitions occur for $V_{SG1} < -4.7$ V; therefore, the QD contains no electrons below this gate voltage. This charge sensing measurement thus enables the accurate number of electrons in the QD to be determined as $N = 0$, 1, and 2 charge occupancy. Although the transition line between $N = 0$ and $N = 1$ is clearly visible in the SET dI_{SET}/dV_{SG1} data of Fig. 4.2(b), no Coulomb peak corresponding to this transition in I_{QD} is evident in Fig. 4.2(c), because the tunneling rates between the QD and the leads are too small to observe a current though the QD for this transition, which is discussed in chapter 6.

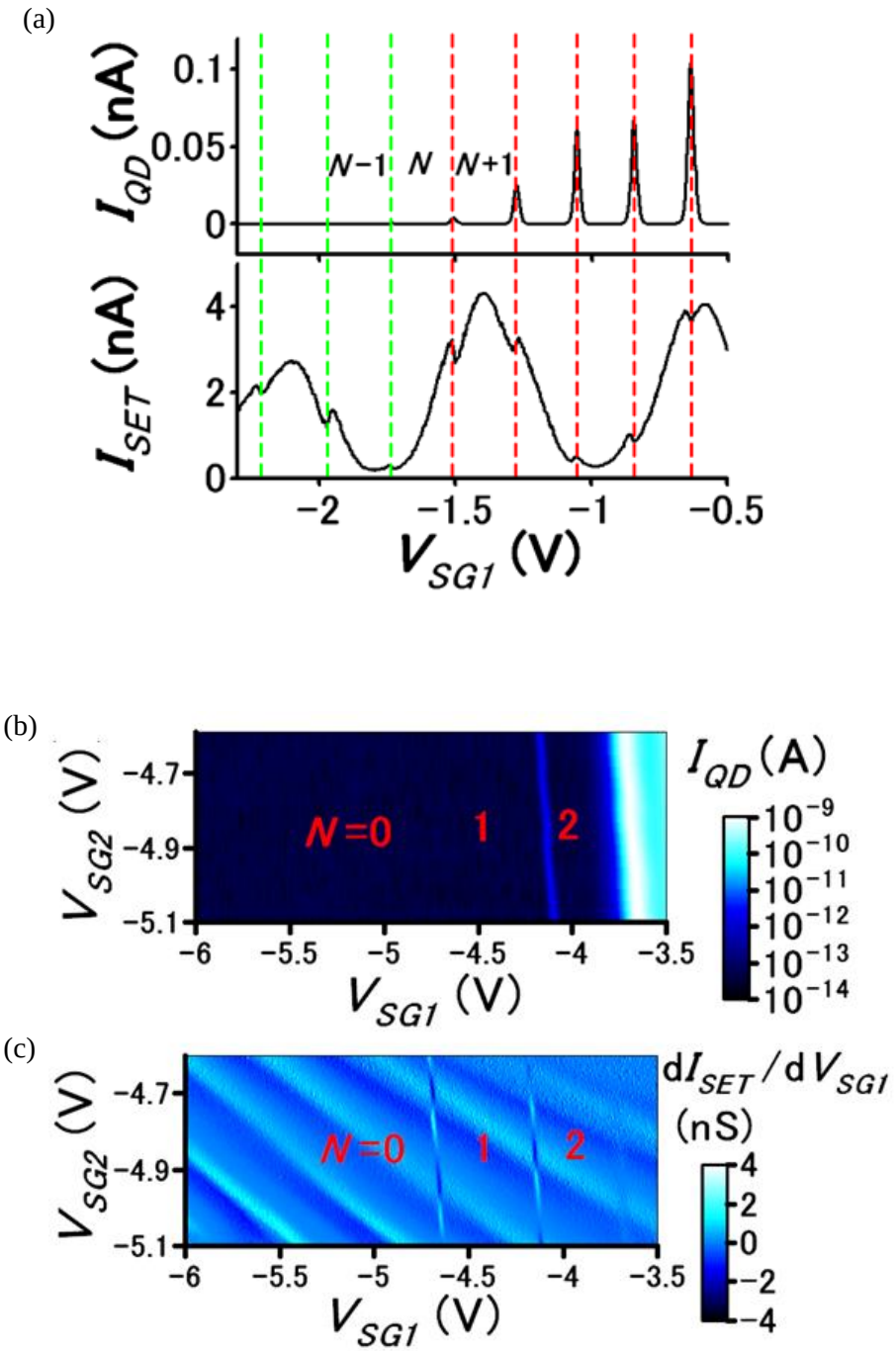


FIG. 4.2: (a) Current through the QD (I_{QD}) and the SET (I_{SET}) as a function of the side-gate voltage V_{SG1}; V_D = 0.3 mV, V_{DSET} = 6 mV, V_{TG} = 5.414 V, and V_{SG2} = -4 V. Red and green dashed lines indicate fixed values of V_{SG1}, which represent different amounts of electrons in the QD, where red represents Coulomb peaks and green represent no Coloumb peaks. (b,c) Plots of (b) I_{QD} and (c) the SET transconductance dI_{SET}/dV_{SG1} as functions of V_{SG1} and V_{SG2}, measured simultaneously; V_D = 1 mV, V_{DSET} = 5 mV, and V_{TG} = 3.8 V.

4.5 Observation of few-electron regime in a silicon double quantum dot

Figure 4.3(a) shows the plot of the SET transconductance dI_{SET}/dV_{SG1}, as functions of the side-gate voltage V_{SG1} and V_{SG2}. Figure 4.3 (b) shows a schematic diagram of ideal charge stability diagram for few-electron DQDs. In figure 4.3(a), the charge stability diagram for the DQD is obtained from charge transition lines of the charge sensing, where the few-electron regime of the DQD is clearly evident. The thick (broad) oscillations on the background of the figure 4.3 (a) are Coulomb oscillations of the SET itself. Typically the current which flows through the DQD is observable at charge triple point in the charge stability diagram []. However we cannot observe the DQD current because the resistance of the tunnel barriers in the QDQ is too high in this few-electron regime. Therefore we cannot estimate the conversion factor between energy and gate voltage in a DQD system (described in chapter 2) in this sample. The charging energy, tunnel coupling, and capacitive coupling for few-electron DQDs are estimated in another DQD sample and they are discussed in chapter 6 in detail.

Typically, it is more difficult to form few-electron regime if the number of coupled QD is increased, for example single QDs to double QDs because the device structure becomes more complex and requires higher reliability of the device pattern and cleanliness of surface states in material interfaces. To observe the few-electron regime it is essential to keep the tunnel coupling at all the tunnel barriers. In our lithographically-defined device, it is relatively difficult to conserve the tunnel coupling when the large negative voltage is applied to side-gates because the tunnel coupling greatly depends on width of the lithographically-defined construction region at the tunnel barriers. In the chapter 6 we tried to control the tunnel coupling by tuning the top gate voltage V_{TG}. Another important issue for the device is traps at the Si/SiO_2 interface. Generally the Si/SiO_2 interface has dangling bond, which is an unsatisfied valence on an immobilized atom. One unsatisfied valence can trap one electron and in the low temperature measurements it causes unexpected potential fluctuations near the QDs and also cause the random telegraph noise (RTN) [106]. Therefore it is important to reduce the dangling bond and traps at the at the Si/SiO_2 interface for observation of few-electron QDs and creation of electron spin qubits. To reduce the traps we add additional thermal oxidation before EBL mentioned above. We also adopt extension of the operation time for the forming gas annealing (FGA) before measurement of the device from 10 min to 3 hours before measurement of the device. We expect the long time FGA causes the hydrogen-termination of the dangling bonds at the Si/SiO_2

interface and traps reduce. Actuary before adoption of these improvements we could observe the few-electron DQD at less than 1 device among 10 devices. On the other hand after adoption of the improvements we could observe the few-electron DQD at around 5 devices among 10 devices. This results show the improvements in the fabrication can reduce the traps at the Si/SiO_2 interface.

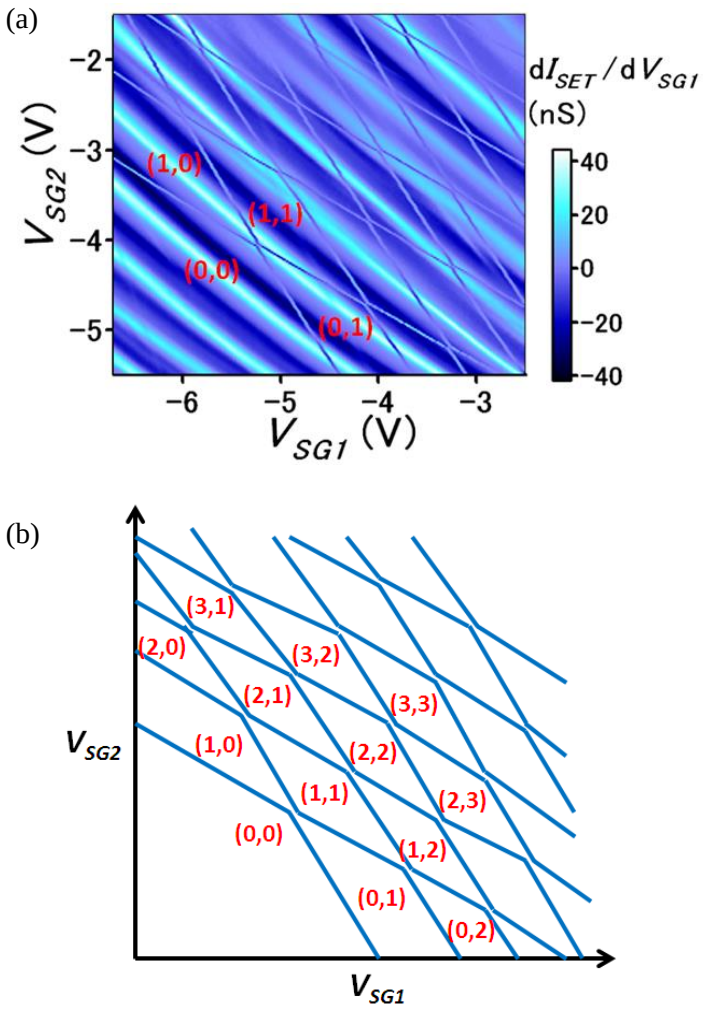


FIG. 4.3: (a) Transconductance of the SET charge sensor dI_{SET}/dV_{SG1}, as functions of V_{SG1} and V_{SG2} in a DQD sample; V_{TG} = 5.8 V and V_{SG3} = 0 V, $V_D = V_S$ = 0.9 V, and V_{DSET} = 3 mV. A charge stability diagram of the few-electron regime in the DQD is clearly obtained. (b) Schematic of ideal charge stability diagram for few-electron double QDs.

4.6 Summary

In summary, we have reported fabrication of QD device with a SET charge sensor and charge sensing measurements. Charge sensing was clearly observed at a single QD with a SET charge sensor. Improvement in our device fabrication process reduced the traps at the Si/SiO_2 interface and realized measurements of the few-electron regime of single QD and double QD devices using charge sensing measurements. Operation of the exchange-only qubit [33,34], which is expected as a powerful architecture for the qubit integration, requires coupled triple QD structure and therefore formation of few-electron triple QD in silicon devices is an important issue. This device structure reported here is close to that of conventional CMOS structures and has a very high potential for integration because confinement gates are not required. The will become a more significant advantage for practical application with expansion to more complicated structures.

Chapter 5

Key capacitive parameters for designing single-electron transistor charge sensors

5.1 Introduction

As described in chapter 1, Single electron transistors (SETs) have strong charge sensitivity and therefore it has been used as charge sensors for reading out spin or charge qubits. The charge sensitivity of SETs has been investigated theoretically [102, 103, 104, 107, 108] and experimentally [109, 110, 111, 112, 113, 114, 115] to evaluate their effectiveness as charge sensors for dc or radio frequency (RF) measurements. However, the SNR during qubit readout, which determines the effectiveness of the SET charge sensor, depends not only on the charge sensitivity of the SET itself but also on the capacitive coupling between the QDs and the SET. [113, 116. 117] Since both of these factors depend in turn on the configuration of the SET, e.g., its dimensions and distance from the QD, it is necessary to take this into consideration when designing an effective SET charge sensor.

In this chapter we present investigation of key capacitive parameters in SET charge sensors to find out good design guides to increase signal-to-noise ratio (SNR) in qubit measurements. We fabricate silicon single QD device to investigate the dependence of the charge sensitivity and capacitive coupling on the SET configuration, a lithographic process was used to fabricate twin silicon single QDs. The QDs have different diameters and either can act as an SET charge sensor. The physical dimensions of the QDs and their spacing could be directly measured using

scanning electron microscopy, and these values are valid in the many-electron regime. This information could then be used to calculate the theoretical electrostatic coupling between the QDs, which could then be compared to the experimentally determined value. We estimated the difference in the charge sensitivities of the two QDs from their charging energies, and identified the key capacitive parameter that determines the SNR. In addition, using another device in which the smaller QD was in the few-electron regime, we measured the electrostatic coupling between the QDs and observed its enhancement as the number of electrons decreased. Finally, we performed numerical calculations to estimate the dependence of the SNR in RF single-shot measurements on the SET diameter and the distance between the qubit and the SET.

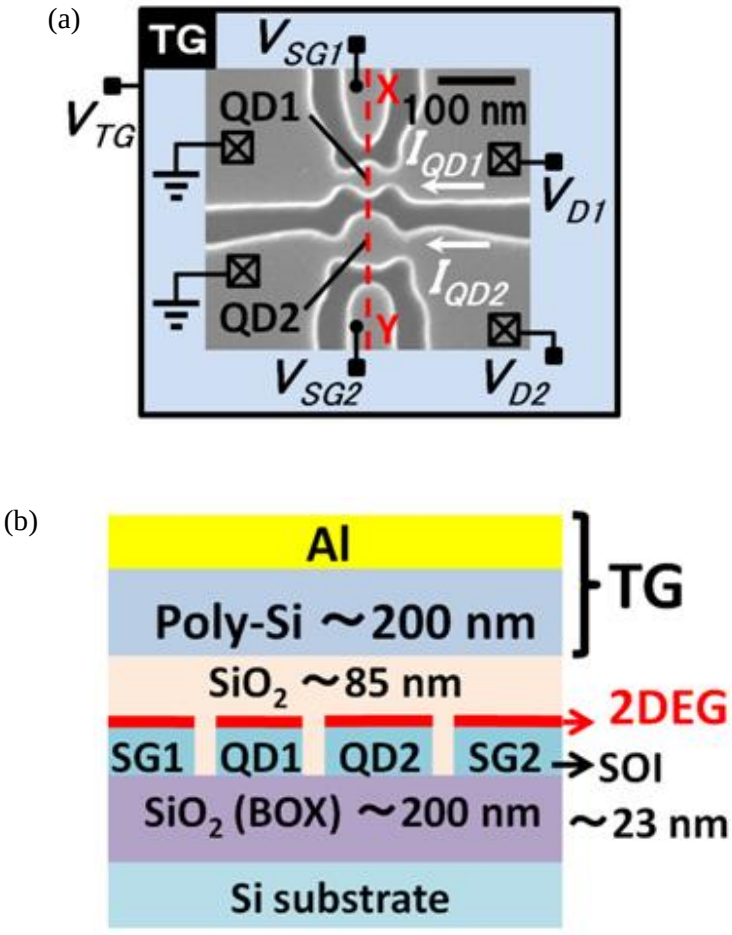


FIG. 5.1: (a) Scanning electron microscopy image of the device and with the measurement setup indicated. (b) Schematic cross section of the device structure along the line XY in (a).

5.2 Device structure and measurement settings

Figure 5.1(a) shows a top-view scanning electron microscopy image of the device with the measurement setup indicated, and Fig. 5.1(b) shows a schematic cross section of the device structure. The device fabrication process is the same as that described in chapter 3 and chapter 4. The small and large single QDs (labeled QD1 and QD2, respectively) were patterned in the Si layer by electron beam lithography and reactive ion etching. All measurements in this chapter were performed at a temperature of 4.2 K.

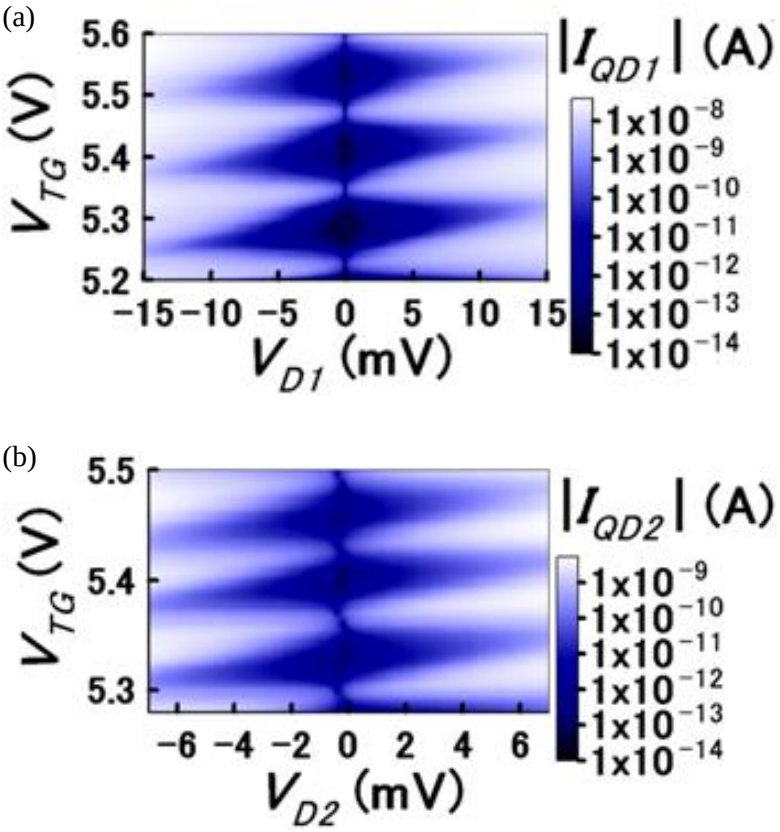


FIG. 5.2: (a) (b) Stability diagrams for QD1 and QD2, respectively. (a) V_{SG1} =0 V and V_{SG2} = − 4 V, (b) V_{SG1} =0 V and V_{SG2} = − 4 V. From the observed Coulomb diamonds, a charging energy of E_{QD1} ≈14.0 meV for QD1 and E_{QD2} ≈6.2 meV for QD2 was obtained.

5.3 Measurement of capacitive parameters of SET charge sensors

Stability diagrams for QD1 and the QD2 are shown in Fig. 5.2(a) and 5.2(b), respectively. The appearance of regular Coulomb diamonds indicates the presence of single QDs. From the observed Coulomb diamonds, we obtain a charging energy of E_{QD1} ≈14.0 meV for QD1 and E_{QD2} ≈6.2 meV for QD2. Figures 5.3(a) and 5.3(b) respectively show plots of the QD1 current I_{QD1} and the QD2 current I_{QD2} as functions of V_{TG} and the side gate voltage V_{SG1}, which were measured simultaneously. The Coulomb peaks in Fig. 5.3(b) for I_{QD2} have a zigzag structure with shifts at identical bias positions as the Coulomb peaks of I_{QD1}. This result indicates the QD2 behaves as a charge sensor to probe change in the number of electrons confined in QD1. Similarly, in Fig. 5.3(a), the Coulomb peaks for I_{QD1} are shifted at identical bias positions as the Coulomb peaks of I_{QD2}. This result indicates the QD1 also behaves as a charge sensor to probe change in the number of electrons confined in QD2. Figure 5.4(a) shows a schematic drawing of the twin single QD structure with the various electrical parameters indicated. The electrochemical potential of an N-electron QD1 (μ_{QD1}) and an n-electron QD2 (μ_{QD2}) can be expressed as

$$\mu_{QD1}(N,n) = \frac{E_{QD1}}{e}\left(Ne - \frac{e}{2} - C_{L1}V_{L1} - C_{R1}V_{R1} - \sum_i C_iV_i\right) + \frac{E_{QD1}}{e}k_{QD1}\left(ne - C_{L2}V_{L2} - C_{R2}V_{R2} - \sum_j C_jV_j\right) + E_N \quad (5.1)$$

$$\mu_{QD2}(N,n) = \frac{E_{QD2}}{e}\left(ne - \frac{e}{2} - C_{L2}V_{L2} - C_{R2}V_{R2} - \sum_j C_jV_j\right) + \frac{E_{QD2}}{e}k_{QD2}\left(Ne - C_{L1}V_{L1} - C_{R1}V_{R1} - \sum_i C_iV_i\right) + E_n \quad (5.2)$$

Here, $C_{QD1}=C_C+C_{L1}+C_{R1}+\Sigma C_i$ and $C_{QD2}=C_C+C_{L2}+C_{R2}+\Sigma C_j$ are the total capacitances of QD1 and QD2, respectively, and C_i (C_j) are the capacitances between QD1 (QD2) and other gates or environments for voltages V_i (V_j). E_N and E_n are the energies of the topmost filled single-particle states for QD1 and QD2, respectively. $E_{QD1}=\alpha e^2/C_{QD1}$ and $E_{QD2}=\alpha e^2/C_{QD2}$ are the charging

energies of QD1 and QD2 respectively, where $\alpha=(1-C_C^2/C_{QD1}C_{QD2})^{-1}$. Eq. (1) and (2) are equivalent to the electrochemical potentials of two QDs coupled in series as described in Ref. 85, except that there is no tunnel coupling between the parallel QDs here. $ek_{QD2}=eC_C/C_{QD1}$ is equivalent to the charge induced in QD2 when the number of electrons in QD1 decreases from N to N–1. Similarly, $ek_{QD1}=eC_C/C_{QD2}$ represents the charge induced in QD1 when the number of electrons in QD2 decreases from n to n–1. At the Coulomb peaks of I_{QD2} in Fig. 5.3(b), the value S_{QD2} is defined, which is the ratio of the peak shift magnitude to the peak-to-peak spacing in V_{TG}. It can be expressed as $S_{QD2}=k_{QD2}(1+\Delta E_n/E_{QD2})^{-1}$, where $\Delta E_n=E_n-E_{n-1}$. A value of $k_{QD2}=S_{QD2}=0.088\pm0.005$ is obtained from Fig. 5.3(b) because ΔE_n is negligibly small in the large n regime. Similarly, $k_{QD1}=S_{QD1}=0.038\pm0.003$ is obtained from Fig. 5.3(a), where $S_{QD1}=k_{QD1}(1+\Delta E_N/E_{QD1})^{-1}$ is identical to k_{QD1} because of the large value of N. k_{QD2} is larger than k_{QD1} because the QD2 diameter L_{QD2} (≈70 nm) is larger than the QD1 diameter L_{QD1} (≈35 nm).

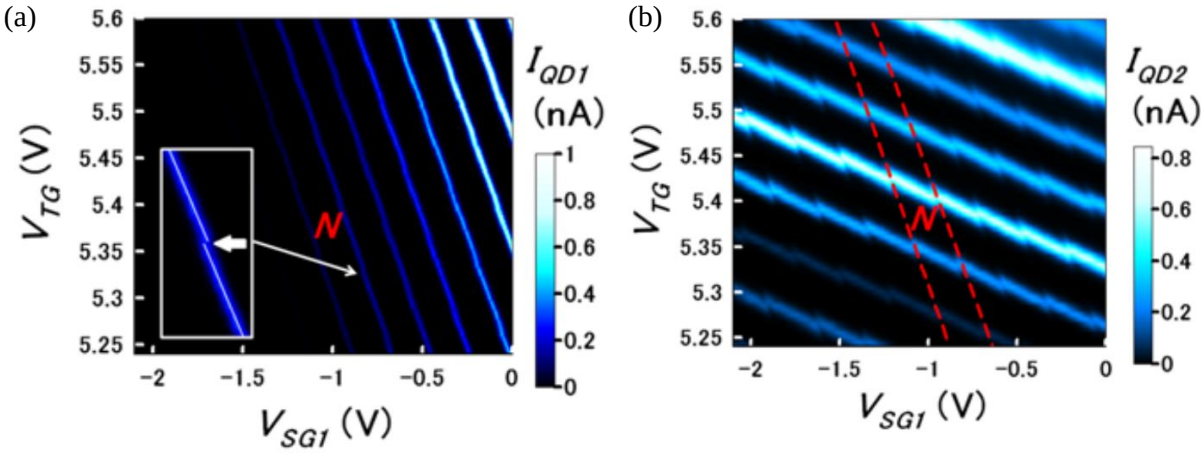


FIG. 5.3: (a) (b) Plots of (a) I_{QD1} and (b) I_{QD2} as functions of V_{TG} and V_{SG1}. V_{D1} = 1 mV, V_{D2} = 1 mV, and V_{SG2} = –4 V. The two red dashed lines in (b) show the positions of two Coulomb peaks in (a). (inset) Higher magnification view of a shift of a Coulomb peak. The solid white lines are visual guides. Actually similar shifts occur at all the crossing point between the Coulomb peaks of QD1 and QD2 though it is very tiny and not easy to see.

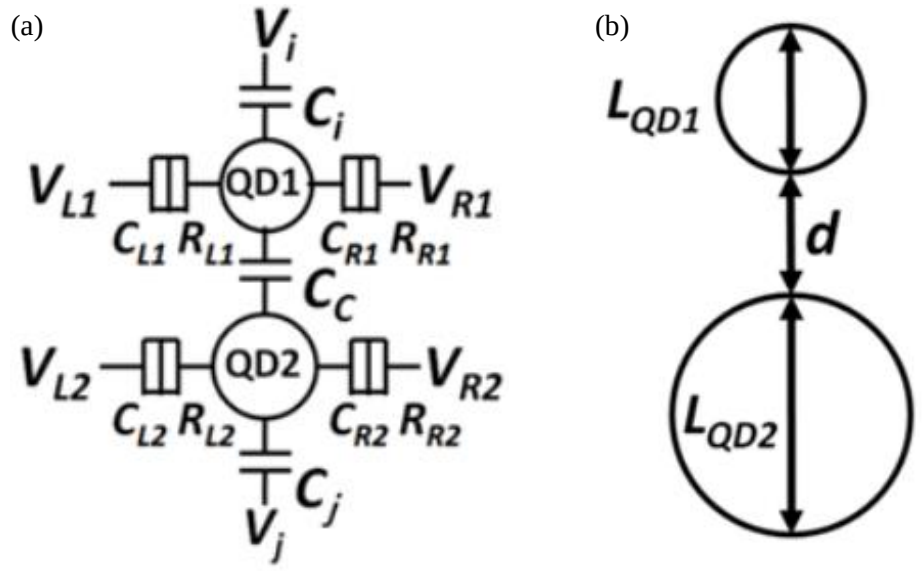


FIG. 5.4: (a) Schematic diagram of QD1 and QD2 and various electrical parameters. (b) Schematic diagram of twin QDs for numerical calculations.

5.4 Numerical calculation for capacitive parameters of SET charge sensors and the signal-to-noise ratio in DC measurements

To numerically calculate k_{QD1} and k_{QD2} as functions of L_{QD2}, it is assumed that QD1 and QD2 correspond to two-dimensional conductive disks, that the distance d between their edges is constant, and that L_{QD1} is also constant (see Fig. 5.4(b)). The real situation of the systems has capacitive coupling between the QDs and leads (source and drain regions of the QDs), or other gate contacts. We used approximation that affect of these capacitive couplings to the total capacitance of the QDs are small and does not influence it. We also use approximation that the two-dimensional electron gas (2DEG) is confined near the Si/SiO_2 interface by z-direction electric fields and adequately thin, and that affect of the SOI region under the 2DEG to the coupling capacitance C_C is small. 5.5(a) shows the calculation results obtained using the three-dimensional Poisson equation. The results indicate that increasing L_{QD2} causes k_{QD2} to increase and k_{QD1} to decrease, and that both k_{QD2} and k_{QD1} are larger for $d = 0.5L_{QD1}$ than for $d = L_{QD1}$. Using the measured device parameters (L_{QD1}≈35 nm, L_{SET1}≈70 nm, and d≈25 nm) the calculations give k_{QD2}=0.086 and k_{QD1}=0.036. These are very similar to the measured values,

which confirm the validity of the calculation method. These calculation results are valid even if materials surrounding the two QDs have variation of the dielectric constant in vertical directions, and are thus adaptable to other 2DEG systems such as GaAs/AlGaAs and Si/SiGe heterostructures.

To examine the charge sensitivity of the QDs when used as SET charge sensors, the SET current I_{SET} and the low-frequency spectral density of the SET shot noise S_I were calculated using the master equations [107, 118, 119, 120] for charge states corresponding to *N-1* (*n*–1) and *N* (*n*) excess electrons in QD1 (QD2). Assuming $R_{L(R)} \gg R_Q = \pi\hbar/2e^2$ and the quasistationary condition $\omega \ll I_{SET}/e$, [103, 104, 108, 118] we obtain

$$I_{SET} = e\frac{\Gamma_{L-}\Gamma_{R+} - \Gamma_{L+}\Gamma_{R-}}{\Gamma_+ + \Gamma_-} \tag{5. 3}$$

$$S_I = 2e^2 \frac{\sum_{\pm} \Gamma_{\pm}^2 \left(2\Gamma_{L\mp}\Gamma_{R\mp} + \Gamma_{L\mp}\Gamma_{R\pm} + \Gamma_{L\pm}\Gamma_{R\mp}\right)}{\left(\Gamma_+ + \Gamma_-\right)^3} \tag{5. 4}$$

Here, the electron tunneling rates are $\Gamma_{L(R)\pm} = (1/e^2 R_{L(R)})\gamma(\pm[-eV_{L(R)} - \mu_{SET}(N, n)])$, $\Gamma_+ = \Gamma_{L+} + \Gamma_{R+}$, $\Gamma_- = \Gamma_{L-} + \Gamma_{R-}$, $\gamma(\varepsilon) = \varepsilon/[1 - \exp(-\varepsilon/k_B T)]$ (see Ref. 28), and the electrochemical potential of the SET $\mu_{SET}(N, n)$ is identical to that given in Eq. (1) for QD1 and Eq. (2) for QD2. For the case of dc measurements, the charge sensitivity δq is given by $\delta q = (S_I)^{-1/2}/(\partial I_{SET}/\partial Q)$, [102, 121] where Q is the gate charge in the SET and can be expressed as $\Sigma C_i V_i$ ($\Sigma C_j V_j$) in Eq. (1) or (2). From these equations, we find that if QD1 and QD2 have the same resistance conditions (i.e., the same parasitic and tunnel resistances: $R_{L1} = R_{L2}$ and $R_{R1} = R_{R2}$) the charge sensitivities δq_1 and δq_2 are inversely proportional to E_{QD1} and E_{QD2}, respectively. Therefore, the charging energy E_{QD1} and E_{QD2} are key capacitive parameters for determining δq, and here $\delta q_2/\delta q_1 = E_{QD1}/E_{QD2}$. From the Coulomb diamonds shown in Fig. 5.2(a) and (b), a value of $E_{QD1}/E_{QD2} \approx 2.26$ is obtained, which is not very different to the numerically calculated value of 2.38 from Fig. 5.5(a). The difference between E_{QD1} and E_{QD2} is related to the QD diameters and this result indicates that a smaller QD is a more sensitive SET charge sensor. It should be emphasized that increasing the SET

diameter increases the amount of charge induced on it but reduces its sensitivity, so that a trade-off situation exists.

In the approximation k_{QD2}<<1, which is commonly valid for experiments in 2DEG systems, the SNR of the charge detection signal due to a change in N on the dc measurement limit is given by $SNR=20Log_{10}[ek_{QD2}(\Delta f)^{-1/2}(\delta q_2)^{-1}]$ (hereinafter we consider QD2 to be the SET charge sensor), where Δf is the measurement bandwidth. By simultaneously considering the capacitive coupling k_{QD2} and the charge sensitivity δq_2, the key capacitive parameter determining the SNR is found to be the coupling energy $E_m=e^2\alpha k_{QD2}/C_{QD2}$, because in view of the above discussion, $k_{QD2}/\delta q_2$ is proportional to E_m. Figure 5.5(b) shows the numerically calculated E_m as a function of L_{QD2}. It can be seen that increasing L_{QD2} or d leads to a reduction in E_m; that is to say, decreasing the SET diameter leads to an increase in the SNR. It is noteworthy that decreasing the SET diameter reduces the capacitive coupling k_{QD2} but causes a larger increase in the sensitivity, which results in an increase in the SNR.

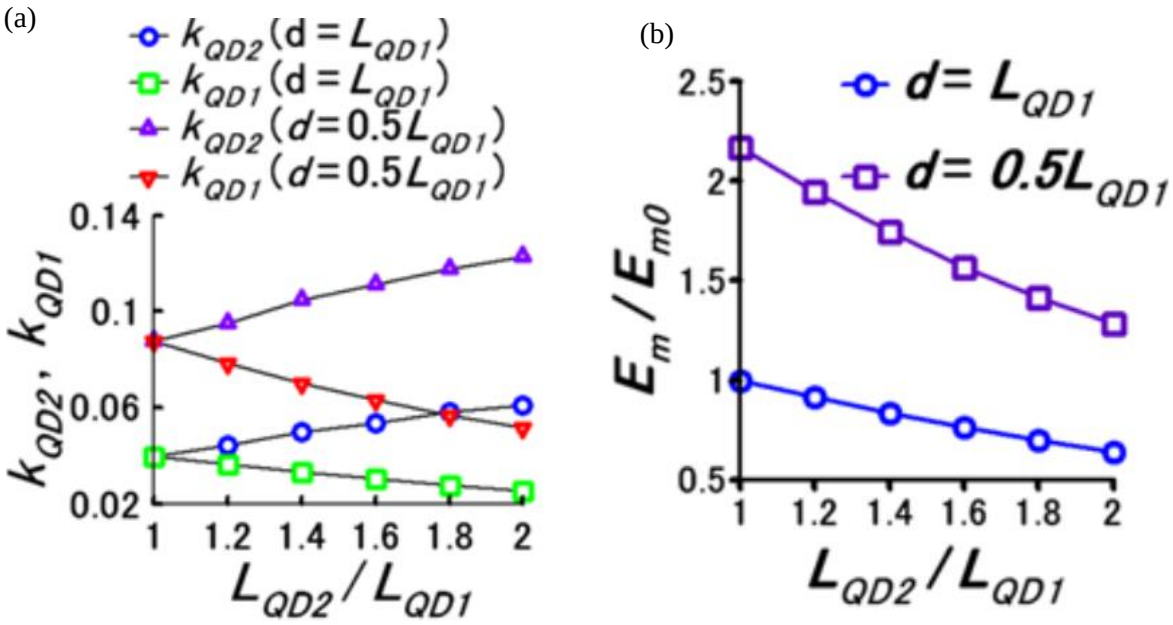


FIG. 5.5: (a) Calculation results for k_{QD1} and k_{QD2} as a function of L_{QD2} (in units of L_{QD1}) using the three-dimensional Poisson equation. L_{QD1} and the distance d between the edges of QD1 and QD2 are fixed. (b) Calculated E_m/E_{m0} as a function of L_{QD2} (in units of L_{QD1}) by the same method as for panel (a). E_{m0} is the value of E_m when $L_{QD2}=L_{QD1}$ and $d=L_{QD1}$. In panel (a) and (b), the calculation results are shown for $d = L_{QD1}$ and $d = 0.5L_{QD1}$.

5.5 Measurement of capacitive parameters of SET charge sensors probing few-electron QDs

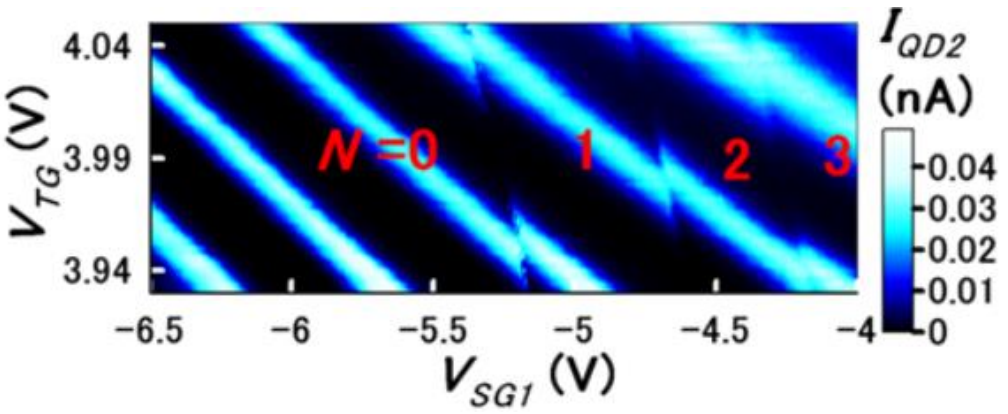


FIG. 5.6: Plots of I_{QD2} as a function of V_{TG} and V_{SG1} for another device. V_{D1} = 1 mV, V_{D2} = 5 mV, and V_{SG2} = –5.8 V.

Figure 5.6 shows plots of I_{QD2} as a function of V_{TG} and V_{SG1} for another fabricated device. In this case, QD1 is the few-electron regime, which is required for manipulation of electron spins. In this low-N regime, k_{QD2} values of 1.10, 0.98, and 0.93 are obtained for the 0↔1, 1↔2, and 2↔3 transitions of N, respectively (note that n is still large in this condition). k_{QD2} increases with decreasing N because the effective size of QD1 becomes smaller than its lithographically defined size due to the small value of N. This indicates that operating in the few-electron regime will improve the SNR when reading charge qubits in lateral QD-SET systems.

5.5 Numerical calculation for the signal-to-noise ratio in RF-SET operation.

Finally, the effect of varying L_{QD2} and d on the SNR was investigated for RF single-shot measurements under the conditions shown in Fig. 5.7(a). Here, exact resonance at the carrier frequency $\omega=(LC_S)^{-1/2}$ and the quasistationary condition $\omega \ll I_{SET}/e$ are assumed. Assuming a low circuit impedance $Z \approx L/C_sR_d \ll R_0$, where R_d is the SET differential resistance and $R_0 \approx 50\ \Omega$ is the cable wave resistance, the SET bias voltage can be expressed by a simple sine wave,

$V_L(t)=V_0+A\sin\omega t$. [103, 104, 108] Here V_0 is a static component and A is the SET bias amplitude. Restricting the analysis to the first harmonic of the reflected wave, [103, 104, 108] we obtain

$$SNR = 20\log_{10}\frac{\left|\left\langle I_{SET}(t)\sin\omega t\right\rangle - \left\langle I'_{SET}(t)\sin\omega t\right\rangle\right|}{\sqrt{\Delta f\left\langle S_I(t)\sin^2\omega t\right\rangle}} \qquad (5.5)$$

Here $\langle\cdots\rangle$ denotes the time average, and I'_{SET} is the current when a charge $\pm ek_{QD2}$ is induced in QD2. From the equations and the numerical calculation of the QD-SET capacitive coupling, it is found that increasing L_{QD2} and d causes a reduction in the SNR, similar to the case for the dc measurements. Figure 5.7(b) shows the numerically calculated SNR as a function of L_{QD2} using the optimized gate bias conditions (included in $\sum C_jV_j$ in Eq. (2)). L_{QD1} is fixed and other calculation parameters are given in the figure caption. Figure 5.7(b) shows that increasing L_{QD2} reduces the SNR, that the SNR for $d = 0.5L_{QD1}$ is larger than that for $d = L_{QD1}$, and that increasing C_L/C_{QD2} causes a slight increase in the SNR. We found that decreasing L_{QD2}/L_{QD1} from 2 to1 yields approximately twice greater signal power both in $d = 0.5L_{QD1}$ and in $d = L_{QD1}$. Generally the distance between the QD and the SET charge sensors is designed as small as possible for experiments to enhance the capacitive coupling between the QD and the SET. However device structures provide the limitation of the minimal distance between the QD and the SET on the device fabrication. In this situation, decreasing the SET diameter is another effective means of improving the SNR.

This study focused on the capacitive parameters of an SET charge sensor in order to establish guidelines for improving the SNR during qubit readout. However, reducing the parasitic resistance of the device is still an effective means of improving the SNR, as is asymmetric tuning of the tunnel resistance of the SET [103, 104, 108].

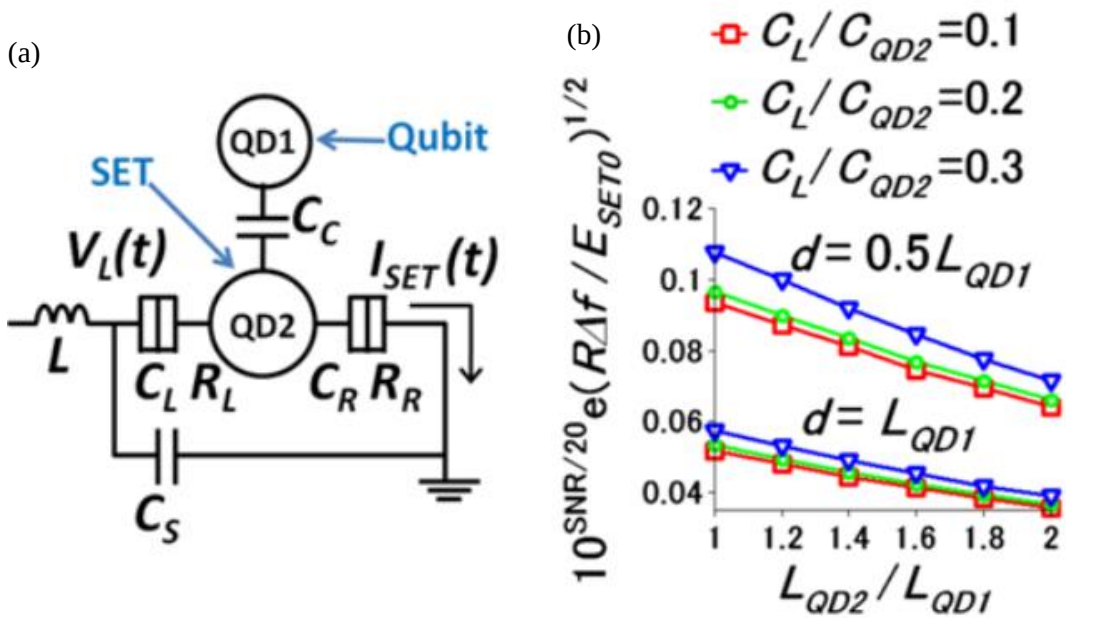


FIG. 5.7: (a) Schematic diagram of RF measurement setup. (b) Numerical calculation results for the SNR as a function of L_{QD2} (in units of L_{QD1}) for optimized gate bias conditions. Using y-axis value $Y=10^{SNR/20}e(R\Delta f/E_{SET0})^{1/2}$ in (b), the SNR can be expressed as $SNR=20\mathrm{Log}_{10}[Y/\{e(R\Delta f/E_{SET0})^{1/2}\}]$. Here, $R_L = R_R = R$, $k_BT = 0.01E_{SET0}$ (E_{SET0} is the charging energy of QD2 when $L_{QD2} = L_{QD1}$ and $d = L_{QD1}$), $A = 0.2E_{SET0}/e$, $V_0 = 0$, and L_{QD1} is fixed. Calculations were performed for C_L/C_{QD2} = 0.1, 0.2, and 0.3. Calculation results for $d = L_{QD1}$ and $d = 0.5L_{QD1}$ are shown.

5.6 Summary

In summary, twin silicon single QDs were fabricated using a lithographic process, and capacitive parameters which relate the charge sensitivity of SET charge sensors were investigated. The dependence of the charge sensitivity on QD size was evaluated based on the charging energy. The measured electrostatic characteristics were found to be in good agreement with numerical calculations, and the key capacitive parameter determining the SNR was identified. When one QD was in the few-electron regime, it was found that decreasing the number of electrons in this QD led to an increase in the electrostatic coupling between the QDs. Numerical calculations of the QD-SET coupling suggested that decreasing the SET diameter and the distance between the QD and the SET leads to an increase in the SNR for both dc and RF single-shot measurements. Since these results are independent of the device materials, they

are useful for establishing guidelines for the design of SET charge sensors in lateral QD-SET structures based on a 2DEG.

Chapter 6

Control of the tunnel coupling between coupled quantum dots

6.1 Introduction

Electron spin qubit architecture require to control and use the exchange coupling between tunnel coupled QDs as mentioned in chapter 1. Usually the exchange coupling energy *J* can be controlled by applying pulse voltage into the gate contact in which the stats on the charge stability diagram in the tunnel coupled QDs moves detuning direction. This method is valid in our device. However it is necessary to control the maximum value of *J* to allow flexible qubit operation. In our lithographically-defined device, it is relatively difficult to control the maximum value of *J* because the tunnel coupling greatly depends on width of the lithographically-defined construction region at the tunnel barriers. In this chapter we introduce control of the tunnel coupling between coupled QDs, i.e. control of the maximum value of *J* by tuning the top gate voltage. In the few-electron regime of QDs, tunnel couplings at tunnel barriers of the QDs can be controlled by tuning the TG voltages in both the single and double QD structures, which indicates the device structure has adaptability for the manipulation of electron spins using exchange coupling between tunnel-coupled QDs.

6.2 Device structures and measurement setups

Figure 5.1(a) and (b) show a scanning electron microscopy (SEM) image of a single QD and double QD (DQD) structure with an SET charge sensor. The device fabrication process is the same as that described in chapter 3, chapter 4, and chapter 5. In this chapter measurements for single QDs and double QDs are performed at base temperature of 4 K and 300 mK respectively. The side-gate voltages (V_{SG1} and V_{SG2}) are applied to control electrochemical potentials in the QD and the SET. The SET is used as a charge sensor to probe change in the number of electrons confined in the QD.

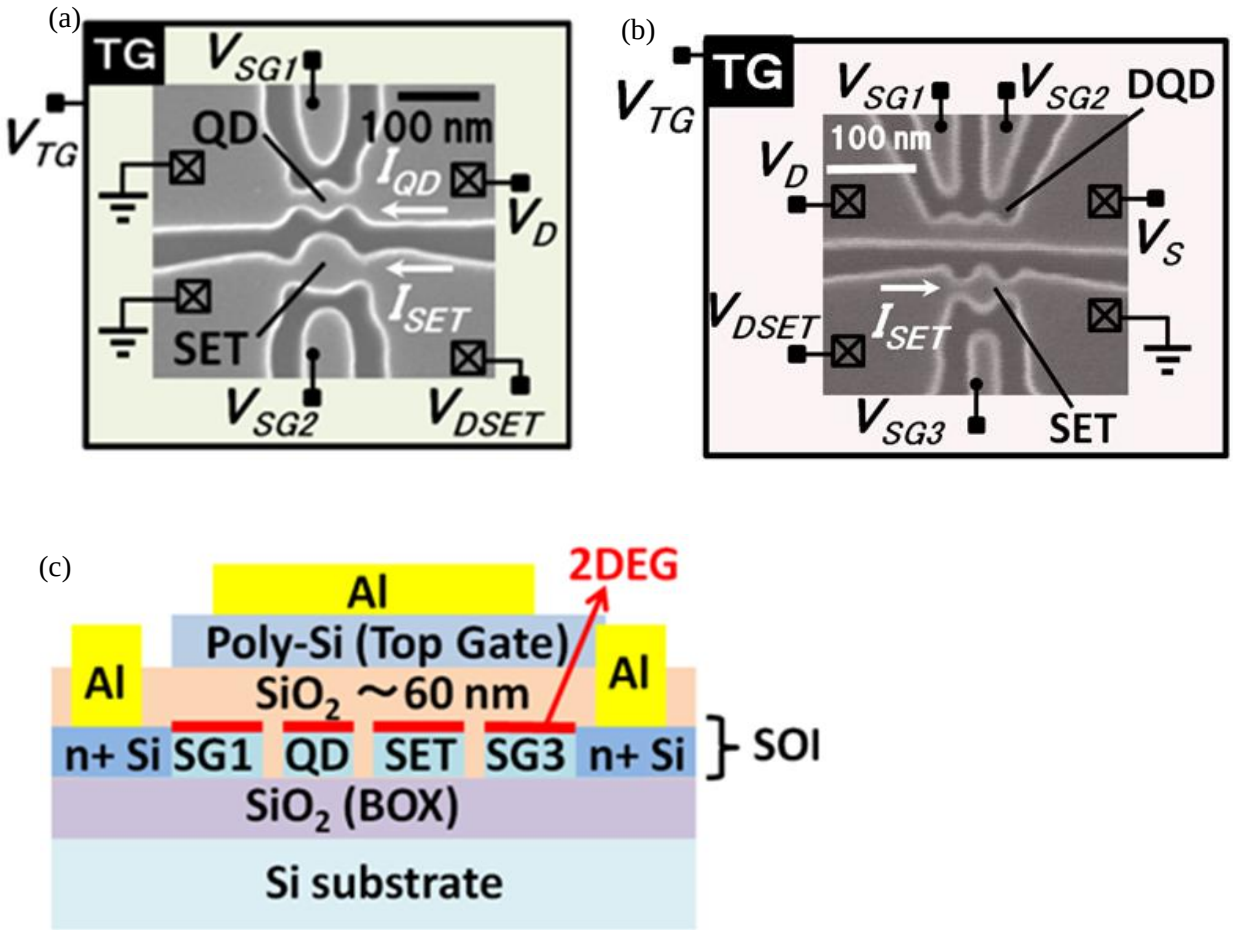
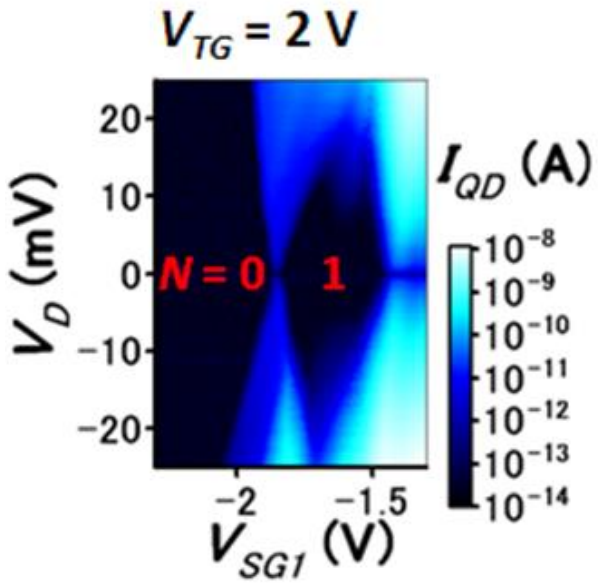


FIG. 6.1: (a) Scanning electron microscopy (SEM) image of a single QD device and and schematic measurement setups. (b) SEM image of a double QD (DQD) device and schematic measurement setups. DQD device is fabricated by the same process as that for the single QD device. Measurement of the single QD and DQD devices was performed at a base temperature of 4.2 K and 300 mK respectively. (c) Schematic cross section of the device structure.

6.3 Control of the tunnel rates at tunnel barriers in few-electron silicon single quantum dots

First we tried to control the tunnel coupling at tunnel barriers in few-electron silicon single QDs. Here we measured identical single QD sample to that introduced in chapter 4. This sample shows clearly few-electron regime, such as N = 0, 1, and 2, by using charge sensing measurements. In this device, although the transition line between N = 0 and N = 1 is clearly visible in the SET dI_{SET}/dV_{SG1} (see Fig. 4.2(b)), no Coulomb peak corresponding to this transition in I_{QD} is evident (see Fig. 4.2(c)), because the tunneling rates between the QD and the leads are too small to observe a current though the QD for this transition, which is discussed later. Figures 6.2(a) and 6.3(b) show the plots of I_{QD} as functions of V_{SG1} and drain voltage V_D at different TG voltages of V_{TG} = 2 and 3.8 V, respectively. Here typical Coulomb diamonds for the single QD system are observed [2]. We confirmed exact number of confined electrons in the QD for each of Coulomb diamonds by charge sensing measurements mentioned in chapter 4. In Fig. 6.2(b), the diamond for the second electron (N = 2) is visible; however, the diamond for the first electron (N = 1) is not. This is because the tunnel rates on the tunnel barriers of the QD are too small to observe the current for the N = 1 region at high V_{TG}. In contrast, the diamond for N = 1 is clearly visible in Fig. 6.2(a) because of the large tunnel rates at lower V_{TG} compared to that in Fig. 6.2(b). Figure 6.3(a) shows I_{QD} with respect to V_{TG} and V_{SG1}, which represents the dependence of the tunnel rates on these gate voltages. An increase in V_{TG} while retaining the same electron number N results in a higher negative V_{SG1} to compensate for the electrochemical potential of the QD. In Fig. 6.3(a), the Coulomb peak between N = 0 and N =1 disappears as V_{TG} increases positively and V_{SG1} becomes more negative, which indicates the tunnel rates on the tunnel barrier of the QD are controllable by tuning these voltages. When a positively higher V_{TG} and negatively higher V_{SG1} are applied to the QD, the wave function of the electrons confined in the QD shrinks in the horizontal plane and becomes pressed to the edge of the lithographical QD shape (Figure 6.4(b)). The distance between the QD and the source-drain leads then becomes separated and the tunnel couplings between the QD and the leads become small.

(a)



(b)

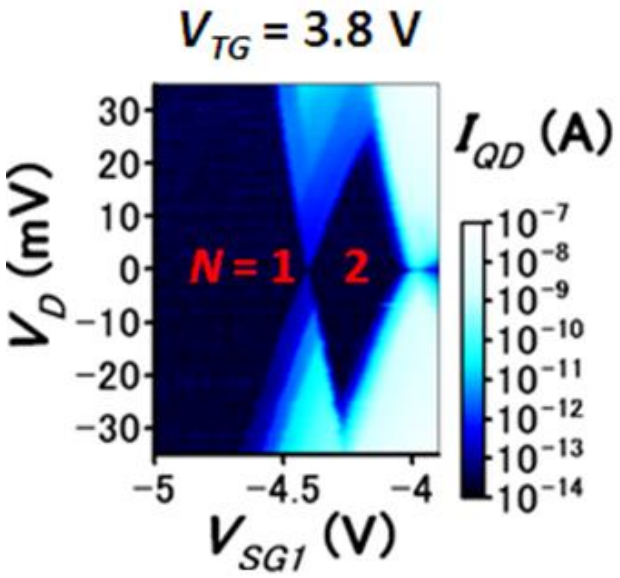


FIG. 6.2: (a)(b) Measured Coulomb diamonds of the QD current I_{QD} in the same single QD device shown in Fig. 2(d) at different TG voltage conditions of (a) V_{TG} = 2 V and (b) V_{TG} = 3.8 V.

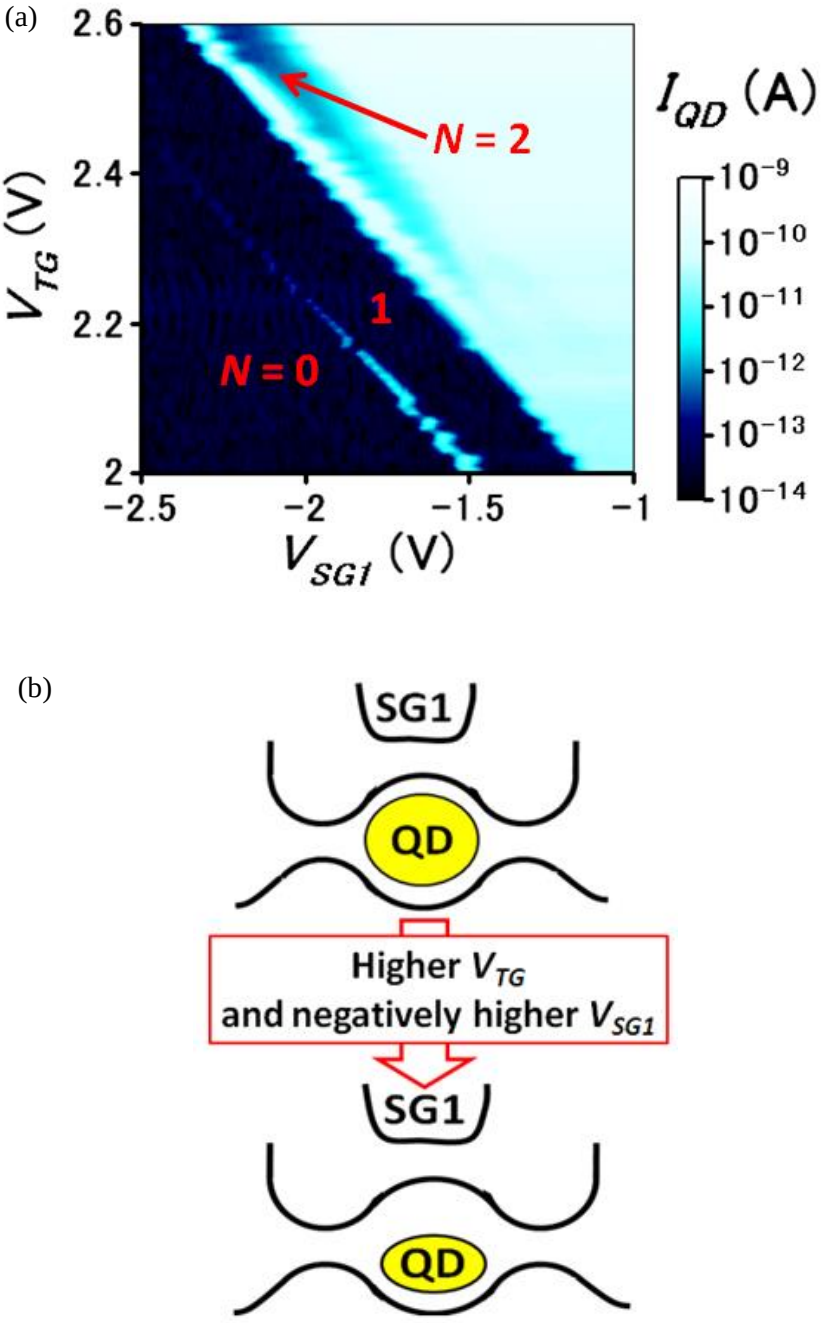


FIG. 6.3: (a) Plot of I_{QD} as functions of V_{TG} and V_{SG1}. The coulomb peak between N = 0 and N =1 disappears with the increase of V_{TG} due to a decrease of the tunnel rates on the tunnel barriers of the QD. (b) Schematic diagram of change in the wave function shape for an electron confined in the single QD when the positively higher TG voltage V_{TG}, and negatively higher side-gate voltage V_{SG1}, are applied while preserving the same number of electrons, N.

6.4 Control of the tunnel coupling between coupled few-electron double QDs

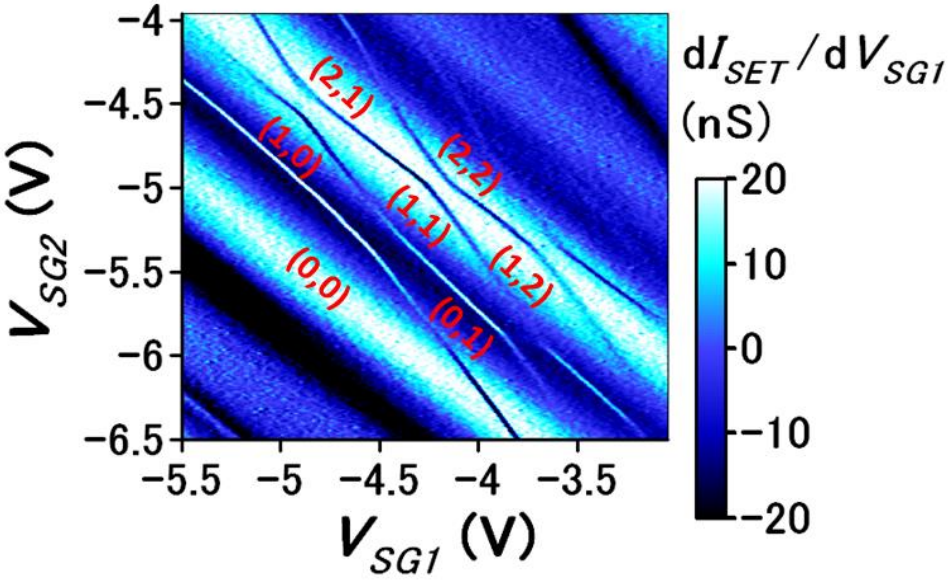


FIG. 6.4: Transconductance of the SET charge sensor dI_{SET}/dV_{SG1}, as functions of V_{SG1} and V_{SG2} in a DQD sample; V_{TG} = 5.8 V and V_{SG3} = 0 V, V_D = V_S = 0.9 V, and V_{DSET} = 3 mV. A charge stability diagram of the few-electron regime in the DQD is clearly obtained.

Figure 6.4 shows the plot of the SET transconductance dI_{SET}/dV_{SG1}, as functions of the side-gate voltage V_{SG1} and V_{SG2}. Here the charge stability diagram for the DQD is obtained from charge transition lines of the charge sensing, where the few-electron regime of the DQD is clearly evident. Figures 6.5(a) and 6.5(b) show plots of the SET transconductance dI_{SET}/dV_{SG1}, as functions of V_{SG1} and V_{SG2} in another DQD sample at different TG voltages of V_{TG} = 2.6 and 3.7 V, respectively. Here we focus on the charge stability diagram near the transition point between the (2,1) and (1,2) electron states. The electron state separation (length of the red double-headed arrow) in Fig. 6.5(a) is longer than that in Fig. 6.6(b), which indicates that both the tunnel and capacitive coupling between the tunnel-coupled QDs at V_{TG} = 2.6 V (Fig. 6.5(a)) are larger than those at V_{TG} = 3.7 V (Fig. 6.5(b)). The tunnel coupling between QDs generates anticrossing between the bonding and antibonding states in the energy versus detuning diagram, and the tunnel coupling energy t_c, can be estimated by bending of the charge transition lines reflected from the anticrossing in the DQD stability diagram. the tunnel coupling energy t_c was estimated to be *ca.* 0.48 meV in Fig. 6.5(a) and *ca.* 0.28 meV in Fig. 6.5(b) using the conversion factors

between the gate voltages and energy. If the states has singlet-triplet configuration (similar to the singlet (1,1) and triplet (1,1) configuration), the maximum value of the exchange coupling energy J is moderated J = 0.06 to 0.18 meV, which is estimated by the equation $J = 4t^2/E_C$, here E_C is charging energy of each QDs of the DQD [61]. This value is sufficiently large compared to few μeV order of J used in qubit manipulations in Si/SiGe heterostructure [20]. The capacitive coupling energy E_m, is also estimated to be *ca.* 2.5 meV in Fig. 6.5(a) and *ca.* 2.0 meV in Fig. 6.5(b) by the separation between the triple points at the (1,1)-(1,2)-(2,1) and (2,2)-(1,2)-(2,1) states [100]. The reason for the change in these coupling between QDs is explained in the same way as that for the single QD case: The positively higher V_{TG} and negatively higher V_{SG1} and V_{SG2} make the electron wavefunctions in the QDs shrink. The distance between the electron wavefunctions in each QD is then separated, and both the tunnel and capacitive coupling become small. The controllability of the tunnel coupling between the QDs represents that of the exchange coupling between electrons in the QDs; therefore, the measurement results indicate that the flexibility of the lithographically-defined device structure introduced here is acceptable for electron spin manipulation using the exchange interactions between QDs for the electron spin qubit. The addition energies E_{add}, for the addition of the second electron in the DQD at V_{TG} = 2.6 V are also estimated as $E_{add} \approx 8.4$ meV for the right dot and $E_{add} \approx 5.7$ meV for the left dot. In contrast, when V_{TG} = 3.7 V, $E_{add} \approx 9.5$ meV for the right dot and $E_{add} \approx 6.0$ meV for the left dot are obtained. The increase in the addition energy for the higher V_{TG} indicates the wavefunction of the electrons confined in the QD shrinks in the horizontal plane as V_{TG} increases and the side-gate voltages increase negatively.

The capacitive coupling energy E_m, is also estimated to be ∼ 2.5 meV in Fig. 6.5(a) and ∼ 2.0 meV in Fig. 6.5(b) by the separation between the triple points at the (1,1)-(1,2)-(2,1) and (2,2)-(1,2)-(2,1) states [100]. The reason for the change in these coupling between QDs is explained in the same way as that for the single QD case: The positively higher V_{TG} and negatively higher V_{SG1} and V_{SG2} make the electron wavefunctions in the QDs shrink. The distance between the electron wavefunctions in each QD is then separated, and both the tunnel and capacitive coupling become small. The controllability of the tunnel coupling between the QDs represents that of the exchange coupling between electrons in the QDs; therefore, the measurement results indicate that the flexibility of the lithographically-defined device structure introduced here is acceptable for electron spin manipulation using the exchange interactions

between QDs for the electron spin qubit. The addition energies E_{add} [2, 100], for the addition of the second electron in the DQD at V_{TG} = 2.6 V are also estimated as $E_{add} \approx 8.4$ meV for the right dot and $E_{add} \approx 5.7$ meV for the left dot. In contrast, when V_{TG} = 3.7 V, $E_{add} \approx 9.5$ meV for the right dot and $E_{add} \approx 6.0$ meV for the left dot are obtained. The increase in the addition energy for the higher V_{TG} indicates the wavefunction of the electrons confined in the QD shrinks in the horizontal plane as V_{TG} increases and the side-gate voltages increase negatively.

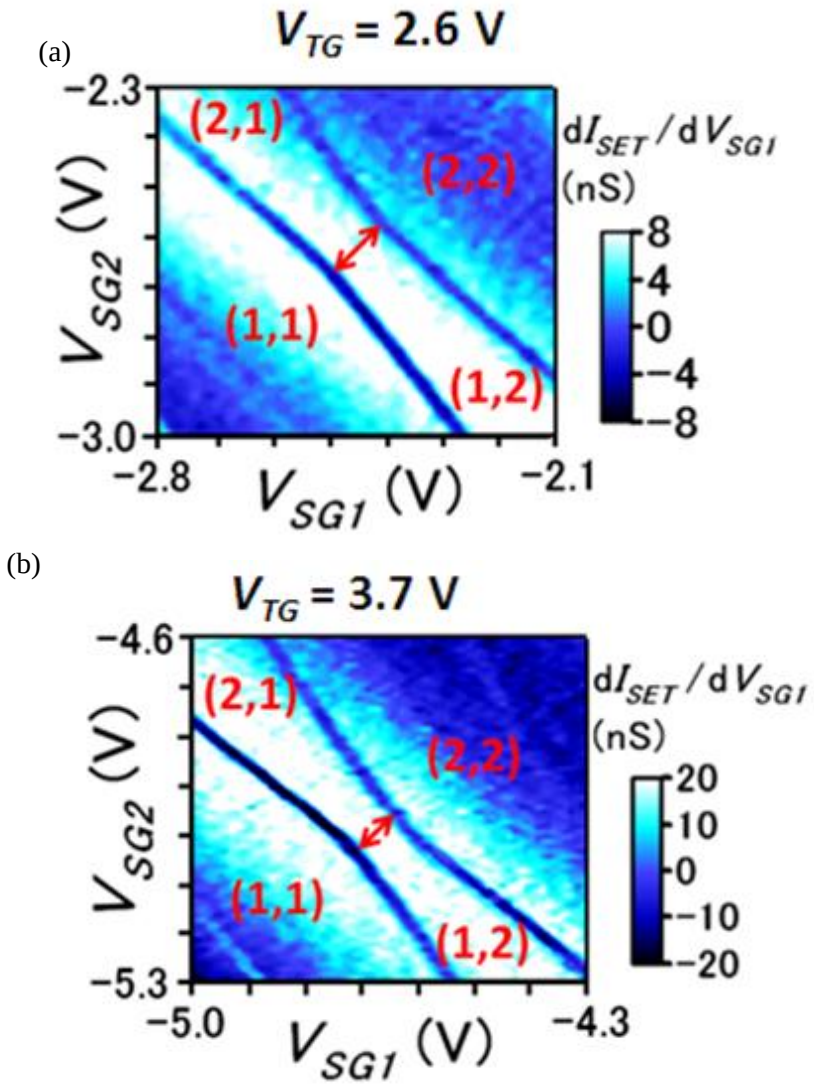


FIG. 6.5: (a,b) Charge stability diagram near the tunneling region between the (2,1) and (1,2) charge states in another sample with different TG voltages of (a) V_{TG} = 2.6 V and (b) V_{TG} = 3.7 V. The red double-headed arrows indicate the separation between the (1,1) and (2,2) charge states along the (2,1)-(1,2) tunneling line.

6.5 Summary

In summary, we have reported control of tunnel coupling between coupled QDs. Tunnel couplings on the tunnel barrier could be controlled by tuning the gate voltages. In few-electron double QDs the tunnel coupling energy t_c is moderated t_c = 0.28 to 0.48 meV, corresponding to moderations of maximum J = 0.06 to 0.18 meV in singlet-triplet configurations. This flexibility indicates that the lithographically-defined structure is acceptable for electron spin manipulation using the exchange interactions between QDs. This device structure is close to that of conventional CMOS structures and has a very high potential for integration because confinement gates are not required. The will become a more significant advantage for practical application with expansion to more complicated structures.

Chapter 7

Back-action-induced excitation of electrons in a silicon quantum dot with a single-electron transistor charge sensor

7.1 Introduction

As described in chapter 1, the back-action in charge sensing measurements cause qubit relaxation and dephasing and efforts must be made to minimize this back-action effect while maintaining a desirable level of sensitivity. In this chapter we demonstrate SET induced back-action measurements in silicon QDs and SET structures. The lithographically defined QD structure based on a silicon-on-insulator substrate reported here allows for a shorter distance between the QD and the SET compared with the conventional gate-defined QD structure. This produces a high-sensitivity charge sensor as well as significant coupling of the back-action between the QD and the SET. This system enables us to clearly observe the excitation of an electron in a QD to a higher state by the back-action of the SET during charge sensing measurements for a few-electron QD. By fitting curves to the results obtained, we found that there are conditions under which both an SET charge sensor with desirable sensitivity and low back-action-induced transition rates (less than 1 kHz) can be realized. When a magnetic field

was applied to the device, we observed the excitation of electrons from ground singlet (S) states to triplet (T_) states, which corresponds to the two-electron spin configuration in QDs. The measurements demonstrated here confirm the necessity to address the back-action in silicon devices for qubit architectures but also reveal the existence of measurement conditions under which the back-action of SET charge sensors can be suppressed.

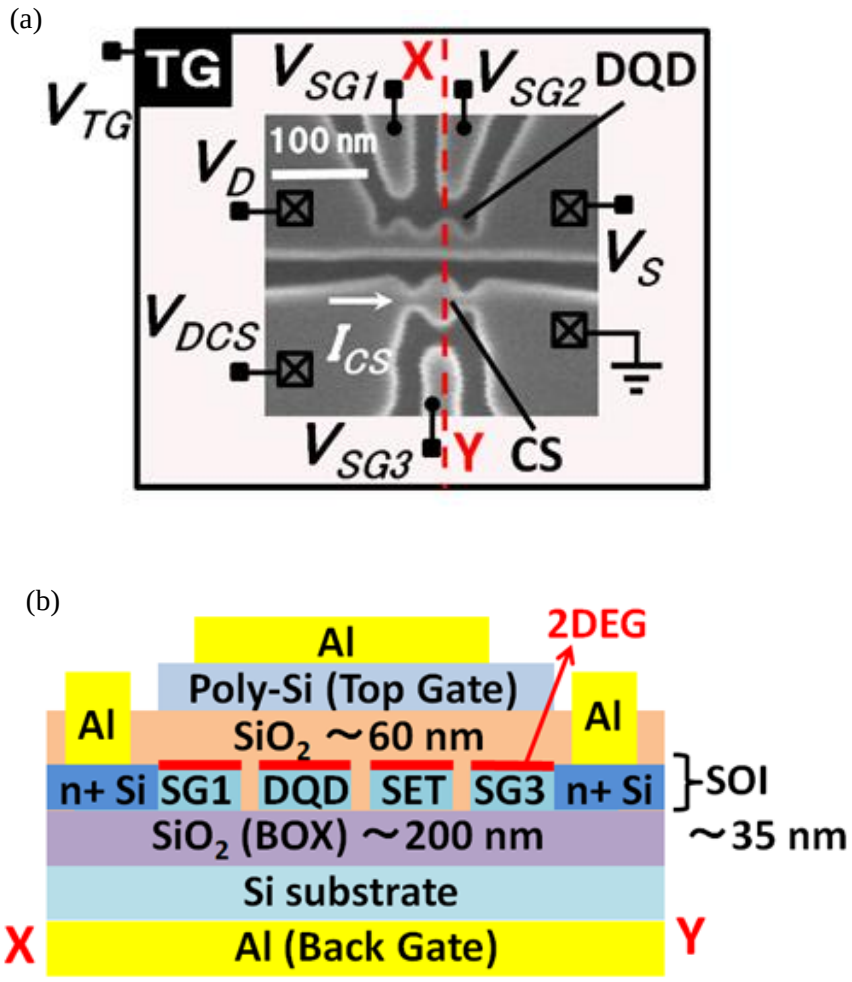


FIG. 7.1: (a) Scanning electron microscopy image of the device and measurement setup. (b) Schematic cross-section of the device structure along the XY line in (a).

7.2 Device structure and measurement settings

We fabricated a silicon double QD (DQD) device with an SET charge sensor (labeled CS in Fig. 7.1(a)) as same as chapter 4 to 6. Figure 7.1(a) shows a top-down scanning electron microscopy image of the device after the etching process. Figure 7.1(b) shows a schematic cross-section of the device structure. The experiment was carried out at a base temperature of 300 mK.

7.3 Observation of back-action-induced excitation of electrons in silicon quantum dots

Charge stability diagrams for few-electron states of the DQD, as measured by the SET, are shown in Figure 7.2. In this study we focused on the tunneling between the (0,1) and (0,2) charge states. This electron tunneling takes place between the right side lead and the right side dot (simply called the 'lead' and 'QD' hereafter, respectively) of the DQD. We measured the transconductance of the SET near the (0,1)↔(0,2) tunnel as functions of the charge sensor drain voltage V_{DCS} and the side gate voltage V_{SG2} (Figure 7.3(a)). The two parallel lines in the figure represent the tunneling of electrons between the QD and the lead. The left and right lines correspond to tunneling via a ground state and an excited state of the QD with two-electron occupancy, respectively. As the absolute value of V_{DCS} increases, the line on the right becomes more distinct, which indicates that back-action occurs. The energy dissipated from the SET charge sensor excites the electron from the ground state to the excited state. This excitation causes additional tunneling from the excited state of the QD to the lead, which produces the two parallel lines shown in the figure. In the two-electron-occupancy QD, the ground state is a spin singlet S, and the first excited state is three energy-degenerate spin triplet T_0, T_-, and T_+ (Figure 7.3(b)), which is consistent with the measurement made in the presence of a magnetic field reported later. The second excited state is an excited singlet S' and we believe this state has almost no contribution to our measurements, because the relaxation rate in spin invariant processes such as the transition from S' to S is predicted to be considerably faster (lower bound estimate of 15 MHz for a silicon QD [33]) than the tunneling rate between the QD and the lead (~250 kHz). The energy splitting between the ground and excited state $\Delta E \sim 390$ μeV, which is obtained using a conversion factor $\alpha = 12.53$ V/eV between energy and the side gate voltage

V_{SG2}, is consistent with the valley splitting in the order of several hundred μeV in silicon QDs [26, 32, 78].

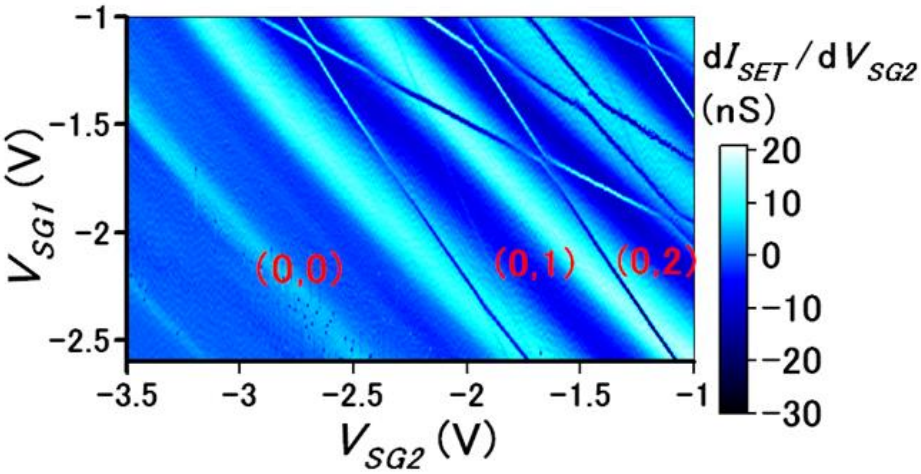
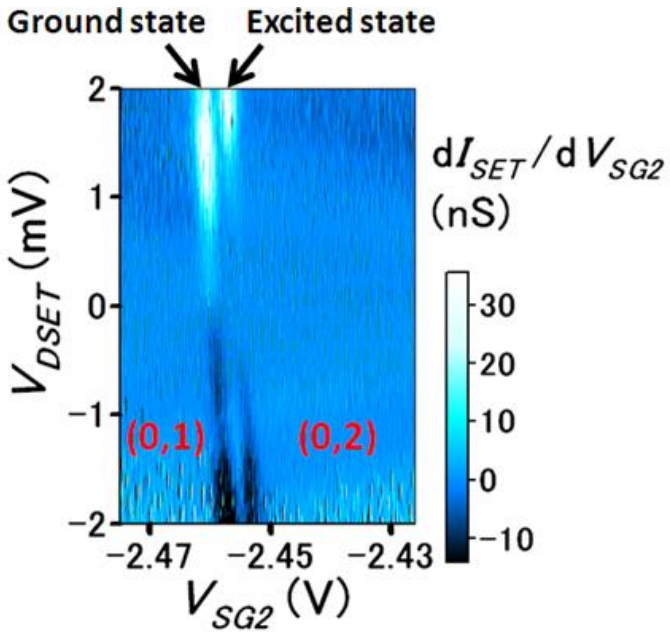


FIG. 7.2: Transconductance dI_{SET}/dV_{SG2} as a function of V_{SG1} and V_{SG2}. The stability diagram for a few-electron DQD is seen. n and m in (n, m) indicate the numbers of electrons confined in the left and right QDs of the DQD. V_{TG} = 3.85 V, V_D = 602 mV, V_S = 600 mV, V_{DSET} = 13 mV, and V_{SG3} = 0 V.

(a)



(b)

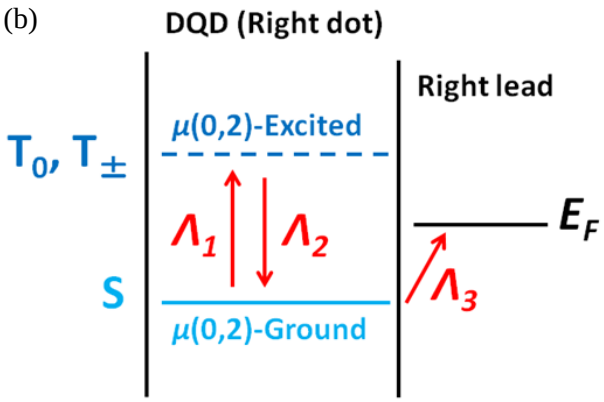


FIG. 7.3: (a) Transconductance dI_{SET}/dV_{SG2} of the SET as a function of V_{SG2} and V_{DSET}. V_{TG} = 4.35 V, V_D =V_S = 600 mV, V_{SG1} = -2.49 V, and V_{SG3} = -155 mV. (b) Schematic of the back-action-induced excitation.

7.4 Comparison of the back-action between at different operation point in the SET Coulomb oscillations and fitting calculations

Next, we compare the influence of the back-action in charge sensing measurements at different operation points in the SET Coulomb oscillations. The operation point can be changed by tuning the side gate voltage V_{SG3}. Figures 7.4(a) and 7.4(b) show the Coulomb diamonds of the SET current at V_{SG3} = -175 mV and V_{SG3} = -155 mV. It can be seen that the (0,1)↔(0,2) tunneling in the DQD occurs near the Coulomb blockaded region (in other words, the deep inside Coulomb blockade region) and near the Coulomb peak region, respectively.

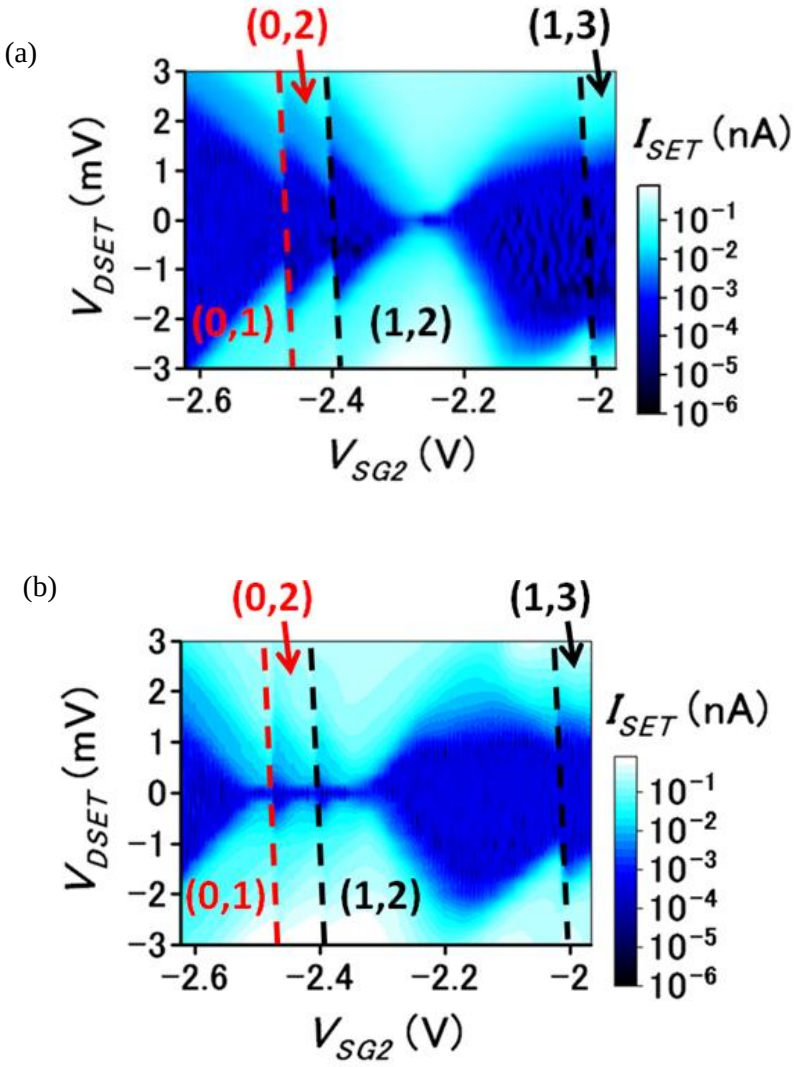


FIG. 7.4: (a) (b) Plots of the current through the SET (I_{SET}) as functions of V_{SG2} and V_{DSET} at V_{SG3} = -175 mV (a) and V_{SG3} = -155 mV (b).

Figures 7.5(a) and 7.5(b) show the transconductance of the SET in each of the two regions, respectively. Figure 7.6(a) shows the plot of I_{SET} along the red dashed line in Figure 7.5(a) with a fitted curve. The two-step decrease of I_{SET} as a function of V_{SG2} represents the tunneling of electrons between the QD and the lead. To fit a curve to these results, we used a master-equation model [96, 122] and the following rate equations.

$$\frac{d}{dt}P_i = \sum_j \left[\left(\Gamma_{ij} - \delta_{ij} \sum_k \Gamma_{ki} \right) p_j \right] \tag{7. 1}$$

Here i, j, and k = 0, 1, and 2, P_0 denotes the probability of finding an electron in the (0,1) state, and P_1 and P_2 denote probabilities of finding an electron in the ground and excited states, respectively (for zero magnetic field, we treat the three-degenerate triplet states as a single excited state), of the (0,2) state. Γ_{ij} is the tunneling rate from state j to i. These rates can be expressed as

$$\Gamma_{10} = \Gamma_{\max} f(\mu_1) \tag{7. 2}$$

$$\Gamma_{01} = 2\Gamma_{\max}(1 - f(\mu_1)) + \Lambda_3 \tag{7. 3}$$

$$\Gamma_{20} = \Gamma_{\max} f(\mu_2) \tag{7. 4}$$

$$\Gamma_{02} = 2\Gamma_{\max}(1 - f(\mu_2)) \tag{7. 5}$$

$$\Gamma_{21} = \Lambda_1 \tag{7. 6}$$

$$\Gamma_{21} = \Lambda_2 \tag{7. 7}$$

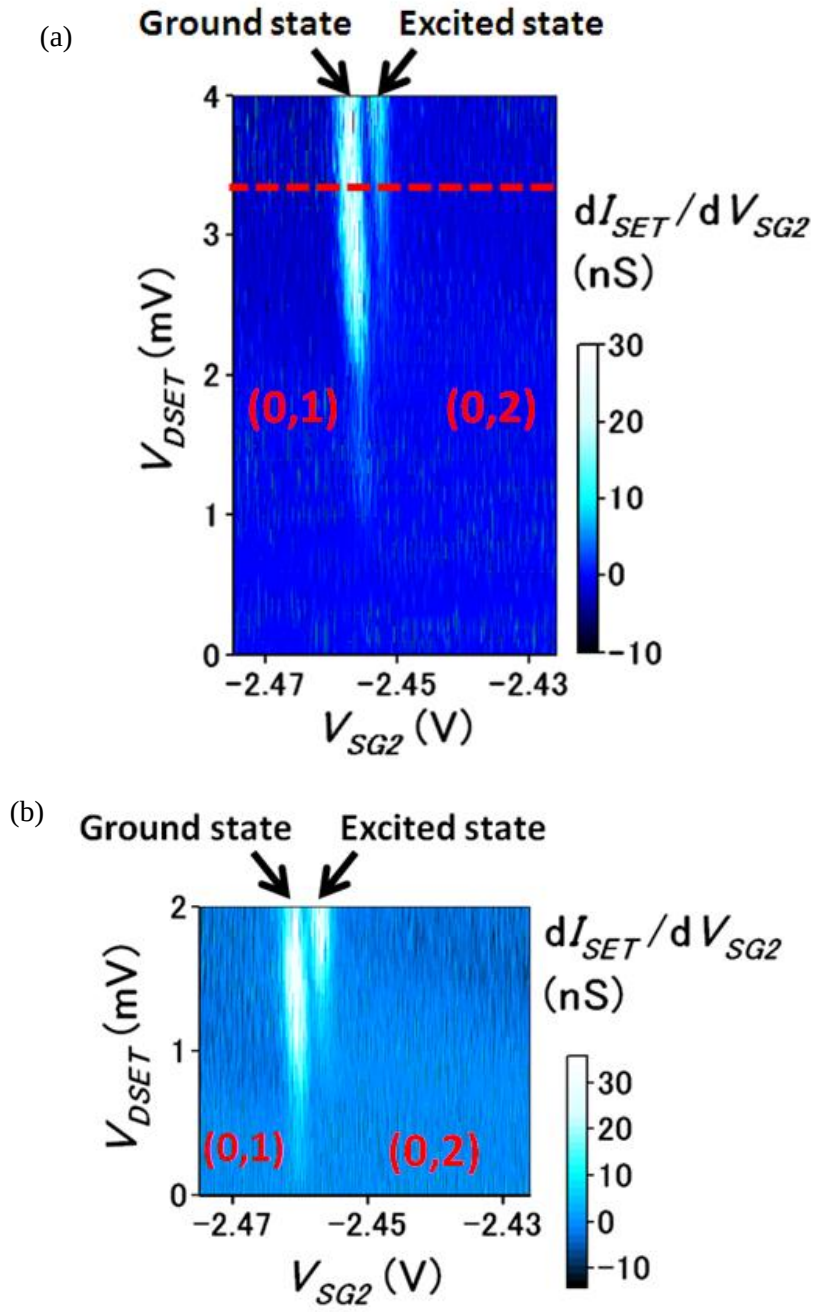


FIG. 7.5: (a) (b) Transconductance dI_{SET}/dV_{SG2} of the SET as a function of V_{SG2} and V_{DSET} at (a) V_{SG3} = -175 mV (near the Coulomb blockade region) and (b) V_{SG3} = -155 mV (near the Coulomb peak region).

Here, μ_1 and μ_2 denote the electrochemical potential of the ground state and excited state respectively, f(μ) is the Fermi-Dirac function, and Γ_{max} is the thermal-equilibrium maximum tunneling rate between the QD and the lead. Λ_1, Λ_2, and Λ_3 denote back-action-induced transition rates (Figure 7.3(b)) and $\Lambda_1 = \Lambda_2$. We do not take into account the natural relaxation rate from the triplet to singlet state in this calculation, because this relaxation rate is predicted to be considerably lower (millisecond-order triplet-singlet relaxation time in silicon QDs [26]) than Γ_{max} in this measurement. There are many electrons and exited states in the lead and then these electrons have many other processes to lose their energy. Therefore we do not take into account the excitation rate from the lead to the triplet exited states because it is considerably small compared with other excitation rates. We use equation $\Sigma P_i = 1$ and the steady-state condition $dP_i/dt = 0$. Using the fitted curve, we found that the excitation rate Λ_3 of the transition directly from the ground state to the lead is negligibly small compared to Λ_1. Figures 7.6(b) and 7.7(a) show the maximum I_{SET} value at the sensing point ($I_{SET\text{-}MAX}$) and the excitation rate Λ_1, respectively, as a function of V_{DSET}, for both the conditions near the Coulomb peak and the Coulomb blockade region. We found that there is a threshold $I_{SET\text{-}MAX}$ of ~20 pA at which Λ_1 becomes detectable in our measurement, implying the back-action strongly depends on the number of photons/phonons generated by the tunneling electrons constitute the SET current and not on the energy of photons/phonons. Figure 6.7(b) shows the change in the SET current ΔI_{SET}, which directly contributes to the charge sensitivity [102, 103, 104, 107, 108] of a charge sensor. From Figures 7.7(a) and 7.7(b), we can see that a non-zero value of ΔI_{SET} is obtained with an almost-zero Λ_1 (less than 1 kHz) in the range of 0.1 mV $\leq V_{DSET} \leq$ 0.5 mV for near the Coulomb peak region and 0.8 mV $\leq V_{DSET} \leq$ 1.7 mV for near the Coulomb blockade region. These low V_{DSET} ranges are considered desirable for qubit readout due to the weak back-action strength. In Ref. 95 the back-action in the QD-QPC system has investigate. In this report the back-action strength increase as increasing the QD-QPC coupling and the drain voltage of the QPC charge sensor. Typically QPCs do not have the Coulomb blockade characteristics and we cannot distinguish which is critical for the back-action the drain voltage of the sensor or the current through the sensor. On the other hand in the QD-SET system we can distinguish it. Based on our measurement results, we suggest a way to reduce the back-action by making the SET current as small as possible with keeping the required signal-to-noise ratio of the charge sensing signal.

Although we cannot conclude whether the SET mainly emits photons or phonons in our measurements, some speculations could be allowed for it. Firstly, we conjecture that the density of phonons generated from back-action in our SOI-based QD device is lower than that in bulk Si MOS devices because our SOI-based device has SiO_2 wall between the QDs and the SET, and there is an impedance mismatch for phonons on the Si-SiO_2 interface. Existence of the impedance mismatch on the interface between different materials could reduce the transmission probability of the phonon. Similar discussion has been described in Ref. 123. Secondly, the SET can behave as an alternating voltage source shaking the electrochemical potential in the QD. The QD-SET distance is small (about 20 nm) compared to the radiation wavelength and therefore the capacitive (photonic) coupling between the QD and the SET is large. Then no free propagation of photons occurs and therefore photon-assisted tunneling could be generated as the back-action [123].

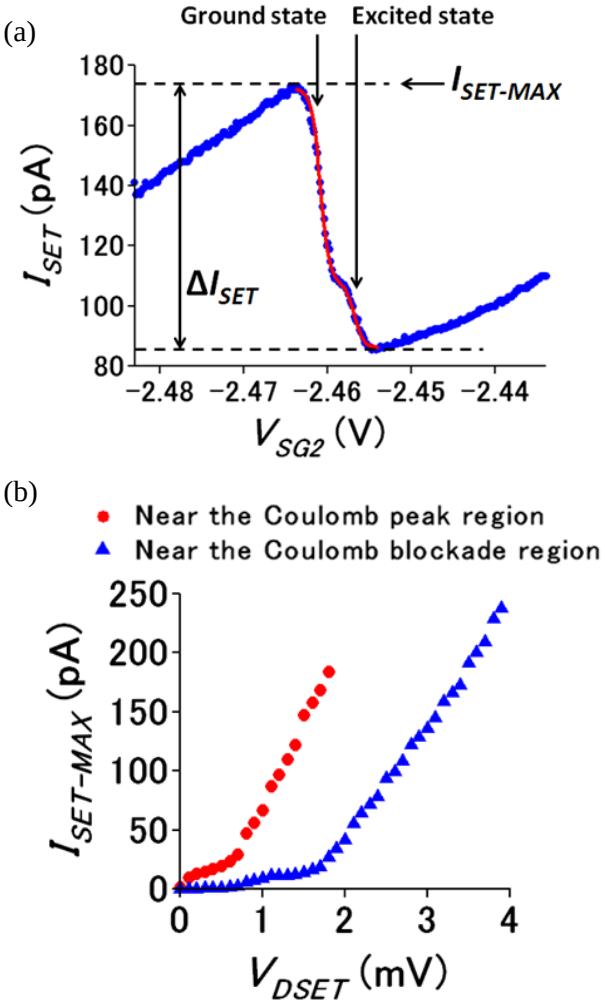
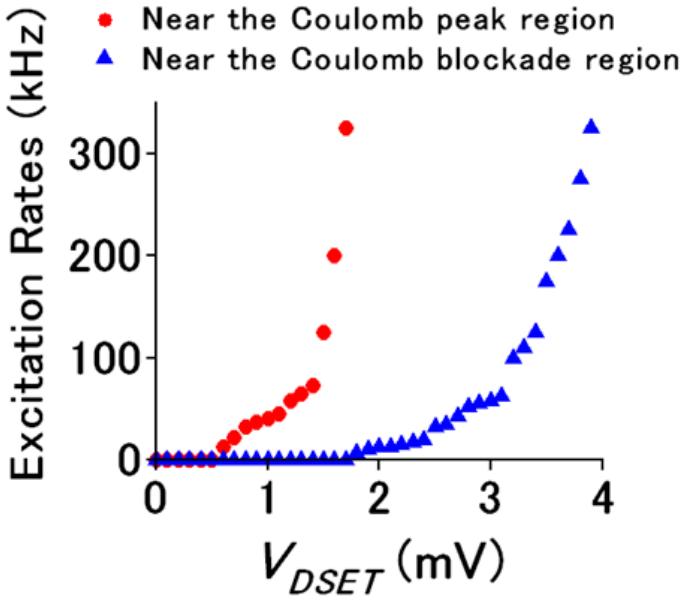


FIG. 7.6: (a) Plot of I_{SET}. The blue circles represent the plot of I_{SET} at V_{DSET} = 3.4 mV (along the red dashed line in Fig. 6.5(a)). The red solid curve was fitted numerically (T_e = 500 mK, Γ_{MAX} = 250 KHz, Λ_1 = 125 kHz, Λ_3 = 0 Hz, and ΔE = 390 μeV). (b) Plots of $I_{SET-MAX}$ for both cases when the sensing point of the SET current is near the Coulomb peak region (V_{SG3} = -155 mV) and near the Coulomb blockade region (V_{SG3} = -175 mV), respectively.

(a)



(b)

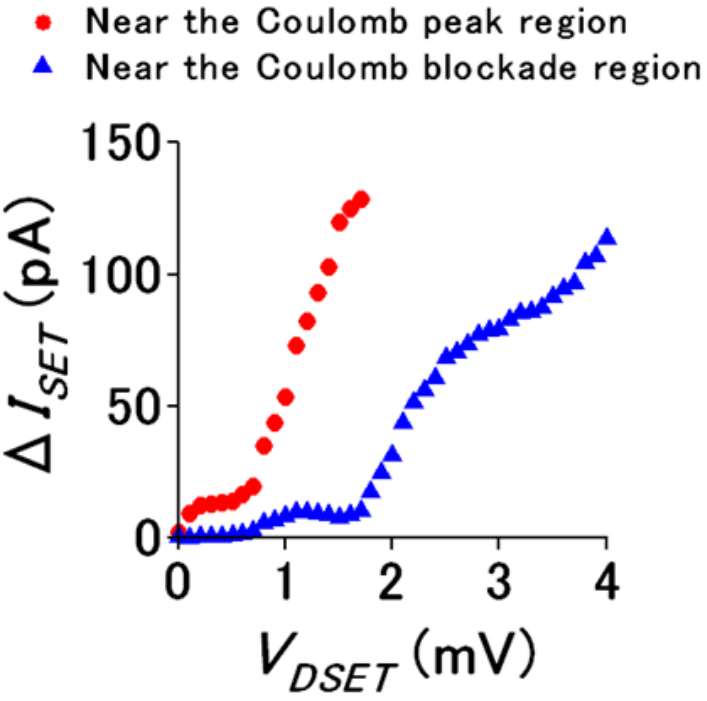


FIG. 7.7: (a) (b) Plots of (a) the excitation rate Λ_1, and (b) ΔI_{SET}, for both cases when the sensing point of the SET current is near the Coulomb peak region (V_{SG3} = -155 mV) and near the Coulomb blockade region (V_{SG3} = -175 mV), respectively.

7.5 Magnetic field dependence of the electron excitation

The in-plane magnetic field dependence of the charge sensor current I_{SET} ($B_{//}$ = 0, 1, and 2 T) is shown in Figure 7.8(a). Applying a magnetic field makes the triplet$_-$ (T$_-$) state approach the singlet (S) state due to Zeeman splitting (Figure 7.8(b)). We explain about the S and T state in section 8 in detail. Another step in the I_{SET} vs V_{SG2} curve can be seen in Figure 7.8(a), which corresponds to the T$_-$ state being lowered by the Zeeman energy in a parallel magnetic field. From the measurement result at $B_{//}$ = 2 T, we extract a g-factor of g ~ 1.97, which agrees with the theoretical value of g = 2, and supports the occurrence of the S-T transition induced by the back-action in our measurement.

7.6 Summary

In summary, we reported SET induced back-action measurements in a silicon device with QDs and an SET charge sensor. We clearly observed the back-action-induced excitation of electrons from the ground singlet state to the excited triplet state in a QD with two-electron occupancy. Our measurements and fitted curves show that the back-action largely depends on the number of phonons generated by the SET current. From this result we conjecture that the back-action is caused by photons generated from shot noise of the SET current. We also identified conditions that make possible both a desirable sensitivity for qubit readout and back-action-induced transition rates of less than 1 kHz.

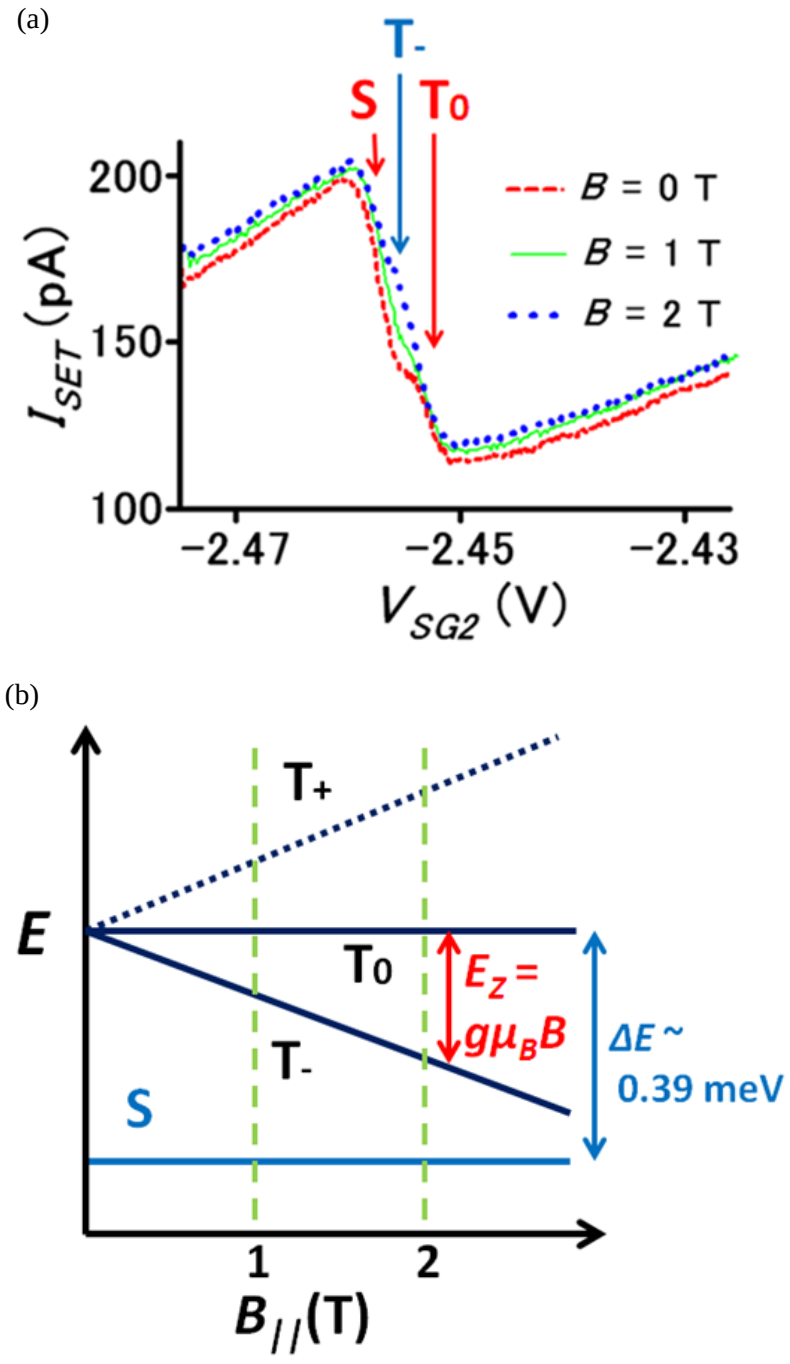


FIG. 7.8: (a) Plots of I_{SET} at different in-plane magnetic fields. (b) Schematic energy diagrams for the right dot as a function of the magnetic field.

Chapter 8

Pulse measurements of Pauli spin blockade in few-electron silicon double quantum dots

8.1 Introduction

Pauli spin blockade is greatly useful for measurements of electron spin qubits. The spin to charge conversion has been used to probe the spin stats in double QD systems. In the qubit measurements, single-shot measurements (i.e. time-resolved measurements) of the spin states using pulse measurements required to achieve qubit manipulation. In this chapter we introduce pulse measurement of Pauli spin blockade in few-electron silicon double QDs (DQDs). We observed the spin blockade (5,1)-(4,2) tunneling region of a DQD by applying pulse voltage to two side-gate. We performed time-averaged measurements of the charge sensing signals. This measurement will be an important mediation for single-shot measurements of singlet-triplet qubits using pulse voltage measurements.

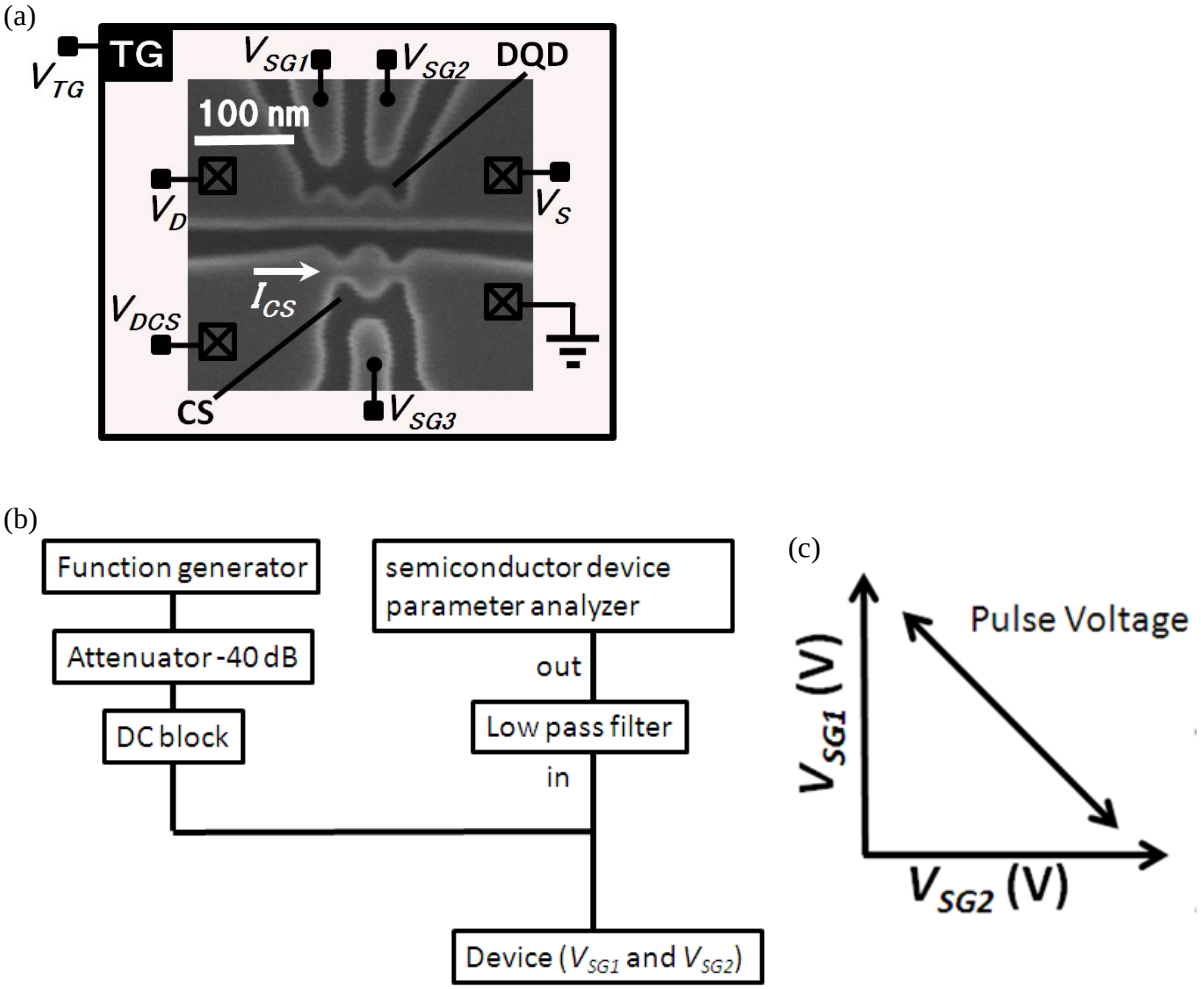


FIG. 8.1: (a) Scanning electron microscopy image of the DQD device with an SET charge sensor (SC) (b) Setup of pulse measurements. Function generator is used for creating pulse voltage (50% duty ratio) and semiconductor device parameter analyzer (4142B) is used to add a DC voltage offset to the pulse signal. (c) Schematic of pulse direction in the pulse measurements. We used two function generator and applied pulse voltage to V_{SG1} and V_{SG2} respectively. Two pulses is synchronized with phase of 180 degree each other (opposite phase) and the pulse direction is along with the detuning axis (see section 2) on the charge stability diagram.

8.2 Device structure and measurement settings

Figure 8.1 (a) shows a scanning electron microscopy image of the DQD device with an SET charge sensor (SC). The device fabrication is the same as that in chapter 4 to 7. Figure 8.1 (b) shows the setup of pulse measurements. Function generator is used for creating pulse voltage (50% duty ratio) and semiconductor device parameter analyzer (4142B) is used to add a DC voltage offset to the pulse signal. DC block is used for preventing the DC voltage from transmitting to the function generator. Low pass filter is used for preventing the pulse voltage signal from reflecting at the semiconductor device parameter analyzer. Figure 8.1 (c) shows a schematic of pulse direction in the pulse measurements. We used two function generator and applied pulse voltage to V_{SG1} and V_{SG2} respectively. Two pulses is synchronized with phase of 180 degree each other (opposite phase) and the pulse direction is along with the detuning axis (see section 2) on the charge stability diagram. The charge sensor signals are measured with time-averaged measurement by the source measure unit (SMU) of a semiconductor device parameter analyzer. Measurement was performed at base temperature of 300 mK.

8.3 Observation of Pauli spin blockade by pulse measurements

Figure 8.2(a) shows transconductance dI_{CS}/dV_{SG2} as a function of V_{SG1} and V_{SG2}. In this measurement no pulse voltage is applied and the stability diagram of few-electron regime of a DQD is obtaind. Figure 8.2(b) shows transconductance dI_{CS}/dV_{SG2} as a function of V_{SG1} and V_{SG2}. We focus of the stability diagram near the (5,1)-(4,2) region because the tunnel rates between QDs are suitable to measure spin blockade in the pulse measurements. Figure 8.3(a) shows transconductance dI_{CS}/dV_{SG2} as a function of V_{SG2} and pulse amplitude for V_{SG2} in pulse measurements. 100 kHz pulse voltage is applied to V_{SG1} and V_{SG2}. The right-hand charge sensing line corresponds to the (4,2)→(5,1) tunneling and the left-hand charge sensing line corresponds to the (5,1)→(4,2) tunneling respectively. The right-hand line has the stronger signal than the left-hand line, indicating in the (5,1)→(4,2) tunneling the charge transition is blocked because of Pauli spin blockade. Pauli spin blockade occurs transition between spin singlet (S) states and spin triplet (T) states based on the Pauli-exclusion principle. The S and T states consist of the two spin system [61]. The wavefunction of the spin component for the S state is expressed as $|S\rangle = \left(|\uparrow\downarrow\rangle - |\downarrow\uparrow\rangle\right)/\sqrt{2}$ and it has total *z*-projected momentum of 0.

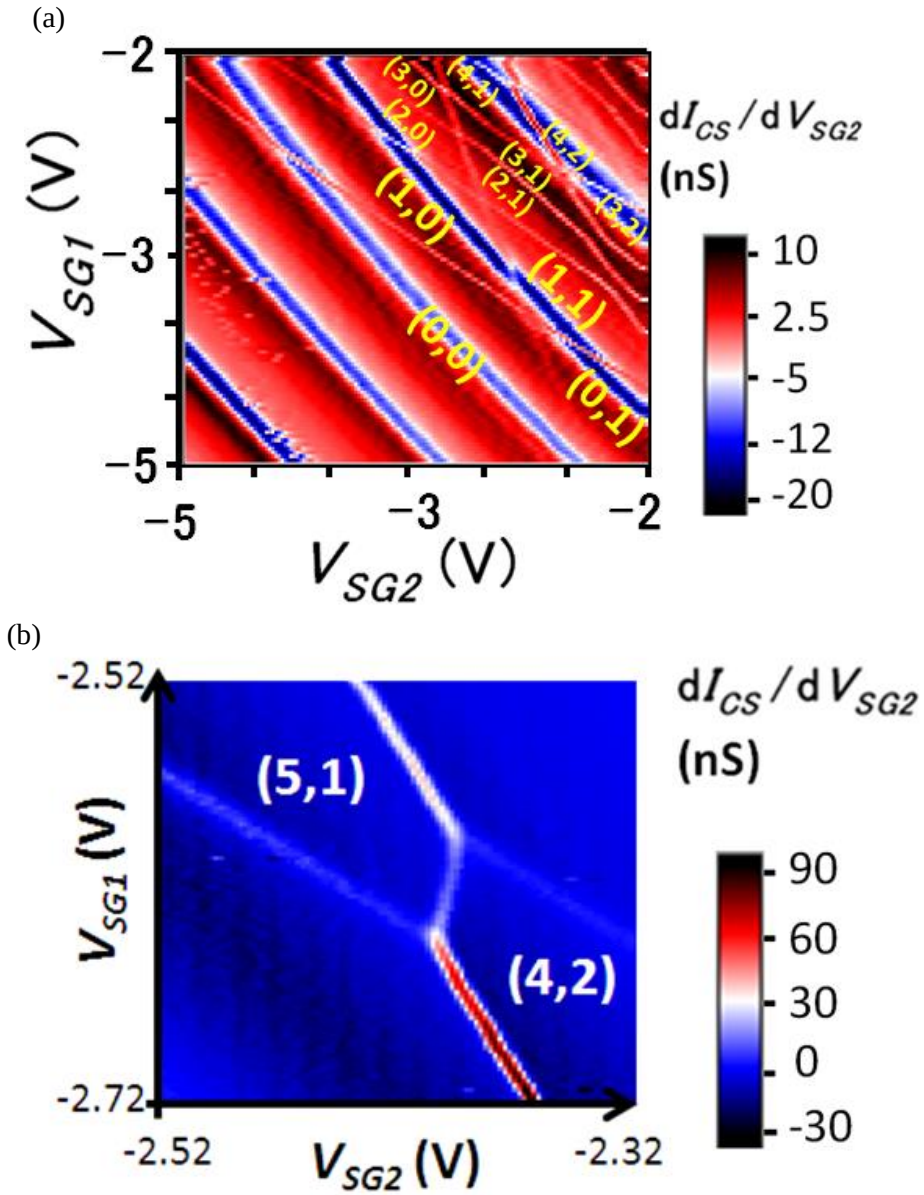


FIG. 8.2: (a) Transconductance dI_{CS}/dV_{SG2} as a function of V_{SG1} and V_{SG2}. In this measurement no pulse voltage is applied. The stability diagram for a few-electron DQD is seen. *n* and *m* in (*n*, *m*) indicate the numbers of electrons confined in the left and right QDs of the DQD. V_{TG} = 1.8 V, V_D = 0 mV, V_S = 0 mV, V_{DCS} = 4 mV, and V_{SG3} = 0 V. (b) Transconductance dI_{CS}/dV_{SG2} as a function of V_{SG1} and V_{SG2}. In this measurement no pulse voltage is applied. We focus on (5,1)-(4,2) tunneling region. V_{TG} = 1.9 V, V_D = 0 mV, V_S = 0 mV, V_{DCS} = 5 mV, and V_{SG3} = 20 mV.

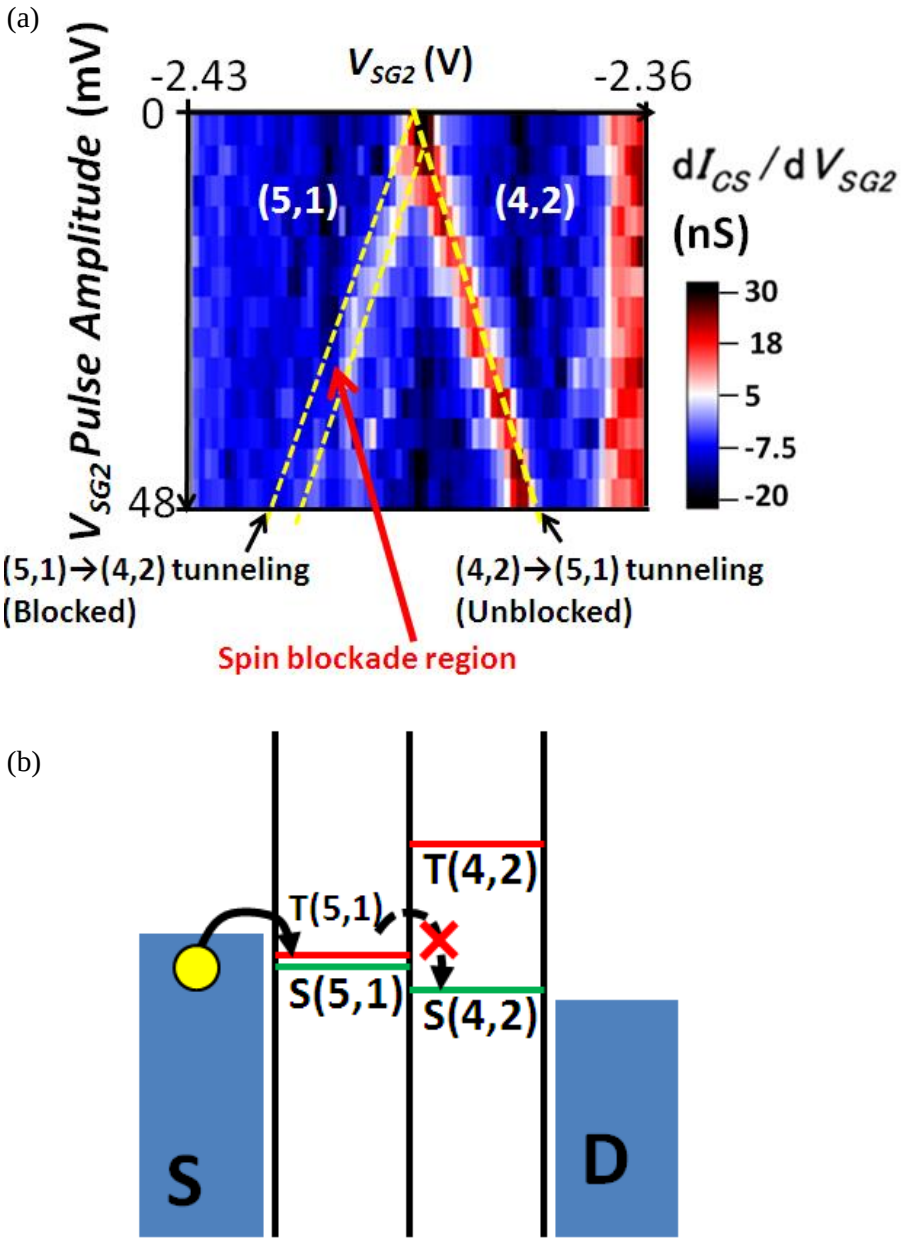


FIG. 8.3: (a) Transconductance dI_{CS}/dV_{SG2} as a function of V_{SG2} and pulse amplitude for V_{SG2} in pulse measurements. 100 kHz pulse voltage is applied to V_{SG1} and V_{SG2}. V_{TG} = 1.8 V, V_D = 0 mV, V_S = 0 mV, V_{DCS} = 4 mV, and V_{SG3} = 0 V. (b) Schematic of electrochemical potentials at (5,1)-(4,2) charge configuration. In this configuration, it is predicted that there are singlet and triplet states and Pauli spin blockade occurs in the tunneling from S(5,1) to S(4,2) states.

On the other hand, the T state has three different is total *z*-projected momentum of 0, -1, and +1. The wavefunction of the spin component for the corresponding triplet states are expressed as $|T_0\rangle = \left(|\uparrow\downarrow\rangle + |\downarrow\uparrow\rangle\right)/\sqrt{2}$, $|T_-\rangle = |\downarrow\downarrow\rangle$, and $|T_+\rangle = |\uparrow\uparrow\rangle$. Figure 8.3 (b) shows schematic of electrochemical potentials at (5,1)-(4,2) charge configuration. In this configuration, it is predicted that there are singlet (S) and triplet (T) states and Pauli spin blockade occurs in the tunneling from (5,1) to (4,2) charge states because (5,1) charge state has odd number of electrons in each QD and can have T(5,1) triplet states. In the (5,1) region with completely separated from detuning 0 (detuning 0 means the resonance point between the (5,1) ground state and the (5,1) ground state), the S(5,1) state and T(5,1) state are almost degenerate each other at the zero magnetic field. The T(4,2) state has larger energy than the S(4,2) state with energy spacing of the singlet-triplet energy splitting ΔE_{ST}. When the state is S(5,1) the electron can tunnel to the S(4,2) state even if the detuning voltage is located on the spin blockade region. On the other hand, when the state is T(5,1) the electron cannot tunnel to the S(4,2) state on the spin blockade region.

Here we explain about the pulse voltage measurement in detail to understand figure 8.3(a). Figure 8.4 (a) shows schematics of charge sensing signal of the SET charge sensor without and with applied pulse voltage in time-averaged measurements. With no applied pulse voltage, the charge sensor current (I_{CS}) has one sharp variation (sharp inflection) at the position of side gate voltage (here V_{SG2}) for $N \leftrightarrow N+1$ electron transition in the QDs as described in section 4. When we apply pulse voltage to the side gate, the one sharp variation in I_{CS} splits into two sharp variations. Here we consider the situation that the tunneling rate is sufficiently faster than the pulse frequency. In the V_{SG2} region between these two sharp variations, the time-averaged charge state is $N+0.5$ with 50 % duty squire pulse because the N electron occupancy and $N+1$ electron occupancy is repeated with the same time period following applied pulse voltage. In this case the values of change in I_{CS} in these two sharp variations are identical each other. The V_{SG2} width between two sharp variations corresponds to the amplitude of the pulse voltage applied to side gate 2 (SG2). Figure 8.4(b) shows schematic of time evolution of spin states and charge states in the pulse voltage measurement. The transition between S(5,1) and T(5,1) states in the (5,1) charge state can occur through the spin-orbit interaction or hyperfine interaction [61]. The transition rates for S(5,1)→T(5,1) and S(5,1)→T(5,1) transition are predicted to be almost the same in the case of no applied external magnetic field. The (5,1)↔(4,2) charge transition occurs with synchronized to the applied pulse voltage if the Pauli spin blockade do not occur. Therefore if the spin state is the singlet, the charge transitions between S(5,1) and S(4,2) states occur. On the other hand, if the spin state is the triplet, the charge transition from T(5,1) to S(4,2) is blocked because of the Pauli spin blockade and the charge state stays in (5,1) charge

occupancy even if the pulse voltage is applied. The existence of time period for these unblocked and blocked charges transition change the time-averaged charge occupancy. Figure 8.5(a) shows schematic of charge sensing signal of the SET charge sensor in our pulse measurement. If no spin blockade occurs the time-averaged charge states between the two sharp variations is predicted to be the (5-0.5, 1+0.5) charge occupancy (i.e. (4.5, 1.5) charge occupancy). On the other hand, the existence of the Pauli spin blockade change the time-averaged charge occupancy to (5-x, 1+x) with $x < 0.5$, which means that the charge states is closer to (5,1) charge occupancy than to (4,2) charge occupancy. In addition, another sharp variations in I_{CS}, which is corresponds to T(5,1)→T(4,2) tunneling, appears because the T(5,1) state can tunnel into the T(4,2) states which is exited states in the (4,2) charge occupancy. In this case the values of change in I_{CS} in the three sharp variations in figure 8.5(a) are different each other and the most right one, which is corresponding to the S(4,2)→S(5,1) tunneling, is largest because $x < 0.5$. This is result in the strong signals of the transconductance dI_{CS}/dV_{SG2} in the left-hand transition line in figure 8.3(a). Figure 8.5(b) shows schematic of charge stability diagram as a function of side gate voltage V_{SG2} and pulse amplitude for V_{SG2} in our pulse measurement. The region of the Pauli spin blockade is surrounded by the charge transition lines for the S(5,1)→S(4,2) and T(5,1)→T(4,2) and the singlet-triplet energy splitting ΔE_{ST} in the (4,2) charge occupancy can be estimated by separation of these charge transition lines. In figure 8.3(a) we observed region of the Pauli spin blockade and estimated the singlet-triplet splitting energy $\Delta E_{ST} \sim 0.3$ meV using conversion factor between energy and the side-gate voltage.

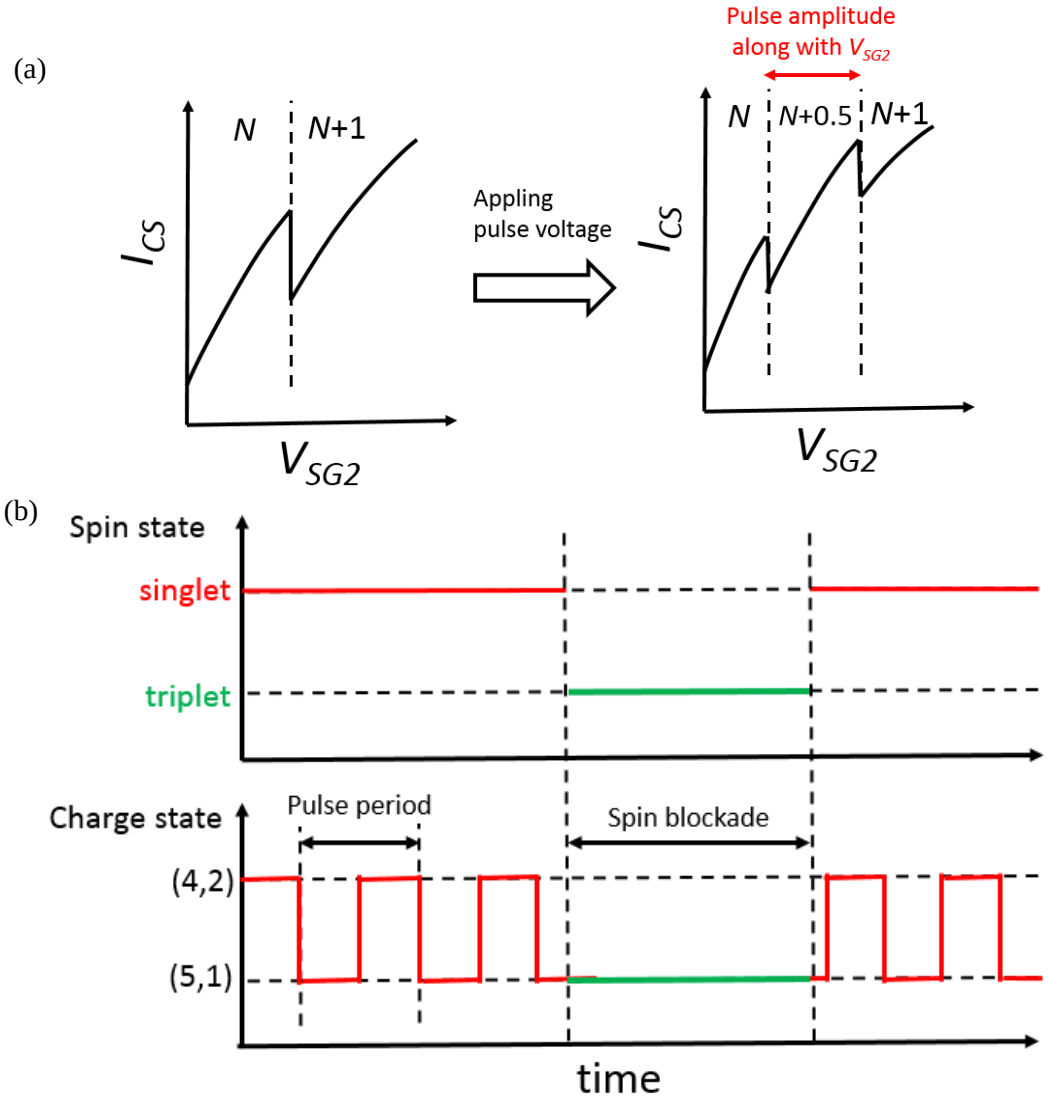


FIG. 8.4: (a) Schematic of charge sensing signal of the SET charge sensor without and with applied pulse voltage in time-averaged measurements. In the V_{SG2} region between these two sharp variations, the time-averaged charge state is N+0.5 with 50 % duty squire pulse because the N and N+1 electron occupancy is repeated with the same time period following applied pulse voltage. (b) Schematic of time evolution of spin states and charge states in the pulse voltage measurement. The existence of time period for these unblocked and blocked charge transition changes the time-averaged charge occupancy.

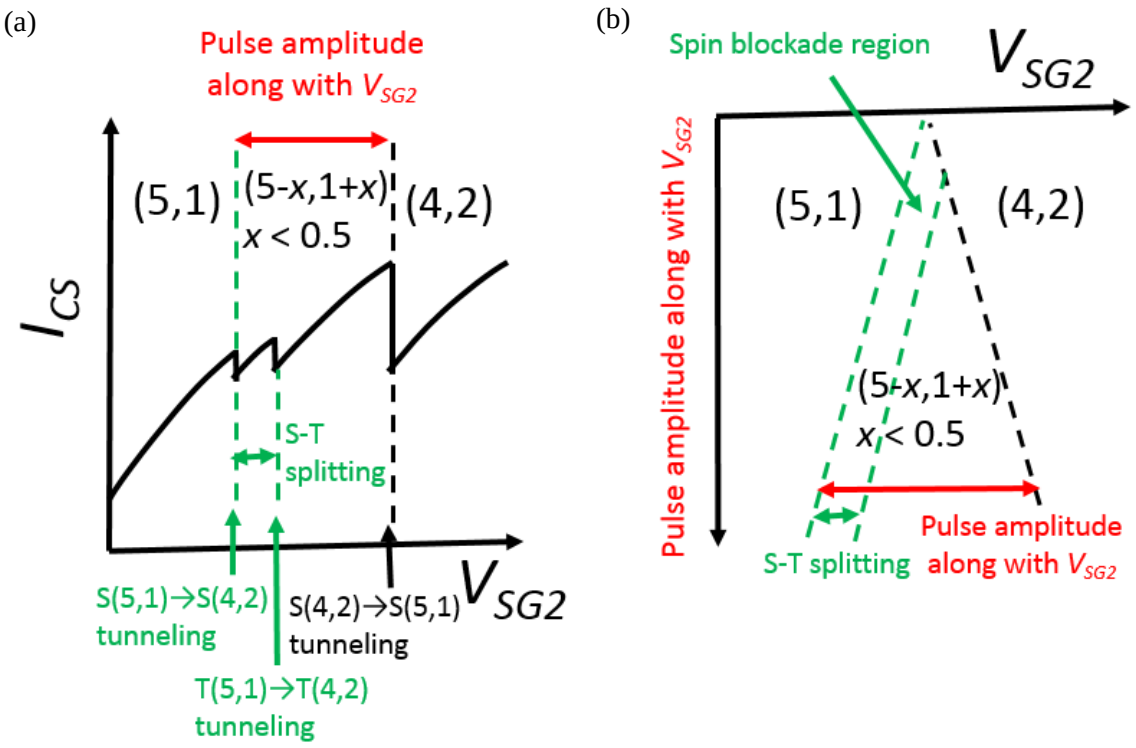


FIG. 8.5: (a) Schematic of charge sensing signal of the SET charge sensor in our pulse measurement. The existence of the Pauli spin blockade change the time-averaged charge occupancy to (5-x, 1+x) with x < 0.5 (b) Schematic of charge stability diagram as a function of side gate voltage V_{SG2} and pulse amplitude for V_{SG2} in our pulse measurement. The region of the Pauli spin blockade is surrounded by the charge transition lines for the S(5,1)→S(4,2) and T(5,1)→T(4,2). The singlet-triplet energy splitting ΔE_{ST} in the (4,2) charge occupancy can be estimated by separation of the S(5,1)→S(4,2) and T(5,1)→T(4,2) transition lines.

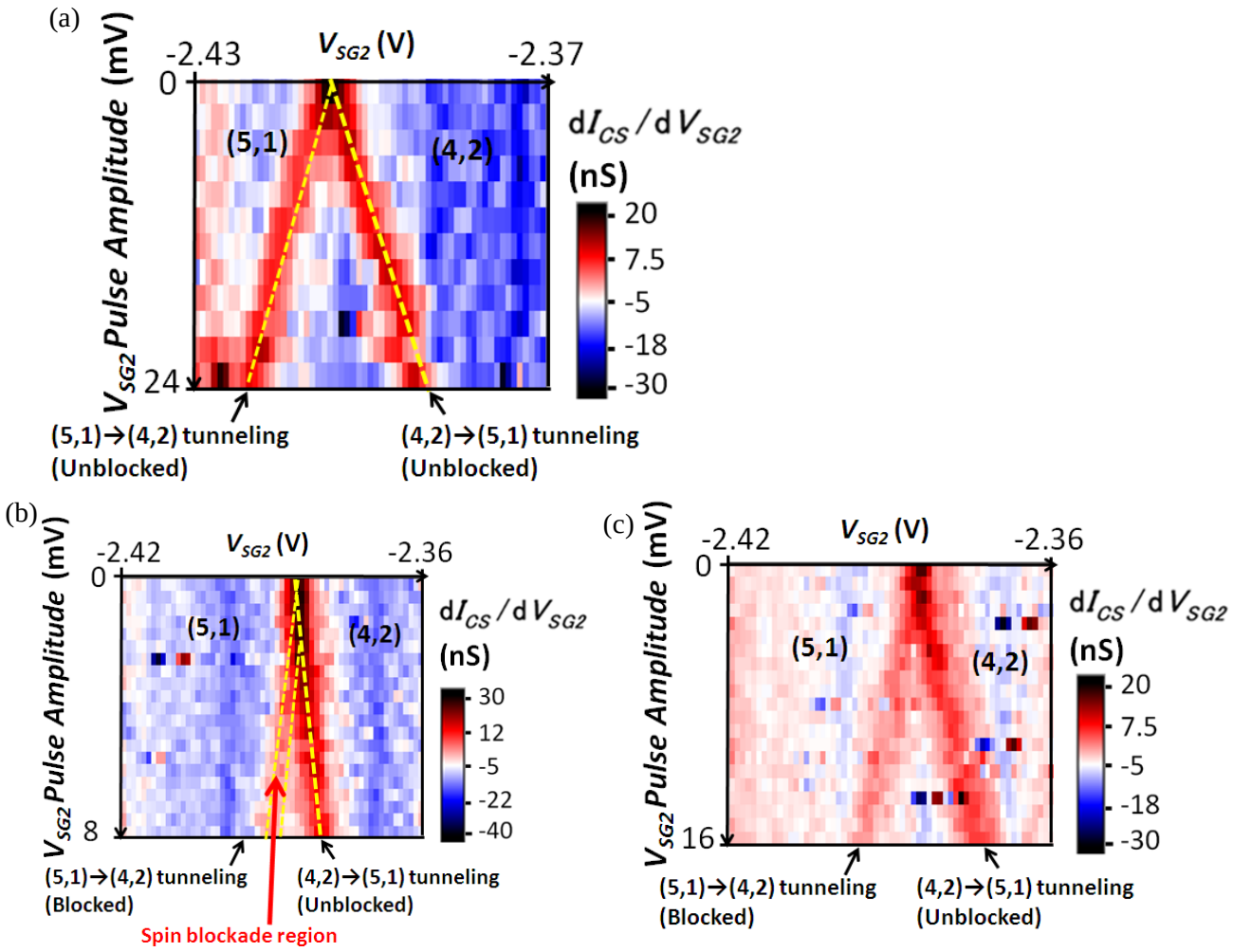


FIG. 8.6: (a) (b) (c) Transconductance dI_{CS}/dV_{SG2} as a function of V_{SG2} and pulse amplitude for V_{SG2} in pulse measurements. (a) 1 kHz, (b) 10 kHz, and (c) 5 kHz pulse voltage is applied to V_{SG1} and V_{SG2}. V_{TG} = 1.8 V, V_D = 0 mV, V_S = 0 mV, V_{DCS} = 4 mV, and V_{SG3} = 0 V.

Next we applied the pulse voltages with different frequency to estimate the relaxation time T_1 for (5,1) triplet states to (5,1) singlet relaxation process. In figure 8.4(b), if the relaxation time T_1 is shorter than the time scale of the pulse period, the Pauli spin blockade is no longer observed because the T(5,1) state can relax to S(5,1) within the pulse period. Therefore we can estimate T_1 by comparing signals of the Pauli spin blockade in the measurement using different pulse frequency. Figure 8.6(a), (b), and (c) show the results for 1kHz, 10kHz, 5kHz pulse measurements. In figure 8.6(a) (5,1)→(4,2) tunneling is visible, indicating the relaxation time T_1 for (5,1) triplet states to (5,1) singlet relaxation process is shorter than 1 ms. In the 10 kHz pulse

measurements the Pauli spin blockade is clearly observed, indicating T_1 is longer than 0.1 ms order. In the 5 kHz pulse measurements the blockade at (5,1)→(4,2) tunneling is slightly observed. Form these results we estimate T_1 is around 0.5 ms at the zero magnetic field. This value is relatively shorter than T_1 of 10 ms in a Si/SiGe heterostructure [23]. The results in Ref. 23 have been measured in S(1,1)-T(1,1) qubit and we conjecture the larger number of electron in our device cause electron spin-spin interaction and the relaxation time becomes shorter than that in Ref. [23]. After this measurements a charge trap near the (5,1)-(4,2) region prevent us from perform stable measurement and we cannot measure magnetic field dependence of the relaxation time.

8.4 Summary

We presented pulse measurements of the Pauli spin blockade in (5,1)-(4,2) charge states in a silicon DQD device. The relaxation time T_1 is estimated as 0.5 ms from frequency of the applied pulse. This value is relatively small compared to that in Si/SiGe heterostructure. We estimated the singlet-triplet splitting energy ΔE_{ST} ～0.3 meV. This measurement will be significant progress for achieving the single-shot measurement of spin stats and manipulation of singlet-triplet qubits.

Chapter 9

Conclusions

9.1 Introduction

We regard the exchange-only qubit system as the promising architecture for achieving the quantum computing. Our final goal is to achieve manipulation of the exchange-only qubit in the silicon device which have long coherence time of electron spin states.
In this work we fabricate lithographically-defined silicon QDs, which are presented. This device structure has great advantage for integration of QDs because the QDs formed by lithographically-defined physical shape of the structure and does not require gate contacts to create the confinement potential of the QD. Therefore it has high potential to possess complicated structures such as multiple QDs ant it has adaptability for the exchange-only qubit.
However this device structure has also many assignments to achieve and our purpose in this work is resolving these assignments.

We tackled the significant assignment to achieve the spin manipulation on our attractive device structure. Our work is listed in following.

①Charge sensing of the electron occupancy in QD using charge sensor
Charge sensing is significant for measurement of spin states. However we had not achieved the charge sensing in our attractive device structure.

②Achievement of forming few-electron regime of the single and double QDs

Observing the few-electron regime of QDs is essential to reduce unnecessary interactions between spins of electrons. Therefore this assignment is significant to achieve the spin manipulation.

③Obtaining the strategy for designing the SET charge sensor to improve the SNR of charge sensing signal by experiment and numerical calculations

There had not been the strategy for designing the SET charge sensor to improve the SNR. We focused on an advantage that the practical diameter of the QD and the SET can been seen from the SEM image of the device when the QD and the SET contain many electrons. Utilizing this advantage the capacitive parameters of the QD and the SET can be calculated and analyzed.

④Control of the tunnel coupling between QDs

Exchange coupling between tunnel-coupled QDs are strongly depends on the tunnel coupling between QDs. Therefore to achieve the spin manipulation using exchange coupling, controlling the tunnel coupling is required.

⑤Investigation for the back-action generated from charge sensor

The back-action destroys the coherence of the qubit and the revealing the strategy to reduce the back-action is significant.

⑥Observation of the spin blockade in the few-electron regime of the QDs using pulse voltage measurements

In the qubit measurements, single-shot measurements (i.e. time-resolved measurements) of the spin states using pulse measurements required to achieve qubit manipulation.

9.2 Charge sensing measurements and Observation of few-electron silicon quantum dots

We fabricated the device with a single QD and an SET charge sensor, and the charge sensing

signal is clearly observed for the first time in this device structure. We have improved our device fabrication process and realized measurements of the few-electron regime of single QD and double QD devices using charge sensing via an SET charge sensor. This is notable achievements for our attractive device structure.

9.3 Key capacitive parameters for designing single-electron transistor charge sensors

Twin silicon single QDs were fabricated using a lithographic process, and the electrostatic coupling between them was investigated. The dependence of the charge sensitivity on QD size was evaluated based on the charging energy. The measured electrostatic characteristics were found to be in good agreement with numerical calculations, and the key capacitive parameter determining the SNR was identified. Numerical calculations of the QD-SET coupling suggested that decreasing the SET diameter and the distance between the QD and the SET leads to an increase in the SNR for both dc and RF single-shot measurements. Because these results are independent of the device materials, they are useful for establishing guidelines for the design of SET charge sensors in lateral QD-SET structures based on a 2DEG.

9.4 Control of the tunnel coupling between quantum dots

Tunnel couplings on the tunnel barrier of the QDs could be controlled by tuning the gate voltages and this flexibility indicates that the lithographically-defined structure is acceptable for electron spin manipulation using the exchange interactions between QDs.

9.5 Back-action measurements in silicon quantum dots

We preformed SET induced back-action measurements in a silicon device with QDs and an SET charge sensor. We clearly observed the back-action-induced excitation of electrons from the ground singlet state to the excited triplet state in a QD with two-electron occupancy. Our measurements and fitted curves show that the back-action largely depends on the number of

phonons generated by the SET current. From this result we conjecture that the back-action is caused by photons generated from shot noise of the SET current. We also identified conditions that make possible both a desirable sensitivity for qubit readout and back-action-induced transition rates of less than 1 kHz.

9.6 Observation of the spin blockade in the few-electron regime of the QDs using pulse voltage measurements

We demonstrated pulse measurements of the Pauli spin blockade in (5,1)-(4,2) charge states in a silicon DQD device. The relaxation time T_1 is estimated as 0.5 ms from frequency of the applied pulse. This value is relatively small compared to T_1 of 10 ms in Si/SiGe heterostructure. This measurement will be significant progress for achieving the single-shot measurement of spin stats and manipulation of singlet-triplet qubits.

9.7 Summary and significance of this work

We achieved significant assignments in our device structure; Realizing the Charge sensing measurements, Observation of few-electron silicon quantum dots, Revealing the strategy for designing the SET charge sensor to improve the SNR of charge sensing signal by experiment and numerical calculations, Modulating the tunnel coupling between QDs, revealing the strategy to reduce the back-action, and pulse measurement of the Pauli spin blockade. These results will leads further developed measurements such as This device structure is close to that of conventional CMOS structures and has a very high potential for integration because confinement gates are not required. This will become a more significant advantage for practical application with expansion to more complicated structures.

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Acknowledgements

I would like to express the deepest appreciation to Prof. Shunri Oda and assistant Prof. Tetsuo Kodera for giving the opportunity and guidance of my research. I would like to express my gratitude to assistant Prof. Yukio Kawano and Prof. Ken Uchida (Keio University). I would like to offer my special thanks to Prof. Mutsuko Hatano, Prof. Yasuyuki Miyamoto, and Dr. Akira Fujiwara (NTT Basic Research Laboratories) for examining this thesis. I want to thank Dr. Ryuta Suzuki, Dr. Koichi Usami, and Prof. Toshiro Hiramoto (Tokyo University) for experimental assistance. I want to thank Secretary Ayumi Saito, Yoko Tashiro, Kaori Hashimoto, Yuko Unzai, and Jyunko Nakamura for great helps. I also want to thank the alumni and members of Oda Kawano laboratory, Taihei Hippo, Xin Zhou, Gento Yamahata, Yu Nagami, Jun Ogi, Muhamad Amin Sulthoni, Yoshifumi Nakamine, Berrin Pinar Algul, Jean L. Tarun, Tetsuya Isikawa, Masanori Fukada, Yohei Nagahama, Syogo Miyoshi, Hiroki Nikaido, Yunaki Takahashi, Naoki Kadotani, W. Lin, Tomohiro Kambara, Masao Koge, Kazuhiro Hikita, Daisuke Kobayashi, Marolop D. K. Simanullang, Sheng Jiun Chou, Ryotaro Kogure,Yusuke Sakka, Masayuki Saito, Yoshiharu Yanai, Hisashi Hayashi, Yuya Sakatoku, Norio Hosoda, Ken Someno, Yuji Fukuoka, Yuki Fukuda, Mr. Chin, Akihiro Naito, Tomotaka Sawada, Tei Zen, Takahiko Morita, Ryotaro Suzuki, Kenta Hirakata, Yorinobu Fuzino, Daichi Suzuki, Nobuyasu Beppu, Teruyuki Ohashi, Yu Doioka, Tomoya Syoji, GaNaa OU, Jun Kamioka, Takayoshi Kuga, Nobuhiro Kondo, Ko Yamada, Hiroyuki Ikuse, Yuhei Ozawa, Anis Boudraa (D3), Akhmdi Surawijaya (D3), Tomohiro Noguchi (D2), Raisei Mizakuchi (D1), Kazushi Ikemoto (M2), Satosi Ihara (M2), Yoshihiro Tamura (M2), Kengo Funaki (M2), Tomoyuki Hirano (M2), Koudai Morita (M2), Yi Lu (M2), K. zhang (M1), Alan Huynh (M1), Lu Shigong (M1), Mira Thoen Feiring (M1), Taneli Juntunen (M1), Naoki Fuzimura (M1), Takumu Honda (M1), Syotaro Yamazaki (M1), Ko Ishikawa (M1), Kazuma Iwasaki (M1), Takashi Iguchi (B4), Aiko Kunisaki (B4), Yusuke Shimamoto (B4), Soichiro Hiraoka (B4), Sho Hosoya (B4), Yu Yamaoka (B4), and Munehiko Yoshida (B4).

This work was financially supported by Kakenhi Grants-in-Aid (Nos. 24102703, 26709023, and 26630151), the PRESTO program of the Japan Science and Technology Agency (JST), the

Yazaki Memorial Foundation for Science and Technology, and the Project for Developing Innovation Systems of the Ministry of Education, Culture, Sports, Science and Technology (MEXT) of Japan.

Publications

(1) Journal

[1] Kosuke Horibe, Tetsuo Kodera, Tomohiro Kambara, Ken Uchida, and Shunri Oda, **"Key capacitive parameters for designing single-electron transistor charge sensors"**, Journal of Applied Physics, Vol. 111, pp. 093715 1-5, May 2012, (Peer-reviewed).

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(3) Domestic conference presentations

[1] Kosuke Horibe, Tetsuo Kodera, and Shunri Oda **"Observation of the spin blockade in a silicon double quantum dot using a charge sensor"**, JSAP 75th autumn meeting, (Oral), 2014, September, Hokkaido, Japan.

[2] Kosuke Horibe, Tetsuo Kodera, Yukio Kawano, and Shunri Oda **"Observation of the excitation of electrons in silicon quantum dots generated from the back-action of a charge sensor"**, JSAP 74th autumn meeting, (Oral), 2013, September, Kyoto, Japan.

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