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Doctoral Thesis

**A study of electrical interface
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based on mobility and
low-frequency noise characterizations**

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Abstract

In this thesis, the gate oxide/channel interface properties were experimentally and comprehensively investigated by carrier transport and low-frequency noise (LFN) characterizations in ultra-scaled nanowire (NW) MOSFETs. NW MOSFETs, which have aggressively downscaled cross-section of the body, are strong candidates for near future CMOS technology nodes. However, the interface quality could be a critical issue due to the NW body formed by etching process, the multiple surface orientations, the large surface/volume ratio, and additional strain technology to enhance the performance. The understanding of carrier transport and channel interface quality in NW MOSFETs with advanced high- κ /metal gate is thus particularly important and needs experimental and theoretical investigations. LFN provides deep insights into the interface properties in MOSFETs and the characterization has no lower limit of the necessary channel area. LFN measurement can be thus a powerful characterization technique for ultra-scaled NW MOSFETs. Also, extraction of fitting mobility (such as low-field mobility) by Y-function method is an efficient method for the evaluation of carrier transport in ultra-scaled FETs.

Our NW MOSFETs were fabricated from fully-depleted silicon-on-insulator (FD-SOI) substrate, and with Hf-based high- κ /metal gate stack (HfSiON/TiN) in order to reduce detrimental effects by device downscaling. In addition, strain technologies to the channel were additively processed to efficiently improve the MOSFET's performance. Tensile strained-SOI substrate was used for NMOS FETs, whereas compressive stressors were used for PMOS devices. Compressively strained Si channel was processed by raised SiGe S/D and CESL formations. In addition, strained SiGe channel was also fabricated for further high-performance PMOS FETs.

Firstly, the most common I_d - V_g characteristics were studied in single-channel Ω -gate NW MOSFETs to understand the basic performance. The reference SOI NWs successively provided the excellent static control down to short channel device with $L_g=17\text{nm}$. The stressors dramatically enhanced the on-current owing to a modification of the channel energy-band structure. Then, low-field mobility in single-channel NW devices was characterized and also demonstrated large improvement of the performance by stressors. L_g dependent mobility degradation was observed in NW devices as with planar MOSFETs, highlighting the specific behavior in NW architecture. The mobility

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extraction exhibits the effectiveness for MOSFET's performance evaluation even for ultra-scaled single-channel NW architecture.

The LFN investigation was effectively applied for the evaluation of various technological and architectural parameters. Carrier number fluctuations with correlated mobility fluctuations (CNF+CMF) model described the $1/f$ noise behavior in all our devices down to the shortest and narrowest NW MOSFET. The drain current noise behavior was basically similar in both N- and PMOS devices regardless of device technological splits. Larger $1/f$ noise stemming from S/D regions in PMOS devices was perfectly interpreted by the CNF+CMF model completed with a term of R_{SD} fluctuations. This observation highlighted an advantage of SGOI NW with the lowest level of S/D region noise.

Geometrical variations with W_{top} and L_g altered the CNF component, the flat-band voltage noise S_{Vfb} , with simple impact of device scaling (reciprocal to both W_{tot} and L_g). No significant impact of surface orientation difference between the channel (100) top and (110) side-walls was observed. The scaling regularity with both W_{tot} and L_g , without quantum confinement, could be attributed to the use of HfSiON/TiN gate stack and the carrier transport occurring mostly in 2D surfaces of top and side-walls even in NW geometry. Meanwhile, the CMF factor, Coulomb scattering parameter $\alpha_{sc}\mu_{eff}$, was not altered by decreasing dimensions or 3D structure impacts, while the mobility strongly depends on the impacts.

Extracted oxide trap density N_t was roughly steady with scaling, architecture, and technological parameter impacts. Simple separation method of the contributions between channel top surface and side-walls was demonstrated in order to evaluate the difference. It revealed that the oxide quality on (100) top and on (110) side-walls was roughly comparable in all the [110]-oriented devices. The N_t values lie in similar order as the recently reported data. Consequently, an excellent quality of the interface with HfSiON/TiN gate stack was sustained for all our technological and geometrical splits.

Finally, the both strained and unstrained NWs fulfilled the $1/f$ LFN requirements stated in the ITRS in 2013 for future CMOS logic node with MG FETs. Consequently, we concluded that the appropriate strain technologies powerfully provide improvement of both carrier transport and $1/f$ LFN properties for future CMOS circuits consisting of NW FETs, without a significant concern about the oxide/channel interface quality.

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*To my family
for everything to date*

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List of Symbols, Acronyms, and Abbreviations

Symbol	Unit	Meaning
C_{acc}	F (F/cm ²)	Accumulation layer capacitance (per channel area)
C_{BOX}	F (F/cm ²)	Buried-oxide capacitance
C_{dep}	F (F/cm ²)	Depletion layer capacitance
C_{gb}	F (F/cm ²)	Gate-to-body capacitance
C_{gc}	F (F/cm ²)	Gate-to-channel capacitance
C_{in}	F	Input capacitance
C_{inv}	F (F/cm ²)	Inversion layer capacitance
C_{it}	F (F/cm ²)	Capacitance of interfacial traps
C_{it_BOX}	F (F/cm ²)	Capacitance of traps at Si/BOX interface
C_{load}	F	Total load capacitance
C_{out}	F	Output capacitance
C_{ox}	F (F/cm ²)	Gate oxide capacitance
C_{tot}	F (F/cm ²)	Total capacitance
C_{wire}	F	Wiring capacitance
D_{it}	eV ⁻¹ cm ⁻²	Density of interface traps
E_C	eV	Conduction band edge energy
E_{eff}	V/cm	Effective electric field
E_F	eV	Fermi level
E_i	eV	Intrinsic Fermi level
E_V	eV	Valence band edge energy
f	Hz	Frequency (operating frequency = clock frequency)
f_{max}	Hz	Maximum operating frequency
f_p	Hz	Frequency of pulse signal in CP technique
g_m	S	Transconductance
h	Js	Planck's constant ($=6.626 \times 10^{-34}$)
H_{NW}	cm	Channel height of nanowire
I	A	Current
I_{CP}	A	Maximum charge pumping current
I_d	A (μA/μm)	Drain current (normalized by channel width)
I_{d_lin}	A	Drain current in linear region
I_{d_sat}	A	Drain current in saturation region
I_{d_sub}	A	Drain current in subthreshold region
I_{leak}	A	Off-state leakage current
I_{ON}	A (μA/μm)	On-state drain current
I_{ox}	A	Leakage current due to gate oxide tunneling
I_{sat}	A (μA/μm)	Saturated on-current in short channel devices
I_{sc}	A	Direct short-circuit current
I_{sub}	A	Subthreshold leakage current
$I(t)$	A	Time dependent fluctuating current
$i(t)$	A	Randomly fluctuating component of current
k	J/K	Boltzmann's constant ($=1.38 \times 10^{-23}$)
K		Proportional constant
L	cm	Channel length
L_g	cm	Gate length
m		Body-effect coefficient
m^*	g	Carrier effective mass

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Symbol	Unit	Meaning
n	cm^{-2}	Electron density
n		Effective number of gate
N		Number of conducting carriers
N_A	cm^{-2}	Acceptor (hole) doping density
N_{ch}		Number of parallel channel finger
n_i	cm^{-3}	Intrinsic carrier density in the substrate
N_{inv}	cm^{-2}	Inversion carrier density
N_t	$\text{eV}^{-1}\text{cm}^{-3}$	Oxide trap density
$N_{t_side-walls}$	$\text{eV}^{-1}\text{cm}^{-3}$	Oxide trap density in the channel side-walls
N_{t_top}	$\text{eV}^{-1}\text{cm}^{-3}$	Oxide trap density in the channel top
p	cm^{-2}	Hole density in the substrate
P_{all}	W	Overall power consumption
P_{sc}	W	Direct short-circuit power consumption
P_{st}	W	Static power consumption
P_{sw}	W	Dynamic switching power consumption
q	C	Elementary charge ($=1.602 \times 10^{-19}$)
Q_{dep}	C/cm^2	Depletion charge density
Q_{inv}	C/cm^2	Inversion charge density
Q_{ox}	C/cm^2	Oxide charge density
R	Ω	Resistance
$R(s)$		Autocorrelation function
R_{SD}	Ω	Source/drain series resistance
$S(f)$		Power spectral density
S_I	A^2/Hz	Power spectral density of current noise
S_{Id}	A^2/Hz	Power spectral density of the drain current noise
S_R	Ω^2/Hz	Power spectral density of the resistance fluctuations
$S_{R_{\text{sd}}}$	Ω^2/Hz	Power spectral density of the R_{SD} fluctuations
S_V	V^2/Hz	Power spectral density of voltage noise
$S_{V_{\text{fb}}}$	V^2/Hz	Power spectral density of the flat-band voltage noise
S_{V_g}	V^2/Hz	Power spectral density of the gate voltage noise
t	s	Time
T	K	Absolute temperature
$T_{\text{high-k}}$	cm	High- κ gate dielectric thickness
T_{ox}	cm	Gate oxide (insulator) thickness
t_{sc}	s	Duration of direct short-circuit
T_{Si}	cm	Si film thickness
T_{SiO_2}	cm	Gate silicon dioxide thickness
t_{sw}	s	Duration of switching
V	V	Voltage
V_{base}	V	Base level of gate voltage pulse in CP technique
V_{ch}	V	Potential along the channel
V_d	V	Drain (-to-source) voltage
V_{dd}	V	Power supply voltage
V_{d_lin}	V	Drain voltage in linear region
V_{d_sat}	V	Drain voltage in saturation region
V_{fb}	V	Flat-band voltage

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Symbol	Unit	Meaning
V_g	V	Gate voltage
V_{gt}	V	Gate voltage overdrive ($= V_g - V_t $)
V_{in}	V	Input voltage
v_{inj}	cm/s	Injection velocity of carriers
v_{lim}	cm/s	Limiting velocity of carriers
V_{out}	V	Output voltage
v_{sat}	cm/s	Saturation velocity of carries
V_t	V	Threshold voltage
V_{t_lin}	V	Threshold voltage in linear region
V_{t_sat}	V	Threshold voltage in saturation region
W	cm	Channel width
W_{dep}	cm	Depletion layer width
W_{Si}	cm	Si body width
W_{top}	cm	Top-view channel width
W_{tot}	cm	Total effective channel width
$x(t)$		Variable in time domain
$X(f)$		Fourier-transformed variable in frequency domain
z	cm	Oxide trap location from the channel interface
ΔE	J, eV	Energy splitting
ΔE_{g_Si}	eV	Band gap energy of Si ($=1.12$)
Δf	Hz	Loss of operating frequency by DIBL effect
ΔI	A	Difference between two current levels in RTS
ΔI_d	A	Fluctuating (AC) component of drain current
ΔN^2		Variance of the fluctuating number of carriers
ΔV_g	V	Constant amplitude of trapezoidal gate voltage pulse in CP technique
α		Generalized scaling factor of electric field
α_H		Hooge parameter
α_{sc}	Vs/C	Coulomb scattering coefficient
α_{sw}		Switching activity rate
α_μ	nmVs/cm ²	Mobility degradation factor
β		Proportionality constant
β_0	$\mu A/V^2$	Transistor (transconductance) gain
γ		Frequency or temperature exponent
δQ_{ox}		Fluctuation of oxide charge
δV_{fb}		Fluctuation of flat-band voltage
$\delta \mu_{eff}$		Fluctuation of carrier effective mobility
ϵ_0	F/cm	Permittivity in vacuum ($=8.854 \times 10^{-10}$)
ϵ_{ox}		Relative permittivity of gate oxide
ϵ_{Si}		Relative permittivity of silicon ($=12$)
ϵ_{SiO2}		Relative permittivity of silicon dioxide ($=3.9$)
ϵ_{high-k}		Relative permittivity of high- κ dielectric
ζ		Current exponent in 1/f noise definition

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Symbol	Unit	Meaning
η		Empirical parameter for E_{eff} definition
κ		Scaling factor of MOSFET or chip size
λ	cm	Attenuation length of carrier wave function in oxide
λ_n	cm	Natural length (parameter with respect to SCE)
μ_0	cm^2/Vs	Low-field mobility
μ_C	cm^2/Vs	Mobility limited by Coulomb scattering
μ_{const}	cm^2/Vs	Assumed constant mobility along the channel
μ_{eff}	cm^2/Vs	Effective mobility
μ_{max}	cm^2/Vs	Peak mobility
μ_n	cm^2/Vs	Electron mobility
μ_p	cm^2/Vs	Mobility limited by phonon scattering
μ_{sat}	cm^2/Vs	Effective mobility in saturation region
$\mu_{\text{side-wall}}$	cm^2/Vs	Effective mobility in the channel side-walls
μ_{SR}	cm^2/Vs	Mobility limited by surface roughness scattering
μ_{TG}	cm^2/Vs	Effective mobility in tri-gate nanowire devices
μ_{top}	cm^2/Vs	Effective mobility in the channel top
μ_Y	cm^2/Vs	Mobility approximated by Y-function method
π_L	Pa^{-1}	Longitudinal piezoresistive coefficient
$\theta_1, \theta_{1.0}$	V^{-1}	First order mobility attenuation factor
θ_2	V^{-1}	Second order mobility attenuation factor
ρ	C/cm^2	Local charge density
ρ_{SD}	$\Omega\mu\text{m}$	Source-drain series resistivity
σ	S/cm	Conductivity
σ_{stress}	Pa	Applied stress in the longitudinal direction
τ	s	Time constant of carrier transitions
τ_0	s	Time constant based on SRH process (often $=10^{-10}$)
τ_h	s	Duration for higher current state in RTS
τ_l	s	Duration for lower current state in RTS
τ_{phonon}	s	Relaxation time due to intervalley phonon scattering
τ_{trap}	s	Relaxation time due to intervalley phonon scattering
ϕ_{ms}	eV	Work function difference between gate and channel materials
Φ_B	eV	Tunneling energy barrier height
Ψ_B	V	Difference between E_F and E_i potentials ($= E_F - E_i /q$)
Ψ_{Bp}	V	Ψ_B in p-type substrate (NMOS)
Ψ_S	V	Surface potential (band bending of substrate)
3PNMS		Programmable Point Probe Noise Measuring System
AC		Alternate current
ALD		Atomic layer deposition
BEOL		Back-end of line
BOX	cm	Buried oxide
CESL		Contact etch stop layer
CMF		Correlated mobility fluctuations
CMOS		Complementary metal-oxide-semiconductor

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Symbol	Unit	Meaning
CNF		Carrier number fluctuations
C-V		Capacitance-voltage
CVD		Chemical vapor deposition
DC		Direct current
DG		Double gate
DIBL	mV/V	Drain induced barrier lowering
DUT		Device-under-test
DUV		Deep ultraviolet
e-beam		Electron beam
CMP		Chemical mechanical polishing
CP		Charge pumping
EOT	cm	Equivalent oxide thickness
FD		Fully depleted
FET		Field-effect transistor
GAA		Gate-all-around
g-r		Generation-recombination
high- κ		High dielectric constant (permittivity)
HDD		Highly doped drain
HH		Heavy holes
HP		High performance
IC		Integrated circuit
IL		Interfacial layer
ITRS		International Technology Roadmap for Semiconductors
LCR		Inductance (L) - capacitance (C) - resistance (R)
LDD		Lightly doped drain
LFN		Low frequency noise
LH		Light holes
LNA		Low noise amplifier
LSTP		Low standby power
MF		Mobility fluctuations
MG		Multi-gate
MOSFET		Metal-oxide-semiconductor field-effect transistor
NMOS		N-channel MOS
NW		Nanowire
PBA		Programmable biasing amplifier
PD		Partially depleted
PDP	J	Power-delay product
PMOS		P-channel MOS
poly-		Polycrystalline
PR		Piezoresistance
PSD		Power spectral density
QM		Quantum-mechanical
RF		Radio frequency
RTS		Random-telegraph-signal
SCE		Short-channel effects
S/D		Source and drain

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Symbol	Unit	Meaning
SEM		Scanning electron microscopy
SGOI		SiGe-on-insulator
SOI		Silicon-on-insulator
SRB		Strained-relaxed buffer
SS	mV/dec	Subthreshold swing
sSi		Strained-Si
sSOI		Strained-Si-on-insulator
TEM		Transmission electron microscopy
Tri-gate (TG)		Triple-gate
Ω -gate (Ω G)		Omega-gate
Π -gate		Pi-gate

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Introduction

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1.1 MOSFET downscaling

Metal-oxide-semiconductor field-effect transistor (MOSFET) is the core technology of today's microelectronics. MOSFETs are mainly used as switches in logic microcircuits, and the devices can also fulfill other purposes. A modern microprocessor can contain more than 7 billion MOSFETs. Moreover, 128-gigabyte memory card contains 1024 billion (over 1 trillion) MOSFETs, while the card only weighs approximately 0.4g. 1 trillion is comparable to the number of fixed stars in the Andromeda Galaxy, which is the largest galaxy in the local group of galaxies included the Milky Way Galaxy, the solar system, and the earth where we live.

The concept of MOSFET was first invented around 1925-30 by Julius Lilienfeld [1-1,1-2]. After the development of point-contact transistor in 1947 by William Shockley, John Bardeen, and Walter Brattain [1-3], Martin Atalla and Dawon Kahng developed first MOSFET in 1959 [1-4]. The MOSFET technology was combined with the invention of integrated circuit (IC) in 1958 by Jack Kilby (and also by Robert Noyce) [1-5,1-6], and the growth has been accelerated and continued over 50 years up to the present days. The huge growth of semiconductor industry mainly based on silicon devices has lead to the miniaturization, the price drop, and the performance enhancement for lots of appliances and multimedia applications, such as computers and mobile phones.

1.1.1 Moore's law

In 1965, Gordon Moore published a paper [1-7], in which he predicted that density of MOSFETs on a chip would increase twice every 18 months. Although this “Moore's law” is empirically based on data within only 6 years between 1959 when the first Si IC was fabricated and 1965, the law has held amazingly up to the present, over 45 years (Fig.1-1). This clearly means that size reduction of MOSFETs allows increase of the density in an IC chip. The circuit capability thus increases for a constant chip size. However, there are other motivations for downscaling of MOSFET size. Double increase of MOSFETs density in a chip provides reduction of the chip dimensions,

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which are the length and width, divided by $2^{1/2}$. This scaling rate is usually represented as a factor of κ . In 1974, Dennard *et al.* published a paper [1-8], and he expressed the scaling benefits. Based on the ideal supposition for maintaining a constant electric field inside the MOSFET, device scaling by the factor κ (*i.e.* twice the integration density) increases the switching speed by κ and reduces the power dissipation by κ^2 . Table 1-1 shows the scaling MOSFET and circuit parameters under the constant field scaling and the generalized scaling rules [1-9]. The generalized scaling rule assumes that the electric field intensity changes by a factor of α . Dennard's law was suitable for the chip scaling until around 2005. After, the conventional scaling ended, and the performance enhancement originating from the device scaling, such as microprocessor clock frequency, has been saturated. This performance saturation has been caused by short-channel effects (SCE), which appeared in MOSFETs with aggressively shortened distance between the source and drain regions. Unfortunately, it is anticipated that SCE becomes more salient as the length is downscaled.

Table 1-1. Scaling MOSFET device and circuit parameters [1-9].

	MOSFET device and circuit parameters	Multiplicative factor ($\kappa > 1$)		
		Constant-field scaling	Generalized scaling	
			Long Ch.	Short Ch.
Scaling assumptions	Device dimensions (t_{ox} , W , L)	$1/\kappa$	$1/\kappa$	
	Doping concentration (N_A , N_D)	κ	$\alpha\kappa$	
	Voltage (V)	$1/\kappa$	α/κ	
Derived scaling behavior of device parameters	Electric field (E)	1	α	
	Carrier velocity (v)	1	α	1
	Depletion-layer width (W_{dep})	$1/\kappa$	$1/\kappa$	
	Capacitance ($C = \epsilon A/t$)	$1/\kappa$	$1/\kappa$	
	Inversion-layer charge density (Q_{inv})	1	α	
	Drift current (I)	$1/\kappa$	α^2/κ	α/κ
	Channel resistance (R_{ch})	1	$1/\alpha$	1
Derived scaling behavior of circuit parameters	Circuit delay time ($\tau \sim CV/I$)	$1/\kappa$	$1/\alpha\kappa$	$1/\kappa$
	Power dissipation per circuit ($P \sim VI$)	$1/\kappa^2$	α^3/κ^2	α^2/κ^2
	Power-delay product per circuit ($P\tau$)	$1/\kappa^3$	α^2/κ^3	
	Circuit density ($\sim 1/A$)	κ^2	κ^2	
	Power density (P/A)	1	α^3	α^2

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As shown in Fig.1-1 [1-10], minimum feature size of MOSFETs, which corresponds to the gate length, has been downscaled from 10 μ m down to 28nm (yellow circles; right y axis) between 1970 and 2011. In parallel, the number of MOSFETs per square millimeter (mm⁻²) increased from 200 to over 1 million (other objects show data for the four main microprocessor manufacturers; left y axis). The gate length in the current MOSFET generation lies between 22nm and 17nm. In practice, the distance between the source and the drain is approximately 50% shorter than the gate length, resulting in an effective channel length of only ~10nm. It is predicted that the effective channel length will approach about 5nm in 2020, which is only ten-fold size of the lattice parameter of a silicon crystal.

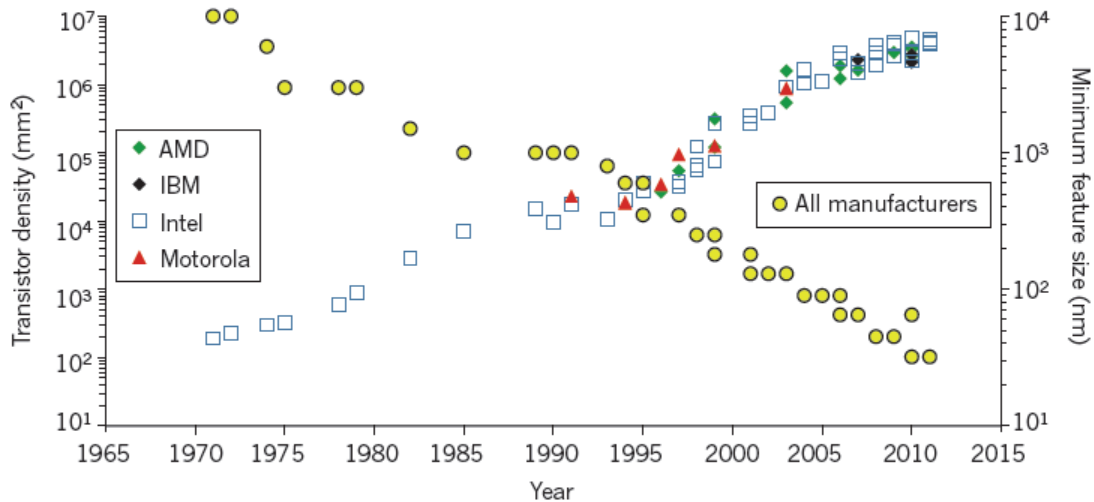


Fig. 1-1. The evolution of MOSFET minimum feature size (gate length) and the density of MOSFETs in microprocessors over time [1-10].

1.1.2 Power consumption of CMOS logic circuits

The most basic component of digital logic microcircuits is a complementary-MOS (CMOS) inverter as a switch. The CMOS configuration was first invented in 1963 by Frank Wanlass [1-11,1-12]. It consists of a symmetrical pairs of two types of MOSFETs, which are an n-channel MOSFET (NMOS FET) and a p-channel MOSFET (PMOS FET), as shown in Fig.1-2a. The source terminal of the NMOS FET is grounded, while the supply voltage V_{dd} is applied to the PMOS FET source. The gates of both MOSFETs

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are connected and common signal is input to the gates. The drains are also connected as the output node. The C_{load} is the total load capacitance including the output capacitance C_{out} , the input capacitance C_{in} , and the wiring capacitance C_{wire} .

The current through the PMOS FET (I_P) flows from the source into the drain and charges up the output voltage to V_{dd} (pull-up), meanwhile the current through the NMOS FET (I_N) flows from the drain into the grounded source and discharges the output voltage to zero (pull-down), as shown in Fig.1-2b and c. In CMOS system, the complementary essence allows only one of the MOSFETs to be switched-on (*i.e.* one FET of the pair is always switched-off). In principle, the power dissipation thus occurs only during momentary switching when the charging or discharging current flows through the inverter. Therefore, CMOS system dissipates significantly less static power and has higher noise immunity than other logic circuits with resistive loads, such as transistor-transistor logic (TTL) and NMOS logic. Moreover, CMOS process allows a high-density integration of logic functions on an IC. Since these advantages have been efficiently improved, the huge majority of modern IC manufacturing is based on CMOS processes.

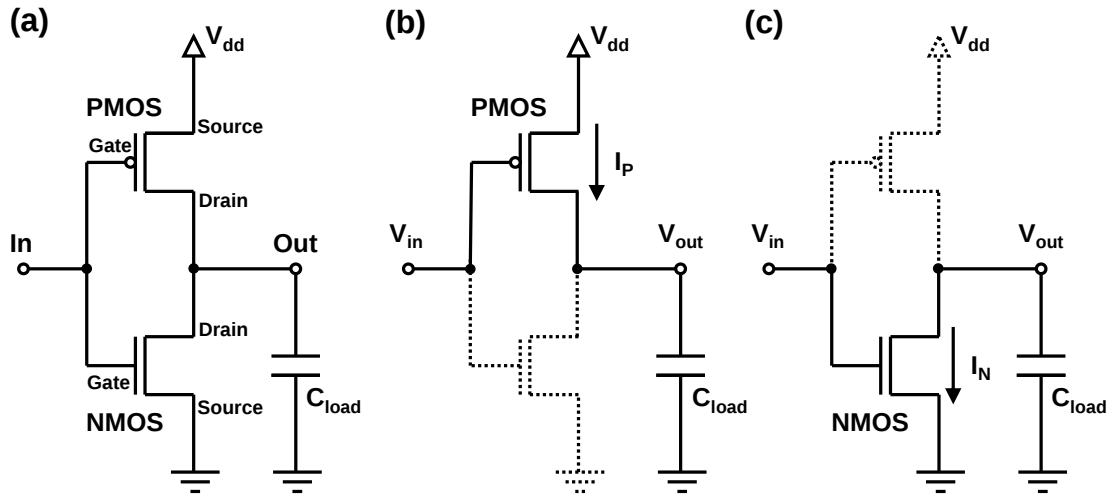


Fig. 1-2. (a) Circuit schematic of CMOS inverter. Equivalent circuits of (b) pull-up and (c) pull-down conditions.

Overall power consumption P_{all} in a CMOS logic IC is defined by the sum of dynamic switching power P_{sw} , direct short-circuit power P_{sc} , and static power P_{st} as

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[1-13,1-14]:

$$P_{all} = P_{sw} + P_{sc} + P_{st} \quad (1-1)$$

$$\text{with } P_{sw} = \alpha_{sw} C_{load} V_{dd}^2 f \quad (1-2)$$

$$P_{sc} = \alpha_{sw} t_{sc} I_{sc} V_{dd} f \quad (1-3)$$

$$P_{st} = (1 - \alpha_{sw}) \cdot I_{leak} V_{dd} = (1 - \alpha_{sw}) \cdot (I_{sub} + I_{ox}) \cdot V_{dd} \quad (1-4)$$

where α_{sw} is the switching activity rate, f is the operating frequency (clock frequency), t_{sc} is the required short-circuit time, I_{sc} is the short-circuit current flowing directly from the V_{dd} line to the ground line, and I_{leak} is the off-state leakage current. The I_{leak} is divided into two components: the subthreshold leakage current I_{sub} and the tunneling current in the gate oxide I_{ox} . Generally, the power consumption P_{all} is dominated by the dynamic component P_{sw} and is reduced by the scaling factor κ^2 . Furthermore, the average energy consumed per switching operation can be reduced by κ^3 . The average switching energy, also known as the power-delay product (PDP), is a figure of merit about energy efficiency in logic circuits. It is the product of dynamic power consumption and duration of the switching t_{sw} ($=1/f$), thus the PDP is expressed as:

$$PDP = P_{sw} t_{sw} = \frac{P_{sw}}{\alpha_{sw} f} = C_{load} V_{dd}^2 \quad (1-5)$$

As mentioned above, the P_{st} leakage is negligible in theory since CMOS circuits dissipate power only during switching, and it is the primary advantage of CMOS system. In practice, however, the continuing MOSFET scaling and the resulting circuit density growth has recently caused an unacceptable level of the P_{st} . Figure 1-3 shows the power consumption trends in CMOS logic IC chips [1-14]. As the size of MOSFETs is decreased with each advanced process technology, the clock frequency of CMOS circuits is increased. As a result, the dynamic switching power P_{sw} has been increased year by year. On the other hand, the static power consumption P_{st} , which is the sum of the subthreshold leakage and the gate oxide leakage components, is exponentially increased by shortening the gate length of MOSFET. Particularly, the P_{st} exceeds the P_{sw} after 2005 in the prediction. Therefore, reduction of the P_{st} has been a major challenge for recent CMOS technology node.

Increase of the I_{sub} is mainly due to short-channel effects (SCE). Meanwhile I_{ox} is

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increased owing to the aggressively scaled gate oxide thickness for enhancement of the electrostatic gate control. This gate oxide leakage can be reduced by replacing the conventional gate insulator, silicon dioxide (SiO_2), with materials with higher dielectric constant (high- κ). For the issue of I_{sub} increase, change of the gate architecture has been proposed in order to effectively enhance the electrostatic gate control.

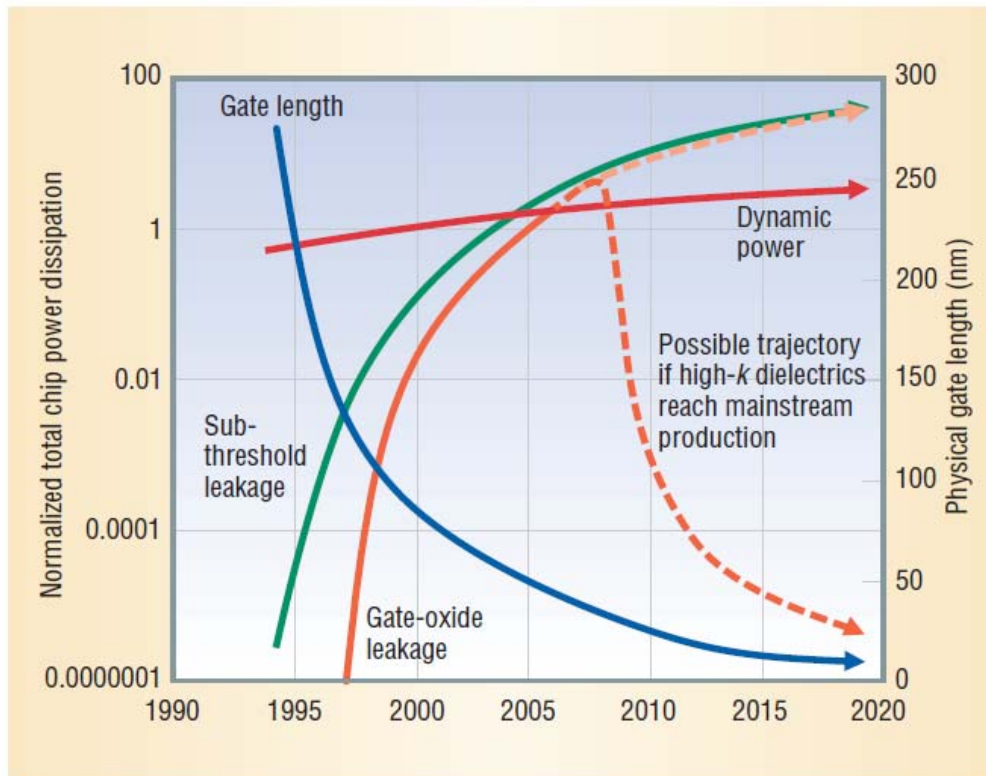


Fig. 1-3. Total chip dynamic and static power dissipation trends based on the International Technology Roadmap for Semiconductors. [1-14].

1.1.3 End of scaling era?

Unfortunately, MOSFETs are thus not perfect switches. The off-current is not zero, the on-current is limited by semiconductor resistance, and the switching takes longer time. Moreover, the switching does not occur suddenly at exact gate voltage bias but needs some voltage range and the gradual change. Furthermore, the switching behavior and the leakage power consumption are degraded by SCE as the size of MOSFET is downscaled, and it has been a serious issue for recent and future technology nodes.

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For continuous MOSFET downscaling *i.e.* the performance enhancement, huge efforts have been actually made to solve various issues mainly stemming from SCE. For instance, recent MOSFET structures released by Intel are shown in Fig.1-4 [1-15]. Some solutions to overcome the deterioration of the switching properties have been considered by using novel technologies, such as silicon-on-insulator (SOI) substrate [1-16,1-17] (Fig.1-5 [1-18]) and 3D multi-gate (MG) structures [1-10] (such as Tri-Gate device in Fig.1-4). For further performance improvement, solutions to the resolution limit of optical lithography, alternative oxide/metal gate, and high-performance channel materials have been also investigated as well.

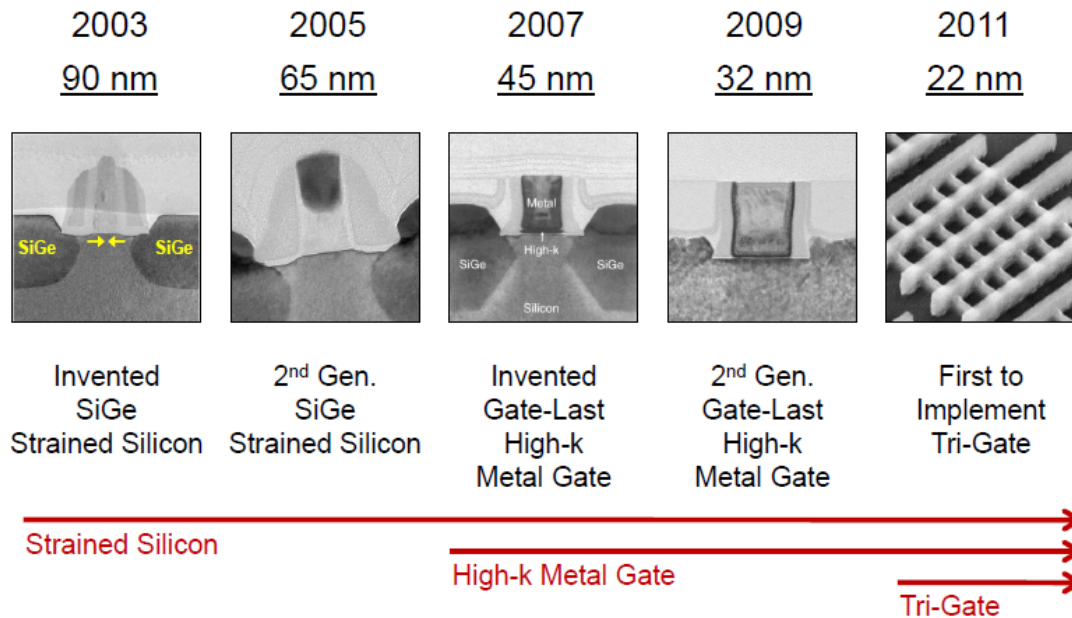


Fig. 1-4. Recent MOSFET architectures and process nodes released by Intel Corporation [1-15].

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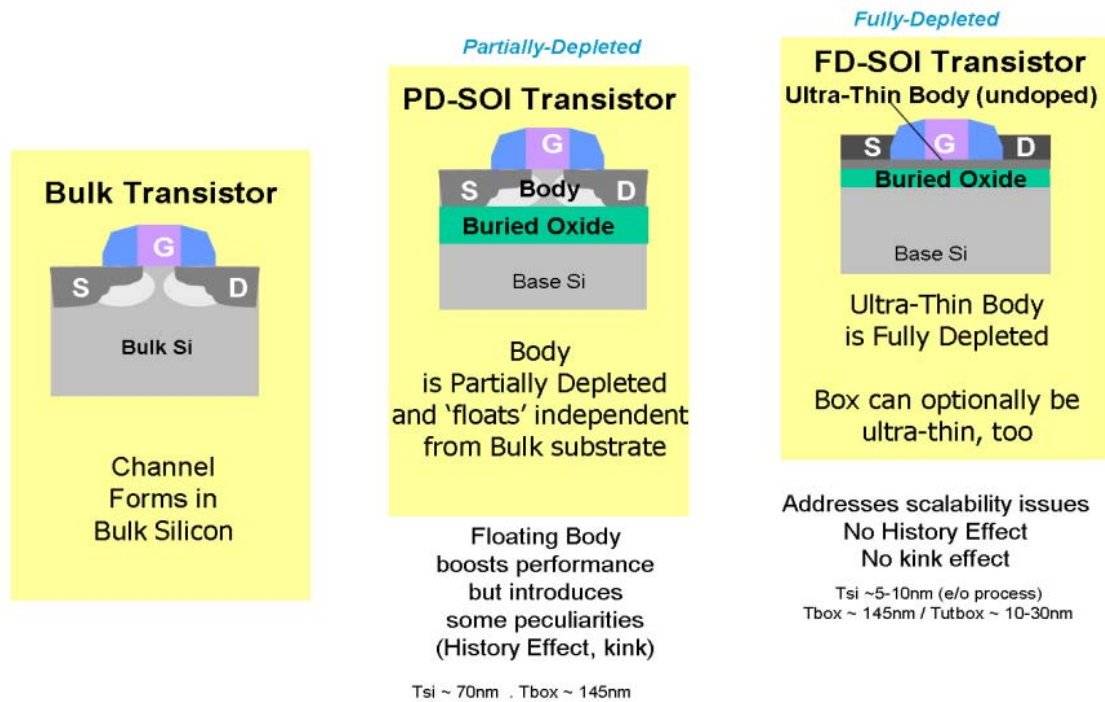


Fig. 1-5. Schematic of MOSFET structure based on silicon-on-insulator (SOI) technology [1-18].

Figure 1-6 shows the schematic of future device technology as reported by the international technology roadmap for semiconductors (ITRS) in 2011 [1-19]. The gate-stack, composed of high- κ dielectric/metal gate materials instead of SiO_2 /Poly-Si, has been practically introduced from the 45nm process node in 2007 by Intel (Fig.1-4). This technology is going to be maintained and the materials will be further optimized to obtain better gate control and lower gate leakage current I_{ox} . For high-speed operating devices, strained Si channel exhibiting higher carrier mobility has been intensively investigated. Moreover, substitute materials, such as Ge and III-V compounds, have been also studied to achieve much higher mobility. As mentioned above, SOI and MG technologies have been proposed to improve electrostatic control by the gate and strongly reduce the SCE (*i.e.* I_{sub}). First commercial MG MOSFET was released in 2011 by Intel, using the structure of a bulk FinFET [1-20] (Fig.1-4). For the next device generation, MG with extremely shrunk body (nanowire) on bulk or SOI substrates has been intensively expected. The gate length of MOSFET should become sub-10nm within 10 years, and approach 6-7nm in 2026. It is awaited that performance requirements

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could be achieved by MG architectures (Fig.1-7) [1-21].

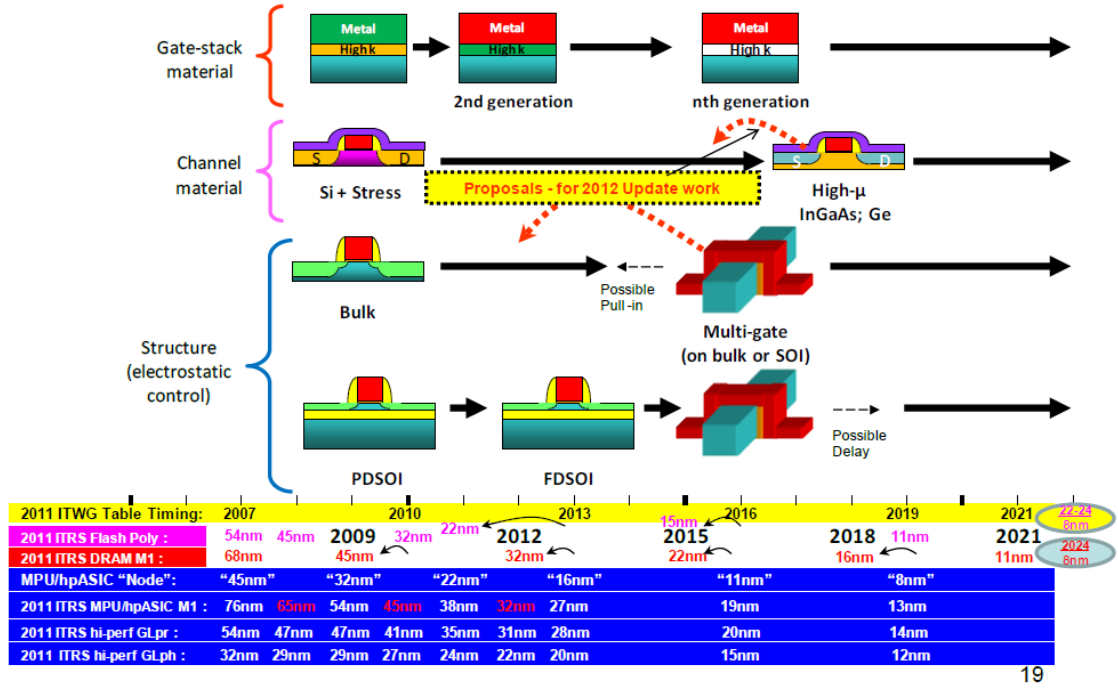


Fig. 1-6. ITRS 2011 "equivalent scaling" process technologies timing compared to overall roadmap technology characteristics (ORTC) and industry "node" naming [1-19].

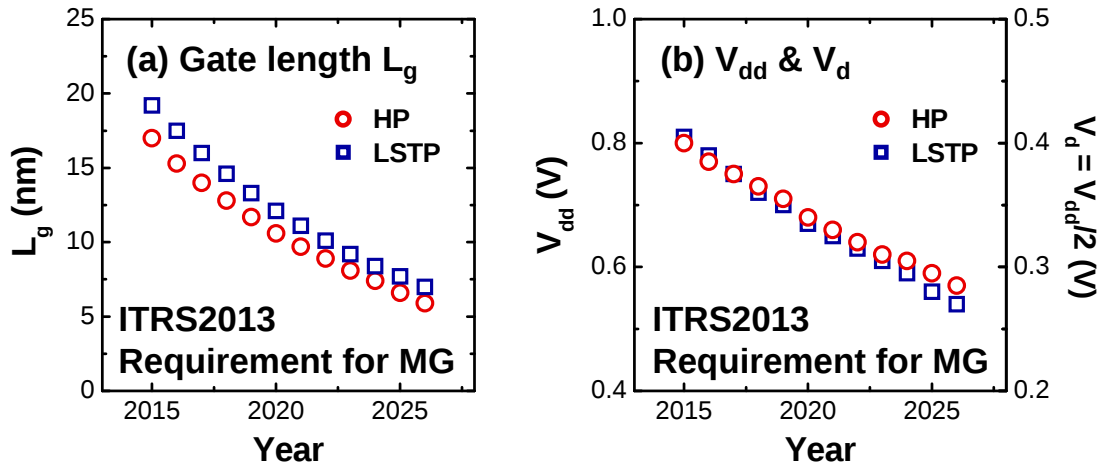


Fig. 1-7. ITRS requirements for future high performance (HP) and low standby power (LSTP) logic circuits consisting of MG FETs. (a) MOSFET gate length L_g , and (b) circuit supply voltage V_{dd} and MOSFET drain voltage V_d are plotted as a function of year between 2015 and 2026 (sourced from ITRS 2013 data in Table RFAMS1 CMOS technology requirements [1-21]).

1.2 MOSFETs for the next technological nodes

1.2.1 Fundamentals of MOSFET

1.2.1.1 MOSFET as a switch

A schematic view of classical bulk silicon MOSFET is shown in [Fig.1-8 \[1-10\]](#). The NMOS FET basically consists of p-type silicon substrate and two opposite n-type regions called the source and drain (S/D). On the other hand, PMOS FET has the n-type substrate and the p-type S/D. The $n^+ - p - n^+$ type structure (source-substrate-drain) can be seen as two p-n diodes connected back-to-back, and the structure normally prevents flow of current between the S/D regions except small diffusion current. The S/D regions are heavily doped in order to reduce the S/D resistances as small as possible. The substrate is typically silicon in current MOSFET technology, but other semiconductor materials with capability for faster transport of inversion carriers are also being considered for future microelectronics. A thin insulator layer, such as silicon dioxide, covers the substrate region between the S/D regions. This insulating layer is capped by a metal or heavily doped poly-Si called gate electrode, and is called gate oxide.

Under distinctive bias conditions; a positive voltage is applied to the drain, the source is grounded, and an enough large positive voltage is applied to the gate. As a result, electrons flow from the n-type source to the drain regions through a formed thin electron-rich layer called channel in the substrate beneath the gate oxide. The gate bias with a positive voltage increases the surface potential and repels holes from the surface. If the gate bias surpasses the threshold voltage, the substrate type near the surface inverts and the electrons, which are opposite type carriers for p-type substrate, can largely flow between the S/D regions. When the channel, which behaves as a minority carrier path, is formed, then the MOSFET is turned on and the state corresponds to a closed switch. If the gate voltage bias is much smaller than the on-state, the channel is dissolved and electrons do not flow except by diffusion effect. This means that the MOSFET is turned off and the state equals an open switch.

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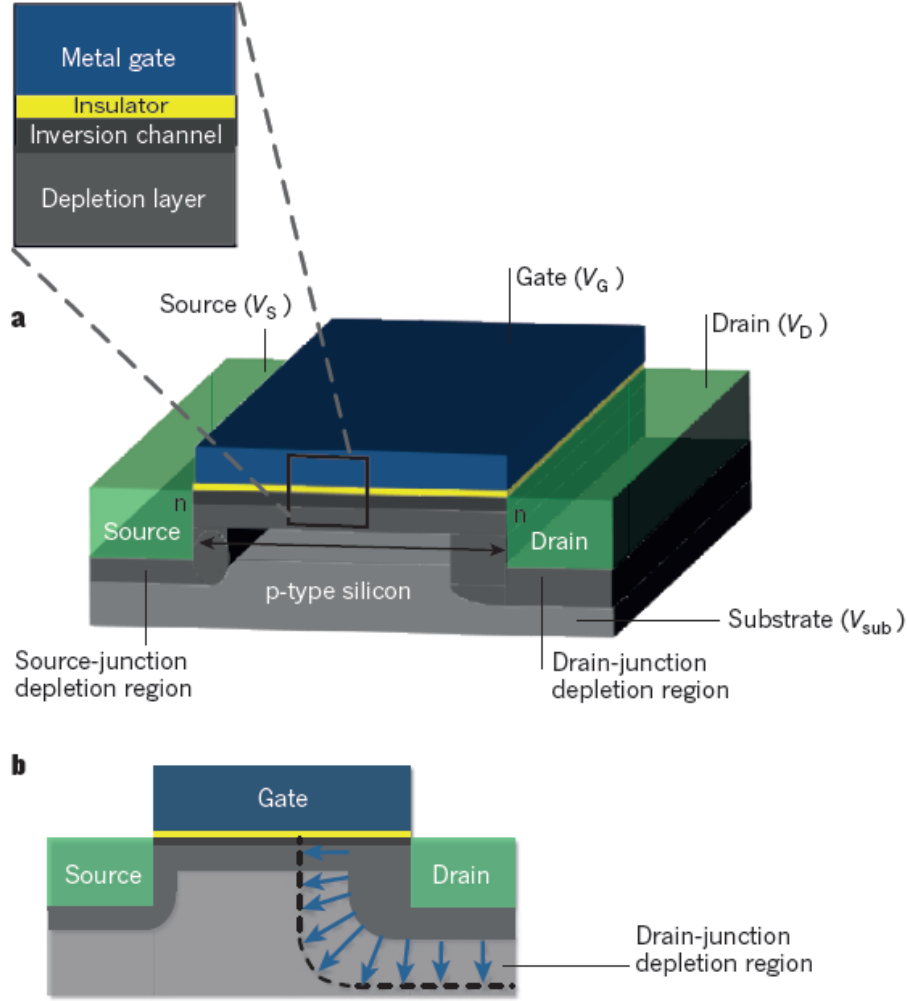


Fig. 1-8. A schematic view of a classical bulk n-channel MOSFET [1-10].

As mentioned above, the gate voltage V_g controls the conductivity between the S/D regions. The drain current I_d between S/D regions therefore depend on the conductivity and the applied electric field along the channel. The I_d in linear region of drain voltage V_d bias (V_{d_lin}) can be expressed as [1-9,1-22]:

$$I_{d_lin} = \mu_{eff} C_{ox} \frac{W}{L} \left\{ (V_g - V_t) \cdot V_{d_lin} - \frac{m}{2} V_{d_lin}^2 \right\} \quad (1-6)$$

where W is the channel width, L is the channel length, V_t is the threshold voltage, μ_{eff} is the effective mobility of carriers in the channel, C_{ox} is the gate oxide capacitance, and m is the body-effect coefficient. If the V_{d_lin} is enough small, this equation can be simplified as:

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$$I_{d_lin} \approx \mu_{eff} C_{ox} \frac{W}{L} (V_g - V_t) \cdot V_{d_lin} = \mu_{eff} C_{ox} \frac{W}{L} V_{gt} V_{d_lin} \quad (1-7)$$

where V_{gt} is the gate voltage overdrive ($=V_g-V_t$).

The I_d increases with the V_d until the I_d reaches a maximum, and then the saturation occurs. The V_d at the saturation region (V_{d_sat}) can be derived by a relationship of $dI_d/dV_d=0$ in Eq. (1-6) and is written as:

$$V_{d_sat} = \frac{V_{gt}}{m} \leftarrow \left. \frac{dI_d}{dV_d} \right|_{V_d=V_{d_sat}} = \mu_{eff} C_{ox} \frac{W}{L} (V_{gt} - mV_{d_sat}) = 0 \quad (1-8)$$

At this V_d point, the channel at the end of the drain region is vanished, and this phenomenon is called pinch-off. The electric field along the channel between the source and the pinch-off point is steady with the V_d increase over V_{d_sat} , and thus this basically results in the saturated I_d . By substituting the $V_{d_sat}=V_{gt}/m$ into Eq. (1-6), the I_d in the saturation region can be derived as:

$$I_{d_sat} = \mu_{eff} C_{ox} \frac{W}{L} \cdot \frac{(V_g - V_t)^2}{2m} = \mu_{eff} C_{ox} \frac{W}{L} \cdot \frac{V_{gt}^2}{2m} \quad (1-9)$$

Actually, the pinch-off point approaches slightly the source region in the condition of $V_d > V_{d_sat}$, and that results in slight decrease of the channel length. This is called channel length modulation and causes a little increase of I_d in the saturation region in practice. It should be noticed that the pinch-off occurs for long device only. If the electric field ($E \propto L^{-1}$) is higher than 10^4 V/m, here is saturation of the carrier velocity before the pinch-off. The V_g and the V_d both dependent MOSFET operations are classified as three regions; linear, saturation, and subthreshold regions as shown in Fig.1-9.

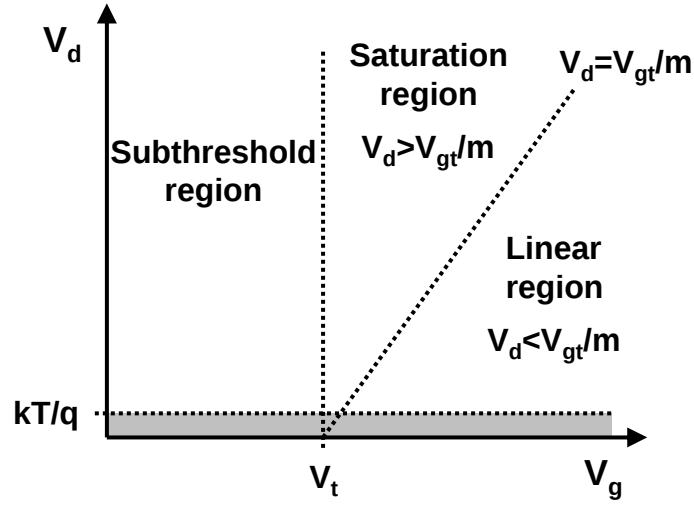


Fig. 1-9. A schematic of three regions in the V_g and V_d both dependent MOSFET operation.

1.2.1.2 Threshold voltage

Threshold voltage V_t is one of the most important and fundamental device parameters for the MOSFET characterization. Precise control of the V_t is a major issue in CMOS applications. It represents the V_g value which is the transition point between weak and strong inversion regions of the MOSFET operation. The definition of V_t was first suggested in 1953 [1-23], and is commonly understood that the V_t provides a bend of the semiconductor energy band at the substrate-insulator interface (surface potential Ψ_s) equaling twice the energy difference between the Fermi level E_F and the intrinsic Fermi level E_i (Ψ_{Bp}) [1-24], as shown in Fig.1-10 [1-22]. The surface potential Ψ_s for NMOS FET comprised of p-type substrate at the V_t can be expressed as:

$$\Psi_s|_{V_g=V_t} = 2\Psi_{Bp} = 2\frac{kT}{q}\ln\left(\frac{p}{n_i}\right) \approx 2\frac{kT}{q}\ln\left(\frac{N_A}{n_i}\right) \quad (1-10)$$

where q is the elementary charge, k is the Boltzmann's constant, T is the absolute temperature, also kT is defined as the thermal energy, n_i is the intrinsic carrier density, p is the hole density, and N_A is the acceptor doping density. The threshold voltage V_t in bulk Si NMOS FET can be given by:

$$V_t = V_{fb} + 2\Psi_{Bp} + \frac{2\sqrt{q\varepsilon_0\varepsilon_{Si}N_A\Psi_{Bp}}}{C_{ox}} \quad (1-11)$$

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where V_{fb} is the flat-band voltage, ϵ_0 is the permittivity in vacuum, and ϵ_{Si} is the relative permittivity of silicon. The flat-band voltage V_{fb} depends on the work function difference between the gate and substrate materials ϕ_{ms} and the equivalent oxide charge density Q_{ox} including the fixed and trapped charges, and is described as:

$$V_{fb} = \phi_{ms} - \frac{Q_{ox}}{C_{ox}} \quad (1-12)$$

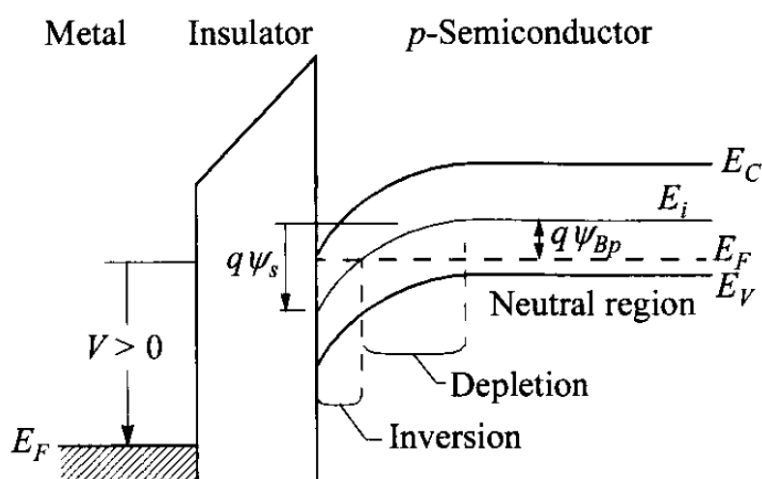


Fig. 1-10. Band diagram of an ideal n-type metal-insulator-semiconductor capacitor under strong inversion [1-22].

In strong inversion mode of MOSFET operation, minority carriers are confined in a potential well near the substrate surface, which is illustrated in Fig.1-10 as an inversion layer. The inversion layer corresponds to the channel region, and thus is formed by a strong bending of substrate energy band in the vicinity of interface between the dielectric barrier and the substrate conduction or valence bands, respectively for electrons or holes as the minority carriers. Consequently, a large number of the carriers can flow from the source toward the drain through the nearly 2D-like channel region in the physical device dimension.

In a MOSFET characteristic of the I_d as a function of the V_g , the I_d seems to approach zero rapidly below the V_t on the linear scale, whereas on the logarithmic scale, the I_d abruptly drops to the off-state, but does not reach zero (Fig.1-11 [1-10]). The V_t corresponds to the beginning point of the on-state, and region where $V_g < V_t$ is called subthreshold (below threshold) region.

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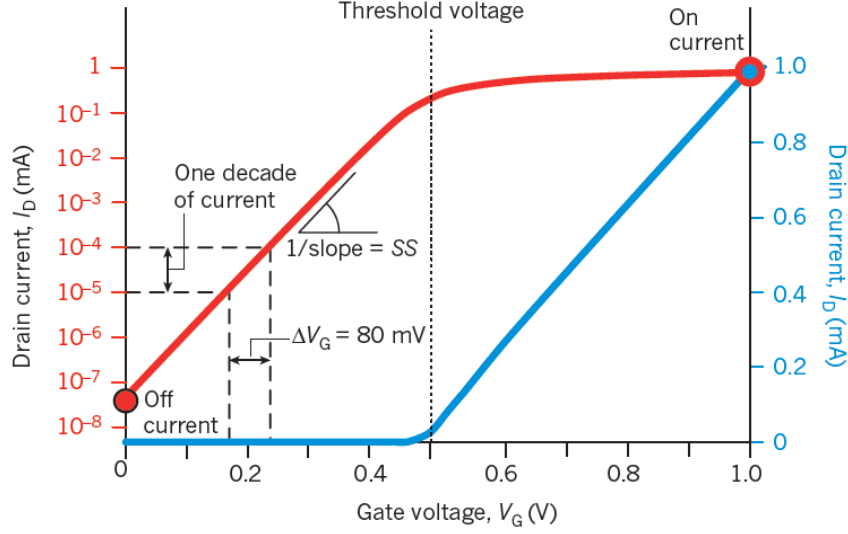


Fig. 1-11. The drain current as a function of the gate voltage in a MOSFET [1-10].

1.2.1.3 Subthreshold swing

In MOSFET operation, when the applied V_g is below V_t (i.e. in subthreshold region), a small I_d exists whereas the channel is not formed yet. Once larger V_d than kT/q is applied to MOSFET in subthreshold region, the current transport is occurred independently of the V_d . The subthreshold current is dominated by the diffusion current and is exponentially increased by V_g . The small I_d in subthreshold region is expressed as [1-9,1-22]:

$$I_{d_sub} = \mu_{eff} C_{ox} \frac{W}{L} (m-1) \left(\frac{kT}{q} \right)^2 \exp \left(\frac{qV_{gt}}{mkT} \right) \left\{ 1 - \exp \left(- \frac{qV_d}{kT} \right) \right\} \quad (1-13)$$

Subthreshold swing (SS) corresponds to the inverse slope of steep and nearly straight I_d - V_g curve in subthreshold region on logarithmic scale as shown in Fig.1-11. This indicates the MOSFET performance of switching steepness between off-state and on-state. The SS value is defined as the reciprocal of the slope and given by:

$$SS = \left(\frac{d(\log_{10} I_{d_sub})}{dV_g} \right)^{-1} = \ln(10) \frac{mkT}{q} = 2.3 \frac{mkT}{q} \quad (1-14)$$

The value thus exhibits the necessary V_g range to increment I_d by one decade on logarithmic scale, and the steep slope is desirable. The SS has a lower boundary of

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59.6mV/decade at room temperature, and the limit cannot be altered by any device parameters of MOSFETs [1-25].

1.2.1.4 Short-channel effects

Short-channel effects (SCE) result from the sharing of the electrical charges in the channel region between the gate and the S/D. The S/D junctions with the body form depletion regions encroaching laterally to the channel region from both sides underneath the gate, thus the effective channel length is shortened. The depletion layers overlaid on the channel region deteriorate the channel controllability by the gate, thereby the control loss is amplified as the V_d increases. This effect is schematically illustrated in Fig.1-8b. The channel control thus does not only depend on the V_g and is also influenced from the V_d bias and the distance between the S/D regions as shown in Fig.1-12. Consequently, the off-current is increased and threshold voltage V_t is decreased, as the channel length is shrunk and high V_d is applied. These could impede the normal operation as MOSFET. Two effects indicating the charge control degradation are mainly observed; drain induced barrier lowering (DIBL) and SS increase. These effects additively increase the gate leakage current, which is a serious obstruction to further downscaling of MOSFETs. Degradation of the maximum operating frequency $f_{\max}$ (*i.e.* deterioration of the maximum switching speed) originated from DIBL effect is expressed by [1-10]:

$$\Delta f = -f_{\max} \frac{2DIBL}{V_{dd} - V_t} \quad (1-15)$$

Therefore, the DIBL and SS are important properties characterizing SCE and electrostatic controllability in MOSFET operation.

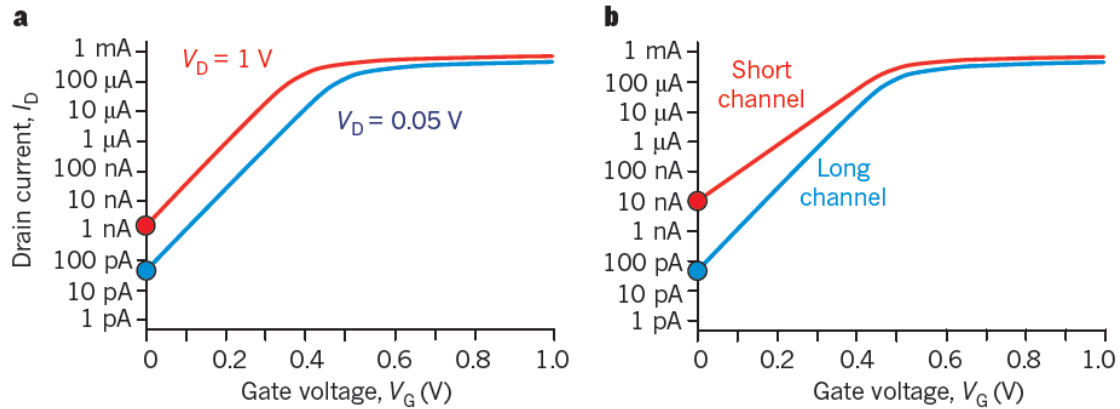


Fig. 1-12. Illustration of short-channel effects [1-10]. (a) The DIBL and (b) the SS increase impacts are shown in the relationship between the drain current I_d and the gate voltage V_g .

1.2.2 Key concepts for advanced MOSFET

1.2.2.1 FD-SOI devices

Silicon-on-insulator (SOI) substrate consists of a thin single-crystalline Si layer placed on an insulator, which is generally silicon dioxide (SiO_2) and is called buried oxide (BOX). The SOI technology was first introduced to military and space applications in the 1970s. For general fabrication of SOI wafers, the founders of Soitec pioneered a new wafer bonding technique, Smart CutTM [1-26,1-27], which was developed at CEA-LETI and ramped up in mid 1990s. Figure 1-13 illustrates the Smart CutTM technology. At first, a donor Si wafer A is thermally oxidized to obtain SiO_2 layer as a BOX in SOI structure. The transferred Si thickness is settled by cleavage layer creation by ion implantation of hydrogen. After surface cleaning and wafer bonding between the donor wafer A and handle wafer B, the cleavage layer is split. As a result, the structure with thin Si film on BOX layer is achieved. The process is finished with polishing, annealing, and treatment of the thin Si film to ensure the targeted Si thickness.

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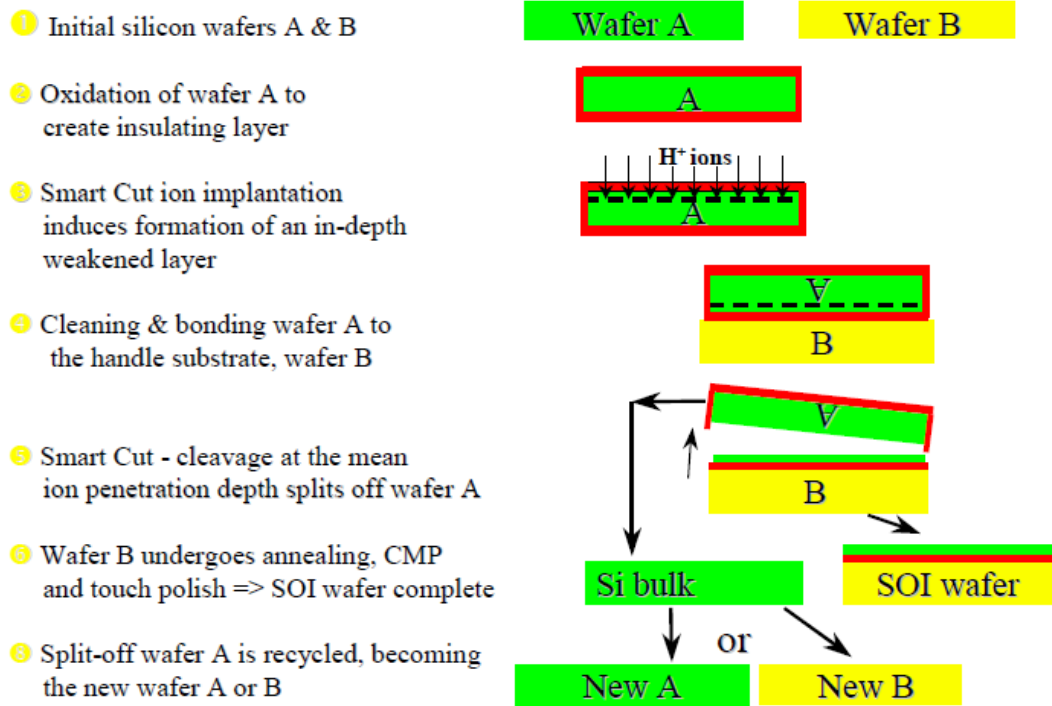


Fig. 1-13. Process flow schematics of SOI substrate fabrication by Smart Cut™ technology [1-27].

The SOI is classified into two categories; partially depleted (PD) or fully depleted (FD) substrates depending on the targeted Si film thickness T_{Si} [1-28~1-30]. In general, FD-SOI structure with thinner T_{Si} (typically, $T_{Si} < 20\text{nm}$) is more advantageous for high- or low-speed digital and analog applications, and also in the mixed-mode IC. The extremely thin body film and dielectric isolation permitting undoped channel provides several advantages: suppression of random dopant fluctuation (RDF), reduced parasitic capacitances, reduction of leakage currents and power consumption, better switching, suitability for low power operation, suppressed latch-up, and simplified lateral isolation process [1-26~1-35].

In addition, body-effect suppression is well known as an important advantage in FD-SOI. The body-effect coefficient, m , is an image of the coupling inefficiency (usually for bulk FET) between the gate and the channel of MOSFET. Impact of the body-effect is discussed with comparison between conventional bulk Si and FD-SOI

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MOSFETs in the following. The equivalent circuit capacitance in bulk Si and FD-SOI MOSFETs is shown in Fig.1-14. The total capacitance C_{tot} in bulk MOSFET is given as:

$$\frac{1}{C_{tot_bulk}} = \frac{1}{C_{ox}} + \frac{1}{(C_{acc} \text{ or } C_{dep} \text{ or } C_{inv}) + C_{it}} \quad (1-16)$$

where C_{acc} , C_{dep} , and C_{inv} are the capacitances in accumulation, depletion, and inversion layers, and C_{it} is the capacitance of traps at gate oxide/channel interface. Figure 1-15 illustrates the C_{tot} - V_g characteristics in bulk Si NMOS FETs [1-36]. Focusing on the ideal curve (metal gate case without quantum-mechanical (QM) effect), the three modes correspond to; upper saturation region on negative bias is accumulation mode, upper saturation region on positive bias is inversion mode, and in-between lower saturation region is depletion mode. Great amount of majority or minority carries, respectively in accumulation and inversion modes, screens the dielectric from the substrate. Thus, in these regions, measured C_{tot} corresponds to C_{ox} (i.e. C_{acc} and $C_{inv} \gg C_{ox}$). In depletion region, depletion layer has the width W_{dep} towards the substrate body. Now C_{tot} and C_{dep} in bulk MOSFETs are written as:

$$\frac{1}{C_{tot_bulk}} = \frac{1}{C_{ox}} + \frac{1}{C_{dep} + C_{it}} \quad (1-17a)$$

$$\text{with } C_{dep} = \frac{\epsilon_0 \epsilon_{Si}}{W_{dep}} \quad (1-17b)$$

For FD-SOI case, the C_{tot} is modified as following:

$$\frac{1}{C_{tot_SOI}} = \frac{1}{C_{ox}} + \frac{1}{(C_{acc} \text{ or } C_{dep_SOI} \text{ or } C_{inv}) + C_{it}} \quad (1-18a)$$

$$\text{with } \frac{1}{C_{dep_SOI}} = \frac{1}{C_{dep}} + \frac{1}{C_{BOX} + C_{it_BOX}} \quad (1-18b)$$

where C_{BOX} is the capacitance in BOX, and C_{it_BOX} is the capacitance of traps at Si/BOX interface. Here, the W_{dep} equals the Si film thickness T_{Si} , thereby $C_{dep} = \epsilon_0 \epsilon_{Si} / T_{Si}$ is obtained.

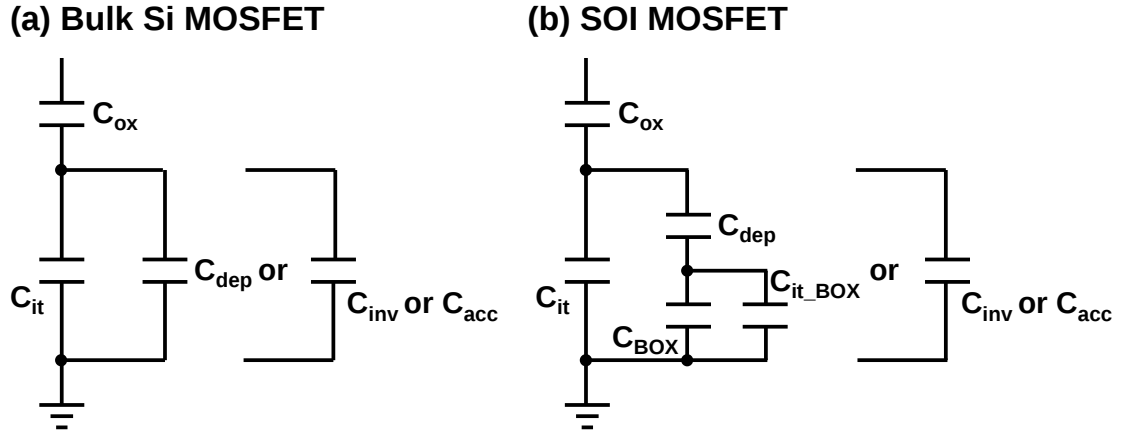


Fig. 1-14. Equivalent circuits of (a) bulk Si and (b) FD-SOI MOSFETs for capacitance.

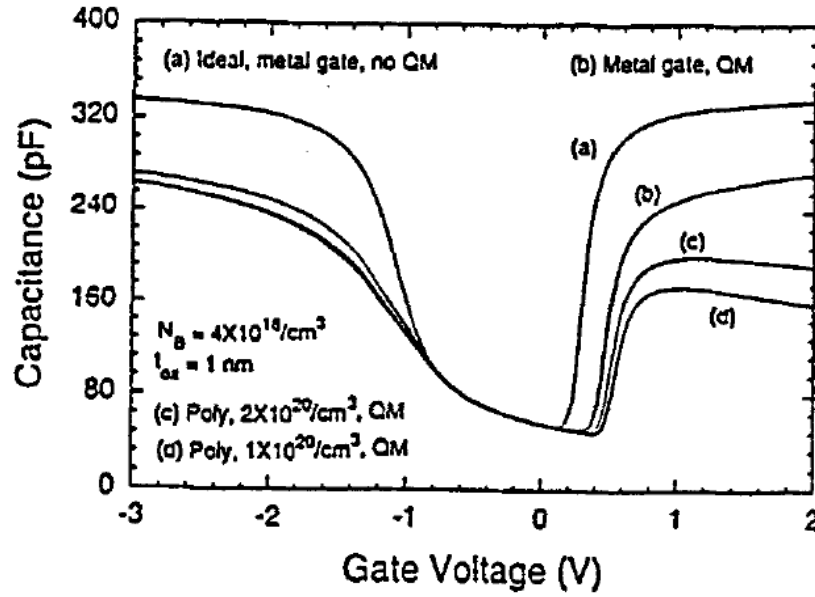


Fig. 1-15. Illustration of C_{tot} - V_g characteristic in bulk Si NMOS FET (Illustration of QM and poly-silicon depletion effects on C-V) [1-36].

Body-effect coefficient m is defined as the capacitance divider ratio, and the coefficient in bulk MOSFET is expressed as:

$$m_{bulk} = 1 + \frac{C_{dep} + C_{it}}{C_{ox}} \quad (1-19)$$

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On the other hand, the coefficient in FD-SOI case is given by:

$$m_{_SOI} = 1 + \frac{C_{it}}{C_{ox}} + \frac{C_{dep}(C_{BOX} + C_{it_BOX})}{C_{ox}(C_{dep} + C_{BOX} + C_{it_BOX})} \quad (1-20)$$

Here, assuming that the ideal circuits exclude C_{it} and C_{it_BOX} , the two equations are simplified as:

$$m_{_bulk} \approx 1 + \frac{C_{dep}}{C_{ox}} \quad (1-21)$$

$$m_{_SOI} \approx 1 + \frac{C_{dep}C_{BOX}}{C_{ox}(C_{dep} + C_{BOX})} \quad (1-22)$$

The coefficient is typically $m \approx 1.05-1.1$ in FD-SOI devices with thick BOX ($C_{BOX} \ll C_{ox}$ and C_{dep}), thus the body-effect is roughly unity, meanwhile the effect is non-negligible with $m \approx 1.2-1.5$ in bulk FETs [1-22,1-32]. Therefore, higher on-state current I_{ON} is achievable by using FD-SOI technology, as mentioned above in Eq. (1-9). Furthermore, nearly ideal SS in Eq. (1-14) i.e. sharper switching property is also provided.

1.2.2.2 Multi-gate devices

3D architectures are also key features for further MOSFET performance improvement. These multi-gate (MG) architectures provide a better electrostatic integrity, thus limiting the SCE [1-22,1-34~1-36]. The innovative structures allow the continuing enhancement of device performance and offer advantages for both the node downscaling and reduction of power consumption. First commercial MG MOSFET based on bulk FinFET technology was released in 2011 by Intel [1-15,1-20] (cf. Fig.1-4). For future CMOS technology nodes, the MG device with aggressively shrunk channel cross-section, which is called nanowire (NW) MOSFET, is thought to be a strong candidate. Various MG structures are schematically shown in Fig.1-16 [1-10].

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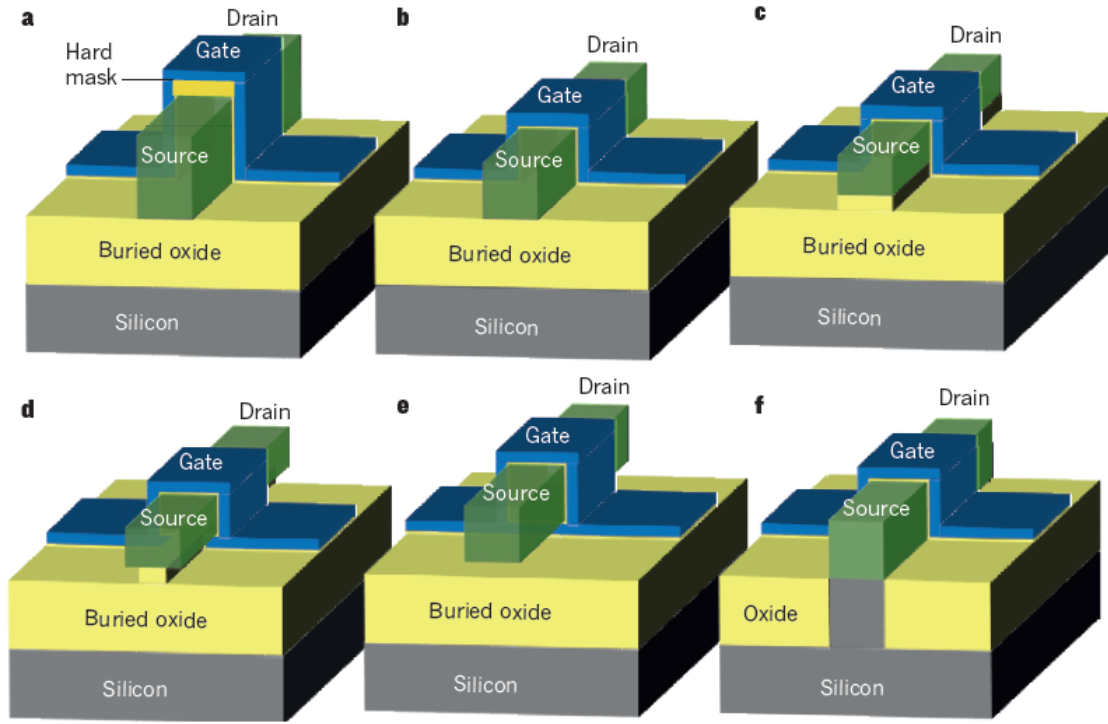


Fig. 1-16. Types of MG MOSFETs. (a) SOI DG FinFET, (b) SOI tri-gate FET, (c) SOI II-gate FET, (d) SOI Ω-gate FET, (d) SOI quadruple-GAA FET, and (e) bulk tri-gate FET [1-10].

Advantage of the immunity against SCE in MG architecture is discussed in the following. SS degradation and DIBL are caused by lateral penetration of the electric field from the S/D regions into the channel. The distribution of electrical potential in the channel of a Si MOSFET is described by Poisson equation, which is one of the Maxwell's equations as:

$$\nabla \cdot \mathbf{E} = \frac{dE_x}{dx} + \frac{dE_y}{dy} + \frac{dE_z}{dz} = -\frac{\rho}{\epsilon_0 \epsilon_{Si}} = \text{Const.} \quad (1-23)$$

where $\mathbf{E}$ is the vector of the electric field, ρ is the local density of electrical charge. In MG devices, increased gate control is exerted in the z (by the top and/or bottom gates) and/or y (by the left- and right-hand side gates) directions, and this decrease the electric field penetration from S/D regions to the channel (x direction). Based on the 3D Poisson equation, a parameter, natural length λ_n which represents the lateral extension of the

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electrical field, can be introduced [1-35,1-37]. This describes that a MOSFET is free from SCE, if the L_g is six-fold longer than the λ_n ($L_g > 6\lambda_n$). If the MG FET has a square cross-section ($T_{Si}=W_{Si}$, where T_{Si} is the Si body thickness and W_{Si} is the Si body width), then the λ_n value is given by:

$$\lambda_n = \sqrt{\frac{\epsilon_{Si}}{n\epsilon_{ox}}} T_{Si} T_{ox} \quad (1-24)$$

where T_{ox} is the gate oxide thickness, ϵ_{ox} is the relative permittivity of the gate oxide, and n is the effective gate number. By extensive numerical simulations, the value of n is defined as shown in Fig.1-17, and this figure shows the universal dependence of DIBL and SS on the scaling parameter $L/2\lambda_n$ for the various MG configurations [1-38]. In addition, these explanations indicate that SCE can be reduced by using the thinner gate oxide, the shallower S/D regions, and the gate oxide material with the higher dielectric constant.

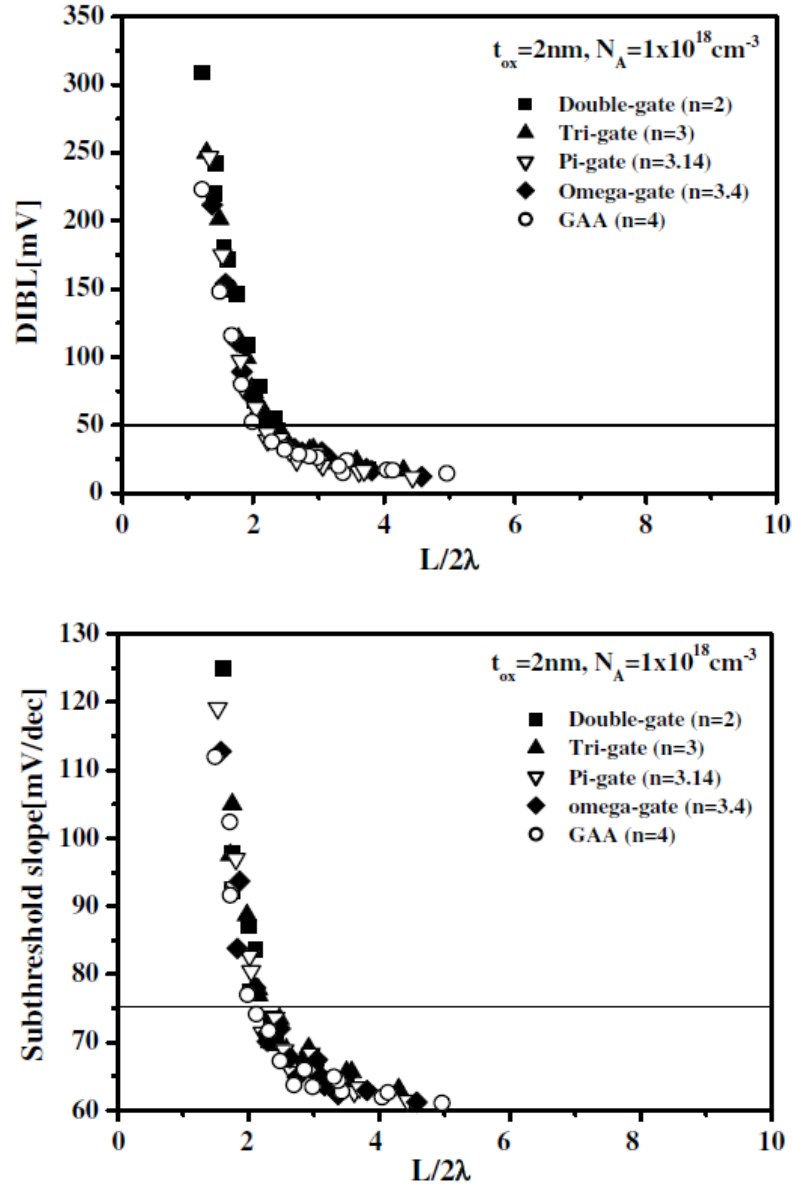


Fig. 1-17. Dependence of DIBL and SS on the scaling parameter [1-38].

In the history of MG devices, a double-gate (DG) structure was first proposed in 1984 [1-39]. The DG architecture was invented based on laterally positioned Si film (similar to FD-SOI structure) and the additional bottom gate. The first DG MOSFET, the fully depleted lean-channel transistor (DELTA), was actually fabricated in 1989 [1-40]. The DG FET consisted of a vertically positioned Si film, and the vertical

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channel technology continued later to DG FinFETs [1-41]. In the DG FinFET (Fig.1-16a), channel conduction is exerted only in both side-walls of Si fin structure. The top has no contribution to the conduction, since the top is covered with hard mask, which is a thick dielectric.

Other MG MOSFET structures have been then excogitated in a stream, such as triple-gate (tri-gate) (Fig.1-16b) [1-42,1-43], pi-gate (Π -gate) (Fig.1-16c) [1-44], omega-gate (Ω -gate) (Fig.1-16d) [1-45], and gate-all-around (GAA) architectures. In tri-gate FETs, gate control is exerted from three surfaces of the channel; the top and two side-walls. Π -gate and Ω -gate FETs improve gate control over tri-gate FET because of better lateral electric field at the bottom, and of increased channel region, respectively. The names of Π -gate and Ω -gate reflect that the gate shapes resemble each Greek character. First GAA device was reported in 1990 [1-46], and consisted of quadruple-gate which has rectangular channel cross-section shape (Fig.1-16e). The all four sides contribute to the channel conduction. In addition, a circular-GAA structure, which has the circularly surrounded channel shape and the aggressively scaled diameter, has been investigated in Refs. [1-47,1-48].

The MG FETs with aggressively downscaled body cross-section are often called nanowire (NW) devices. In this work, we expediently define our devices with narrower channel top width than $\approx 30\text{nm}$ and with body height $\approx 10\text{-}15\text{nm}$ as Ω -gate and tri-gate NWs. It should be noticed that the performances of Fin- and NW FETs with rectangular cross-section shape of the body are not significantly different.

In practice, NW FETs are usually designed with several channel fingers aligned parallel and with a common gate electrode. This configuration allows simple increase of the drive current and the total effective channel area by increasing the number of fingers (*e.g.* tri-gate array structure with the 50-multiple fingers is shown in Fig.1-18 [1-49]). Especially, increment of the total effective channel width is important technology to perform accurate measurements (*e.g.* capacitance, charge pumping, etc.) in actively miniaturized MG architectures, such as NW FETs. Moreover, 3D-stacked MG devices have been also contrived with a concept of the finger multiplication in the vertical direction [1-50~1-53].

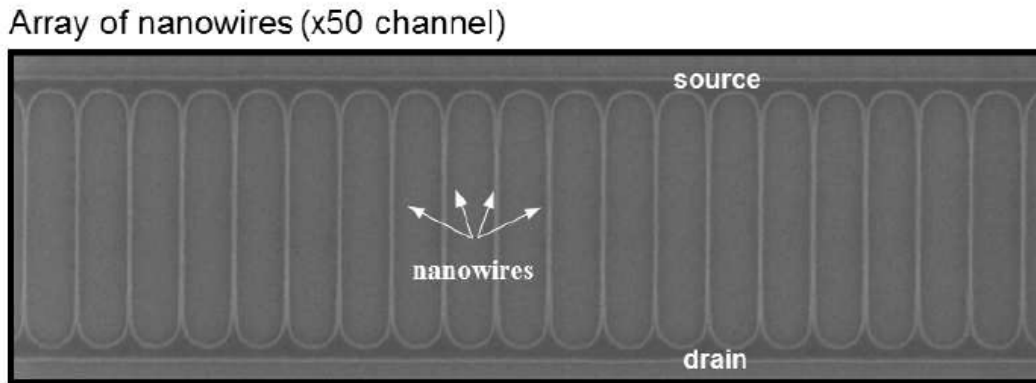


Fig. 1-18. Array of Si NW on oxide ($\times 50$ channels) obtained by SEM [1-49].

SOI substrates have good compatibility with MG device fabrication. Particularly, most of the advanced MG devices mentioned above were fabricated by using FD-SOI substrates. FD-SOI substrate is more beneficial than bulk Si case for fabrication of miniaturized MG devices, such as NW FETs, due to the intrinsic device isolation by BOX layer. Although more complicated process are required, bulk DG FinFET and tri-gate devices have been also investigated (Fig.1-16f), and good SCE immunity has been reported [1-15,1-20,1-54]. Basically, MG fabrication process is same as conventional planar device process. Furthermore, the advanced technologies are also applicable, though more process optimization is required.

However, the channel interface quality is often considered in MG FETs as a critical issue, due to MG body formed by etching process, the multiple surface orientations, and the large surface/volume ratio. In fact, the ultra-scaled dimensions with the diameter of NW below sub-10nm can lead to the volume inversion [1-55], and the QM confinement of inversion carriers changes the transport properties in NW FETs [1-56~1-58]. Moreover, the difference of crystallographic orientation between the top (equal to bottom) and side-wall planes change the carrier transport property compared to conventional planar MOSFETs [1-49,1-59,1-60]. Etched MG surfaces usually show the less quality (higher interface states and degraded carrier mobility) than that in the perfect surface of planar devices. The circular shape, curved surface, and rounded corner of NW body with complex crystallographic orientations could also contribute to change of the carrier transport property [1-47~1-54]. Thus, the understanding of carrier

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transport behavior and oxide/channel interface quality is particularly important and needs experimental and theoretical investigations.

1.2.2.3 High- κ dielectric/metal gate system

Success of Si MOSFET has proceeded from the excellent MOS structure with the interface of Si/SiO₂. However, as a consequence of aggressively MOSFET downscaling, the replacement of SiO₂ by dielectric with higher permittivity (high- κ) is imperative in order to prevent the excess gate leakage current by enlarged QM tunneling effect. A relationship of physical thickness between SiO₂ (T_{SiO_2}) and the alternative high- κ dielectric ($T_{\text{high-}\kappa}$) with same gate capacitance C_{ox} is described as:

$$C_{\text{ox}} = \frac{\epsilon_0 \epsilon_{\text{SiO}_2}}{T_{\text{SiO}_2}} = \frac{\epsilon_0 \epsilon_{\text{high-}\kappa}}{T_{\text{high-}\kappa}} \quad (1-25)$$

where ϵ_{SiO_2} is the relative permittivity of silicon dioxide, and $\epsilon_{\text{high-}\kappa}$ is the relative permittivity of high- κ dielectric. A high dielectric constant thereby allows physically thicker layer to obtain the same C_{ox} than the required T_{SiO_2} . The required T_{SiO_2} is called the equivalent oxide thickness (EOT), and is given by:

$$EOT = \frac{\epsilon_{\text{SiO}_2}}{\epsilon_{\text{high-}\kappa}} T_{\text{high-}\kappa} \quad (1-26)$$

Effectiveness of the high- κ dielectric is interpreted by using the EOT, *i.e.* the gate leakage current is reduced with the high- κ dielectric due to thicker $T_{\text{high-}\kappa}$, while a small EOT is maintained.

To select a good alternative, a number of considerations are required; high dielectric constant, large band gap and band offset to channel material, thermodynamic stability, process compatibility, reliability, and interface quality. SiO₂ is an excellent gate dielectric in terms of band gap and band offset to Si, since the band gap is 9eV and is roughly intermediately placed around Si band gap with 1.1eV thus forming high barriers for both electrons and holes. Most of high- κ dielectric candidates has smaller band gap than the 9eV of SiO₂, and some indicates considerably worse band offsets and symmetry as shown in Fig.1-19 [1-61~1-63]. Moreover, excessively high dielectric constant is ineligible because of a trade-off relationship between the dielectric constant and the band gap as shown in Fig.1-20 [1-61~1-63].

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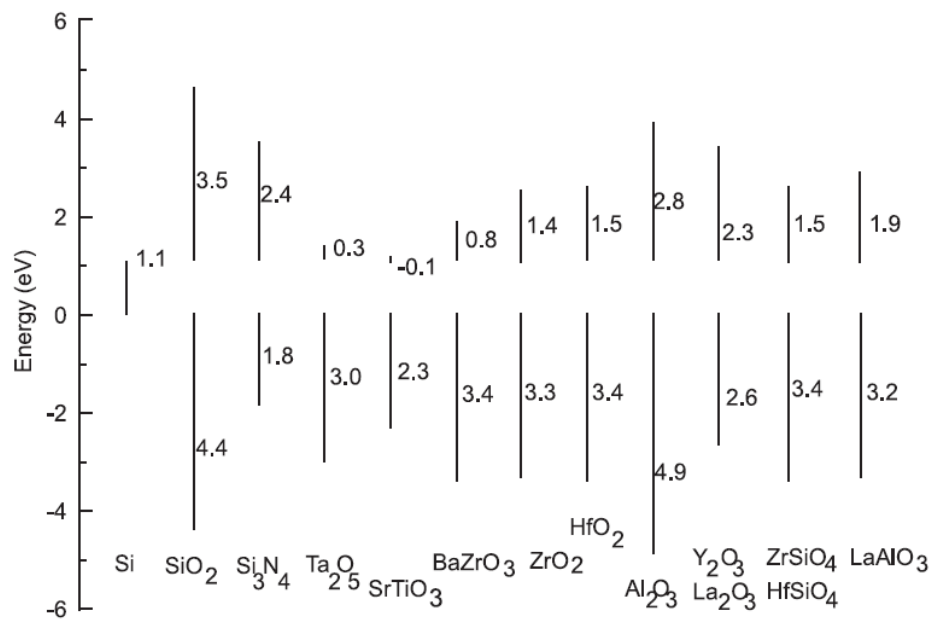


Fig. 1-19. Conduction and valence band offsets for various dielectrics [1-61~1-63].

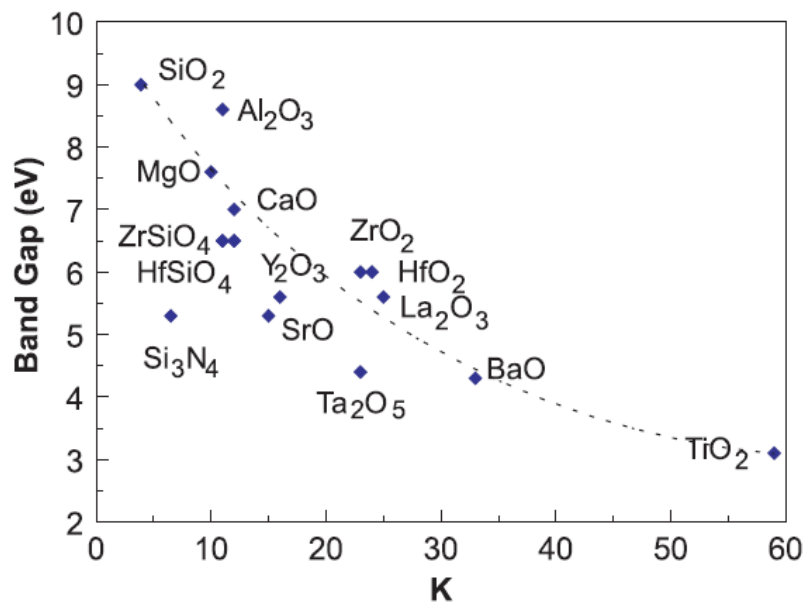


Fig. 1-20. Band gap energy as a function of relative permittivity for various dielectrics [1-61~1-63].

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Hf-based oxides have been widely and intensively investigated as attractive high- κ dielectrics due to the good trade-off between the dielectric constant and the band gap, as shown in Figs.1-19 and 1-20. Firstly, Hafnium dioxide (HfO_2) has been focused significantly, but the oxide is difficult to etch [1-64], and reacts with the gate electrode [1-65,1-66]. Furthermore, HfO_2 is typically amorphous like SiO_2 , however through thermal process in the FET fabrication, the oxide becomes crystalline or poly-crystalline. The poly-crystalline oxide is undesirable, since the dielectric is composed of grains [1-67]. The grains can generate large dispersion of the dielectric property, due to the randomly varied size, orientation, and number in each oxide film. In addition, boundary of the grains possibly makes defects trapping/de-trapping carriers and large leakage current path. These drawbacks can be suppressed by forming hafnium silicate ($\text{Hf}_x\text{Si}_{1-x}\text{O}_2$ or HfSiO). To achieve more thermal stability, nitrogen-incorporated hafnium silicate, hafnium silicon oxy-nitride (HfSiON), has been proposed. Both reliability and dielectric constant enhancements by the Hf-N bonds were reported [1-64,1-68,1-69].

In conventional gate stack with SiO_2 , highly-doped poly-Si gate is used due to good compatibility in device fabrication process. The poly-Si gate similarly behaves as metal due to modulated Fermi level near conduction or valence bands by ion implantation. This technique is greatly advantageous for tuning of threshold voltage V_t of MOSFET. However, depletion of the poly-Si gate leading to the spurious C_{ox} measurement (smaller than the net value) is non-negligible with FET downscaling (cf. Fig.1-15). The dopant penetration to gate dielectric is also a problem. Therefore, an appropriate metal gate is also necessary to further scaled MOSFET. For integration, not only metal work function corresponding to Fermi level, which is basically intrinsic property in each metal, but also thermodynamic stability and process compatibility must be taken into account.

Large efforts to integrate high- κ dielectrics and metals as the gate stack system in CMOS devices have been made. Today TiN metal gate has been applied worldwide due to the good stability and compatibility [1-69~1-71]. Moreover, the TiN work function can be adjusted by different deposition process or thickness [1-72,1-73]. Consequently, the work function can be roughly conformed to mid-gap of Si band structure. Thus, as one of the most optimized high- κ /metal gate stack, the Hf-based oxide/TiN system is

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utilized. Negative impacts of high- κ /metal gate integration in MOSFETs (degraded inversion carrier mobility and reliability [1-74~1-76]) and the solutions have been also investigated. Most detrimental effects in advanced Hf-based high- κ /TiN devices are ascribed to nitridation processes such as the TiN deposition rather than high- κ dielectric processes [1-77].

1.2.2.4 Strain technology

Strain introduction to the channel material has been considered as one of the most attractive solutions to improve the I_{ON}/I_{OFF} ratio, transconductance, and carrier mobility against the downscaling limits of MOSFETs [1-78,1-79]. For NMOS, largely improved electron mobility and lower threshold voltage V_t are achieved by introducing in plane tensile strain in the channel [1-80,1-81]. The enhancement of electron mobility and the V_t lowering results from splitting of the conduction band [1-82~1-87], as shown in Fig.1-21. The tensile strain separates the six-fold degenerate valleys in unstrained Si into two groups; four-fold (Δ_4) valleys with higher energy and two-fold (Δ_2) valleys with lower energy. The Δ_2 valleys lead to decrease of the averaged conductivity mass owing to the preferential occupancy with lighter conductivity mass than Δ_4 valleys. Furthermore, intervalley phonon scattering between the Δ_2 and Δ_4 valleys is suppressed due to the energy splitting. The latter contribution can be expressed as follows:

$$\frac{1}{\tau_{phonon}} \propto \Delta E \quad (1-27)$$

where τ_{phonon} is relaxation time due to intervalley phonon scattering and ΔE is the energy splitting between the Δ_2 and Δ_4 valleys of the Si conduction band. The scattering rate decreases as the energy splitting enlarges due to the applied tensile stress in NMOS case. Recently, tensile strained SOI (sSOI) has been proposed as a powerful technology for enhancement of NMOS FET performance with combination of each advantage in SOI and tensile strain technologies [1-27,1-88].

For PMOS, significantly higher hole mobility and lower V_t are obtained from introduction of in plane compressive strain in the channel [1-89~1-91]. The improvement stems from unraveled Δ_2 degeneracy to heavy and light holes (HH and LH) bands in the valence band [1-92] (Fig.1-21). The light hole band provides reduced

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conductivity mass. In addition, intervalley (interband) phonon scattering is suppressed by the degeneracy resolution. Uniaxially compressive strained Si channel has been obtained by embedded SiGe-S/D formation [1-93] (cf. Fig.1-4). For future high-performance CMOS node, compressively strained SiGe-on-insulator (SGOI) structure is a serious alternative technology [1-94,1-95]. In addition, a contact-stop-etch-layer (CESL) deposition has been also used as a uniaxial stressor for either tensile or compressive strain depending on the deposition conditions [1-96].

As a consequence, the use of strain technology is thought as an efficient booster to reduce power consumption by lowering the supply voltage without losing circuit performance. At the same time, influence to the oxide/channel interface quality and reliability from the stress technologies would be an issue. Thus, the understanding of comprehensive oxide/channel interface characteristics is absolutely imperative.

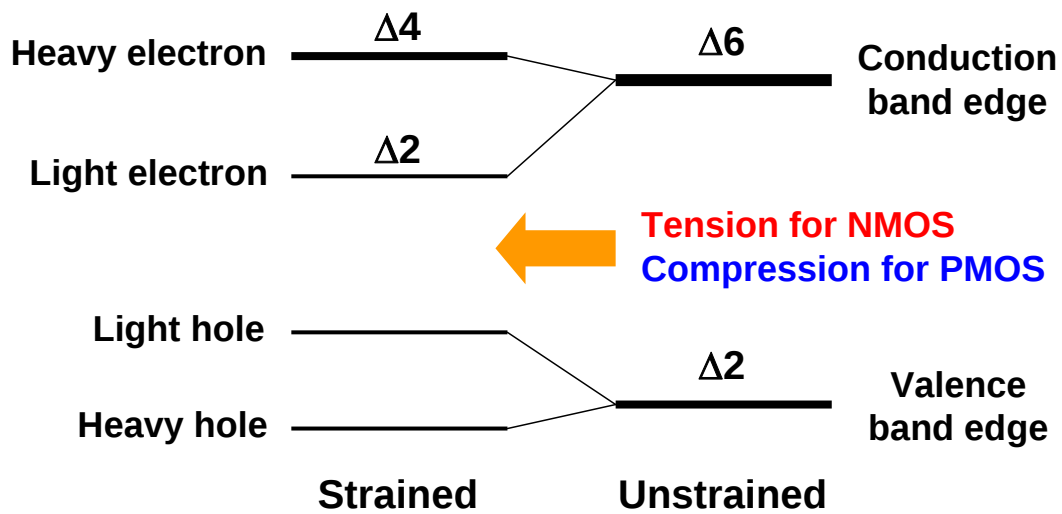


Fig. 1-21. Diagram of degenerate conduction and valence bands splitting owing to strain effect.

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1.3 Low-frequency noise

Generally, “noise” is referred to as unwanted and detrimental signal mainly appearing in telecommunications, such as sounds and images. Noise usually interferes with communications through transmitting/receiving processes by distorting the raw data. Noise spontaneously and randomly arises in every electronic device, on the current or voltage, and could disrupt the signals. Noise from external sources such as vibrations, lights, interferences from AC power lines, etc... is often considered as a main hindrance, but it can be suppressed or removed by appropriate shielding, filtering, and layout design for electronic devices and circuits. Despite reduction of external noise, inherent noise still exists in each electronic device. Internal noise in the devices cannot be completely eliminated and sets a lower limit on signal detection in RF/analog devices and circuits. For instance, when excess noise at low-frequency region (1/f noise) stemming from MOSFET appears in phase noise of voltage-controlled-oscillators (VCO), the signal-to-noise ratio (SNR) in mixers for homodyne receivers is degraded. The internal noise can be efficiently reduced by optimizing the fabrication process and design of the devices and circuits. Consequently, from an engineer’s point of view, performance limits of RF/analog circuits and devices are determined by noise properties.

On the other hand, from a physicist’s point of view, low-frequency noise (LFN) provides insight into the carrier transport mechanisms in the MOSFET’s channel that cannot be revealed by DC characterization. Moreover, the noise characterization has no lower limit of the necessary MOSFET channel area. Therefore, measurement and understanding of internal noise are important in order to evaluate the performance and study the carrier transport in MOSFETs.

In general, the study of internal electronic noise in solid-state devices is carried out by measuring the current fluctuations. [Figure 1-22](#) illustrates the time dependent fluctuating current $I(t)$ due to random noise effect through a device [\[1-97\]](#), that can be expressed as:

$$I(t) = \bar{I} + i(t) \tag{1-28}$$

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In this expression, $\bar{I}$ is the average value of the current and $i(t)$ is the randomly fluctuating component as a function of time. The average of $i(t)$ monitored over a long time should always equal zero (stationary), since the value of $i(t)$ is completely random at any point in time domain. Noise investigation requires to be performed with mathematical methods based on probability theory, which allows defining the appropriate averages of randomly fluctuating variables. A commonly-used and powerful method to interpret and characterize noise relies on variable transformation from the time domain to the frequency domain by Fourier transform.

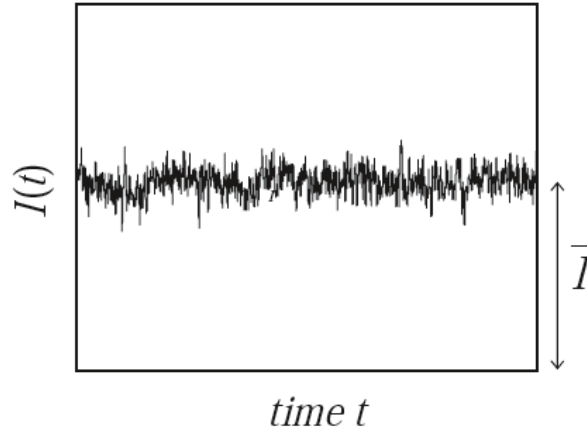


Fig. 1-22. An illustration of typical noise waveform [1-97].

The Fourier transform method is defined as:

$$X(f) = \int_{-\infty}^{\infty} x(t) \exp(-j2\pi ft) dt \quad (1-29a)$$

and reciprocally, inverse Fourier transform:

$$x(t) = \int_{-\infty}^{\infty} X(f) \exp(j2\pi ft) df \quad (1-29b)$$

where $x(t)$ is a stationary variable in time domain and $X(f)$ is the Fourier-transformed variable in frequency domain. The Fourier transform separates the random signal into the sum of simple frequency components represented mathematically as sine and cosine waves. To properly describe the noise distributed within frequency regime, the mean random signal squared (noise power) per unit frequency, named the power spectral

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density (PSD) $S(f)$ is generally used. The PSD is given by the autocorrelation function $R(s)$ according to the Wiener-Khintchine theorem [1-98,1-99] and can be derived as:

$$S(f) = 4 \int_0^{\infty} R(s) \cos(2\pi fs) ds \quad (1-30a)$$

$$\text{equivalently: } R(s) = \int_0^{\infty} S(f) \cos(2\pi fs) df \quad (1-31b)$$

The PSD can be measured with a spectrum analyzer for the current noise S_I and voltage noise S_V in A^2/Hz and V^2/Hz , respectively.

There are various kinds of noise sources leading to different behaviors in frequency or time domain. In the following, representative fundamentals of the noise sources are described [1-97].

1.3.1 Main noise sources

1.3.1.1 Thermal noise

Thermal noise stems from the random thermal motion of electrons in a material. In 1906, A. Einstein predicted that Brownian motion of electrons would cause fluctuations of the material resistance in thermal equilibrium [1-100]. Each time an electron is scattered and the velocity is randomized by the thermal energy. If there are more electrons moving in a certain direction than electrons moving in the other directions, a small net current is flowing. Strength and direction of the current fluctuates, but the average over time is always zero. Thus, thermal noise is nearly constant over frequency, and is also called white noise. It was first experimentally discovered by J. B. Johnson and theoretically explained by H. Nyquist in 1928 [1-101,1-102]. For this reason, thermal noise is also called Johnson or Nyquist noise.

If a piece of material with resistance R and temperature T is considered, the PSD of thermal noise current S_I or the voltage counterpart S_V can be written as:

$$S_I = \frac{4kT}{R} \quad (1-31a)$$

$$S_V = S_I R^2 = 4kTR \quad (1-31b)$$

Thermal noise exists in every resistor and resistive part of devices except at absolute zero point ($T=0K$), and needs no applied voltage bias. It is thereby frequently used for comparison with other noise sources and temperature measurement characterizing the

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resistance R . For instance, thermal noise is usually used to calibrate a noise measurement system, because it determines the lower limit of measured noise level in the system.

1.3.1.2 Shot noise

Shot noise is generally observed in the current flowing across a potential barrier, such as p-n junction and Schottky junction. The current is not continuous due to the discrete nature of the charge carriers (electrons) and is given by the number of carriers flowing through the barrier during a period of time. Shot noise was firstly discovered in vacuum tubes by W. Schottky in 1918, and an equation was also derived as the Schottky formula [1-103]. The PSD of shot noise is expressed as:

$$S_I = 2qI \quad (1-32)$$

Shot noise is also considered as a white noise source, since the behavior has no frequency dependence likewise thermal noise. But, the level of shot noise is generally much lower than the thermal noise, thus it cannot be distinguished easily.

1.3.1.3 Generation-recombination noise

Generation-recombination (g-r) noise in semiconductors is caused from random generation and recombination of charge carriers (*i.e.* electrons or holes) via trapping sites. It leads to the fluctuation of the number of carriers related to the current flowing. Electronic states localized within the forbidden bandgap are referred to as traps, and exist due to the presence of various defects or impurities in the semiconductor or at the surface [1-104]. The carrier number fluctuations by capturing/emitting the carriers can also induce several fluctuations in the carrier mobility, electric field, barrier height, width of space charge region, etc... The g-r noise PSD can be expressed as:

$$\frac{S_I}{I^2} = \frac{S_N}{N^2} = \frac{\overline{\Delta N^2}}{N^2} \cdot \frac{4\tau}{1 + (2\pi f)^2 \tau^2} \quad (1-33)$$

where N is the averaging number of carriers, $\overline{\Delta N^2}$ is the variance of the fluctuating number of carriers, and τ is the time constant of the transitions. The shape of g-r noise spectrum in Eq. (1-33) is illustrated in Fig.1-23 and is called a Lorentzian [1-97]. In general, the time constant and the relative strength of the traps differ and strongly

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depend on the trap energy level and spatial location. The g-r noise is only significant when the Fermi energy level is close to the trap energy level (within a few kT), and then the capture time and the emission time are almost equal. On the other hand, when the Fermi level is far above or below the trap level, the trap is occupied or emptied most of the time and few g-r events occur.

1.3.1.4 Random-telegraph-signal (RTS) noise

A special case of g-r noise is the random-telegraph-signal (RTS) noise (also called burst noise or popcorn noise), which is monitored as discrete switching events of the I_d level in the time domain in a MOSFET. The RTS noise is commonly observed in MOSFETs with small channel area and is correlated to individual carrier trapping/de-trapping between the Si substrate and traps in the gate oxide [1-105,1-106]. If only one or a few traps in the gate oxide are involved, I_d can switch between two or more states owing to random trapping/de-trapping of carriers.

For a two-level system with step difference ΔI and time durations for the lower state τ_l and for the higher state τ_h , the PSD of the current fluctuations is derived under Poisson distribution (Fig.1-24) as:

$$S_I = \frac{4(\Delta I)^2}{(\tau_l + \tau_h) \cdot \left\{ \left(\tau_l^{-1} + \tau_h^{-1} \right)^2 + (2\pi f)^2 \right\}} \quad (1-34)$$

Both PSD shapes of RTS noise and g-r noise exhibit a Lorentzian type (Fig.1-23). When the number of traps contributing to the current fluctuations is small, the g-r noise is only observed as a sum of the RTS noise stemming from one or a few traps with identical time constants. In typical RTS noise investigation, the random switching process of the I_d level involved by just one trap, i.e. by a single electron, can be studied in the time domain. The trap energy level, spatial location of the trap, and the capture and emission behavior can be derived from the g-r and RTS noise characterizations with measuring the temperature and bias dependencies [1-104, 1-107~1-109].

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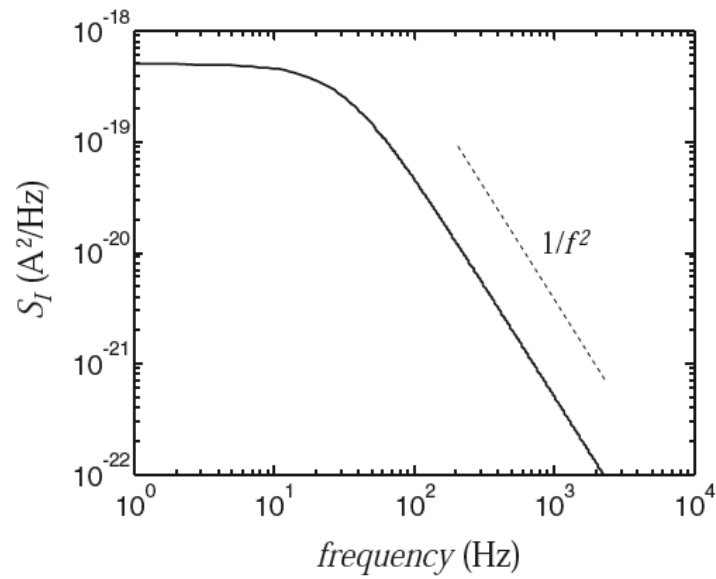


Fig. 1-23. A Lorentzian shaped PSD, plotted for the RTS noise waveform in Fig.4-3 [1-97].

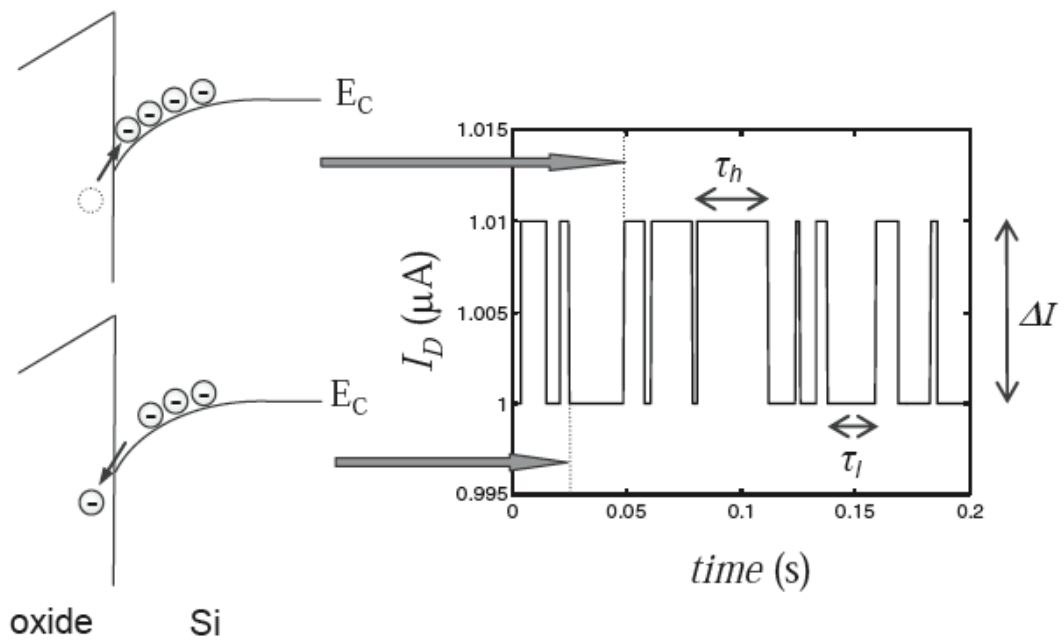


Fig. 1-24. Schematic description of RTS noise, exemplified for a MOSFET. The drain current switches between two discrete levels when a channel electron moves in and out of a trap in the gate oxide [1-97].

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1.3.1.5 1/f noise

1/f noise, also called flicker noise, is the general name of fluctuations with a PSD being proportional to $1/f^\gamma$ with the value of frequency exponent γ around 1. The general form of PSD for 1/f noise is given as:

$$S_I = \frac{K \cdot I^\zeta}{f^\gamma} \quad (1-35)$$

where K is a proportional constant and ζ is a current exponent. The 1/f noise was firstly observed in vacuum tubes by J. B. Johnson in 1925 [1-110], and then was first interpreted by W. Schottky [1-111]. It has been accepted as the most general noise type in low-frequency regime of the spectrum (10^{-5} - 10^7 Hz) in most conductive materials and various semiconductor devices up to the present date. In general, the 1/f noise is difficult to find at high-frequency part due to the overlap with thermal noise. There are essentially two physical mechanisms of current fluctuations: fluctuations in the carrier mobility or fluctuations in the number of carriers.

For the carrier number fluctuations, the g-r noise stemming from a large number of traps can produce 1/f noise by the PSD superposition for a certain distribution of various time constants as shown in Fig.1-25. The idea of Lorentzians superposition to yield the 1/f noise behavior was suggested by J. Bernamont in 1937 [1-112] and by M. Surdin in 1939 [1-113]. The 1/f noise from fluctuations of the carrier number has been well described in large area down to small area MOSFETs. However, 1/f noise can be still observed even though the RTS noise is not involved. In such case, the 1/f behavior is attributed to the fluctuations in the carrier mobility. The physical origin of 1/f noise (carrier number fluctuations vs. mobility fluctuations) still remains controversial and the search of mechanisms of this noise is being intensively continued to the present day.

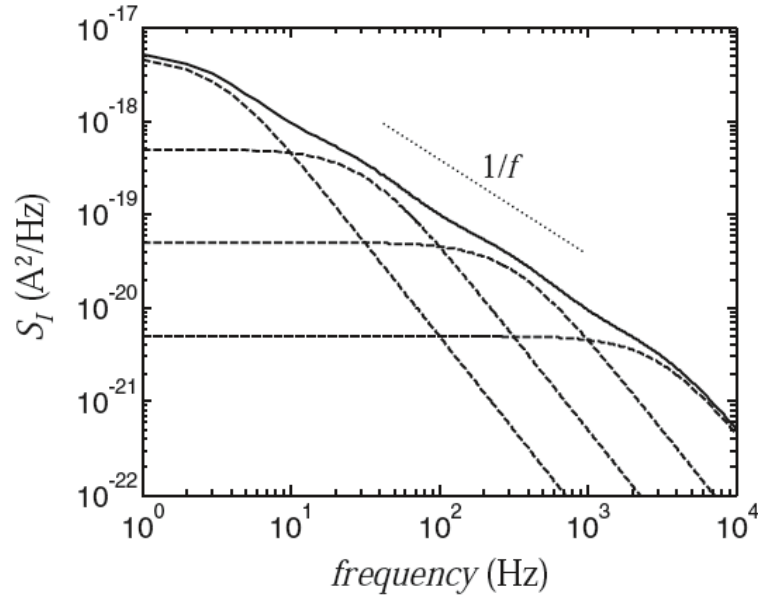


Fig. 1-25. Superposition of 4 Lorentzians giving a total spectrum that approximately exhibits a $1/f$ dependence over several decades of frequency [1-97].

1.3.2 Low-frequency noise in MOSFET

1.3.2.1 LFN measurements as a diagnostic tool

Measurement of LFN appearing in the drain current I_d is an efficient diagnostic tool to characterize the electrical properties of MOSFETs, mainly focusing on the oxide/channel interface properties. In general, LFN spectra in a MOSFET show the frequency dependent components; $1/f$ and/or $1/f^2$ (g-r) components, as mentioned above. [Figure 1-26](#) shows a schematic of the PSDs for the $1/f$, g-r, and thermal noise at low frequency region [1-97].

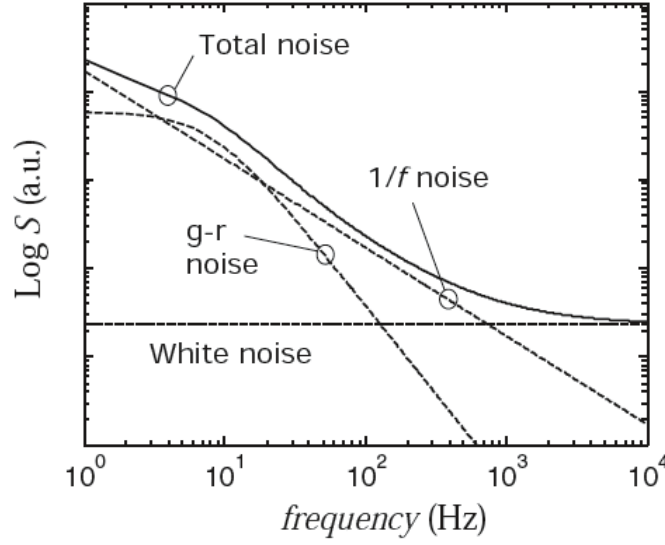


Fig. 1-26. The PSD for low-frequency noise and white noise plotted vs. frequency. The excess noise above the white noise floor is called low-frequency noise and may consist of 1/f noise or g-r noise [1-97].

Even if 1/f noise is considered to be universal for various devices, there have been controversies for its origin. The current fluctuations in materials can be understood as conductivity fluctuations. The conductivity σ is defined for drift of electrons as:

$$\sigma = qn\mu_n \quad (1-36)$$

where n is the carrier (electron) density as carrier and μ_n is the electron mobility. From the idea of conductivity fluctuations, two fluctuation models can be considered; carrier number fluctuations (CNF, Δn) and mobility fluctuations (MF, $\Delta\mu$). Several theories have been proposed to interpret 1/f noise in MOSFETs, and there are two most essential frameworks:

- (i) Hooge empirical model, which presumes the MF [1-114~1-118]
- (ii) McWhorter model, which assumes the CNF by the QM tunneling transitions between oxide traps and channel [1-119~1-123]

In MOSFETs, the drain current flows in the channel, *i.e.* a narrow path confined close to the substrate surface beneath the gate oxide. In such case, CNF is mostly expected, and is actually dominant as the 1/f noise source in some reports [1-124~1-127].

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Nevertheless, other published works have reported that the MF noise model tends to be better to explain the 1/f noise especially in PMOS FETs [1-128,1-129].

Concerning 1/f noise in recent advanced MOSFETs, such as MG devices (FinFETs [1-130~1-143] and NW devices [1-53,1-144~1-152]), the origin is attributed to the carrier number fluctuations with correlated mobility fluctuations (CNF+CMF) [1-153,1-154]. This model assumes that CNF additionally induces fluctuations of the carrier mobility due to Coulomb interactions between charge carriers in the channel and trapped charges. In practice, this CNF+CMF model is suitable for MG devices [1-53, 1-130,1-131,1-134,1-137,1-138,1-141~1-144,1-146,1-147,1-149~1-152]. Consequently, LFN measurement is thought to be enough powerful to characterize the oxide/channel interface properties even for future device nodes with more complex and ultra-scaled architectures, such as NW MOSFETs.

1.3.2.2 Hooge empirical model - Mobility fluctuations

In 1969, an empirical relation between the conductivity fluctuations showing the 1/f noise and the number of conducting carriers N was proposed by F. N. Hooge [1-114]. It is simply given as [1-114~1-118]:

$$\frac{S_{\sigma}}{\sigma^2} = \frac{S_R}{R^2} = \frac{S_I}{I^2} = \frac{\alpha_H}{fN} \quad (1-37)$$

where S_{σ}/σ^2 is the normalized conductivity noise PSD, S_R/R^2 is the normalized resistance noise PSD, and α_H is a dimensionless parameter usually referred to as the Hooge parameter. The Hooge model has successfully explained the 1/f noise in metals and bulk semiconductors. In Eq. (1-37), the factor N^{-1} means that the fluctuations only result from mobility fluctuations of the conducting carriers [1-115]. It was also proposed that only phonon scattering contributes to the mobility fluctuations [1-117].

Unfortunately, the Hooge model does not suggest any physical explanations of the MF, and cannot provide a further explanation for 1/f noise. In spite of the success of the empirical model, the lack of physical principles is a weakness. Several efforts have been made to develop a theory of MF noise model. However, none of them is widely accepted so far. Nevertheless, it has often been used to compare the noise behavior between different devices or materials.

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The Hooge MF model was applied for the linear and saturation regions in MOSFET operation [1-155~1-158]. In linear region, the normalized current noise spectral density S_{Id}/I_d^2 can be defined involving the total number of inversion carriers $N=WLQ_{inv}/q$ as:

$$\frac{S_{Id}}{I_d^2} = \frac{q\alpha_H}{fWLQ_{inv}} \quad (1-38)$$

Substituting the definition of effective mobility μ_{eff} (cf. Eq. (3-1)) into this equation, it can be seen that the S_{Id}/I_d^2 is inversely proportional to I_d as:

$$\frac{S_{Id}}{I_d^2} = \frac{q\alpha_H\mu_{eff}V_d}{fL^2I_d} \quad (1-39)$$

In saturation region, on the other hand, Q_{inv} is non-uniformly distributed. In fact, it varies parabolically along the channel and reaches zero at the drain region edge. In such case, S_{Id}/I_d^2 is expressed considering the non-uniform inversion charge as:

$$\frac{S_{Id}}{I_d^2} = \frac{q\alpha_H}{fWL^2} \int_0^L \frac{dx}{Q_{inv}(x)} \quad (1-40)$$

Introducing here the gradual channel approximation (GCA) [1-159], the I_d leads to:

$$I_d = W\mu_{eff}Q_{inv}(x)\frac{dV}{dx} \quad (1-41)$$

Substituting the approximated Eq. (1-41) into Eq. (1-40) and assuming a constant mobility along the channel μ_{const} , a similar relationship to Eq. (1-39) is obtained as:

$$\frac{S_{Id}}{I_d^2} = \frac{q\alpha_H}{fWL^2} \int_0^L \frac{dx}{Q_{inv}(x)} = \frac{q\alpha_H}{fWL^2} \int_0^{V_d} \frac{\mu_{eff}W}{I_d} dV = \frac{q\alpha_H\mu_{const}V_d}{fL^2I_d} \quad (1-42)$$

Therefore, MOSFETs in linear and saturation regions show the same S_{Id}/I_d^2 behavior decreasing in inverse proportion to I_d in the Hooge MF model.

1.3.2.3 McWhorter model - Carrier number fluctuations

In 1957, A. L. McWhorter dealt with 1/f noise spectra observed in germanium-based MOS structure, and proposed the charge fluctuations model caused by the tunneling between the bulk and the oxide defects as the physical mechanism of the 1/f noise [1-119]. This model has been considered as a prototype of the carrier number fluctuations (CNF) model, and accepted widely [1-120~1-123,1-158,1-160]. The CNF in a NMOS FET is schematically illustrated in Fig.1-27 [1-97]. Generally, it is

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understood that the fluctuations of drain current I_d stem from the fluctuations of the oxide charges, and the oxide charge fluctuations result from the dynamic trapping and de-trapping of carriers between the channel and oxide traps located near the interface. The oxide charge fluctuation δQ_{ox} is equivalent to the flat-band voltage fluctuation δV_{fb} by considering the V_{fb} definition in Eq. (1-12), and it is written as:

$$\delta Q_{ox} = -C_{ox} \delta V_{fb} \quad (1-43)$$

$$\text{with } V_{fb} = \phi_{ms} - \frac{Q_{ox}}{C_{ox}} \quad (1-12)$$

Therefore, the drain current fluctuation δI_d can be derived as [1-158,1-160]:

$$\delta I_d = \frac{\partial I_d}{\partial Q_{ox}} \delta Q_{ox} = \frac{\partial I_d}{\partial V_{fb}} \delta V_{fb} = -\frac{\partial I_d}{\partial V_g} \delta V_{fb} = -g_m \delta V_{fb} \quad (1-44)$$

here noticing that V_g and V_{fb} play a symmetric role. Consequently, a relationship between the S_{Id}/I_d^2 and the flat-band voltage noise PSD S_{Vfb} is given as:

$$\frac{S_{Id}}{I_d^2} = \frac{g_m^2}{I_d^2} S_{Vfb} \quad (1-45)$$

From Eq. (1-45), it is shown that the normalized drain current noise S_{Id}/I_d^2 in the CNF model is proportional to $(g_m/I_d)^2$. The S_{Id}/I_d^2 curve shows a plateau in weak inversion region, whereas the curve decreases in inverse proportion to I_d^2 in strong inversion region. An illustration of the S_{Id}/I_d^2 behavior difference between CNF and Hooge MF models from subthreshold to strong inversion regions is shown in Fig.1-28.

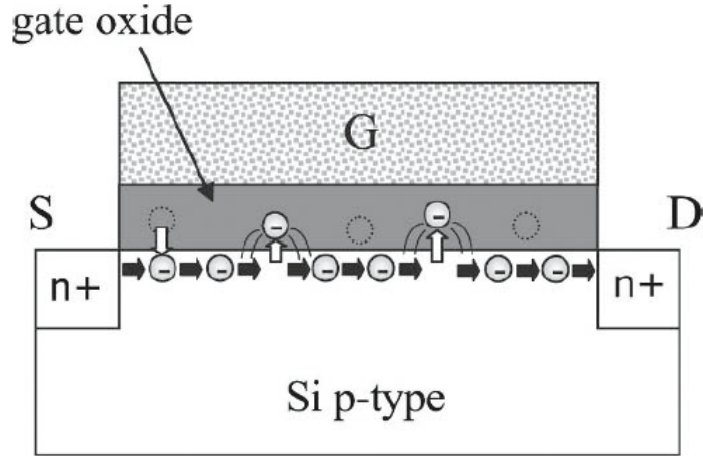


Fig. 1-27. Schematic illustration of electrons in the channel of a MOSFET moving in and out of traps, giving rise to fluctuations in the inversion charge density and thereby the drain current [1-97].

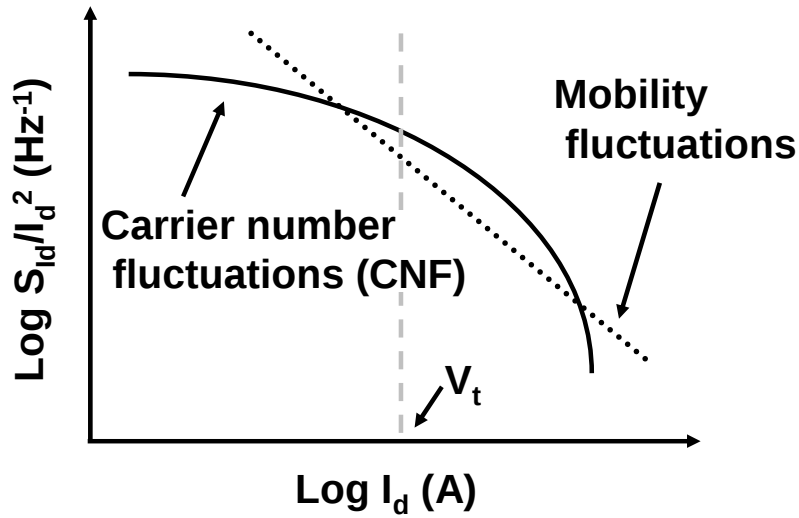


Fig. 1-28. Schematic of the mobility fluctuation noise and carrier number fluctuation noise from subthreshold to the strong inversion regime.

Equation (1-45) is a common expression without supposing the mechanism of the flat-band voltage fluctuations. Physical carrier trapping and de-trapping between the gate oxide and the channel by the tunneling is assumed as the mechanism, and it is the

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essence of McWhorter model as the explanation of 1/f noise in MOSFETs. In the tunneling process, the trapping time constant τ_{trap} is given by:

$$\tau_{trap} = \tau_0(E) \cdot \exp\left(\frac{z}{\lambda}\right) \quad (1-46)$$

where τ_0 is the time constant based on Shockley-Read-Hall (SRH) process and often taken as 10^{-10} s, z is the distance of a trap located in the gate oxide from the interface ($z=0$), and λ is the tunneling attenuation length of the electron or hole wave function in the gate oxide. The value of λ is predicted by the Wentzel-Kramers-Brillouin (WKB) approximation, and is defined as [1-120]:

$$\lambda = \left(\frac{4\pi}{h} \sqrt{2m^* \Phi_B} \right)^{-1} \quad (1-47)$$

where Φ_B is the tunneling barrier height felt by the carriers at the interface, h is the Planck's constant, and m^* is the effective mass of the carriers. The values of λ depends on the gate oxide materials, however the reported values lie in the range of ≈ 0.07 - 0.21 nm [1-97]. Especially, λ is estimated as ≈ 0.1 nm in the Si/SiO₂ gate. For the electron tunneling, this yields $z=2.3$ nm and 0.9 nm for a frequency of 1Hz and 1MHz, respectively. Thus, oxide traps located near the channel interface are fast, and those located more than 2.5 nm from the interface are slow contributing to high and low frequency range, respectively.

Based on the tunneling process model, S_{Vfb} can be evaluated as:

$$S_{Vfb} = \frac{q^2 kT \lambda N_t}{f^\gamma WLC_{ox}^2} \quad (1-48)$$

where N_t is the gate oxide trap density per volume in unit of $eV^{-1}cm^{-3}$. The frequency exponent γ deviates from 1 if the trap density is non-uniformly distributed for the depth [1-161,1-162]. It is noticed that the responsible traps for the fluctuations are those located within $2kT$ range from quasi-Fermi energy level (*i.e.* total $4kT$ range) [1-120].

The band diagram shown in Fig.1-29 illustrates the tunneling transition of carrier (electron) from the Si substrate to the gate oxide, in (i) direct process [1-120] or (ii) indirect one via interface traps as steppingstones [1-163]. The window of traps with $4kT$ range seen at a particular bias point is shown as the shaded area. From the interface trap density D_{it} studies, the D_{it} often shows a U-shaped distribution as a function of energy

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in the Si band gap, with an increased value toward the conduction or valence band edges [1-164]. Assuming that N_t follows the same behavior as D_{it} , the N_t is predicted to increase with V_g bias, because the quasi-Fermi level approaches the band edge E_C or E_V (e.g. the quasi-Fermi level for electron E_{Fn} is close to the E_C in Fig.1-29). Owing to the band bending of the gate oxide, the N_t distribution in the traps window could become non-uniform. Thus, the frequency exponent γ could also deviate from 1 in inversion region.

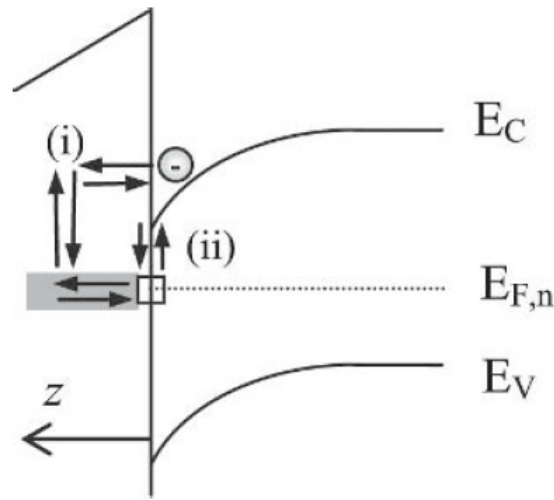


Fig. 1-29. Energy band diagram showing the tunneling transitions of electrons between the conduction band and traps in the gate oxide, (i) corresponds to direct tunneling and (ii) to indirect tunneling via interface traps [1-97].

1.3.2.4 CNF+CMF model

In 1990, Hung *et al.* suggested a unified model which combines the CNF and the MF frameworks [1-153]. In 1991, a more popular definition was proposed by Ghibaudo *et al.* [1-154]. In this advanced theory, the influence on the conduction through the Coulomb interaction with the trapped carriers is also considered. This means that the oxide charge fluctuations, *i.e.* the CNF, can additively induce a change of the mobility which causes an extra I_d variation. Based on this idea for the MF correlated to the CNF, the drain current fluctuations δI_d can be expressed with Eq. (1-44) as:

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$$\delta I_d = \frac{\partial I_d}{\partial V_{fb}} \delta V_{fb} + \frac{\partial I_d}{\partial \mu_{eff}} \delta \mu_{eff} = -g_m \delta V_{fb} + \frac{\partial I_d}{\partial \mu_{eff}} \frac{\partial \mu_{eff}}{\partial Q_{ox}} \delta Q_{ox} \quad (1-49)$$

Since I_d is proportional to effective mobility μ_{eff} (cf. Eq. (3-1)) then this equation yields to:

$$\delta I_d = -g_m \delta V_{fb} + \frac{I_d}{\mu_{eff}} \frac{\partial \mu_{eff}}{\partial Q_{ox}} \delta Q_{ox} = -g_m \delta V_{fb} - \frac{I_d}{\mu_{eff}} \frac{\partial \mu_{eff}}{\partial Q_{ox}} C_{ox} \delta V_{fb} \quad (1-50)$$

Here a scattering parameter can be introduced to reflect the coupling between the oxide charge and the mobility variations. The Coulomb scattering coefficient α_{sc} is defined as:

$$\alpha_{sc} = -\frac{\partial(1/\mu_{eff})}{\partial Q_{ox}} = \frac{1}{\mu_{eff}^2} \frac{\partial \mu_{eff}}{\partial Q_{ox}} \quad (1-51)$$

Substituting Eq. (1-51) into Eq. (1-50), then δI_d is written as:

$$\delta I_d = -g_m \delta V_{fb} - I_d \alpha_{sc} \mu_{eff} C_{ox} \delta V_{fb} = -g_m \left(1 + \alpha_{sc} \mu_{eff} C_{ox} \frac{I_d}{g_m} \right) \delta V_{fb} \quad (1-52)$$

Consequently, a definition of S_{Id}/I_d^2 in the “carrier number fluctuations with correlated fluctuations (CNF+CMF)” model can be given by:

$$\frac{S_{Id}}{I_d^2} = \left(\frac{g_m}{I_d} \right)^2 \left(1 + \alpha_{sc} \mu_{eff} C_{ox} \frac{I_d}{g_m} \right)^2 S_{V_{fb}} \quad (1-53)$$

In Eq. (1-53), the first term corresponds to the CNF component and the second term indicates the CMF factor by trapped charges. If α_{sc} is close to zero, it means that CMF does not influence the LFN and the behavior can be described by the CNF only. In contrast, when the α_{sc} is high enough, the slope of S_{Id}/I_d^2 vs. I_d in strong inversion region is impacted by the CMF and departed from the proportion to I_d^{-2} . However, CMF does not influence the noise behavior in weak inversion region, and CNF is predominant.

A constant α_{sc} has been frequently used in the LFN models, but this is not physically correct for several reasons, such as the screening effect [1-109,1-127]. In practice, α_{sc} is expected to decrease with increasing inversion charge density Q_{inv} due to the screening effect. In addition, the product of $\alpha_{sc} \mu_{eff} = \mu_{eff}^{-1} \delta \mu_{eff} / \delta Q_{ox}$ is anticipated as a key and fairer parameter, which is called Coulomb scattering parameter, in the CMF investigation [1-137,1-165].

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The relationship between the drain current noise PSD S_{Id} and the input gate voltage noise counterpart S_{Vg} is expressed as [1-154]:

$$S_{Vg} = \frac{S_{Id}}{g_m^2} = \left(1 + \alpha_{sc} \mu_{eff} C_{ox} \frac{I_d}{g_m} \right)^2 S_{Vfb} \quad (1-54)$$

It is thus confirmed that I_d noise spectrum can be simply transformed to the V_g noise characteristic by measuring g_m .

Lastly, a relationship between MOSFET's operation mode and evaluation of CNF/CMF components is illustrated in Fig.1-30. The CNF component is usually extracted at subthreshold region exhibiting plateaued noise level, whereas the CMF component can become predominant and be determined at inversion region. Moreover, ITRS requirements for upper limit of $1/f$ noise level are defined at an inversion condition ($V_g - V_t = 0.2V$) [1-21].

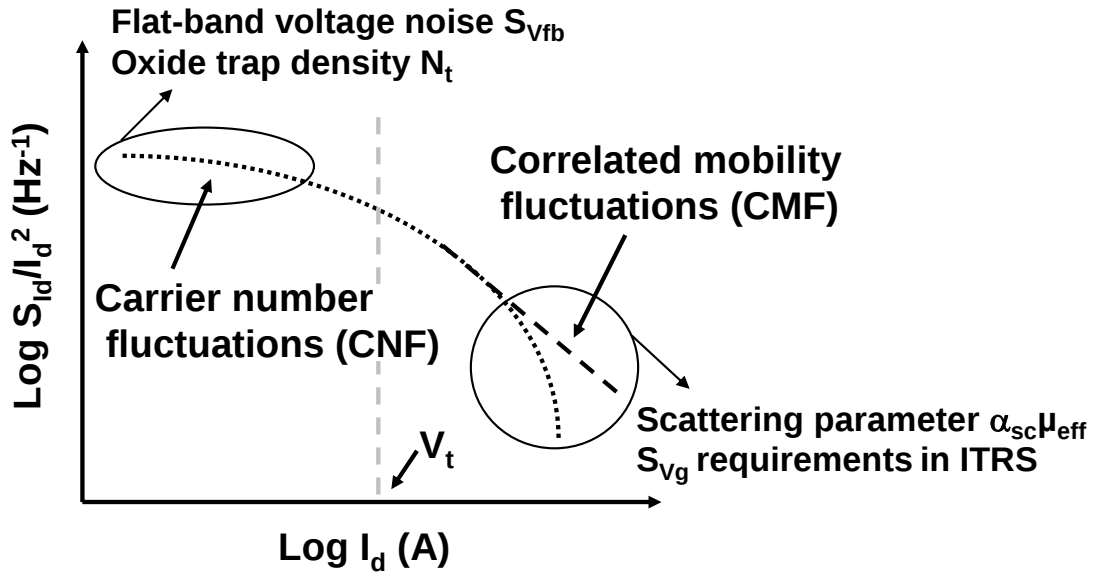


Fig. 1-30. Schematic of the mobility fluctuation noise and carrier number fluctuation noise from subthreshold to the strong inversion regime.

1.4 Purposes and scopes of this work

Future MOSFET technology node should require MG architectures. However, it became difficult to rigorously examine the electrical characterizations of MG FETs, especially for NW devices, with general characterization method based on capacitance measurement (such as split C-V). Low-frequency noise (LFN) also provides deep insights into electrical properties of the gate oxide/channel interface in MOSFETs. Moreover, it is a powerful advantage that LFN characterization has no lower limit of the necessary MOSFET channel area. Therefore, LFN measurement can be a powerful characterization technique for ultra-scaled NW MOSFETs. Consequently, measurements and understanding of LFN are highly important in order to evaluate the electrical interface properties and the performance in MOSFETs.

Tables 1-2 and 1-3 summarize previous reports of MG FETs with conventional gate oxide (mainly SiO₂/poly-Si gate stack) and with Hf-based high- κ /metal gate stack, respectively. Nowadays, a number of reports for LFN measurement even in MG devices (for FinFETs [1-130~1-143] and for NW FETs [1-53,1-144~1-152]) have been published. Concerning LFN characterizations in recent MG devices, the origin of $1/f$ noise is mainly attributed to unified CNF+CMF. In fact, the model is suitable for most of MG devices, and have been discussed in previous reports [1-53,1-130,1-131,1-134,1-137,1-138,1-141~1-144,1-146,1-147,1-149~1-152]. However, few reports of comprehensive study on each parameter defined in the CNF+CMF model as functions of MOSFET channel size (width W and length L), architectural difference (planar vs. MG), and technological parameters (channel orientation, strain effect, etc...), have been published.

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Table 1-2. Previous reports of MG FETs with conventional gate oxide.

Authors	Year	Ref.	Channel material	Gate type	Gate material	LFN study
S. D. Suk, <i>et al.</i>	2005	[1-47]	Si	GAA	SiO ₂ /TiN	No
K. H. Yeo, <i>et al.</i>	2006	[1-166]				
S. D. Suk, <i>et al.</i>	2007	[1-167]				
M. Li, <i>et al.</i>	2007	[1-168]	Si, sSi			
	2009	[1-169]	Si			
J. Zhuge, <i>et al.</i>	2009	[1-144]				
S.-H. Lee, <i>et al.</i>	2012	[1-150]				sSi
	2014	[1-152]				
N. Singh, <i>et al.</i>	2006	[1-48] [1-170]	Si	GAA	SiO ₂ /poly-Si	No
Y. Jiang, <i>et al.</i>	2008	[1-171]			SiO ₂ /NiSi	
C. Wei, <i>et al.</i>	2009	[1-145]			SiO ₂ /poly-Si	Yes
		[1-146]			SiO ₂ /NiSi	
		[1-135]		Tri-gate	SiO ₂ /poly-Si	
F. Crupi, <i>et al.</i>	2006	[1-130]	Si	Tri-gate	SiON/poly-Si	Yes
T. Ohguro, <i>et al.</i>	2009	[1-133]	Si	Tri-gate	SiON/poly-Si	Yes
J. Chen, <i>et al.</i>	2008	[1-59]	Si	GAA	SiO ₂ /poly-Si	No
	2010	[1-172]				
M. Saitoh, <i>et al.</i>	2010	[1-60]	Si	Tri-gate	SiO ₂ /poly-Si	No
	2012	[1-173]				Yes
	2013	[1-151]				
R.-H. Baek, <i>et al.</i>	2011	[1-148]	Si	GAA	SiO ₂ , SiON	Yes
S. Sato, <i>et al.</i>	2011	[1-174]	Si	GAA	SiO ₂ /poly-Si	No
W. Feng, <i>et al.</i>	2011	[1-149]	Si	Tri-gate	SiO ₂ /poly-Si	Yes

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Table 1-3. Previous reports of MG FETs with Hf-based high- κ /metal gate stack.

Authors	Year	Ref.	Channel material	Gate type	Gate material	LFN study
T. Ernst, <i>et al.</i>	2006	[1-50]	Si	GAA	HfO ₂ /TiN	No
K. Tachi, <i>et al.</i>	2009	[1-53]	Si, SiGe			Yes
	2010	[1-175]	Si			No
M. Cassé, <i>et al.</i>	2010	[1-164]				Yes
D. Jang, <i>et al.</i>	2010	[1-147]	SiGe			No
L. Hutin <i>et al.</i> ,	2010	[1-176]	Si, SiGe	Tri-gate		
M. Fulde, <i>et al.</i>	2007	[1-132]	Si	Tri-gate	HfO ₂ /TiN	Yes
K. Bennamane, <i>et al.</i>	2009	[1-134]	Si	Tri-gate	HfO ₂ /TiN	Yes
S. Bangsaruntip, <i>et al.</i>	2009	[1-177]	Si	GAA	Hf-based oxide/TaN	No
	2013	[1-178]				
C. Auth, <i>et al.</i>	2011	[1-20]	Si, sSi	Tri-gate	Hf-based oxide/metal	No
C. G. Theodorou, <i>et al.</i>	2012	[1-137]	Si	Tri-gate	HfO ₂ /TiN	Yes
	2013	[1-141]				
J. W. Lee, <i>et al.</i>	2013	[1-142] [1-143]	Si	Tri-gate	HfO ₂ /TiN	Yes
B. Rajamohanan, <i>et al.</i>	2012	[1-138]	SiGe	Tri-gate	HfO ₂ /TiN	Yes
T. Romeo, <i>et al.</i>	2012	[1-139]	SiGe	Tri-gate	HfO ₂ /TiN	Yes
R. Coquand, <i>et al.</i>	2012	[1-49]	Si	Tri-gate	HfSiON/TiN	No
		[1-179]	Si, sSi	Tri- & Ω-gate		
2013	[1-180]	Tri-gate				
M. Cassé, <i>et al.</i>	2012	[1-181]	Si, sSi	Ω-gate		
S. Barraud, <i>et al.</i>	2012	[1-182]				
	2013	[1-183]				
P. Nguyen, <i>et al.</i>	2014	[1-184]	Si, SiGe			

According to Eqs. (1-25), (1-26), (1-48), (1-53), and (1-54), contribution of MOSFET scaling (channel width W and length L , and EOT) to LFN based on

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CNF+CMF is derived as:

$$S_{Vg} = \frac{S_{Id}}{g_m^2} \propto \frac{1}{WLC_{ox}^2} \propto \frac{EOT^2}{WL} \quad (1-55)$$

Therefore, it is predicted that LFN improves with EOT scaling, whereas the channel size scaling increases the noise level. However, EOT scaling techniques by nitridation of the SiO₂ gate oxide (leading to SiON) and by using high-κ dielectric such as Hf-based oxide generally introduces charged traps into the oxide, which become origin of higher 1/f noise. Figure 1-31 by Morfouli *et al.* in 1996 [1-185] shows increase of oxide trap density N_t with increase of incorporated nitrogen percentage for the Si/SiO₂ interface. M. Fulde *et al.* reported in 2007 that the S_{Vg} level increases as Hf content increases from SiON to pure HfO₂, whereas EOT and gate leakage current are reduced owing to Hf (Fig.1-32) [1-132].

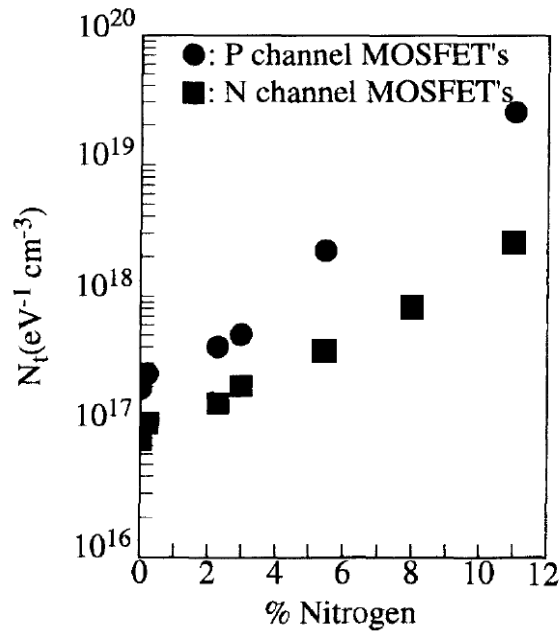


Fig. 1-31. Oxide trap density N_t variation with nitrogen percentage for p- and n-channel devices [1-185].

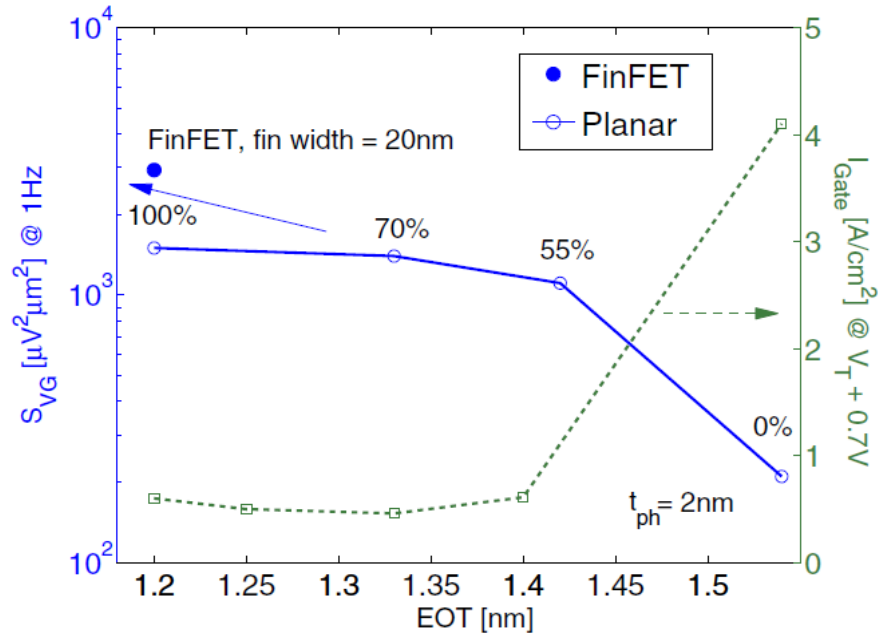


Fig. 1-32. Gate leakage and corresponding 1/f-noise for varying Hf content [1-132].

In intensive investigations of high- κ /metal gate stack, a number of LFN researches for Hf-based gate dielectric have been reported even in MG devices [1-132,1-134, 1-137~1-143]. But, there are few reports of LFN study in NW FETs with high- κ /metal gate stack. Tachi *et al.* reported a figure exhibiting LFN behavior of vertically-stacked GAA NWs in 2009, as shown in Fig.1-33 [1-53]. They found that the trap density of Si NWs is higher than the value of planar FD FET. Therefore, there is a concern about the degraded interface quality in NW FETs with Hf-based high- κ /metal gate.

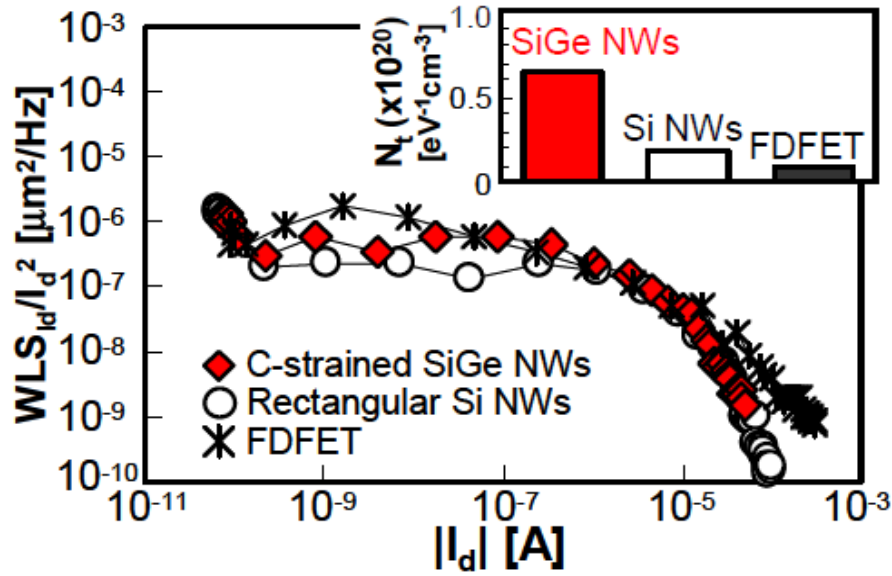


Fig. 1-33. Low-frequency noise of Si and c-strained SiGe NWs. Inserted figure is a comparison of oxide trap density (N_t). L_G and W_{NW} are $\sim 290\text{nm}$ and $\sim 20\text{nm}$, respectively [1-53].

Similarly with the report by Tachi *et al.*, Zhuge *et al.* reported LFN characterization of GAA NW with thermal Si oxide (SiO_2) with higher oxide trap density than conventional $\text{SiO}_2/\text{poly-Si}$ gate stack in 2009 [1-144]. They considered that the degradation could be caused by various surface orientations and small diameter of GAA NW. On the other hand, Crupi *et al.* reported similar values of oxide trap density between tri-gate and planar NMOS FETs with $\text{SiON}/\text{poly-Si}$ gate stack in 2006, as shown in Fig.1-34 [1-130]. Contributions of different crystallographic orientations of channel surface among the interfaces (*i.e.* MG top (and bottom) surface vs. side-walls) into oxide trap density should be thus evaluated in detail.

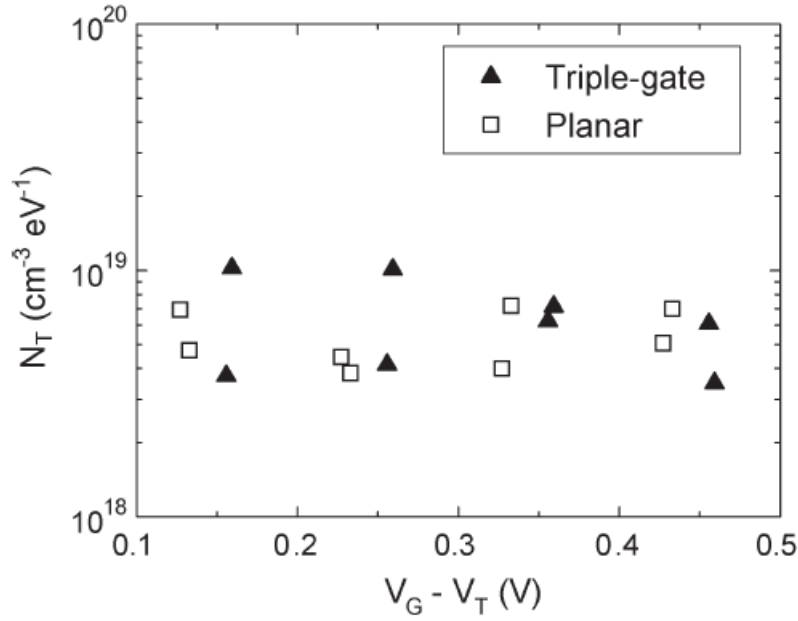


Fig. 1-34. Effective trap density versus gate voltage overdrive for the 30-fin triple-gate devices ($W_{\text{FIN}}=60\text{nm}$, $L=1\mu\text{m}$) and planar devices ($W \times L=1\mu\text{m} \times 1\mu\text{m}$). No significant difference between the two structures is observed. [1-130].

Meanwhile, LFN level ($S_{\text{Id}}/I_{\text{d}}^2$) decrease was observed in SOI tri-gate NW FETs with $\text{SiO}_2/\text{poly-Si}$ by Feng *et al.* in 2011 [1-149], and in GAA Si NW FETs with SiO_2/TiN by Lee *et al.* in 2012 as shown in Fig.1-35 [1-150]. It could be ascribed to quantum confinement of carriers due to large surface/volume ratio of NW, as shown in the simulation results in SOI tri-gate NW FETs by Feng *et al.* in 2011 (Fig.1-36 and 1-37) [1-149]. The deeper location of electron charge-centroid from the interface in the NW channel in comparison with planar FET results from the quantum confinement effect. This volume inversion impact may also be observed in aggressively scaled NWs with Hf-based high- κ /metal gate stack.

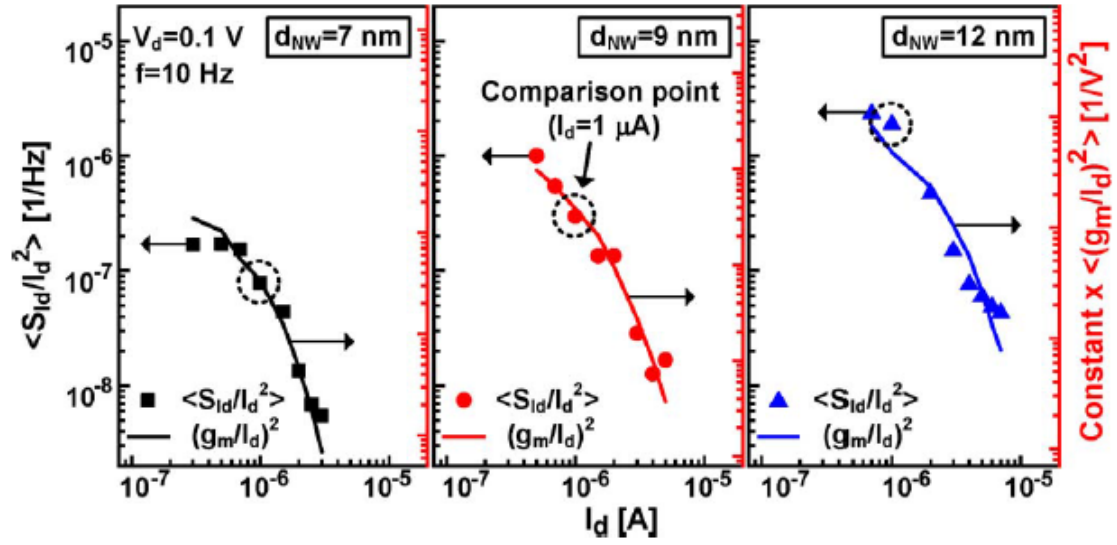


Fig. 1-35. Averaged noise spectral densities (symbols) $\langle S_{I_d}/I_d^2 \rangle$ and (lines) $\langle (g_m/I_d)^2 \rangle$ versus I_d at $V_d = 0.1$ V and $f = 10$ Hz for 7-, 9-, and 12-nm d_{NW} , respectively. All the left axes represent $\langle S_{I_d}/I_d^2 \rangle$, whereas all the right axes (red colored) represent $\langle (g_m/I_d)^2 \rangle$ multiplied by a constant. The symbols within the dotted circle at the same current level (1 μA) are for the comparison of $\langle S_{I_d}/I_d^2 \rangle$ for each d_{NW} . [1-150].

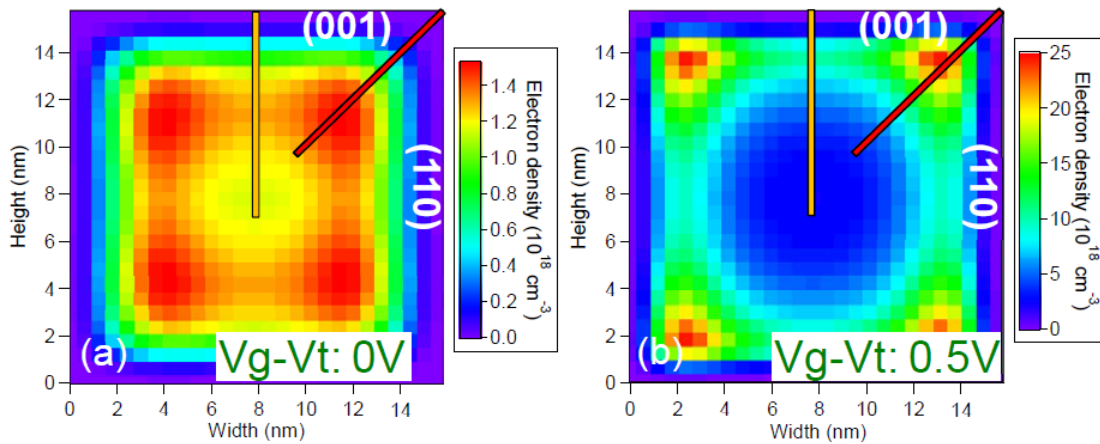


Fig. 1-36. Electron density mappings of NW FET with (a) $V_g - V_t = 0$ V and (b) 0.5 V, demonstrating the charge-centroid position (red in color) moving to the corners of the NW with increasing V_g . The density profiles along the lines are shown in Fig.1-37 [1-149].

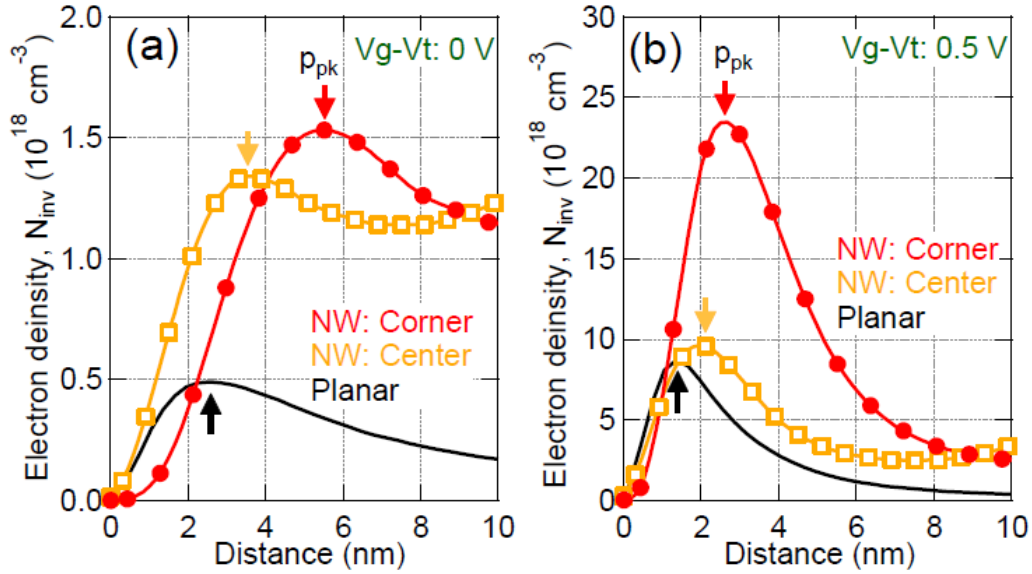


Fig. 1-37. Change in electron density along a diagonal (corner) and from the center of an edge in Fig.1-36 as a function of distance from the interface for (a) $V_g - V_t = 0 \text{ V}$ and (b) 0.5 V , showing that the peak position p_{pk} of the electron density in the NW is much further from the interface than that of a planar FET. Taking the electric permittivity into account, the 2-nm-shift in the charge-centroid causes a change of 0.7nm in the equivalent oxide thickness. Nevertheless, the higher drivability is maintained due to the large value of N_{inv} in the NW [1-149].

Influence of strain technology into the interface quality has also been a significant concern, and has been studied. Contributions of strain effect to the interface quality and mobility fluctuations are in fact concerns. For improvement of NMOS performance, tensile strained Si fabricated on SiGe virtual layers has been used and reported the LFN characteristics mostly for planar FETs [1-97,1-186~1-192]. The upgraded [1-186~1-188], constant [1-97], and degraded [1-189~1-192] LFN results compared with reference Si devices have been reported. For example, Fig.1-38 shows a deteriorated oxide trap density with increase of Ge content in strained-relaxed-buffer (SRB) SiGe virtual layer reported by Wang *et al.* in 2007 [1-192]. LFN data of sSi NW is necessary for future CMOS node.

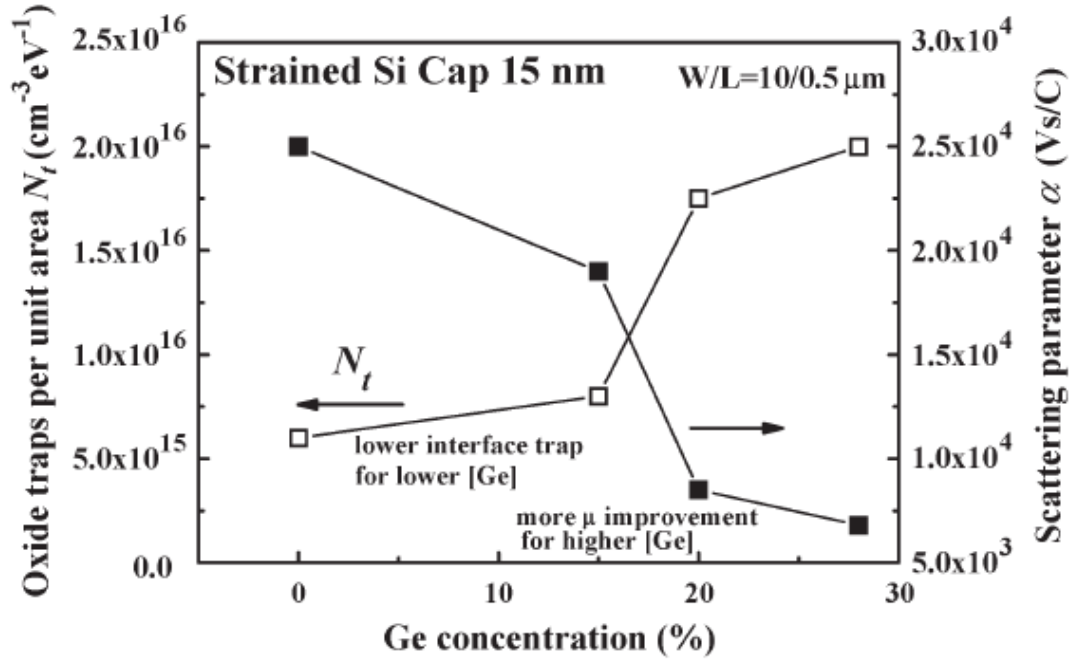


Fig. 1-38. Relationship between equivalent oxide traps per unit area N_t and scattering parameter α and with different Ge content of SRB layers [1-192].

For PMOS enhancement, compressively strained channel has been fabricated by SiGe source/drain (S/D) and SiGe channel formations. There are few reports of LFN study for SiGe S/D technique in planar [1-193~1-195] and NW [1-152] FETs. Also, LFN properties for SiGe channel FinFETs [1-138,1-139] and NWs [1-53,1-147] have been investigated. As Tachi *et al.* reported a 3.5 times higher oxide trap density for SiGe NWs than for Si NWs (Fig.1-33 [1-53]), there is a concern about the interface quality.

Finally, upper limit requirements of $1/f$ LFN level defined by the ITRS for future CMOS logic circuits consisting of MG FETs should be accomplished. The ITRS requirements (in 2013 edition) of gate voltage noise S_{V_g} normalized by channel area are summarized in Fig.1-39 [1-21].

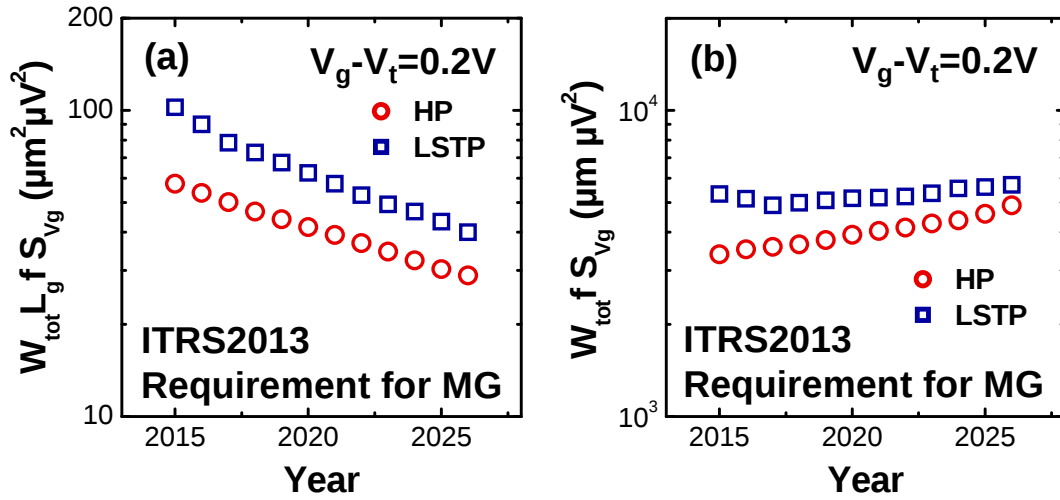


Fig. 1-39. ITRS requirements for future high performance (HP) and low standby power (LSTP) logic circuits consisting of MG FETs. Upper limit requirements of gate voltage noise S_{V_g} normalized by (a) channel area ($W_{\text{tot}} \times L_g$), and by (b) gate length L_g only, are plotted as a function of year between 2015 and 2026 (sourced from ITRS 2013 data in Table RFAMS1 CMOS technology requirements [1-21]).

As a consequence, important concerns about LFN characteristics in ultra-scaled NW MOSFETs should be discussed in detail as follows;

- (i) CNF+CMF model parameters as a function of channel size down to NW
- (ii) NW FETs with advanced Hf-based high- κ /metal gate stack
- (iii) Difference of crystallographic orientations between channel top and etched side-wall surfaces
- (iv) Large channel surface/volume ratio (volume inversion effect?) of NW
- (v) Strained NW technology;

NMOS - tensile strain *PMOS* - compressive strain
- (vi) ITRS requirements for future CMOS logic circuits comprised of MG FETs

Accordingly, the purpose of this work is experimental and comprehensive investigation of electrical characteristics in the gate oxide/channel interface by LFN and carrier

Chapter 1. Introduction

transport measurements in ultra-scaled NW MOSFETs with Hf-based high- κ /metal gate stack, in order to evaluate the significant concerns of (i)-(vi).

Our silicon nanowire (NW) MOSFETs were fabricated from advanced fully-depleted SOI (FD-SOI) substrate, and with Hf-based high- κ /metal gate stack (HfSiON/TiN) in order to suppress detrimental SCE and gate leakage. In addition, strain introduction technologies to the channel were additively processed to efficiently improve the MOSFET's performance. Tensile strained-SOI substrate was used for NMOS FETs, whereas compressive stressors were used for PMOS devices. Compressively strained Si channel can be processed by raised SiGe S/D and contact-etch-stop-layer (CESL) formations. In addition, compressively strained SiGe-on-insulator channel was also fabricated for further high-performance PMOS FETs. These fabrication technologies and processes are described in detail in chapter 2. Then, measurement methodologies are explained in chapter 3.

The gate oxide/channel interface characteristics in the various NW MOSFETs are examined on carrier transport characterizations as the channel properties in chapter 4, and on LFN characterizations for the interface properties in chapter 5. In chapter 4, DC gate voltage dependent drain current (I_d - V_g), temperature dependent effective mobility (μ_{eff}), and extracted low-field mobility (μ_0) characteristics are investigated. In chapter 5, drain current noise S_{Id}/I_d^2 behavior, parameter evaluations based on advanced $1/f$ noise model (involving flat-band voltage noise $S_{V_{fb}}$, Coulomb scattering parameter $\alpha_{sc}\mu_{\text{eff}}$, and oxide trap density N_t), and drain bias dependency of noise (S_{Id}/I_d^2 - and $S_{V_g-V_d}$) behavior compared with the ITRS requirements are characterized.

Finally, this study of electrical characterizations for the oxide/channel interface in NW MOSFETs is concluded in chapter 6. The perspectives of LFN investigation on future device nodes are also described.

Chapter 1. Introduction

- MOSFET downscaling
- Key concepts for advanced MOSFETs
SOI, multi-gate, high- κ /metal gate, stressors
- Low-frequency noise
- Purposes and scopes of this thesis

Chapter 2. Nanowire MOSFETs fabrication

- Ω -gate NW with HfSiON/TiN gate stack
- Tensile strained SOI for PMOS
- Compressive strained SGOI, SiGe-S/D,
and CESL for PMOS

Chapter 3. Measurement methods

Chapter 4. Carrier transport characterizations

- I_d - V_g characteristics: V_t , **DIBL**, **SS**, I_{ON}
- Effective mobility: $\mu_{eff}(T)$ - W_{top}
- Low-field mobility: μ_0 - L_g

Chapter 5. Low-frequency noise characterizations

- $1/f$ S_{I_d}/I_d^2 characteristics
- CNF+CMF model parameter: S_{Vfb} , $\alpha_{sc}\mu_{eff}$
- Oxide trap density N_t
- V_d dependence and ITRS requirements

Chapter 6. Summary and Conclusions

Fig. 1-40. Outline diagram in this work on electrical characteristics of the gate oxide/channel interface in ultra-scaled NW MOSFETs.

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2.1 Process step overview

Our NW FETs were fabricated starting from 300nm (001) SOI or sSOI wafers with $\approx 10\text{-}15\text{nm}$ Si layer and 145nm BOX, and following the process steps given in Fig.2-1. FD-SOI-based device fabrication results in an undoped *i.e.* high purity channel. For PMOS enhancement, a process to form compressively strained SGOI was performed in some SOI wafers. It should be noticed that following device fabrication processes can introduce slight stress/strain to the channel. In our devices, additional preparation (sSOI for NMOS) and processes (SGOI, SiGe-S/D, compressive CESL for PMOS) were performed to introduce large tensile/compressive strain in plane to the channel.

The devices have been patterned by using the top-down approach, consisting of mesa isolation and hybrid DUV/e-beam lithography followed by a resist trimming process [2-1~2-6]. It was carried out in order to achieve NW structures as narrow as 10nm (top-view width). A Hf-based high- κ /metal gate stack (HfSiON/TiN) was then processed. After the gate patterning, first nitrided spacer (SiN) was formed, and then raised S/D were realized by epitaxial Si (or SiGe for PMOS improvement), in order to get low parasitic resistance. Next, S/D implantation with phosphorus for NMOS and with boron for PMOS, respectively, was performed in twice. By the first lightly doped drain (LDD) and second highly doped drain (HDD) implantation processes, SCE and hot-carrier generation are effectively reduced. Compressive CESL was deposited to enhance the performance in some PMOS devices. After dopants activation and silicidation of S/D regions, the fabrication ended with a standard back-end of line (BEOL) process.

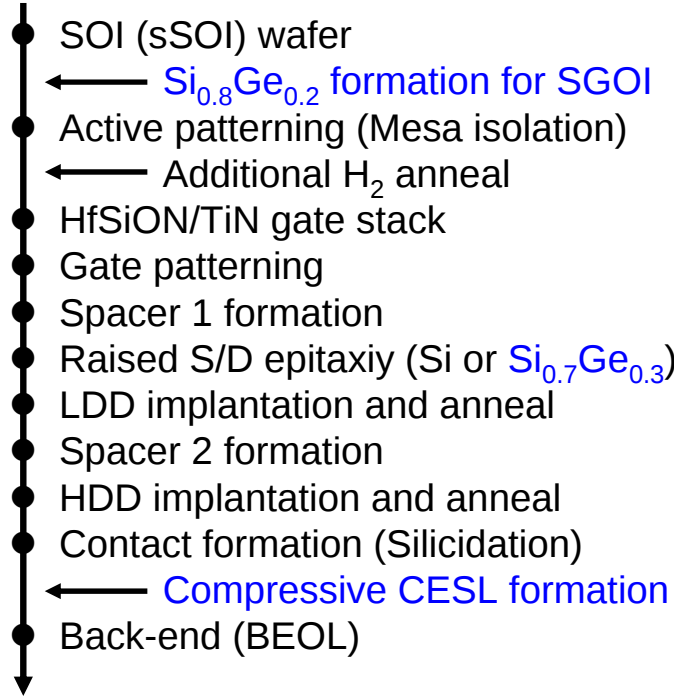


Fig. 2-1. Process integration schematic of our MOSFETs.

2.2 Key device parameters

2.2.1 Architectural splits

FET structures with gate length L_g were processed from $10\mu\text{m}$ down to 17nm . Varied top-view width W_{top} of the channel were fabricated from $10\mu\text{m}$ (the widest FET) down to $\approx 10\text{nm}$ (NW FET). We expediently defined our devices with narrower W_{top} than $\approx 30\text{nm}$ as Ω -gate and tri-gate NWs in this work. The thickness of Si, strained-Si, and SiGe layers under the gate oxide is equivalent to the NW height (H_{NW}), which is also equal to all the device heights in each technology configuration.

For the convenient investigations, the total effective width W_{tot} is readily given by:

$$W_{\text{tot}} = N_{\text{ch}} (W_{\text{top}} + 2H_{\text{NW}}) \quad (2-1)$$

where N_{ch} is number of parallel channel fingers (1 or 50 in this work). The conduction in $[110]$ -oriented NW takes place in (001) top surface and (-110) left- and right-side

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surfaces (side-walls), respectively. On the other hand, in [100]-oriented NWs fabricated by 45°-rotated process, both top and side-walls have the same conduction as (100) surface. Also, it should be noticed that small bottom surfaces of Ω -gate structure may contribute to the MOSFET performance.

2.2.2 High- κ /metal gate stack

All the devices have a high- κ /metal gate (HfSiON/TiN) stack consisting of ≈ 2.5 nm HfSiON deposited by chemical vapor deposition (CVD), and 5nm TiN deposited by atomic layer deposition (ALD) with capped 50nm poly-Si. Note that a ≈ 0.8 nm SiO₂ interfacial layer (IL) between the body and HfSiON was formed. This leads to $EOT \approx 1.2$ -1.3nm calculated by Eqs. (1-18), (1-25), and (1-26). The EOT value is maintained from conventional 2D FETs down to 50-channel NW FETs for both N- and PMOS cases (cf. Section 3.2, “C_{gc}-V_g measurement”).

2.2.3 Additional H₂ anneal

Additional hydrogen anneal has been performed to obtain a circular-like cross-sectional shape of the NW channel. By applying this process, Ω -gate and GAA architectures with rounded corner (semi-circular shape) have been fabricated [2-7~2-10]. The H₂ annealing was processed before the gate stack formation. In previous reports by Tachi *et al.* in 2009 and 2010 [2-8,2-9], circular GAA Si NWs were formed as shown in Fig.2-2. As a consequence, the effective mobility of electron at high inversion charge density is improved, whereas the mobility at low inversion region is degraded, in comparison with the rectangular NWs. This means that their surface roughness is reduced by the H₂ annealing process, and the interface trap density is increased in the rounded NWs.

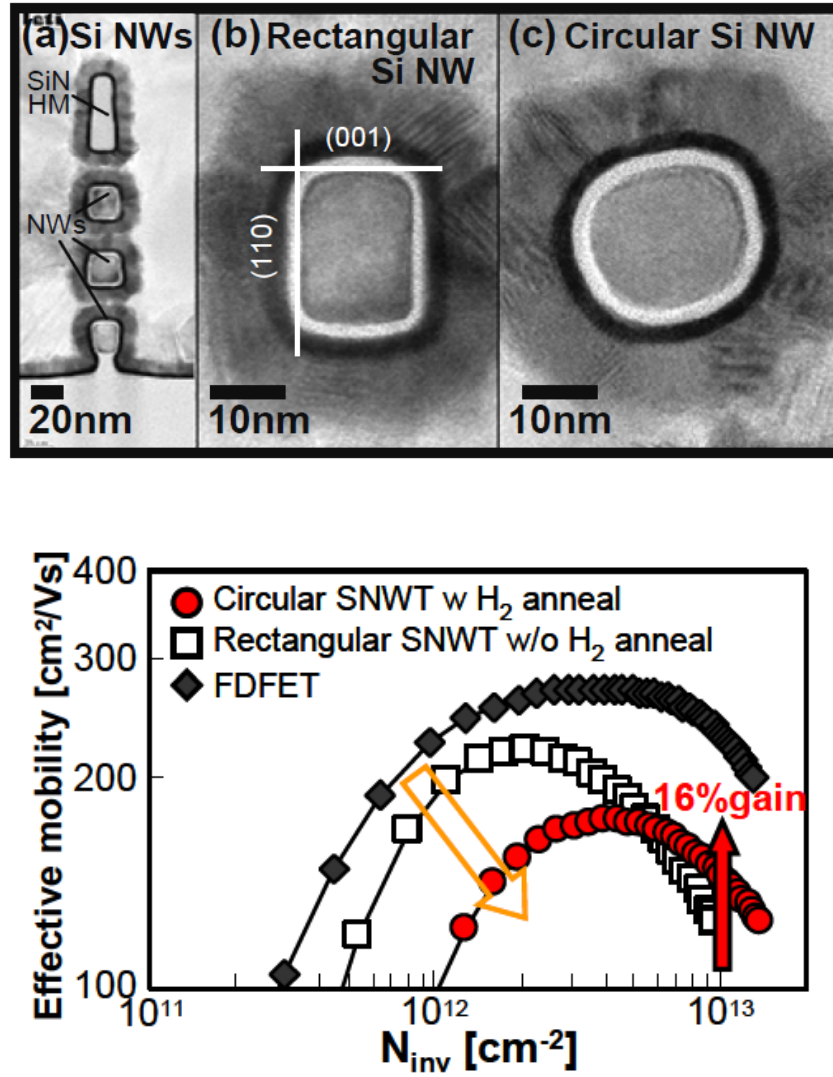


Fig. 2-2. Cross-sectional TEM micrographs of 3D-stacked SNWTs with high- κ /metal gate stacks; (a) 3D-stacked SNWTs, (b) enlarged image of a rectangular nanowire, (c) circular nanowire by H_2 annealing. Impact of H_2 annealing; the high field mobility is increased by H_2 anneals, whereas the low field mobility is degraded. Rectangular and circular NWs are $W_{\text{NW}}/H_{\text{NW}}=15\text{nm}/20\text{nm}$ and 20nm in diameter ((b) and (c)) [2-8].

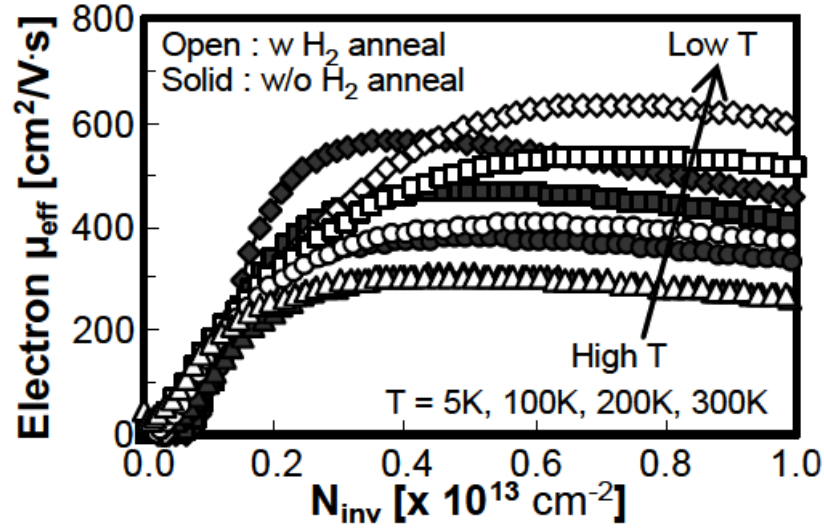


Fig. 2-3. Effective electron mobility as a function of inversion charge density for 1-level-SNWTs with and without H_2 annealing for different temperatures [2-9].

2.2.4 Tensile strained-SOI (sSOI) devices for NMOS

To introduce large tensile strain in the Si channel, a method using $\text{Si}_{1-x}\text{Ge}_x$ strained-relaxed buffer (SRB) layer has been widely applied in [2-11~2-20]. A schematic of strained Si/SiGe SRB/Si substrate or BOX is illustrated in Fig.2-4a [2-21]. Crystalline Si and crystalline Ge have the same lattice structure (diamond structure), but the size of Ge atoms is larger and the lattice constant is 4.2% greater ($5.66\text{\AA}$) than crystalline Si ($5.43\text{\AA}$). SiGe alloys thus have a lattice constant between those of Si and Ge, and the value can be tuned selectively by adjusting the ratio of Ge content. When a thin Si layer is epitaxially grown on a relaxed SiGe layer, the Si atoms attempt to perfectly align with the SiGe lattice without crystalline defects (Fig.2-5 [2-12]). The lattice constant difference between Si and Ge is too large, and Si epitaxy on Ge is imperfect in practice. As a consequence of parallel stretch of the thin Si layer, tensile strained-Si (sSi) layer can be fabricated on the SiGe virtual substrate. Today, tensile strained SOI (sSOI) without the SiGe SRB layer is being explored in order to achieve the combination of enhanced performances by FD-SOI and tensile sSi [2-22~2-25]. It is also known as another name, strained Si directly on insulator (SSDOI).

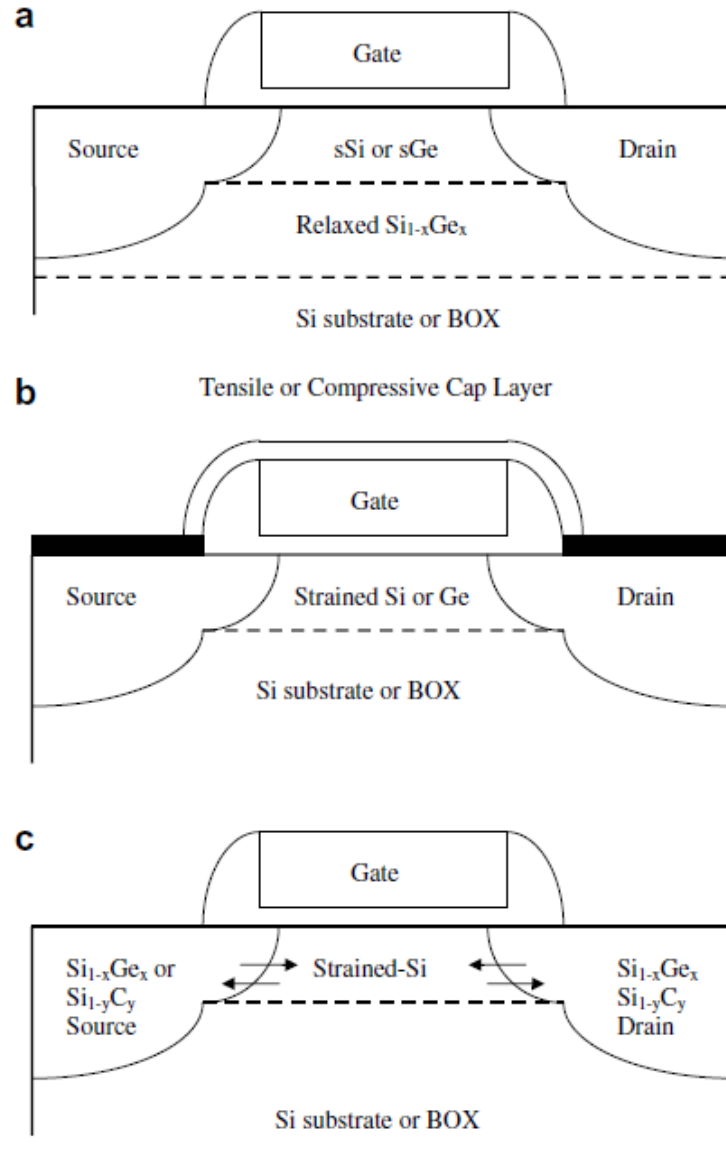


Fig. 2-4. Schematic representation of the different strain-engineering approaches: (a) global strain, using a tensile strained (sSi) ($x < 0.5$) or compressively strained-Ge (sGe) ($x > 0.5$) fabricated on a silicon or SOI substrate. The sSi or sGe layer may be directly on the BOX; (b) local tensile or compressive stress induced by a SiN cap layer in the Si, Ge or $\text{Si}_{1-x}\text{Ge}_x$ channel; (c) local tensile or compressive strain induced by embedded $\text{Si}_{1-y}\text{C}_y$ or $\text{Si}_{1-x}\text{Ge}_x$ source/drain regions [2-21].

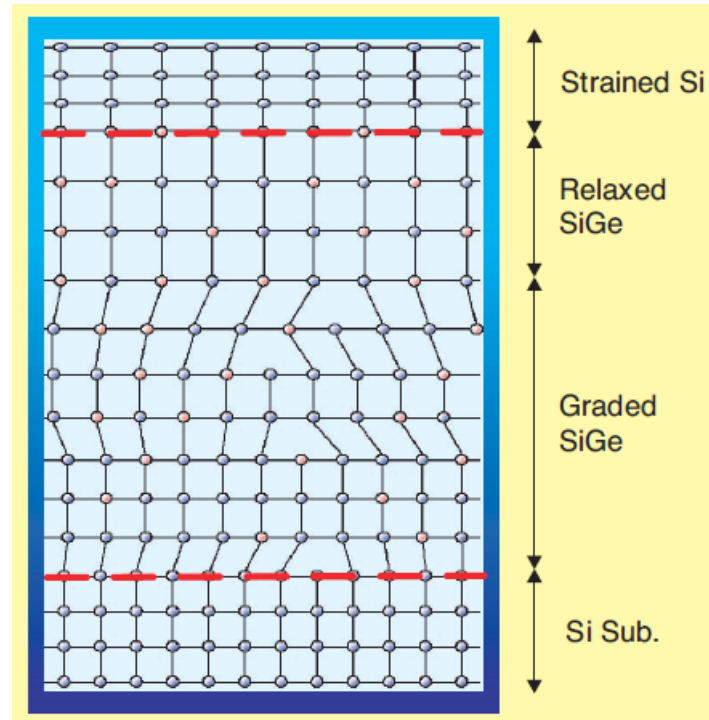


Fig. 2-5. The lattice arrangement of strained Si layer on the virtual $\text{Si}_{1-x}\text{Ge}_x$ substrate structures with increasing the Ge concentration in steps or linearly [2-12].

Our sSOI substrate is based on a standard Smart CutTM technology (cf. Fig.1-13). This can thus be realized with transfer of a strained Si film grown on donor wafer onto handle wafer, and can maintain the strain integrity. Figure 2-6 shows the process flow of sSOI wafer fabrication [2-25]. Oxidation of handle wafer is adjusted as targeted BOX layer thickness. On the other hand, sSi layer is successively created by using SiGe SRB and sSi epitaxy steps in donor wafer. Ge content and relaxation rate of the SiGe allows to tune the stress value in the sSi wafer. The steps, ion implantation, cleaning, bonding, and splitting, are all based on Smart CutTM technology (cf. Section 1.2.2.1, “FD-SOI devices”). The sSOI fabrication process is finished with removal of the SiGe layer by selective etching.

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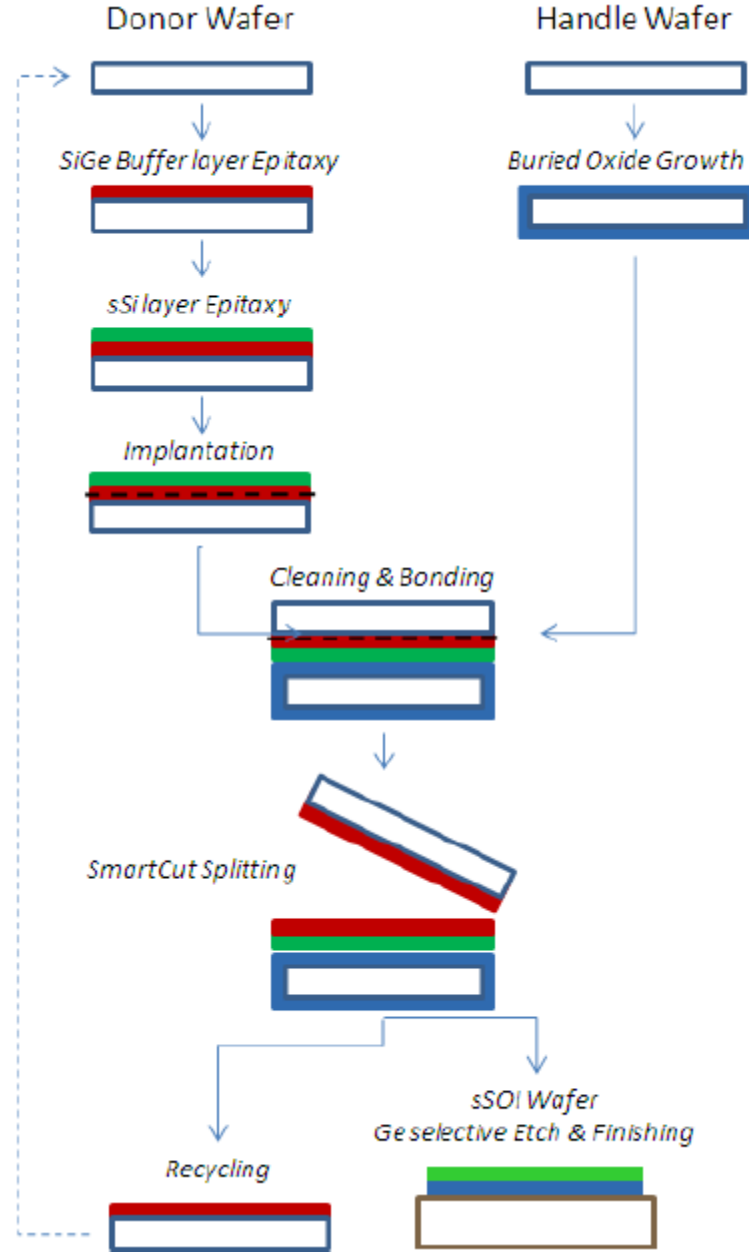


Fig. 2-6. Process schematics of sSOI substrate preparation [2-25].

In sSOI substrate used in this work, a biaxial tensile stress $\sigma_{\text{stress}} \approx 1.4 \text{ GPa}$ has been initially introduced, corresponding to a virtual substrate with 20% Ge. NWs processed on the sSOI wafer have finally a uniaxial tensile strain along the channel direction due to lateral strain relaxation [2-2,2-4,2-5], as illustrated in Fig.2-7.

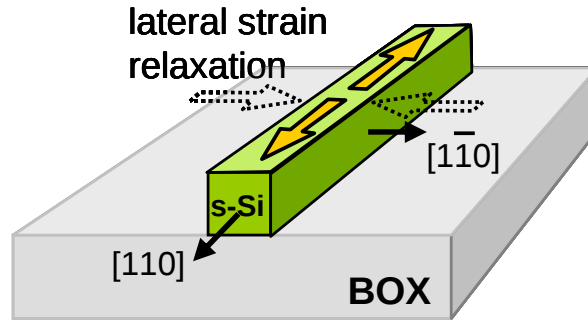


Fig. 2-7. Schematic of lateral strain relaxation occurred in sSOI TGNW structure.

2.2.5 Compressively strained SiGe-on-insulator (SGOI) for PMOS

Compressively strained SiGe layer sitting directly on BOX, *i.e.* SiGe-on-insulator (SGOI) [2-26~2-33], has been fabricated by Ge condensation technique [2-34,2-35]. The technique enables to achieve thin and fully strained SGOI substrate with low defect rate. Fabrication process of the compressively-strained SGOI starts from $\text{Si}_{1-x}\text{Ge}_x$ film epitaxy by CVD on blanket SOI wafer with 145nm BOX. Then, the SiGe layer is capped by 2nm Si. Next, a dry oxidation is carried out to diffuse Ge atoms towards the bottom of Si film in SOI wafer and consume the Si atoms. As a consequence, the total semiconductor thickness (Si+SiGe layers) decreases while the average Ge content increases when the oxidation duration is prolonged. The oxidation is finally stopped to obtain the enriched unitary $\text{Si}_{1-x}\text{Ge}_x$ layer with initial thickness and Ge concentration x or thinner film with more condensed Ge ratio (Fig.2-8). Our $\text{Si}_{1-x}\text{Ge}_x\text{OI}$ substrates have been fabricated with Ge content of 20% ($x=0.2$). Cross-sectional TEM image of the final $\text{SiO}_2/\text{SiGe}/\text{BOX}$ structure shown in Fig.2-9 exhibits a good crystalline lattice quality [2-33]. The initial biaxial stress in $\text{Si}_{0.8}\text{Ge}_{0.2}\text{OI}$ sample corresponds to $\sigma_{\text{stress}} \approx -1.2\text{GPa}$ and is laterally relaxed to a uniaxial compressive stress in NW structures.

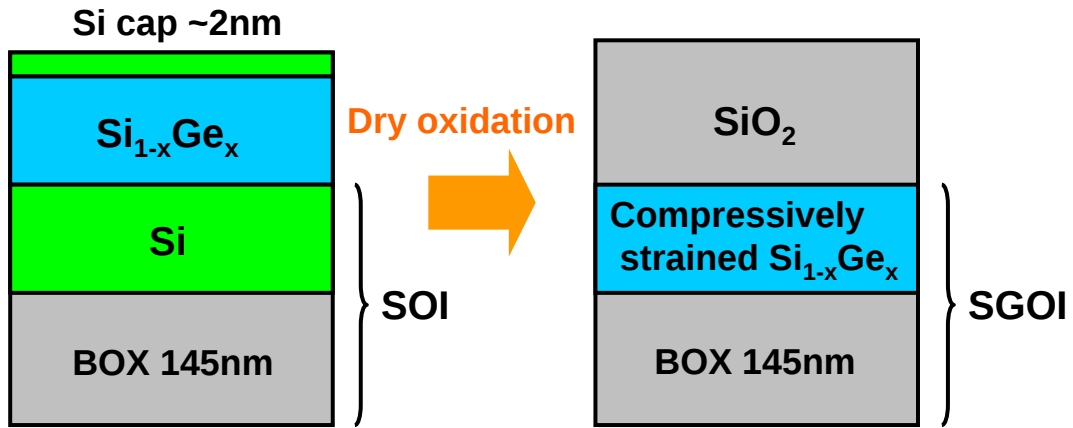


Fig. 2-8. Schematic of SGOI substrate preparation by Ge condensation technique. The initial pre-structure with SiGe on SOI finally becomes enriched and compressive strained SGOI by dry oxidation.

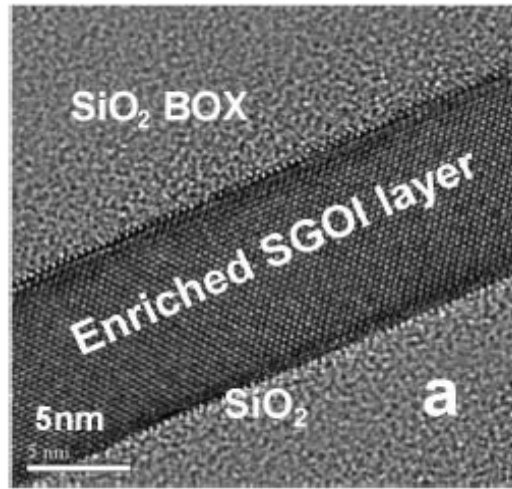


Fig. 2-9. Cross-sectional TEM picture of final SiO₂/SiGe/BOX structure after Ge condensation process [2-33].

It should be noticed that compressive strain in SiGe layer is the key feature providing large enhancement of hole mobility. In previous research by Tachi *et al.* in 2009, un-strained SiGe GAA NWs show much smaller hole mobility than the compressively strained counterparts, as shown in Fig.2-10 [2-8].

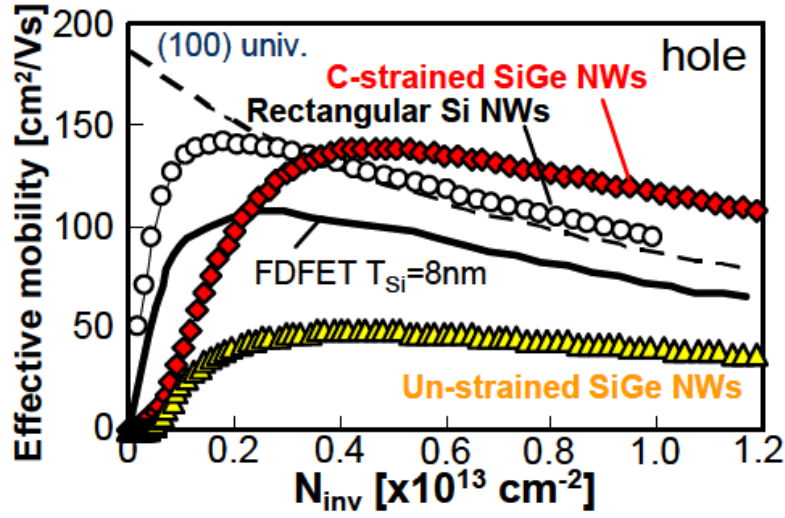


Fig. 2-10. Effective hole mobility of Si, strained and un-strained SiGe NWs. The W_{NW} of all NWs are $\sim 20\text{nm}$ [2-8].

2.2.6 Additional strain sources: SiGe source/drain and CESL

For some PMOS devices, a longitudinal uniaxial compressive strain by raised SiGe S/D and CESL formations was additionally introduced to the Si channel. Figure 2-4b and c sketches the use of CESL or embedded SiGe S/D resulting in a uniaxial strain in the channel [2-21].

The CESL consisting of SiN_x is deposited after the S/D formation and silicidation processes. The tensile and compressive CESL deposition is processed on NMOS and PMOS FETs, respectively, to effectively enhance the performance in short channel devices [2-36,2-37], even for MG FETs [2-38~2-40].

The use of $\text{Si}_{1-x}\text{Ge}_x$ S/D was firstly proposed for higher boron activation, the abrupt junction profile, and reduced external resistance [2-41]. Meanwhile SiGe S/D provides PMOS performance enhancement owing to significant uniaxial compression in the Si channel [2-42~2-46]. The SiGe S/D in our devices was formed by boron doped $\text{Si}_{1-x}\text{Ge}_x$ epitaxy resulting in $\text{Si}_{0.7}\text{Ge}_{0.3}$ with boron dopant. Figure 2-11 shows a TEM picture of the $\text{Si}_{0.8}\text{Ge}_{0.2}$ channel and raised $\text{Si}_{0.7}\text{Ge}_{0.3}$ S/D with perfect interface in Ω -gate NW FET [2-33].

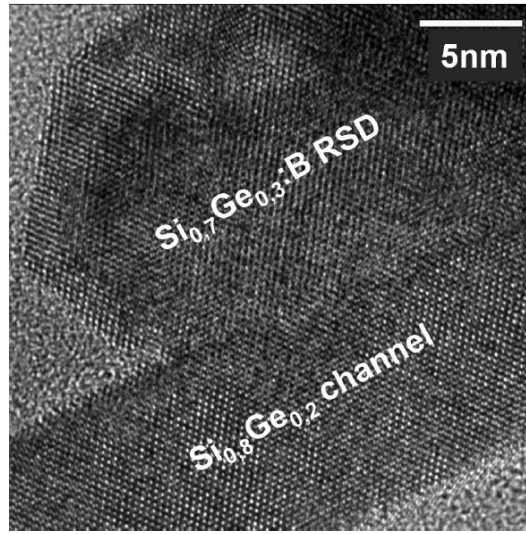
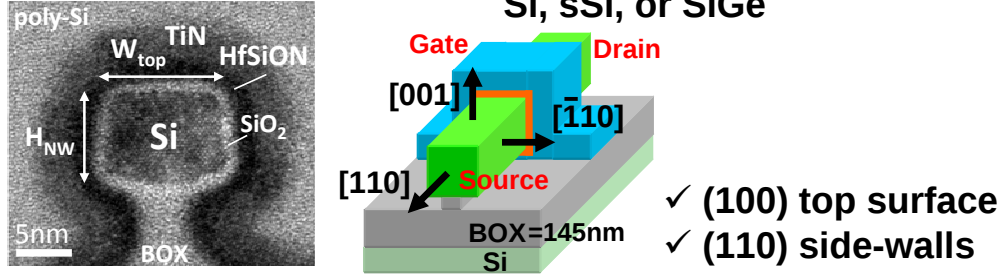


Fig. 2-11. Cross-sectional TEM image of a perfect interface between $\text{Si}_{0.8}\text{Ge}_{0.2}$ channel and raised $\text{Si}_{0.7}\text{Ge}_{0.3}$ S/D with doped B in Ω -gate NW FET [2-33].

2.3 Descriptions of all the device parameters

MOSFETs with various structural and technological parameters were fabricated based on FD-SOI technology. Schematic and cross-sectional TEM image of [110]- and [100]-oriented NW MOSFETs are shown in Fig.2-12. Device characterizations were performed on basic carrier transport properties (I_d - V_g , effective mobility, low-field mobility) (cf. Chapter 4) and low-frequency noise measurements (cf. Chapter 5).

✓ [110]-oriented Ω -gate nanowire



✓ [100]-oriented Ω -gate nanowire

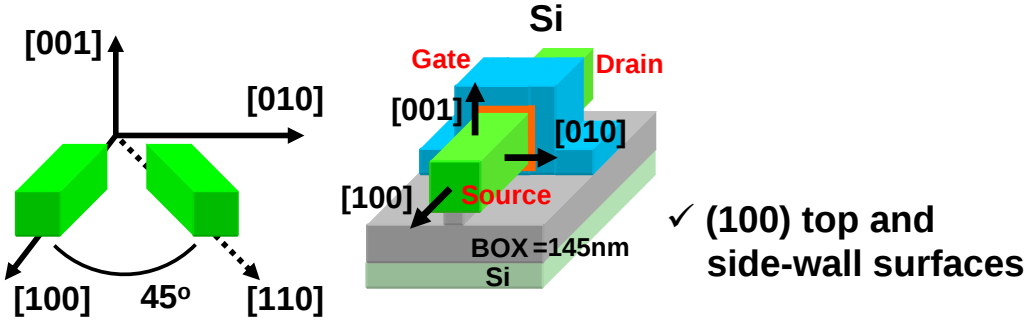


Fig. 2-12. Schematic and cross-sectional TEM image of Ω -gate NW MOSFETs.

NMOS FETs with 4-types of technological device parameters have been studied in this thesis: reference SOI with [110]-oriented channel, [110]-channel SOI with additional H_2 anneal process, SOI with [100]-oriented channel, and tensile strained SOI (sSOI) with [110]-channel. The different splits are summarized in Table 2-1 with architectural parameters, H_{NW} and W_{top} .

On the other hand, 6-types of PMOS FETs have been investigated: reference SOI, SOI with additional H_2 anneal process (SOI- H_2 A), SOI with raised $Si_{0.7}Ge_{0.3}$ -S/D (SG-S/D), SOI with SiGe-S/D and additional compressive CESL (cSG-S/D), compressively strained $Si_{0.8}Ge_{0.2}$ OI (SGOI), and SGOI with compressive CESL (cSGOI). All PMOS FETs have been processed with [110]-oriented channel. Each of the devices was briefly named (noted in brackets), and these are summarized in Table 2-2.

Other multiple-channel tri-gate and Ω -gate NWs, fabricated with a previous process mask, were also used for the purpose of our effective mobility study (cf. Section 4.2).

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Table 2-1. Summary of all our technological and architectural parameters for NMOS.

Ω -gate NW NMOS FETs	Undoped channel		H_2 anneal	NW height H_{NW}	Narrowest NW top width W_{top}
	Material	Direction			
SOI	Si	[110]	No	11nm	13nm
SOI with H_2 anneal	Si	[110]	Yes	10nm	11nm
[100]-oriented SOI	Si	[100]	No	10nm	10nm
Strained-SOI (sSOI)	sSi	[110]	No	11nm	11nm

Table 2-2. Summary of all our technological and architectural parameters for PMOS.

[110]-oriented Ω -gate NW PMOS FETs	Undoped channel	Raised S/D with B dope	C- CESL	H_2 anneal	NW height H_{NW}	Narrowest NW top width W_{top}
SOI	Si	Si	No	No	13.5nm	17nm
SOI- H_2A	Si	Si	No	Yes	12nm	11nm
SG-S/D	Si	$Si_{0.7}Ge_{0.3}$	No	No	9.5nm	14nm
cSG-S/D	Si	$Si_{0.7}Ge_{0.3}$	Yes	No	13.5nm	17nm
SGOI	$Si_{0.8}Ge_{0.2}$	$Si_{0.7}Ge_{0.3}$	No	No	11.5nm	13nm
cSGOI	$Si_{0.8}Ge_{0.2}$	$Si_{0.7}Ge_{0.3}$	Yes	No	11.5nm	13nm

2.4 References

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Chapter 3

Measurement methods

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3.1 I_d - V_g measurement

Gate voltage V_g dependent drain current I_d characteristics (I_d - V_g) were measured by a parameter analyzer Agilent B1500A for all the technological and architectural device parameters. This is the most common measurement to characterize FET performance [3-1,3-2]. DC V_g is applied from negative to positive bias conditions for NMOS (contrary, positive to negative for PMOS) to evaluate the off-state and on-state properties by monitoring the drain current I_d . Figure 3-1 shows one of the results for the narrowest single-channel NW N- and PMOS FETs with $L_g \approx 110\text{nm}$ in linear ($|V_d|=40\text{mV}$) and saturation ($|V_d|=0.9\text{V}$) regimes of V_d bias conditions.

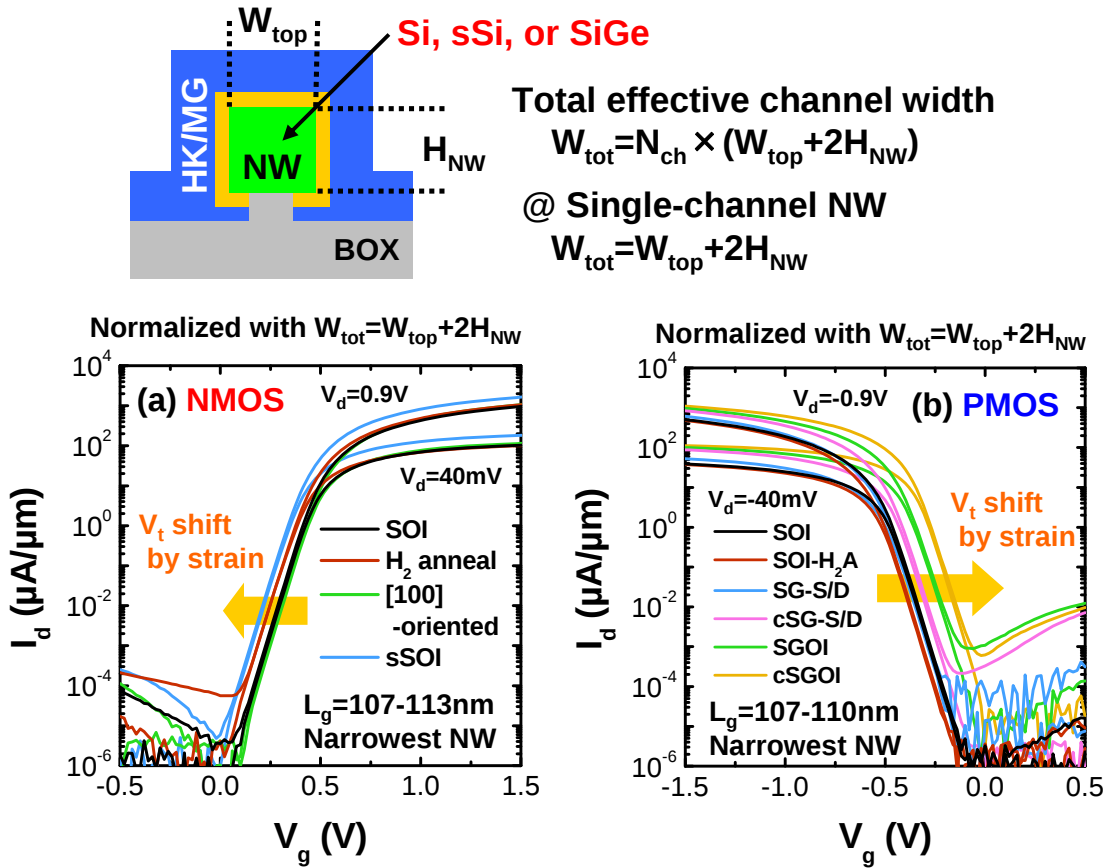


Fig. 3-1. I_d - V_g characteristics of the narrowest NW FETs with $L_g \approx 110\text{nm}$ for all the technological parameters in (a) NMOS and (b) PMOS devices.

3.2 C_{gc} - V_g measurement

Gate voltage V_g dependent gate-to-channel capacitance C_{gc} characteristics (C_{gc} - V_g) were measured by a precision LCR (inductance-capacitance-resistance) meter Agilent E4980A. A small AC signal is superimposed to the DC voltage V_g , consequently the capacitance, which is the charge change ΔQ responding to the AC voltage, is measured from AC current signal through S/D. The measurement results in the widest FET and the narrowest 50-channel NW with long $L_g=10\mu m$ is shown in Fig.3-2. The normalized curves by channel area ($W_{tot} \times L_g$) are identical between the widest FET and NW. This means that the equivalent oxide thickness (EOT) and gate oxide capacitance C_{ox} , defined here as a saturated C_{gc} value at strong inversion region, are sustained from the widest FETs down to the narrowest NW FETs. Here C_{ox} is constantly acquired as $C_{ox} \approx 2 \times 10^{-6} F/cm^2$ for both N- and PMOS devices.

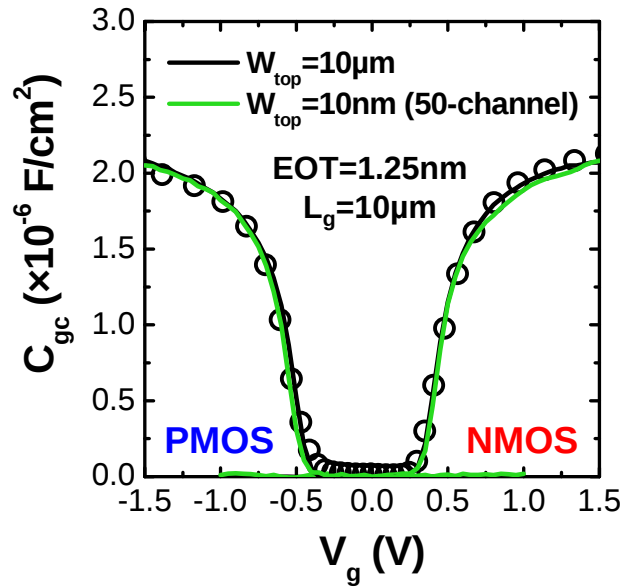


Fig. 3-2. C_{gc} - V_g characteristics of the widest FET and narrowest multiple 50-channel NW with $L_g=10\mu m$ in both SOI N- and PMOS devices. Sustained EOT value of 1.25nm for both wide and NW FETs was extracted by fitting between (lines) measured C_{gc} data and (circles) the simulated curve.

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3.3 Mobility extraction

3.3.1 Effective mobility

Carrier mobility in MOSFET operation is a very important parameter, involved in the I_d definitions (cf. Eqs. (2-2) and (2-4)). Several techniques are available for the mobility extraction [3-3,3-4]. One of the techniques, split C-V technique proposed by J. Koomen [3-5] has been widely applied [3-6~3-8]. The technique needs enough large device channel area to allow accurate C_{gc} - V_g measurement. The split C-V extracts the carrier effective mobility μ_{eff} as a function of the effective field E_{eff} or the inversion carrier density N_{inv} . The μ_{eff} in linear region is obtained as:

$$\mu_{eff} = \frac{L}{W} \cdot \frac{I_d}{Q_{inv} V_d} \quad (3-1)$$

where Q_{inv} is the inversion charge density. The Q_{inv} at a given V_g is obtained by integrating the C_{gc} to the given V_g , and the relationship is written as:

$$Q_{inv} = \int_{-\infty}^{V_g} C_{gc} dV \quad (3-2)$$

For bulk FET case, the depletion charge density Q_{dep} is also necessary, and evaluated from the gate-to-body capacitance C_{gb} measurement. The Q_{dep} is similarly extracted as Q_{inv} by integrating from flat-band voltage V_{fb} to given V_g , and the equation is shown as:

$$Q_{dep} = \int_{V_{fb}}^{V_g} C_{gb} dV \quad (3-3)$$

For SOI substrates, the C_{gb} measurement cannot be carried out because of the BOX. However, the Q_{dep} is negligible compared with the Q_{inv} in FD-SOI FETs with undoped ultra-thin channel and thick BOX. Therefore, the E_{eff} in our SOI FETs is expressed as:

$$E_{eff} = \frac{\eta Q_{inv} + Q_{dep}}{\epsilon_{Si}} \approx \frac{\eta}{\epsilon_{Si}} Q_{inv} \quad (3-4)$$

where η is an empirical parameter corresponding to 1/2 for electrons and to 1/3 for holes. The carrier density N_{inv} is simply calculated as:

$$N_{inv} = \frac{Q_{inv}}{q} = \frac{1}{q} \int_{-\infty}^{V_g} C_{gc} dV \quad (3-5)$$

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The carrier density in the channel under strong inversion condition N_{inv} is often approximated by:

$$N_{inv} = \frac{Q_{inv}}{q} \approx \frac{C_{ox}}{q} (V_g - V_t - mV_{ch}) \quad (3-6)$$

where V_{ch} is the potential along the channel. In general, the equation can be further simplified as:

$$N_{inv} \approx \frac{C_{ox}}{q} (V_g - V_t) = \frac{C_{ox} V_{gt}}{q} \quad (3-7)$$

A well known schematic showing the three dominant scattering mechanisms which limit carrier mobility of MOSFET is shown in Fig.3-3. Mobility limited by phonon scattering μ_P depends on temperature more keenly than others. Phonon scattering influence disappears at low temperature, and below 77K, the mobility is only limited by Coulomb scattering at low N_{inv} regime (μ_C) and surface roughness scattering at higher N_{inv} region (μ_{SR}) [3-9,3-10]. Figure 3-3 shows the mobility extracted on 10 μ m-wide FET as an illustration of the three scattering mechanisms.

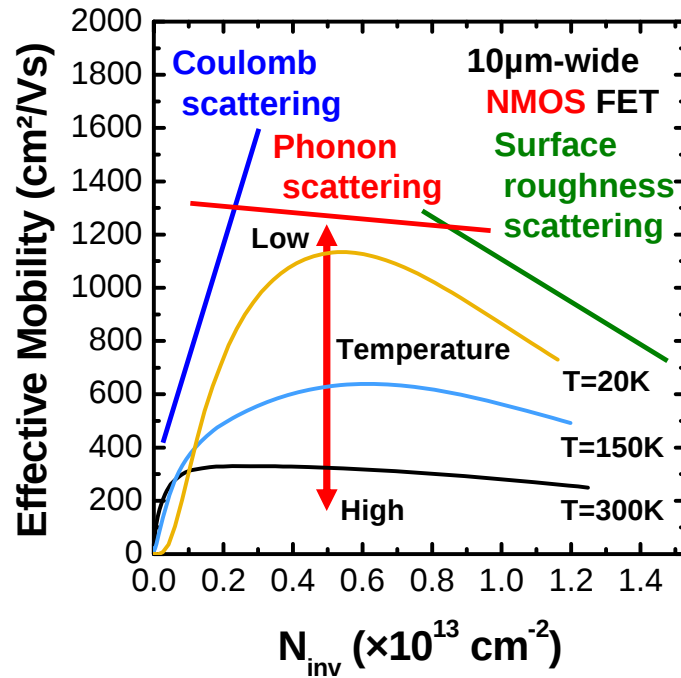


Fig. 3-3. Schematic exhibiting the three dominant scattering mechanisms which limit carrier mobility of MOSFET, and the temperature dependent mobility behavior from 300K down to 20K on 10 μ m-wide NMOS FET.

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3.3.2 Low-field mobility

Extraction and evaluation of the low-field mobility μ_0 based on Y-function method [3-4,3-11~3-13] is very effective for ultra-scaled FETs, as effective mobility μ_{eff} investigation needs enough large size of the channel area. The μ_0 is extracted as the mobility at low electric field region, in other words, low inversion carrier density region ($N_{inv} \approx 0$), without consideration of Coulomb scattering influence. With this assumption, the relationship between low-field mobility μ_0 and effective mobility μ_{eff} is expressed as:

$$\mu_{eff} = \frac{\mu_0}{1 + \theta_1(V_g - V_t) + \theta_2(V_g - V_t)^2} = \frac{\mu_0}{1 + \theta_1 V_{gt} + \theta_2 V_{gt}^2} \quad (3-8a)$$

$$\text{with } \theta_1 = \theta_{1,0} + R_{SD}\beta_0 \quad (3-8b)$$

where θ_1 ($\theta_{1,0}$) and θ_2 , are the first and second order mobility attenuation factors, respectively, R_{SD} is the series resistance of source and drain contacts, and β_0 is the transistor gain. The attenuation factors express mobility degradation at strong inversion region, and θ_1 includes mainly phonon scattering impacts, while θ_2 correspond roughly to surface roughness scattering influence. However, Eq. (3-8a) gives only an empirical expression of μ_{eff} , so that θ_1 and θ_2 have no physical meaning [3-13]. In linear region ($V_d \ll V_{d,sat}$), μ_0 can be deduced from the transistor gain β_0 as:

$$\mu_0 = \mu_{eff}(N_{inv} \approx 0) = \frac{\beta_0 L}{C_{ox} W} \quad (3-9)$$

The parameter β_0 is extracted from the slope of the Y-function vs. V_{gt} curve, and the Y-function is given by:

$$Y = \frac{I_d}{\sqrt{g_m}} = V_{gt} \sqrt{\frac{\beta_0 V_{d_lin}}{1 - \theta_2 V_{gt}^2}} \quad (3-10)$$

where g_m is the transconductance and is defined as dI_d/dV_g . This equation can be simplified for $\theta_2 V_{gt}^2 \ll 1$ as:

$$Y = \frac{I_d}{\sqrt{g_m}} \approx V_{gt} \sqrt{\beta_0 V_{d_lin}} \quad (3-11)$$

The method allows to extract V_t , θ_1 , θ_2 , and β_0 after several fitting procedures.

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Figure 3-4 shows illustration of the relationships among experimental μ_{eff} , and computed μ_0 and μ_Y in the widest FET and narrowest 50-channel NWs with $L_g=10\mu\text{m}$. The $\mu_{\text{eff}}-N_{\text{inv}}$ curves can be completely reconstructed by the Y-function method using Eq. (3-8a) by adding Coulomb scattering limitation in small N_{inv} range. Note that μ_0 extracted by this method is free from R_{SD} effect, which limits the I_d especially for short channel device.

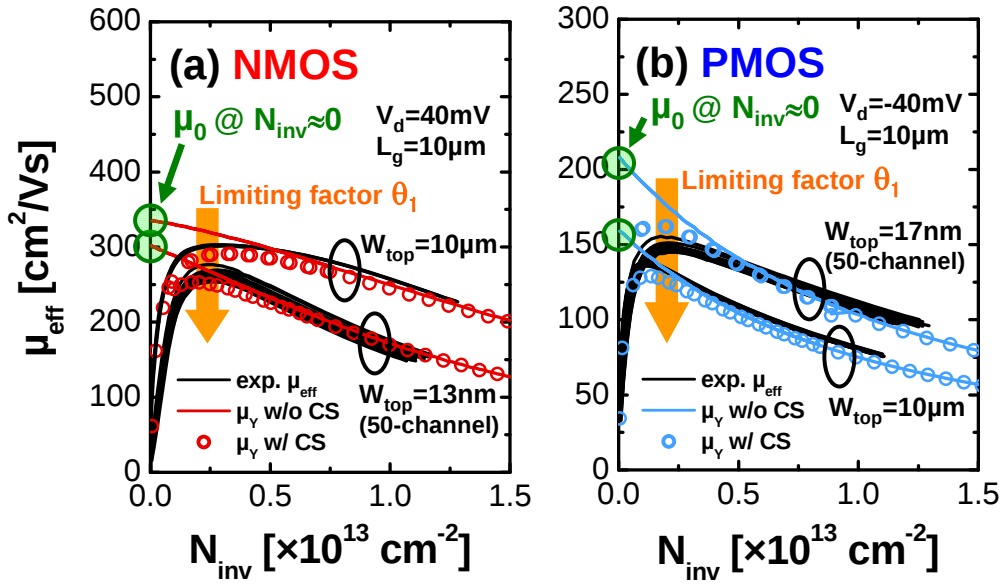


Fig. 3-4. Illustration of the relationship between μ_{eff} and μ_0 on (a) NMOS and (b) PMOS cases. The computed μ_Y curves considering Coulomb scattering (CS) influence show good agreement with experimental μ_{eff} data measured by split C-V in the narrowest 50-channel NW and the widest FETs with $L_g=10\mu\text{m}$.

3.4 Low-frequency noise measurement

LFN measurements were performed at room temperature under a probe level using a semi-automatic noise measurement system by Synergie Concept [3-14]. The system is well configured for delicate measurements. The system is called Programmable Point Probe Noise Measuring System (3PNMS), and was operated by control software

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NOISYS (version 4.1) with programmable biasing amplifier (PBA2). Figure 3-5 shows a schematic of the LFN measurement system with device under test (DUT) and PBA2. The PBA2 is composed of batteries without AC signals and low-noise amplifiers. Input V_d , V_g , and the measuring steps are finely programmable, and DC and AC components of output I_d are monitored.

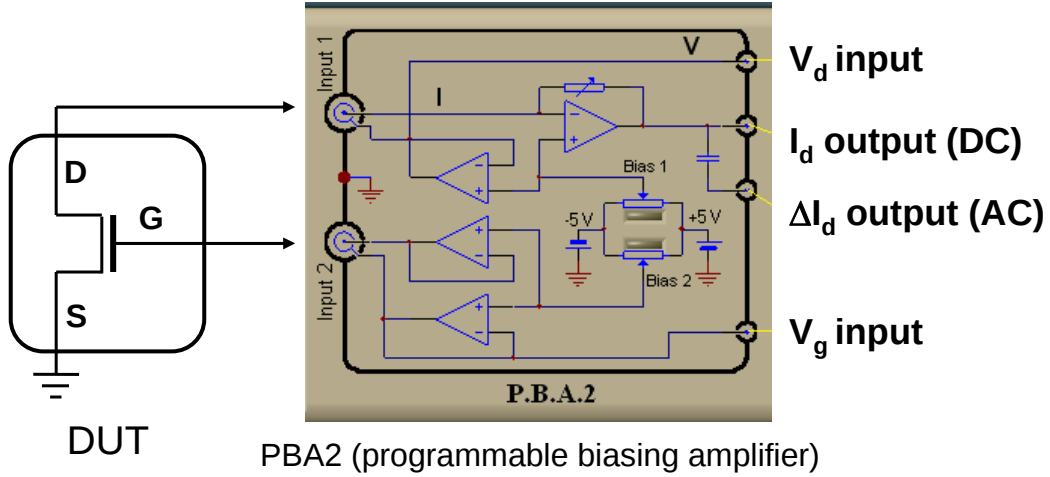


Fig. 3-5. Schematic of the LFN measurement system 3PNMS with PBA2 and DUT.

The noise signal is computed by converting the output AC component (ΔI_d) in time domain into the PSD in frequency domain with fast Fourier transform (FFT). For the accurate measurement of noise characteristic in MOSFETs, the system was shielded by a metal box enclosure and isolated from extrinsic noise sources. In addition, each component of the system was appropriately grounded to prevent an unexpected electric shock from affecting the measurement. The system noise floor of 3PNMS was measured around $\sim 2 \times 10^{-27} \text{ A}^2/\text{Hz}$. It accomplishes the recommended noise floor level below $10^{-26} \text{ A}^2/\text{Hz}$.

In this work, the PSD of drain current noise S_{I_d} was acquired at 400 sample points of frequency, and with 32 times averaging. The V_g was varied from subthreshold region (actually with the current lower limit of $|I_d| > 10^{-9} \text{ A}$) up to strong inversion region ($|V_g| > 1.0 \text{ V}$). The V_d bias were varied from linear region ($|V_d| = 40 \text{ mV}$) up to saturation region ($|V_d| = 0.9 \text{ V}$).

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Chapter 4

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4.1 I_d - V_g characteristics

I_d - V_g characteristics in the narrowest single-channel NW FETs with varied gate length L_g from $1\mu\text{m}$ down to 17nm are discussed for all the technological parameters. The curves in reference SOI and strained devices (sSOI for NMOS, and SGOI for PMOS) are shown in [Fig.4-1](#) for NMOS NW, and in [Fig.4-2](#) for PMOS NW FETs, respectively. The curves are parallel and vertically shifted as the L_g is shortened in both linear and saturation regions, and also for both unstrained and strained FETs. In the following, we discuss the main electrical parameters for all the narrowest NW devices; threshold voltage V_t , drain induced barrier lowering (DIBL), subthreshold swing (SS), and on-state drain current I_{ON} .

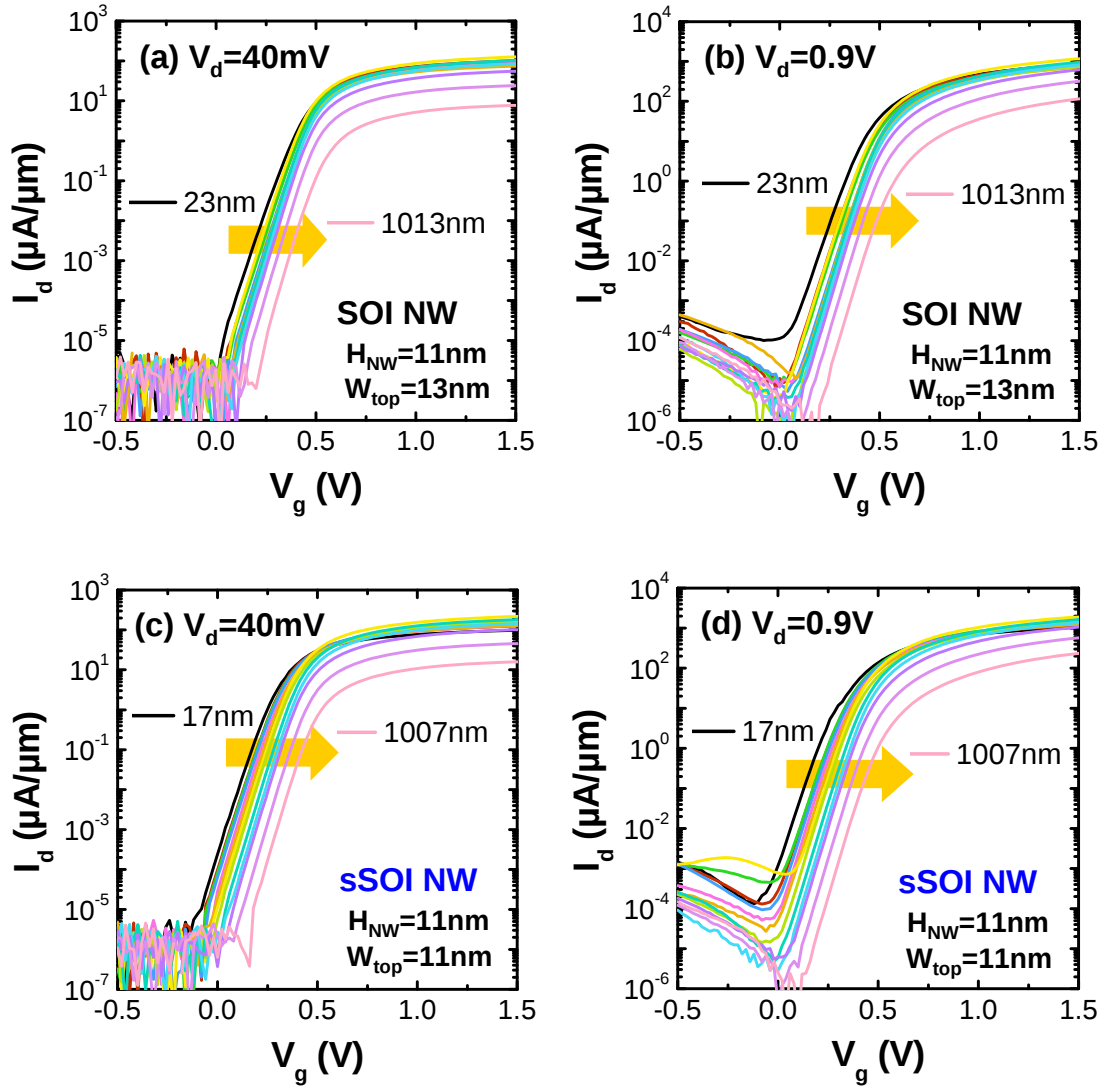


Fig. 4-1. I_d - V_g characteristics as a function of L_g in the narrowest NWs for (a,b) SOI and (c,d) sSOI NMOS devices with comparison between (a,c) linear ($V_d=40\text{mV}$) and (b,d) saturation ($V_d=0.9\text{V}$) regions.

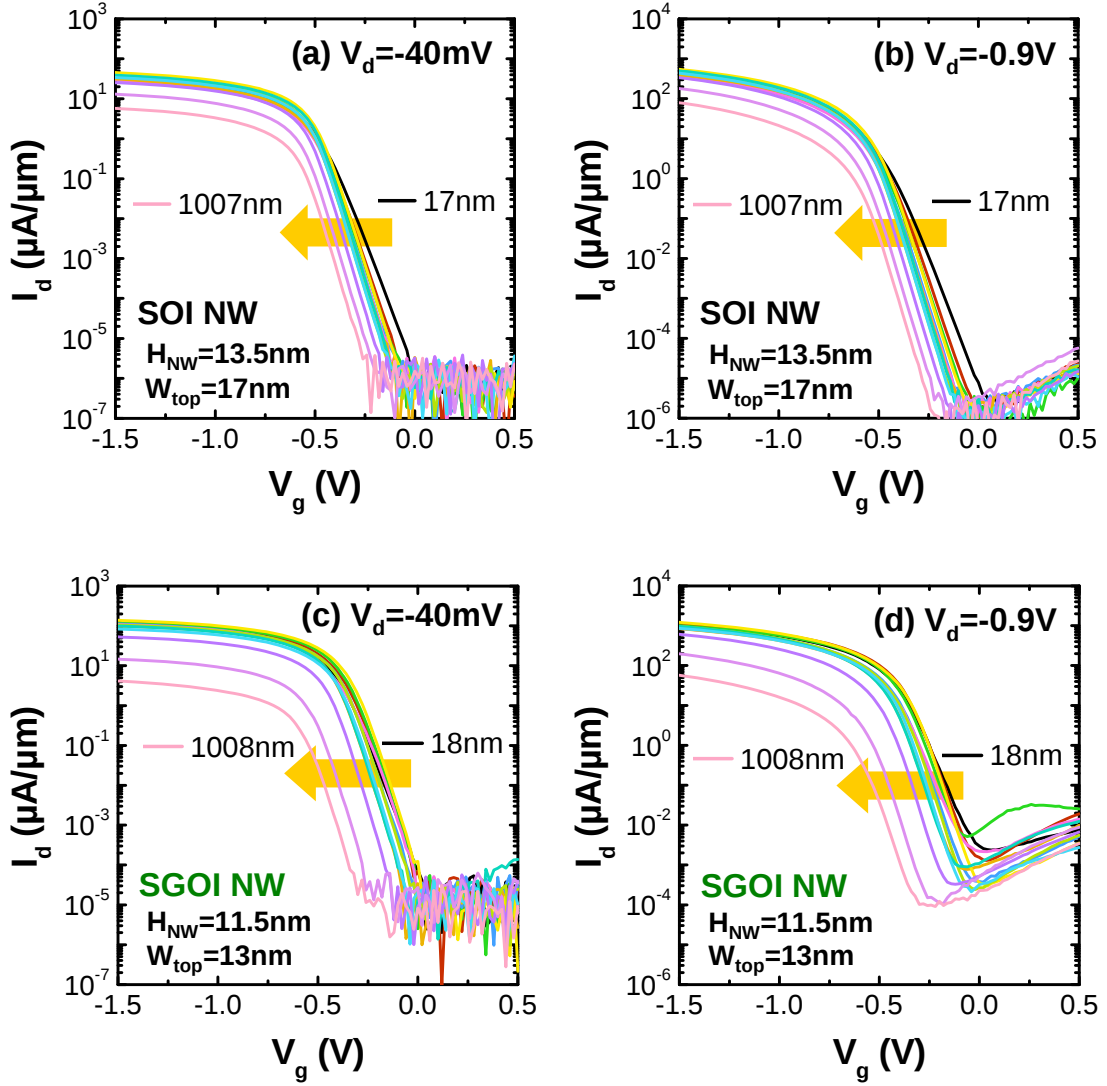


Fig. 4-2. I_d - V_g characteristics as a function of L_g in the narrowest NWs for (a,b) SOI and (c,d) SGOI PMOS devices with comparison between (a,c) linear ($V_d=-40\text{mV}$) and (b,d) saturation ($V_d=-0.9\text{V}$) regions.

4.1.1 Threshold voltage

Threshold voltage V_t is extracted by constant-current method, and the arbitrary constant I_d is defined as $(W_{\text{tot}}/L_g) \times 10^{-7}$ [4-1,4-2]. The V_t extracted at linear ($|V_d|=40\text{mV}$) and saturation ($|V_d|=0.9\text{V}$) regions in the widest ($W_{\text{top}}=10\mu\text{m}$) and the narrowest NW FETs for reference SOI N- and PMOS devices is shown in Fig.4-2. The V_t values are

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dependently shifted on the L_g by SCE [4-3], thus the absolute values ($|V_t|$) decrease for shorter L_g in both NMOS and PMOS devices [4-4~4-7]. It is noticed that SOI PMOS NWs with shorter $L_g < 50\text{nm}$ exhibit ascending of the $|V_t|$. The decreasing tendency of $|V_t|$ in NWs is much smaller than wide FET cases, and this means that NW devices have better endurance to detrimental SCE.

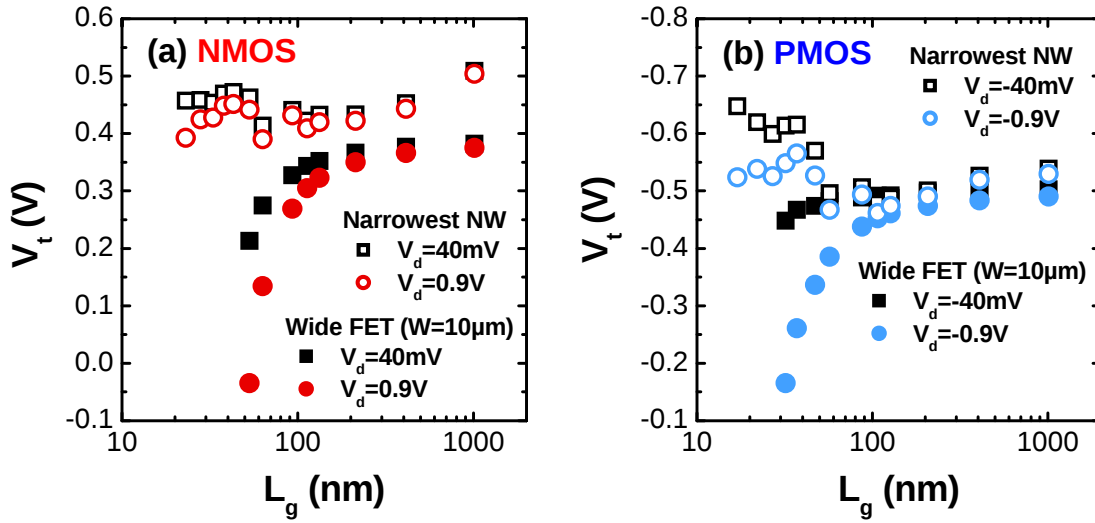


Fig. 4-3. Threshold voltage V_t as a function of L_g extracted at linear ($|V_d|=40\text{mV}$) and saturation ($|V_d|=0.9\text{V}$) regions in the widest and the narrowest NW FETs for SOI (a) NMOS and (b) PMOS devices.

The V_t values for all N- and PMOS NWs are shown in Figs.4-4 and 4-5, respectively. The decreasing tendency of $|V_t|$ is in agreement with all NWs (except shorter range with $L_g < 50\text{nm}$ in PMOS NWs). Moreover, the technological parameters sensitively alter the L_g dependent V_t behavior. For NMOS, [100]-oriented NWs show somewhat higher V_t values, in contrast H_2 annealed NWs exhibit lower V_t values than reference SOI devices. The V_t shifts could be attributed to the interface dipole alteration, which may depend on crystallographic surface orientation and cross-sectional shape of the NW body [4-5]. Strain effect also enlarges the L_g dependent V_t shift indicating the lower values than SOI NWs [4-8,4-9], and this result is in good agreement with tensile strain effect which introduces the significant band offset [4-10~4-12]. In PMOS, SOI- H_2A NW shows higher $|V_t|$ values and more drastic ascending of the $|V_t|$ behavior especially in shorter

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L_g region than reference SOI NW. This could be also ascribed to the surface dipole modulation. Similarly to NMOS, the compressive strain impact is appeared with the lower $|V_t|$ values in cSG-S/D [4-9], clearly in both n- and cSGOI devices [4-5~4-7].

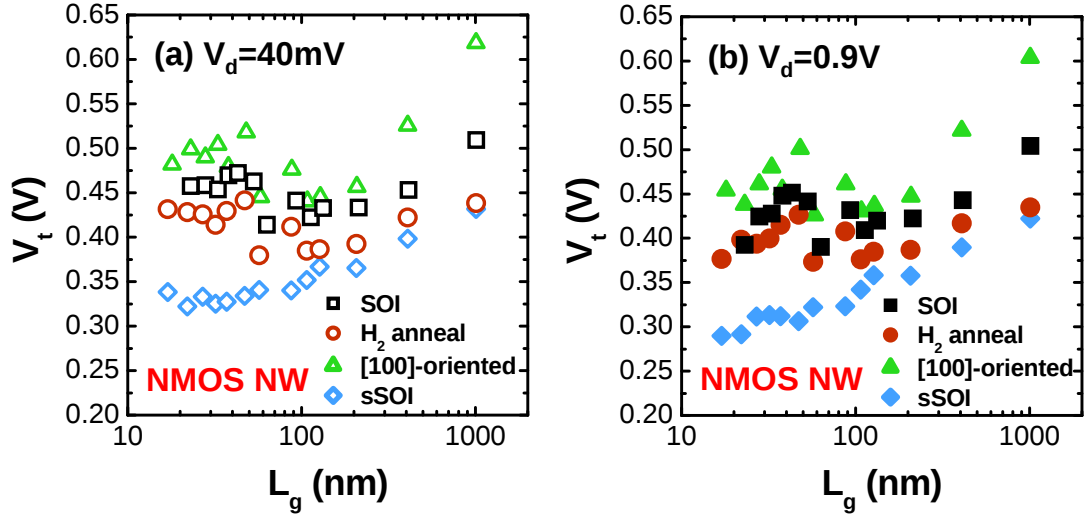


Fig. 4-4. Threshold voltage V_t as a function of L_g in the narrowest NMOS NWs at (a) linear ($V_d=40mV$) and (b) saturation ($V_d=0.9V$) regions for all the technological parameters.

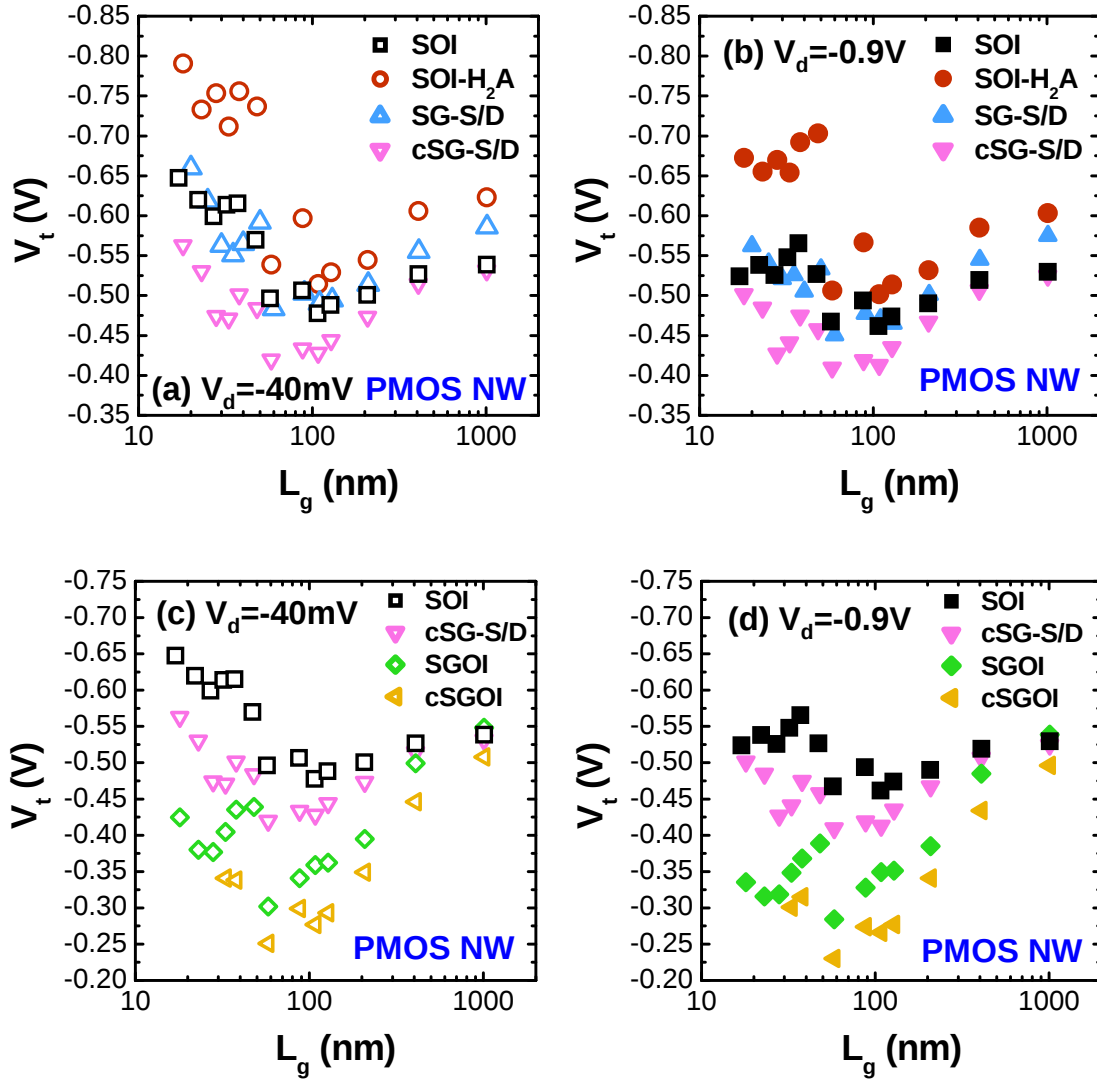


Fig. 4-5. Threshold voltage V_t as a function of L_g in the narrowest PMOS NWs at (a,c) linear ($V_d=-40\text{mV}$) and (b,d) saturation ($V_d=-0.9\text{V}$) regions for all the technological splits.

4.1.2 Drain induced barrier lowering

Drain induced barrier lowering (DIBL) causes the threshold voltage V_t decrease as the V_d bias is increased. The DIBL is defined by assigning the extracted V_t values in linear and saturation regimes (V_{t_lin} and V_{t_sat} in Figs.4-3~4-5) as [4-13]:

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$$DIBL = \frac{|V_{t_sat} - V_{t_lin}|}{|V_{d_sat} - V_{d_lin}|} = \frac{|V_{t_sat} - V_{t_lin}|}{0.86} \quad (4-1)$$

The DIBL in the widest and the narrowest NW FETs for reference SOI N- and PMOS devices is evaluated in Fig.4-6. The widest FETs exhibit a drastic increase of the DIBL values as the L_g is shortened below 100nm for both N- and PMOS devices, whereas the DIBL are similar with the values in NWs maintained below 30mV/V for the L_g range over 200nm. On the other hand, NWs sustain the much smaller values in entire L_g range, with a maximum DIBL=75.5mV/V at L_g =23nm for NMOS, and with 143.6mV/V at L_g =17nm for PMOS NWs. It is thus reconfirmed that NW devices have much better electrostatic control than planer devices.

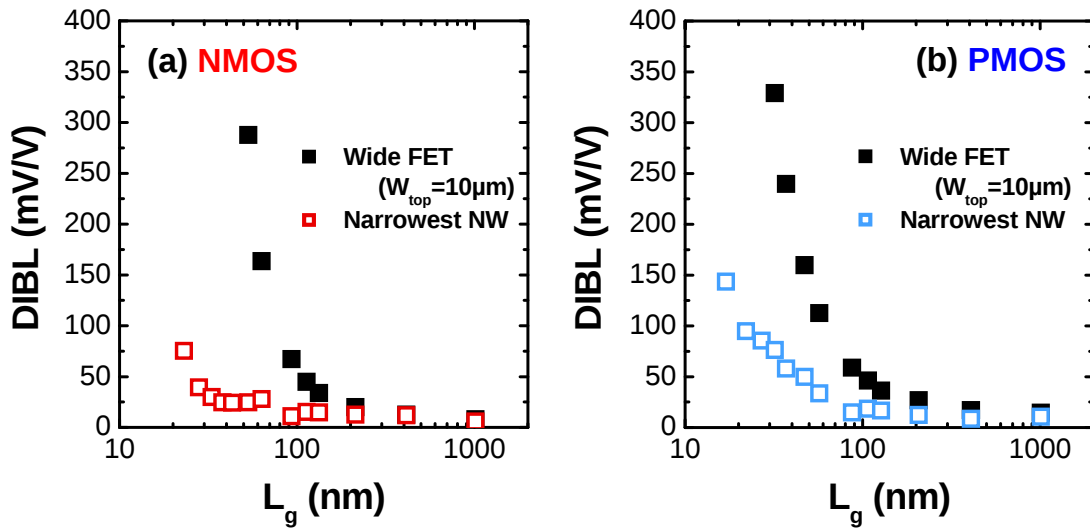


Fig. 4-6. Extracted DIBL as a function of L_g in the widest and the narrowest NW FETs for SOI (a) NMOS and (b) PMOS devices.

Figures 4-7 and 4-8 summarize the DIBL extracted in all N- and PMOS NW devices, respectively. In both NWs, the L_g dependent DIBL behavior draws roughly the same curves. In NMOS, it is observed that additional H_2 anneal process provides slightly better SCE immunity in whole L_g range [4-13]. For PMOS, cSG-S/D shows the best performance. It is found that electrostatic control against detrimental SCE is more effective in NMOS than PMOS NWs for short channel region. Moreover, the tensile and

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compressive strain technologies do not largely influence the DIBL behaviors. The extracted DIBL behaviors are comparable with our recent studies for NW MOSFETs [4-9,4-13,4-14].

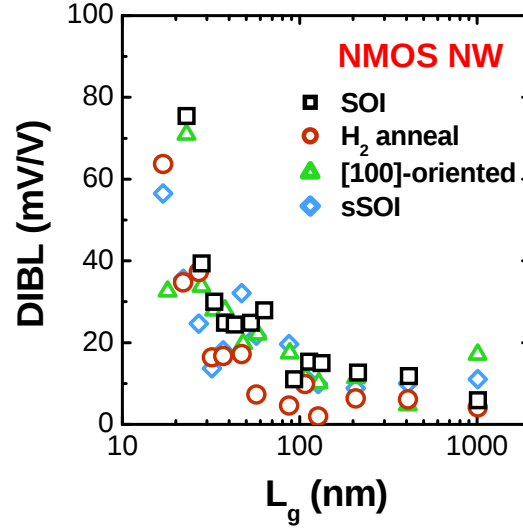


Fig. 4-7. Extracted DIBL as a function of L_g in the narrowest NMOS NWs for all the technological parameters.

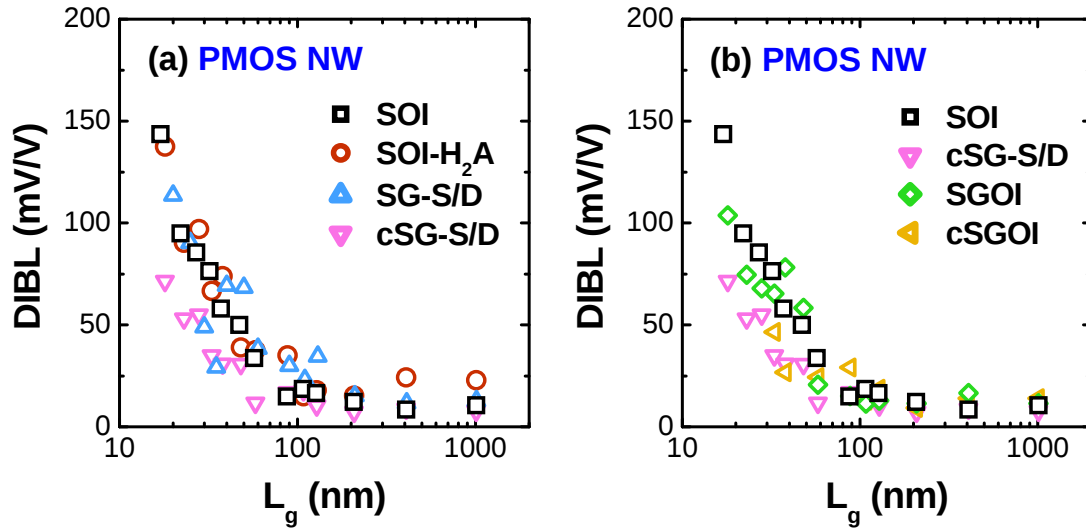


Fig. 4-8. Extracted DIBL as a function of L_g in the narrowest PMOS NWs for all the technological splits.

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4.1.3 Subthreshold swing

Extracted subthreshold swing (SS) in the widest and the narrowest NW FETs for reference SOI N- and PMOS devices is shown in Fig.4-9. Similarly with DIBL characterization, the SS in widest FETs drastically increase with decreasing of the L_g below 100nm for both N- and PMOS devices, while the almost ideal $SS \approx 60\text{mV/dec}$ is obtained for the L_g range above 200nm. In contrast, SOI NWs maintain the SS close to the ideal value in whole L_g range even for the shortest devices and at high $|V_d|$ condition. The worst $SS = 69.5\text{mV/dec}$ for NMOS NW with $L_g = 23\text{nm}$ and $SS = 76.7\text{mV/dec}$ for PMOS NW with $L_g = 17\text{nm}$ are extracted. The SOI NWs thus demonstrate the excellent electrostatic control.

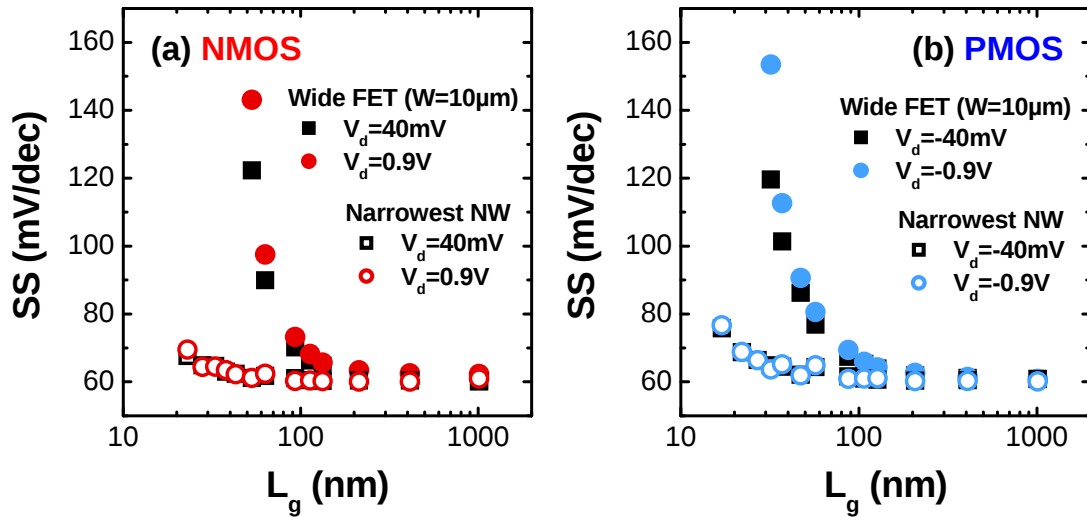


Fig. 4-9. Subthreshold swing SS as a function of L_g in the widest and the narrowest NW FETs for SOI (a) NMOS and (b) PMOS devices.

The SS observed in all NWs is shown in Figs.4-10 and 4-11 for N- and PMOS devices, respectively. For NMOS, the SS is close to the ideal value ($\approx 60\text{mV/dec}$) in longer region of $L_g > 80\text{nm}$, and the value increases below L_g of 70nm. This reflects SCE impact enlarging the body-effect. H_2 anneal processed NWs show the values above the universal value at low $V_d = 40\text{mV}$, even in the longer L_g range. However, the data dispersion roughly disappears at high V_d condition. Therefore, all NMOS NWs show

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the similar and excellent behavior the SS values sustaining below 69.5mV/V at high $V_d=0.9V$.

In PMOS devices, the L_g dependent SS behavior at low $V_d=-40mV$ is similar to NMOS case, but with the higher SS accession. Furthermore, the control is deteriorated at high $V_d=-0.9V$ compared to the low V_d case, unlike with NMOS devices. The SiGe strain technologies introduce degraded SS values of 82-85mV/dec compared to reference SOI NW with 76.7mV/dec at the minimum $L_g=17-20nm$ at high V_d regime. These conclude that PMOS NWs, especially SiGe processed devices, are more influenced by SCE than NMOS NWs. The SS behavior is better in NMOS and is comparable in PMOS NW FETs compared to our recent works on NW MOSFETs [4-9,4-13,4-14].

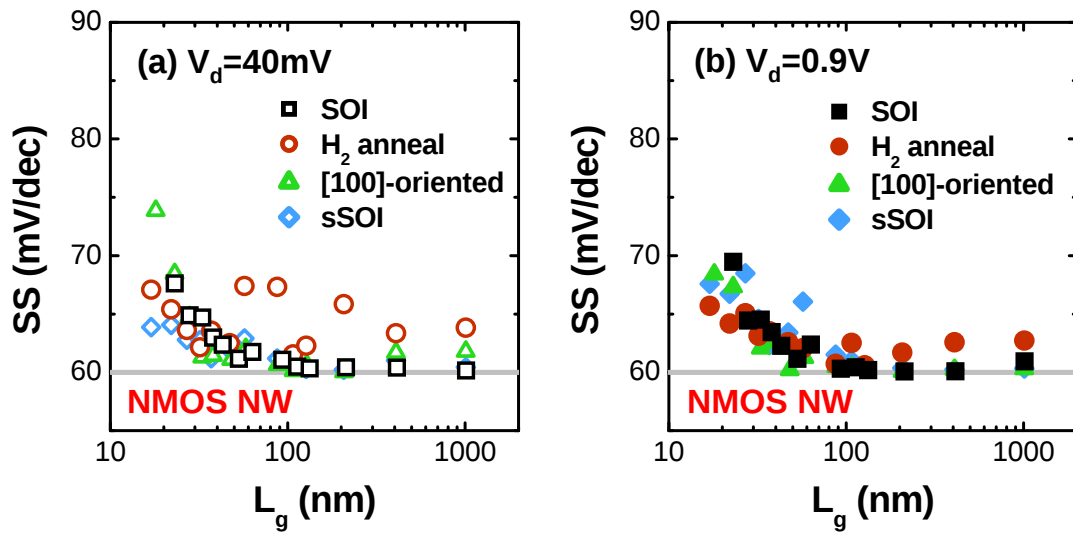


Fig. 4-10. Subthreshold swing SS as a function of L_g in the narrowest NMOS NWs at (a) low $V_d=40mV$ and (b) high $V_d=0.9V$ for all the technological parameters.

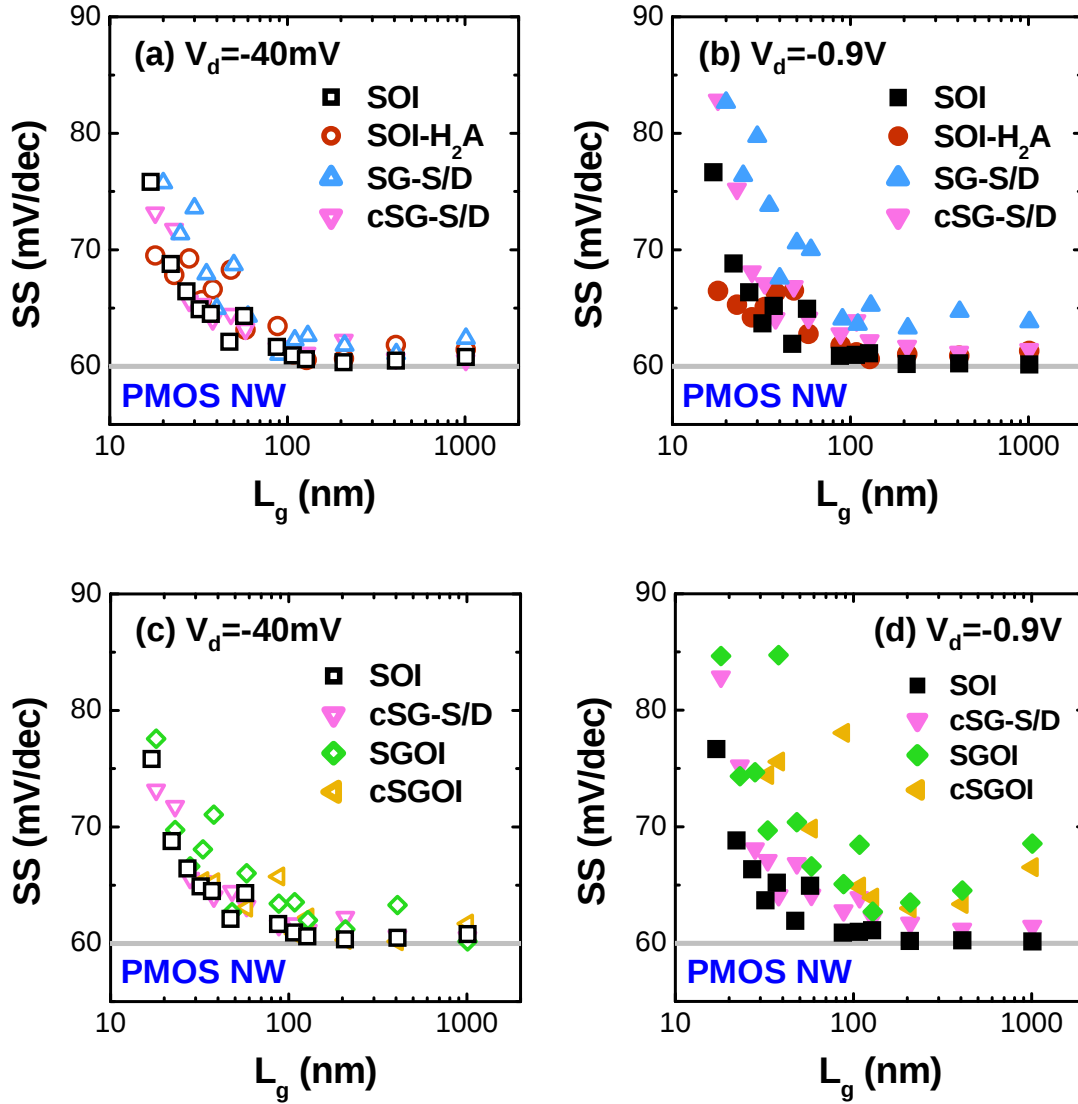


Fig. 4-11. Subthreshold swing SS as a function of L_g in the narrowest PMOS NWs at (a,c) low $V_d = -40\text{mV}$ and (b,d) high $V_d = -0.9\text{V}$ for all the technological splits.

4.1.4 Challenge of I_{ON} enhancement

On-state current I_{ON} in saturation region is here defined as I_d measured at $|V_g| = |V_d| = 0.9\text{V}$. The extracted I_{ON} is shown in Figs.4-12 and 4-13 for N- and PMOS FETs, respectively. The I_{ON} in both N- and PMOS NWs over $L_g > 100\text{nm}$ follows the general I_d behavior in saturation region illustrated as straight lines, and the equation without body-effect coefficient m is shown as (cf. Eq. (1-9)):

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$$I_{d_sat} = \mu_{eff} C_{ox} \frac{W_{tot}}{L_g} \cdot \frac{V_{gt}^2}{2} \quad (4-2)$$

In contrast, the I_{ON} is saturated below $L_g < 100\text{nm}$, and the limitation is occurred by carrier velocity limit and is interpreted as:

$$I_{sat} = C_{ox} W_{tot} V_{gt} v_{lim} \quad (4-3)$$

where v_{lim} is the limiting velocity of the carriers during transport. The velocity v_{lim} is limited by the saturation velocity v_{sat} in drift-diffusion transport and the injection velocity v_{inj} in quasi-ballistic transport [4-15].

For NMOS, [110]-SOI with H_2 anneal and [100]-SOI devices show roughly the same values as reference [110]-SOI NWs, except in over $L_g > 400\text{nm}$. Beneficial impact of the tensile strain can be clearly seen with the I_{ON} gain of +61% at least in entire L_g range compared with reference SOI NWs. The I_{ON} enhancement over 60% at $L_g = 22\text{-}23\text{nm}$ is higher than previous sSOI devices [4-8,4-16].

For PMOS, SOI- H_2A devices show degraded I_{ON} with the maximum loss of -69% in whole L_g range. This agrees with the prediction for the strange V_t behavior that channel conduction in SOI- H_2A NW could be worse than reference SOI device. On the other hand, the compressive strain provides the huge advantage, especially in shorter L_g region (*e.g.* at minimum L_g of 17-18nm with the gain of +137% for cSG-S/D, and of +323% for SGOI, respectively). Consequently, it is concluded that the uniaxial strain technologies in ultra-scaled NW N- and PMOS FETs efficiently improve the I_{ON} , especially for PMOS a dramatic enhancement is achieved by SGOI NW architecture.

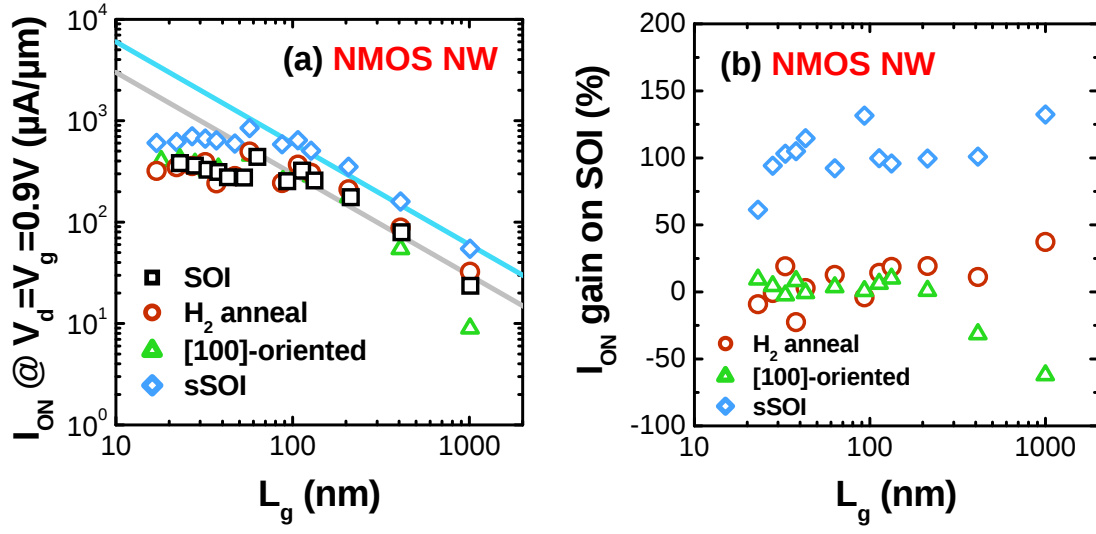


Fig. 4-12. (a) Extracted I_{ON} and (b) the gain compared with reference SOI as a function of L_g in the narrowest NMOS NWs for all the technological parameters.

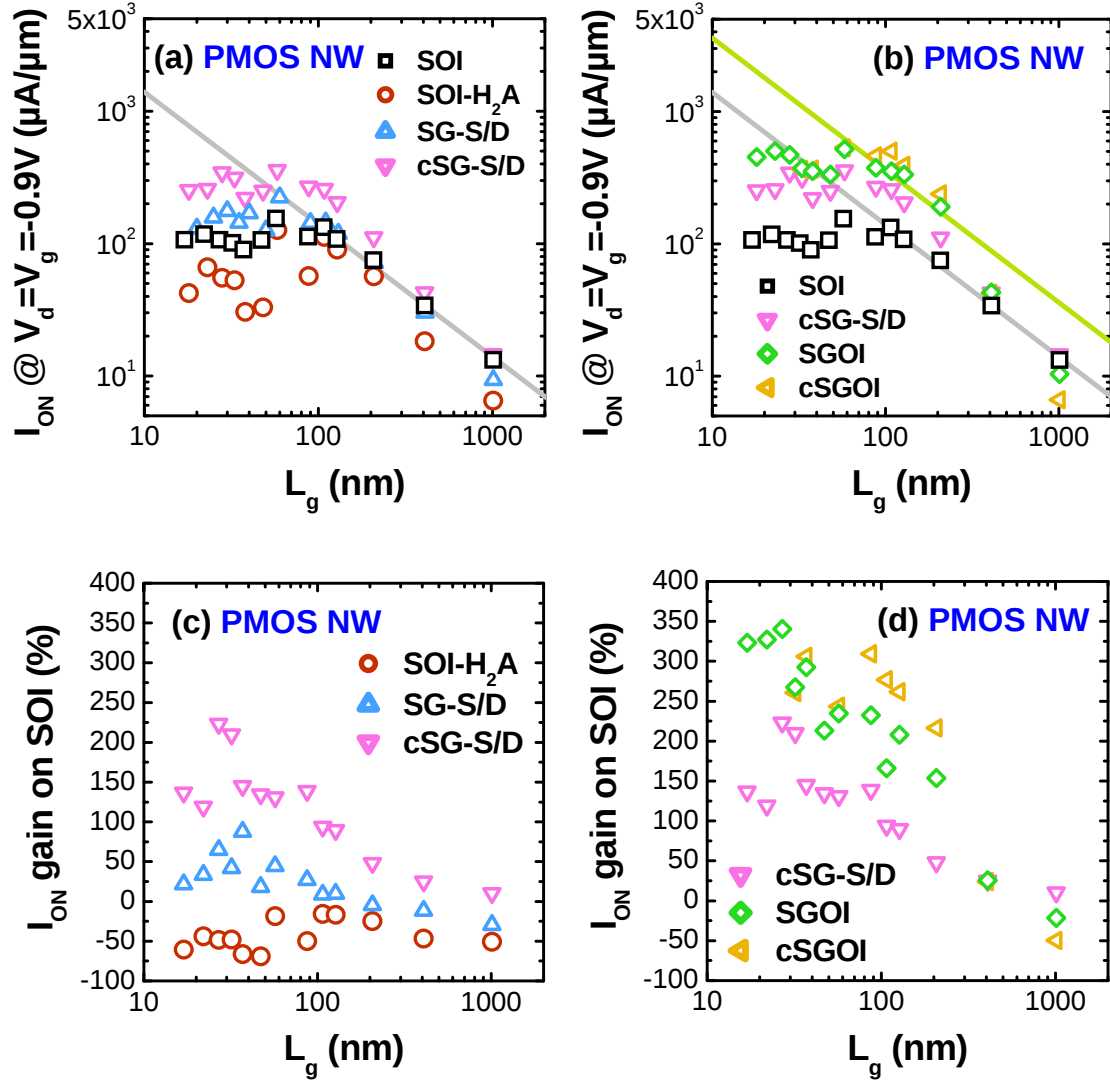


Fig. 4-13. (a,b) Extracted I_{ON} and (c,d) the gain compared with reference SOI as a function of L_g in the narrowest PMOS NWs for all the technological splits.

The I_{ON} - I_{OFF} performance in the narrowest NWs with L_g between ~ 110 nm and 17 nm is reported in Fig.4-14. Off-state current I_{OFF} is extracted at $V_g=0$ V and $|V_d|=0.9$ V. The I_{ON} enhancement and level shift of I_{OFF} by stressors effect are visible.

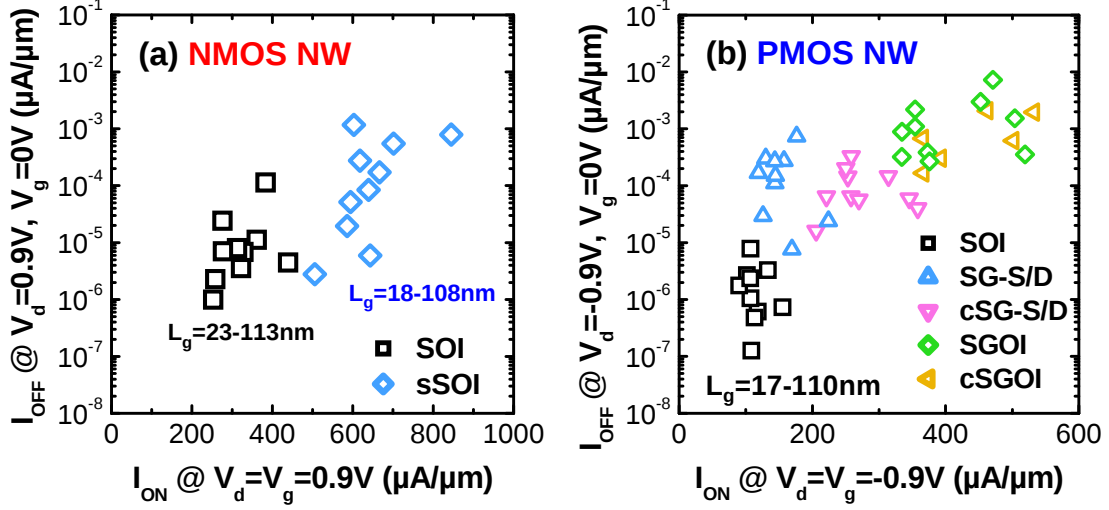


Fig. 4-14. I_{ON} - I_{OFF} performance in the narrowest NW (a) NMOS and (b) PMOS FETs with comparison of stressor impacts.

4.2 Temperature dependent effective mobility

Effective carrier mobility μ_{eff} has been systematically measured as a function of temperature, from room temperature (300K) down to 20 K, in order to investigate the different scattering mechanism involved in carrier transport. Here, the measurements have been performed in 10 μ m-long tri-gate (TG) and omega-gate (Ω G) NWs with multiple 50-channel fingers, since sufficient channel area is necessary for μ_{eff} extraction based on split C-V technique. Ω GNW structure was formed with additional H₂ anneal process. Figure 4-15 shows the μ_{eff} of electron and hole extracted as a function of inversion carrier density N_{inv} for SOI TGNW and wide FETs. For NWs, μ_{eff} was obtained through C_{gc} measurement which takes into account inversion carrier density in the whole structure, involving side-walls and top surface.

The electron mobility in NMOS TGNW is degraded as compared to wide FET in the whole range of N_{inv} . In particular, the degradation in NMOS is larger in high N_{inv} region above $0.4 \times 10^{13} \text{ cm}^{-2}$, and is more severe at low temperature. The maximum peak

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mobility $\mu_{\max}$ is shifted to lower N_{inv} for NMOS TGNW (*e.g.* $\mu_{\max} \approx 650 \text{ cm}^2/\text{Vs}$ at $N_{\text{inv}} \approx 0.2 \times 10^{13} \text{ cm}^{-2}$ and $T=100\text{K}$) compared to wide FET ($\mu_{\max} \approx 800 \text{ cm}^2/\text{Vs}$ at $N_{\text{inv}} \approx 0.6 \times 10^{13} \text{ cm}^{-2}$ and $T=100\text{K}$). The degradation for NMOS in TGNW is in good agreement with the increasing contribution of the (110)-oriented side-walls as the transistor width is reduced down to NW [4-13,4-17]. Indeed, the electron mobility is degraded in (110)/[110] channel [4-18]. The impact of the 3D architecture for NMOS can be clearly evidenced in TGNWs. Figure 4-16 shows comparison of the μ_{eff} behavior between $W_{\text{top}}=10\text{nm}$ and $W_{\text{top}}=30\text{nm}$ SOI TGNWs. The peak shift of $\mu_{\max}$ and deep mobility deterioration in the narrowest NW with $W_{\text{top}}=10\text{nm}$ at higher N_{inv} region are visible. Furthermore, below 100K, $\mu_{\max}$ in the narrowest NW becomes lower than in wider NW.

On the other hand, the hole mobility of TGNW is improved in medium-high N_{inv} region. Moreover, there is no significant shift of $\mu_{\max}$ for PMOS NWs. As for NMOS, the mobility improvement for PMOS TGNW is in good agreement with the increasing contribution of the (110)-oriented side-walls, as the hole mobility in (110)/[110] channel is higher than the one in (100)/[110] channel.

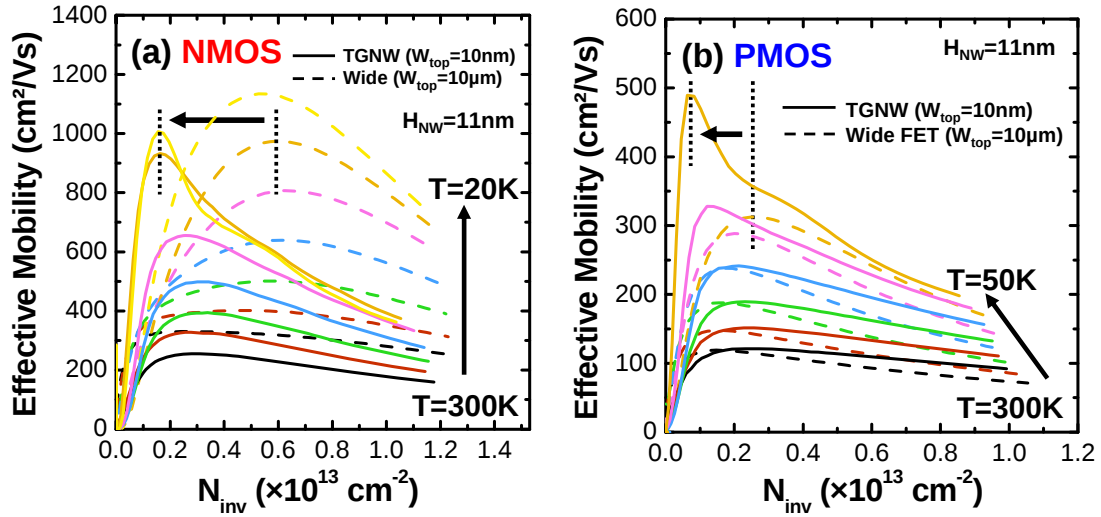


Fig. 4-15. Effective mobility μ_{eff} extracted as a function of N_{inv} in SOI TGNW and wide FETs at varying temperatures (from 300K down to 20K) for (a) NMOS and (b) PMOS devices.

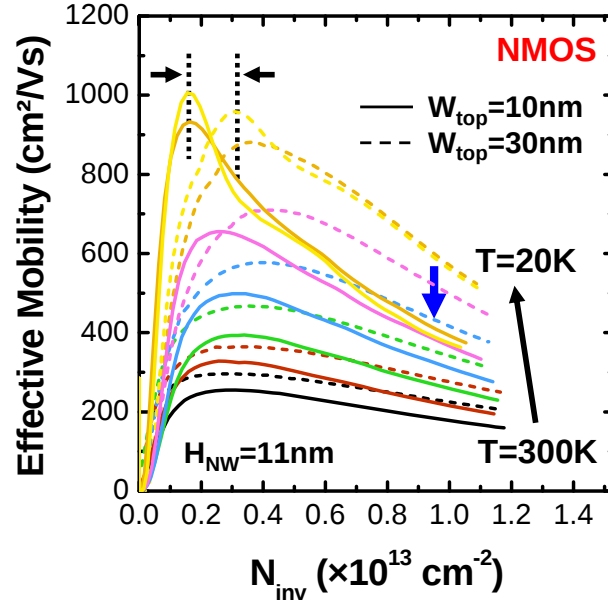


Fig. 4-16. Effective mobility μ_{eff} extracted as a function of N_{inv} in SOI TGNW NMOS FETs with $W_{\text{top}}=10\text{nm}$ and $W_{\text{top}}=30\text{nm}$ at varying temperatures (from 300K down to 20K).

4.2.1 Extraction of contributions of side-wall and top surfaces

In the following, the contribution of the top and side-wall surfaces on mobility of TGNW μ_{TG} is discussed, using the total mobility expressed as [4-14,4-17]:

$$\mu_{\text{TG}} = \frac{W_{\text{top}}}{W_{\text{tot}}} \mu_{\text{top}}^{(100)} + \frac{2H_{\text{NW}}}{W_{\text{tot}}} \mu_{\text{side-wall}}^{(110)} \quad (4-4)$$

where μ_{top} and $\mu_{\text{side-wall}}$ are the mobility corresponding to each surface orientation, which is (100) top surface, and (110) side-walls, respectively. Using this equation and making the reliable assumption that the mobility in (100) top surface μ_{top} is simply given by the 10 μm -wide FETs, the mobility contributions of the top and the side-walls can be de-correlated for both N- and PMOS TGNWs. The extracted contributions as a function of N_{inv} at 300 K are shown in Fig.4-17. The $\mu_{\text{side-wall}}$ of both N- and PMOS is in good agreement with the experimental data of reference Si(110) wide FET, showing that the transport properties of TGNWs in strong inversion regime are mainly governed by the independent inversion surfaces.

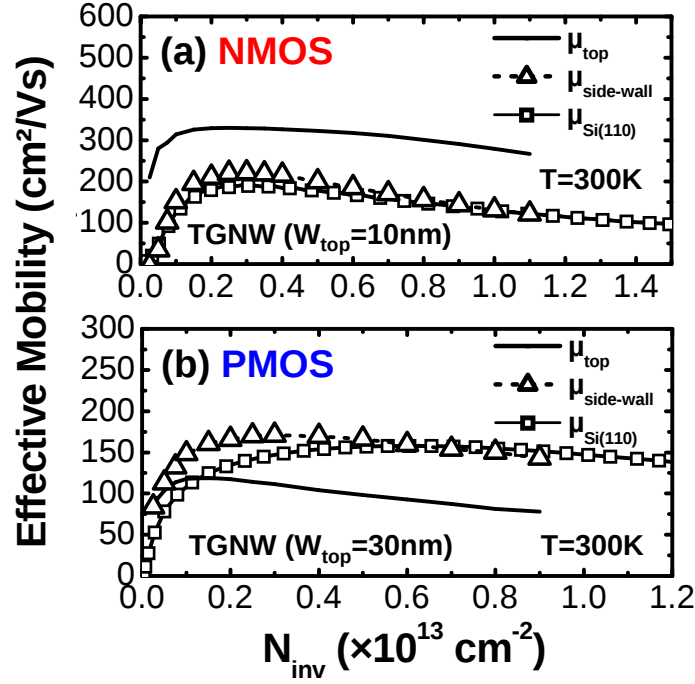


Fig. 4-17. Extraction of the (100) top and (110) side-wall mobility contributions at 300K in SOI TGNW FETs as a function of N_{inv} for (a) NMOS with $W_{\text{top}}=10\text{nm}$ and (b) PMOS with $W_{\text{top}}=30\text{nm}$. The experimental data in Si(110) wide MOSFET $\mu_{\text{Si(110)}}$ is also shown as a reference.

The different contributions have also been extracted at 50K, and plotted in Fig.4-18. For NMOS, the contribution of surface roughness scattering in NW is drastically increased due to the enhanced side-wall contribution, and is in good agreement with data reported for (110)/[110] electrons in literature [4-18,4-19]. Furthermore, the μ_{max} in NW is shifted to lower N_{inv} , and could indicate a reduced contribution of Coulomb scattering for the side-walls. For PMOS, the mobility limited by surface roughness scattering μ_{SR} in side-walls is slightly enhanced, leading to better mobility at high N_{inv} region for NW compared to the wide FET. Similarly to NMOS, (110) side-walls in PMOS also show dramatically reduced Coulomb scattering contribution.

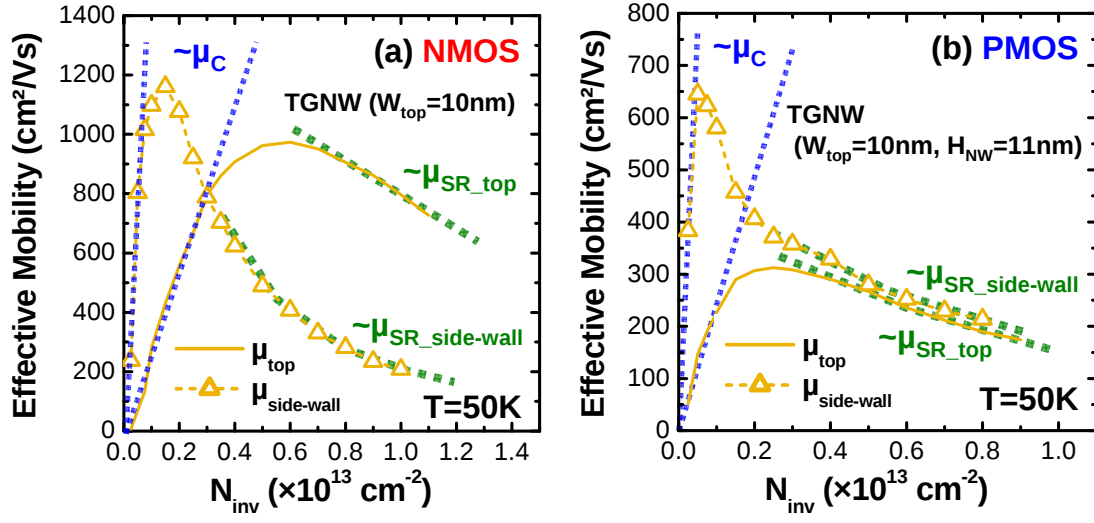


Fig. 4-18. Extraction of the μ_{top} and $\mu_{\text{side-wall}}$ contributions at 50K in SOI TGNW FETs with $W_{\text{top}}=10\text{nm}$ as a function of N_{inv} for (a) NMOS and (b) PMOS devices.

4.2.2 Tri-gate vs. omega-gate

The μ_{eff} of electron and hole is compared for SOI TG and Ω G NW FETs with similar width in Fig.4-19. For PMOS, the mobility in Ω G and TG NWs are very similar in the whole range of N_{inv} and temperature, with a slightly higher mobility at low N_{inv} for Ω GNW. On the other hand, differences appear for NMOS at low temperature: the mobility is higher for Ω GNW at low N_{inv} , while it is deteriorated at high N_{inv} region. A different surface roughness influence due to circular shape can be distinguished below 50K. However, these results show that the shape of the NWs (rectangular vs. semi-circular) has only a little influence on carrier transport for the dimension as small as $10\text{nm} \times 10\text{nm}$ at room temperature. Impact of the (110) side-wall surface can still be distinguished even in the semi-circular geometry of Ω GNW. The difference at low N_{inv} could indicate a lower contribution of Coulomb scattering in the case of Ω GNWs, due to additional H_2 anneal process, in contrast with previous study in 3D-stacked GAA NW FETs [4-5,4-20]. The change of Coulomb scattering contribution originating from additional H_2 anneal is also confirmed even in $10\mu\text{m}$ -wide FETs in Fig.4-20.

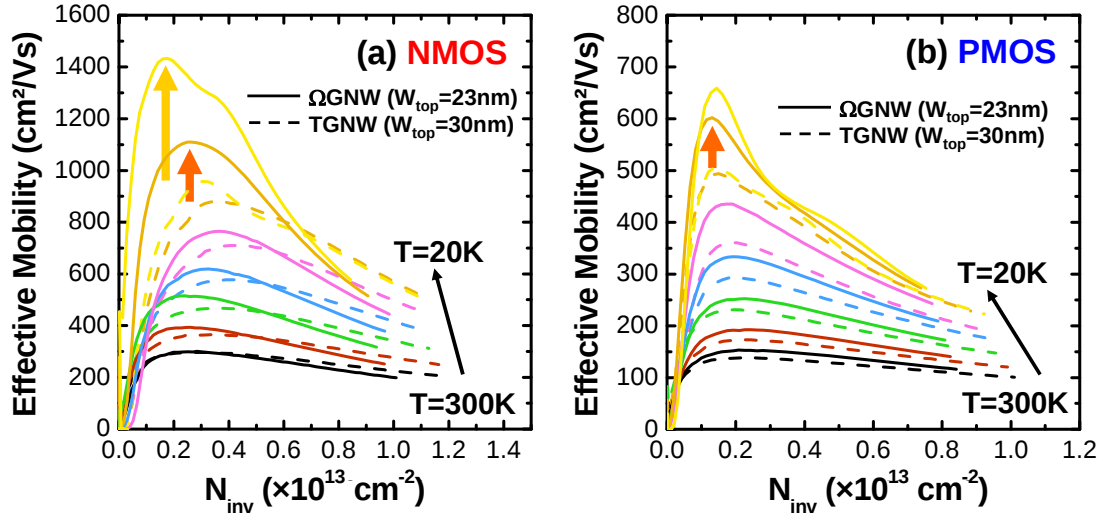


Fig. 4-19. Effective mobility μ_{eff} as a function of N_{inv} extracted at varying temperatures for SOI TG and ΩG NW (a) NMOS and (b) PMOS devices.

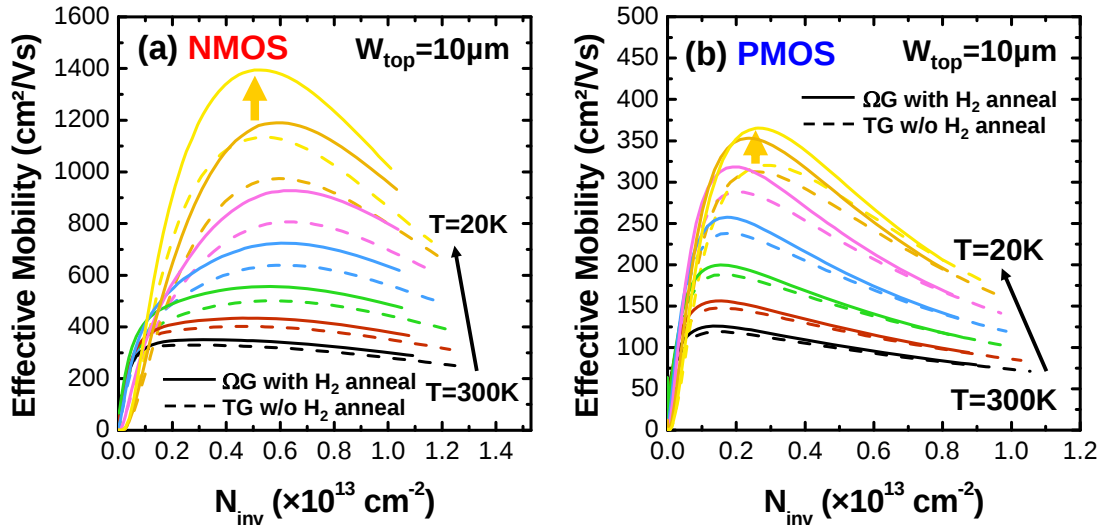


Fig. 4-20. Effective mobility μ_{eff} as a function of N_{inv} extracted at varying temperatures in SOI wide FET with or without additional H_2 anneal process for (a) NMOS and (b) PMOS devices.

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4.2.3 Impact of tensile strain

In the following, the impact of an additional tensile strain on transport properties is discussed. The tensile strain is expected to be beneficial for electron transport in NMOS FETs. The significant improvement of electron mobility with tensile strain at various temperatures is confirmed in Fig.4-21a for TGNWs. The maximum mobility values for sSOI FETs, $\mu_{\max} \approx 750 \text{ cm}^2/\text{Vs}$ at $N_{\text{inv}} \approx 0.2 \times 10^{13} \text{ cm}^{-2}$ and $T=100\text{K}$ in TGNW and $\mu_{\max} \approx 950 \text{ cm}^2/\text{Vs}$ at $N_{\text{inv}} \approx 0.7 \times 10^{13} \text{ cm}^{-2}$ and $T=100\text{K}$ in wide FET, are enhanced (Fig.4-21b). In addition, the $\mu_{\max}$ peak shift between wide FET and TGNW is similarly observed for sSOI FETs.

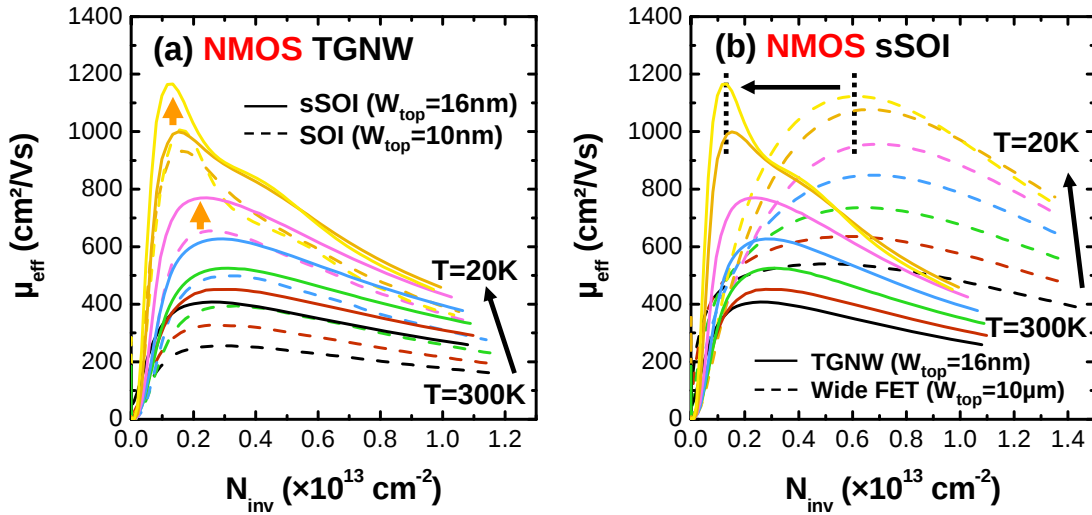


Fig. 4-21. Effective mobility μ_{eff} as a function of N_{inv} extracted at varying temperatures, showing (a) comparison between sSOI wide FET and TGNW devices, and (b) comparison between SOI and sSOI TGNW FETs.

Figure 4-22 shows the μ_{eff} extracted at high $N_{\text{inv}}=1.0-0.8 \times 10^{13} \text{ cm}^{-2}$ as a function of channel width W_{top} with comparison between SOI and sSOI devices in TG and ΩG FETs. For SOI devices, the behavior is well explained by the contribution of top and side-wall mobility and the surface orientation dependence of the mobility (Table 4-1). The Si(110) side-walls are beneficial to hole transport parallel to [110]-oriented channel, while Si(100) top surface is advantageous to electron transport. For NMOS, the

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mobility is therefore degraded as top surface area decreases, *i.e.* as the W_{top} decreases. On the other hand, the mobility in PMOS is increased as side-wall contribution enlarges. The hole mobility enhancement and the electron mobility degradation as W_{top} decreases is similar in TG and Ω G NWs as already noticed.

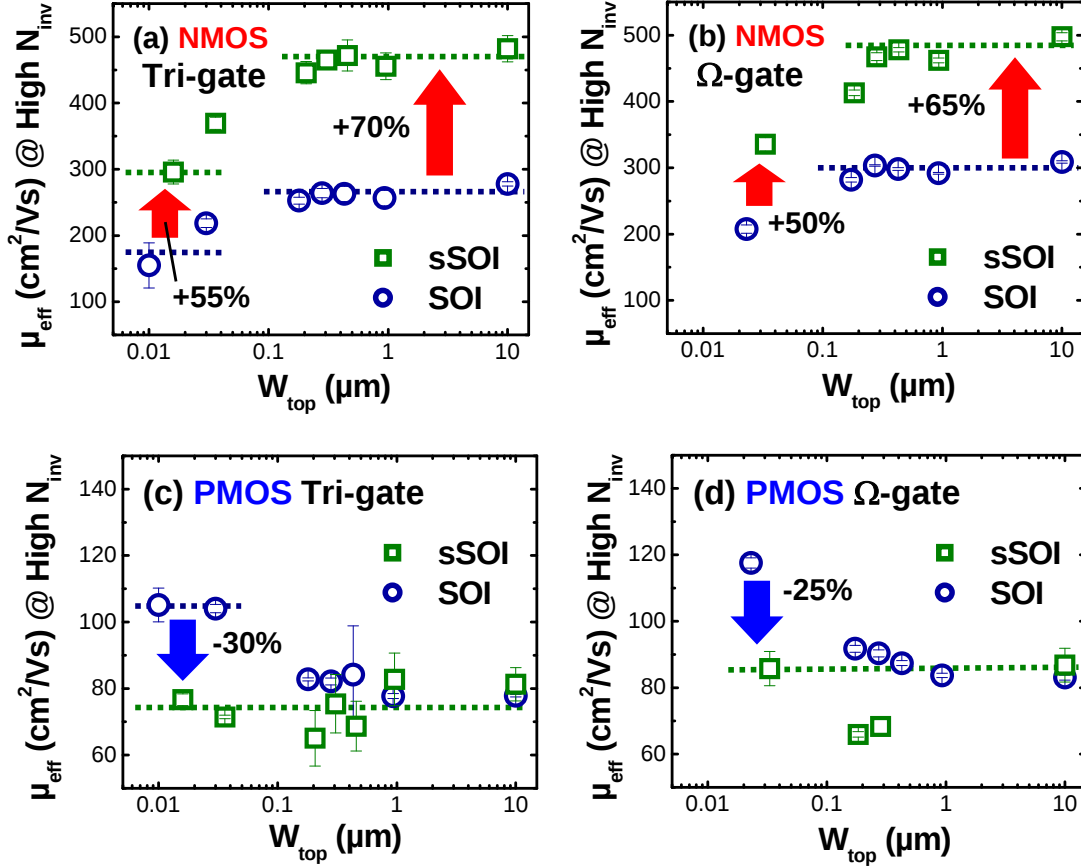


Fig. 4-22. Effective mobility μ_{eff} at high N_{inv} as a function of W_{top} for SOI and sSOI (a,b) NMOS and (c,d) PMOS FETs at room temperature (300K) with comparison between (a,c) TG and (b,d) Ω G devices. The mobility was extracted at $N_{\text{inv}}=10^{13} \text{ cm}^{-2}$ for the both N- and PMOS TG FETs. In Ω G devices, the mobility was extracted at $N_{\text{inv}}=0.9 \times 10^{13} \text{ cm}^{-2}$ for NMOS, and $N_{\text{inv}}=0.8 \times 10^{13} \text{ cm}^{-2}$ for PMOS FETs, respectively.

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Table 4-1. Brief summary of strain effect on carrier transport along [110]-oriented channel for various stress configurations (mainly established from piezoresistive coefficients and results given in Refs. [4-19,4-21~4-28]).

Strain (transport //[110])	NMOS		PMOS	
	(100)	(110)	(100)	(110)
no strain	0	-	0	+
biaxial tensile	+		- / =	
uniaxial tensile // [110]	++	++	--	-

For sSOI devices the effect of tensile strain for different surface orientations and stress conditions (biaxial vs. uniaxial) has to be taken into account to understand our results. As the width decreases, the biaxial stress in wide (100) plane changes to a uniaxial stress along the [110]-oriented channel direction originating from lateral strain relaxation (cf. Fig.2-7). Physical and electrical characterizations have shown that full lateral relaxation occurs in our NWs for W_{top} below roughly 50 nm [4-8].

Figure 4-22 shows that the addition of a uniaxial tensile strain is very effective in TG NMOS devices. In particular we have obtained electron mobility enhancement in sSi NWs (with up to +55% gain in μ_{eff} for $W_{\text{top}}=10\text{nm}$) which overcomes the electron mobility loss inherent to unstrained Si NWs with (110) side-walls (Fig.4-22a,b). On the contrary, for PMOS, the hole mobility is degraded by tensile uniaxial stress along the channel, especially for (100) surface (Table 4-1 [4-21]). In (110) side-wall surface the better hole mobility in unstrained case is counterbalanced by the detrimental effect of a uniaxial tensile strain. As a result, as the width W_{top} is decreased the total hole mobility in sSOI NWs is no more improved as compared to wide transistors, and remains roughly constant with W_{top} variation (Fig.4-22c,d).

We also noticed that both TG and Ω G NWs exhibit roughly the same mobility improvement/degradation for the similar W_{top} , for NMOS as well as for PMOS. This result suggests that the strain relaxation is the same in both geometries, and that the piezoresistive properties are identical in TG and Ω G NWs despite the more complex inversion surface orientations of Ω GNW.

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In order to have a better understanding of the physics behind, and a more quantitative model, one must also account for the confinement effect in NWs [4-29~4-32]. For NMOS NWs, a uniaxial tensile strain favors the proportion of fast electrons, and suppresses intervalley scattering, which enhances the mobility. The strain has also significant effects on the transport mass of -z valleys in [110] Si NWs [4-30]. In particular a shear stress breaks the symmetry between transverse mass axes of the Δ_z valleys, leading to the decrease of the transport effective mass for tensile strain ($\epsilon_{||}>0$). The decrease of effective mass enhances the average velocity of the carriers, reduces intersubband scattering, and therefore increases the mobility. For PMOS, the confinement of Si NWs tends to promote light holes (LH) bands in [110] directions. A compressive strain strengthens the LH character of the highest valence subbands, pushing heavy hole (HH) subbands down. This leads to a large increase of the mobility. On the contrary, tensile strain brings back up HH subbands which degrade the total mobility.

All these results are in qualitative agreement with the piezoresistance (PR) measurements performed on corresponding NWs, giving the longitudinal piezoresistive coefficients $\pi_L = -545 \times 10^{-12} \text{Pa}^{-1}$ and $\pi_L = +280 \times 10^{-12} \text{Pa}^{-1}$ for NMOS and PMOS TGNWs, respectively [4-33,4-34]. In the PR theory, we have $\Delta\mu/\mu = -\pi_L \times \sigma_{\text{stress}}$, with σ_{stress} the applied stress in the longitudinal direction. The sign of π_L denotes an increase or a decrease of mobility with a compressive ($\sigma_{\text{stress}} < 0$) or a tensile ($\sigma_{\text{stress}} > 0$) stress.

Next, the μ_{eff} extracted at a constant high N_{inv} (0.7 and $0.8 \times 10^{13} \text{cm}^{-2}$ for PMOS and NMOS, respectively) has been plotted as a function of temperature, for both SOI and sSOI FETs (Fig.4-23). Below 100 K, the phonon scattering contribution is negligible, and the mobility at high N_{inv} saturates, as a consequence of the dominant surface roughness scattering contribution. TG and Ω G NWs also exhibit the same mobility behavior in both N- and PMOS case. For NMOS, phonon-limited mobility at high temperature (above 100K) is improved for strained devices. Electron mobility is degraded on the narrowest W_{top} in both SOI and sSOI FETs without correlation to the channel shape, in agreement with dominant (110) side-walls for NWs. For PMOS, the mobility improvement of wide FETs and the degradation of NWs in sSOI FETs are observed in the whole temperature range. The hole mobility is degraded by surface

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roughness scattering on uniaxial strained NWs in contrast to the improvement in biaxial strained wide FETs.

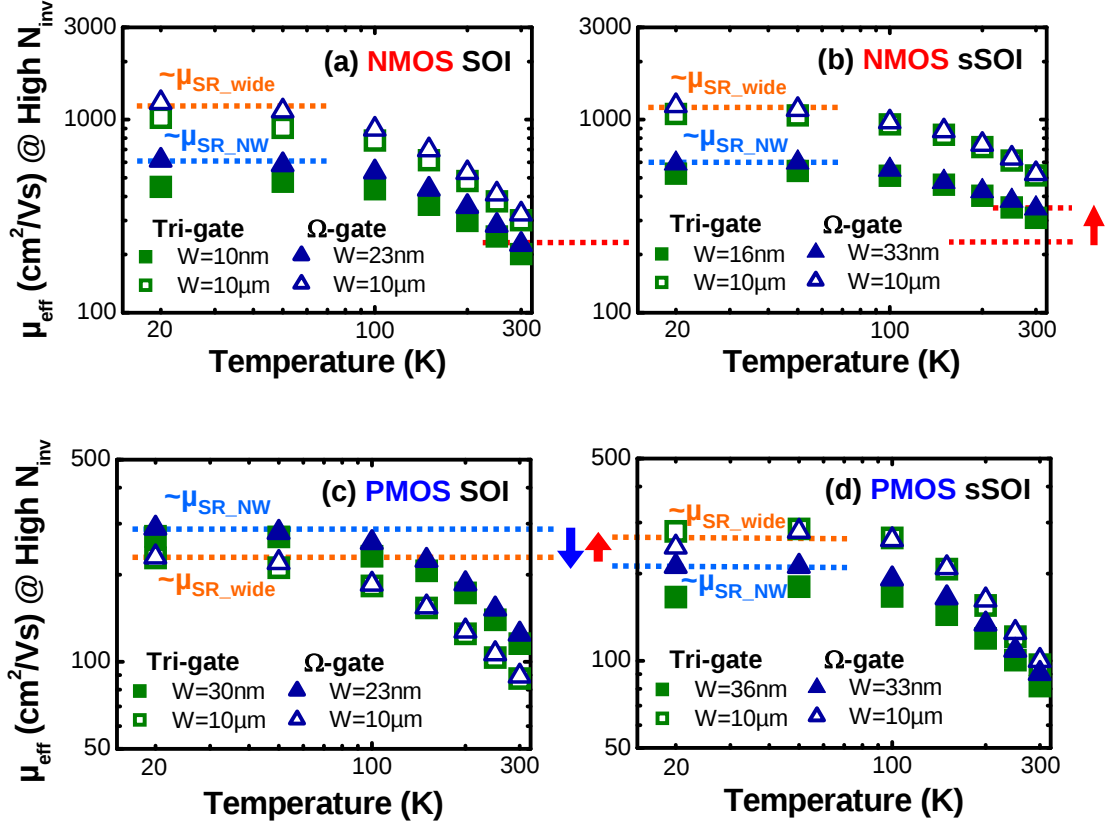


Fig. 4-23. Effective mobility μ_{eff} extracted at high N_{inv} as a function of temperature in (a,c) SOI and (b,d) sSOI devices for (a,b) NMOS and (c,d) PMOS FETs. The mobility was extracted at $N_{\text{inv}}=0.8 \times 10^{13} \text{ cm}^{-2}$ for NMOS and $N_{\text{inv}}=0.7 \times 10^{13} \text{ cm}^{-2}$ for PMOS devices, respectively.

Finally, Fig 4-24 and Table 4-2 show the values of the power law exponent γ of the temperature dependent maximum mobility ($\mu_{\text{max}} \sim T^{-\gamma}$) extracted for all the FETs studied here. Above 77 K, the slope of the temperature dependent mobility is driven by phonon scattering, especially at moderate N_{inv} (typically around μ_{max}). For SOI or sSOI, the values do not differ significantly for each structure: wide, TG or Ω G NW FETs. On the other hand, the temperature dependence changes significantly when comparing unstrained (SOI) and strained (sSOI) devices, especially for NMOS. These results are in

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good agreement with values of the temperature coefficient which are similar for (100) and (110) planes [4-18]. They also indicate that the temperature dependence of phonon-limited electron mobility and the hole mobility is mainly governed by the strain effect down to NW with W_{top} of 10nm. A decrease of the values of γ in sSOI NMOS FETs highlights the reduced intervalley phonon scattering by tensile strain. Furthermore, no significant difference in the temperature dependence of μ_{eff} can be observed between TG and Ω G NWs, revealing again no significant influence of cross-sectional shape and dimension of the channel.

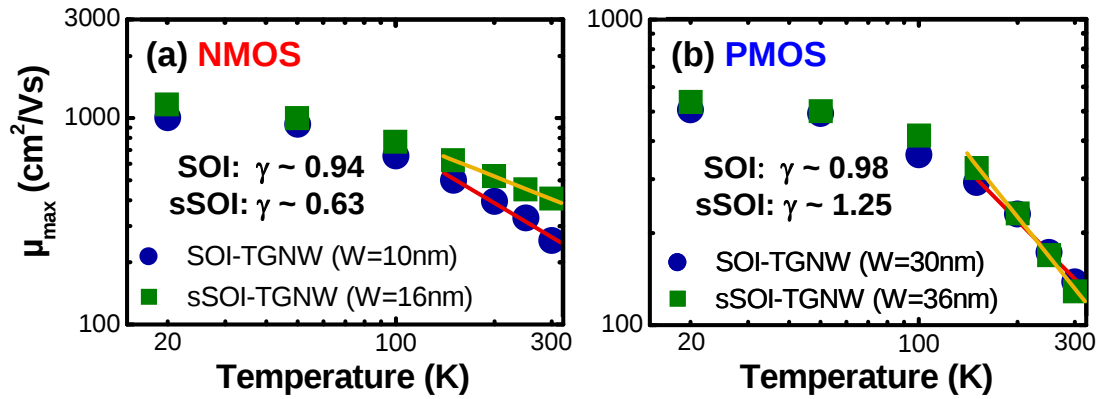


Fig. 4-24. Maximum mobility μ_{max} extracted as a function of temperature in SOI and sSOI (a) NMOS and (b) PMOS TGNW FETs.

Table 4-2. Extracted power law exponent γ in the temperature dependence of maximum mobility $\mu_{\text{max}} \sim T^{-\gamma}$.

Values of power law exponent γ		NMOS		PMOS	
		SOI	sSOI	SOI	sSOI
Tri-gate w/o H ₂ anneal	Wide (10 μ m)	0.95	0.64	1.00	1.18
	NW	0.94	0.63	0.98	1.25
Ω -gate with H ₂ anneal	Wide (10 μ m)	1.05	0.69	1.03	1.07
	NW	1.05	0.41	1.12	1.13

4.3 Low-field mobility

4.3.1 Dependence property on gate length

The μ_0 is extracted using the Y-function method as a function of L_g for the narrowest single-channel NW and widest FETs for reference SOI in Fig.4-25. Both N- and PMOS devices exhibit a decreasing trend of μ_0 with L_g below 200nm and this trend is in agreement with previous observations on wide bulk and SOI devices [4-15,4-35~4-37]. This degradation with decreasing L_g is often attributed to the enhanced impurity scattering influence due to closer proximity between S/D regions [4-38]. The degradation is more abrupt in NWs, mainly occurring in the range below 100nm. This may be attributed to emphasized one dopant influence in NW, *i.e.* the narrow contact between body and S/D regions. For PMOS case, it should be noticed that NW shows lower μ_0 than wide FET in the degraded region. As mentioned above, studies on effective mobility in 10 μ m-long 50-multiple channel tri-gate NW FET with (100) top surface shows mobility improvement compared to the wide FET owing to (110) side-wall contribution with an advantage for hole transport [4-14,4-17]. These extractions seem to indicate that the length dependent μ_0 deterioration is more significant for NW device, compensating and exceeding the mobility advantage by surface orientation contribution.

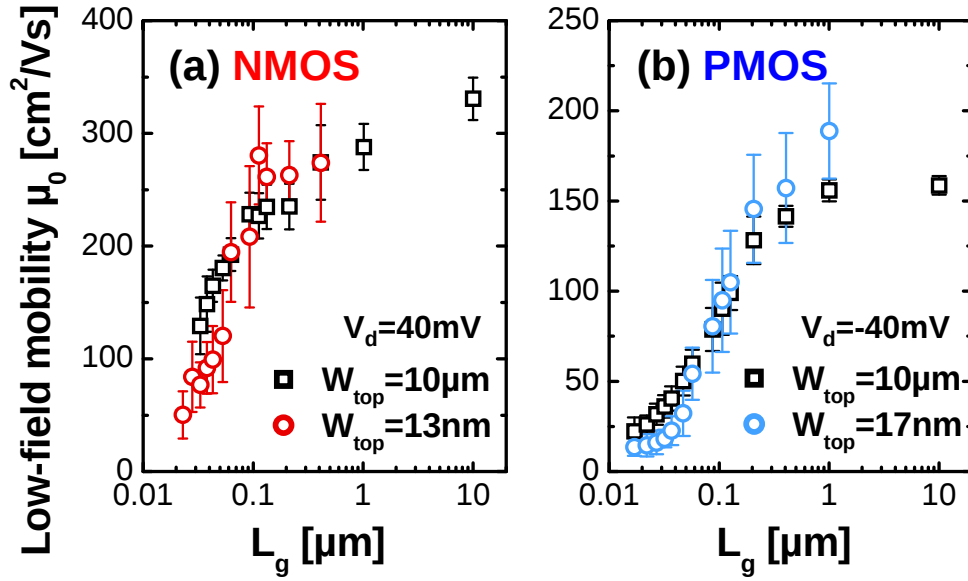


Fig. 4-25. Low-field mobility μ_0 as a function of L_g with comparison between the widest FETs and narrowest NWs in reference SOI (a) NMOS and (b) PMOS devices.

Figure 4-26 demonstrates again that sSOI devices provide great advantage to enhance electron transport compared to the others. For the widest FETs, the mobility gain relative to reference SOI devices is decreased as L_g is shortened (Fig.4-26c), while the long devices have a μ_0 gain as high as +110% at a maximum. The advantage is sustained in the narrowest NWs, and the gain is maintained in whole L_g range with a value of $\sim +50\%$ whatever L_g (Fig.4-26d). The difference in the gain behavior between wide FETs and NWs results from the strain configuration: biaxial tensile strain for wide FETs or uniaxial tensile strain for NWs. Additional H_2 anneal process degrades the μ_0 in entire L_g range with the detrimental gain (loss) down to -49% for both widest and narrowest NW FETs. [100]-oriented devices show similar μ_0 level for wide FETs and the narrowest NWs despite a better conduction expected for electrons in the side-walls [4-37].

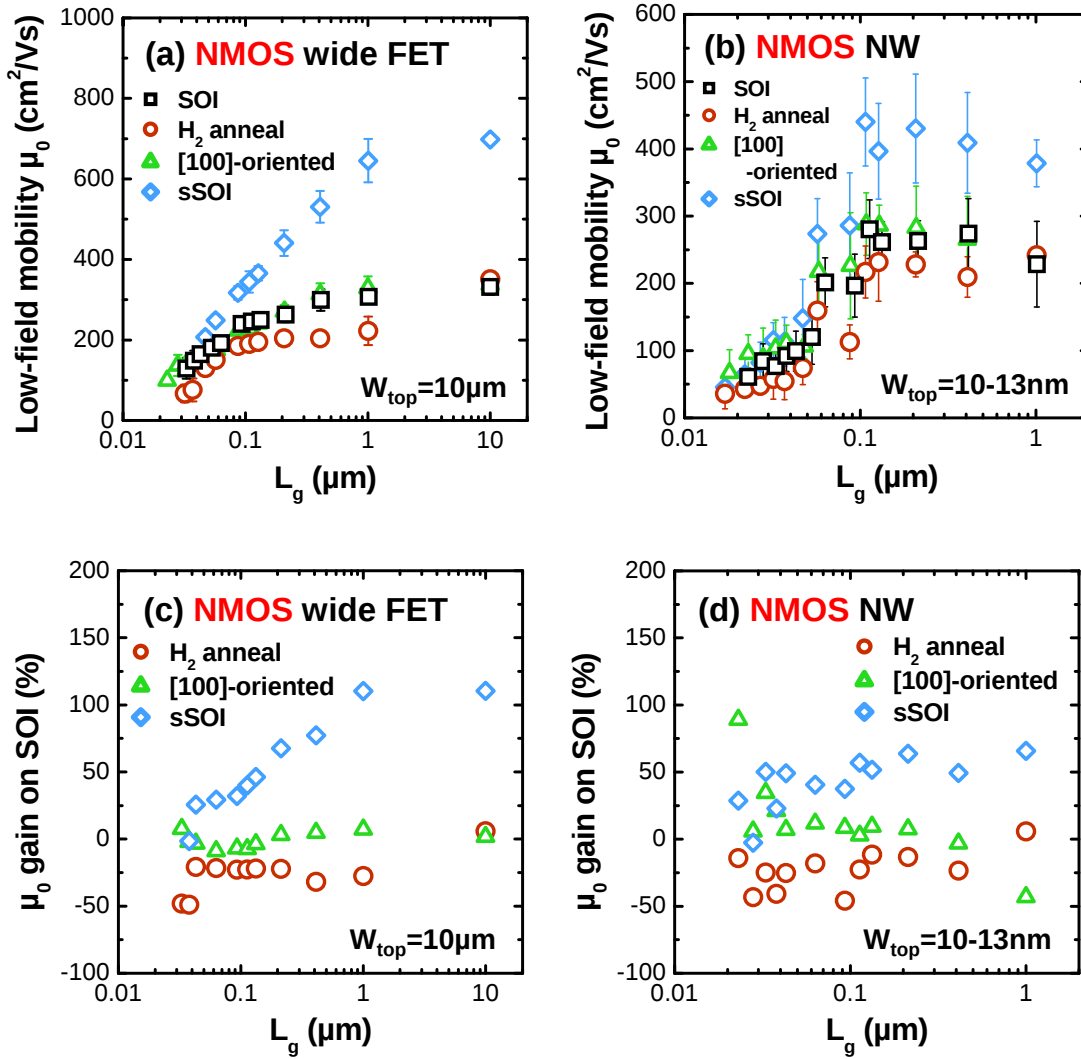


Fig. 4-26. Low-field mobility μ_0 as a function of L_g with comparison among NMOS technological splits in (a) the widest FET and (b) the narrowest NW devices. (c,d) Summary of μ_0 gain compared with reference SOI case.

Figure 4-27 summaries low-field mobility for PMOS devices. Additional H₂ anneal degrades somewhat the hole mobility in wide FETs, and almost maintains the performance for the narrowest NWs except long devices with $L_g = 1 \mu\text{m}$. The 3-types of stressor (SiGe channel, SiGe S/D, and compressive CESL) efficiently improves hole mobility in both wide and NW FETs, especially for NW devices. For wide FETs, all stressors are effective in the devices with shorter L_g than 400nm, and a maximum μ_0

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peak is observed at $L_g=400\text{nm}$ for n- and cSG-S/D devices. The μ_0 gain compared to reference SOI case is calculated and plotted in Fig.4-27e. We have obtained a gain as high as $\sim+60\text{-}65\%$ for L_g ranging from 32nm to 127nm for cSG-S/D and cSGOI devices.

Strained NWs show a maximum μ_0 around $L_g=100\text{nm}$ as a competition between strain enhanced mobility (which could depend on L_g as for cCESL and SiGe-S/D), and mobility degradation with decreasing L_g due to S/D proximity (as in unstrained NWs). An increasing mobility gain is however observed for decreasing L_g (Fig.4-27f), reaching values as high as $\sim+525\text{-}540\%$ for cSG-S/D and SGOI NWs. In particular SGOI NWs exhibit a spectacular μ_0 gain of $+333\%$ for the shortest L_g of 17-18nm. This result suggests the higher efficiency of a uniform high uniaxial compressive strain on hole transport, compared to a uniaxial strain which depends on the position under the gate (cCESL or SiGe S/D).

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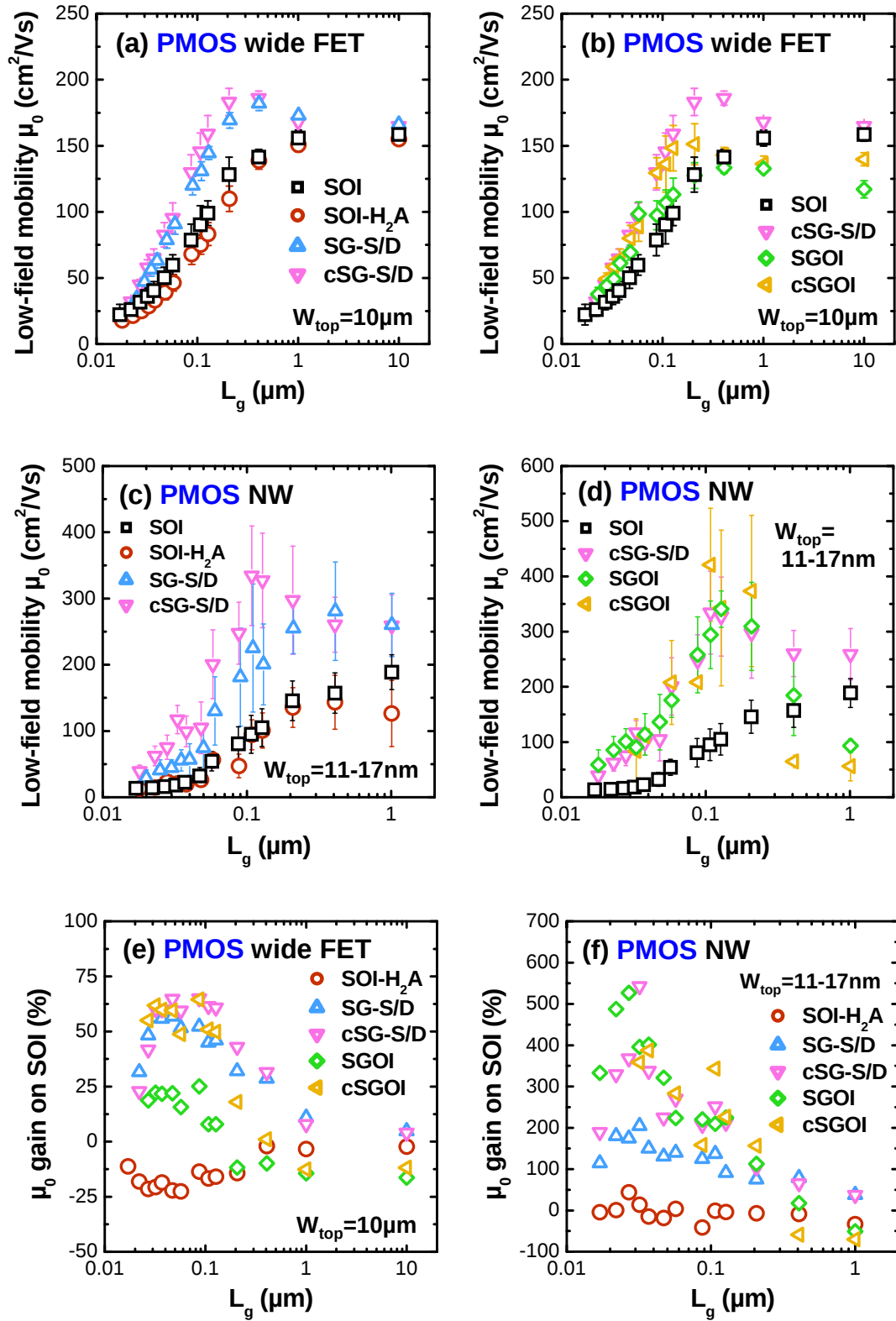


Fig. 4-27. Low-field mobility μ_0 as a function of L_g with comparison among PMOS technological splits in (a,b) the widest FET and (c,d) the narrowest NW devices. (e,f) Summary of μ_0 gain compared with reference SOI case.

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4.3.2 Mobility degradation factor

We use an empirical model to describe the channel length dependent mobility decrease as following [4-15]:

$$\frac{1}{\mu_0(L_g)} = \frac{1}{\mu_{0_max}} + \frac{\alpha_\mu}{L_g} \quad (4-5)$$

Here, two fitting parameters are defined: μ_{0_max} is the maximum low-field mobility, which is almost equal to the saturated value in long channel case, and α_μ is the mobility degradation factor. The extracted degradation factor α_μ shown in Fig.4-28 is a good indicator of the mobility degradation strength in short channel device: the higher α_μ means the larger degradation.

For all NMOS devices, higher degradation rates are found for NW FETs. PMOS SOI and SOI-H₂A devices show the same trend ($\alpha_{\mu_NW} > \alpha_{\mu_wide}$), however the values are largely higher than NMOS cases. For other PMOS FETs with stressors, the degradation rates in NWs are roughly comparable or slightly lower than wide FETs. It is thus summarized that the attenuation tendency in reference SOI PMOS is much more serious compared to NMOS case. But, the issue is relieved by using the compressive strain technologies.

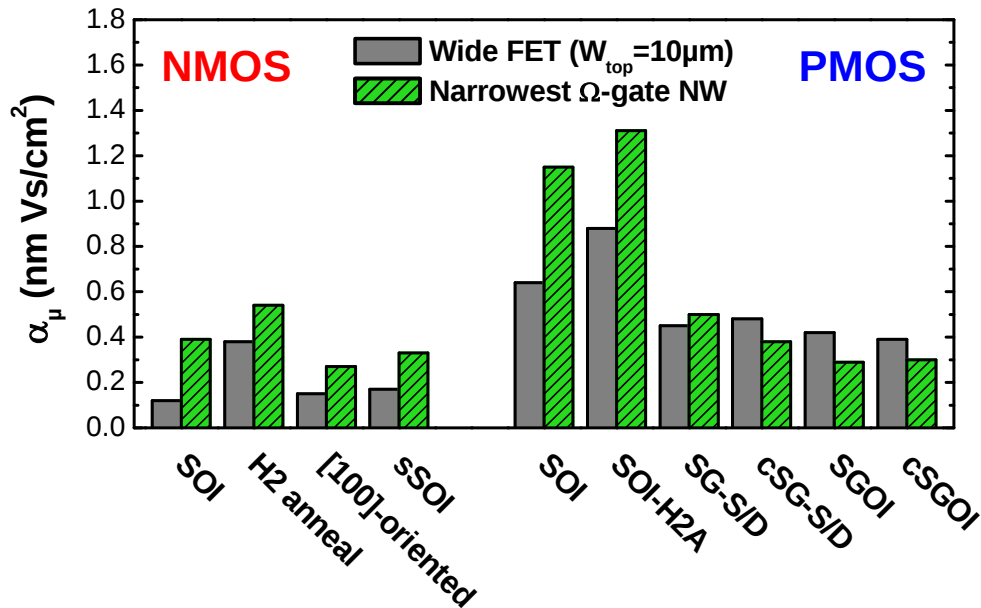


Fig. 4-28. Mobility degradation factor α_μ in the widest FETs and narrowest NWs for all the technological parameters.

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4.3.3 Evaluation of source/drain series resistance

Normalized source/drain series resistance by the total effective channel width W_{tot} , $R_{\text{SD}} (\Omega \mu\text{m}) = R_{\text{SD}} (\Omega) \times W_{\text{tot}} (\mu\text{m})$, extracted by Y-function method is shown in Fig.4-29. We observed a relatively higher resistivity in PMOS ($\sim 150 \Omega \mu\text{m}$) than NMOS ($\sim 100 \Omega \mu\text{m}$) devices. Our results also show higher values of R_{SD} in both N- and PMOS NWs for reference SOI cases, revealing the need to optimize access regions in our NW devices. This tendency is however not clearly observed in other NMOS devices. The normalized resistance in H_2 annealed SOI and [100]-oriented SOI NWs is ameliorated as compared to reference SOI NW, while wide FET in SOI with H_2 anneal shows the deeply worsened. Furthermore, the both widest and narrowest NW FETs in sSOI are upgraded, therefore the benefit of biaxial and uniaxial tensile strain can be reconfirmed. For PMOS devices, the higher resistance of S/D regions in NWs is found for most of technological splits (except cSG-S/D). Even though, 3-types of strained NW FETs, cSG-S/D, SGOI, and cSGOI obtain lower R_{SD} values than reference SOI NW. This indicates the advantage of compressive strain technologies using SiGe in the S/D and/or channel regions.

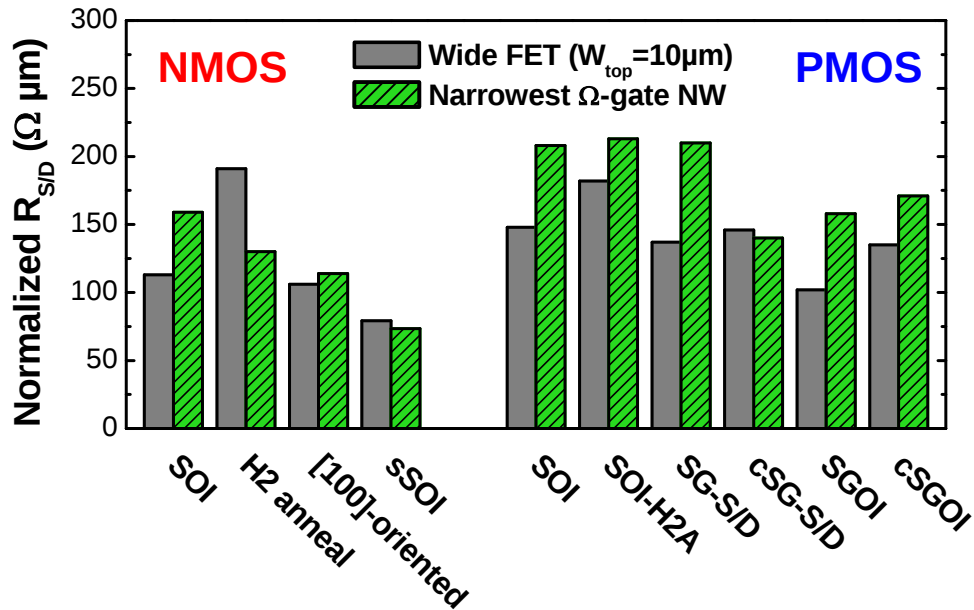


Fig. 4-29. Normalized source/drain resistance R_{SD} in the widest FETs and narrowest NWs for all the technological splits.

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5.1 1/f noise behavior and CNF+CMF model

Normalized drain current noise S_{Id}/I_d^2 as a function of frequency in the narrowest single-channel SOI and sSOI Ω -gate NMOS NWs is shown in Fig.5-1. Although the single NWs show dispersions of noise level and shape, the averaged spectrum measured for 5 or 6 devices exhibits good 1/f noise behavior from threshold up to strong inversion regions for both SOI and sSOI devices. For PMOS, the 1/f noise curves can be also seen in both reference SOI and SGOI NWs as shown in Fig.5-2. Although SGOI NWs show larger dispersion of the noise behavior, the 1/f behavior is sustained on the averaged spectrum for 6 devices. This clearly means that LFN behavior in our both N- and PMOS NWs has the potential to be interpreted by CNF+CMF model [5-1,5-2] even for strain-processed devices.

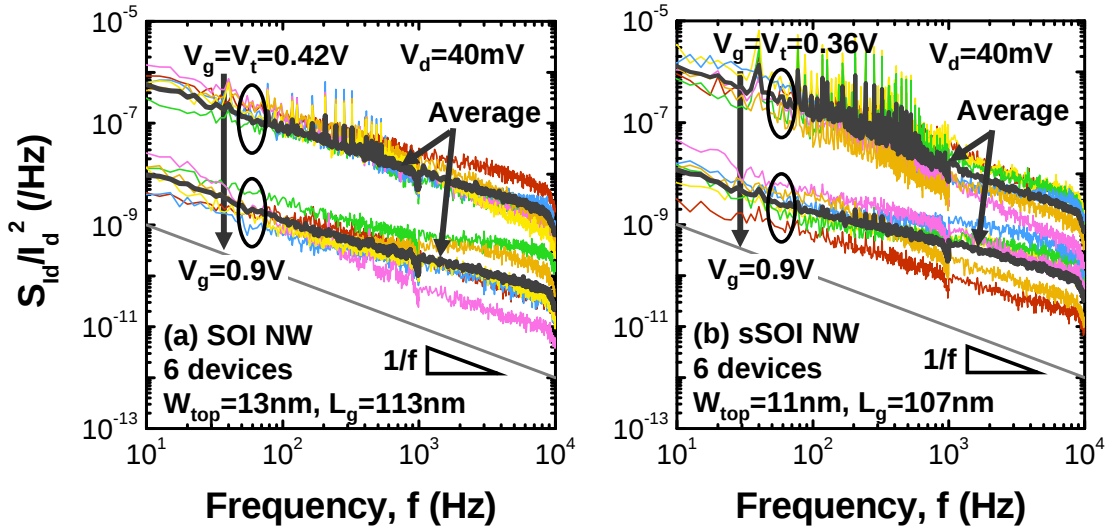


Fig. 5-1. S_{Id}/I_d^2 as a function of frequency in the (a) SOI and (b) sSOI narrowest Ω -gate NW NMOS FETs with $L_g \sim 110\text{nm}$, showing good 1/f behavior at threshold voltage ($V_g = V_t$) up to strong inversion region.

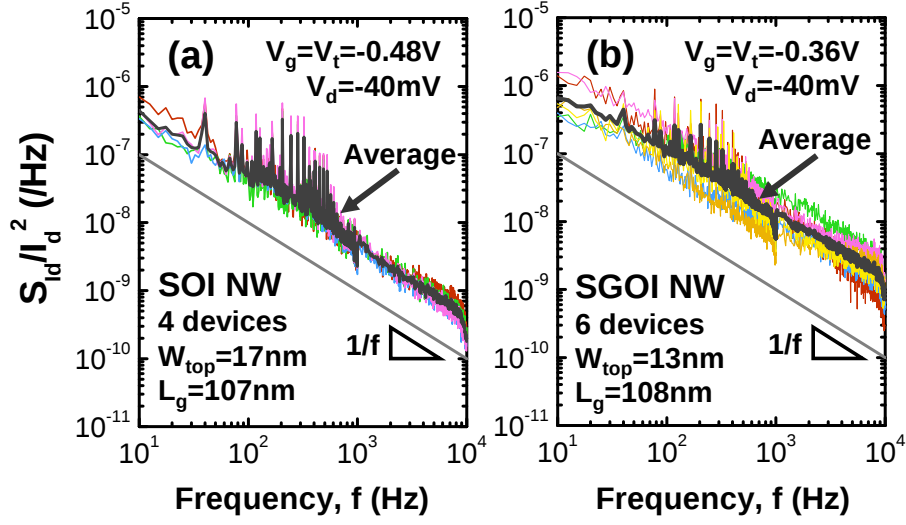


Fig. 5-2. S_{id}/I_d^2 as a function of frequency in the SOI and SGOI narrowest Ω -gate NW PMOS FETs with $L_g=107$ - 108 nm, showing good $1/f$ behavior at threshold voltage ($V_g=V_t$).

In the following, the presence of g-r and/or RTS noise is more carefully discussed. SOI NMOS NWs with $L_g=113$ nm exhibits clear $1/f$ noise as shown in Fig.5-1, however some devices include additional $1/f^2$ noise components. Figure 5-3 shows I_d fluctuation measured for the device including a $1/f^2$ -like spectrum in time domain using three sampling frequencies covering the frequency range of noise measurement between 1Hz and 1MHz. No typical RTS is observed at the three sampling frequencies, whereas a small $1/f^2$ noise spectrum is found. This means that the Lorentzian should correspond to g-r noise caused by a charge trap in silicon body as distinct from the interfacial trap event.

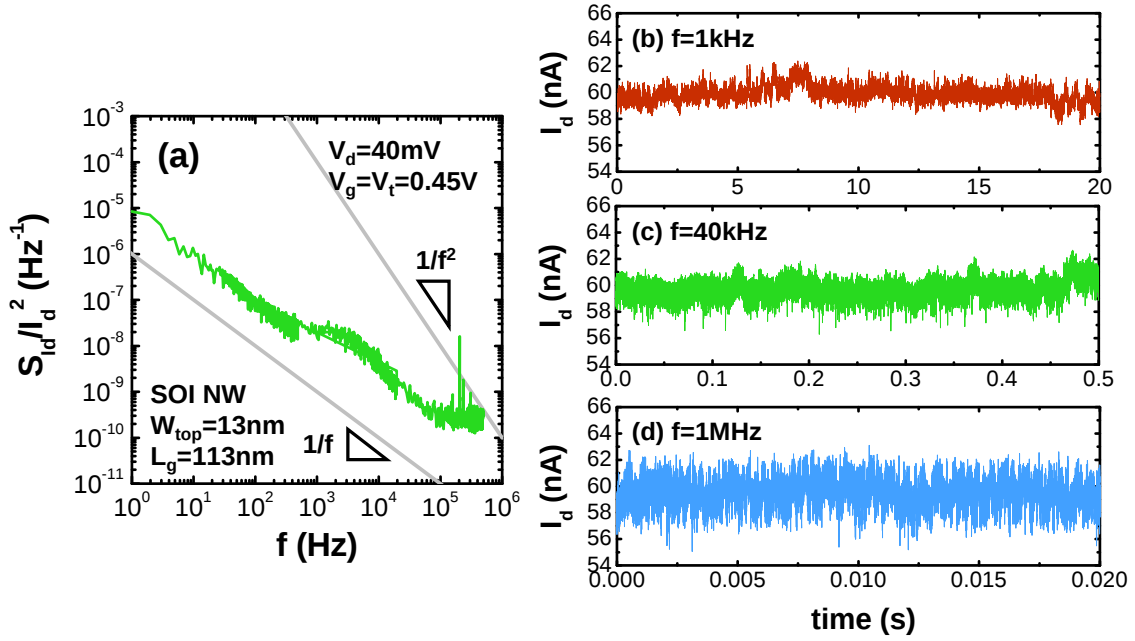


Fig. 5-3. (a) S_{Id}/I_d^2 as a function of frequency in the narrowest SOI Ω -gate NW NMOS FETs with $L_g=113\text{nm}$, showing $1/f$ and additional $1/f^2$ noise components at threshold voltage ($V_g=V_t$). I_d fluctuation as a function of time for sampling frequency of (b) $f=1\text{kHz}$, (c) $f=40\text{kHz}$, and (d) $f=1\text{MHz}$.

On the other hand, I_d fluctuation measurement in time domain for an SOI NMOS NW with short $L_g=28\text{nm}$ exhibiting two large $1/f^2$ noise component (one is at the range of 1Hz - 10Hz , and other appears around 100kHz) is shown in Fig.5-4. A clear RTS is observed at sampling frequency of 1kHz corresponding to the lower frequency region (Fig.5-4b). However, no RTS is observed at sampling frequency of 1MHz , and this means that the $1/f^2$ spectrum at higher frequency region does not correspond to RTS noise (Fig.5-4d). This could be attributed to charge trapping/de-trapping event occurring in the Si body (*i.e.* g-r noise via traps in substrate). The additional $1/f^2$ noise spectra are more visible also in other short channel NWs than longer device cases, as shown in Fig.5-5. However, it is thereby concluded that $1/f$ noise behavior is basically observed and less RTS noise is found in low-frequency region for most of our devices, even for single short channel NWs.

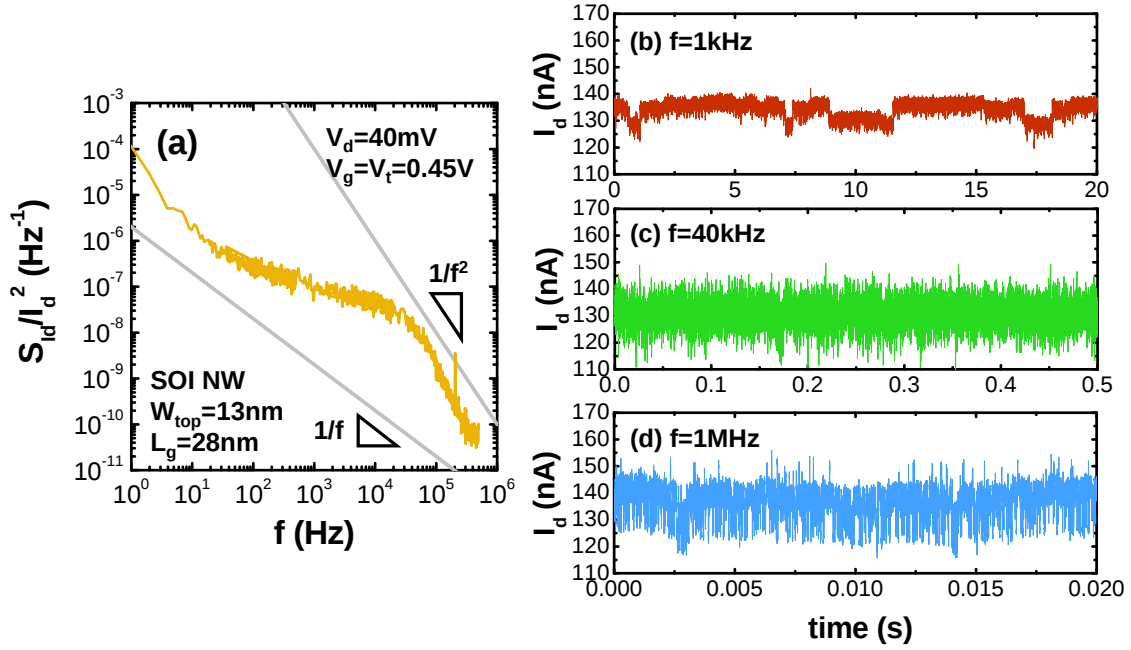


Fig. 5-4. (a) S_{Id}/I_d^2 as a function of frequency in the narrowest SOI Ω -gate NW NMOS FETs with $L_g=28\text{nm}$, showing large $1/f^2$ noise components at threshold voltage ($V_g=V_t$). I_d fluctuation as a function of time for sampling frequency of (b) $f=1\text{kHz}$, (c) $f=40\text{kHz}$, and (d) $f=1\text{MHz}$.

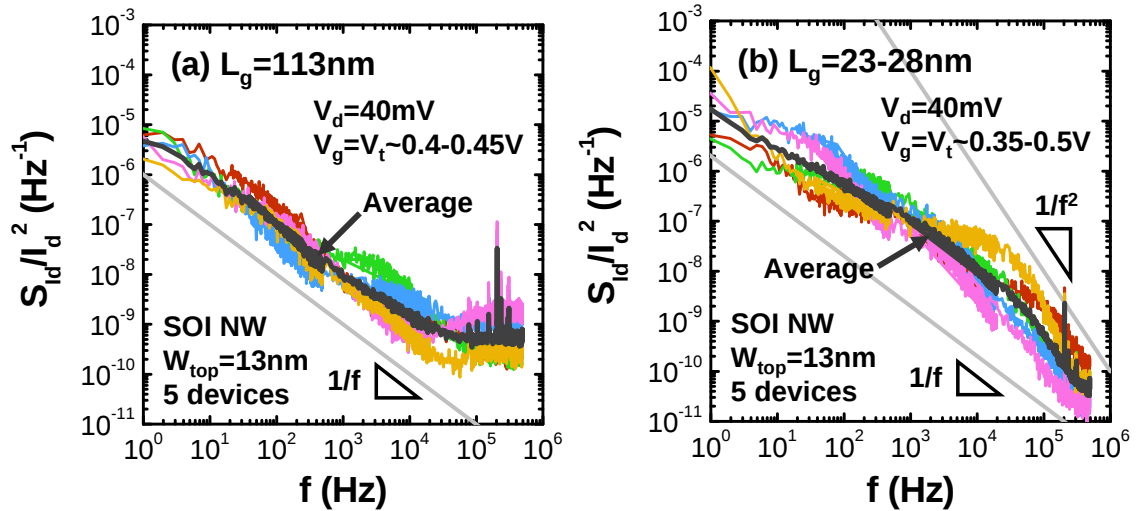


Fig. 5-5. S_{Id}/I_d^2 as a function of frequency in the narrowest SOI Ω -gate NW NMOS FETs with (a) $L_g=113\text{nm}$ and (b) short channel $L_g=23-28\text{nm}$, showing $1/f$ behavior in low-frequency region at threshold voltage ($V_g=V_t$).

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5.1.1 Comparison between experimental data and CNF+CMF model

The measured S_{Id}/I_d^2 extracted at frequency of $f=10\text{Hz}$ as a function of I_d with normalization by the channel area parameters (both W_{tot} and L_g) is shown in Fig.5-6 for a number of NMOS technological splits (channel orientation, H_2 anneal, and strained channel). Actually, good agreement between S_{Id}/I_d^2 plot and the corresponding $(g_m/I_d)^2$ curve is observed in all the devices. This indicates that the LFN properties in all the technological parameters are well described by CNF+CMF model. Furthermore, the almost merged LFN data in Fig.5-6a indicates that there is no significant influence of the orientation differences ([110]- vs. [100]-orientation [5-3], and (001) top surface vs. (110) side-walls in [110]-oriented SOI [5-4,5-5]). The wide FET processed with additional H_2 anneal shows larger noise level in subthreshold region exhibiting plateaued noise level, whereas the noise curve of NW perfectly agrees with the case w/o H_2 anneal (Fig.5-6b). In Fig.5-6c, sSOI devices show slight noise level increase in the entire region for both wide and narrowest NW cases. This can be partly attributed to the I_d enhancement.

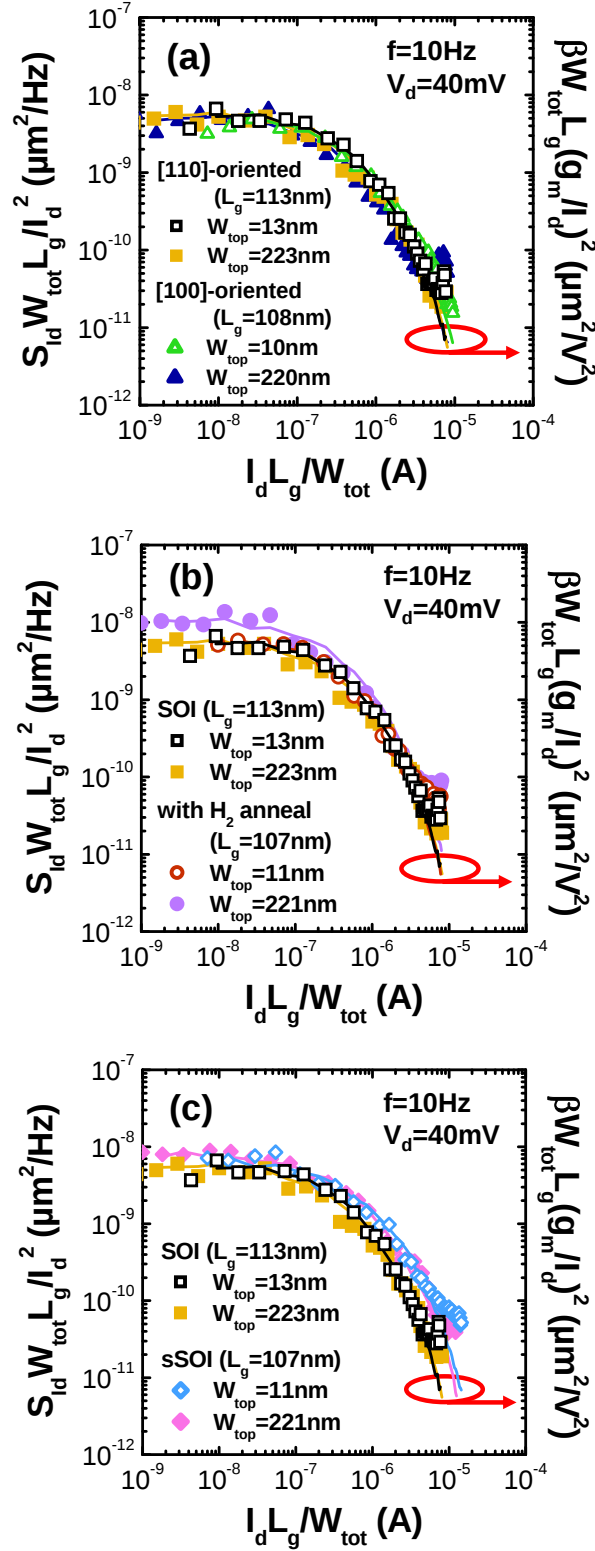


Fig. 5-6. I_d dependent (symbols) S_{id}/I_d^2 and (lines) corresponding $(g_m/I_d)^2$ curve characteristics normalized by channel size parameters (W_{tot} and L_g) in reference SOI wide FETs and the narrowest NWs compared with (a) [100]-oriented SOI, (b) SOI with additional H_2 anneal, and (c) sSOI for NMOS devices.

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Same measurements have been also performed for PMOS (Fig.5-7). Good agreement between noise data and CNF+CMF model is also observed and sustained for reference SOI, SG-S/D, and SGOI devices. In SOI devices for both NW and wide FETs, and in SG-S/D NWs, a large augmentation of the noise level in strong inversion region is observed. This indicates a strong contribution from S/D series resistance R_{SD} [5-6~5-8]. This phenomenon is discussed in detail in the next section. In Fig.5-8, we compare the 3-types of PMOS technological variants. The noise curves in wide FETs are superposed below the strong inversion region, *i.e.* for $I_d \times L_g / W_{tot} < 10^{-6}$ A in Fig.5-8a. On the other hand, the noise curve related to SGOI NWs exhibit a large shift due to huge I_d (I_{ON}) improvement in the narrowest NWs, whereas the plots corresponding to SOI and SG-S/D devices are roughly merged (Fig.5-8b). In both wide and NW FETs, the plateaued noise level in subthreshold region is maintained.

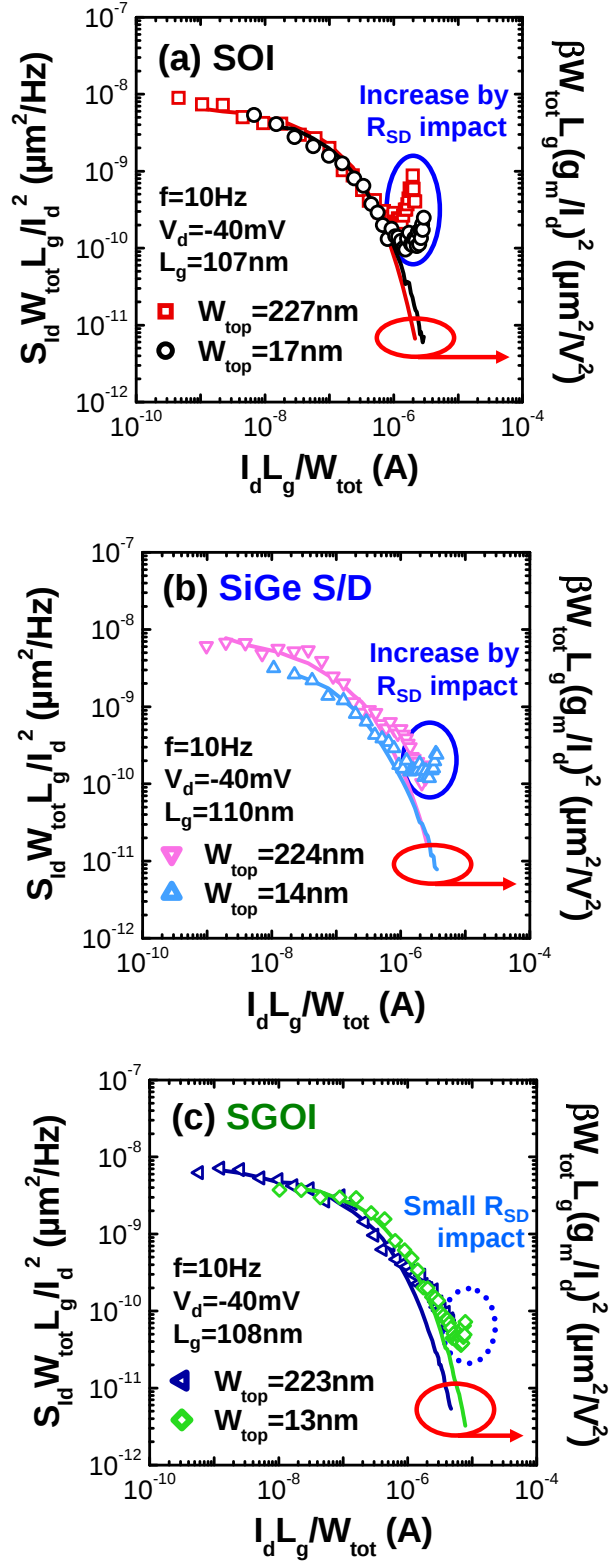


Fig. 5-7. I_d dependent (symbols) S_{id}/I_d^2 and (lines) corresponding $(g_m/I_d)^2$ curve characteristics normalized by channel size parameters (W_{tot} and L_g) in wide FETs and the narrowest NWs for (a) SOI, (b) SG-S/D, and (c) SGOI for PMOS devices.

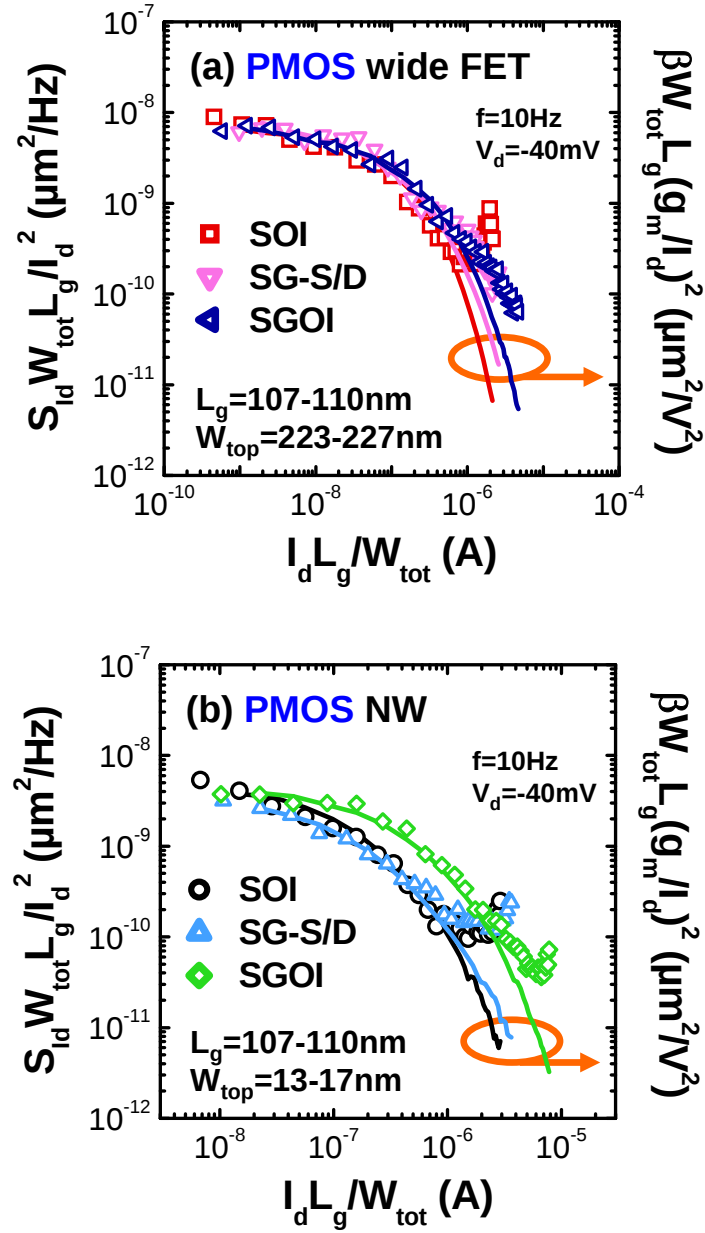


Fig. 5-8. Comparison of 3-types of PMOS device variants; SOI, SG-S/D, and SGOI, in I_d dependent (symbols) S_{Id}/I_d^2 and (lines) corresponding $(g_m/I_d)^2$ curve characteristics normalized by W_{tot} and L_g for (a) wide FETs and (b) the narrowest NWs.

It can be noticed that the noise level decrease due to the volume inversion, reported in SOI tri-gate NW FETs with $\text{SiO}_2/\text{poly-Si}$ gate stack [5-5], and in GAA Si NW FETs with *in-situ* steam-generated (ISSG) SiO_2/TiN gate stack [5-9], is not observed in our

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case. In our SOI-based Ω -gate NWs, the scaling regularity with both W_{tot} and L_g , without much quantum effect, could be attributed to the use of Hf-based high- κ gate oxide (HfSiON) and the carrier transport occurring mainly in 2D surfaces of top and side-walls even in NW geometry.

5.1.2 Impact of 1/f noise stemming from source/drain regions

Here, the R_{SD} contribution to 1/f LFN properties is discussed. A large increment of the noise level in strong inversion region, shown in Fig.5-7a and b, stems from the strong contribution of S/D access regions. The R_{SD} is additively fluctuating by trapping/de-trapping events of carriers caused via defects in the spacers 1 and 2 consisting of SiN_x and/or in the silicon film, as illustrated in Fig.5-9. The fluctuations contribute to the rise of 1/f noise level in strong inversion regime, and are distinct from thermal noise which is frequency independent. Worse quality of the S/D regions in PMOS devices than NMOS is generally attributed to less controllability of the boron dopant due to the lighter mass of B than P or Ar. This could explain the higher contribution of R_{SD} to noise observed for PMOS than for NMOS. The definition of CNF+CMF model (cf. Eq. (1-53)) can be simply completed by considering the additional noise impact caused by the S/D regions as [5-6]:

$$\frac{S_{I_d}}{I_d^2} = \left(\frac{g_m}{I_d} \right)^2 \left(1 + \alpha_{sc} \mu_{\text{eff}} C_{\text{ox}} \frac{I_d}{g_m} \right)^2 S_{V_{fb}} + \left(\frac{I_d}{V_d} \right)^2 S_{R_{sd}} \quad (5-1)$$

where $S_{R_{sd}}$ is the PSD of the R_{SD} fluctuations.

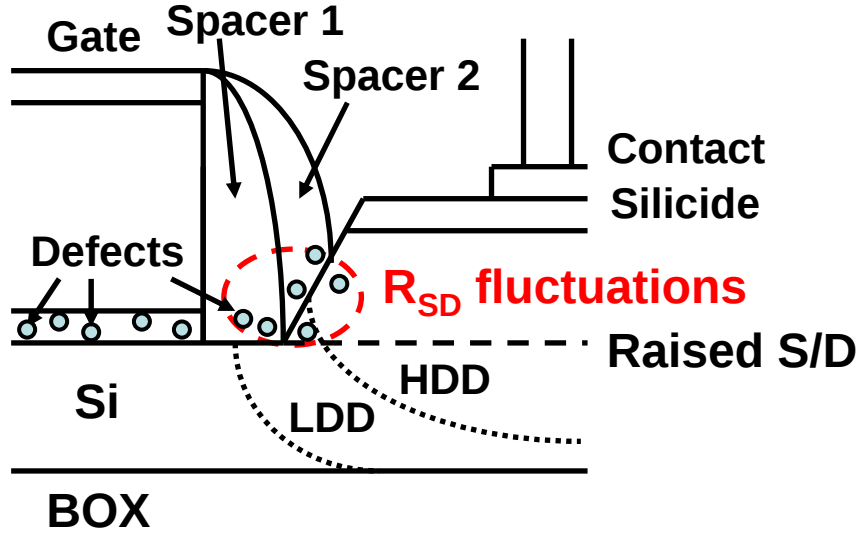


Fig. 5-9. Schematic of defects in spacers 1 and 2 and/or in Si film contributing to R_{SD} fluctuations in SOI MOSFET architecture.

In Fig.5-10, experimental $S_{Id}/I_d^2-I_d$ plots are shown together with the theoretical expression Eq. (5-1) using two fitting parameters β and S_{Rsd} . The experimental curves above V_t for SOI devices can be perfectly described by the included R_{SD} impact (Fig.5-10a). For both SG-S/D and SGOI devices, the spectra in NWs are well interpreted by considering both $\alpha_{sc}\mu_{eff}$ and S_{Rsd} components (Fig.5-10b), whereas for wide FETs, the $\alpha_{sc}\mu_{eff}$ factor is only dominant without the S_{Rsd} term (Fig.5-10c). The values of S_{Rsd} are summarized in Table 5-1. They highlight the advantage of SGOI device which exhibits much lower impact of R_{SD} , in relation with a lower R_{SD} value by Y-function method (cf. Fig.4-29).

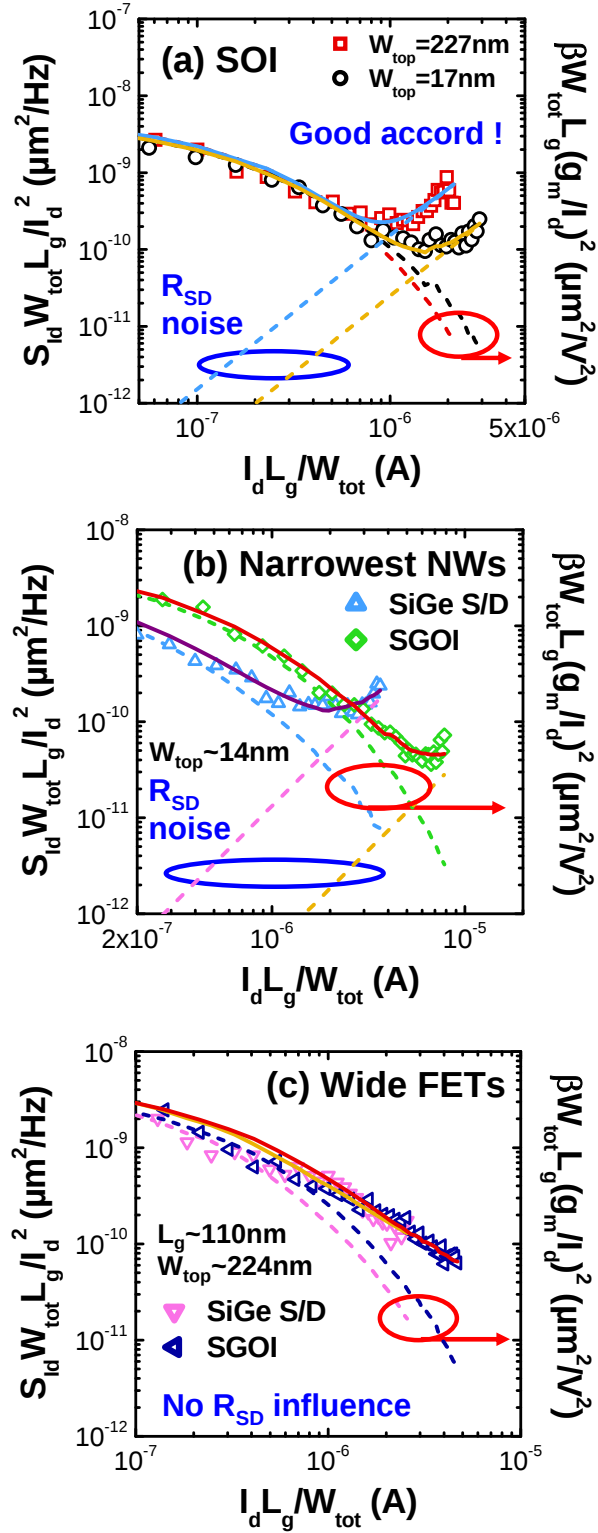


Fig. 5-10. I_d dependent (symbols) S_{Id}/I_d^2 and (lines) corresponding $(g_m/I_d)^2$ curves with consideration of the $\alpha_{\text{sc}}\mu_{\text{eff}}$ and S_{Rsd} term shown in Eq. (5-1), showing (a) the narrowest NW vs. wide FETs in SOI devices, and SiGe S/D vs. SGOI devices in (b) NWs, and in (c) wide FETs.

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Table 5-1. Summary of the extracted $\alpha_{sc}\mu_{eff}$ and S_{Rsd} values in Fig.5-10 with the extracted S/D series resistance R_{SD} normalized by W_{tot} for NWs in Fig.4-29.

[110]-oriented Ω -gate PMOS	$\alpha_{sc}\mu_{eff} (\times 10^6 \text{ cm}^2/\text{C})$		$S_{Rsd} (\Omega^2/\text{Hz})$		$R_{SD} (\Omega \mu\text{m})$
	Wide	NW	Wide	NW	NW
SOI	No impact	No impact	1.6	50	208
SG-S/D	1.5	1.1	No impact	65	210
SGOI	1.4	0.75	No impact	1.7	158

We have also extracted the Hooge parameter α_H (cf. Eq. (1-37) and (1-38)), which is based on an empirical model considering only mobility fluctuations. In fact, Hooge's empirical model has no theoretical argument, even though it has been often able to explain the $1/f$ noise behavior. Meanwhile, the Hooge parameter α_H has been often reported to discuss the noise behavior difference for technological and structural parameters in overdrive operation. The values of α_H extracted in our NW FETs are shown in Fig.5-11 as a function of the voltage overdrive V_{gt} . Different trends depending on the technological splits can be distinguished.

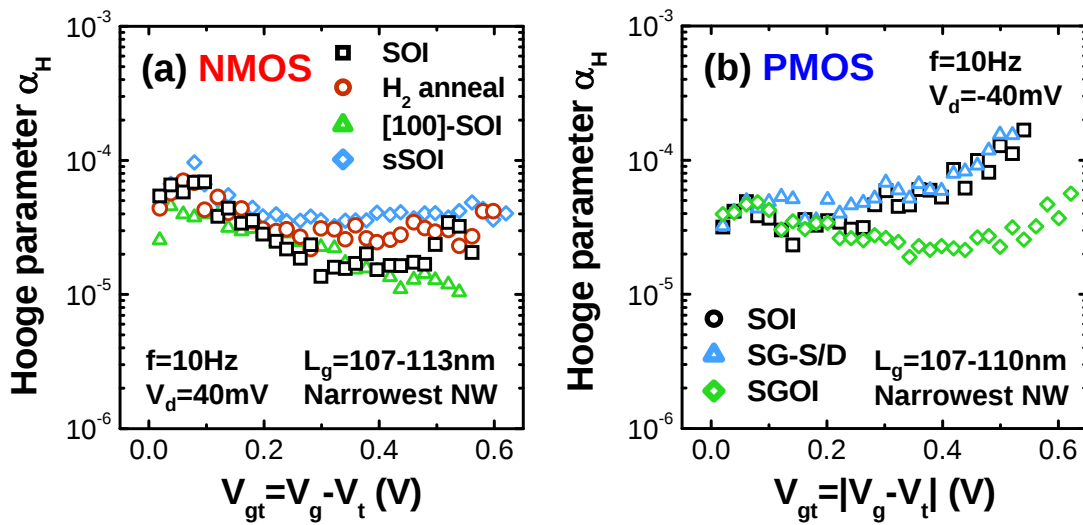


Fig. 5-11. Hooge parameter α_H as a function of gate voltage overdrive V_{gt} for various technological splits in the narrowest (a) NMOS and (b) PMOS NW FETs.

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For NMOS, higher values of α_H is observed in SOI NW with additional H₂ anneal process and in sSOI NW, compared to reference SOI NW especially for V_{gt} above 0.2V. It is ascribed to the relatively large influence of CMF component (values of $\alpha_{sc}\mu_{eff}$). On the other hand, [100]-oriented NW exhibits similar or lower values than reference [110]-NW in almost entire V_{gt} range, suggesting no large impact of side-wall orientation. In $V_{gt}>0.5V$ region, it should be noticed that α_H level of reference SOI NW rises and reaches the levels in H₂ annealed SOI and sSOI NWs. This can be attributed to the effect of R_{SD} fluctuations.

For PMOS, level of α_H is equal among the three technological splits in V_{gt} region below 0.2V. Above 0.2V, reference SOI and SG-S/D NWs show the higher value and steeper upward trend compared to SGOI device. Lower noise level for SGOI NW in strong inversion region is here reconfirmed. The large increase tendency in SOI and SG-S/D NWs is attributed to strong R_{SD} noise contribution as discussed in last chapter.

We conclude that Hooge's empirical parameter α_H well reflects $\alpha_{sc}\mu_{eff}$ and S_{Rsd} impacts in strong inversion region, even though the noise behaviors are in accordance with CNF+CMF model, not only MF. Moreover, it is visibly concluded that the S_{Rsd} influence in PMOS is much stronger than NMOS devices, and SGOI technology is advantageous for PMOS NW FETs.

5.1.3 Flat-band voltage noise

5.1.3.1 Extraction

For more detailed investigations, two important parameters S_{Vfb} and $\alpha_{sc}\mu_{eff}$ in Eq. (1-53) can be obtained from experimental data. Both parameters are simultaneously extracted from experimental $S_{Vg}^{1/2}$ plot as a function of I_d/g_m as:

$$S_{Vg}^{1/2} = \sqrt{\frac{S_{Id}}{g_m^2}} = \left(1 + \alpha_{sc}\mu_{eff} C_{ox} \frac{I_d}{g_m} \right) S_{Vfb}^{1/2} \quad (5-2)$$

Figure 5-12 shows $S_{Vg}^{1/2}$ versus I_d/g_m characteristics with varying V_g from weak to strong inversion regions for SOI TGNW devices. The two parameters, namely $S_{Vfb}^{1/2}$ and $S_{Vfb}^{1/2}\alpha_{sc}\mu_{eff}C_{ox}$ are provided by the intercept with the vertical axis and the slope, respectively [5-10]. The straight line indicates the linear regression calculated for

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reference wide and 1ch-TGNW FETs. However, lower S_{Vfb} values than the actual values are extracted by the linear regression method for 1ch-NWs, whereas no mismatch is seen in reference wide FETs.

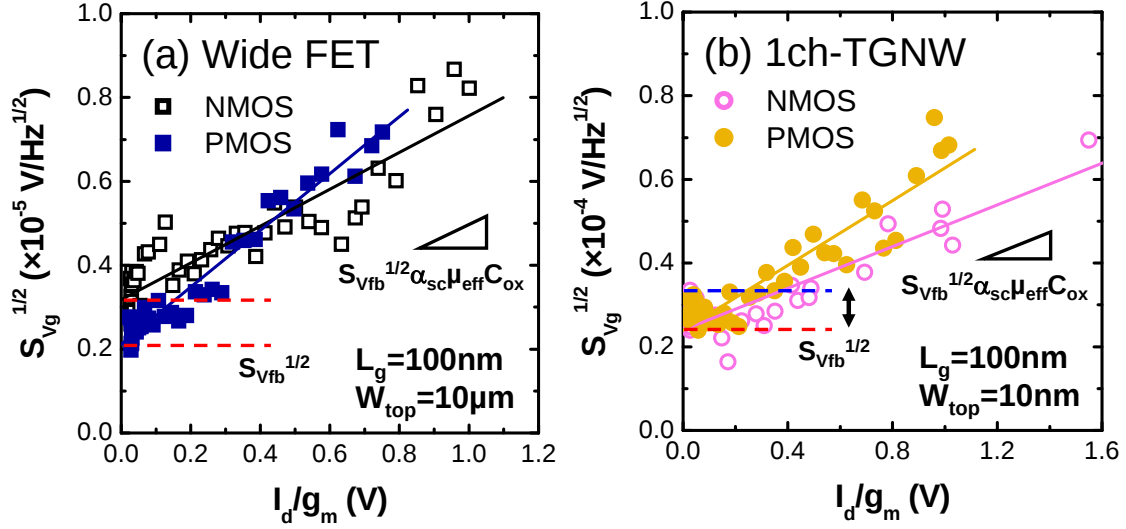


Fig. 5-12. (Symbols) $S_{Vg}^{1/2}$ versus I_d/g_m characteristics and (lines) the linear regression for extraction of S_{Vfb} and $\alpha_{sc}\mu_{eff}$ in (a) wide and (b) 1ch-TGNW both N- and PMOS FETs.

S_{Vfb} value can also be extracted by direct fitting of S_{Id}/I_d^2 versus $(g_m/I_d)^2$ curves, in the subthreshold region showing the plateaued noise level (cf. Figs.5-6~5-8). In this regime where CNF is predominant, the coefficient $(1+\alpha_{sc}\mu_{eff}C_{ox}I_d/g_m)$ in Eq. (1-53) reduces to 1. The proportionality constants β used in Figs.5-6~5-8 and 5-10 thereby corresponds to the value of S_{Vfb} in the plateau region, where CNF noise can be approximated as:

$$\frac{S_{Id}}{I_d^2} \approx \beta \left(\frac{g_m}{I_d} \right)^2 \approx S_{Vfb} \left(\frac{g_m}{I_d} \right)^2 \quad (5-3)$$

This method seems more relevant for NW devices with less mismatched values compared to those obtained by the linear regression method.

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5.1.3.2 Influence of scalability

Extracted flat-band voltage noise $S_{V_{fb}}$ in Fig.5-13 shows roughly simple channel scaling effect, *i.e.* the noise level increases as the inverse of both W_{tot} [5-11] and L_g decreasing, without any large deviation from the different technological parameters for NMOS devices. This result well agrees with predicted LFN scaling rule [5-1] (cf. Eq. (1-55)) and S_{Id} studies in published reports [5-8,5-12~5-17].

For PMOS, cSGOI devices in the narrowest NW region exhibit relatively higher noise level than other splits as shown in Fig.5-14a. From Fig.5-14b, we also evidenced that the narrowest PMOS NWs exhibit different noise levels depending on the technological splits, whereas wide FETs have the same level whatever splits. In particular, SiGe channel NWs (SGOI & cSGOI) show slightly higher noise than Si channels. For the other technological splits within reasonable uncertainty, we conclude that $S_{V_{fb}}$ in PMOS devices exhibits the simple scaling effect and the unity among the technological parameters in analogy with the NMOS case.

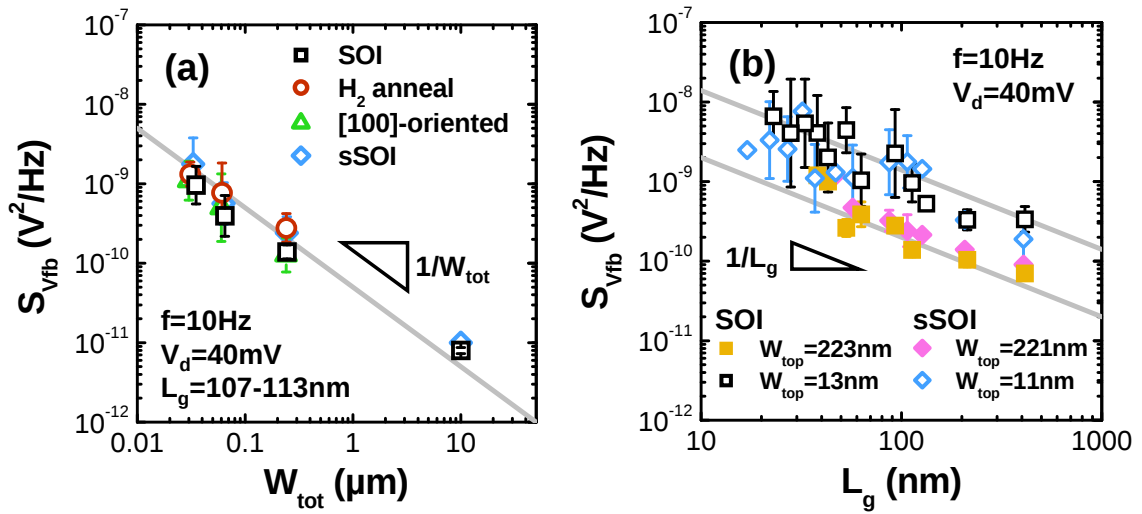


Fig. 5-13. Flat-band voltage noise $S_{V_{fb}}$ as a function of (a) W_{tot} and (b) L_g for all the technological splits in NMOS devices.

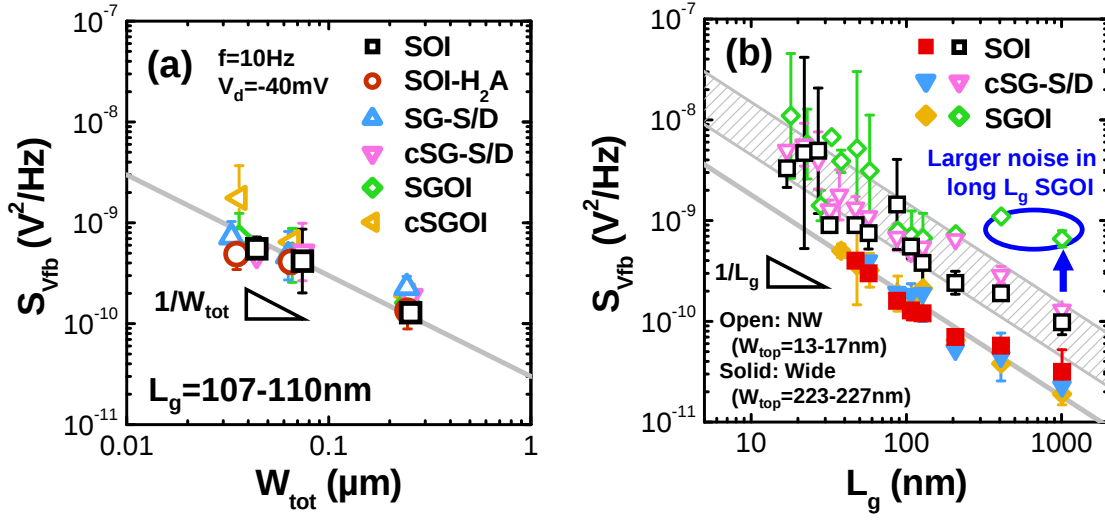


Fig. 5-14. Flat-band voltage noise $S_{V_{fb}}$ as a function of (a) W_{tot} and (b) L_g for all the technological parameters in PMOS devices.

5.1.4 Coulomb scattering parameter

5.1.4.1 General feature

The linear relationship between $S_{V_g}^{1/2}$ and I_d/g_m shown in Fig.5-12 suggests that the Coulomb scattering parameter $\alpha_{sc}\mu_{eff}$ is constant from weak to strong inversion regions in agreement with previous works [5-10,5-11], and that this relationship is applicable even in ultra-scaled TGNW devices. The values of $\alpha_{sc}\mu_{eff}$ -corresponding to CMF factor- as a function of the device channel area $W_{tot}L_g$ is extracted in Fig.5-15. It is found that the parameter is not altered by scaling effect (W_{top} or L_g downscaling) for both N- and PMOS devices within measurement uncertainty. We conclude that the device-to-device dispersion is only dominant for CMF. Finally, the values of $\alpha_{sc}\mu_{eff}$ roughly agree with previously reported data ($\alpha_{sc}\mu_{eff} \sim 2.5 \times 10^5 - 2 \times 10^6 cm^2/C$) [5-10,5-18].

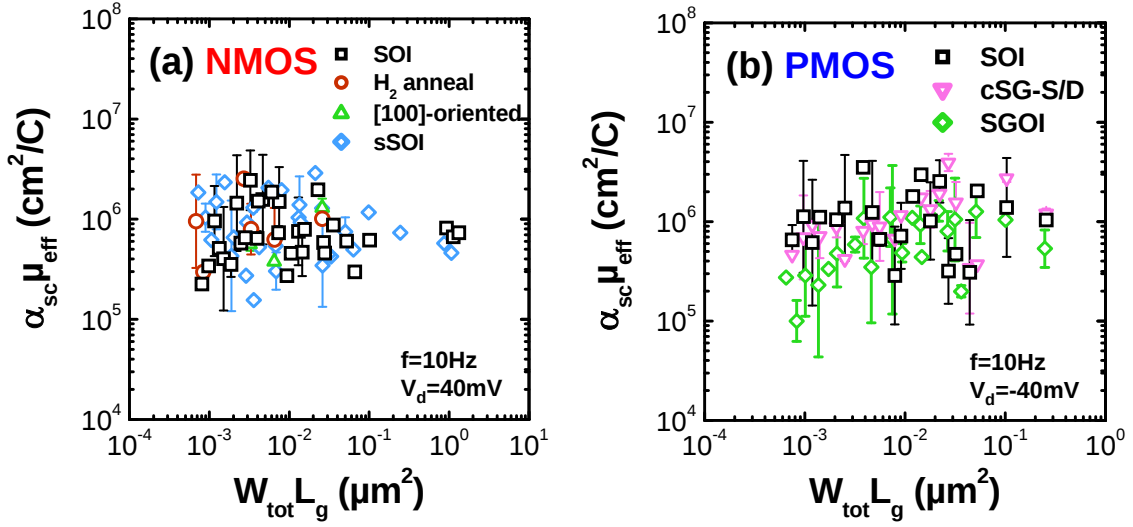


Fig. 5-15. Coulomb scattering parameter $\alpha_{sc}\mu_{eff}$ as a function of the channel area $W_{tot}L_g$ in all the devices with single-channel for (a) NMOS and (b) PMOS FETs.

5.1.4.2 Comparison with transport parameter: low-field mobility

The extracted $\alpha_{sc}\mu_{eff}$ from LFN study is compared with extracted μ_0 by the Y-function method (cf. Section.4.3.1) in the narrowest NW devices. Figure 5-16 shows $\alpha_{sc}\mu_{eff}$ as a function of μ_0 for reference SOI and strained NW devices (sSOI for NMOS, cSG-S/D and SGOI for PMOS, respectively). For NMOS, it could be seen that SOI NWs with lower mobility ($\mu_0 < 150 \text{ cm}^2/\text{Vs}$) exhibit relatively lower values of the $\alpha_{sc}\mu_{eff}$ ($\approx 2 \times 10^5 - 10^6 \text{ cm}^2/\text{C}$) and higher mobility ($\mu_0 > 150 \text{ cm}^2/\text{Vs}$) corresponds to the higher values ($\approx 4 \times 10^5 - 3 \times 10^6 \text{ cm}^2/\text{C}$). However, the difference of $\alpha_{sc}\mu_{eff}$ range is small. Moreover, sSOI NWs show the opposite trend; devices with lower $\mu_0 < 200 \text{ cm}^2/\text{Vs}$ exhibit relatively higher values of the $\alpha_{sc}\mu_{eff}$ ($\approx 6 \times 10^5 - 2 \times 10^6 \text{ cm}^2/\text{C}$), and higher $\mu_0 > 200 \text{ cm}^2/\text{Vs}$ corresponds to the lower values ($\approx 2.5 \times 10^5 - 1.5 \times 10^6 \text{ cm}^2/\text{C}$). For PMOS, SOI and cSG-S/D NWs show roughly no tendency. The $\alpha_{sc}\mu_{eff}$ range is $\approx 3.1 \times 10^5 - 3.5 \times 10^6 \text{ cm}^2/\text{C}$ for SOI, and is $\approx 3.4 \times 10^5 - 1.3 \times 10^6 \text{ cm}^2/\text{C}$ for cSG-S/D NWs, respectively. It could be seen that SGOI NWs have the $\alpha_{sc}\mu_{eff}$ values ($\approx 1 \times 10^5 - 6.6 \times 10^5 \text{ cm}^2/\text{C}$) decreasing with the lower μ_0 .

It is concluded that $\alpha_{sc}\mu_{eff}$ does not clearly correlate to the mobility behavior in

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inversion region and the magnitude extracted at low-field regime regardless of the mobility enhancement induced by strain for both N- and PMOS NW FETs.

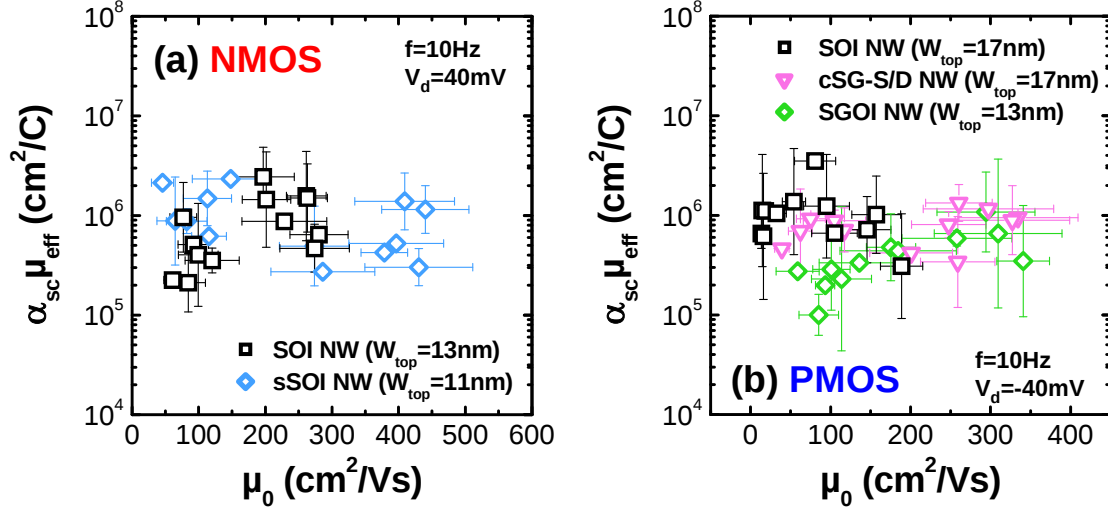


Fig. 5-16. Coulomb scattering parameter $\alpha_{sc} \mu_{eff}$ as a function of low-field mobility μ_0 extracted in Figs.4-26b and 4-27d for the narrowest NW (a) NMOS and (b) PMOS FETs.

5.2 Oxide trap density

5.2.1 General tendency

The gate oxide trap density N_t ($\text{eV}^{-1}\text{cm}^{-3}$) around quasi-Fermi energy level within $4kT$ range can be written from Eq. (1-48) as:

$$N_t = \frac{f W_{tot} L_g C_{ox}^2 S_{Vfb}}{q^2 k T \lambda} \quad (5-4)$$

The tunneling attenuation length λ is estimated as $\approx 0.1\text{nm}$ for electron and $\approx 0.14\text{nm}$ for hole in the Si/HfO₂ system with SiO₂ interfacial layer (IL) [5-19~5-22]. The trap density N_t calculated from S_{Vfb} data (Figs.5-13 and 5-14) is shown and discussed here.

Figure 5-17 shows N_t as a function of W_{tot} and L_g in NMOS FETs with $L_g \approx 110\text{nm}$. Again, slightly higher N_t is measured in SOI with H₂ anneal and sSOI as compared with

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reference SOI (nearly twice higher) (Fig.5-17a). This result is in agreement with a previous work reporting higher interface trap density D_{it} for additional H_2 anneal in 3D-stacked Si NW FETs [5-23]. However, N_t in both SOI and sSOI MOSFETs as a function of L_g is distributed within one decade (10^{17} to 10^{18} eV⁻¹cm⁻³) due to device-to-device dispersion, especially in the narrowest NWs (Fig.5-17b). Some sSOI NWs thus have similar or lower N_t as compared to SOI NWs. Published LFN studies on sSi MOSFETs fabricated from SiGe virtual layers have reported lower [5-24~5-26], constant [5-1], or higher [5-27~5-30] trap density compared to reference Si devices. References [5-27~5-30] suggest that diffusion of Ge atoms from the SiGe layers into the Si channel and the gate oxide as well as the threading dislocations can severely degrade the gate oxide/channel interface quality (D_{it} increase has been also reported in correlation [5-31]). Therefore, extrinsic process parameters associated with sSOI substrate preparation, such as the SiGe and sSi epitaxial growth, selective etching of the SiGe, and the reliability (*i.e.* device-to-device dispersion), could dominate compared with intrinsic tensile strain impact on the gate oxide/channel interface quality.

For PMOS, the cSGOI NW shows slightly larger N_t value than the other devices in Fig.5-18a. In Fig.5-18b it can be seen that SGOI NWs with longer $L_g < 400$ nm have relatively higher N_t . However, the influence of the compressively strained SiGe channel is not large in magnitude, while very high D_{it} [5-32~5-34] and N_t [5-35,5-36] were found in previous NW studies due to Ge content.

In literature, some work have reported N_t increase due to SiGe S/D process in FETs with HfO_2 gate oxide [5-25,5-37,5-38], and a slight increase of the noise level and D_{it} in FETs with SiO_2 or nitrided oxide [5-39~5-41]. Fortunately, it has been reported that replacing HfO_2 by $HfSiON$ provides steady noise level with the reference Si S/D device owing to a better robustness against the thermal budget of the SiGe S/D process [5-42]. Our SiGe S/D devices show no large deviation of N_t values from reference SOI devices regardless of the compressive CESL effect. This could be ascribed to the use of $HfSiON/TiN$ gate stack. It could be also attributed to an optimized technological process. As a result, the device-to-device dispersion is only dominant similarly to the NMOS case.

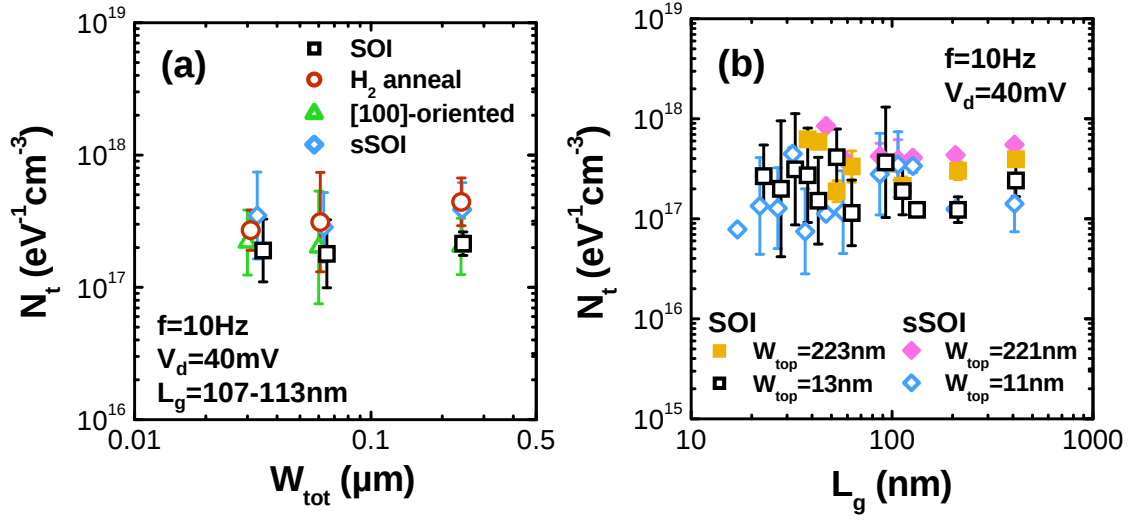


Fig. 5-17. Oxide trap density N_t as a function of (a) W_{tot} and (b) L_g for all the technological splits in NMOS devices.

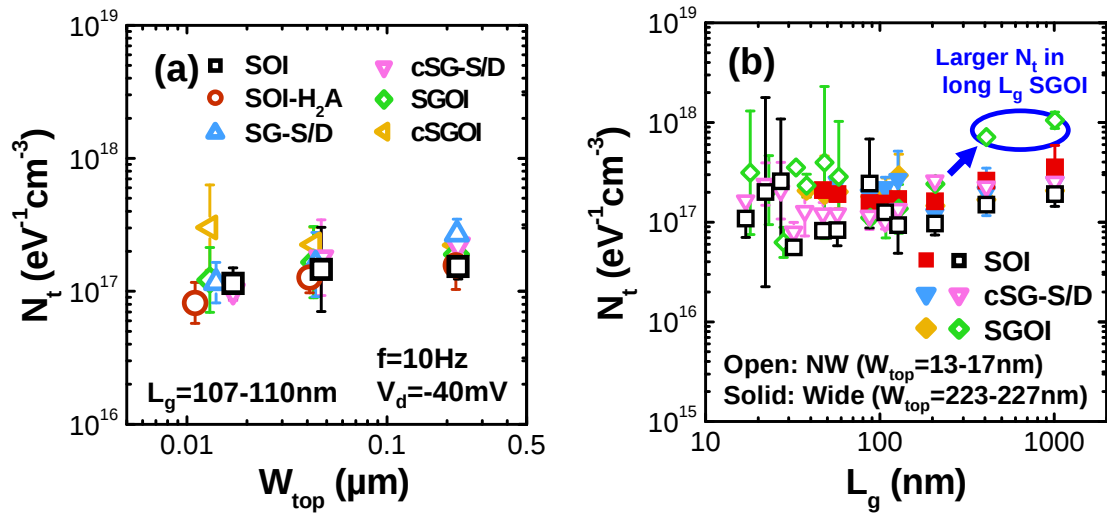


Fig. 5-18. Oxide trap density N_t as a function of (a) W_{top} and (b) L_g for all the technological parameters in PMOS devices.

Our most important conclusion is that the mean N_t values for all the devices lie in roughly similar order ($\approx 5 \times 10^{16}$ - $10^{18} \text{eV}^{-1}\text{cm}^{-3}$) as the values recently reported for state-of-the-art Hf-based high- κ /metal gate technology ($N_t \sim 10^{17}$ - $10^{19} \text{eV}^{-1}\text{cm}^{-3}$) [5-10,

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5-14,5-15,5-21,5-43,5-44]. The N_t values averaged over all L_g in NW and wide FETs are shown in Fig.5-19. Data from reference SOI and strained devices (sSOI for NMOS, cSG-S/D and SGOI for PMOS, respectively) are compared. NWs exhibit somewhat lower values in most of the devices (except SGOI with $2.0 \times 10^{17} \text{ eV}^{-1} \text{ cm}^{-3}$ for both wide and NW FETs). This clearly indicates that the N_t values are not altered by the scaling effect of W_{top} , *i.e.* by the 2D or 3D architectural impact [5-45,5-46]. As a consequence, it is concluded that the excellent oxide/interface quality is achieved and maintained in all our N- and PMOS devices, especially in NWs with side-wall surfaces which play an increasing role as W_{top} is scaled down.

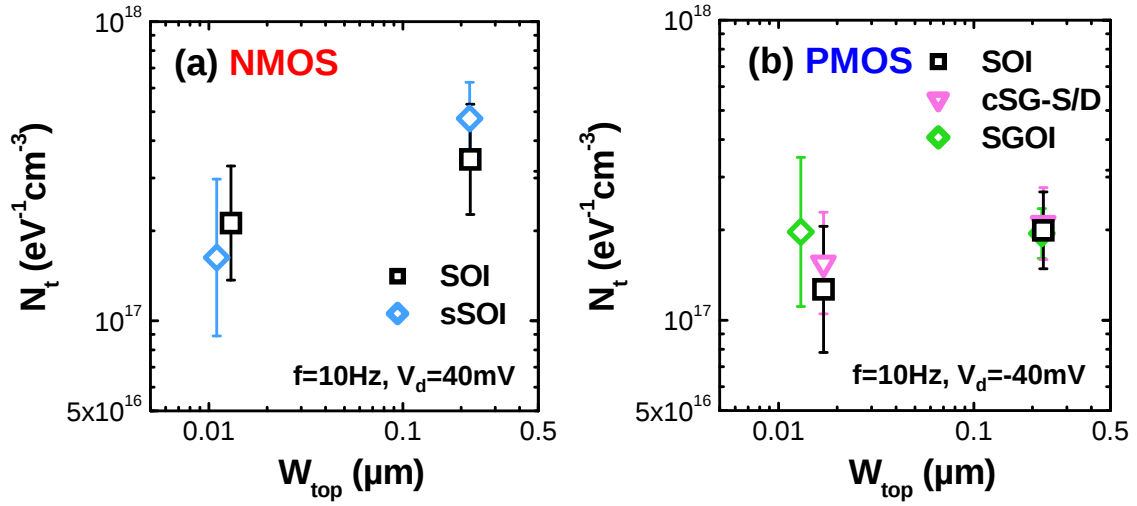


Fig. 5-19. N_t averaged over all L_g in wide and NW FETs for (a) NMOS and (b) PMOS devices, with comparison between SOI and sSOI for NMOS, and among SOI, cSG-S/D, and SGOI for PMOS.

5.2.2 Assessment of the contributions of the different surface orientations

For more rigorous assessment of the interface quality, a separation method of the N_t contribution between top surface (N_{t_top}) and side-walls ($N_{t_side-wall}$) could be introduced as follows:

$$N_{t_tot} = \frac{W_{top}}{W_{tot}} N_{t_top} + \frac{2H_{NW}}{W_{tot}} N_{t_side-wall} \quad (5-5)$$

In this work, the relation of the N_t contributions in Eq. (5-5) can be approximated as

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$N_{t_tot} \approx 1/3 N_{t_top} + 2/3 N_{t_side-wall}$ for all the narrowest NW FETs. Using this simple formula, we have extracted N_{t_top} and $N_{t_side-wall}$ for three different width W_{top} ($L_g \approx 110\text{nm}$) as shown in [Figs.5-20 and 5-21](#).

For NMOS, the (100) plane, which corresponds to surface orientation of the top surface of reference [110]-oriented SOI, and to the orientation of both the top and side-walls of [100]-oriented SOI (cf. [Fig.2-12](#)), show very similar values $\sim 2 \times 10^{17} \text{eV}^{-1} \text{cm}^{-3}$. This agreement in (100) planes therefore confirms the reliability of the separating method. Surprisingly, the (110) plane in side-walls of [110]-oriented NW leads to slightly lower N_{t_top} values than the (100) top surface. In the devices performed with additional H_2 anneal, the (100) top surfaces degrades, whereas the quality of (110) side-walls is improved. Tensile strain relatively deteriorates both the top and side-wall surfaces compared to reference SOI devices.

For PMOS, the (110) planes in side-walls also show improved N_t values compared to the (100) planes (except in cSGOI devices). This could indicate that CESL process affects the side-wall quality, and that process optimization is needed. Strain process technologies otherwise (SiGe channel material or SiGe S/D) and additional H_2 anneal degrade somewhat the quality of (100) top surfaces, whereas the quality of (110) side-walls is enhanced. It is further noticed that the H_2 anneal process is less harmful in PMOS than in NMOS case.

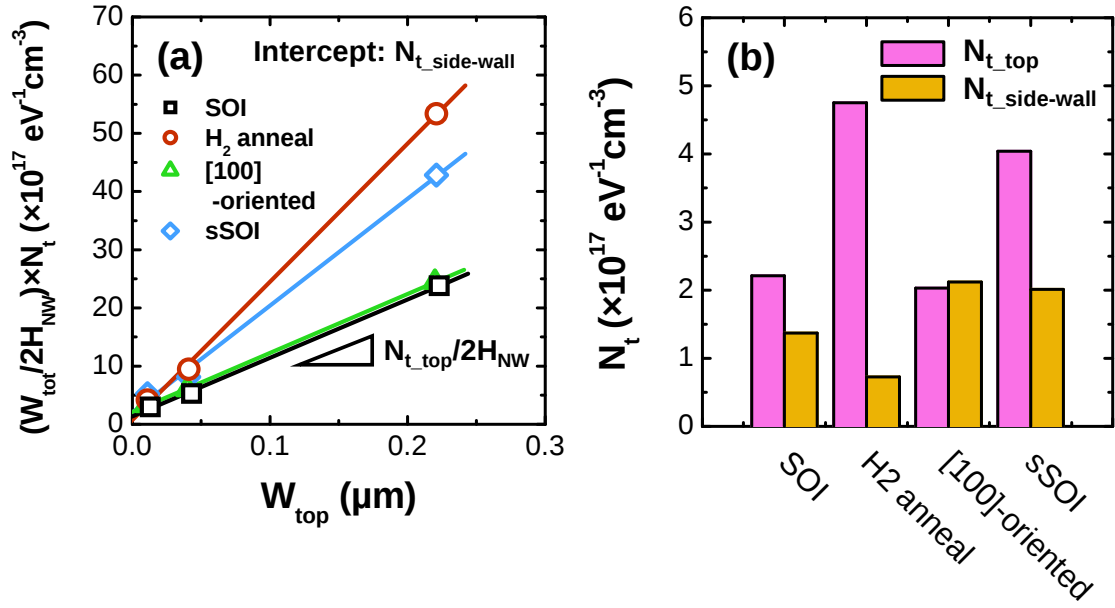


Fig. 5-20. (a) Demonstration of the extraction and (b) the extracted N_t contribution of top surface and side-walls by the N_t separation method for all the NMOS devices.

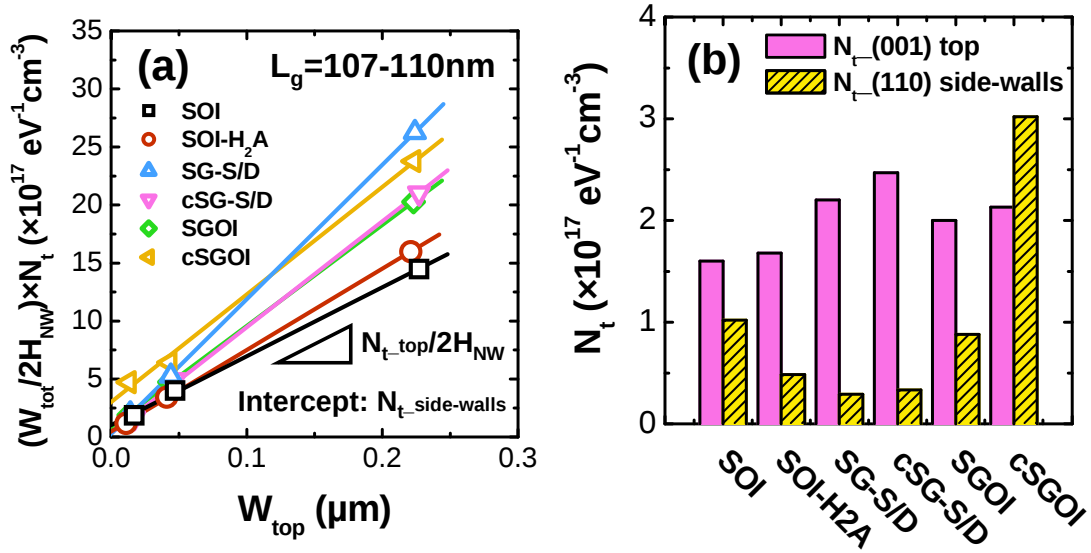


Fig. 5-21. (a) Demonstration of the extraction and (b) the extracted N_t contribution of top surface and side-walls by the N_t separation method for all the PMOS devices.

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5.2.3 Interface quality comparison with charge pumping measurement

Oxide/channel interface quality evaluated by LFN measurement has been compared with charge pumping (CP) measurement [5-47,5-48]. To perform CP measurement on FD-SOI devices, gated diode structures with N^+ and P^+ contacts (P-i-N gated diode) are needed [5-49,5-50], as illustrated in Fig.5-22. In the CP technique, a trapezoidal voltage pulse is applied to the gate with a varying base level V_{base} and a constant amplitude ΔV_g greater than the band gap energy of Si $\Delta E_{g_Si}=1.12\text{eV}$ (here, $\Delta V_g=1.3\text{eV}$ is fixed). This pulse causes a recombination current flowing in the N^+ and P^+ regions by capture/release process of electrons and holes at the interface states. The maximum CP current I_{CP} can be expressed by:

$$I_{CP} = qf_p W_{tot} L_g \overline{D_{it}(E)} \Delta E \quad (5-6)$$

where f_p is the frequency of the pulsed signal, and $\overline{D_{it}(E)}$ is the mean D_{it} over the Si band gap, and ΔE is the swept energy range ($\approx 1\text{eV}$). Note that the mean D_{it} extracted by CP technique takes into account the traps distributed over the Si band gap, and is thus distinct from N_t evaluated from LFN characterization which gives a value at $E_F \pm 2kT$.

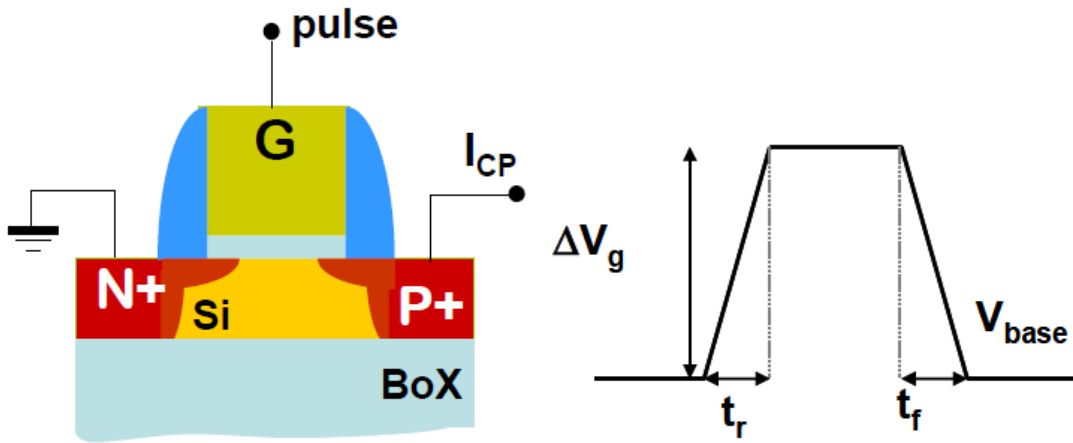


Fig. 5-22. Schematics of the experimental set-up used for charge pumping spectroscopy. A trapezoidal pulse (amplitude ΔV_g , rise and fall time t_r, t_f), with constant amplitude and varying base level V_{base} , is applied to the gate and I_{CP} is measured on the P^+ contact [5-50].

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Figure 5-23 shows the extracted mean D_{it} in [110]-oriented SOI devices with $H_{NW}=11\text{nm}$ and $L_g=0.5\mu\text{m}$. Wide device with $W_{top}=2\mu\text{m}$ and multiple channel Ω -gate NWs with 75 fingers varying the W_{top} from 75nm down to 40nm have been measured. All devices exhibit mean D_{it} in the $1\text{-}3\times 10^{10}\text{eV}^{-1}\text{cm}^{-2}$ range. The NWs exhibit slightly lower D_{it} compared to wide devices in agreement with our results using LFN. This corroborates our conclusions that lower trap density is present in (110) side-walls compared with (100) top surface in most of our MOSFETs.

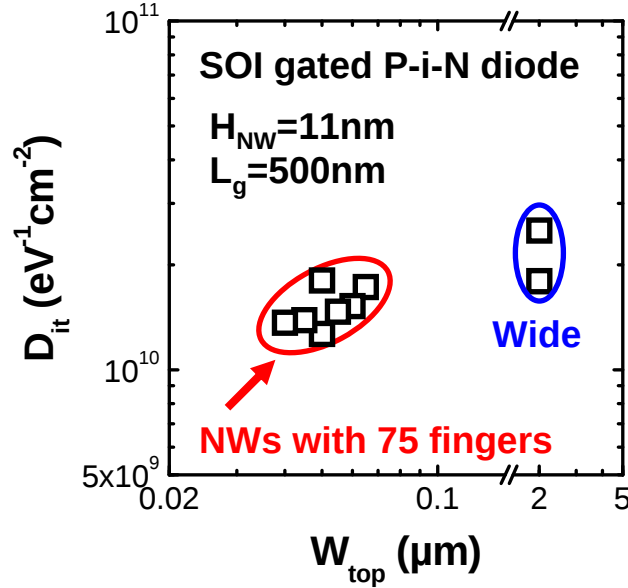


Fig. 5-23. Mean D_{it} obtained by CP measurement as a function of W_{top} in wide gated P-i-N diode and 75-multiple channel NW devices.

5.3 Drain bias influence

It was also studied how V_d variation from linear regime up to saturation region impact the LFN properties. S_{Id}/I_d^2 - I_d characteristics have been plotted in Fig.5-24 for SOI and sSOI narrowest NW NMOS FETs. We found that a good agreement with CNF+CMF model is retained from linear ($|V_d|=40\text{mV}$ and 0.2V) to saturation regions ($|V_d|=0.9\text{V}$).

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Furthermore, the plateaued noise level in subthreshold region is also maintained regardless of the drain bias variation. Both trends, agreement of CNF+CMF model and constancy of plateaued noise level for varied V_d , are also observed in SOI and SGOI PMOS NWs, even in the devices with shortest L_g (Fig.5-25). These results mean that $S_{V_{fb}}$ and N_t properties are nearly independent of V_d without any strain impact in N- and PMOS NWs.

In literature, V_d dependent S_{Id}/I_d^2 behavior at strong inversion region ($V_g=1.2V$) has been discussed by Boutchacha and Ghibaudo in 2011 [5-51]. The experimental and simulation results show a slight increase of the noise level by a factor of less than 2 as V_d increases from 0V up to 1.0V. These results are in agreement with NMOS SOI NW (Fig.5-24a), and PMOS SOI and SGOI NWs (Fig.5-25a and b). NMOS sSOI NW show the opposite behavior, decreasing S_{Id}/I_d^2 level as V_d increases from 40mV to 0.9V. It is attributed to CMF and/or $1/f$ S/D noise is reduced due to V_d increase. On the other hand, PMOS SGOI NW shows a less noise level than that in SOI NW at strong inversion region. This highlights the advantage of SGOI NW for less $1/f$ S/D noise at inversion region, *i.e.* better quality of S/D regions (cf. Section 5.1.2).

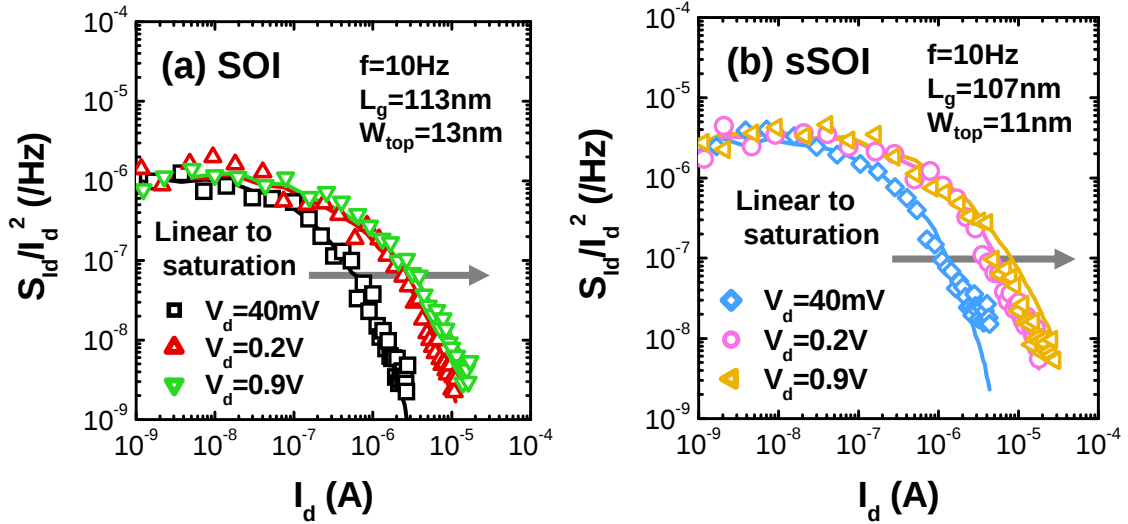


Fig. 5-24. V_d impact for (symbols) S_{Id}/I_d^2 - I_d characteristics of the narrowest NW NMOS FETs in (a) SOI ($L_g=113\text{nm}$) and (b) sSOI ($L_g=107\text{nm}$), with (lines) corresponding $(g_m/I_d)^2$ curves.

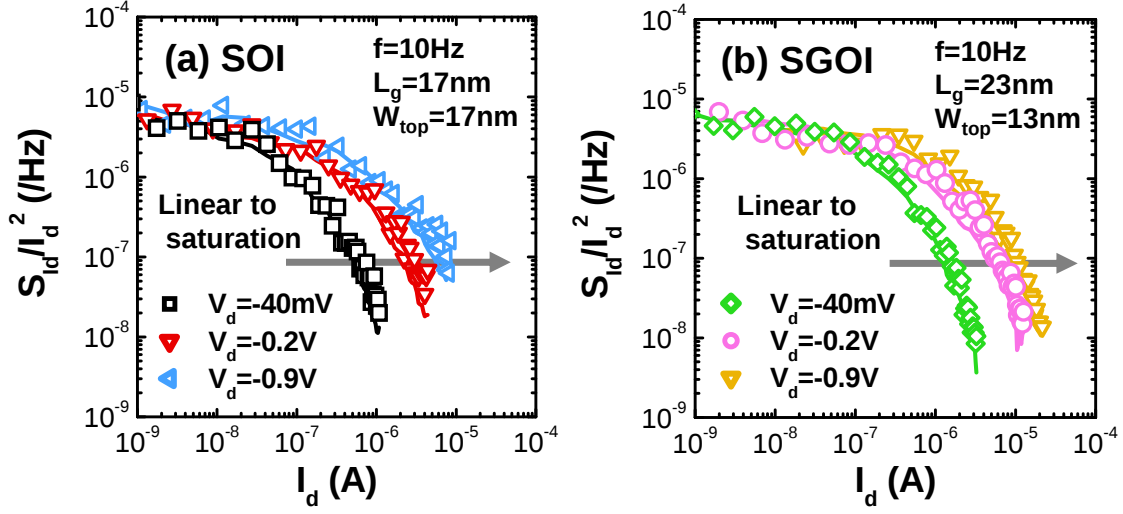


Fig. 5-25. V_d impact for (symbols) S_{Id}/I_d^2 - I_d characteristics of the narrowest NW PMOS FETs with short channel in (a) SOI ($L_g=17\text{nm}$) and (b) SGOI ($L_g=23\text{nm}$), with (lines) corresponding $(g_m/I_d)^2$ curves..

5.4 Comparison with ITRS requirements for 1/f LFN

Finally, gate voltage noise S_{Vg} obtained from measured S_{Id} was compared with ITRS requirements for LFN showing 1/f behavior for CMOS logic application [5-53]. S_{Vg} values are extracted at an overdrive operation ($V_g = V_t + 0.2\text{V}$ for NMOS, and $V_g = V_t - 0.2\text{V}$ for PMOS, respectively), and in saturation regime ($|V_d| = 0.3\text{--}0.4\text{V}$). The comparisons are shown in Figs.5-26~5-29. Table 5-2 (graphically plotted in Fig.1-7 and 1-39) summarizes the yearly requirements of L_g , V_{dd} , V_d (defined as $V_d = V_{dd}/2$), and S_{Vg} normalized by channel area ($W_{\text{tot}} \times L_g$) and frequency for high performance (HP) and low standby power (LSTP) logic circuits consisting of MG MOSFETs.

For NMOS, The narrowest NWs in both SOI and sSOI with gate length $L_g = 22\text{--}28\text{nm}$ already fulfill the noise requirements for year 2015 with approaching $L_g = 17\text{--}19\text{nm}$. They also almost satisfy the requirements for future CMOS technology node by 2026. In addition, sSOI shows slightly lower noise level that can help fulfill ITRS requirements more easily (Fig.5-27). No L_g and V_d dependence of the noise level

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on L_g range up to 113nm is observed, and device-to-device dispersion influence is just visible in both devices (Fig.5-26). In a previous reports for V_d dependent S_{Vg} [5-51,5-52], experimentally extracted and simulated S_{Vg} at strong inversion region ($V_g=1.2V$) decreases (by a factor of less than 3) as V_d increases from 0V up to 1.0V. This disagrees with our S_{Vg} results exhibiting roughly constant level without any V_d dependence. It is ascribed to difference of inversion condition, *i.e.* to weaker inversion condition in our results and required data in ITRS ($|V_g-V_t|=0.2V$).

For PMOS, L_g and V_d independent behavior as well as device-to-device dispersion effect is similarly observed with NMOS results (Fig.5-28). The normalized S_{Vg} of NWs with $L_g=22-23nm$ satisfy the demands until 2026 whatever technological splits (SOI, SiGe S/D or SiGe channel) (Fig.5-29). At minimum $L_g=17-18nm$, the noise level in SOI and cSG-S/D exceeds the ITRS requirements in 2026, while the three options still fulfill the data in 2015. SGOI NWs exhibit reduced noise level compared to Si channel NWs, mostly due to reduced $1/f$ S/D fluctuations (cf. Fig.5-10 and 5-11).

It can be thus concluded that both tensile and compressive strain technologies, besides electrical performance improvement (mainly through transport properties), are also attractive features in terms of the future $1/f$ noise requirements.

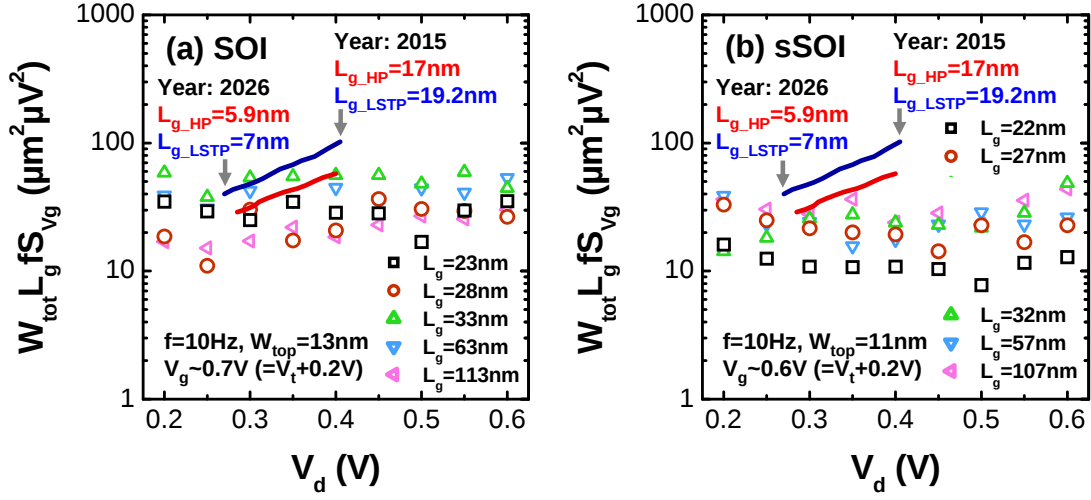


Fig. 5-26. (Symbols) S_{V_g} with normalization by channel size parameters (W_{tot} and L_g) and frequency as a function of V_d in the (a) SOI and (b) sSOI narrowest NW NMOS FETs. These data are compared with (lines) the requirements for $1/f$ LFN in ITRS 2013 (Table RFAMS1 CMOS technology requirements) for high performance (HP) and low standby power (LSTP) logics MG FETs [5-53].

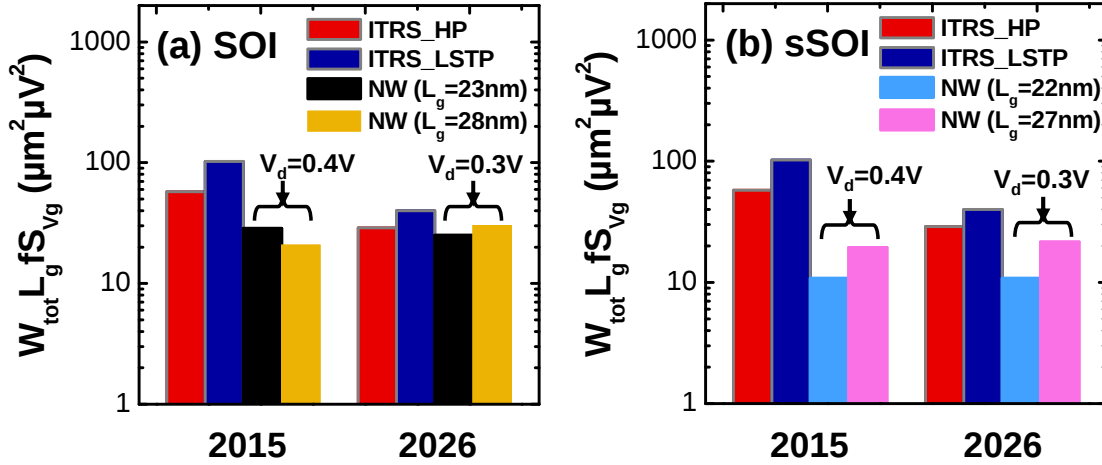


Fig. 5-27. Comparison of the normalized S_{V_g} between our experimental data and ITRS requirements in 2015 and 2026 in NMOS MG FETs [5-53].

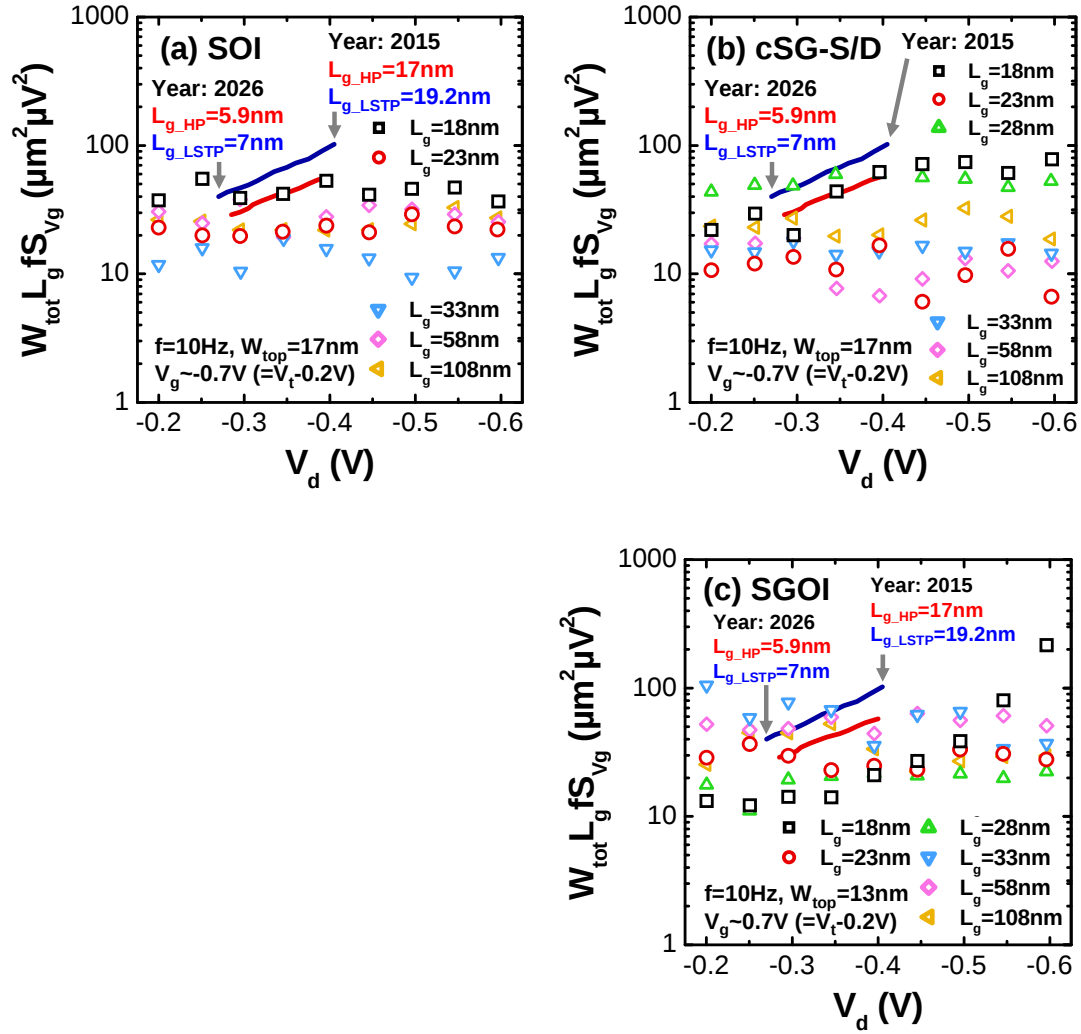


Fig. 5-28. (Symbols) S_{V_g} with normalization by channel size parameters (W_{tot} and L_g) and frequency as a function of V_d in the narrowest NW PMOS FETs for (a) SOI, (b) cSG-S/D, and (c) SGOI devices. These data are compared with (lines) the requirements for 1/f LFN in ITRS 2013 data [5-53] (cf. Fig.5-26).

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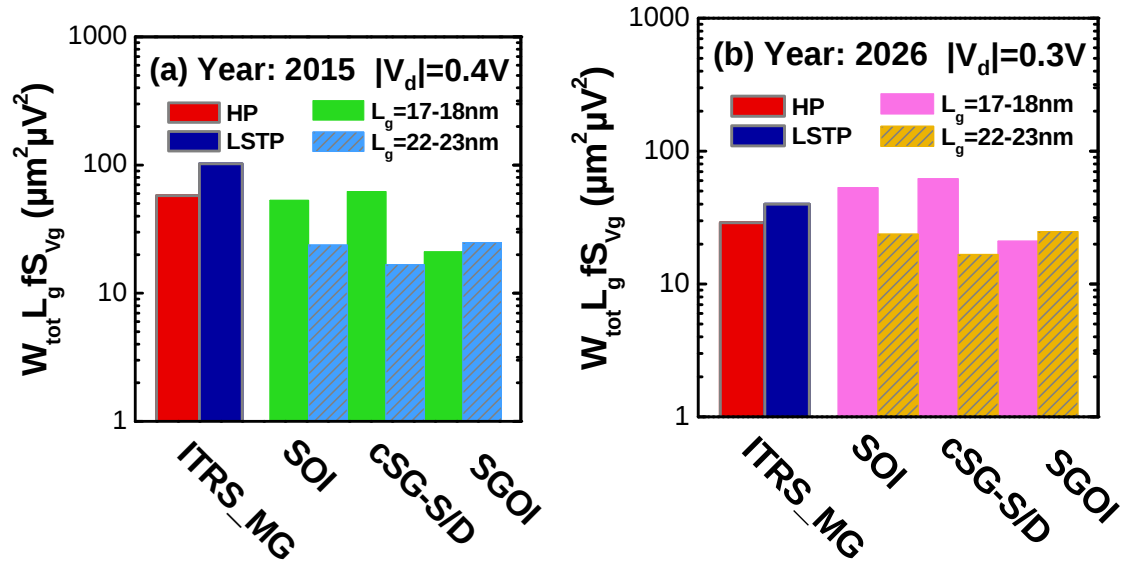


Fig. 5-29. Comparison of the normalized S_{Vg} between our experimental data and ITRS requirements in 2015 and 2026 for PMOS MG FETs [5-53].

Table 5-2. ITRS requirements data of L_g , V_{dd} , V_d , and normalized S_{Vg} conditions for high performance (HP) and low standby power (LSTP) logic circuits consisting of MG FETs (cf. Fig.1-7 and 1-39) [5-53].

ITRS for MG	HP logic				LSTP logic			
	L_g (nm)	V_{dd} (V)	V_d (V)	$W_{tot} L_g f S_{Vg}$ ($\mu m^2 \mu V^2$)	L_g (nm)	V_{dd} (V)	V_d (V)	$W_{tot} L_g f S_{Vg}$ ($\mu m^2 \mu V^2$)
2015	17	0.8	0.4	57.6	19.2	0.81	0.41	102.4
2016	15.3	0.77	0.39	53.8	17.5	0.78	0.39	90
2017	14	0.75	0.38	50.2	16	0.75	0.38	78.4
2018	12.8	0.73	0.37	46.7	14.6	0.72	0.36	72.9
2019	11.7	0.71	0.36	44.1	13.3	0.7	0.35	67.6
2020	10.6	0.68	0.34	41.6	12.1	0.67	0.34	62.5
2021	9.7	0.66	0.33	39.2	11.1	0.65	0.33	57.6
2022	8.9	0.64	0.32	36.9	10.1	0.63	0.32	52.9
2023	8.1	0.62	0.31	34.6	9.2	0.61	0.31	49.3
2024	7.4	0.61	0.31	32.4	8.4	0.59	0.30	46.7
2025	6.6	0.59	0.30	30.3	7.7	0.56	0.28	43.3
2026	5.9	0.57	0.29	28.9	7	0.54	0.27	40

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5.5 References

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Chapter 6. Summary and Conclusions

In this work, the gate oxide/channel interface properties were experimentally and comprehensively investigated by carrier transport and low-frequency noise (LFN) characterizations in ultra-scaled NW MOSFETs. The purpose and originality of this work are to understand electrical properties of the gate oxide/channel interface mainly by LFN investigations with important concerns as follows;

- (i) CNF+CMF model parameters as a function of channel size down to NW
- (ii) NW FETs with advanced Hf-based high- κ /metal gate stack
- (iii) Difference of crystallographic orientations between channel top and etched side-wall surfaces
- (iv) Large channel surface/volume ratio (volume inversion effect?) of NW
- (v) Strained NW technology;
NMOS - tensile strain *PMOS* - compressive strain
- (vi) ITRS requirements for future CMOS logic circuits comprised of MG FETs

Our Si NW MOSFETs were fabricated from advanced fully-depleted SOI (FD-SOI) substrate to efficiently reduce detrimental SCE, resulting in the cross-section as small as 10nm×10nm. As the gate stack, Hf-based high- κ /metal (HfSiON/TiN) was used in order to suppress the gate leakage effects. Furthermore, strain introduction to the channel was additively processed to further improve the MOSFET's on-state performance. Tensile strained-SOI substrate was applied for NMOS, on the other hand, three-types of compressive stressors were used for PMOS devices; strained Si channel by raised SiGe-S/D and CESL formations, and strained SiGe-on-insulator (SGOI) substrate. In addition, impacts on channel direction difference ([110] vs. [100]) and on NW cross-sectional shape (with or without additional H₂ anneal resulting in the rectangular or rounded shape, respectively) were parametrically tested.

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6.1 Carrier transport characterizations

Firstly, the most common and important I_d - V_g characteristics were studied in single-channel Ω -gate NW MOSFETs to understand the basic performance. 4-types of parameters; threshold voltage V_t , drain induced barrier lowering (DIBL), subthreshold swing (SS), and on-state current I_{ON} were extracted and discussed. The reference SOI NWs successively provided the excellent static control against SCE as shown in DIBL and SS discussions. The stressors dramatically enhanced the I_{ON} owing to a modification of the channel energy-band structure. However, the SCE endurance was negatively affected, especially for PMOS consisted of SGOI NWs. This trade-off relationship thus needs to more optimize the strain processing.

Next, carrier effective mobility μ_{eff} was carefully studied in strained and unstrained Si NWs with the 50-multiple channel fingers along [110]-direction and with the rectangular (TG) or rounded (Ω G) NW cross-sectional shapes. We found that: (i) the μ_{eff} properties in TGNW with (100) top and (110) side-wall surfaces are well described by the separate contribution of inversion surfaces for the rectangular section as small as 10nm×10nm; (ii) Ω GNW mainly exhibits the similar μ_{eff} behavior as TGNW, in spite of the more complex geometry with multiple surface orientations, for the top-view width W_{top} down to 23 nm; (iii) lower Coulomb scattering was observed in Ω GNW, as a possible consequence of the additional H_2 anneal process; (iv) uniaxial tensile strain obtained from sSOI substrate was effective in NMOS NWs, independently of the NW geometry, and can thus be exploited to enhance entirely NMOS performance in NW dimension.

Then, low-field mobility μ_0 in the single-channel NW devices was extracted from Y-function method and characterized for L_g down to 17nm. We observed that: (i) the L_g dependent μ_0 degradation is appeared in NW devices as with wide MOSFETs, highlighting the specific behavior in NW architecture for both N- and PMOS by degradation factor α_μ discussion; (ii) sSOI NWs for NMOS maintains the advantage of uniaxial tensile strain down to the shortest L_g =22-23nm with smaller normalized S/D

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resistance R_{SD} ; (iii) 4-types of compressive stressors for PMOS NWs largely improve the performance, especially SGOI NW shows the lowest normalized R_{SD} and the highest μ_0 gain at the shortest $L_g=17-18\text{nm}$. The μ_0 extraction exhibits the effectiveness for MOSFET's performance evaluation even for ultra-scaled NW architecture.

6.2 Low-frequency noise characterizations

LFN investigation was effectively applied for the evaluation of various technological and architectural parameters. Carrier number fluctuations with correlated mobility fluctuations (CNF+CMF) model can describe the $1/f$ noise behavior from subthreshold to strong inversion modes in all our devices down to the shortest and narrowest NW MOSFET. The drain current noise behavior is basically similar in both N- and PMOS devices regardless of the technological splits. Increase of $1/f$ noise level at strong inversion region in PMOS devices stems from worse quality of S/D regions. This impact can be perfectly interpreted by the CNF+CMF model completed with a term of R_{SD} fluctuations. This observation shows the lower S/D region noise in SGOI NW, and thus the advantage can be clearly found.

The geometrical variations with the W_{top} and L_g alter the CNF component on LFN, the flat-band voltage noise S_{Vfb} , with simple impact of device scaling, which is reciprocal to both W_{tot} and L_g . Any harmful impact of surface orientation difference between the channel (100) top and (110) side-walls is not observed. The scaling regularity with both W_{tot} and L_g , without much quantum effect, could be attributed to the use of HfSiON/TiN gate stack and the carrier transport occurring mainly in 2D surfaces of top and side-walls even in NW geometry. On the other hand, the CMF factor, Coulomb scattering parameter $\alpha_{sc}\mu_{eff}$, is not altered by decreasing dimensions or 3D structure impacts, while the mobility strongly depends on the impacts. It is only dominated by device-to-device dispersion. No clear relationship between the $\alpha_{sc}\mu_{eff}$ and μ_0 is observed, also without influence of improved mobility in strained NW FETs.

The oxide trap density N_t extracted from the S_{Vfb} is not also significantly modified by scaling, architecture, and technological parameter impacts. The separation method of

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the contributions between top surface and side-walls of the channel is demonstrated in order to strictly assess the difference. It reveals that the oxide quality on (100) top and on (110) side-walls is roughly comparable in all the [110]-oriented devices. This is in good agreement with the result of charge pumping measurement in NW gated P-i-N diode. The extracted N_t values are also roughly steady and same as the recently reported values for state-of-the-art Hf-based gate oxide.

Variation of the drain voltage bias does not significantly influence the LFN behaviors (CNF+CMF model and oxide trap density) in our NW MOSFETs regardless of L_g scaling and strain effect. Furthermore, the both strained and unstrained NWs accomplish the $1/f$ LFN requirements for future CMOS logic node with MG FETs stated in the ITRS in 2013. It is thus well demonstrated that strain technology is a powerful booster of the NW FET performances.

6.3 Feature of advanced NW MOSFETs

LFN characterizations based on CNF+CMF model were successively performed in NW MOSFETs with HfSiON/TiN gate stack. Experimental results about the important concerns are concluded as follows. CNF component shows a simple regularity of channel area scaling without structural impact of NW. This reveals that difference of crystallographic orientation between top and side-wall surfaces and etched side-walls do not have large influence to the interface properties. Also, the quantum effect of carrier confinement is not observed in our NWs with the HfSiON/TiN gate.

An excellent quality of the channel interface with HfSiON/TiN gate is sustained for all our technological and geometrical device parameters by extraction of oxide trap density. A simple separation method of contributions between top and side-wall surfaces to the trap density is demonstrated. It is reconfirmed that the interface quality on (100) top and on etched (100) or (110) side-walls is roughly comparable in all the devices.

It is finally concluded that the appropriate strain technologies powerfully provide beneficial features to improve both carrier transport and $1/f$ LFN properties for future CMOS circuits consisting of NW FETs, without a significant concern on the

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oxide/channel interface quality. Consequently, the channel interface quality is mainly dominated by the extrinsic fabrication parameters appearing such as device-to-device dispersion, in undoped FD-channel technology with HfSiON/TiN gate stack, whereas the carrier transport property strongly depends on intrinsic structural impacts.

6.4 Future perspectives

LFN measurement can be applicable for the characterization of further advanced MG devices, which is GAA junction-less (JL) FET only comprised of uniformly doped body without S/D regions [6-1,6-2]. The GAA JL-FET with a short $L_g=3\text{nm}$ can operate without noticeable SCE [6-3]. In a study by Jang *et al.* in 2011 [6-1], CNF+CMF model well describes the $1/f$ noise behavior.

For characterizations in Schottky S/D device [6-4], thin-film-transistor (TFT) [6-5,6-6], nanowire FETs with the different body materials from Si [6-7~6-10], the LFN measurement has been also used. In a report of Schottky S/D device [6-4], studies of Si [6-5] and IGZO [6-6] TFETs, and in a report of InAs NW [6-8], $1/f$ noise behaviors have been investigated based on CNF.

Moreover, the LFN measurement has been applied for characterization of the different concept device from MOSFET such as tunnel-FET (TFET) [6-11~6-14] and high electron mobility transistors (HEMT) [6-15,6-16]. The TFET and HEMT operated under different carrier transport theory from MOSFET, achieving better switching performance with the steeper SS than MOSFET's lower limit of 60mV/dec by using TFETs in theory, and with availability for further high-frequency operation by using HEMTs. The different noise theory from CNF+CMF model is expected for TFETs owing to the band-to-band tunneling (BTBT) based carrier transport.

Furthermore, LFN investigation has been applied to novel devices consisting of 1D or 2D materials, such as carbon nanotube (CNT) [6-17~6-20], graphene [6-21,6-22], and molybdenum-disulfide (MoS_2) [6-23~6-28]. In these novel materials, CNF(+CMF) model is often suitable for the $1/f$ noise characterizations. Consequently, LFN characterization can be a powerful diagnosis tool even for the future promising devices.

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6.5 References

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List of Publications and Presentations

My publications and presentations between October 2011 and March 2015 as first author are only listed.

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- [1] M. Koyama, M. Cassé, R. Coquand, S. Barraud, C. Vizioz, C. Comboroure, P. Perreau, V. Maffini-Alvaro, C. Tabone, L. Tosti, S. Barnola, V. Delaye, F. Aussenac, G. Ghibaudo, H. Iwai, and G. Reimbold, “Study of carrier transport in strained and unstrained SOI tri-gate and omega-gate silicon nanowire MOSFETs,” *Solid-State Electronics*, vol. 84, pp. 46-52, March 2013.
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- [5] M. Koyama, M. Cassé, R. Coquand, S. Barraud, G. Ghibaudo, H. Iwai, and G. Reimbold, “Influence of Technological and Geometrical Parameters on Low-frequency Noise in Omega-gate Nanowire NMOSFETs,” *21st International Symposium on VLSI Technology, Systems and Applications (VLSI-TSA 2014)*, Hsinchu, Taiwan, April 2014, pp. 27-28.

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