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論 文 要 旨

THESIS SUMMARY

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要旨（英文 800 語程度）
Thesis Summary（approx.800 English Words ）

In this thesis, the gate oxide/channel interface properties were experimentally and comprehensively investigated by carrier transport and low-frequency noise (LFN) characterizations in ultra-scaled nanowire (NW) MOSFETs. NW MOSFETs, which have aggressively downscaled cross-section of the body, are strong candidates for near future CMOS technology nodes. However, the interface quality could be a critical issue due to the NW body formed by etching process, the multiple surface orientations, the large surface/volume ratio, and additional strain technology to enhance the carrier transport performance. The understanding of carrier transport and channel interface quality in NW MOSFETs with advanced high-κ/metal gate is thus particularly important and needs experimental and theoretical investigations. LFN provides deep insights into the electrical interface properties in MOSFETs and the characterization has no lower limit of the necessary channel area. LFN measurement can be thus a powerful characterization technique even for ultra-scaled NW MOSFETs. Also, extraction of fitting mobility (such as low-field mobility) by Y-function method is an efficient method for the evaluation of carrier transport in ultra-scaled FETs.

Our NW MOSFETs were fabricated from fully-depleted silicon-on-insulator (FD-SOI) substrate, and with Hf-based high-κ/metal gate stack (HfSiON/TiN) in order to reduce short channel effects (SCE), which are detrimental effects by device downscaling. In addition, strain technologies to the channel were additively processed to efficiently improve the MOSFET's performance. Tensile strained-SOI substrate was used for NMOS FETs, whereas compressive stressors were used for PMOS devices. Compressively strained Si channel was processed by raised SiGe S/D and CESL formations. In addition, strained SiGe channel was also fabricated for further high-performance PMOS FETs.

Firstly, the most common I_d-V_g characteristics were studied in single-channel Ω-gate NW MOSFETs to understand the basic performance. The reference SOI NWs successively provided the excellent static control down to short channel device with gate length of 17nm. The stressors dramatically enhanced the on-current owing to a modification of the channel energy-band structure. Then, low-field mobility in single-channel NW devices was characterized and also demonstrated large improvement of the performance by stressors. Gate length dependent mobility degradation was observed in NW devices as with planar

MOSFETs, highlighting the specific behavior in NW architecture. The mobility extraction exhibits the effectiveness for MOSFET's performance evaluation even for ultra-scaled single-channel NW architecture.

The LFN investigation was effectively applied for the evaluation of various technological and architectural parameters. Carrier number fluctuations with correlated mobility fluctuations (CNF+CMF) model described the 1/f noise behavior in all our devices down to the shortest and narrowest NW MOSFET. The drain current noise behavior was basically similar in both N- and PMOS devices regardless of the device technological splits. For PMOS FETs, increase of 1/f noise at strong inversion stemming from S/D regions was observed. This impact can be perfectly interpreted by the CNF+CMF model completed with a term of S_{Rsd} fluctuations. This observation highlighted an advantage of SGOI NW with the lowest level of S/D region noise.

Geometrical variations with the channel width and gate length altered the CNF component, the flat-band voltage noise S_{Vfb}, with simple impact of device scaling (reciprocal to both total channel width and gate length). No significant impact of surface orientation difference between the channel (100) top and (110) side-walls, and of etched side-wall surface of NW body were observed. The scaling regularity with both channel width and length, without visible quantum confinement, could be attributed to the use of HfSiON/TiN gate stack and the carrier transport occurring mostly in 2D surfaces of top and side-walls even in NW geometry. Meanwhile, the CMF factor, Coulomb scattering parameter $\alpha_{sc}\mu_{eff}$, was not altered by decreasing dimensions or 3D structure impacts, while the mobility strongly depends on the impacts.

Extracted oxide trap density N_t was roughly steady with scaling, architecture, and technological parameter impacts. Simple separation method of the contributions between channel top surface and side-walls was demonstrated in order to evaluate the difference. It revealed that the oxide quality on (100) top and on (110) side-walls was roughly comparable in all the [110]-oriented devices. The N_t values lie in similar order as the recently reported data. Consequently, an excellent quality of the interface with HfSiON/TiN gate stack was sustained for all our technological and geometrical splits.

Finally, the both strained and unstrained NWs fulfilled the 1/f LFN requirements stated in the ITRS in 2013 for future CMOS logic node with MG FETs. Consequently, we concluded that the appropriate strain technologies powerfully provide improvement of both carrier transport and 1/f LFN properties for future CMOS circuits consisting of NW FETs, without a significant concern about the oxide/channel interface quality.