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著者(和文)	高前田（山崎）伸也
Author(English)	Shinya Takamaeda-Yamazaki
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論 文 要 旨

THESIS SUMMARY

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学生氏名： Student's Name	山崎 伸也		指導教員（主）： Academic Advisor(main)	吉瀬 謙二	
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要旨（英文 800 語程度）
Thesis Summary (approx.800 English Words)

In modern microprocessor architecture research and development, software-based simulators of microprocessors are essential to evaluate and verify an architectural idea. By using a software-based simulator with detailed models of processor cores and memory systems, we can realize and evaluate the proposed idea in an easy way without actual LSI fabrication.

The most critical issue of software-based simulations is simulation speed. Unfortunately, regardless of simulation accuracy, however, simulation speeds of software-based simulators are considerably slower than actual processor LSIs. The simulation speeds of software-based processor simulators are about 100 KHz in the case of a detailed model.

In order to accelerate such processor simulations, the hardware-based prototyping with FPGAs have been commonly used. The fine-grain parallelisms of processor components can be naturally utilized by employing internal fabrics of FPGAs. Moreover fine-grain synchronization for cycle-accuracy is much faster on FPGAs than the software simulators. The faster simulation speed strongly supports system-level evaluations of not only the processor architecture but also the application and system software.

A problem of FPGA-based prototyping is the lack of any scalable simulation methods. In standard prototyping way, a large high-end and expensive FPGA is required for simulation of future many-core processor with over 100 cores. Additionally, the synthesis time that is the elapsed time to create an FPGA circuit image (bitstream) from HDL source codes is very long in large FPGAs. Previous FPGA-based simulators projects proposed some clever techniques to reduce resource consumption of FPGAs. They, however, decrease also the simulation speed if a processor with a large number of cores is simulated.

Another problem is the absence of any suitable abstraction methods to handle bare-metal sea-of-resources of FPGAs. Since there is a gap of resource characteristics between simulated processors and FPGAs, the structure of microprocessors is not necessarily suitable for FPGA characteristics. In respect of the memory system, processors have on-chip cache memory systems. Usually these cache memory systems are implemented by using on-chip fast memory fabrics (block RAM) of FPGAs. Unfortunately, the amount of these on-chip memory fabrics of FPGA is limited and small. If the simulated processor requires larger capacity of on-chip FPGA memory, the simulator developer should consider combining an external memory component (DRAM) for cache system implementation. Development of such a hierarchical memory system with keeping the cycle level accuracy of simulation result is highly error-prone and time-consuming.

This thesis presents a sophisticated prototyping framework for future manycores. The framework comprises of the acceleration method of many-core processor simulations and the design methodology to decrease the development complexity.

The first contribution of the framework is to propose an FPGA-based simulation method which achieves the scalable simulation speed against the increasing core count of simulated processors with the cycle-level accuracy of simulation results. In order to accelerate simulations of many-core processors, I propose a system architecture of fast and cycle-accurate processor simulator employing multiple FPGAs. I developed a test bed platform of multiple FPGAs to evaluate the viability of the proposed method. I evaluated the

proposed method by using the test bed system in point of simulation speed. The evaluation result shows that the proposed method achieves effective scalability of the simulation speed to simulate a large scale many-core processor with keeping the cycle-accuracy of the simulation consequences. As the case studies, I applied the test bed system for two innovative researches of task allocation schemes on many-core processors. By employing the test bed system, the evaluation phases are dramatically accelerated, so that it enables effective evaluations of computer systems.

The second contribution of this framework is to propose a design methodology under the resource abstraction of FPGA platforms. In order to mitigate the development complexity of FPGA-based simulators, I propose a novel design methodology under the abstraction of various resources FPGA platforms have, such as memory systems and inter-FPGA interconnections. I developed the Python-based design tool-chain that automatically synthesizes ready-to-implement RTL designs for actual FPGA platforms from target RTL descriptions under the abstraction. This methodology enables designers to model a prototyping target processor without concern for actual platform resources. I evaluated simulation speed under the abstraction using a standard FPGA platform with large capacity of logic and memory. The evaluation result shows that the simulation speed degradation under the abstraction is not critical so that the abstraction tool-chain offers the helpful support to develop a high-speed processor simulator rapidly.

Finally I evaluated the integrated framework of the two contributions, the scalable simulation accelerator and the abstraction methodology. The evaluation result shows that the simulation system automatically synthesized by the abstraction tool-chain archives almost equivalent performance to manual-tuned multi-FPGA based simulator. The integrated framework aggressively improves the prototyping efficiency for emerging many-core processors by providing the sufficient simulation speed and the effective abstraction reducing the development complexity.