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High performance organic-light-emitting-diode television system for high yield manufacturing

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Abstract

OLED has many great features suitable for television, such as high color reproduction, wide viewing angle and very high contrast. However, due to the premature manufacturing infrastructure, large display could not be fabricated for the market. To make large AMOLED TV happen, two different display designs were tried.

First prototype was a trial with amorphous silicon TFT backplane so that the design rule limitation of AMOLED due to excimer laser annealing might be removed. Driving capability for large AMOLED was demonstrated and the largest issue, TFT instability, was managed by the combination of low stress driving, current-concentration reduction and high stability amorphous silicon film formation.

Second prototype was aiming to have good manufacturability for large AMOLED TVs. At first, yield simulation was made to know how defect density affects the production yield of a large display. As a consequence, "Scalability" for OLED as well as on "Scalable" TFT were employed for the prototype. Color-by-white OLED technology on MILC TFT backplane was used to meet the requirement. Though it was believed that color-by-white approach cannot make

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both high color gamut and low power consumption happen at the same time, by means of the spectrum analysis and color filter development on RGBW sub-pixel configuration, high color gamut over 100% NTSC and lower power consumption than LCD were achieved at the same time to prove that high yield manufacturing of superior display performance can be attained. The technology has been used for generation-8 and is currently dominant technology for large AMOLED TV in the market.

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1.General introduction

1.1 History of OLED technologies

After a quarter century of development, OLED technology has been penetrating into the market, especially for the smart phone display. Fig. 1 shows the device structure and materials of so called "First OLED (Organic Light Emitting Device) " reported by Ching W. Tang and Steven Van Slyke in 1987.[1]

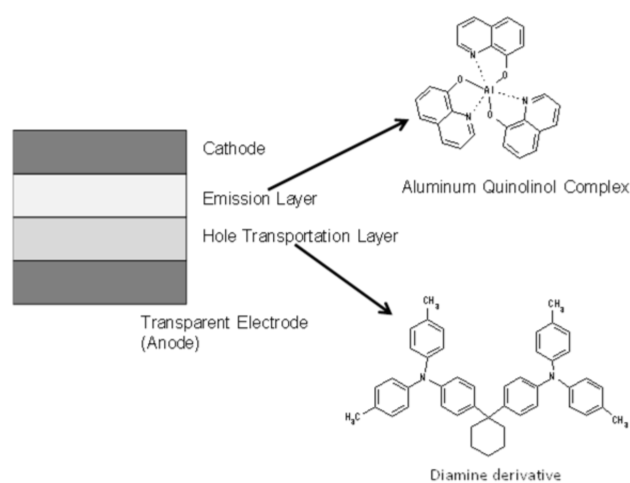


Fig. 1 OLED device reported by C.W.Tang and S.Van Slyke

Since before the "First OLED paper", light emission from organic material, such as anthracene, was observed [2], however Tang's structure was using several novel and advanced concepts such as,

(1) Significant increase in electron-hole recombination by using multiple layers,

(2) Film formation by evaporation to obtain high quality property,

(3) Appropriate anode/ cathode electrode material choice for sufficient charge injection and

(4) Very thin film to enable high electric field for space-charge-limited current,[3]

and these concepts are still used in state-of-art OLED devices. After first OLED product was released for car audio from Pioneer, the new device was used for segment-type indicators and low resolution display using passive-type driving.

Fig. 2 First AMOLED display product (Kodak LS633 Digital Camera)

In 2003, Kodak and Sanyo successfully started manufacturing of active-matrix OLED displays (AMOLED), which revealed the large merit of OLED displays versus conventional display technologies in terms of display performance. (Fig. 2) Since then, OLED display has been gradually adopted for many applications, especially for cellular phones, MP3 players and portable multimedia players. In 2007, Sony started shipment of 11-inch AMOLED television (Fig. 3) and it triggered the use of OLED for television use.

Fig. 3 11-inch AMOLED television (Sony XEL-1)

In 2012, both LG and Samsung demonstrated 55-inch AMOLED television using different technologies. (Fig. 4) LG's display was using color-by-white method and IGZO(Indium-Gallium-Zinc Oxide)-TFT, while Samsung was using shadow-mask patterning and SLS(Sequential-Lateral-Solidification) LTPS TFT.

Recently, LG demonstrated 77-inch AMOLED television in 2014 Consumer Electronics Show. Thus, OLED has been considered as next-generation technology

for large television. In reality, there used to be several technologies, such as SED (Surface-conduction electron-emitter display), FED (Field emission display) and Ferroelectric LCD, regarded as promising technology for large television, but was not successful. Recently, PDP (Plasma Display Panel), which was once thought to become the main stream of future large television, is losing its driving force and its market share against LCDs.

In this thesis, two cases of OLED display prototyping are discussed from the viewpoint of performance and high yield manufacturability to determine how to make high performance large OLED television manufacturing happen.

Fig. 4 LG's 55-inch AMOLED television (Demonstrated at SID2012 exhibition)

1.2 Current situation toward large and high performance OLED displays

Table 1 shows comparison between LCD and OLED display. [4] (1) response time, (2) punching capability, (3) viewing angle and (4) simple structure can be differentiation of OLED against LCDs for television use.

Parameter	LCD	OLED
Response time	Slow; hold-like (delayed)	Fast, impulse-like (rapid)
Punching	Difficult	Possible
Viewing angle	Narrower high contrast angle region	Lambertian distribution
Number of components	More	Fewer

Table 1 Difference between LCD and OLED[4]

(1) Response time

To avoid the efficiency drop caused by the triplet-triplet annihilation, the exciton decay time used in OLED display is about the order of microsecond.[5], so the display has very fast response time, idealistic for moving image reproduction as compared with twisted-nematic (TN) type LCD that has response time about the order of milliseconds.[6]

(2) Punching capability

"Punching" technique [7] is a driving method used in self-emissive television displays like CRT, PDP and OLED. Small highlight area is driven at high luminance, so that the image can be displayed at much higher contrast ratio than its normal capability due to human iris aperture change.

(3) Viewing angle

OLED is a self-emitting device, so the emission from the device has Lambertian distribution, just like a diffusion surface reflection. Also when it shows black level, no emission takes place, so contrast ratio in dark room should be very high. If appropriate display surface is prepared [8] with very low reflection, contrast ratio in television-viewing environment, such as living room that has about 200lx illuminance, can be very high like more than 1000:1.[9] (Called “Living room contrast ratio”)

In terms of LCDs, crossed-nicol polarizer configuration should have very low light output, so LCD-mode like vertical alignment (VA) shows very high contrast ratio from the right-in-front direction. However oblique observation causes deviation from crossed-nicol and light leakage takes place. There are many great compensation films already developed [10], however still the contrast ratio from oblique angle is not as good as OLED displays.

Lack of contrast ratio also reduces color saturation due to mixture of leaked light with original primary color. It is also known that saturated color is perceived as higher brightness (Helmholtz-Kohlrausch effect [11]), so the self-emissive display like OLED can be perceived as with larger contrast ratio further.

(4) Simple structure

Fig. 5 shows structure comparison between LCD module and OLED module. [12] Liquid crystal cell is an optical shutter, so LCD needs a planar light source beneath LCD cell component. For LCD operation control for matrix addressing, TFT arrays are used. In the case of side backlighting system, light source such as LEDs or fluorescent lamp shines and delivers the light to light guide. For high light utilization, reflector attached to the light source is used. Light travels in light guide film and is extracted due to scattering dots marked on the light guide. To enhance the light output, multiple optical film, such as BEF (Brightness Enhancement Film: Prism sheet), DBEF (Dual Brightness Enhancement Film: Light recycling film) and scattering films are used. For light output control, LCD needs two polarizers. Also, as discussed, to compensate for the birefringence, LCD needs compensation films, such as a-axis or c-axis film. Thus, LCD needs many components.

On the other hand, as OLED is a self-emissive device, the structure is much simpler. TFT arrays are used for matrix addressing, just like active-matrix LCDs.

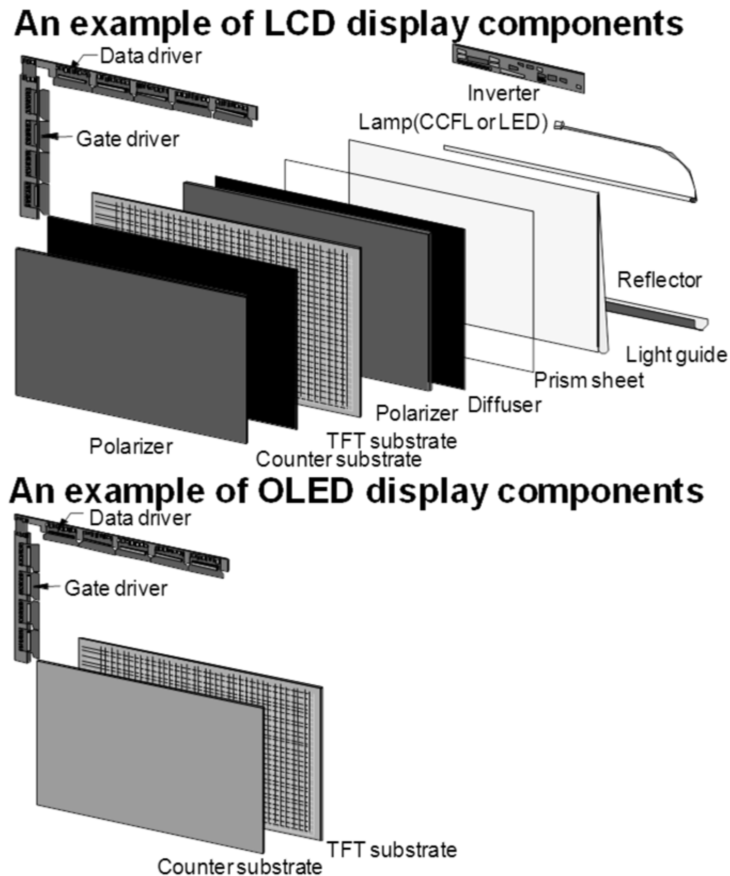


Fig. 5 Comparison between LCD and OLED[12]

The features described in (1)-(4) can bring significant visual merit for television, so large OLED television would promise attractive image suitable for high quality broadcasting. However, in reality, there are other television display technologies, which could not bring into market, such as ferroelectric LCD, SED and FED. In the case of PDP, the technology was once accepted as a viable method for television, however it was left far behind the LCD in actual business. It is quite important to consider how an attractive display technology can win the game against existing mature technologies.

For the active-matrix driving, low temperature poly silicon (LTPS) TFT formed by excimer laser annealing (ELA) are normally used [13], however, ELA process has size limitation. [14] In section 2, non-ELA TFT backplane approach to go over the ELA size limitation is discussed to find out the pros and cons of the story. In section 3, the best scenario for the large AMOLED TV manufacturing is discussed, taking precedent cases into consideration, and a prototype that would deliver both high yield and excellent display performance is fabricated and discussed.

2. Approach to designing a large AMOLED display over ELA size limitation

2.1 OLED display design tradeoffs

Fig. 6 and Fig. 7 show one example of schematic ELA LTPS process flow and the detail respectively. [15] Amorphous silicon is deposited by Chemical Vapor Deposition (CVD) method. The film is annealed to remove hydrogen from the film (Dehydrogenation annealing) and the excimer laser beam is irradiated to crystallize the film using laser equipment like Fig. 8. The silicon pattern is photo-patterned and gate insulator/gate metal are deposited. Gate electrode is patterned by photo-lithography and ion doping to form contact region is made. After interlayer is deposited, via hole is patterned by photo-lithography and source/drain metal is deposited Source/drain metal is patterned by photo-lithography and the TFT is fabricated.

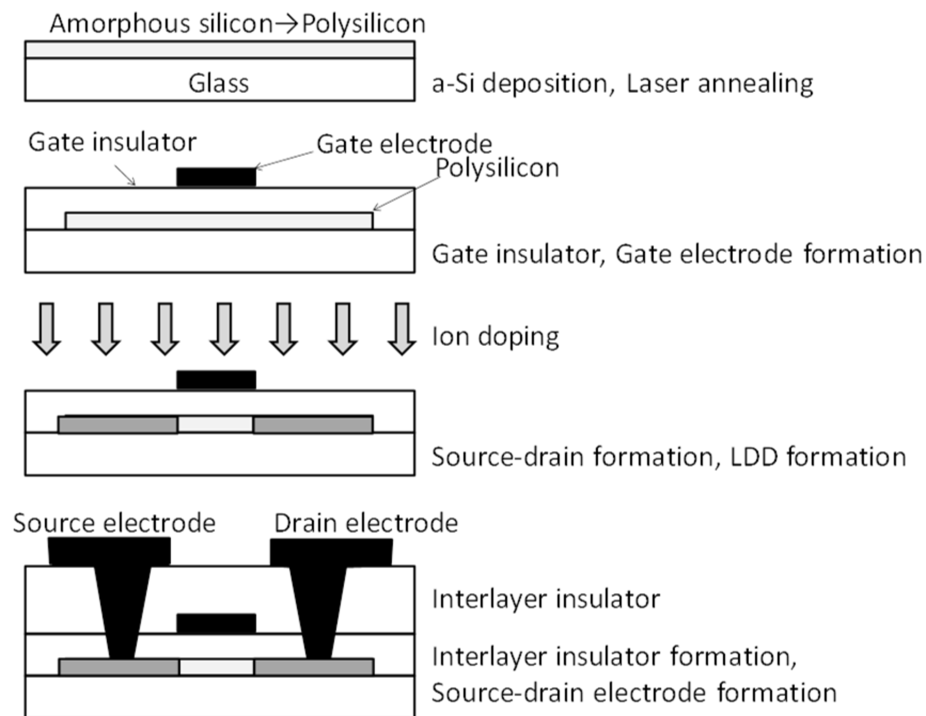


Fig. 6 Polysilicon TFT process by excimer laser annealing [15]

	Cleaning
	CVD(a-Si)
	Dehydrogenation annealing
	Ion doping (Br channel doping)
1 PEP	Si island resist patterning
	Dry etching
2 PEP	P doping mask formation
	Ion doping (P channel doping)
	CVD (Gate insulator)
	Sputter (Gate electrode)
3 PEP	Gate electrode mask formation
	Dry etching
	Ion doping (LDD doping by P)
4 PEP	Br doping mask (p+) formation
	Ion doping (Br)
5 PEP	P doping mask (n+) formation
	Ion doping (P)
	Activation anneal
6 PEP	Contact hole mask formation
	Wet etching
	Sputter (Data line)
7 PEP	Data line mask formation
	Wet etching
	CVD (Passivation)
8 PEP	Passivation patterning mask
	Dry etching
	H2 forming anneal
	Sputter (ITO)
9 PEP	Pixel mask formation
	Wet etching
	Inspection

Fig. 7 An example of CMOS polysilicon TFT process by excimer laser annealing [15]

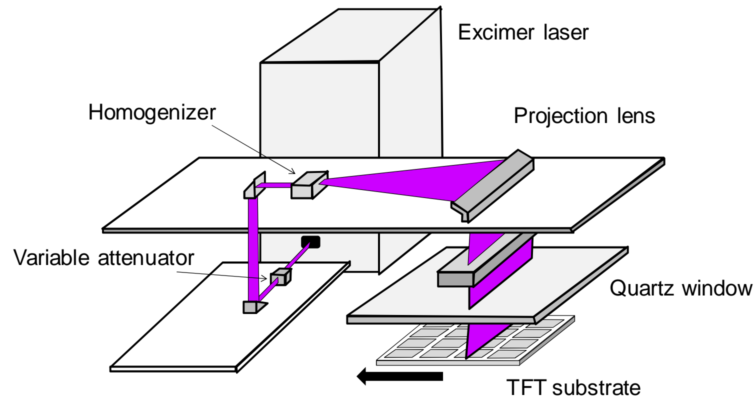


Fig. 8 Excimer laser annealing equipment [15]

To obtain high mobility LTPS TFT, larger grain size is necessary. [16] (Fig. 9) As shown in the glass substrate case of Fig. 10, there is an optimal energy for obtaining the largest grain size during ELA process [15] and lower or higher laser irradiation deteriorates the mobility performance. Laser power obtainable from one excimer laser tube is limited, so there is a size limitation of laser irradiation. In IDW 2002, M.Kobayashi et al. demonstrated 17-inch AMOLED display using ELA-LTPS TFT backplane [17]. At the time, available beam length from ELA tool was about 200mm~300mm [18], so 17-inch was almost the maximum size for ELA processing. (Fig. 11) Fig. 12 shows the CRT (Cathode Ray Tube) shipment in year 2003. [19] The statistics was telling that over 20-inch was necessary for the major television market, however that could not happen using ELA-LTPS process due to beam length limitation. To go beyond 20-inch to apply AMOLED to the mainstream television market, alternate TFT technology was necessary. On the other hand, at the time, 40-inch LCD was already in the market in the case of LCDs using amorphous TFT backplane. [20] A trial to apply amorphous silicon TFT to the large AMOLED application is reported in this section. [4][21][22]

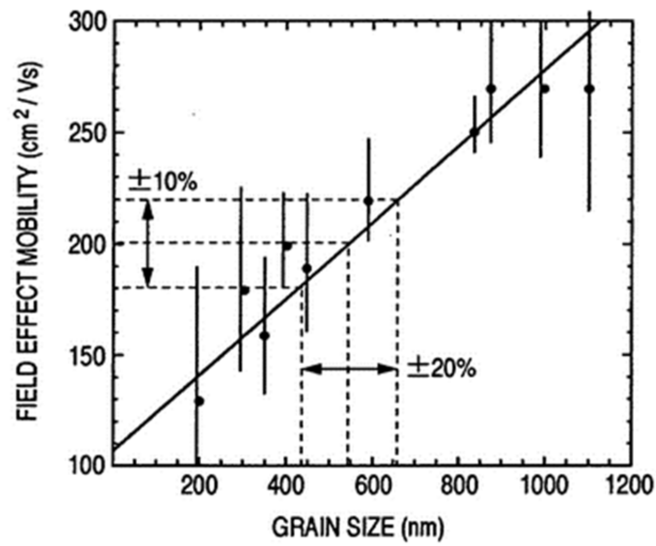


Fig. 9 Grain size dependence of polysilicon field effect mobility [16]

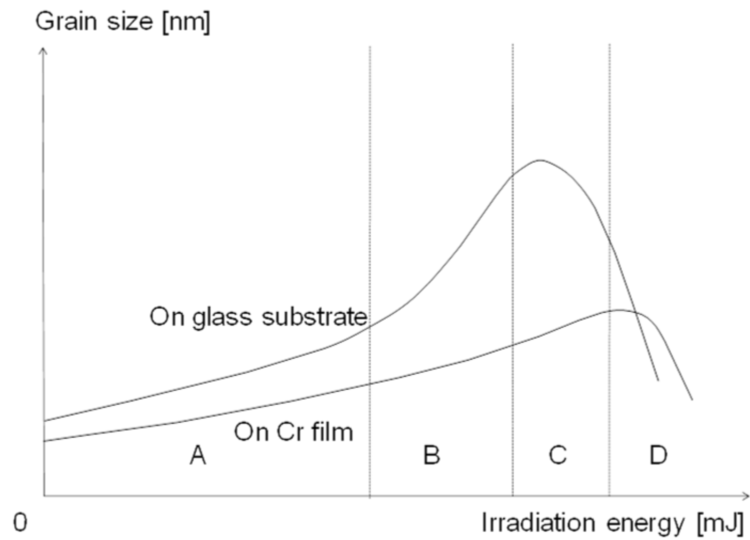


Fig. 10 ELA energy dependence of grain size [15]

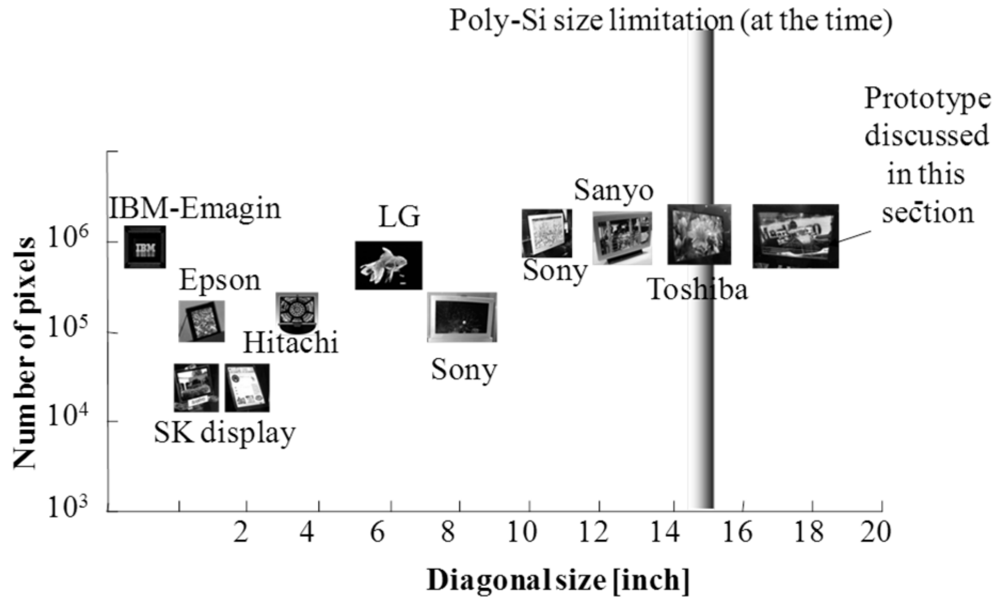


Fig. 11 Active-matrix OLED display size limitation due to poly-Si processing (As of year 2003. [23])

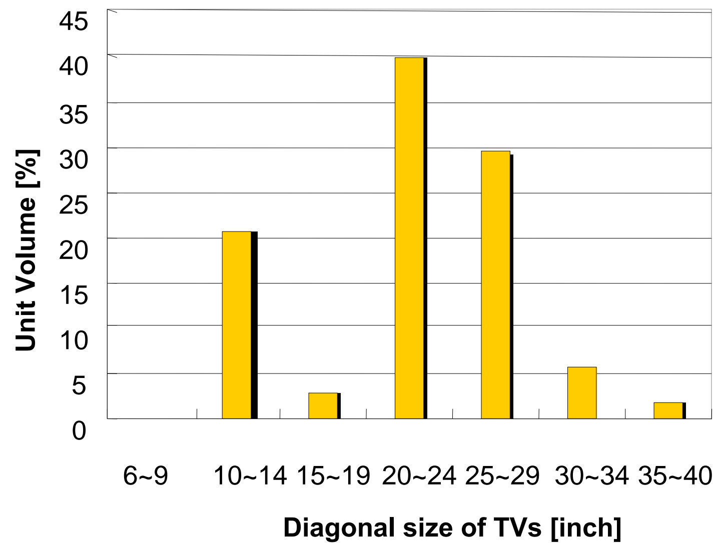


Fig. 12 CRT television shipment (As of year 2003)

2.2 OLED design for over-20-inch display

2.2.1 TFT performance requirement for large OLED television and efficiency improvement by phosphorescent device

2.2.1.1 Estimation of a-Si TFT degradation

As discussed, ELA-LTPS technology has size limit and expensive. As an alternate TFT backplane technology, if amorphous silicon TFT can drive an OLED display, it would bring much cost benefit, because amorphous silicon TFT has been used in TFT-LCD for many years, so many manufacturing line after depreciation are prevalent worldwide with mature low cost fabrication technology, such as 4 mask processing method. Then the question is if amorphous silicon TFT has enough performance to drive an OLED display. Driving capability and reliability of amorphous silicon TFT are investigated.

When OLED device current efficiency is η and sub-pixel pitch (Fig. 13) of a display is a, the electric current to drive the pixel can be described as,

$$I_{pixel} = \frac{B_{MAX} \times 9a^2}{\eta} \quad \text{(Eq.1)}$$

(B_{MAX} : Display maximum luminance, I_{pixel} : Maximum current that flows through OLED device in a pixel)

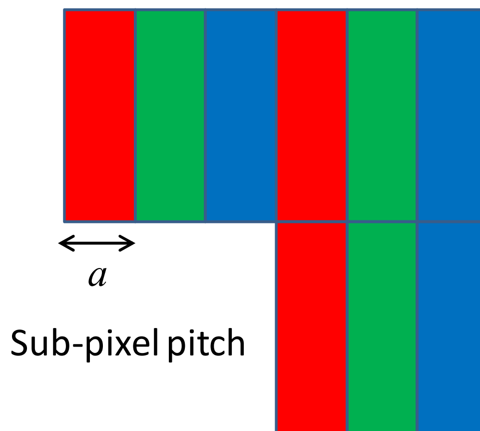


Fig. 13 Definition of a sub-pixel pitch

TFT current can be described as following using Gradual-Channel Approximation.

$$I_{pixel} = \frac{W}{2L}\mu C_{OX}(V_{GS} - V_{TH})^2 \quad \text{(Eq.2)}$$

(W: Channel width of driver TFT, L: channel length of driver TFT, μ: field-effect mobility of TFT, C_{OX}: channel capacitance of TFT, V_{GS}: gate voltage of TFT, V_{TH}: threshold voltage of TFT)

$$W = \frac{18 B_{MAX} a^2 L}{\eta \mu C_{OX} (V_{GS} - V_{TH})^2} \quad \text{(Eq.3)}$$

As multiple TFTs and capacitors must be allocated in a sub-pixel region , it can be assumed that TFT channel width W needs to be shorter than the sub-pixel pitch. Especially, large inter-electrode overlap leads to the reduction of production yield due to inter-layer leakage, smaller TFT should be better. Therefore, W can be regarded as the maximum channel width limit for realistic panel design. (Assumption-1)

If the dielectric constant of TFT gate insulator is 6.5, $\varepsilon_O = 8.854 \times 10^{-8}$[F/cm] and the gate insulator thickness is 400[nm], channel capacitance can be calculated as following.

$$C_{OX} = \varepsilon_r \varepsilon_O \frac{1}{d_{OX}} = 6.5 \times 8.854 \times 10^{-8} \frac{1}{400 \times 10^{-7}} = 1.44 \times 10^{-2} [F/cm^2] \quad \text{(Eq.4)}$$

If B_{max}=500[cd/m^2], L=5[μm], η=10[cd/A], μ=1.0[cm^2/Vsec] (amorphous silicon TFT assumption), V_{GS}=12[V], V_{TH}=3[V], relationship between required channel width and sub-pixel pitch can be shown as Fig. 14 using Eq.3. If required channel width (W) must be smaller than sub-pixel pitch (a), sub-pixel pitch must be below 200μm to drive with this condition. Fig. 15 shows sub-pixel pitch of various size and various resolution. For example, If the maximum sub-pixel pitch is 200μm, amorphous silicon TFT can drive up to 30-inch in 720p resolution case.

,

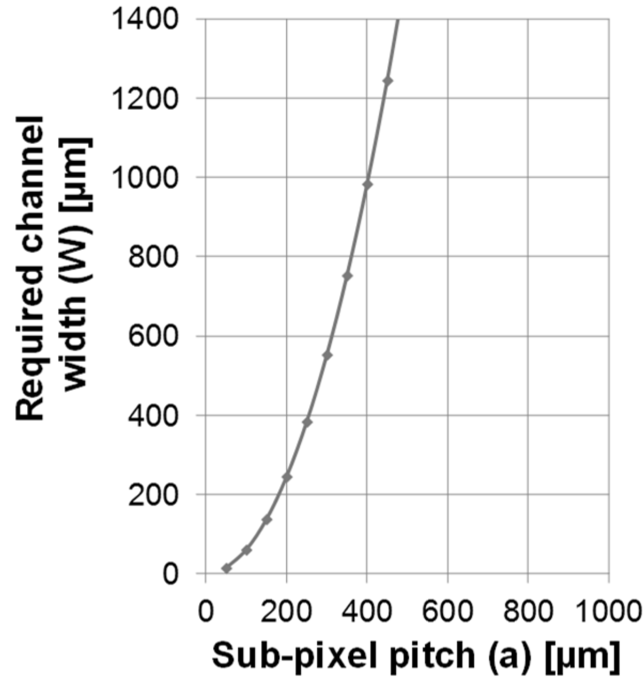


Fig. 14 Relationship between required channel width and sub-pixel pitch

Diagonal size	720p (1280/720)	1080i/p (1920/1080)	2160p (3840/2160)	4320p (7680/4320)	8640p (15360/8640)
15"	86	58	29	14	7
20"	115	77	38	19	10
25"	144	96	48	24	12
30"	173	115	58	29	14
35"	202	135	67	34	17
40"	231	154	77	38	19
45"	259	173	86	43	22
50"	288	192	96	48	24
55"	317	211	106	53	26
60"	346	231	115	58	29
65"	375	250	125	62	31
70"	404	269	135	67	34
75"	432	288	144	72	36

Fig. 15 Subpixel pitch [μ m]of various display size and format

According to this calculation, low mobility TFT like amorphous silicon can drive 30" 720-p HDTV display. However, in reality, amorphous silicon TFT causes reliability issue under electrical stress like Fig. 16, which reduces the driving capability. Fig. 17 shows the current reduction cause analysis during constant voltage stress. (Stress: V_{GS}=10V, V_{DS}=2V) It clearly shows that main cause of current reduction of amorphous silicon TFT under this driving stress is positive V_{TH} shift and mobility reduction is almost negligible.

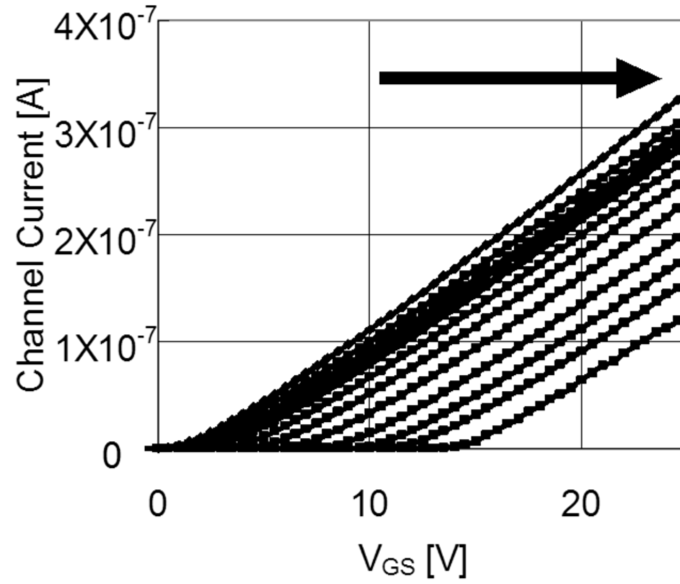


Fig. 16 Threshold voltage shift of amorphous silicon TFT

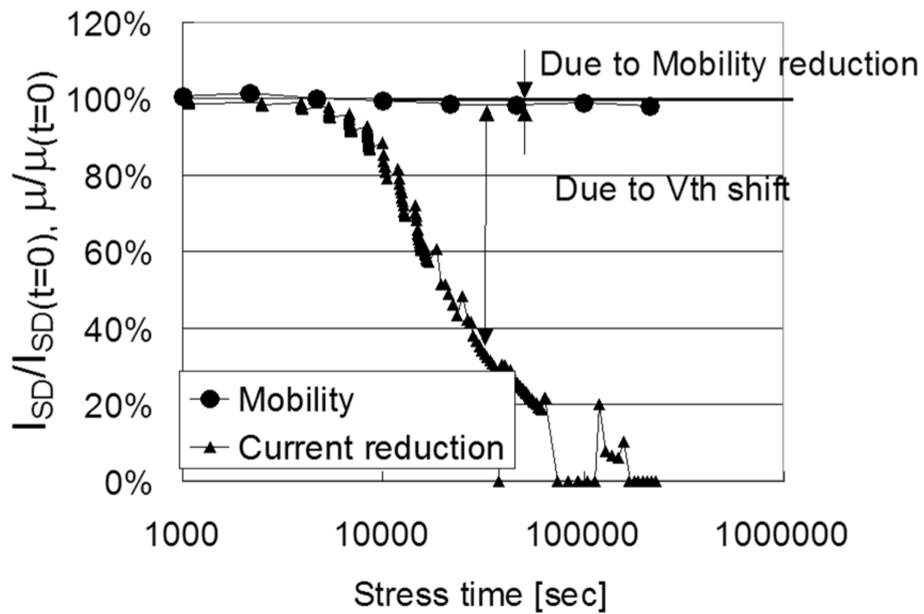


Fig. 17 TFT current reduction

After stress, V_{GS}-V_{TH} becomes gradually smaller than the initial condition, which causes smaller current supply. Therefore, required channel width to drive a sub-pixel OLED becomes wider as shown in Fig. 18.

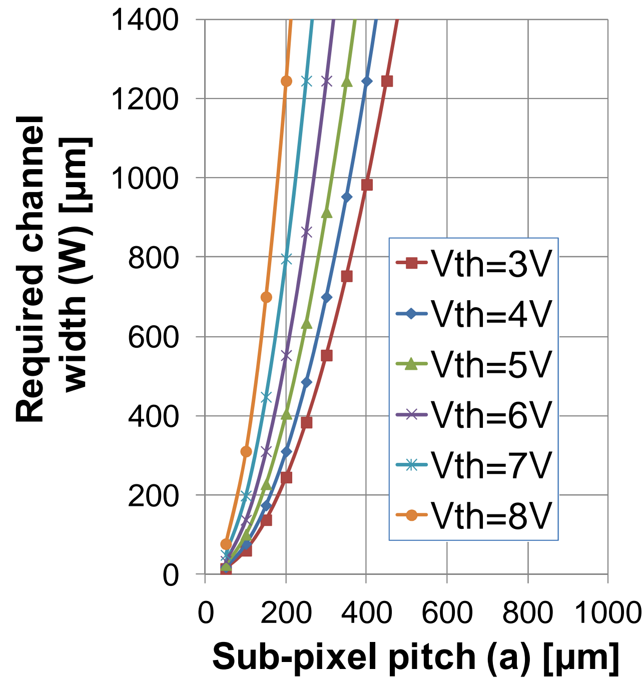


Fig. 18 Required TFT channel width with various V_{TH} condition

According to Assumption-1 (*W* can be regarded as the maximum channel width limit for realistic panel design), 20" HDTV(720p, 115 μ m sub-pixel width) can be driven if V_{TH} is below 6V (115 μ m sub-pixel pitch in Fig. 18 on "V_{TH}=6V" has about 115 μ m "Required channel width".), which means about 3V V_{TH} shift when initial V_{TH} is 3V. Fig. 19 shows the V_{TH} shift of amorphous silicon TFT under V_{GS}=10V, V_{DS}=2V. It is clear that V_{TH} shift of amorphous silicon TFT reaches "3V limit" in 150 hours, obviously too short lifetime to drive an OLED display. Also this kind of V_{TH} shift causes image sticking issue (Also called as "Differential Aging".) like Fig. 20. Then it is necessary to consider how to relax the electrical stress in a TFT so that the lifetime can be extended. There are several approaches discovered to reduce the V_{TH} shift, as reported in this study. Combining multiple approaches, stable amorphous silicon TFT driving suitable for AMOLED TV application might be possible.

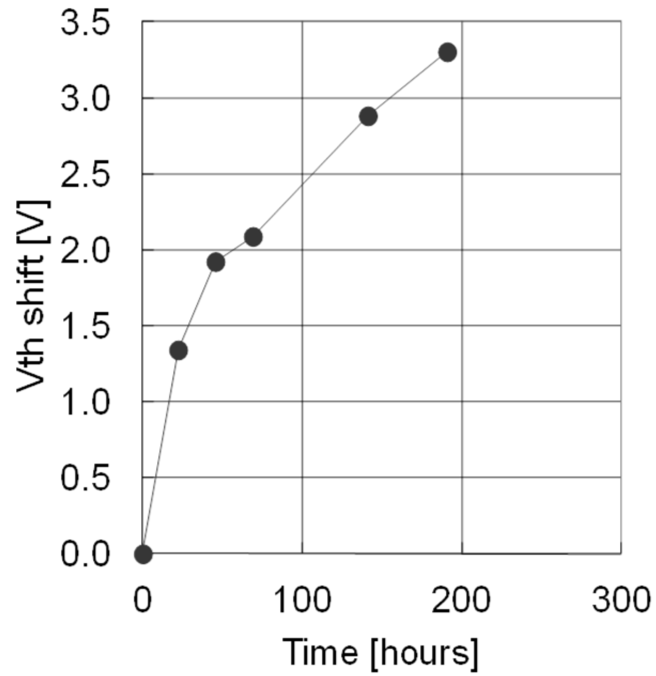


Fig. 19 VTH shift of amorphous-silicon TFT (Stress: V_{GS}=10V, V_{DS}=2V)

Fig. 20 Image sticking after long driving stress

2.2.1.2 Stress relaxation by TFT driving

Fig. 21 shows V_{TH} shift of amorphous silicon TFT under various driving stress. (BTS: Bias Temperature Stress test) TFT current can be described as Eq.2 when

$V_{DS} > V_{GS} - V_{TH}$ (Saturation region operation) and as following when $V_{DS} < V_{GS} - V_{TH}$ (Linear region operation).

$$I_{pixel} = \frac{W}{L}\mu C_{OX}\left\{(V_{GS} - V_{TH})\cdot V_{DS} - \frac{V_{DS}^{\ 2}}{2}\right\} \quad \text{......................(Eq.5)}$$

V_{DS}=2V in Fig. 21 should be in linear region and V_{DS}=10V and 15V should be in saturation region, so $I_{VDS=2V} < I_{VDS=10V} \cong I_{VDS=15V}$. In reality, TFT current shows monotonous increase as shown Fig. 22, as the V_{DS} is increased. However V_{TH} shift in Fig. 21 shows opposite trend as to the driving current. It is a very interesting situation, as large driving current (V_{DS}=15V) shows the least V_{TH} shift, while the smallest case (V_{DS}=2V) shows the largest V_{TH} shift. This trend is very suitable for delivering large driving current to OLED device, while keeping the TFT stress as minimum.

To account for this interesting trend of a-Si TFT degradation, it would be reasonable how the electric potential of three electrodes in a TFT affects the weakest point of a TFT. It has been reported widely that the most major mechanism of a-Si TFT degradation is due to charge trapping in gate insulator and channel/gate insulator surface. [24][25][26][27]

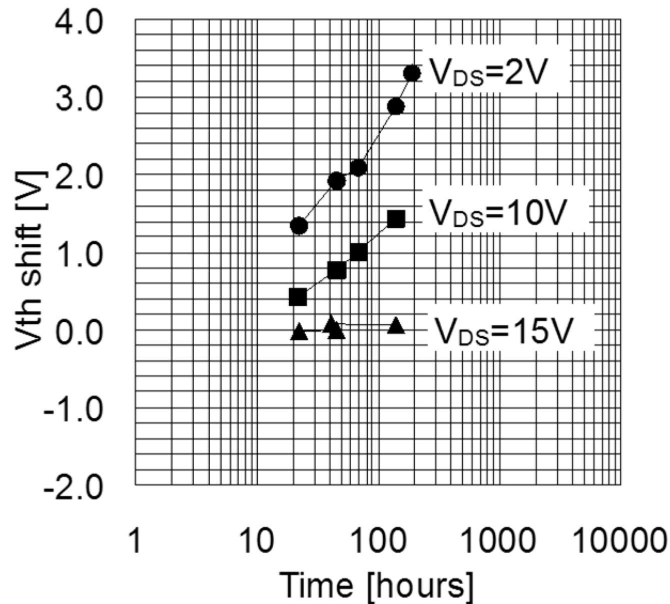


Fig. 21 V_{TH} shift of amorphous silicon TFT under various V_{DS} stress

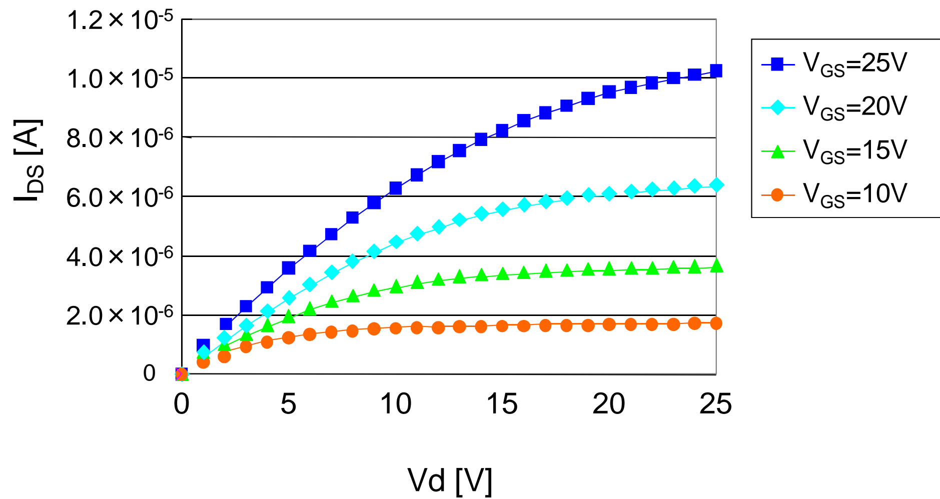


Fig. 22 Transfer characteristics of amorphous silicon TFT

In linear region, such as V_{GS}=10V, V_{DS}=2V case, electrical flux line is from gate electrode to both source and drain electrode. As a result, electrons in the TFT channel are injected to gate insulator regardless of near-source or near-drain region. (Fig. 24)

On the other hand, in deep saturation region, such as V_{GS}=10V, V_{DS}=15V case, situation of electric force line is completely different between source electrode and drain electrode. In near the source electrode side, electric force line is from gate electrode to source electrode, just like linear region. However, in near the drain electrode side, electric force line is from drain to gate electrode and it is causing the loss of TFT channel near the drain electrode. (Fig. 23)

Therefore, electrons near the drain region are collected by drain electrode by means of space-charge-limited conduction (SCLC) mechanism without injection into gate insulator. (Fig. 25) It can be assumed that the stability increase of a-Si TFT is due to the reduction of charge trapping near the drain region.

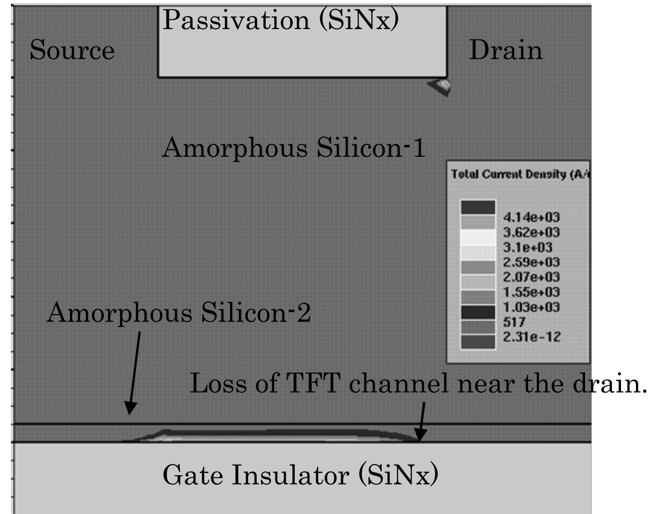


Fig. 23 Device simulation of back-channel-type amorphous silicon TFT at V_{GS}=10V, V_{DS}==10V, V_{BACK}=0V

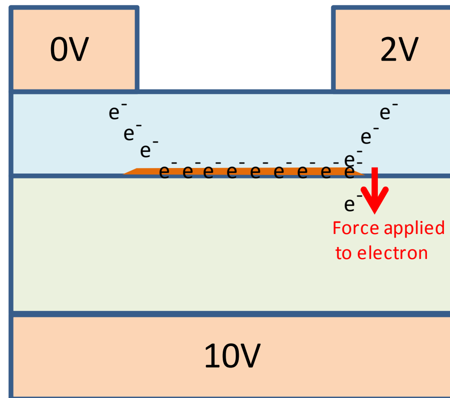


Fig. 24 Electron injection to the silicon/gate insulator interface in linear region operation

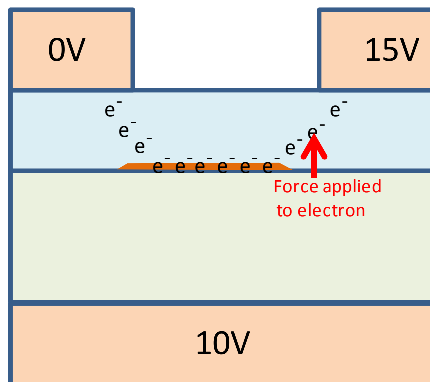


Fig. 25 Electron injection to the silicon/gate insulator interface in saturation region operation

It was revealed that the driving condition changes the degradation behavior of amorphous silicon TFT so much. Then the degradation may be further reduced by means of other driving technique as well. Then various AC driving (Fig. 26) was tried for the amorphous silicon reliability testing. [28] (In all the driving condition, average OLED current is kept the same regardless of the pulse width and the pulse shape.) The conditions used for the experiment is list in Table 2. Fig. 27 shows the result of the AC BTS test. All the AC BTS test result fits with the same curve, while DC BTS test result shows larger V_{TH} shift value. It means that DC BTS measurement is overestimating the V_{TH} shift by about twice. It is reported that the trapped charge is detrapped when the voltage stress is stopped [29]. The reduction of V_{TH} shift by AC stress as compared with DC stress can be explained by the detrapping of electron from the semiconductor / gate insulator interface as shown in Fig. 28.

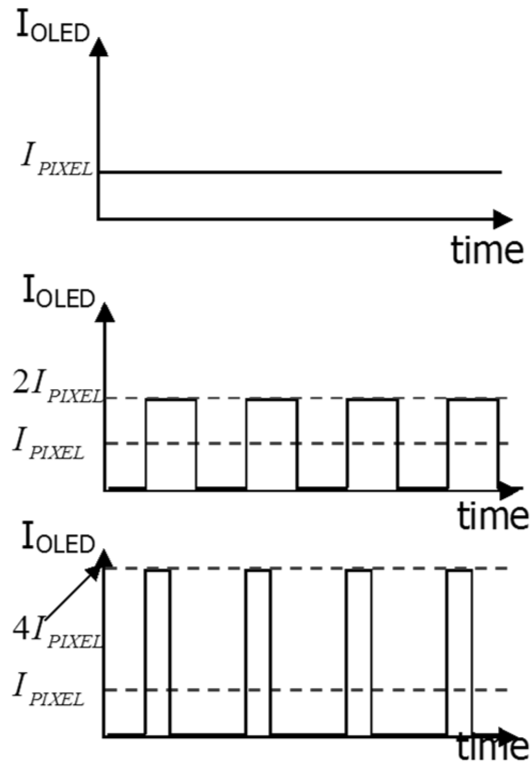


Fig. 26 Various duty driving method

Condition	Electrode	Voltage	Duty
Condition-1	V_{GS}	10V	DC (Duty=100%)
	V_{DS}	10V	DC (Duty=100%)
Condition-2	V_{GS}	10V/0V	Duty=50% (60Hz)
	V_{DS}	10V	DC (Duty=100%)
Condition-3	V_{GS}	10V/0V	Duty=50% (60Hz)
	V_{DS}	10V/0V	Duty=50% (60Hz)
Condition-4	V_{GS}	10V/0V	Duty=25% (60Hz)
	V_{DS}	10V/0V	Duty=25% (60Hz)

Table 2 TFT driving condition used for experiment

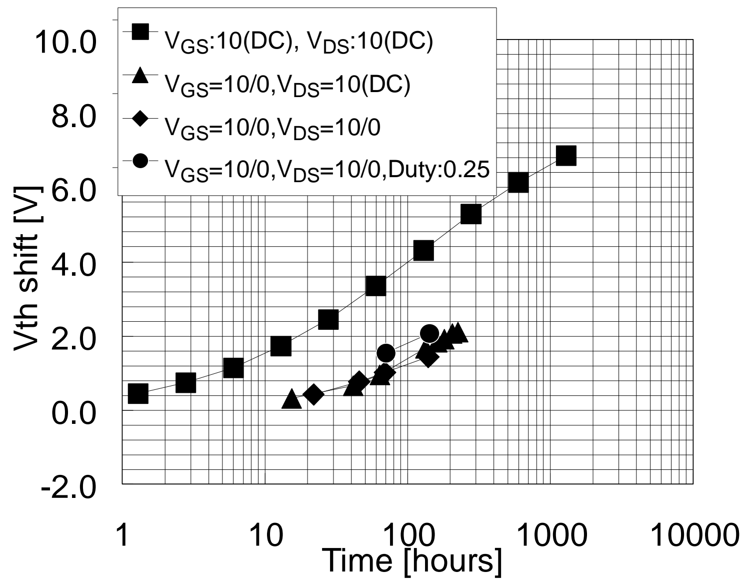


Fig. 27 TFT V_{TH} shift dependence on the gate and drain electrode duty ratio

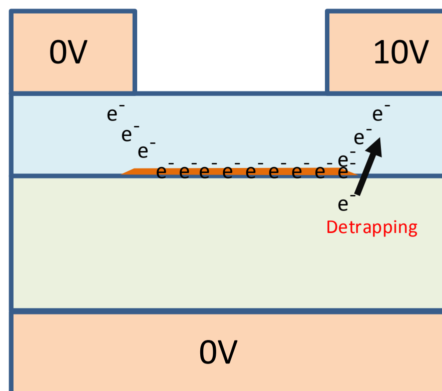


Fig. 28 Charge detrapping due to AC driving

It was also investigated how drain-source swapping affects the V_{TH} shift. Initially, it was intended to extend the lifetime of a TFT by reducing the time for an electrode to be used as a drain. However, as can be seen in Fig. 29, the V_{TH} shift of electrode swapping actually increases the V_{TH} shift.

Fig. 30 shows the situation of the TFT in saturation region when $V_{Source\text{-}Drain}$=10V and $V_{Gate\text{-}Source}$=10V. Near drain electrode, current is dominated by SCLC mechanism as discussed in Fig. 25. For the analysis of swapping, source-side operation should be also investigated. TFT channel region can be expressed as the serial connection of multiple ideal TFTs as shown in Fig. 30. Multiple TFTs are labeled as n=1,2,3,4,... from the near source electrode side. At t=0 second, electron came from source electrode will use the shortest path to the a-Si/gate insulator

interface and flow from n=1 to n_{FINAL}. In the situation, as the electron near the source electrode gets the electrical force toward gate insulator, some of the electron will be trapped in the interface between a-Si and gate insulator, which will generate higher V_{TH} for $TFT_{n=1}$. When V_{TH} for $TFT_{n=1}$ becomes large, the electron injected from source electrode will try to avoid flowing through $TFT_{n=1}$, which has higher impedance than others and starts conduction from $TFT_{n=2}$. Then electron trapping of $TFT_{n=2}$ happens and that will make $TFT_{n=2}$ higher impedance. Then the electron injected from source electrode will try to avoid flowing through $TFT_{n=1}$ and $TFT_{n=2}$, which have higher impedance and starts conduction from $TFT_{n=3}$. This trend continues to happen for n=1,2,3,4,5,...., then as the injected electron can avoid going through high impedance region. That is why source-region-derived V_{TH} shift is not observed for DC operation. However, for the source-drain swapping operation, accumulated electron in near-source region before the swapping causes the voltage offset in the saturation region after the electrodes are swapped.

Therefore, amorphous silicon TFTs show larger V_{TH} shift when source-drain electrodes are swapped than DC operation.

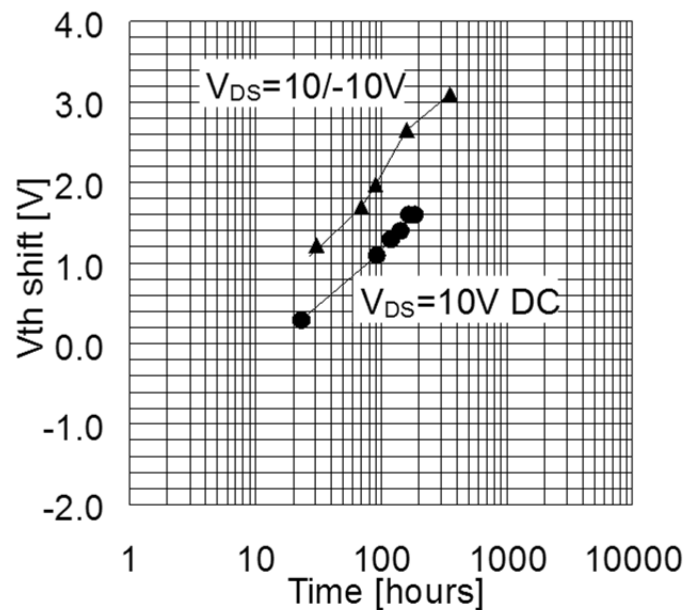


Fig. 29 Effect of drain-source swapping for V_{TH} shift

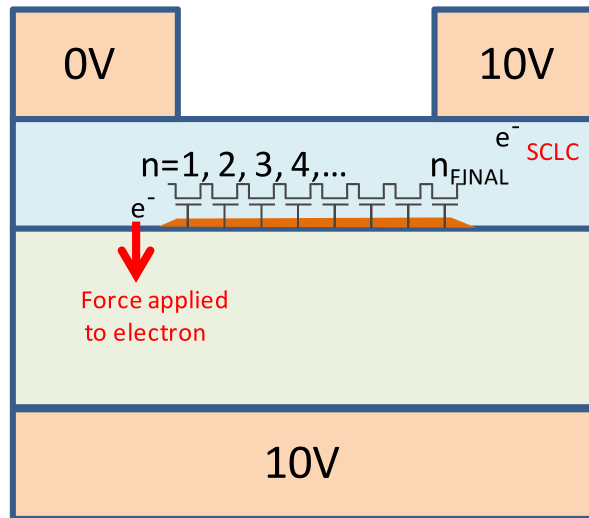


Fig. 30 Situation near source electrode in saturation region operation

According to the AC driving stress experiment, the following conclusion can be made.

1) TFT should be driven in deep saturation region as possible
2) Gate pulse should be driven by AC manner
3) Source/drain role swapping should be avoided

Taking those three into account, charge trapping can be suppressed and the V_{TH} shift can be minimized.

2.2.1.3 Stress relaxation by TFT structure

Another approach to reduce the instability of amorphous silicon TFT is to avoid the current concentration in the TFT channel. Fig. 31 shows the 3-dimensional device simulation result of back-channel-etch type amorphous silicon TFT. It clearly shows that the large portion of current is flowing at the edge of amorphous silicon channel region. This happens because TFT structure is not uniformly along the TFT-width direction. To circumvent this situation, concentric TFT may be able to show lower instability than the conventional structure. Fig. 32 shows the result of positive BTS test. (V_{GS}=V_{DS}=10V) Concentric TFT clearly shows smaller V_{TH} shift than conventional TFT. The V_{TH} shift at 200 hours is about 43% reduction by using concentric electrode arrangement. The improvement is probably due to the lack of discontinuous region in the amorphous silicon channel.

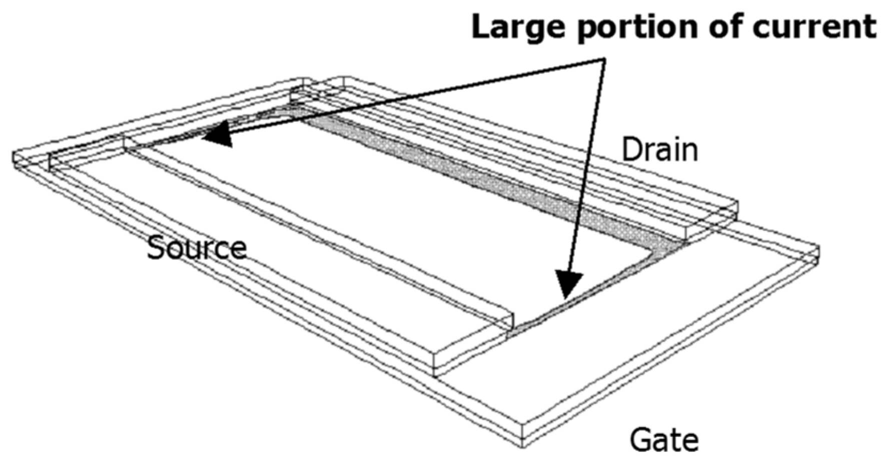


Fig. 31 Current concentration simulation using ATLAS device simulator

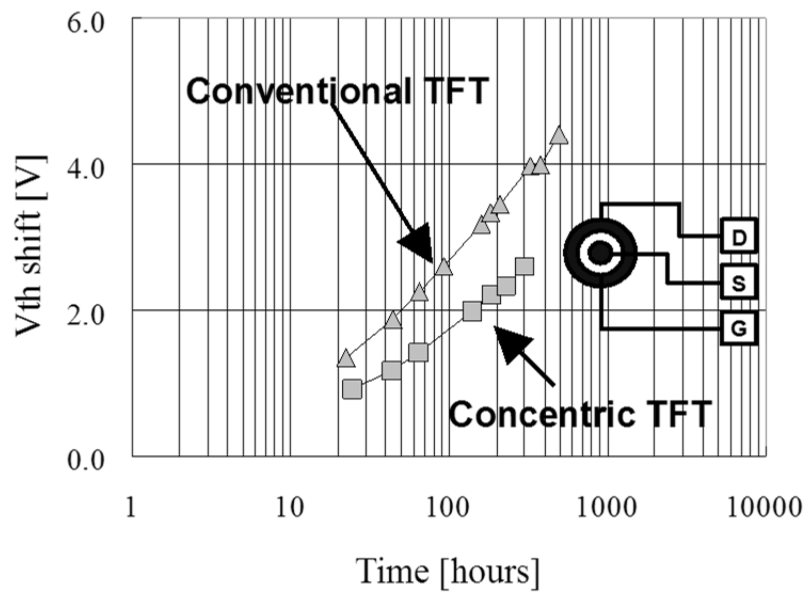


Fig. 32 Comparison of V_{TH} shift between concentric TFT and conventional TFT

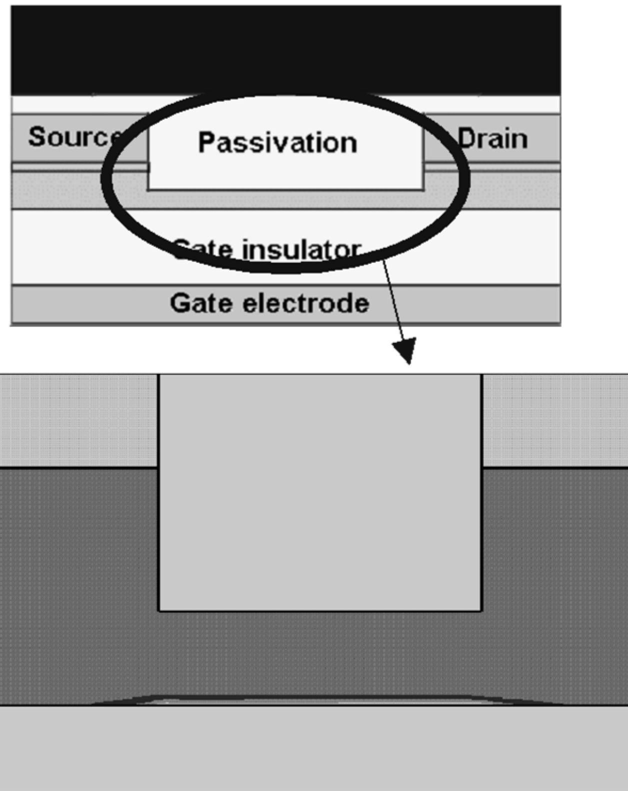


Fig. 33 Current concentration in conventional TFT

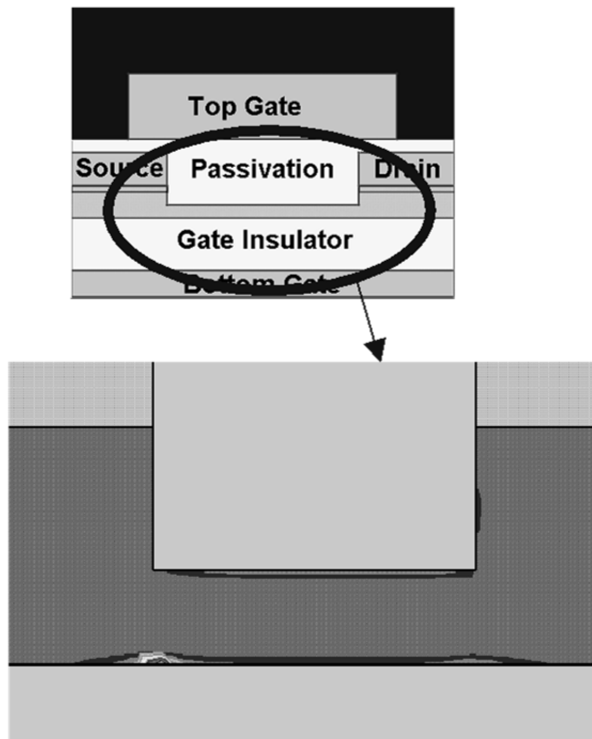


Fig. 34 Dual-channel TFT by applying two gate electrodes to top and bottom

Another approach to reduce the current concentration in amorphous silicon channel is to have multiple TFT channel to deliver the electric current to OLED devices. Normally, TFT has only one gate electrode in either bottom of the TFT device or top. (Fig. 33) Former case is called bottom-gate TFT and latter is called top-gate TFT. If bottom-gate TFT and top-gate TFT are combined, namely if a TFT has two gate electrode on top and bottom, there will be dual channel created in the channel region. If two current path exists, the stress of amorphous silicon TFT would be relaxed. Fig. 35 shows the comparison of V_{TH} shift between conventional TFT and dual-channel TFT. V_{TH} shift is reduced by over 60% with dual-channel TFT device.

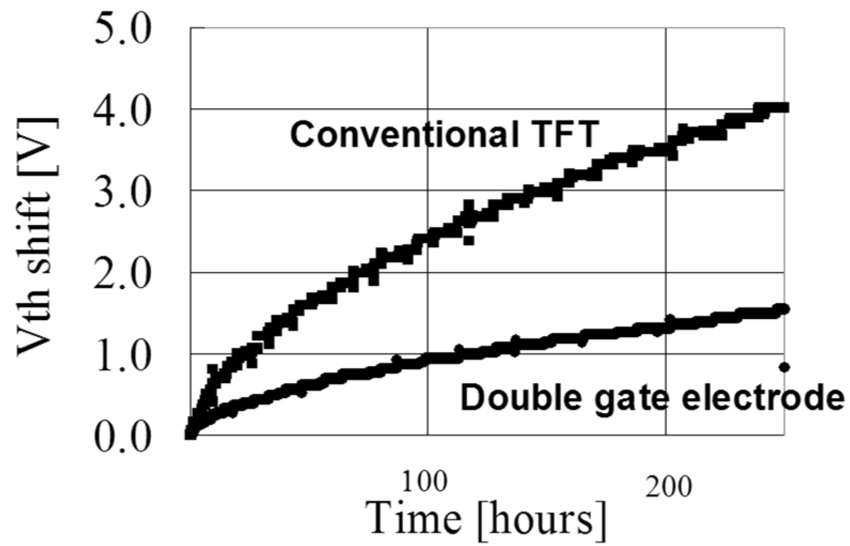


Fig. 35 V_{TH} shift reduction by dual-channel TFT structure

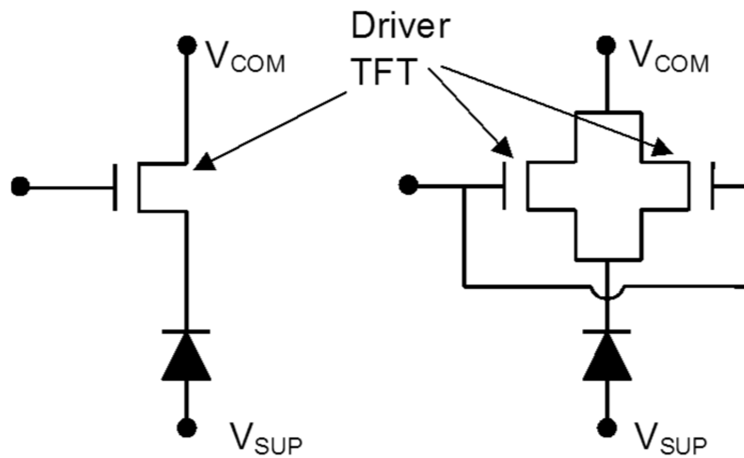


Fig. 36 Conventional TFT-OLED connection (Left) and TFT-OLED connection using dual-channel TFT

From Eq.2, TFT current flows in the conventional TFT-OLED connection (Fig. 36 left) can be described as,

$$I_{conventional} = \frac{W}{2L}\mu_{BOT}C_{OX,BOT}(V_{GS} - V_{TH,BOT})^2 \quad \text{(Eq.6)}$$

, where μ_{BOT} is the mobility of bottom gate TFT, $C_{OX,BOT}$ is the gate insulator

capacitance of bottom gate TFT and $V_{TH,BOT}$ is the threshold voltage of bottom gate TFT.

In the case of dual-channel TFT, which has two channel on top and bottom of the semiconductor layer (Fig. 36 right), TFT current can be described as,

$$I_{dual} = \frac{W}{2L}\{\mu_{BOT}C_{OX,BOT}(V_{GS} - V_{TH,BOT})^2 + \mu_{TOP}C_{OX,TOP}(V_{GS} - V_{TH,TOP})^2\}$$

, where μ_{TOP} is the mobility of top gate TFT part, $C_{OX,TOP}$ is the gate insulator capacitance of top gate TFT and $V_{TH,TOP}$ as the threshold voltage of top gate TFT.

If current is flown to both channel, TFT current is relaxed by

$$\frac{\mu_{BOT}C_{OX,BOT}(V_{GS} - V_{TH,BOT})^2}{\mu_{BOT}C_{OX,BOT}(V_{GS} - V_{TH,BOT})^2 + \mu_{TOP}C_{OX,TOP}(V_{GS} - V_{TH,TOP})^2}$$ times.

If we use the actual condition used in Fig. 35, that is $C_{OX,BOT} = 2.12 \times 10^{-8}[F/cm^2]$、$C_{OX,TOP} = 1.44 \times 10^{-8}[F/cm^2]$, the following value can be calculated.

$$\frac{\mu_{BOT}C_{OX,BOT}(V_{GS} - V_{TH,BOT})^2}{\mu_{BOT}C_{OX,BOT}(V_{GS} - V_{TH,BOT})^2 + \mu_{TOP}C_{OX,TOP}(V_{GS} - V_{TH,TOP})^2} = 0.60 \quad \text{(Eq.7)}$$

Therefore, the current stress would become 0.60 times and, in terms of gate voltage, the stress would become $\sqrt{0.60} = 0.77$ times. Fig. 35 shows V_{TH} shift less than 40% and is much smaller than 0.60 or 0.77. This may be due to the stress relaxation by 3D distribution of channel.

This technique to reduce the instability of TFT is used in actual AMOLED television product. [30]

Though dual-channel TFT reduces the V_{TH} shift significantly, it requires many process steps to fabricate it. Process step reduction to fabricate the dual-channel TFT with reduced cost is described in 2.2.2. [31]

2.2.1.4 Reliability improvement by TFT process

Another possibility to enhance the stability of TFT is to change the processing condition of amorphous silicon TFT. Fig. 37 shows an example of amorphous silicon TFT performance with various CVD conditions. V_{TH} shift becomes larger with improved mobility. (This can be interpreted that the mobility increase causes charge flow increase, which result in the probability increase for a charge to collide with Si bonds.) To make large AMOLED display happen, both high mobility and

high stability must happen altogether, so the recipe tuning like Fig. 37 is not appropriate to be used for AMOLED backplanes.

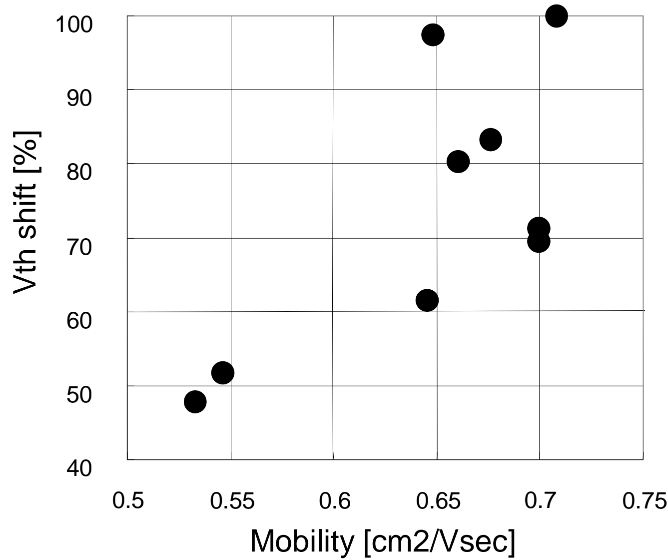
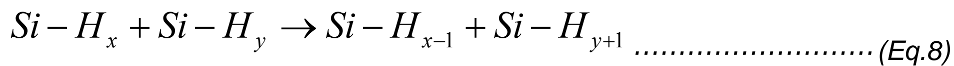


Fig. 37 An example of amorphous silicon TFT performance with various CVD conditions

One possibility to have both high mobility and high stability is to use microcrystalline silicon TFT. Microcrystalline silicon can be formed with the same CVD equipment as amorphous silicon, which is widely used in display manufacturing line, using LBL (Layer-By-Layer) method reported by E.Srinivasan et al. [32]

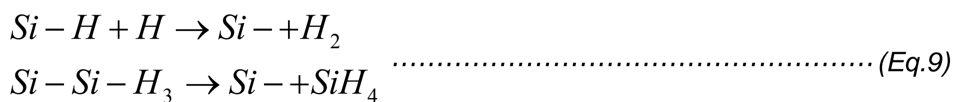
G.Parson reports that following two hydrogen extraction processes are important for fabricating amorphous silicon with good conductivity. [33]

Reaction with hydrogen number change bonded to Si



$$Si-H_x+Si-H_y \rightarrow Si-H_{x-1}+Si-H_{y+1} \quad \text{(Eq.8)}$$

Hydrogen extraction and etching by hydrogen atom



$$\begin{aligned} &Si-H+H \rightarrow Si-+H_2 \\ &Si-Si-H_3 \rightarrow Si-+SiH_4 \end{aligned} \quad \text{(Eq.9)}$$

E.Srinivasan reports that further hydrogen extraction leads to phase transition from amorphous silicon phase to microcrystalline. [32] (Fig. 38)

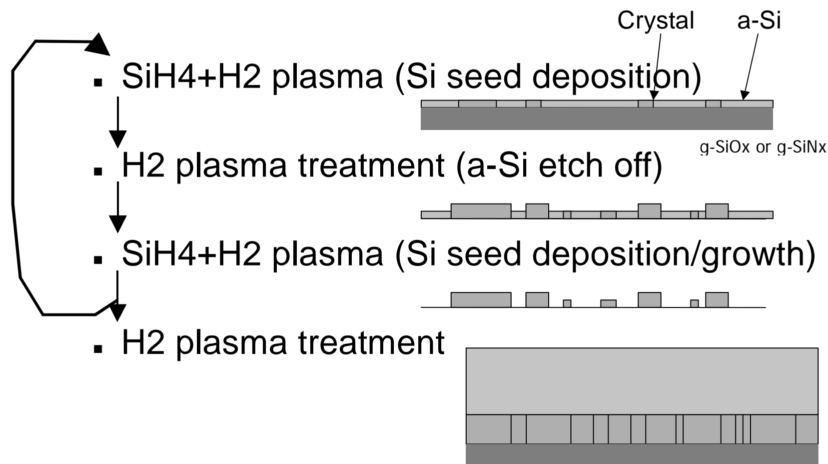


Fig. 38 Conventional LBL deposition method

Roca I Cabarocas [34] reports high stability microcrystalline Si TFT with 1/10th V_{TH} shift than amorphous silicon TFTs. (Fig. 39)

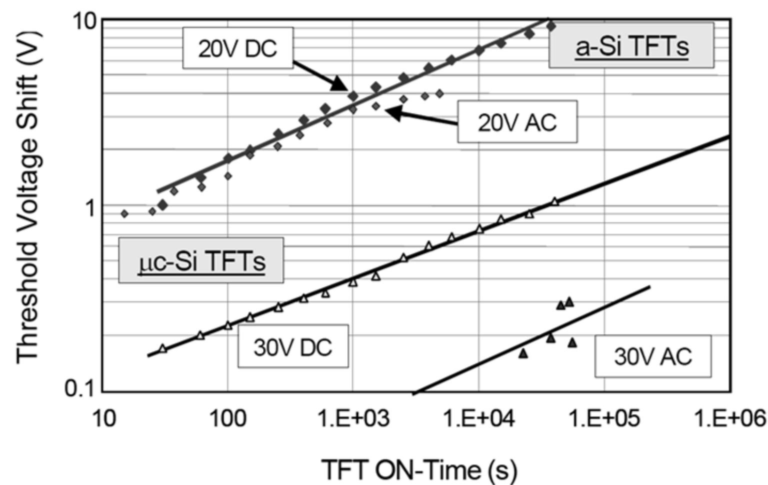


Fig. 39 Comparison of stability between amorphous silicon and microcrystalline Si TFT at 60° C by P. Roca i Cabarrocas et al.

R.B.Wehrspohn gives explanation for the small V_{TH} shift of microcrystalline Si TFT that microcrystalline Si has lower "Attempt Escape Frequency", namely smaller collision cross-section. [35]

Though microcrystalline Si has attractive stability, there is a large issue in the actual mass production use. Basically, LBL method is composed of the deposition + etching iteration, so the total deposition rate is very low compared with conventional amorphous silicon channel layer formation, such as 1/10, which means

the manufacturing line can produce only 1/10 number of panel. Also, process margin is very narrow with LBL method to obtain good performance. Fig. 40 shows a typical transfer characteristics of microcrystalline Si TFT. High off current, large sub-threshold slope and low mobility are observed. These are attributed to unconditioned amorphous silicon in microcrystalline Si grain boundary. [36]

It was investigated how to make both high manufacturability and high performance happen. To obtain enough band bending, channel layer thickness must not be too thin. However thick channel layer film by microcrystalline causes poor throughput. Therefore, in this study, microcrystalline Si / amorphous Si dual layer channel was employed. Band bending should be able to be achieved mostly by amorphous silicon and large conduction in channel should be able to be made by microcrystalline Si beneath the amorphous Si layer. [22]

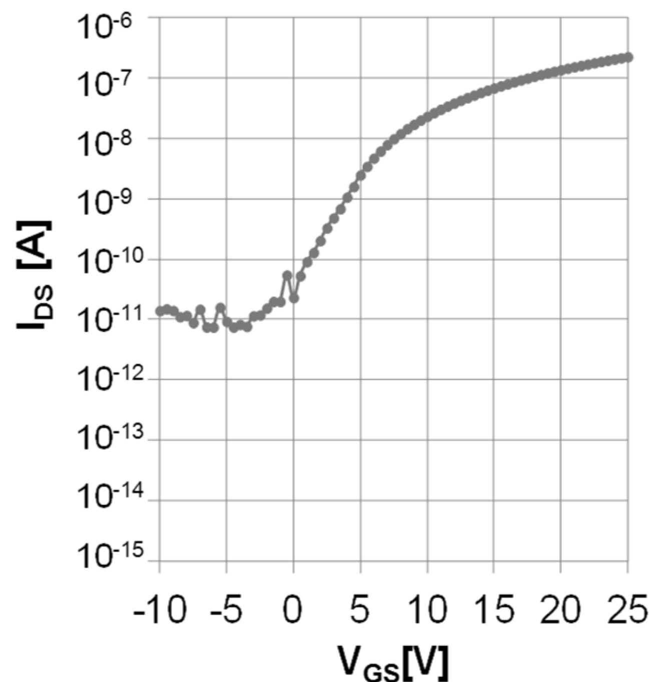


Fig. 40 Typical microcrystalline Si TFT transfer characteristics made by LBL method

Fig. 41 shows the TFT structure used for the experiment. After fabricating aluminum gate metal by DC sputtering and patterning, 400nm SiN_x gate insulator is deposited by AKT-1600 CVD (Chemical Vapor Deposition) Subsequent active layer is deposited in the same CVD chamber, 5nm~10nm microcrystalline Si by LBL method, followed by the amorphous Si deposition using SiH_4+H_2 gas.

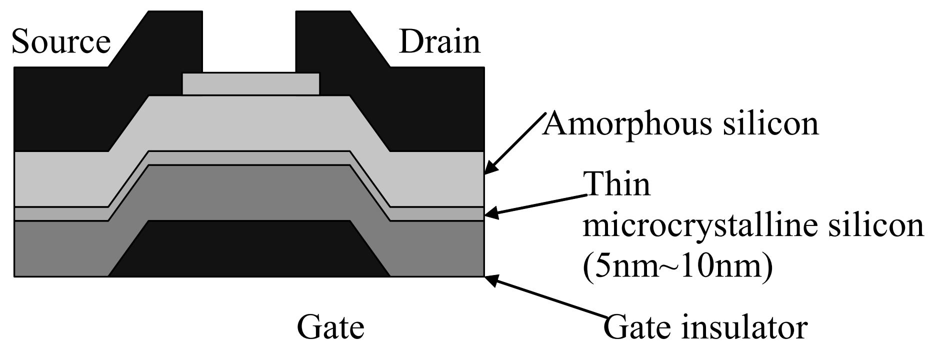


Fig. 41 TFT structure with amorphous Si / microcrystalline Si dual layer channel

Fig. 42 shows the transfer characteristics difference between amorphous Si TFT and microcrystalline / amorphous Si dual-layer-channel TFT. Off current is reduced almost one order of magnitude due to the thickness offset effect, compared with Fig. 40, however having low mobility, poor sub-threshold swing and large V_{TH}, not suitable for AMOLED display driving. To improve the situation, microcrystalline film deposition condition must be optimized.

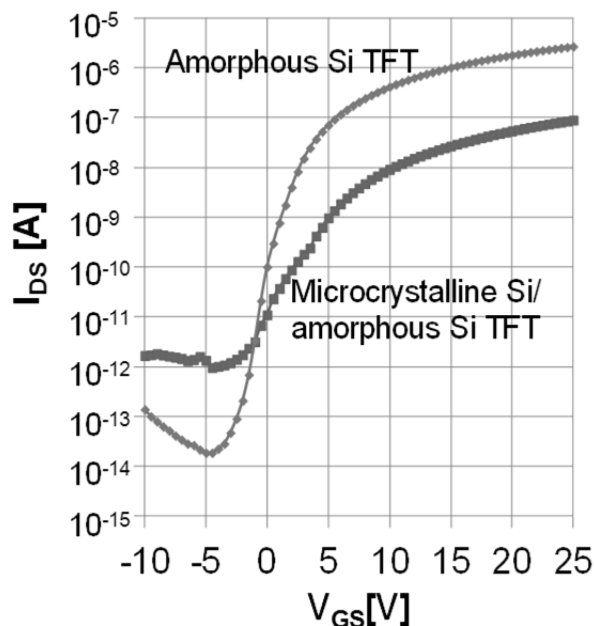


Fig. 42 Transfer characteristics of amorphous silicon TFT vs. microcrystalline Si / amorphous Si dual layer channel TFT

Using conventional LBL method, amorphous Si is converted to microcrystalline Si

by means of hydrogen plasma. However, it also means that amorphous silicon located in the grain boundary of microcrystalline Si is subjected to the plasma damage, which can deteriorate the conductive performance. Sufficient plasma etching capability and minimal plasma damage must co-existent for high performance.

Also high quality microcrystalline film with minimal defect density must be obtained. It is known that SiH_2* deposition species generates particles by forming polymer chain when it meets with other molecules and radicals. For the best quality microcrystalline film, polymer chain growth must be refrained by reducing the probability for a reactive molecule to meet with other molecules.

In this experiment, SiH_4 gas was supplied intermittently so that low enough collision probability of deposition species is made.

Residual time of deposition species can be expressed as following. [37]

$$\tau = \frac{V}{S} = \frac{PV}{PS} = \frac{PV}{Q} \quad \text{(Eq.10)}$$

, where V as the volume, S as the conductance, Q as the gas flow per second.

Using this equation, the residual time τ for this deposition system is 4.03seconds. If SiH_4 gas supply per cycle is shorter than τ, the deposition would be made in the gas phase.

When SiH_4 gas is diluted by H_2, partial pressure of Si deposition species can be described as,

$$P_{Si} = \frac{Q_{SiH4} t_{SiH4}}{Q_{SiH4} t_{SiH4} + Q_{H2} t_{H2}} P \quad \text{(Eq.11)}$$

, where P_{Si} as partial pressure of Si deposition species, Q_{SiH4} as the SiH_4 gas flow, t_{SiH4} as the SiH_4 supply period, Q_{H2} as the H_2 gas flow and t_{H2} as the H_2 gas supply period.

$$n_{Si} = \frac{P_{Si} V}{RT} = \frac{Q_{SiH4} t_{SiH4} PV}{(Q_{SiH4} t_{SiH4} + Q_{H2} t_{H2}) RT} \quad \text{(Eq.12)}$$

On the other hand, mean free path can be described as,

$$\lambda = \frac{1}{\sqrt{2}\pi d^2 n} = \frac{(Q_{SiH4} t_{SiH4} + Q_{H2} t_{H2}) RT}{\sqrt{2}\pi d^2 n Q_{SiH4} t_{SiH4} PV} = 1.49 \times 10^{-3} [m] \quad \text{(Eq.13)}$$

, where λ as the mean free path of Si deposition species, d as the molecular diameter, n as amount of gas.

When H_2 gas flow is kept for residual time τ, average mean free path can be

described as,

$$\lambda = 1.49 \times 10^{-3}[m] \quad \text{(Eq.14)}$$

With this condition, Si deposition species collides 369 times until it is transported to the substrate end and is exhausted. There were no particle nor inter-layer short defect was detected, so it can be interpreted as an enough dilution condition.

Condition	SiH_4 flow period [sec]	H_2 etching period [sec]
Condition-1	t_1 (<4.03 second)	t_1
Condition-2	$2 \times t_1$	$2 \times t_1$
Condition-3	$4 \times t_1$	$4 \times t_1$
Microcrystalline Si/a-Si	$8 \times t_1$	$8 \times t_1$

Table 3 Active layer deposition condition used for the experiment

Table 3 shows the deposition condition of Si active layer. Deposition period (=SiH_4 flow period) and H_2 etching are kept the same for all the conditions. Shorter SiH_4 flow would decrease the probability for a deposition species to meet each other before etching period starts. The minimum SiH_4 flow period was determined to be shorter than residual time τ=4.03 seconds. Fig. 43 shows the transfer characteristics of TFT using these conditions. With the longest flow/etching period (=Microcrystalline Si/a-Si), it clearly shows the feature of microcrystalline Si TFT, poor sub-threshold slope and poor mobility. However, as the flow/etching period are reduced per cycle, the transfer characteristics is improved and in the minimum flow/etching period case (Condition-1), the curve exceeds the amorphous silicon's curve.

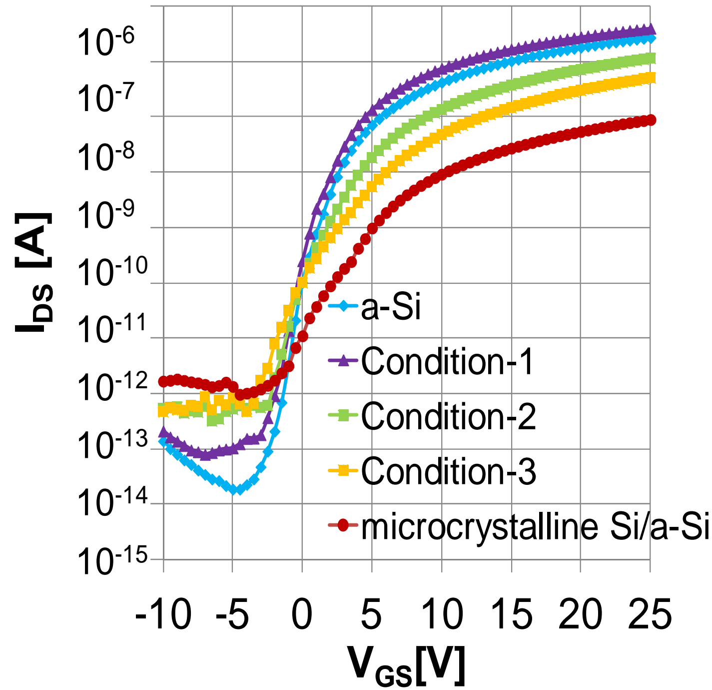


Fig. 43 Transfer characteristics of TFT with various Layer-By-Layer deposition condition

Fig. 44 shows the V_{GS} dependence of source-drain current (Left axis) and the following value, corresponding to the mobility, calculated from gradual-channel-approximation equation (Eq.2), for Condition-1, which showed better characteristics than amorphous silicon TFT.

$$\mu = \frac{L}{C_{OX}W}\left(\frac{\partial(\sqrt{I_{DS}})}{\partial V_{GS}}\right)^2 [cm^2 / V \cdot \sec] \qquad \text{(Eq.15)}$$

(For large V_{GS}, the mobility looks to be reduced, but it is just a deviation from square-root law of gradual-channel-approximation.) The mobility value is about 1.2 [cm^2/Vsec] and is far better than the value of normal amorphous silicon TFT that typically shows about 0.4 ~ 0.7 [cm^2/Vsec].

It can be interpreted that flow period shorter than the residual period τ is causing high mobility value by disassembly of deposition species rather than the etching of deposited film, which dominates the conventional LBL deposition mechanism.

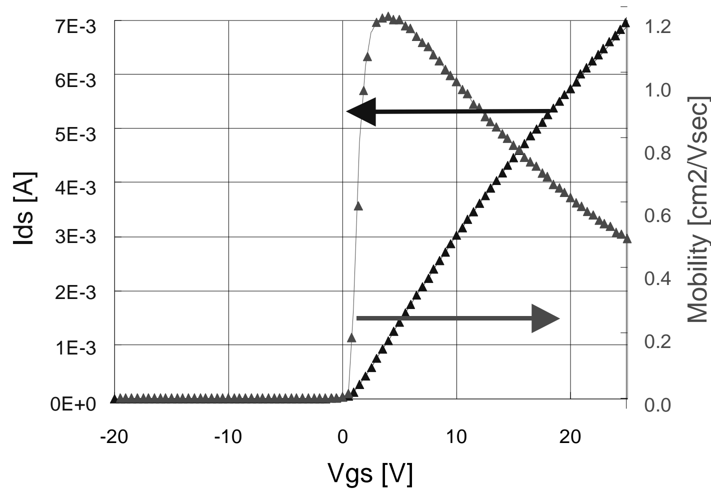


Fig. 44 TFT characteristics of Condition-1

To make sure that the flow period is causing the mobility difference, H_2 plasma period was fixed as constant for Fig. 45. The graph shows that shorter SiH_4 flow period causes the better mobility.

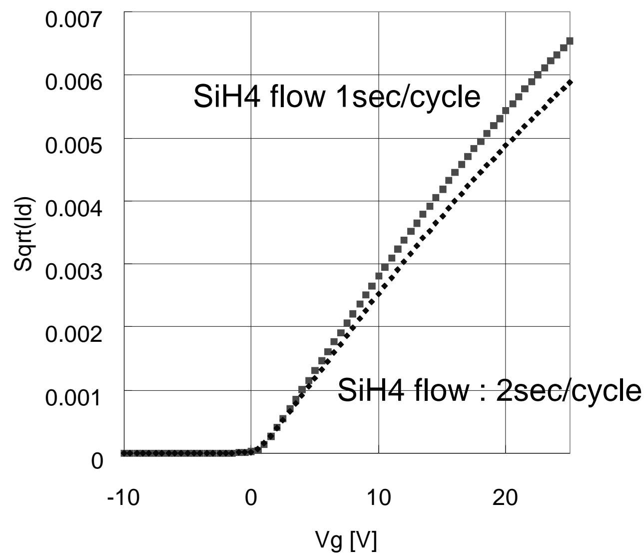


Fig. 45 SiH_4 flow dependence of TFT current

Fig. 46 shows the mobility dependence in a glass substrate on the distance from the gas flow outlet. It clearly shows that the mobility is enhanced as the distance is increased. It is an evidence that the deposition species are transformed in the gas phase.

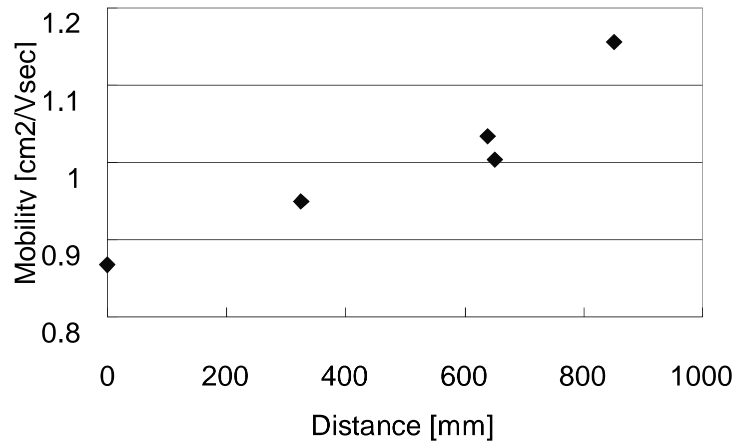


Fig. 46 Mobility change in a glass substrate

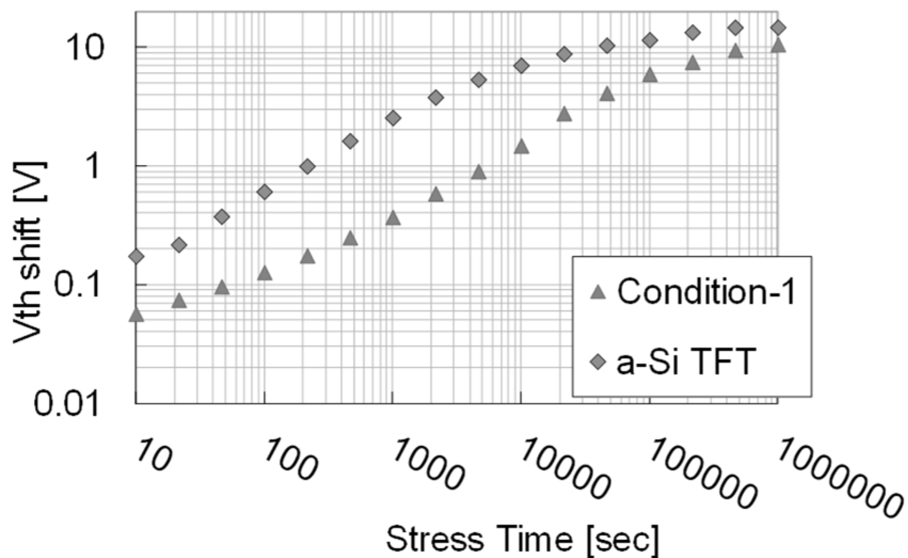


Fig. 47 Positive BTS test result of a-Si TFT and Condition-1
(Stress : 90C V_{GS}=+15V,V_{DS}=0.5V, Measurement : 30C)

Fig. 47 shows the comparison of positive BTS test (Stress : 90C V_{GS}=+15V,V_{DS}=0.5V, Measurement : 30C) of a-Si TFT and the TFT made by Condition-1. With Condition-1, V_{TH} shift is significantly reduced. For example, period to reach 5V V_{TH} shift is 4,081 seconds with a-Si, but the period for Condition-1 would be 62,734 sec by interpolating the curve in Fig. 47. It is approximately 15 times improvement in the lifetime.

Fig. 48 shows the result of Raman microscopy of Condition-1. The curve is almost identical to amorphous silicon except very small bump around 520 [cm^{-1}], which may be caused by the formation of small amount microcrystalline. Therefore, it can

be concluded that the film in Condition-1 experiment is basically amorphous silicon showing excellent stability deposited by the condition on the verge of changing to microcrystalline Si state

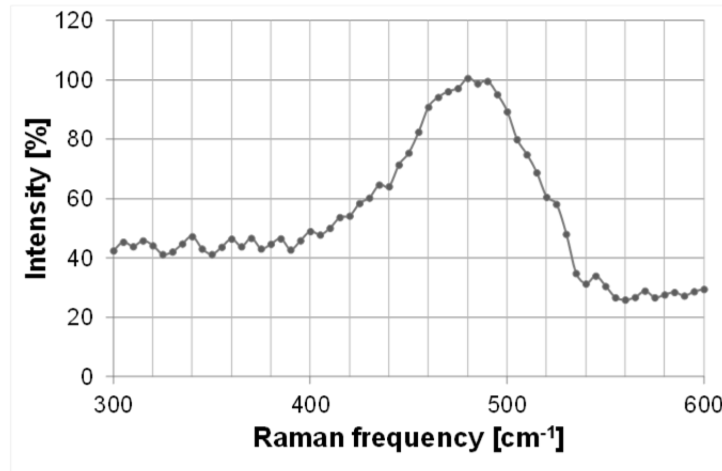


Fig. 48 Raman spectrum of TFT fabricated by LBL method

2.2.1.5 Pixel-level V_{TH} compensation circuit and device structure

Using combination of various approaches reported in this section, such as pulse driving method, circular-shaped TFT, dual-channel TFT and CVD recipe modification, V_{TH} shift of amorphous silicon TFT can be reduced. Such reduced V_{TH} shift can be further decreased by pixel-level compensation circuit. Fig. 49 shows an example of voltage-programming compensation circuit reported by J.Sanford et al. [38]

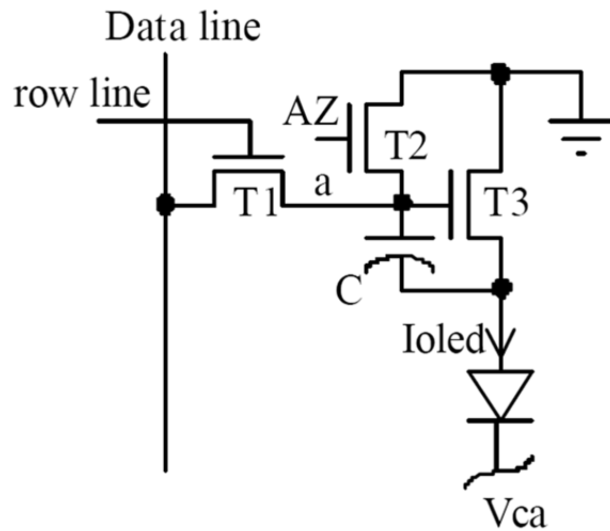


Fig. 49 An example of voltage-programming compensation circuit by J. Sanford et al. [38]

The circuit in Fig. 49 has driver TFT (T3) controlling the OLED current from anode side. (Voltage follower circuit. Also called as "common-cathode" device.) As a-Si TFT is NMOS device normally and OLED normally has anode at the bottom, it is easy to make common-cathode a-Si-driven OLED display by just stacking OLED device on the source electrode of TFTs, as shown in Fig. 50. In this configuration, PV_{DD}-CV is shared by TFT and OLED. As shown in Fig. 51, a-Si TFT current change due to V_{TH} shift becomes smaller than direct measurement of a-Si TFT by the amount of I-V curve slope of OLED device. Similarly as shown in Fig. 52, OLED device characteristics change does not affect the OLED current change very much due to I_{DS}-V_{DS} slope of TFT. This feature is a merit to reduce the image sticking of an AMOLED display. (This configuration is used in actual large AMOLED televisions.)

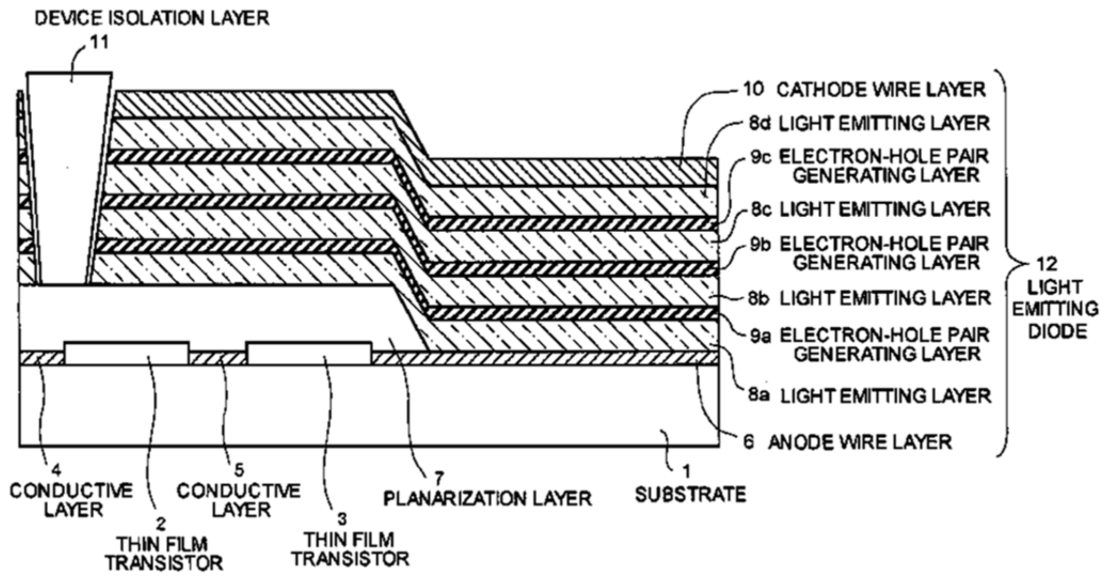


Fig. 50 Common-cathode configuration with white tandem OLED device (T.Tsujimura et al, US7227304B2)

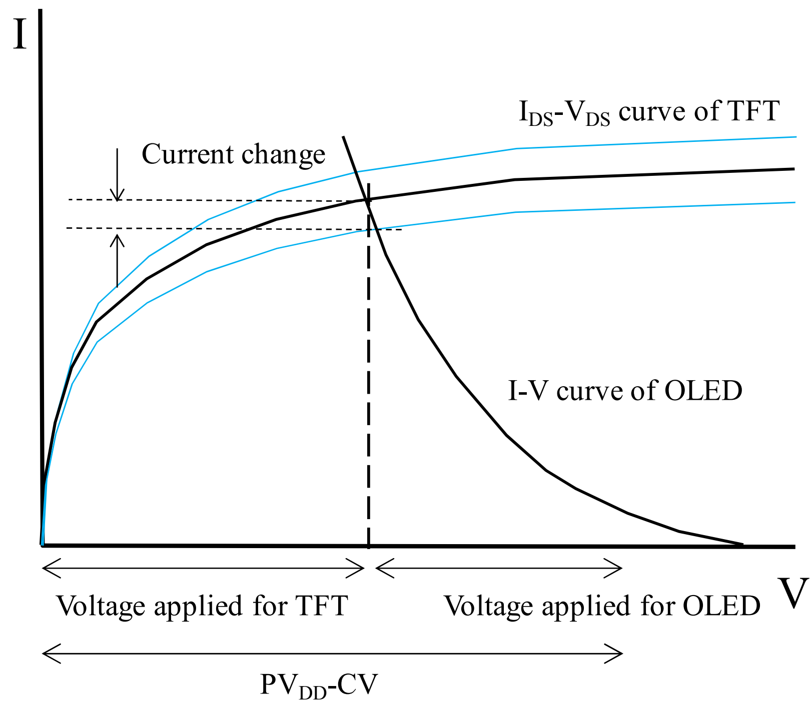


Fig. 51 Current change due to TFT V_{TH} shift

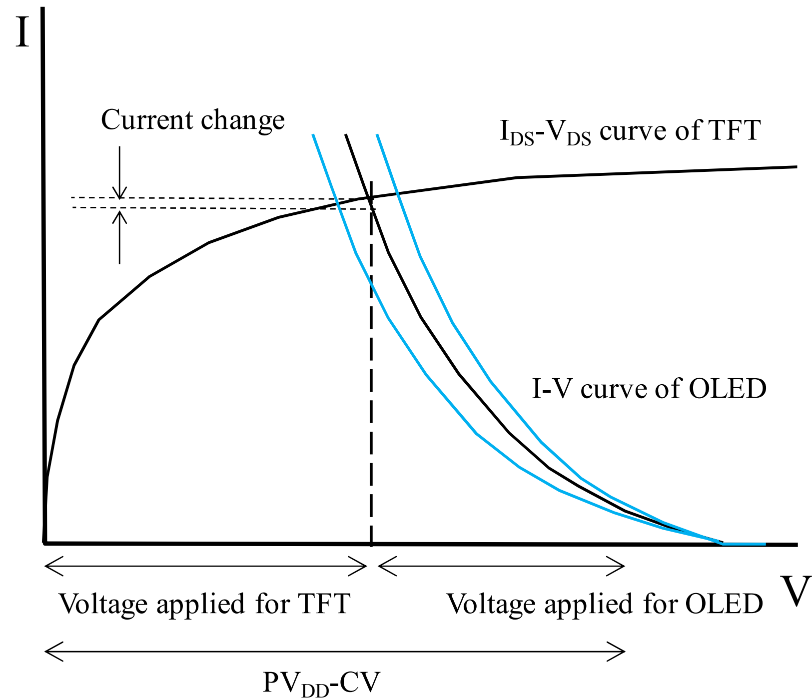


Fig. 52 Current change due to OLED voltage change

Another possible configuration is common-anode circuit as shown in Fig. 53. As a-Si TFT has low mobility, if bottom emission structure is used, the aperture ratio would become very small, which is not sufficient for delivering enough OLED device lifetime. Therefore, top emission structure must be used. To have both top emission and common-anode configuration, device structure shown in Fig. 54 is used. As anode electrode is in common voltage, it can be extended as large area enough to have low voltage drop.

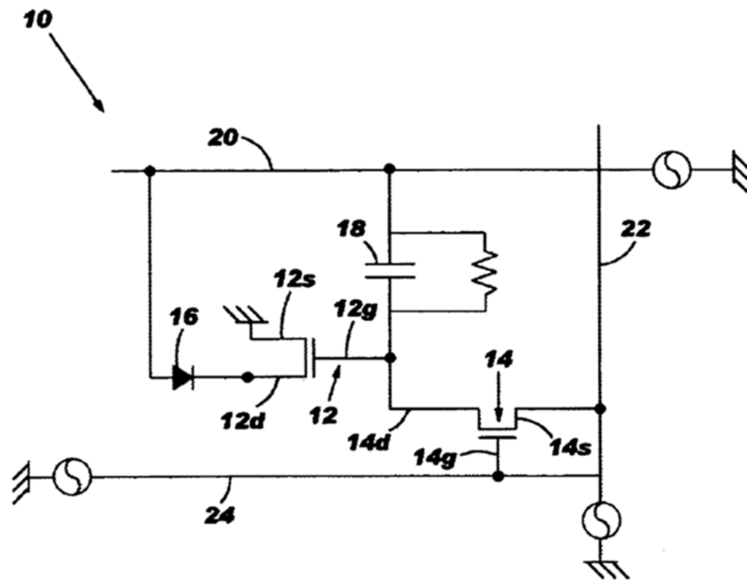


Fig. 53 Common-anode pixel circuitry for a-Si TFT (T.Tsujimura et al, US6727645B2)

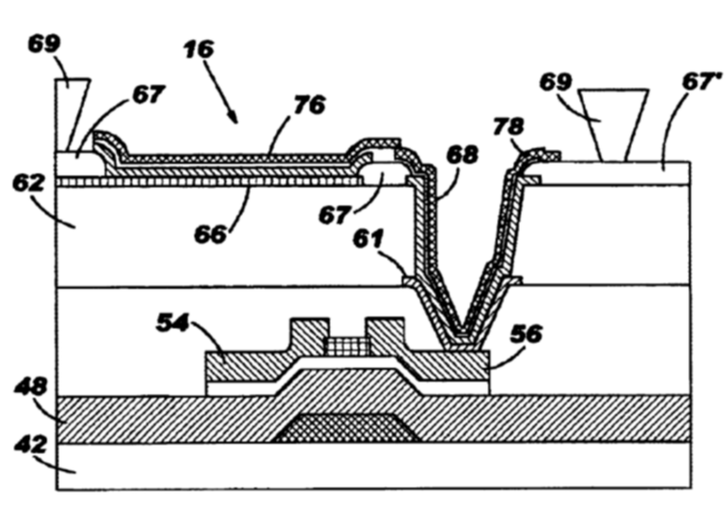


Fig. 54 Common-anode configuration for a-Si TFT (T.Tsujimura et al, US6727645B2)

As described, using various approaches such as pulse driving, structure to avoid current concentration, dual-channel TFT, CVD recipe change and pixel-level compensation circuit, instability of amorphous silicon TFT can be reduced. By combining these technologies, world's largest (at the time) 20.0-inch AMOLED display prototype was fabricated by amorphous silicon TFT backplane, which is

beyond the size limit (17-inch at the time) of excimer-laser annealing equipment as shown in Fig. 55. The specification of the display is shown in Table 4.

Fig. 55 20.0" world's largest (at the time) active-matrix OLED display driven by amorphous silicon TFT backplane

Size	20.0" diagonal
Resolution	WXGA/HDTV compatible
Peak luminance	>500cd/m2 (300cd/m2)
Color number	16M
TFT design	a-Si TFT + compensation circuit
OLED design	Top emit
Color gamut	105%
Response time	<1msec
Contrast ratio	>1000:1

Table 4 Specification of 20.0" AMOLED display

2.2.2 Peripheral technologies used for amorphous-silicon-TFT-driven OLED televisions

2.2.2.1 Gate bus line resistance

a) Gate bus line resistance requirements

Fig. 56 Displays with small voltage drop and large voltage drop

As OLED is a current-driven device, voltage drop consideration is very important to make large display happen. If voltage drop is large, images are not shown in the opposite end of a display from the current supply connection. (Fig. 56)

Current flowing in a supply line can be expressed as,

$$I_{SUPPLY} = I_{pixel} \times 3 \times m \quad \text{(Eq.16)}$$

, where m is vertical number of pixels.

Wiring resistance can be described as,

$$R_{SUPPLY} = \frac{\rho_{SUPPLY} \times 3m \times a}{d_{SUPPLY} W_{SUPPLY}} \quad \text{(Eq.17)}$$

, where ρ_{SUPPLY} is the resistivity of supply line material, , d_{SUPPLY} is the

thickness of supply line, W_{SUPPLY} as the width of supply line.

Therefore the maximum voltage drop during display driving can be written as,

$$V_{DROP} = I_{SUPPLY} R_{SUPPLY} = 9m^2 I_{pixel} a \frac{\rho_{SUPPLY}}{d_{SUPPLY} W_{SUPPLY}} \quad \text{(Eq.18)}$$

If design rule for the LCD display is used, the voltage drop will be terribly large as shown in Fig. 57. This trend will be significant, especially for low OLED device efficiency.

For example, if $\rho_{SUPPLY} = 4[\mu\Omega cm]$, W_{SUPPLY}=5[μm], d_{SUPPLY}=200[nm], I_{pixel}=10[μA], the voltage drop would be V_{DROP}=4.22[V] and will cause significant luminance change in a display.

To solve this issue, very low resistance wiring is necessary.

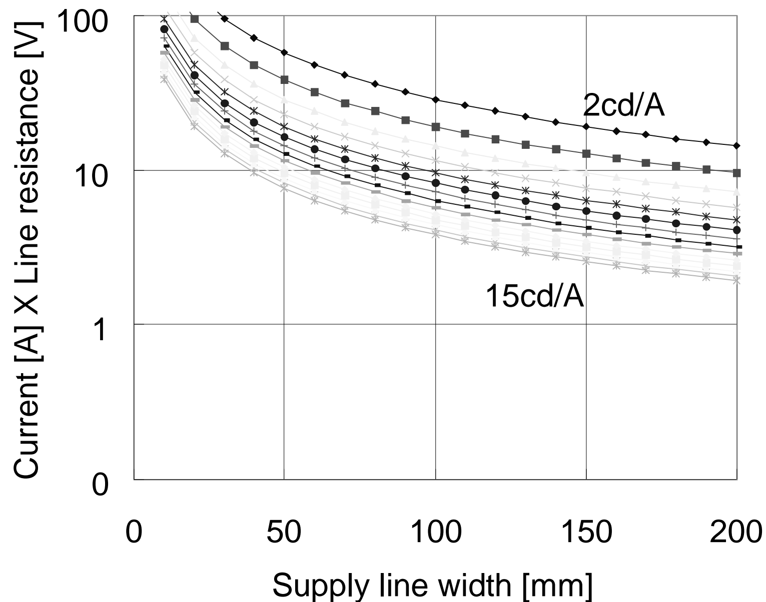


Fig. 57 Voltage drop when LCD-design-rule is used

Choice of low resistivity metal, thickness increase, wide bus wiring and driving technique are effective approaches to improve the situation. Fig. 58 shows the voltage drop reduction by wiring thickness. Also Fig. 59 shows the case for both thick wiring and low resistivity metal. With those, voltage drop can be manageable level. However, as the wiring thickness is increased, the gate insulator becomes worse. In this section, techniques to secure the gate insulator coverage over thick gate metal are studied and it contains two topics, which is necessary to be counter-measured for making large AMOLED display ;

- Several defects regarding the Mo/Al taper etching explained by passivity theory.
- Mouse hole defects regarding the Mo/Al wiring can be explained by stress voiding theory.

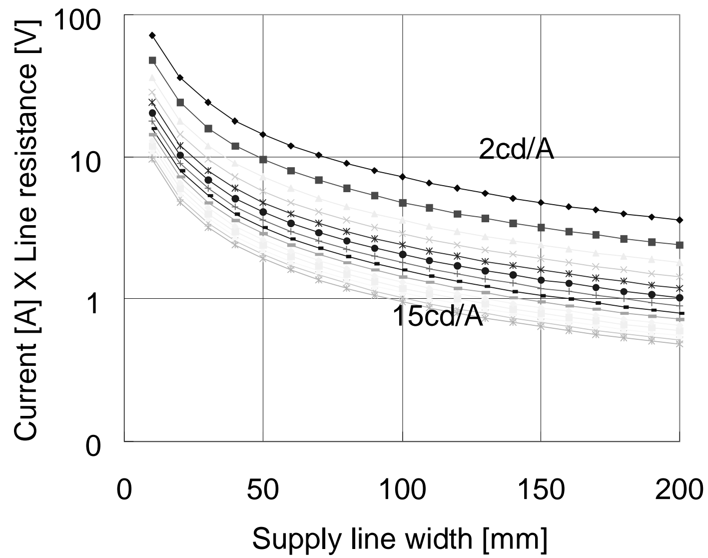


Fig. 58 Voltage drop reduction by wiring thickness increase

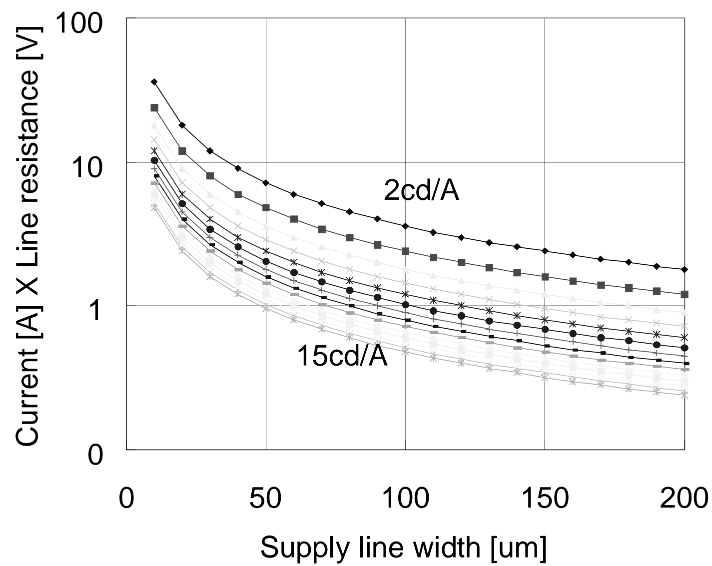


Fig. 59 Voltage drop reduction by wiring thickness increase and resistivity reduction

b) Issues for low resistance wiring using Mo/Al

Fig. 60 shows a SEM picture of Mo/Al multi-layer taper shape. Normally, such multi-layer taper etching is made by using the etching rate difference of two metals, however passivity creation can cause large issue for the taper shape reproduction. For lower resistivity, wiring needs to be as thick as possible, but steep or over-hanged taper edge shape causes poor coverage of gate insulator and causes inter-layer short defect. To make large AMOLED display happen, taper shape control of aluminum wiring to secure the gate insulator coverage is very important.

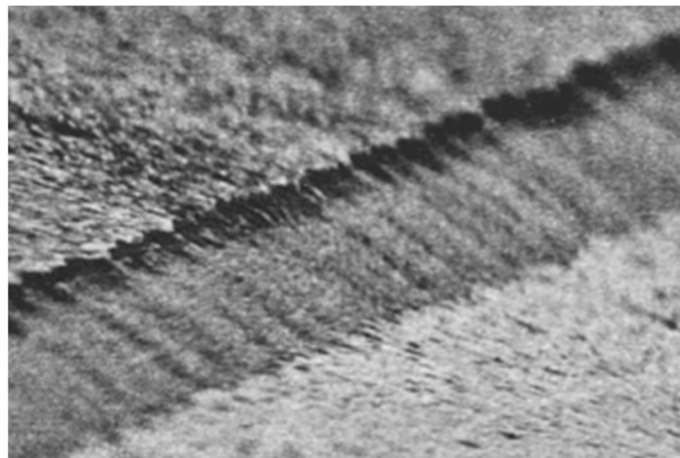


Fig. 60 SEM picture of Mo/Al wiring taper shape

b-1) Various defects regarding the gate insulator coverage

Defects of TFT backplane regarding the gate insulator coverage are categorized and counter-measured.

In this experiment, following equipment and conditions are used.

Sputter:

Equipment		Tokuda 512 Inline-type sputtering system
Temperature		150° C
Condition	Molybdenum	1.8kW, Ar 150sccm, 0.5Pa, 50nm (Columnar structure as shown in Fig. 61)
	Aluminum	7kW, Ar 150sccm, 0.5Pa, 200nm (Large grain about 200nm width as shown in Fig. 61)

Etching:

Equipment	ETS dip-spray etching system
Temperature	40° C

Etching method	Dipping and spray
Etchant	H_3PO_4, HNO_3, CH_3COOH, H_2O mixture

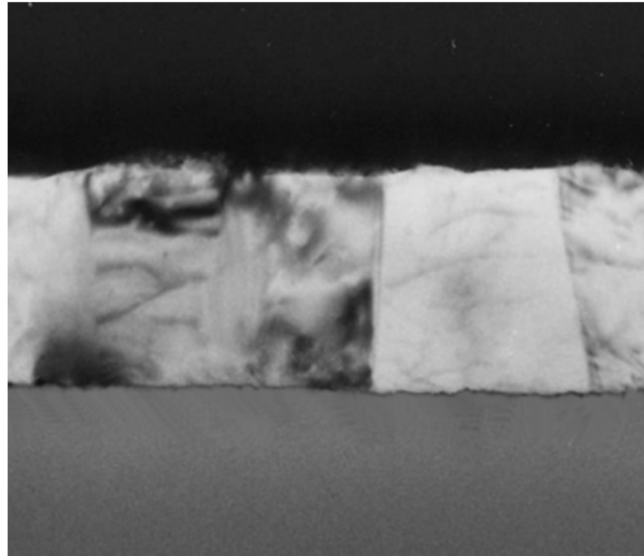


Fig. 61 Cross-sectional TEM picture of Aluminum wiring

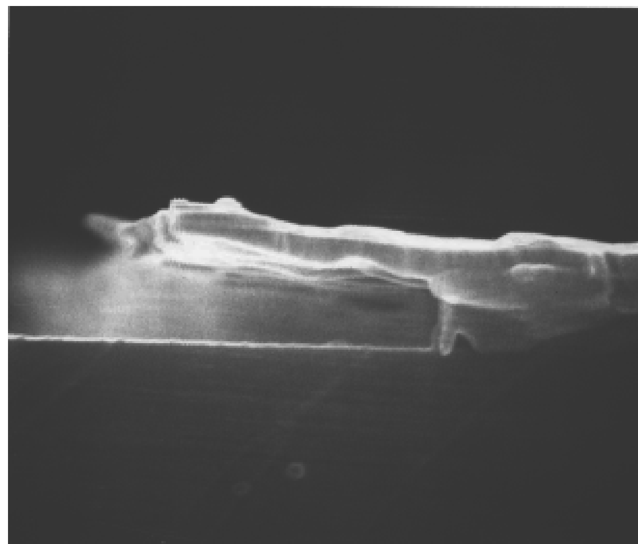


Fig. 62 Over-hanged profile of Mo/Al wiring edge (SEM picture)

<Defect-1> Taper shape defects

When Mo/Al multi-layer stack is etched, in the so called, "PAN" acid (mixture of phosphoric acid, acetic acid, nitric acid and water), aluminum is dissolved by phosphoric acid + acetic acid and molybdenum is dissolved by the nitric acid.

Molybdenum is known to cause passivity in nitric acid environment condition and it can cause etching profile issue, which can cause gate insulator coverage issue. This defect can be explained by passivity theory and can be controlled by the etching method and pattern density. [39]

<Defect-2> Mouse--hole defects

When aluminum wiring is patterned by wet etching, so called "Mouse-hole" defect can be a serious issue. Mouse hole typically has sharp edge and can deteriorate the gate insulator coverage. The diameter of mouse hole in the experiment was about 0.5 μm to 1.0 μm. This defect is related to the grain size of aluminum and aluminum-molybdenum adhesion. It can be controlled by molybdenum-aluminum interface treatment. [40]

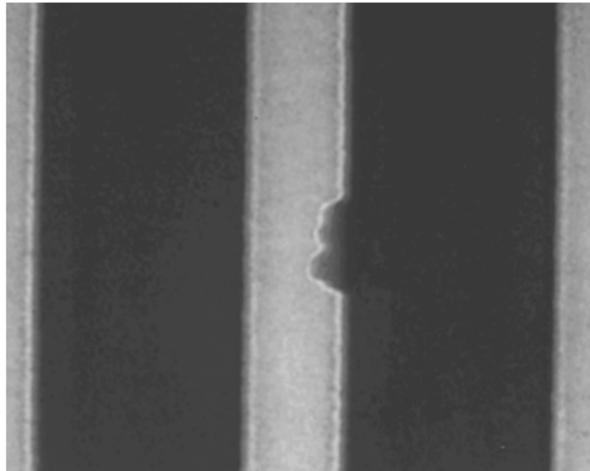


Fig. 63 Mouse-hole defects

Fig. 64 shows the test patter yield dependence of gate insulator thickness for samples with taper shape and for samples without taper shape. Taper shape is very important to secure the good production yield of TFT backplane.

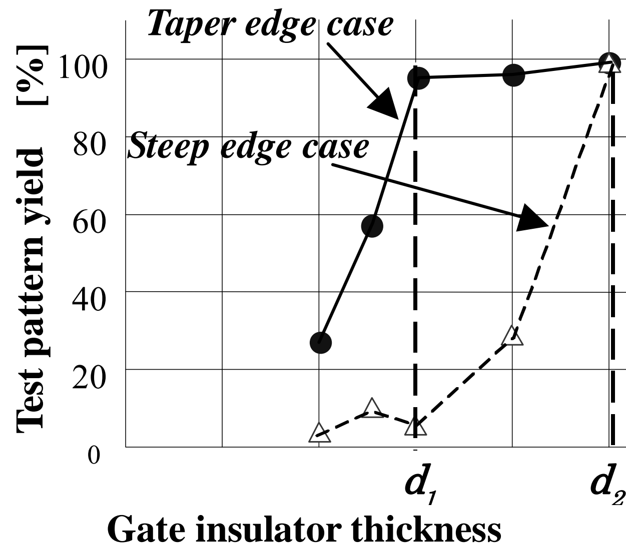


Fig. 64 Test pattern yield dependence of gate insulator thickness

If the edge is steep, the gate insulator coverage is worse, so it needs thicker gate insulator than the taper-shape case. Also Fig. 64 tells that there is a critical thickness like d_1 and d_2, under which the yield becomes significantly decreased.

Fig. 65 shows the microscopic picture of substrate dipping in PAN acid for 10 minutes, with taper-shaped aluminum wiring covered by insulator. Also, Fig. 66 shows the case for with over-hanged edge shape, dipped with the same condition. In the former case with taper shape, the etchant does not damage the wiring, however with over-hanged shape covered by insulator, the etchant is intruded into wiring and etch the aluminum off. Fig. 67 shows the etchant resistance of actual TFT array with over-hanged edge shape. Etchant intruded into the pin-hole caused by the over-hanged edge shape blows off the gate bus line.

For stable TFT backplane manufacturing, it is quite important to understand the instabilities in taper etching process..

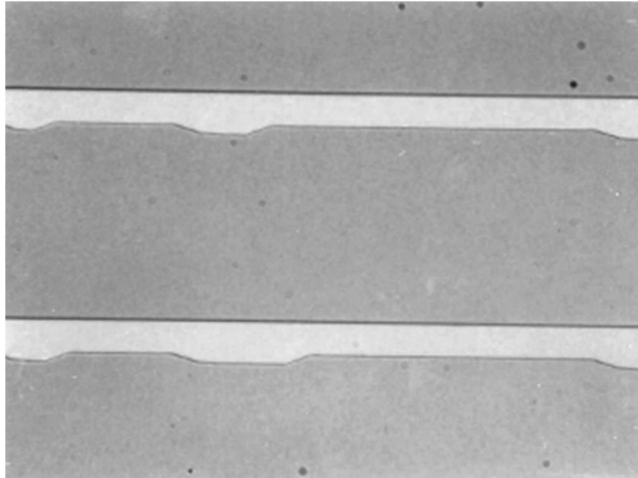


Fig. 65 Etchant resistance of a taper-shaped wiring covered by gate insulator

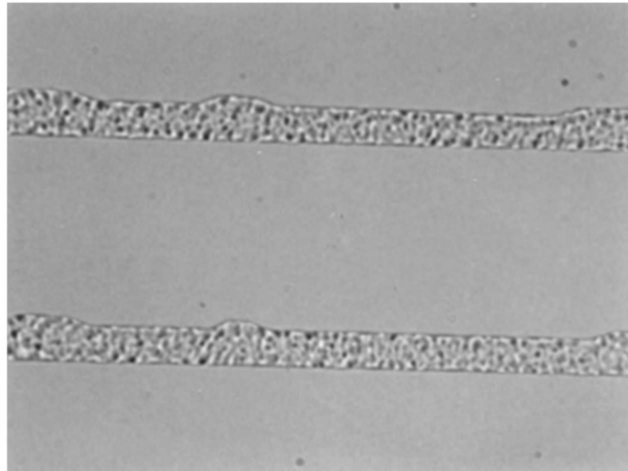


Fig. 66 Etchant resistance of an over-hanged wiring covered by gate insulator

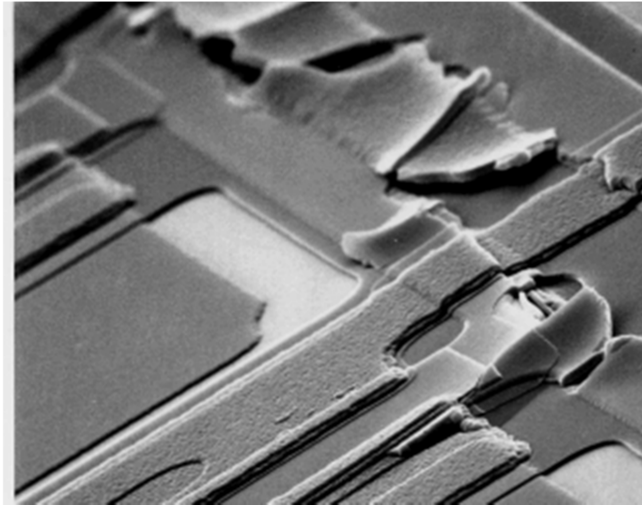


Fig. 67 Etchant resistance of actual TFT array pattern with over-hanged edge shape

c) High-yield low resistance wiring manufacturing for large displays

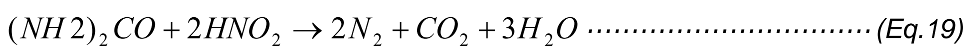
H.Uhlig claims several important information as to the metal passivity creation in his literature. [41]

According to it, aluminum passivity does not show etch resistance in the mixed acid containing phosphoric acid, so the instability of Mo/Al taper creation must be due to molybdenum passivity, rather than aluminum passivity.

Also Uhlig claims several passivity formation mechanism, which is likely to be associated with the taper instability issue as following. [41]

When metals such as Cr, Ni, Mo, Ti, Zr are dipped in the oxidizer solution, anode current flows from metal to solution by means of metal dissolution. In this event, if current density more than critical value $I_{critical}$ flows, the metal is passivated and the current flow is decreased. (I_{passiv}) Current density in the anode metal promotes the passivity creation, so as the ratio *(Cathode area)* / *(Anode area)* becomes larger, the system needs less current to form passivity.

If current flow is stopped, the metal electrode potential is rapidly decreased to so called Flade potential and passivity is collapsed after several seconds to several minutes. Passivity is caused by nitrous acid (passivator) formation in the nitric acid environment If urea is added, passivity is suppressed due to the nitrous acid concentration decrease, described as the following equation.



$$(NH2)_2CO + 2HNO_2 \rightarrow 2N_2 + CO_2 + 3H_2O \quad \text{(Eq.19)}$$

When Mo/Al multi-layer stack is etched by PAN solution, following phenomena are observed.

<Phenomena-1> Taper shape change according to the etching method

Taper shape of Mo/Al multi-layer can be expressed by the side-etching length difference between molybdenum edge and aluminum edge. Fig. 68 shows the side-etching length dependence of molybdenum and aluminum using dip and spray etching method. Clearly side-etching length is very much different according to the etching method. Spray etching gives larger aluminum side etching than molybdenum, while dip etching gives larger molybdenum side etching than aluminum. Taper shape is formed when top molybdenum side etching length is longer than that of bottom aluminum, so dip etching is suitable.

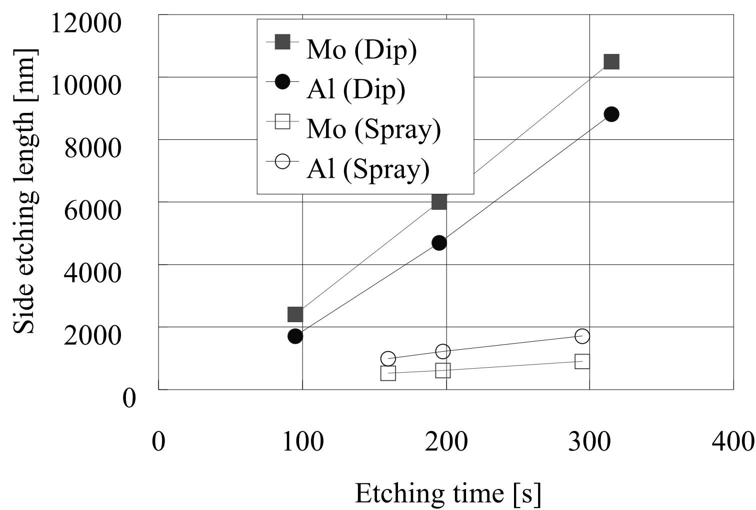


Fig. 68 Side-etching length dependence of molybdenum and aluminum using various etching method

<Phenomena-2> Pattern dependence of taper shape

Fig. 69 shows the taper shape change when wiring pattern is changed. Fig. 69 upper figure case has low pattern density, which shows molybdenum side etching stop and over-hanged shape creation. As the pattern density is increased, the molybdenum side etching becomes larger and the taper shape is created.

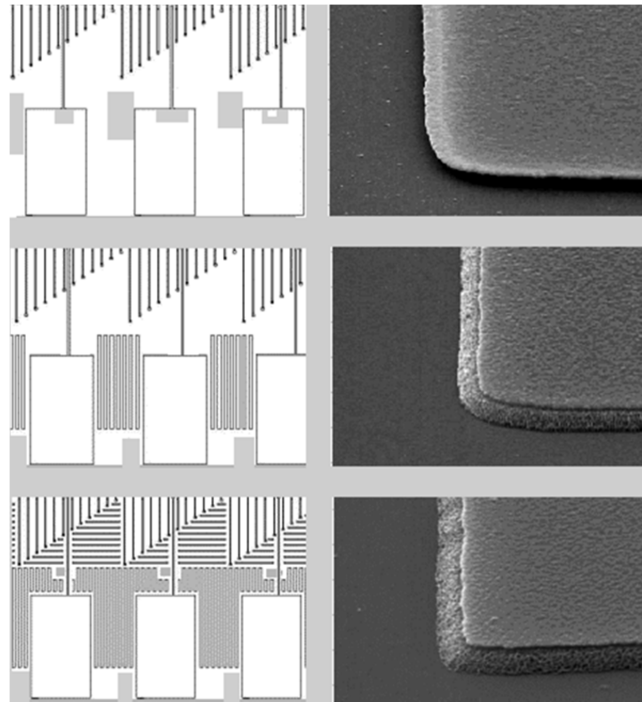


Fig. 69 Pattern dependence of taper shape

To make stable taper etching happen, Uhlig's experimental interpretation [41] was applied to the phenomena.

Regarding the pattern-density dependence of taper shape, the current density model in the Uhlig's interpretation can be applied. In the case when over-hanged shape is not created, exposed area ratio between molybdenum and aluminum is almost equal to the ratio between molybdenum thickness and aluminum thickness. In this situation, in PAN etchant, molybdenum etching rate is faster than aluminum etching rate, so molybdenum metal generates positive molybdenum ion and molybdenum acts as an anode electrode and aluminum acts as a cathode electrode in electro-chemical reaction manner. [41] Electron will flow from molybdenum to aluminum. If molybdenum is initially not covered by passivity, molybdenum will be etched faster than aluminum and taper shape would be created.

However, in the case of molybdenum / aluminum multi-layer etching, there is a critical period when passivity can be easily created. Fig. 70 shows the schematic diagram of Mo/Al cross section when the Mo/Al multi-layer stack is patterned by etching.

When exposed molybdenum is etched off, aluminum surface is suddenly exposed in the etchant. (Fig. 70 lower figure) Exposed area of molybdenum is the portion of the side wall having only some tens of nanometer, however aluminum is exposed all the uncovered region by the photo-resist mask having some micro-meter to some

millimeters scale. Then the ratio between exposed aluminum to exposed molybdenum becomes huge value. Due to this large area ratio causes huge current density in the molybdenum, which would create the molybdenum passivity. [39]

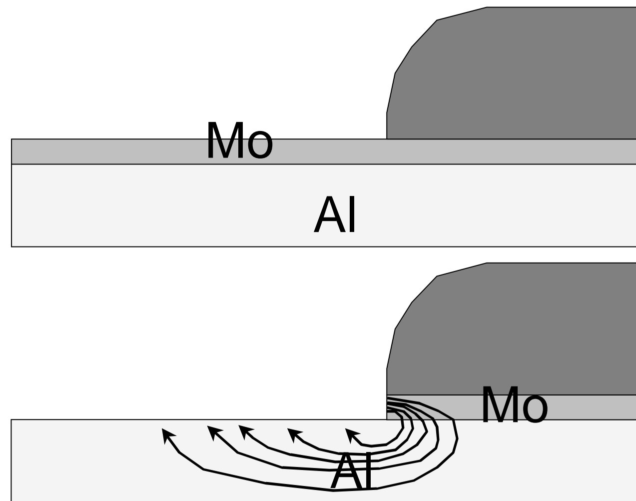


Fig. 70 Passivity formation mechanism of molybdenum in taper etching process

Fig. 71 shows the pattern density dependence of Mo/Al taper shape and the trend is very consistent with the explanation. As pattern density is increased the taper angle becomes shallower. With more than 30% pattern density, the area ratio between molybdenum and aluminum can be reduced, so that the stable taper shape formation can be assured. [39]

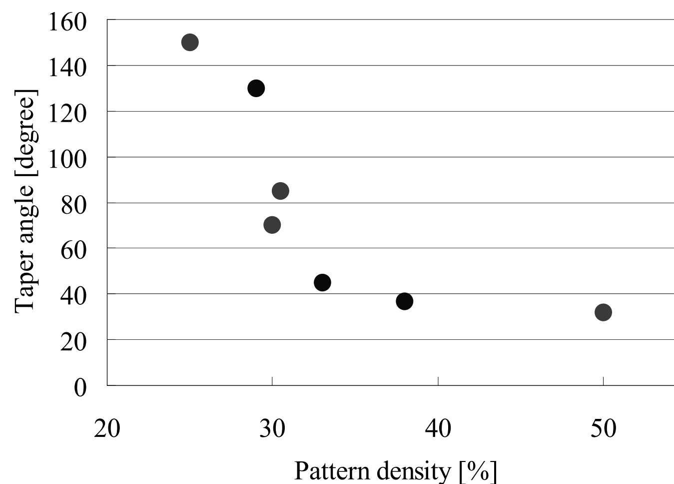


Fig. 71 Pattern density dependence of taper angle of Mo/Al multi-layer stack

As shown in Fig. 68, spray etching suppresses the side etching of molybdenum and the side etching length difference between molybdenum and aluminum causes over-hanged shape. To make sure that the side-etching suppression is caused by molybdenum passivity, electro-chemical experiment was made.

Fig. 72 shows the polarization diagram of molybdenum in the same etchant. Horizontal axis is the potential of molybdenum electrode and vertical axis is the current flowing in the metal. It can be seen that the critical electric current is 0.06A/cm^2.

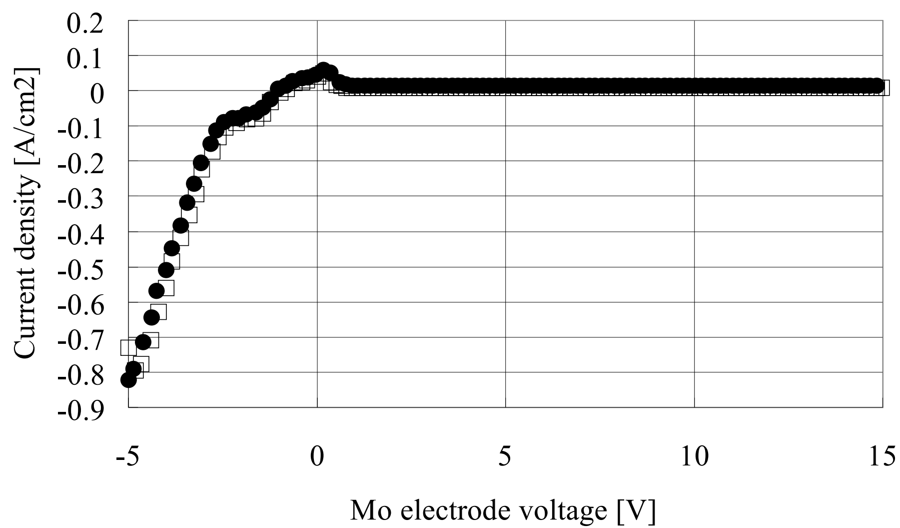


Fig. 72 Measured polarization diagram of molybdenum

Fig. 73 shows the molybdenum potential change after the voltage supply is stopped. When no urea is added, the potential keeps itself around -0.15 [V] for 60 seconds (Semi-stable state) and it is changed to around -0.3 [V] after that. It very well follows the behavior of passivity in Flade potential and its subsequent decay, described in Uhlig's literature. [41]

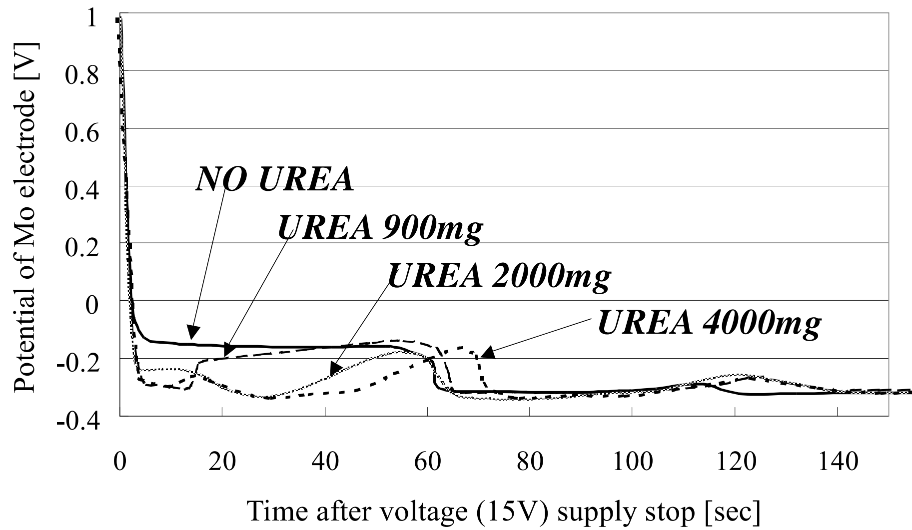


Fig. 73 Transition of molybdenum potential after the voltage supply is stopped

As stated, urea is known to prevent passivity formation. Fig. 73 clearly shows that urea suppresses the potential to be kept in semi-equilibrium state, so it can be concluded that the semi-stable state is due to passivity and the transition from semi-stable state to equilibrium state is due to the collapse of passivity.

Passivity is formed if the current density becomes over 0.06A/cm^2 and it lasts about 60 seconds as shown in Fig. 73 . During this semi-stable state, molybdenum side etching is suppressed and only aluminum side etching is proceeded, so the over-etching period necessary for taper shape formation is reduced, therefore the taper angle becomes steeper in such case.

As described in Fig. 68, spray etching causes over-hanged shape of Mo/Al multi-layer film stack and dip etching creates taper shape. The same etchant and the same patterned photo resist mask are used for both cases, but still causing the difference in the passivity formation. It is important to consider what can change the current density flowing in the molybdenum. One possibility is the fluctuation of (area of aluminum exposure) / (area of molybdenum exposure) ratio by the formed bubble in the etchant. Actually, dip etching in this experiment generates many bubbles on the exposed aluminum surface, while spray etching washes away most of the bubbles.

To verify if bubble is actually fluctuating the passivity formation, dip etching was carried out in a sloped substrate condition where all the bubbles formed on the substrate are washed away during dipping process. Fig. 74 shows the cross-sectional picture of Mo/Al multi-layered stack patterned by sloped etching

condition. With this etching condition, no molybdenum side etching length is observed and over-hanged shape just like spray etching is formed. It can be interpreted that the wash-away of bubbles on the aluminum surface increased the (area of aluminum exposure) / (area of molybdenum exposure) ratio that created molybdenum passivity due to current concentration in the molybdenum film.

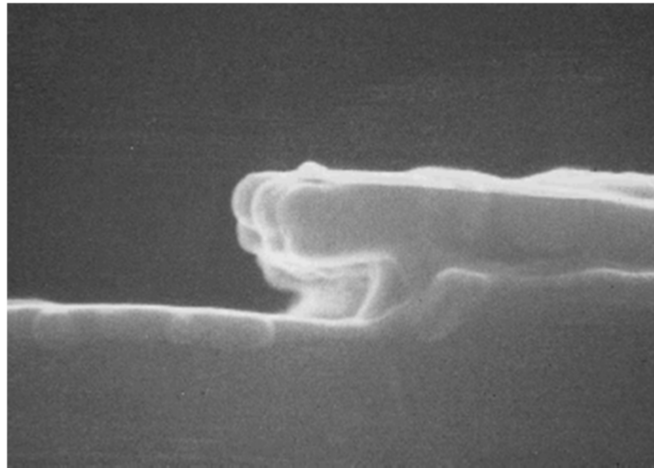


Fig. 74 Cross-sectional SEM picture of Mo/Al multi-layer patterned by sloped etching condition

As a result, to prevent from over-hanged shape of Mo/Al multi-layer film to secure the formation of taper shaped pattern and to secure the coverage of gate insulator over the Mo/Al wiring, following direction should be applied.

Etching method to remain bubbles on the substrate, such as dip etching, is advantageous for taper creation

Pattern density should be increased to decrease the (area of aluminum exposure) / (area of molybdenum exposure) ratio.

2.2.2.2 Process reduction of dual-channel TFT

Though dual-channel TFT has large merit in reducing the V_{TH} shift of amorphous silicon TFT as discussed in 2.2.1.3, dual-channel requires two TFTs in vertical direction and is costly. Therefore, to implement in actual commercial product, process step reduction is very important. [31] Fig. 75 shows the process flow schematic of the dual-channel TFT. By etching amorphous silicon, gate insulator, signal line in the same photolithography step, process step is reduced to 5 mask count.

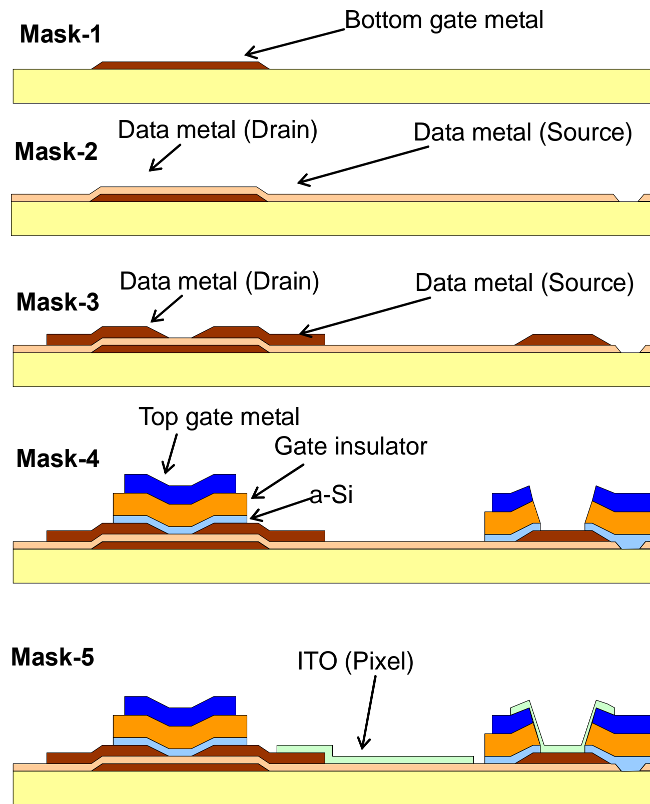


Fig. 75 Dual-channel TFT with process step reduction implemented

Mask step	Process
Mask-1	Bottom gate metal deposition
	Photo lithography
	Etching / resist strip
Mask-2	Bottom insulator deposition
	Photo lithography
	Etching / resist strip
Mask-3	Signal line metal deposition
	Photo lithography
	Etching / resist strip
Mask-4	a-Si / Gate insulator deposition
	Gate metal deposition
	Photo lithography
	Etching / resist strip

Mask-5	ITO deposition
	Photo lithography
	Etching / resist strip

Table 5 Process flow of dual-channel TFT

Fig. 76 shows the TFT transfer characteristics of amorphous silicon TFT fabricated using the process shown in Table 5. Unlike normal TFT transfer characteristics, off current is very high like 10^{-10} [A] and sub-threshold swing is also terrible like S=1.17 [V/dec]. It is necessary to find out the cause of these issues to use the process in Fig. 75.

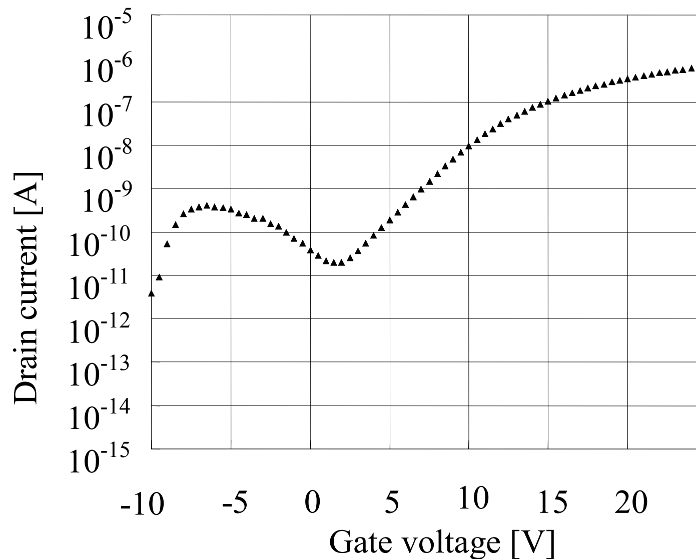


Fig. 76 TFT characteristics of the 5-mask TFT

At first, off current requirement for AMOLED display is estimated. Pixel capacitance can be described as the summation of supplementary capacitance *Cs* and the gate node capacitance of driver TFT as follows.

$$C_{ALL} = C_S + C_{DRIVER} = \frac{\varepsilon_{ox}\varepsilon_o}{d_{ox}}(W \cdot L + 3a^2\beta) \text{ ....} \quad (Eq.20)$$

where ε_o: Permittivity of vacuum, , ε_{ox}: Relative dielectric constant of gate insulator, d_{ox}: Gate insulator thickness, *a*: pixel pitch, β: Ratio of supplementary capacitance area to the pixel area)

Acceptable pixel voltage change is 1LSB (Least significant bit), so it can be

expressed as,

$$V_{allowed} = \frac{Va}{N} \cdots\cdots (Eq.21)$$

where V_a: Data voltage swing, N: Number of gray scale levels)

Amount of charge to be delivered by TFT to C_{ALL} can be expressed using Eq.21,

$$Q = I_{OFF\max} T = C_{all} \frac{Va}{N} \cdots\cdots (Eq.22)$$

where T: One frame period, $I_{OFF\max}$: Allowable maximum off current)

Using Eq.20, Eq.21 and Eq.22, maximum TFT leak level that is unrecognizable by human being can be expressed as,

$$I_{OFF\max} = \frac{C_{all}}{TN} =\approx 2\times 10^{-12}[A] \cdots\cdots (Eq.23)$$

According to this rough calculation, switching TFT needs to have less than $2\times 10^{-12}[A]$ off current level. If this value can be satisfied, AMOLED display with sufficient retention property can be designed.

To apply the low-cost production method described in Table 5, leakage current must be reduced. OBIC (Optical Beam Induced Current) method [42] was used to determine the leakage path of dual-channel TFT. Laser beam was irradiated on TFT under operation. (OBIC works using following principle. If the irradiated location is not within the leakage path, generated electron-hold pair recombines and disappears. If the irradiated location is within the leakage path, the electron flows out in the drain electrode and is detected.) Fig. 77 shows the leakage path analysis by OBIC method. It can be seen that the ungated amorphous silicon region is causing the leakage.

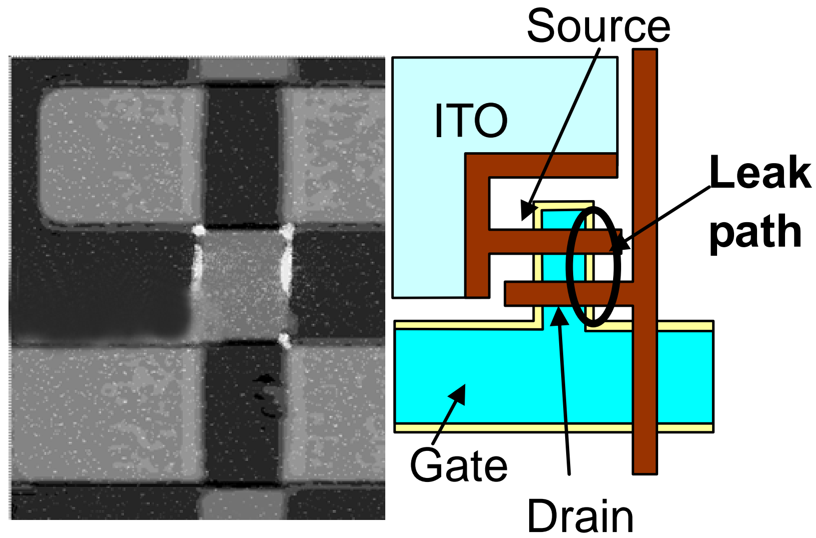


Fig. 77 Leakage path detection by OBIC (OBIC image of ellipse in right figure is the right picture)

Conductance in amorphous silicon in the ungated region is affected by gate electrode and drain electrode. Negative gate voltage suppresses the conduction and large drain voltage than V_{TH} increases it. For the OLED display application, leakage current must be suppressed to keep the gate voltage node of driver TFT with larger drain voltage condition than V_{TH}. Fig. 78 shows the channel length (L) dependence of TFT characteristics. Longer channel length suppresses the ungated region leakage.

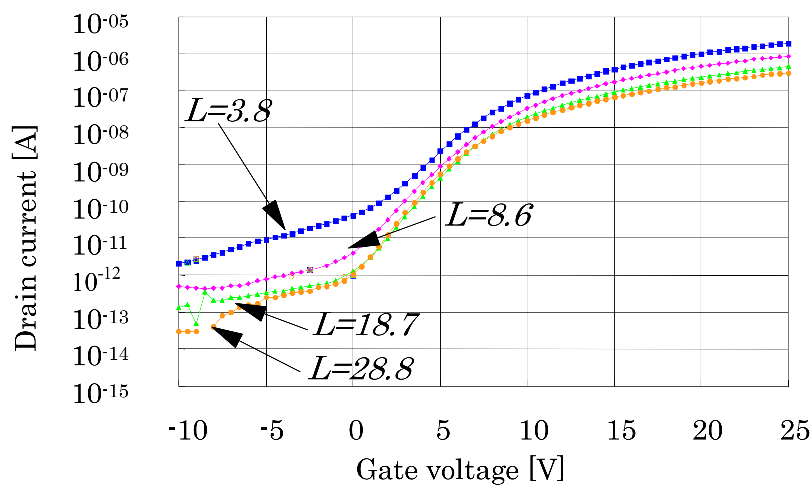


Fig. 78 Channel length dependence of TFT transfer characteristics

To verify the channel length dependence of ungated region behavior, ATLAS device simulation was carried out.

Fig. 79 shows the cross-sectional view of ungated region simulation result when the TFT current is ON. Most distant region of ungated region is carrying the largest portion of leakage current flow. ($10^{14}/cm^3$ in the image)

Fig. 80 a)-c) show that the minimum value of ungated region potential is increased as the channel length is increased. It can be concluded that the such minimum value (most electrically resistant region) is suppressing the ungated region conduction.

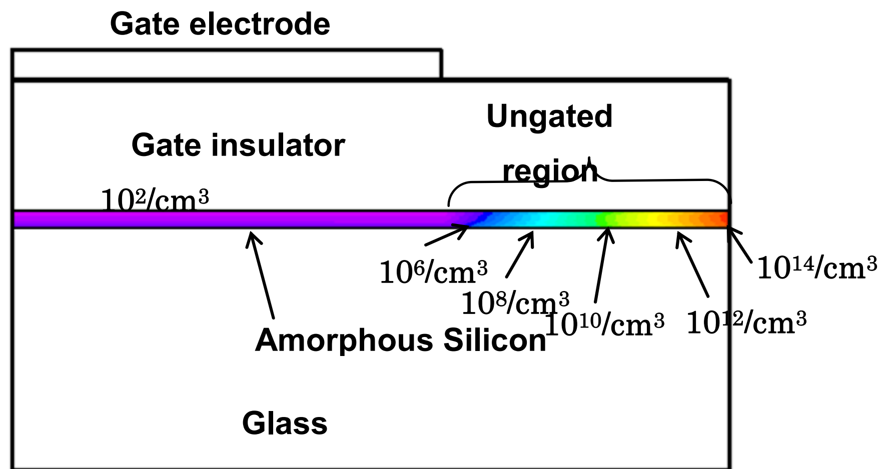


Fig. 79 Current density simulation in the ungated region

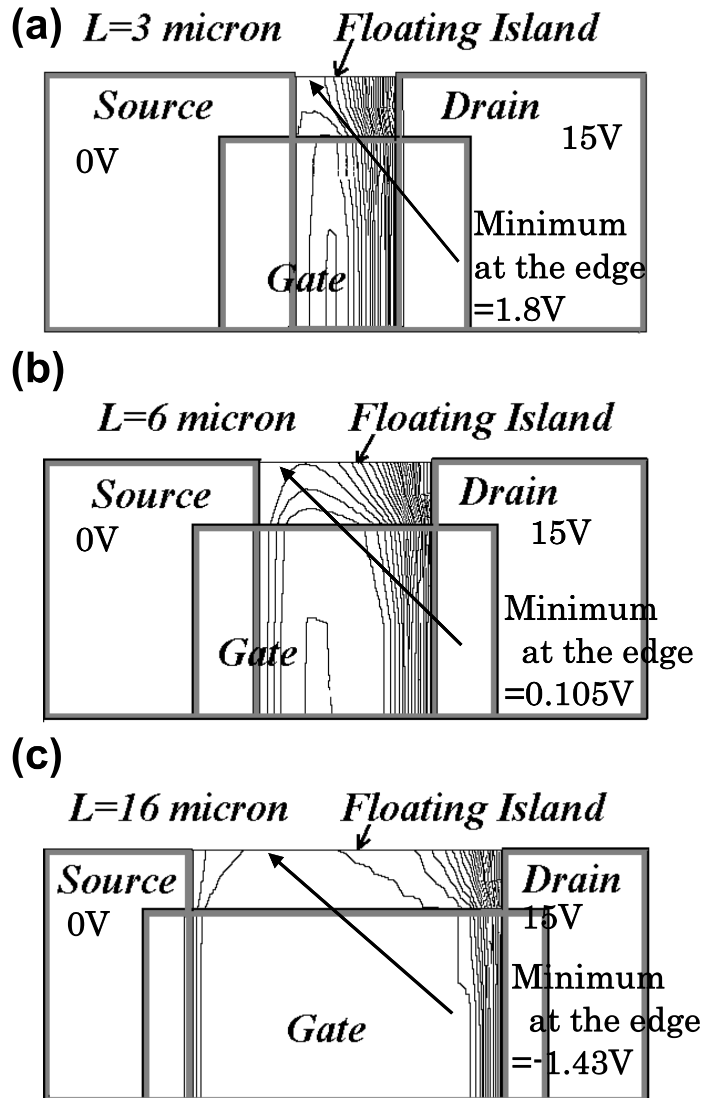


Fig. 80 Potential distribution of dual-channel TFT (Simulation)

Therefore, by extending the channel length (L), the ungated region leakage current can be suppressed. However, channel length extension also reduces the ON current. For the large AMOLED display driving, it is necessary for a TFT to equip with both large ON current and low OFF current, then extension of channel length cannot be the solution. To circumvent the situation, an unique TFT design with long ungated channel length and short ON current channel length is design as shown in the right figure of Fig. 81 (T-shaped TFT). Fig. 82 shows the TFT characteristics comparison between TFT with conventional design and T-shaped TFT, both with ungated amorphous region. With T-shaped TFT, both large ON current and low OFF current can be achieved, suitable for AMOLED display design.

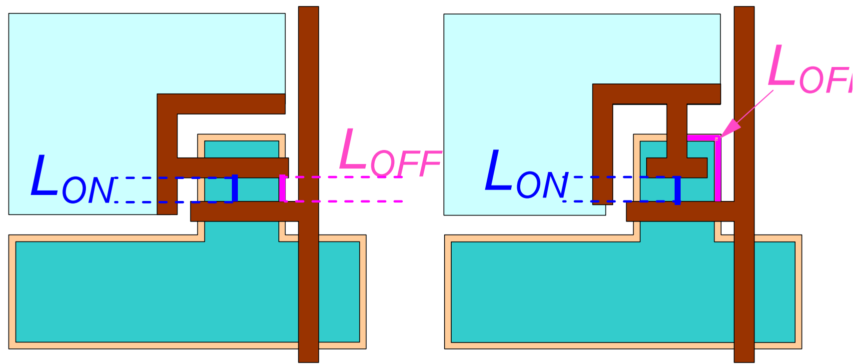


Fig. 81 Conventional design TFT (Left) and T-shaped TFT (Right)

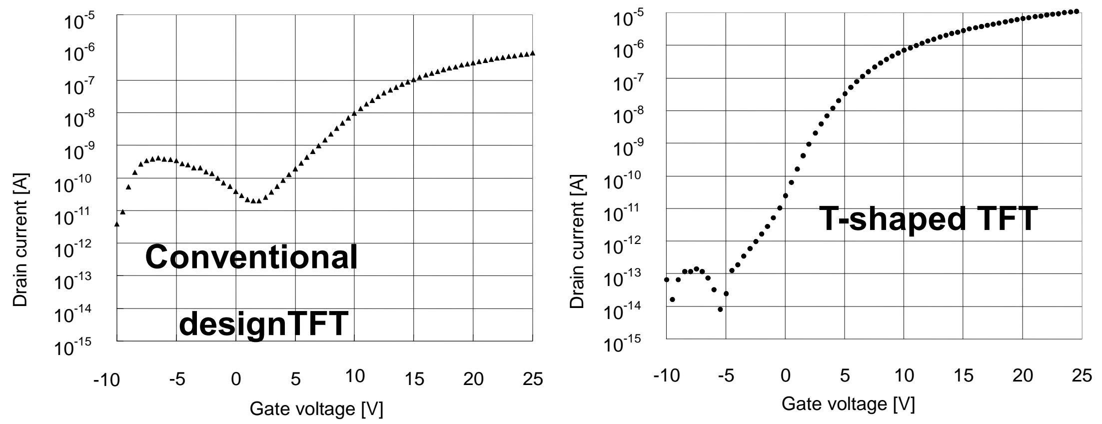


Fig. 82 TFT characteristics of conventional TFT (Left) and T-shaped TFT (Right)

3. Scenario for high yield manufacturing of large high performance OLED televisions

According to the 20-inch prototype, it was proven that large AMOLED TV can be designed with non-ELA-type TFTs. However, the approach used for prototype, such as shadow-masking of OLED brought about many issues during fabrication due to the large size. Also, several TFT technologies with large mobility and better stability were proposed after my 20-inch study, so in the next prototype, the target was set to develop technologies truly applicable for the large AMOLED TV mass-production in terms of both performance and manufacturability. At first, it was considered what kind of feature of a display technology has made it into success or failure in the past.

3.1 Analysis of past display technologies toward high performance large television

As discussed in 1.2, many display technologies were expected as "next generation" , however disappeared or discontinued due to following reasons.

(a) Ferroelectric LCD

In 1990s, when twisted nematic LCDs could bring neither wide viewing angle nor fast response, ferroelectric LCD was regarded as revolutionary technology, which equips with both features and was expected that it would enable attractive large television.[43] **15-inch** display product was shipped in 1995. [44] However, it was reported that the manufacturing was stopped in 1998 [45] and there is no widely-recognized product since then.

(b) FED (Field-emission display)

In 1998, joint development company was formed by a major electronics company [46][47]. However, the JV was filed for bankruptcy in 2004.[48] The electronics companies were targeting to produce **24 to 26-inch** TV product. [49]

(c) SED (Surface-conduction electron-emitter display)

In 2004, a joint venture SED Inc. was formed by two major electronics companies to manufacture SED television [50] and then demonstrated **36-inch** [51] and **55-inch** high quality television prototypes. After 6 years of operation, it was announced to discontinue the JV in 2010. [52] [53]

(d) PDP (Plasma Display Panel)

PDP was once regarded as one of the winner in the flat panel display. [54] A major electronics company president claimed that TVs **over 37-inch** would be for PDPs, not LCDs. [55] However, PDP shipment was reduced from 957K unit (2010) to 67K unit (2013) , while total flat panel shipment is growing 23% a year.[56]

(e) Twisted-Nematic (TN) LCD

TN-LCD was invented in 1971. [57][58] In the early stage, TN-LCD was used only for segment display like calculator, but due to the application of active-matrix driving [59], it obtained the scalability **from below 1-inch to larger size**. Viewing angle and response time were its disadvantage against conventional display CRT, however new alignment technologies, such as IPS, VA and FFS, solved the issues and LCD TVs successfully overtook CRT TVs in 2008 in worldwide. [60]

3.2 Consideration of technology battle in flat panel display

It is notable why only TN-LCD could beat the former technology when so many other technology could not. TN-LCD clearly had disadvantage against CRT in terms of cost, production yield, viewing angle, response time, however it did not die. Ferroelectric LCD, FED, SED, PDP had clear advantage in viewing angle and response time, but such features was not received enough to replace LCD technology.

One conceivable reason is the target display size. Display technology has a feature that the production yield rapidly decreases as the display size is enlarged. (Will be discussed in Section 3.3.) Technologies (a)-(d) discussed in 3.1 are targeting large display size for manufacturing from the beginning. (15-inch is not a large display size currently, but it was a very large size in 1995 when Ferroelectric LCD was developed.)

Fig. 83 shows a comparison of display shipment in 2006 (when PDP was still a major TV technology) over 20-inch. [61] PDP shipment was 10,060K and LCD shipment was 64,625K, about 6 times difference and sounds like a battle by big two technology players. However, a comparison of shipment for all size described in Fig. 84 shows that the situation is one side game, advantageous for LCDs. Large LCD and small LCD have a lot in common. Liquid crystal filling, peripheral sealing, rubbing, all that sort of work was repeated 2,891,720K times in 2006 for LCDs, while only 10,096K times for PDP processing. It can be assumed that LCD could experience much larger processing opportunities than PDPs and that caused much benefit like increased yield, enhanced quality, material cost down and knowledge

accumulation for improvement. Many of the technologies in (a)-(d) had issues when the device becomes smaller (Incapability of scaling) and that may have caused this situation.

According to the hypothesis, it is much safer for a display technology to make much of the small size display manufacturing to make the technology mature. In that sense, OLED technology is equipped with scalability, just like LCDs and is not like (a)-(d), so OLED can be regarded as qualified toward the success in large TV manufacturing after enhancing its maturity by small display manufacturing.

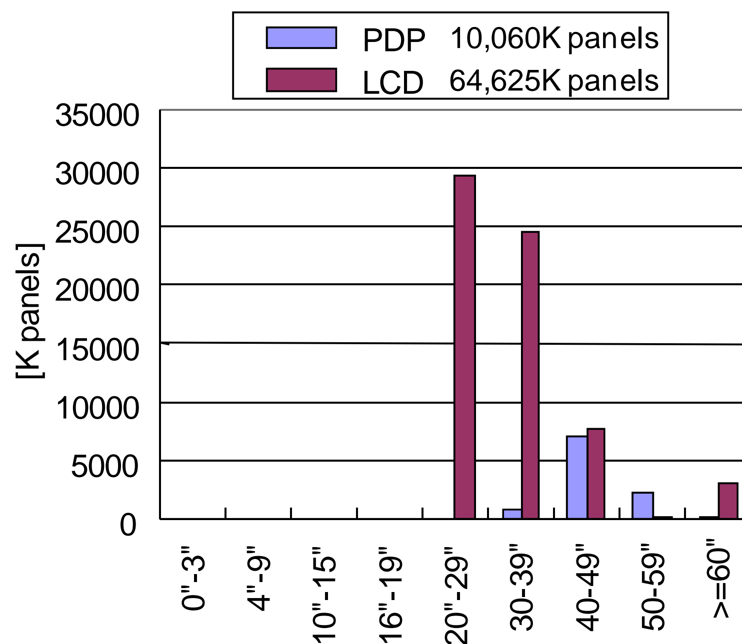


Fig. 83 Comparison of shipment volume between PDP and LCD (Over 20-inch) [61]

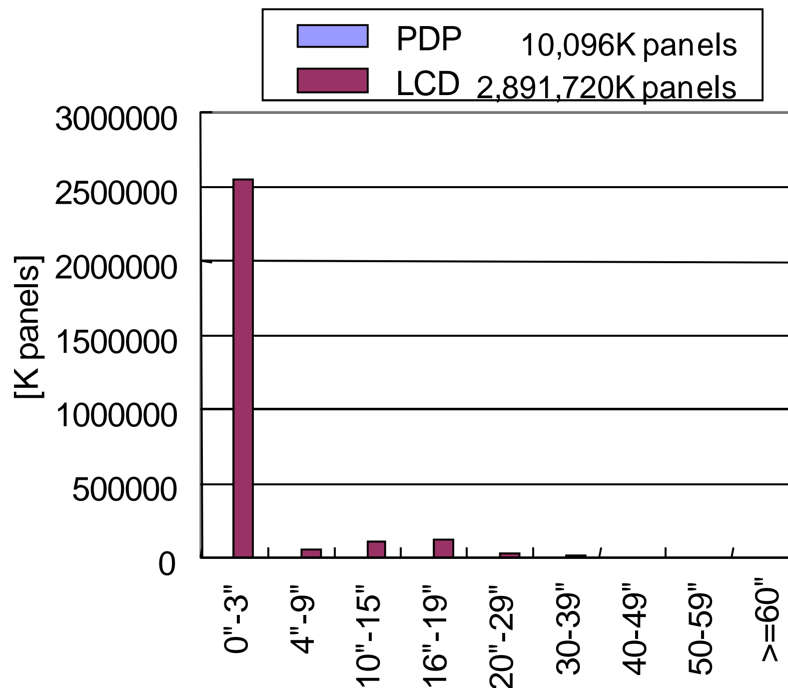


Fig. 84 Comparison of shipment volume between PDP and LCD (All size) [61]

3.3 Production yield simulation for large size display and a "Scalability" scenario of robust large display manufacturing

To make a successful large OLED TV happen, it is very important to judge the risk level by increasing the display size. In semiconductor and TFT-LCD field, yield simulation is widely used to predict the manufacturing applicability of new product designs. R.Troutman made an analysis about the defect number change when the display size is increased. He concluded that very low defect density would be required if no repair method is applied to large size. [62] Similar case can be applied to active-matrix OLED displays.

It is known that Poisson equation can be applied to calculate the probability of having *k* pieces of defective pixel on a display as follows.

$$P_{SC}\{k\} = \frac{\lambda_{SC}^{k}}{k!} e^{-\lambda_{SC}} \quad \text{(Eq.24)}$$

(λ_{sc}: average number of defective pixel on a display)

Fig. 85 illustrates the probability of point defect number calculated by this equation. As the average number is increased, distribution of the curve is also widened.

When the criteria of allowable defective pixel number is N_{SCT} , production yield can be expressed as,

$$Y_{SC} = \sum_{k=0}^{N_{SCT}} \frac{\lambda_{SC}^{k}}{k!} e^{-\lambda_{SC}} \quad \text{(Eq.25)}$$

(Only point defect is taken into consideration for this calculation.)

Fig. 86 shows the parameters of various display resolution and sizes used for the yield simulation. TFT interlayer overlap area and OLED interlayer overlap area are measured using actual display design. (2.2": Kodak LS633, 2.5": ALE294 module, 8.1": Kodak OLED wireless frame, 14": Prototype, 20", 32": displays designed for simulation) To make the simulation model simpler, TFT fault is assumed to cause lit defect and OLED fault is assumed to cause unlit defect. Number criteria of allowable point defects are assumed to be one and three for lit and unlit defect respectively for simplicity. Also in this simulation, it is assumed that the number of defect is proportional to the overlap area.

The simulation result is shown in Fig. 87. In this simulation, 2.2" lit defect average is assumed to be 0.01 per panel and 0.03 per panel for unlit defect, typical number for shadow mask patterning process. It clearly shows that, though the yield loss of 2.2"QCIF device is negligible like 0.005%, the production yield loss of large display, such as 32"HDTV, would be very large like 98%. In reality, the allowable point defect number is increased as the display becomes larger. Simulation result in Fig. 88 takes such effect into account. Allowable unlit defect number is increased from one to six, depend on the display size according to the customer's hearing. Even in this case, yield loss of 32"HDTV is 87% and is very high. The result indicates that the production yield is significantly reduced as the display size becomes larger.

As discussed, the production yield is very much sensitive to the display size. However, the situation is totally relaxed if the defective ratio is reduced. Fig. 89 shows the case of $1/10^{th}$ defective pixels for 2.2-inch. The yield loss of 32-inch is reduced from 87% (Lit defect: 0.01 per panel and unlit defect: 0.03 for 2.2".) to 1.9% (Lit defect: 0.001 per panel and unlit defect: 0.003 for 2.2".) by changing the defect ratio assumption. Fig. 90 shows the yield loss change due to defective ratio assumption difference. "1/n" in the graph means the case when lit defect density is 0.01/n per panel and unlit defect density as 0.03/n for 2.2"QCIF panel. It is assumed that the number of defect is increased proportionally to the overlapped area as before. The graph indicates that defect ratio improvement has significant impact on

the manufacturing yield increase. Shadow-mask patterning method has inherently demerit in the particle generation due to, such as mask-organic contact, mask-electrode contact and debris accumulation on the mask itself. It makes sense to consider patterning method that can decrease the possibility of yield loss due to particles, such as color-by-white method. (Also known as white+color filter method.)

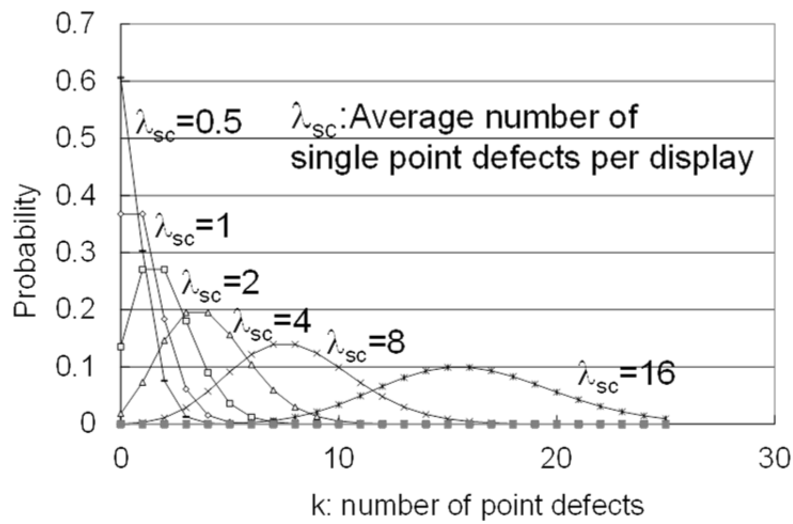


Fig. 85 Probability of point defect number in a display

	2.2"QCIF	2.5"QVGA	8.1" WVGA	14"WXGA	20"WXGA+	32"HDTV
Horizonal number of lines	862	960	3200	5120	5760	7680
Vertical number of lines	240	240	480	768	900	1080
TFT Interlayer overlap area per subpixel [μm^2]	651	937	2314	2773	3350	3428
OLED Interlayer overlap per subpixel [μm^2]	2246	2452	4860	5813	9000	14400

Fig. 86 Design parameters used for the yield simulation

		2.2"QCIF	2.5"QVGA	8.1" WVGA	14"WXGA	20"WXGA+	32"HDTV
Specification	TFT fault (Assumption:Lit defect)	1	1	1	1	1	1
	OLED fault (Assumption: Unlit defect)	3	3	3	3	3	3
Defect	Lit defect (Avg)	0.0100	0.0160	0.2639	0.8096	1.2895	2.1112
	Unlit defect (Avg)	0.0300	0.0365	0.4820	1.4758	3.0123	7.7115
	Yield loss due to lit defect (Theoretical)	0.0%	0.0%	2.9%	19.5%	36.9%	62.3%
	Yield loss due to unlit defect (Theoretical)	0.0%	0.0%	0.2%	6.3%	35.6%	94.9%
	Yield loss due to point defects (Theoretical)	**0.005%**	**0.013%**	**3.1%**	**25%**	**59%**	**98%**

Fig. 87 Yield loss simulation result (constant allowable point defect number case)

		2.2"QCIF	2.5"QVGA	8.1" WVGA	14"WXGA	20"WXGA+	32"HDTV
Specification	TFT fault (Assumption:Lit defect)	1	1	1	1	1	1
	OLED fault (Assumption: Unlit defect)	3	3	4	4	6	6
Defect	Lit defect (Avg)	0.0100	0.0160	0.2639	0.8096	1.2895	2.1112
	Unlit defect (Avg)	0.0300	0.0365	0.4820	1.4758	3.0123	7.7115
	Yield loss due to lit defect (Theoretical)	0.0%	0.0%	2.9%	19.5%	36.9%	62.3%
	Yield loss due to unlit defect (Theoretical)	0.0%	0.0%	0.0%	1.7%	3.4%	65.0%
	Yield loss due to point defects (Theoretical)	**0.005%**	**0.013%**	**2.9%**	**21%**	**39%**	**87%**

Fig. 88 Yield loss simulation result (Increasing allowable point defect number case)

		2.2"QCIF	2.5"QVGA	8.1" WVGA	14"WXGA	20"WXGA+	32"HDTV
Specification	TFT fault (Assumption:Lit defect)	1	1	1	1	1	1
	OLED fault (Assumption: Unlit defect)	3	3	4	4	6	6
Defect	Lit defect (Avg)	0.0010	0.0016	0.0264	0.0810	0.1289	0.2111
	Unlit defect (Avg)	0.0030	0.0036	0.0482	0.1476	0.3012	0.7712
	Yield loss due to lit defect (Theoretical)	0.0%	0.0%	0.0%	0.3%	0.8%	1.9%
	Yield loss due to unlit defect (Theoretical)	0.0%	0.0%	0.0%	0.0%	0.0%	0.0%
	Yield loss due to point defects (Theoretical)	**0.00005%**	**0.0001%**	**0.03%**	**0.31%**	**0.76%**	**1.9%**

Fig. 89 Yield loss simulation result of 1/10th fault (Increasing allowable point defect number case)

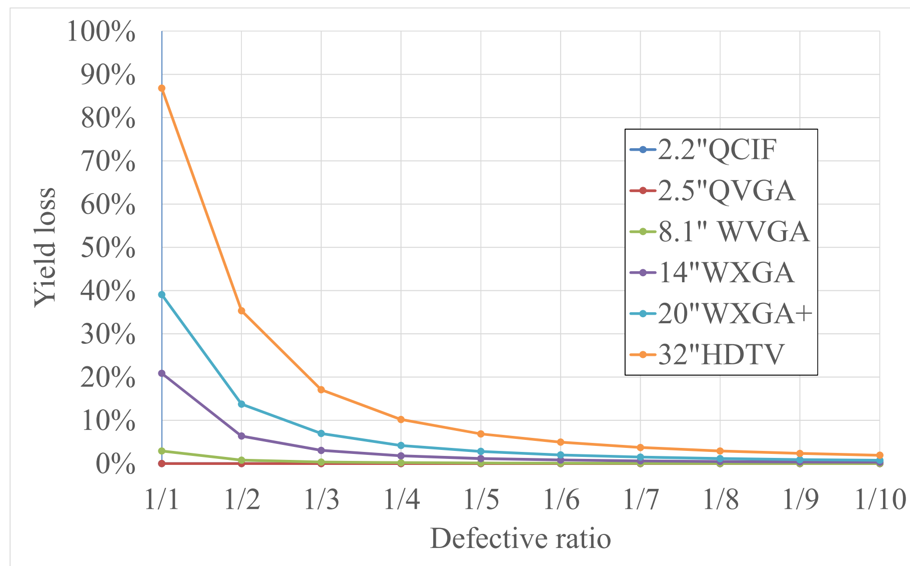


Fig. 90 Yield loss change due to defective ratio assumption

3.4 Choice of technologies for robust manufacturing

As discussed in 3.3, the production yield is significantly reduced as the display size is increased. To secure the manufacturing yield of large display, the technology applied must have robust manufacturing applicability regardless of the size.

Though an approach to design a large AMOLED display using a-Si TFT was reported in Section-2, a-Si TFT has low mobility, so the pixel circuit using the technology is large, which will cause low production yield due to electric short and

open. There was no other TFT technologies to go beyond ELA size limit at the time of Section-2 activities, however after that, many other TFT backplane technologies have been appeared for choice. If high mobility with stable TFT feature can be used, the display design would become much easier and can attempt to have more suitability for manufacturing.

Table 6 describes various display technologies and its applicability to small and large displays. RGB pixelation and poly-silicon TFT by excimer laser annealing have issues when they are applied to large displays. To satisfy with the requirement discussed in 3.3 for making large AMOLED display happen, it is necessary to choose the technologies having compatibility for both small and large displays, namely scalability. As discussed later, color-by-white OLED fabrication, TFT by solid-phase crystallization (Metal-induce polysilicon TFT) and external compensation (GMC method: Global Mura Compensation) are used from the scalability aspect for the prototype study.

		Small display	Large display
OLED	RGB pixelation by shadow mask	OK	Poor yield
	Color-by-white method	OK	OK
TFT	Poly-silicon TFT by excimer laser annealing	OK	Tool size limitation
	Poly-silicon by solid phase crystallization	OK	OK
	Amorphous silicon TFT, Micro-crystalline TFT	OK	OK
	Oxide TFT	OK	OK

Table 6 Scalability of display technologies

4 Choice of OLED structure

4.1 Consideration of performance difference between W-RGB and W-RGBW method

"Color-by-white" approach can give higher production yield than "RGB pixelation" approach, which will bring better probability of success for large AMOLED display manufacturing according to 3.3.

Fig. 91 illustrates the difference between "RGB pixelation" method and "Color-by-white" method. With RGB pixelation (Fig. 91 left figure), red, green and blue sub-pixel OLED devices are formed on the transparent electrode and the emission from each color is directly extracted through the substrate to the air. This method has merit in low light absorption, however has demerit in the production yield loss when shadow-masking method is used for color patterning. On the other hand, "Color-by-white" approach (Fig. 91 right figure) uses white emission OLED device. The white emission light goes through the color filter with red, green and blue transmission spectrum, which provides red, green and blue light output to the air. The difference in production yield between RGB pixelation and color-by-white approach is originated from the color patterning yield difference between shadow-masking and color filter. Fig. 92 shows the, so called, Dark-Spot defect due to shadow mask particle. During shadow-masking patterning process, shadow mask, normally made of stainless steel or nickel alloy, contacts with the organic layer or metal electrode layer of OLED device on glass substrate, which scratches the device and forms organic or inorganic debris. The particle creates pin hole in cathode electrode and passivation films so that the external moisture can sneak into the OLED device and forms non-emissive region to create dark-Spot defects. Also due to the shadow-mask deformation caused by various reason, such as thermal expansion or lack of shadow-mask frame rigidity, creates irregular patterning as shown in Fig. 93 (Green sub-pixel region is showing slight red emission in this case).. The irregular patterning causes colored non-uniformity as can be seen in Fig. 94. Shadow-mask patterning is a process having such complexity that causes production yield loss. In contrast, color filter patterning has been used in TFT-LCD industry for a quarter century and is very much mature with over 95% production yield, even for more than 50-inch display size. It is clear that the production yield of AMOLED display would be significantly improved by switching from RGB pixelation to color-by-white method as discussed in 3.3. However, as the color filter absorbs OLED mission, so the power consumption would be increased. Ecology has

been identified as a very important target for the industry, OLED also needs to achieve low power consumption, hopefully equivalent or better than conventional TFT-LCD displays.

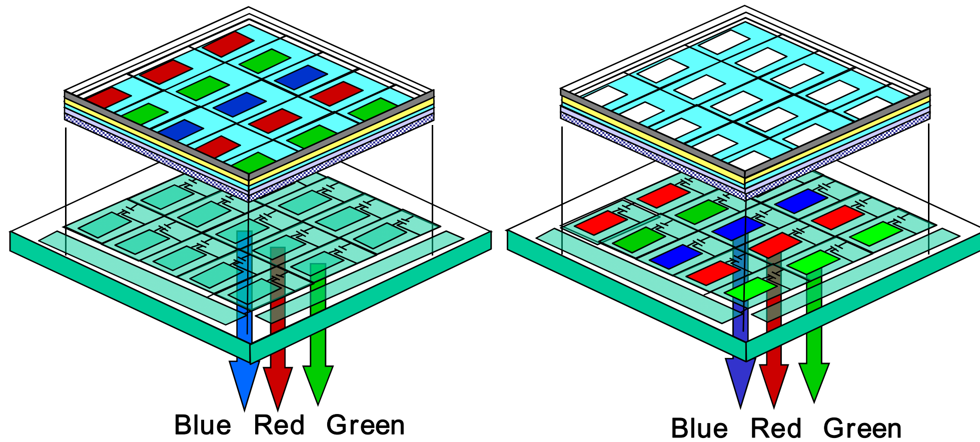


Fig. 91 Comparison between "RGB pixelation" approach and "Color-by-white" approach

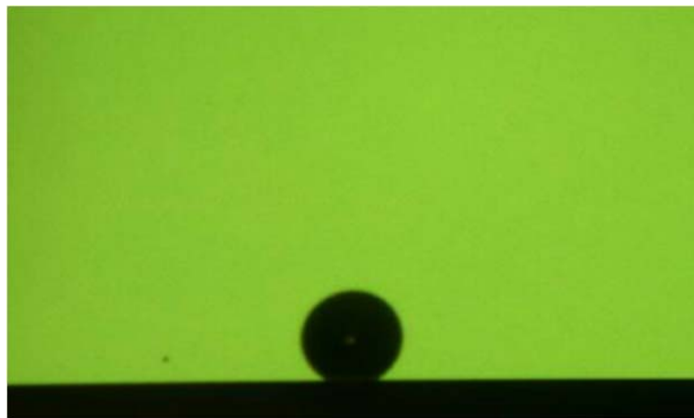


Fig. 92 Dark-spot generated by shadow-mask particle

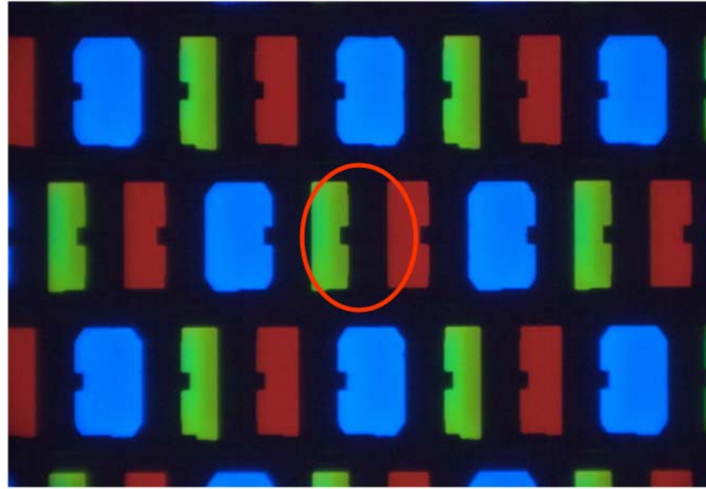


Fig. 93 Misalignment of red sub-pixel region caused by shadow-mask process

Fig. 94 Colored non-uniformity region caused by shadow-mask process

To circumvent the power consumption issue, four color sub-pixel approach (driven by white, red, green and blue) has been proposed by A.Arnold [63]. Fig. 95 left figure shows conventional color-by-white approach. (The same as right figure of Fig. 91. This is called "W-RGB" configuration.) White OLED emission goes through color filter with red, green and blue transmittance spectrum to form colored light output. The right figure in Fig. 95 has additional white sub-pixel in parallel to red, green and blue sub-pixel. (This is called "W-RGBW" configuration.)

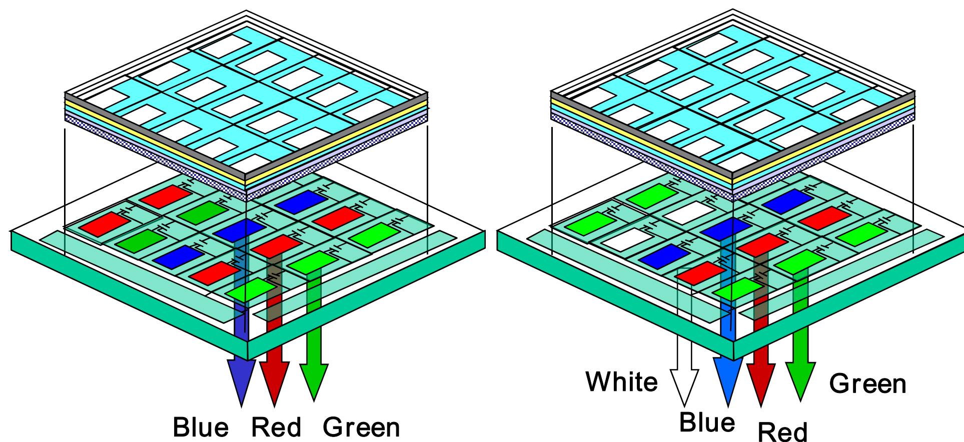


Fig. 95 Comparison between "W-RGB" sub-pixel configuration and "W-RGBW sub-pixel configuration

Fig. 96 shows the example of light output efficiency for each sub-pixel. In W-RGB method case, as an example of efficiency, 36.5 [cd/A] white emission goes through the red, green and blue color filter. As some portion of light is absorbed by the color filters (red: 21.3%, green: 52.8%, blue: 8.7% transmittance in this case.), the light output from each color-filter are, 7.8 [cd/A], 19.3 [cd/A], 3.2 [cd/A] respectively. (3.197 time the current is necessary to make D65 white by color-filtered red, green and blue component than 36.5 [cd/A] D65 white.) A.Arnold's idea is that, as white is made by the mixture of red, green and blue component, unfiltered highly-efficient white component can be used to substitute the white component made by filtered light, which will significantly reduce the power consumption. Arnold's paper claims half the power consumption with W-RGBW configuration than W-RGB configuration.

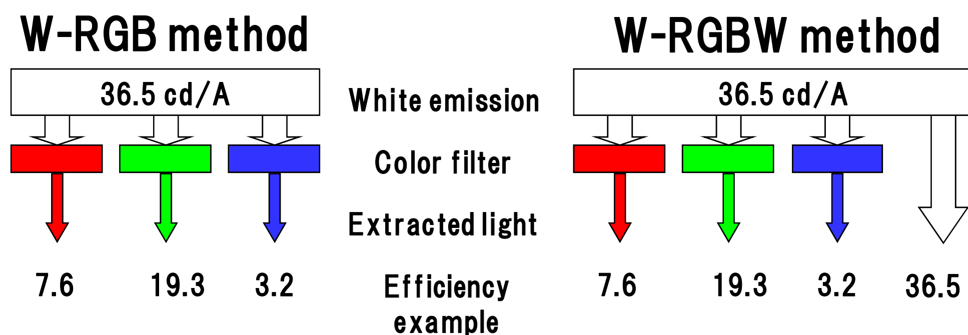


Fig. 96 Efficiency example of W-RGB method and W-RGB method proposed by A.Arnold [63]

With Arnold's algorithm, the triangle on CIE coordinate made by the red-green-blue color primaries are divided into three regions.

Region-1) Region within the triangle made by the white point, blue and green (Fig. 97)

Region-2) Region within the triangle made by the white point, green and red (Fig. 98)

Region-3) Region within the triangle made by the white point, red and blue (Fig. 99)

In Region-1, red sub-pixel takes the rest, in Region-2, blue takes the rest and in Region-3, green takes the rest. Most efficient white sub-pixel is always used in this algorithm.

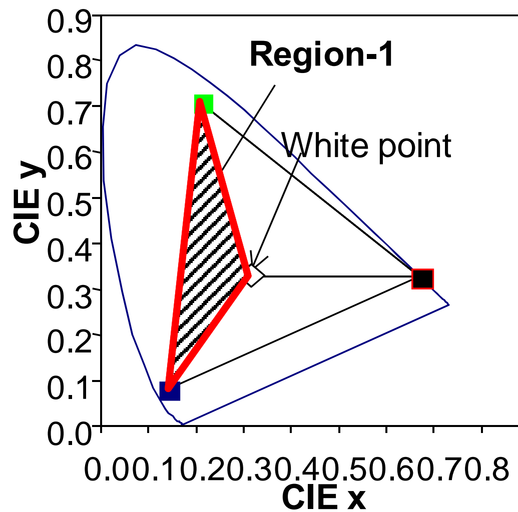


Fig. 97 Color mixture for Region-1

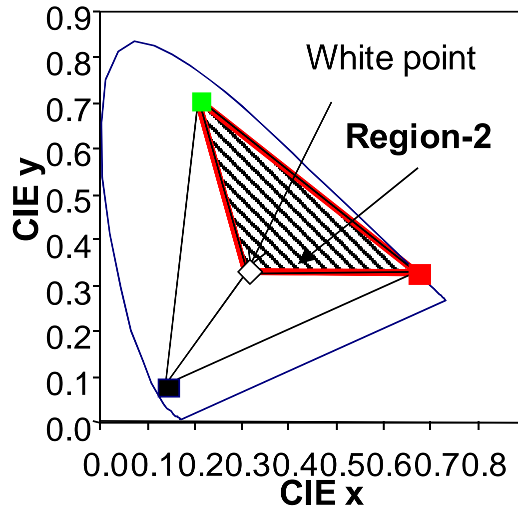


Fig. 98 Color mixture for Region-2

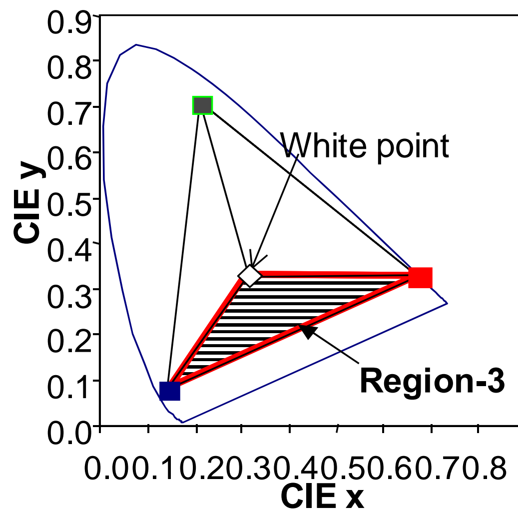


Fig. 99 Color mixture for Region-3

4.2 Issues of color-by-white method for large displays

Though color-by-white approach has merit in terms of production yield, tradeoff between color gamut and display power was a serious issue. For example, in 2005, Kodak and Sanyo released two OLED display products, ALE293 (Color-by-white) and ALE294 (RGB side-by-side) manufactured in SK Display (a joint manufacturing company between these two). The performance [64] of these two products shows good comparison between two technologies.

Method	Power consumption	Color reproduction
Color-by-white	451mW (converted from 2.2-inch to 2.5-inch)	60%NTSC
RGB side-by-side	350mW (2.5-inch)	81%NTSC

Table 7 Power consumption difference between two major display structure as of 2005.

It clearly shows that color-by-white method had disadvantage in terms of power consumption and color gamut, at the time.

Also several papers claimed that color-by-white approach had demerit in power consumption and color gamut, such as,

(1) "LIPS Technology for Manufacturing Large-Sized OLED Displays", IDW2007, p.233.[65]

"*As the alternative methods, white OLED with color filter (WOLED+CF) device has been expected because it does not require OLED patterning process or shadow masks. Sony demonstrated the WOLED+CF prototype display at SID 2004. However higher power consumption and color impurity are the issues of this method for TV application.*", the paper claims in page 233.

(2) "The Outstanding Potential of OLED Displays for TV Applications", Information Display 2008, p.14 [66]

"*A white-emission plus color-filter device has the simplest structure, so the production cost is estimated to be the lowest among these three options. Since the patterning process of the OLED layer is not required in this case, use of a metal mask is not necessary. However, power consumption is a real problem because more than two-thirds of the energy of the white emission from an OLED is absorbed by the color filter. Furthermore, this type of device gives rise to a severe tradeoff between color gamut and brightness. Adding a white subpixel (RGBW color filter) is a potentially smart way to compensate for the transmission loss caused by the RGB color filter. However, a polarizer and quarter-wavelength plate must be put on the panel to eliminate the reflection caused by the white subpixel, once again resulting in a power loss of more than 50%.*", the paper claims in page 16.

As an example, the paper by Hamer et al. in SID 2007 [67] claimed a 14.1" WXGA AMOLED display by W-RGBW method, however it had only 78%NTSC

color gamut, which was far smaller value than the RGB pixelation OLED display that was already achieving 100% NTSC on cellular phone displays. With color-by-white method, higher color gamut means low transmittance color filter use, which increases the power consumption. Power consumption and color gamut were a significant tradeoff, which was making high manufacturability merit of color-by-white method as useless.

Then, in my study, it was investigated if there is any way to get rid of the tradeoffs, so that both low power consumption and high color gamut can be satisfied.

4.3 Analysis of W-RGBW approach to circumvent its tradeoff situation

Though power consumption can be reduced with W-RGBW method as M.Murdoch pointed out, the display power consumption depends on the image content and could not be calculated without experiment. However for the product design, design-experiment iteration takes extra time for development and is not adequate for product planning.

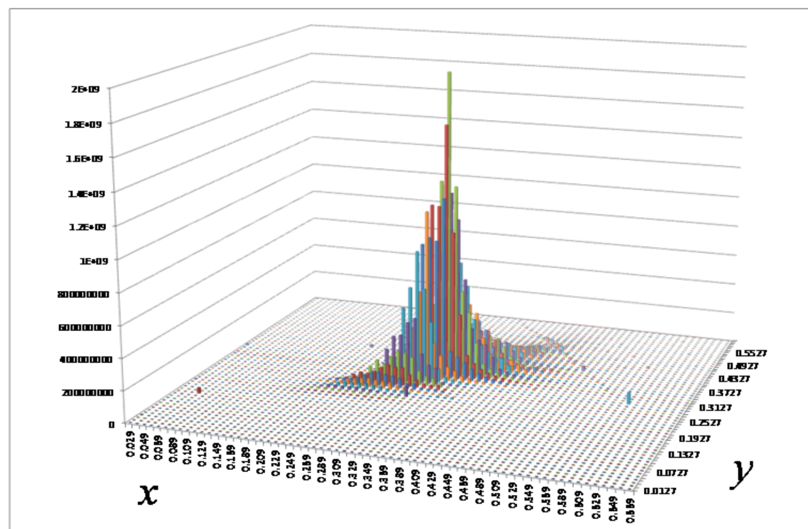


Fig. 100 Histogram of pixel colors in 19419 images (Linear scale)

Fig. 100 shows the histogram of pixel colors in arbitrarily-selected 19419 picture images. This histogram is a replication experimental statistics of A.Arnold's experiment and actually showing very similar shape. [63] This is large enough data quantity and would be showing typical histogram shape of picture images. (In this thesis, the histogram experiment data is used to analyze the color-by-white AMOLED display performance, so that the tradeoff between power consumption and color gamut can be optimized.)

Total pixel number in this analysis is N_{total}=52,464,357,936. It clearly shows that almost all the pixel color is close to the white point color coordinate and the probability of vivid colors, which is apart from the white point, is negligible.

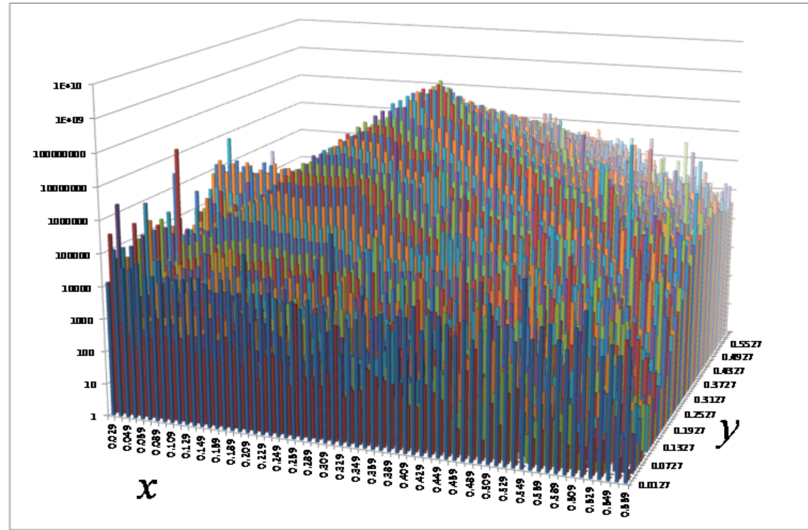


Fig. 101 Histogram of pixel colors in 19419 images (Log scale)

Fig. 101 shows logarithmic plot of histogram and the shape looks like a cone having a white point coordinate as a summit. Cone surface shape can be described as following.

$$(x-x_w)^2+(y-y_w)^2=[\{\log_e(z_{\max})-\log_e(z)\}/a]^2 \quad \text{......} (Eq.26)$$

where z is frequency of each color coordinate, (x_w, y_w) is white point color coordinate, $z=z_{max}$ is the top of the cone and a is the slope of the cone surface in Fig. 101. By the least squares method, Eq.26 can be written as,

$$(x-0.31271)^2+(y-0.32902)^2=[\{20.950-\log_e(z)\}/40.516]^2 \quad \text{..........} (Eq.27)$$

Then, the probability of having color coordinate (x,y) can be calculated as,

$$P(x,y)=z/N_{total}=\frac{1}{N_{total}}\exp\left(\log_e(z_{\max})-a\sqrt{(x-x_w)^2+(y-y_w)^2}\right)$$

$$\text{..........} (Eq.28)$$

where N_{total}=52,464,357,936, a=40.516, $log_e(z_{max})$=20.950, x_w=0.31271, y_w=0.32902.

Now we could obtain the probability of usage for each color coordinate. Calculating the power consumption for each color coordinate, we would be able to calculate the power consumption of a display when it shows picture images, without experiment using this equation.

(Remark: For display designers, the design of RGBW display was not easy, because the display power consumption depends on the images to be displayed. Therefore, the power consumption had to be actually measured using large number of images in the past. Cone-shape fitting of color-coordinate probability statistics described above made it possible to actually calculate the power consumption without measurement on a spreadsheet or coded program.)

(x,y) can be described using (X,Y,Z).

$$x = \frac{X}{X+Y+Z} \quad \text{(Eq.29)}$$

$$y = \frac{Y}{X+Y+Z} \quad \text{(Eq.30)}$$

Using Eq.29 and Eq.30,

$$X = \frac{xY}{y} \quad \text{(Eq.31)}$$

From Eq.30,

$$\frac{yX}{Y} + y + \frac{yZ}{Y} = 1 \quad \text{(Eq.32)}$$

Substituting Eq.31 for Eq.32,

$$Y = \frac{yZ}{1-x-y} \quad \text{(Eq.33)}$$

Using Eq.32

$$X = \frac{xZ}{1-x-y} \quad \text{(Eq.34)}$$

If the luminance is L, as Y=L,

$$(X,Y,Z) = (\frac{x}{y}L, L, \frac{1-x-y}{y}L) \quad \text{(Eq.35)}$$

When R,G,B primary color coordinate is (X_R,Y_R, Z_R), (X_G,Y_G, Z_G), (X_B,Y_B, Z_R) respectively , intended color coordinate can be achieved by the mixture of R,G,B

primary colors with a, b and c times amount respectively. (Definition-1: Y_B, Y_G, Y_R are defined as the luminance of each color sub-pixel when 1[A/m^2] current density flow is applied. Using this definition, *a*, *b* and *c* have the [A/m^2] unit, which is the current density to drive each sub-pixels.)

$$\begin{pmatrix} X \\ Y \\ Z \end{pmatrix} = \begin{pmatrix} X_R & X_G & X_B \\ Y_R & Y_G & Y_B \\ Z_R & Z_G & Z_B \end{pmatrix} \begin{pmatrix} a \\ b \\ c \end{pmatrix} \quad \text{(Eq.36)}$$

Therefore,

$$\begin{pmatrix} a \\ b \\ c \end{pmatrix} = \begin{pmatrix} X_R & X_G & X_B \\ Y_R & Y_G & Y_B \\ Z_R & Z_G & Z_B \end{pmatrix}^{-1} \begin{pmatrix} X \\ Y \\ Z \end{pmatrix} \quad \text{(Eq.37)}$$

similarly, white device can be described as following,

$$\begin{pmatrix} a_w \\ b_w \\ c_w \end{pmatrix} = \begin{pmatrix} X_R & X_G & X_B \\ Y_R & Y_G & Y_B \\ Z_R & Z_G & Z_B \end{pmatrix}^{-1} \begin{pmatrix} X_w \\ Y_w \\ Z_w \end{pmatrix} \quad \text{(Eq.38)}$$

Murdoch's method[68], maximum available white component is driven by white subpixel and the rest is driven by R,G,B sub-pixels. Therefore, dividing Eq.35 by Eq.38, following (X,Y,Z) component is driven by white sub-pixels. (Y_W is also defined as the luminance of white sub-pixel when 1[A/m^2] current density flow is applied.)

$$(X_{wpixel}, Y_{wpixel}, Z_{wpixel}) = \alpha \cdot (X_w, Y_w, Z_w) \quad \text{(Eq.39)}$$

where, α as the white sub-pixel current density.

Also, If $a/a_w = \min\{a/a_w, b/b_w, c/c_w\}$, $\alpha = a$,

if $b/b_w = \min\{a/a_w, b/b_w, c/c_w\}$, $\alpha = b$,

and if $c/c_w = \min\{a/a_w, b/b_w, c/c_w\}$, $\alpha = c$.

Fig. 102 shows the white sub-pixel current density of each (*x*,*y*) color coordinate according to Eq.39. High efficiency white sub-pixel is effectively used for near white point color coordinate.

(In this simulation, following current efficiency values are used; White: 36.5[cd/A], Red: 7.6 [cd/A], Green: 19.3 [cd/A], Blue: 3.2 [cd/A]. Assumed display luminance is 200 [cd/m^2].)

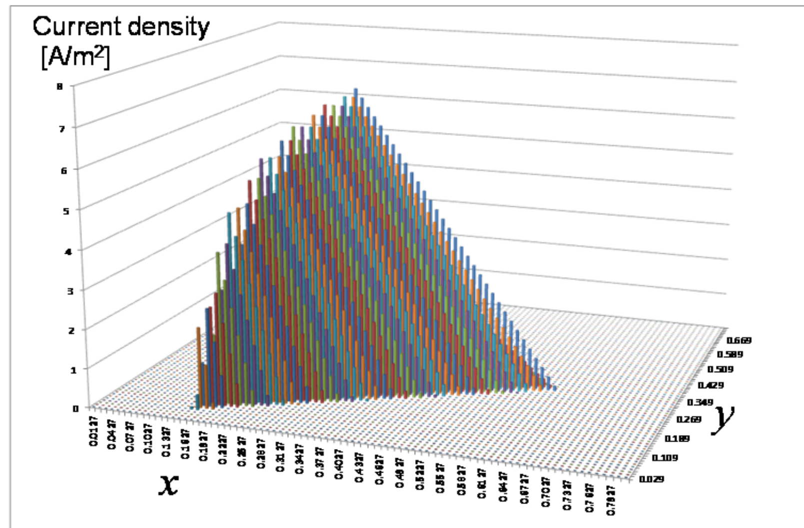


Fig. 102 White sub-pixel driving current for W-RGBW method

On the other hand, emission components driven by R,G,B sub-pixels can be described as following.

$$(X_{colorpixel}, Y_{colorpixel}, Z_{colorpixel}) = (X - X_{wpixel}, Y - Y_{wpixel}, Z - Z_{wpixel})$$

....(Eq.40)

$$\begin{pmatrix} a_{colorpixel} \\ b_{colorpixel} \\ c_{colorpixel} \end{pmatrix} = \begin{pmatrix} X_R & X_G & X_B \\ Y_R & Y_G & Y_B \\ Z_R & Z_G & Z_B \end{pmatrix}^{-1} \begin{pmatrix} X_{colorpixel} \\ Y_{colorpixel} \\ Z_{colorpixel} \end{pmatrix}$$ ....(Eq.41)

Therefore, the current density $[A/m^2]$ for white, red, green and blue can be described as,

$$J_w = \alpha$$

$$J_R = a_{colorpixel}$$

$$J_G = b_{colorpixel}$$ ....(Eq.42)

$$J_B = c_{colorpixel}$$

Fig. 103, Fig. 104 and Fig. 105 are the current density for R,G and B sub-pixel respectively. Color primaries usage is dramatically increased near the pure color region.

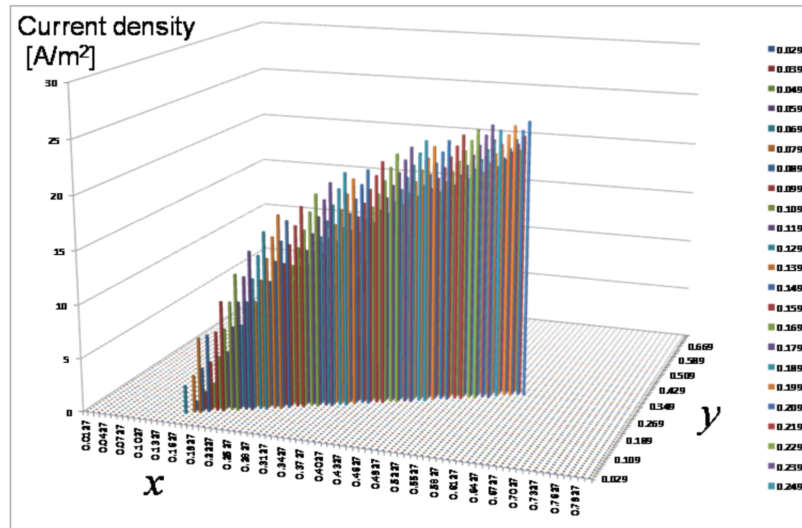


Fig. 103 Red sub-pixel driving current for W-RGBW method

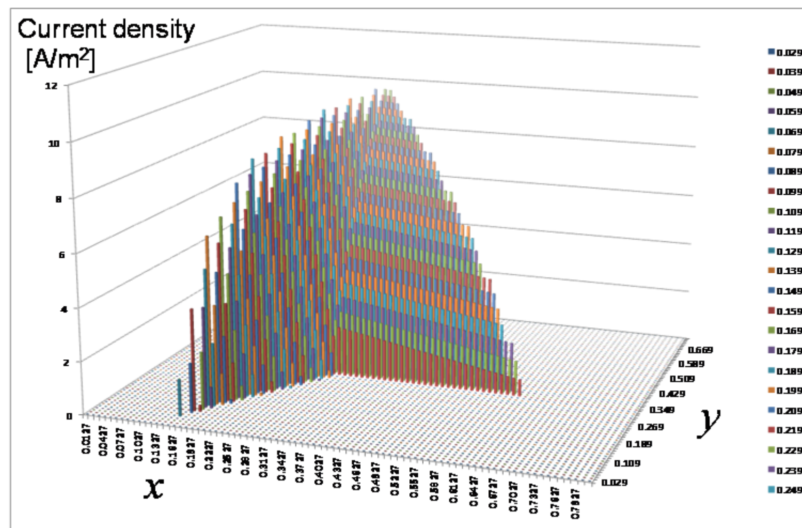


Fig. 104 Green sub-pixel driving current for W-RGBW method

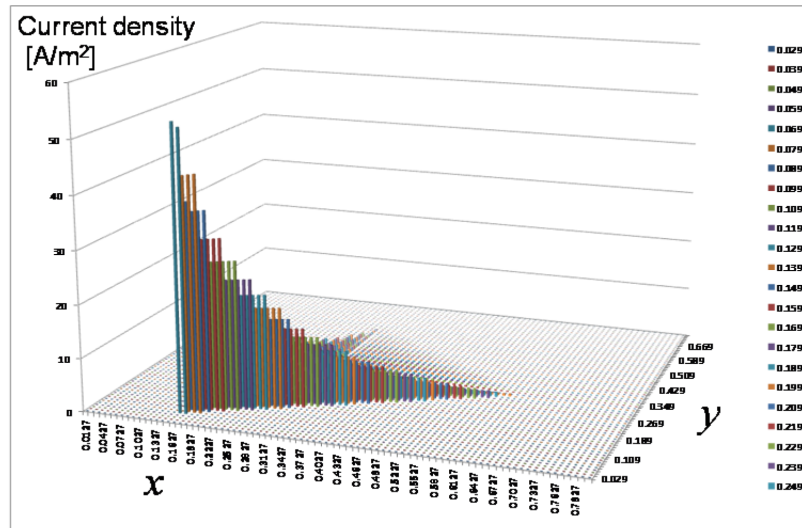


Fig. 105 Blue sub-pixel driving current for W-RGBW method

Total current density for color coordinate (x,y) can be expressed as,

$$J_{TOTAL}(x,y) = J_W(x,y) + J_R(x,y) + J_G(x,y) + J_B(x,y) \quad \cdots\cdots\cdots\cdots \text{(Eq.43)}$$

Fig. 106 shows the current density of (x,y) color coordinate according to Eq.43. Current density shows minimum value at white point and gradually increases as the color is saturated (larger chroma value). Especially, the current density shows very high value near blue color coordinate, as the current efficiency of blue is not very good.

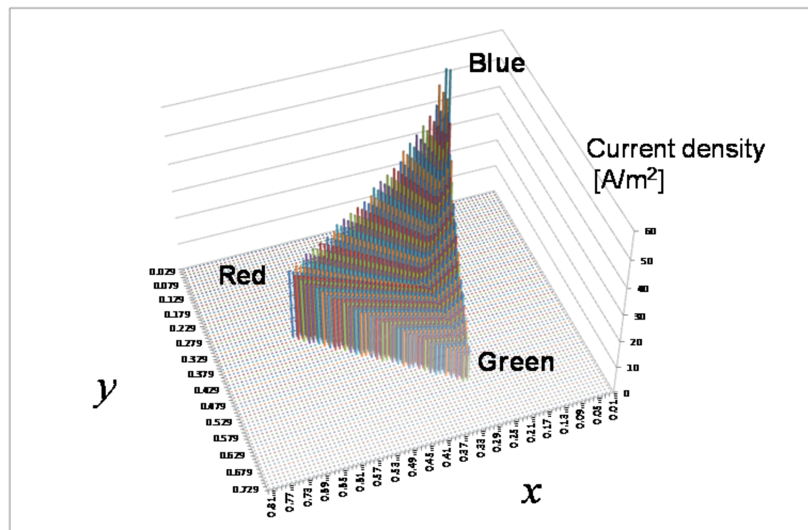


Fig. 106 Total (W+R+G+B) driving current for W-RGBW method

Though pure colors, especially blue, have large current consumption, the

probability of having saturated colors is extremely low according to Fig. 100. To estimate the actual current consumption contribution in a display, Fig. 100 needs to be multiplied by Fig. 106.

$$J_{PICTURE}(x, y) = J_{TOTAL}(x, y) \cdot P(x, y) \cdots\cdots \text{(Eq.44)}$$

Eq.44 gives the histogram of current density of color coordinate (*x*,*y*) as shown in Fig. 107. Pure colors gives minor contributions and most of the current consumption is still made by near-white region. Adding the current density for all the *x* and *y*, the total current density, 9.386A/m^2, was calculated using Fig. 107 for W-RGBW OLED display. Similarly W-RGB OLED display (without white sub-pixel) was simulated and the current density was 21.060 A/m^2.

According to this simulation, it was concluded that W-RGBW OLED display has almost half (1/2.2437) the current consumption of W-RGB OLED display. (In this simulation, no correlation between gray level and color coordinate is assumed.) This corresponds to the observation "half" by the paper of A.Arnold very well. [63]

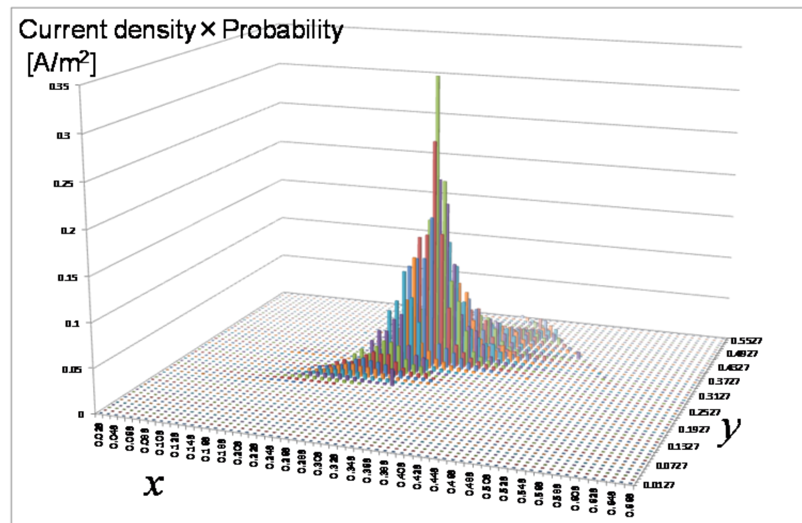


Fig. 107 Current density of color coordinate (*x*,*y*) for actual display showing picture image

When red (7.6 [cd/A]), green (19.3 [cd/A]) and blue (3.2 [cd/A]) are used to create D65 white emission without white sub-pixel component, the efficiency is 1/3.1970 times the white sub-pixel emission (36.5[cd/A]), If Fig. 107 had delta function distribution at white point, the current consumption of W-RGBW would be 1/3.1970 times and has no dependence on the RGB sub-pixel efficiency. However, as the histogram distribution has some width, the gain by using the W-RGBW

approach would be reduced to some degree, down to 1/2.2437.

As to the region apart from the white point, there is almost no contribution according to Fig. 107 due to extremely low possibility of occurrence. In actual, driving current does not change very much due to the RGB sub-pixel efficiency change. (Fig. 108)

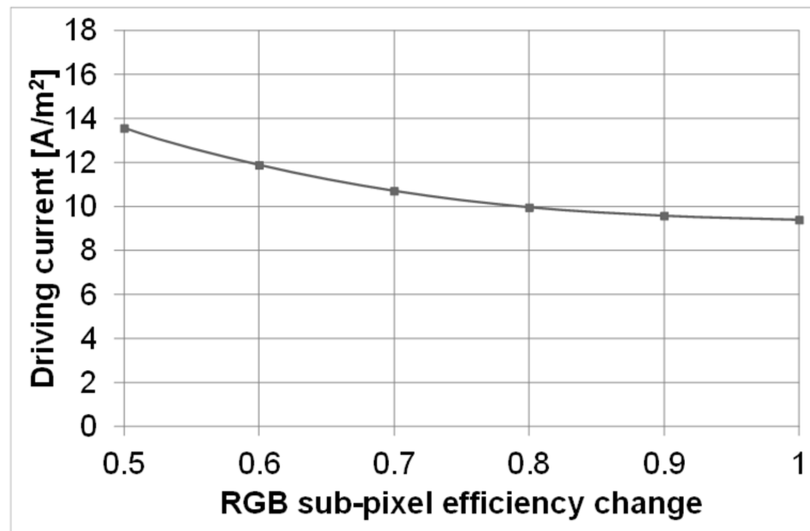


Fig. 108 Driving current dependence of RGB sub-pixel efficiency in W-RGBW system

As R,G,B sub-pixel emissions do not affect the power consumption very much, if we can increase the white intensity without affecting the R,G,B emission intensity, the display power efficiency would be increased with no color-reproducibility handicap. However, R,G,B emission is made from white emission, so R, G, B emission should be proportional to the white emission if white spectrum shape is kept the same. To overcome this situation, a trick can be applied.

For simplicity, Fig. 109 shows idealistic R,G,B sub-pixel emission spectrum after the white light goes through each color filter. If additional peak(s) between the R,G,B emission spectrum like Fig. 110 (yellow and/or sky blue) is added to the white emission, the efficiency of white would be increased. Especially peak-2 in Fig. 110 (yellow ~ orange) increases the efficiency very much because such wavelength is very sensitive according to human eye's relative luminosity curve. At the same time, such additional peak are blocked by color filter, as they are within the color filter's absorption spectrum, when saturated color is displayed. Therefore, by adding such new spectrum emission, power consumption of an AMOLED

display would be reduced without sacrificing the color reproduction.

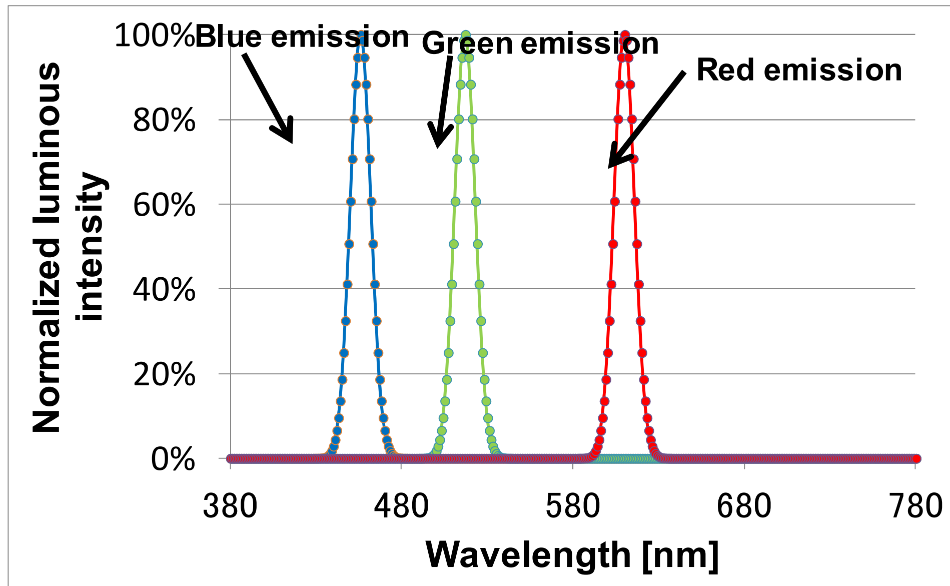


Fig. 109 Idealistic R,G,B sub-pixel spectrum after passing color filter

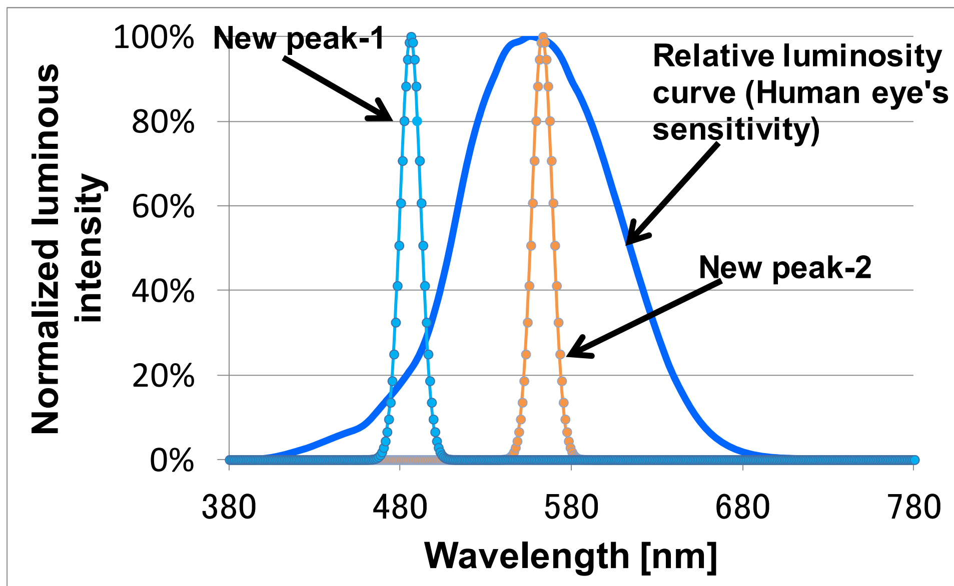


Fig. 110 Additional emission peak to be added in white emission

To verify the hypothesis, idealistic Gaussian spectrum peak added to the white OLED emission and also idealistic Gaussian red / green / blue color filter peaks are assumed for simulation purpose. (In actual implementation, additional

complementary color is necessary to keep white point.) Fig. 112 shows the simulation result of LCD-like wide spectrum color filter. Solid line shows the color gamut change when new additional peak is added to each wavelength as a peak. Contrary to the intended purpose, color gamut is decreased when an emission peak is added between the color filter transmission peak. (Such as near 470nm and 580nm.) The reason of gamut decrease would be due to the light leakage by the color filter transmission slope in the spectrum. To avoid such light leakage, it is necessary to completely block the OLED emission peak by R/G/B color filter. Therefore, the spectrum overlap should be minimized. To verify it, narrow color filter spectrum case was simulated in Fig. 113. It clearly shows that with minimum overlap of color filter spectrum, color gamut can be kept (~580nm) when new additional OLED emission peak is added to the wavelength between color filter peaks.

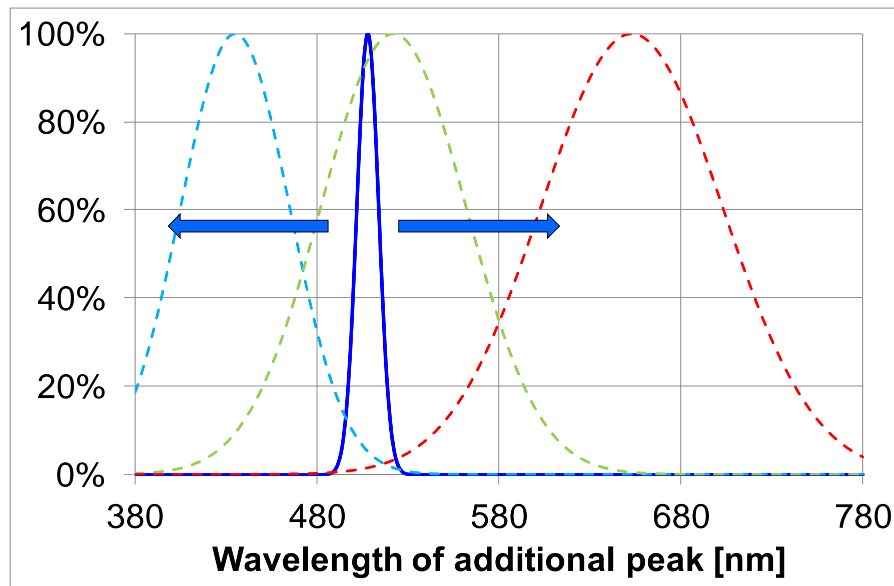


Fig. 111 New additional peak for simulation

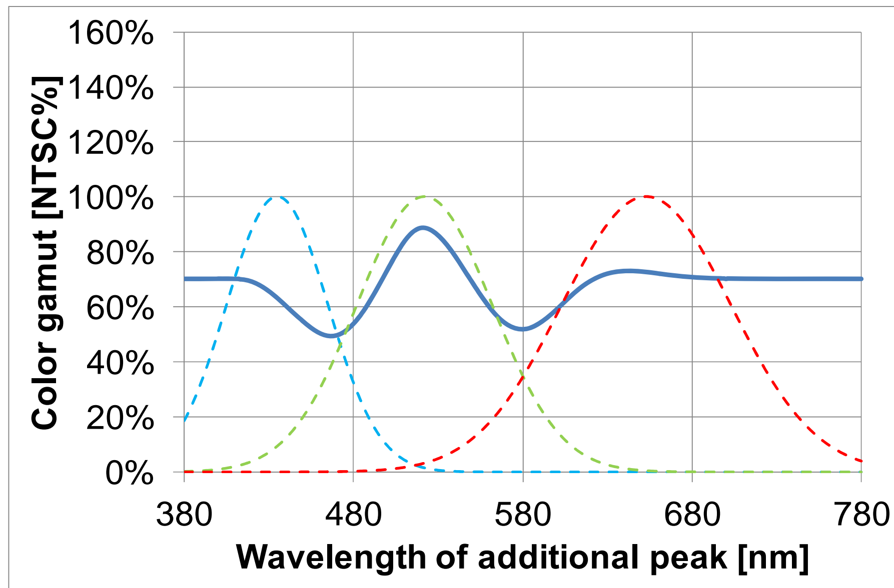


Fig. 112 Wide spectrum color filter case simulation

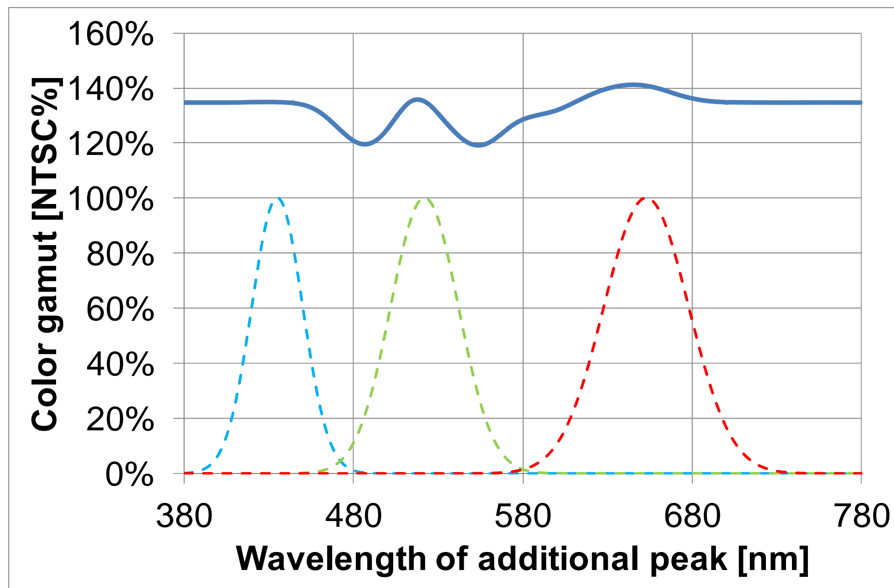


Fig. 113 Narrow spectrum case simulation

Then it was verified how much improvement such intermediate-peak-addition approach can bring using actual OLED emission and color filter. Following table shows the data used in the simulation.

	x	Y	Current efficiency
Red	0.64	0.33	7.6 [cd/A]
Green	0.30	0.60	19.3 [cd/A]
Blue	0.15	0.06	3.2 [cd/A]
White (D65)	0.31	0.33	36.5 [cd/A]

Table 8 Performance assumption used in the simulation

Fig. 114 is the simulation result when assumed white sub-pixel efficiency is changed, keeping R,G,B efficiency the same. As the white sub-pixel efficiency is increased, W-RGBW display driving current is decreased. This trend tells that if white efficiency is further increased, ratio between W-RGB and W-RGBW current consumption would become larger like 3~4 times. Though A.Arnold's paper was claiming that the gain of W-RGBW method, as compared with W-RGB, is twice, it was found that there is a way to increase the gain much further in this simulation as shown in Fig. 115.

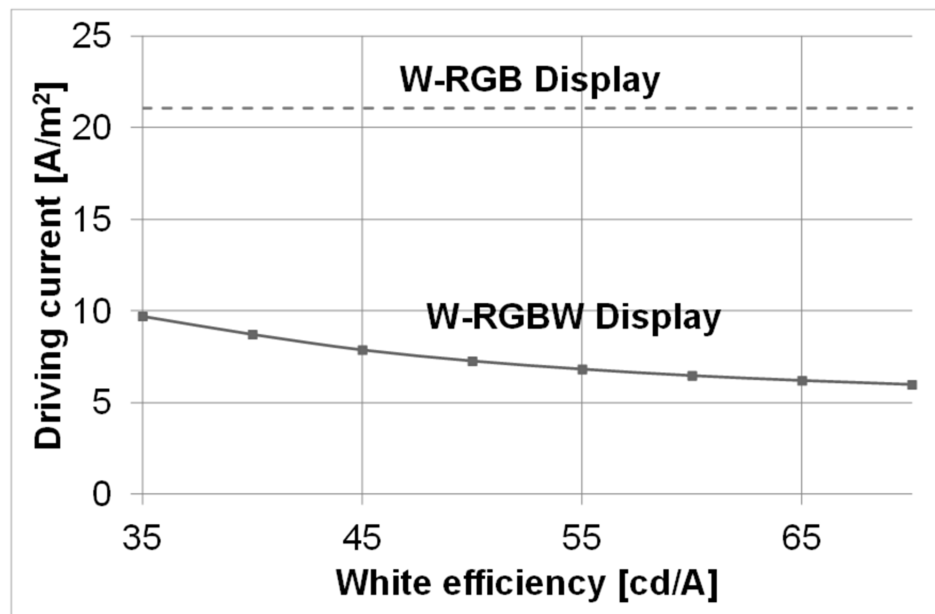


Fig. 114 Driving current comparison between W-RGB and W-RGBW with various white efficiency

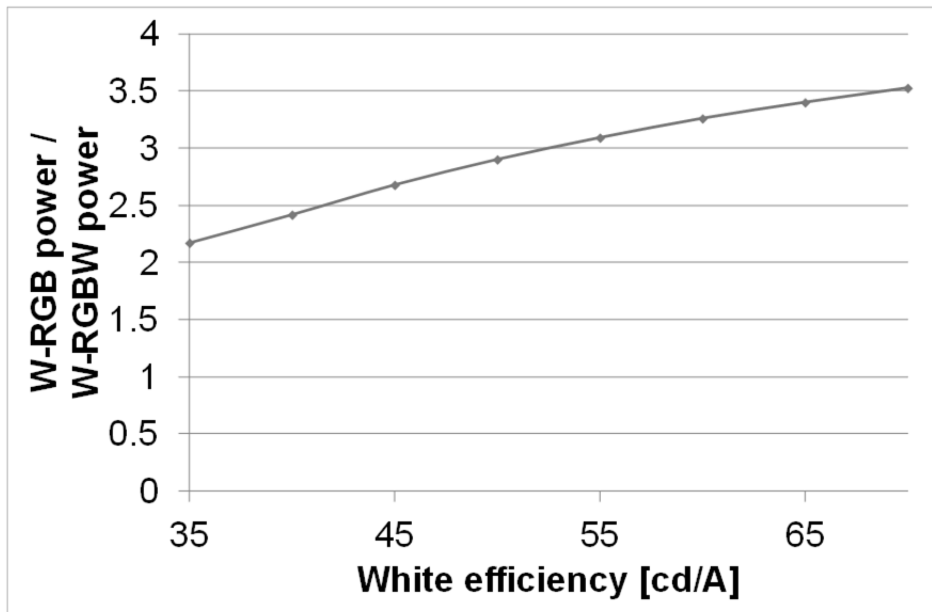


Fig. 115 Power consumption difference between W-RGB display and W-RGBW display

According to this analysis, two conclusions are made.

Conclusion-1)

Current density, namely power is not very much affected by RGB sub-pixel efficiency.

Conclusion-2)

By increasing the white sub-pixel efficiency, the display power would be further improved.

With this approach, low power would be achieved with high color-gamut capability on W-RGBW displays, against common belief. Then the concept was checked through actual display fabrication.

4.4 Formulation for the prototype to prove that low power consumption can be achieved with large color gamut.

For conventional color-by-white method, R+G+B emission has been normally selected so that the peak matches with the position of color filter transmittance. (Fig. 116) This is because emission wavelength between R and G, or between G and B degrades the color gamut capability, as discussed. Also because mismatch between OLED emission spectrum and color filter transmission spectrum decreases the output efficiency.

To prove the concept to achieve low power consumption with high color gamut, a

set of OLED and color filter formulation was developed and applied to a W-RGBW AMOLED display. [69]

R+G+B+Yellow OLED formulation used for the prototype is shown in Fig. 117. The additional yellow spectrum component very well matches with relative luminosity curve, so the formulation makes much higher efficiency possible than conventional RGB-peak white. (As such formulation provides both very good efficiency and good color rendering index, so it was also employed in OLED lighting application after this.)

The largest hurdle was color filter. Existing color filter for LCD could not show large color gamut for R+G+B+Yellow formulation, because the transmission of green color filter and red color filter still remains in yellow wavelength region just like Fig. 113 case. Also blue color filter spectrum was not sharp enough to achieve CIE-y=0.06, which is necessary for Adobe-RGB/s-RGB color space reproduction. New color pigment and special milling / dispersion technology was applied so that the OLED panel demonstrated in IDW2008 [69] achieved NTSC100% with lower power consumption (Less than 2W for 8-inch, which corresponds to 64W for 32-inch television.) than LCD display products on the market.

Color-by-white, the most safest way to produce large AMOLED TV from production yield perspective, but was deemed as unusable due to high power consumption and poor color gamut, could finally achieve both low power consumption and high color gamut.

The technology has been applied to state-of-art 55" AMOLED display in the market and is dominant technology currently for the large AMOLED TVs.

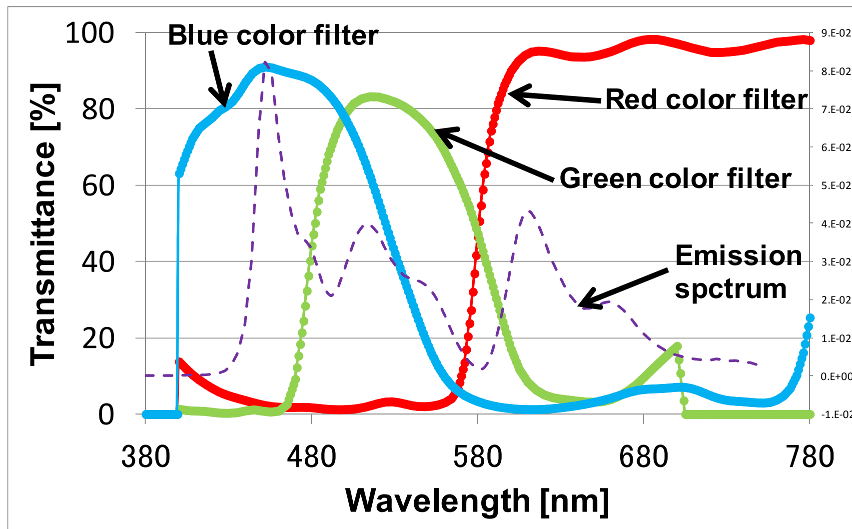


Fig. 116 Conventional Color-by-white approach

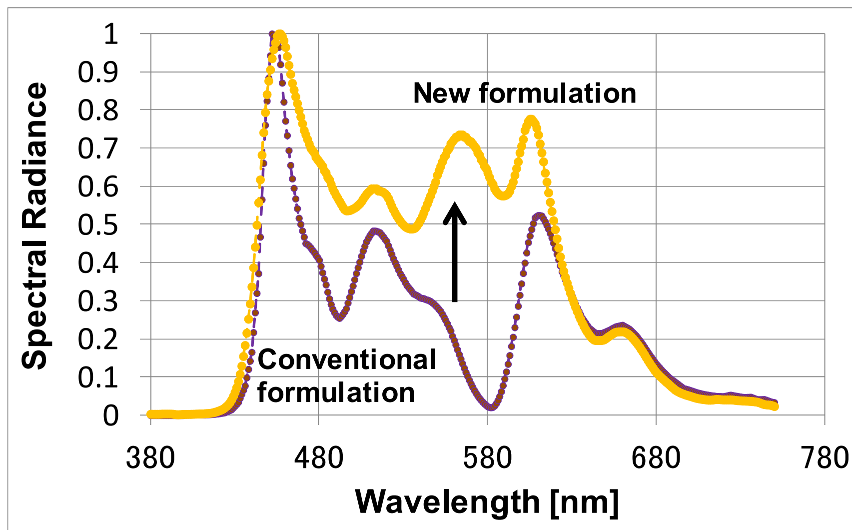


Fig. 117 Wide spectrum white formulation for high white sub-pixel efficiency

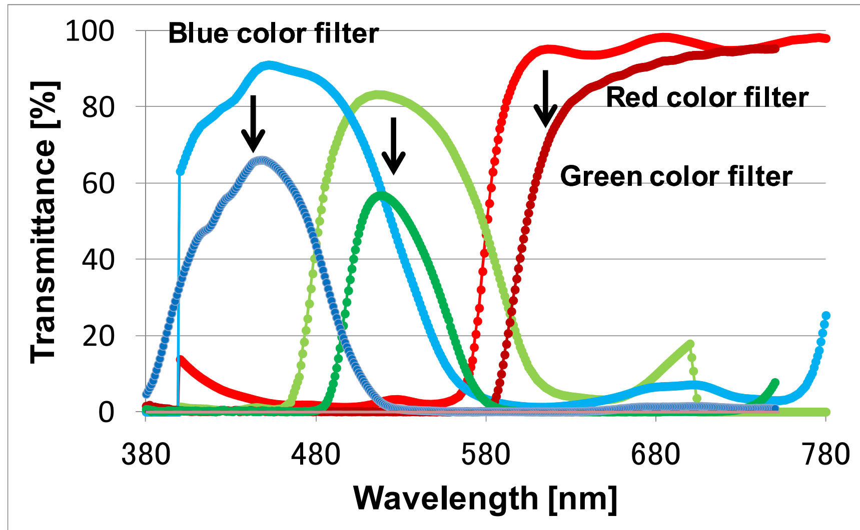


Fig. 118 High color gamut color filter design for wide spectrum white emission

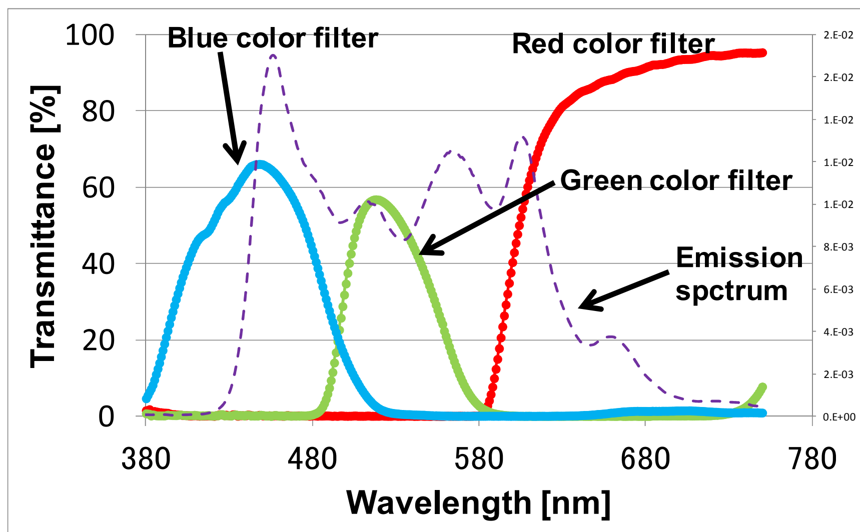


Fig. 119 New formulation with new color filter.

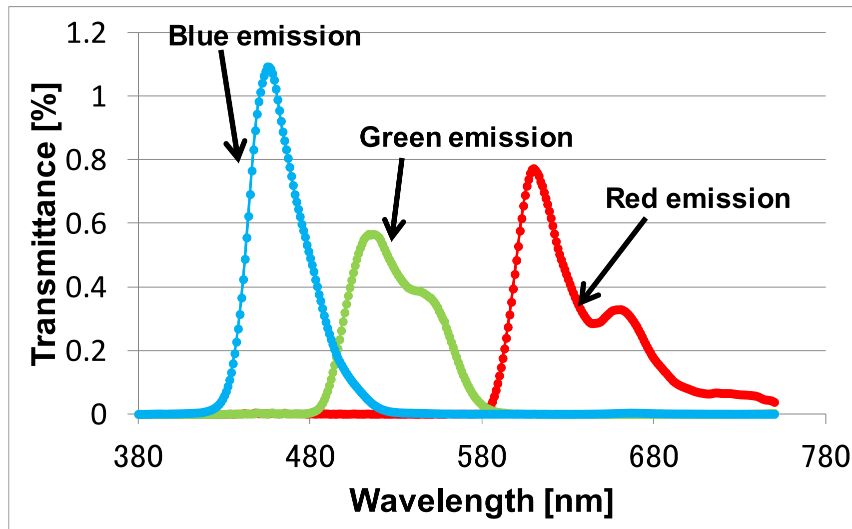


Fig. 120 Emission output of W-RGBW display using new formulation, color filter set

5 Choice of TFT and prototype fabrication

5.1 TFT and compensation circuitry

As discussed in 3.4, scalability is very important to secure the manufacturing yield of large display. For the prototype, metal-induced-lateral-crystallization technology (MILC) [70] was used for this study. Fig. 121 shows an example [70] of MILC process.

After 100nm amorphous silicon deposition by LPCVD at 460° C using Si_2H_6, plasma oxidation (30nm), SiO_2 deposition by ECR-CVD (70nm), P-doped poly-Si films (250nm) by ECR-CVD for gate electrode and subsequent patterning of gate electrode are followed. 0.5nm Ni layer is deposited by the sputtering method, P doping for 3 minutes are performed and MILC for both crystallization and dopant activation is carried out in N_2 ambient. Unreacted nickel on SiO_2 is removed by chemical etching so that self-aligned MILC TFT is fabricated.200nm aluminum film and annealing for making alloy are done at 300° C for 30 minutes in H_2+N_2 ambient. It has been already reported [71] that MILC TFT has much better stability than amorphous silicon TFT and equips with better mobility like 18.5 cm^2/Vsec [71], so the design restriction of AMOLED display should be relaxed than amorphous silicon case.

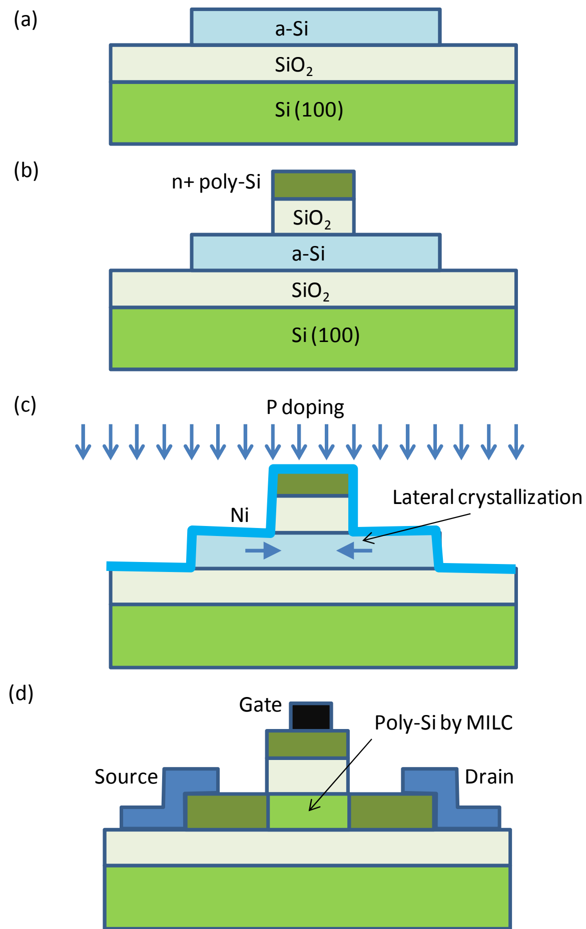


Fig. 121 Metal-Induced-Lateral-Crystallization process

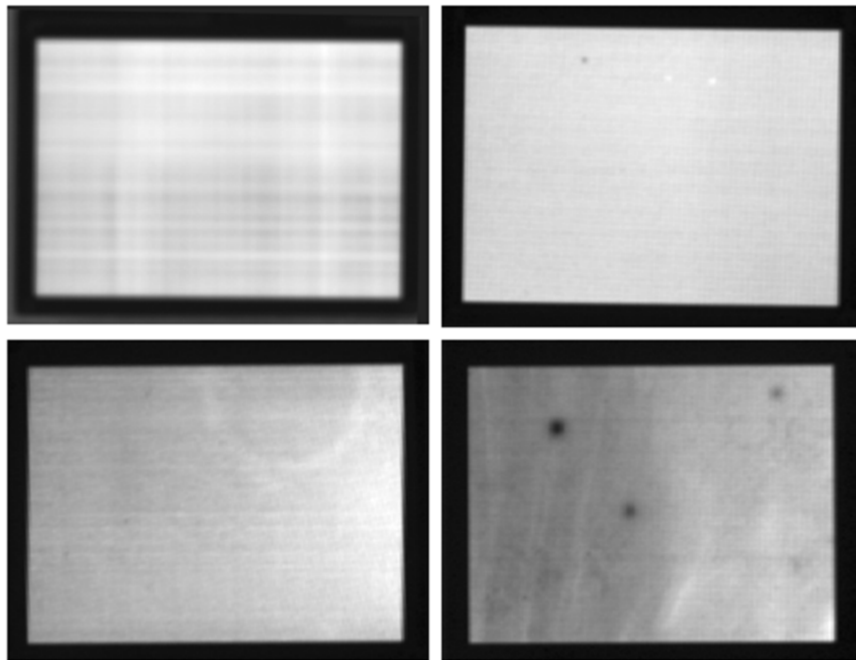


Fig. 122 Various Non-uniformity due to TFT/OLED process

Various types of non-uniformity, called "mura", are shown in Fig. 122. It is quite important to remove or reduce mura to have high quality display.

Fig. 123 shows various cause of AMOLED brightness non-uniformity. Mura caused by cleaning, etching, deposition, doping and voltage drop can be managed by process tuning, design and low resistive metal bus line, however TFT conductance change by crystallization, such as excimer laser annealing and solid phase deposition cannot be managed by such methods.

Device	Process	Countermeasure
TFT-related	Excimer-laser	TFT conductance change
	Solid phase crystallization	TFT conductance change
	Cleaner/ Etcher	Removable by process tuning
	Deposition	Removable by process tuning
	Doping	Removable by process tuning
OLED-related	Deposition	Removable by process tuning
	Voltage drop	Can be reduced by design and low resistive metal bus line

Fig. 123 Cause of AMOLED non-uniformity

For the scalability, external compensation (Global Mura Compensation method. GMC) [72] was applied to this study. Transfer characteristics of every pixels in manufactured displays are measured by an inspection tool (Fig. 124) and the data

(gain and offset) for the compensation are stored in flash memory built in a display IC. When the display is in operation, as shown in Fig. 125, the gain and offset information are read from flash memory and the calibrated signal values are calculated in the chip so that the driver IC can show mura-free image on a AMOLED display. Fig. 126 and Fig. 127 show the display brightness uniformity with and without external compensation method respectively for an LTPS AMOLED display. Fig. 128 and Fig. 129 show the compensation accuracy of a display before and after compensation method. Clearly, the driving current of a display pixel are very well compensated to give excellent uniformity. The same technology was applied to the prototype in this study.

Fig. 124 Equipment used for the external mura compensation

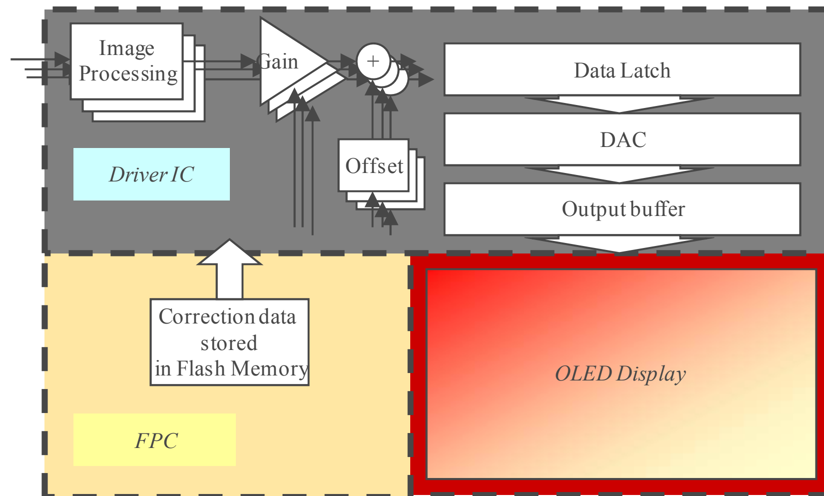


Fig. 125 External mura compensation method

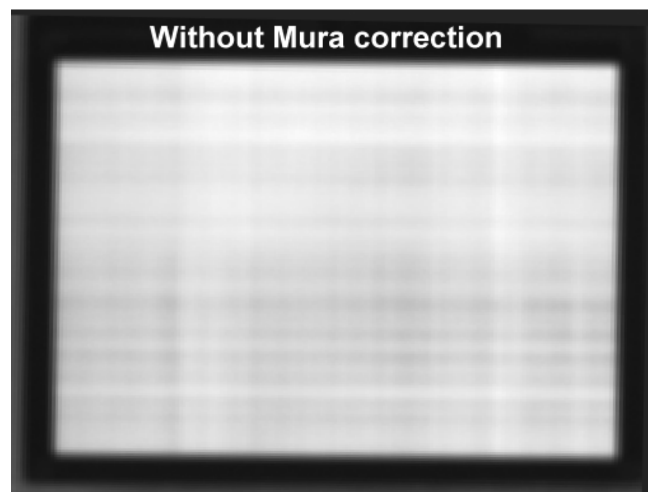


Fig. 126 Display uniformity of LTPS AMOLED display without Mura compensation

Fig. 127 Display uniformity of LTPS AMOLED display with external compensation

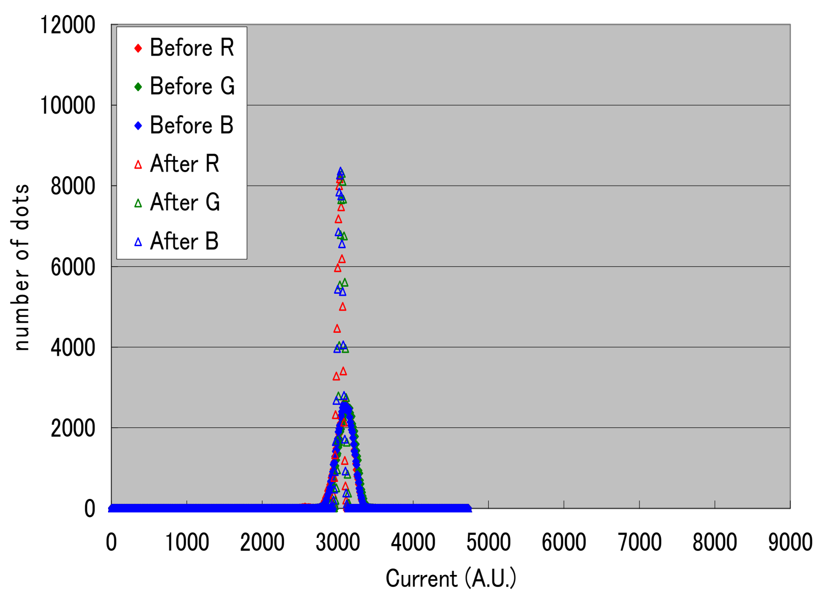


Fig. 128 Compensation accuracy at low current region

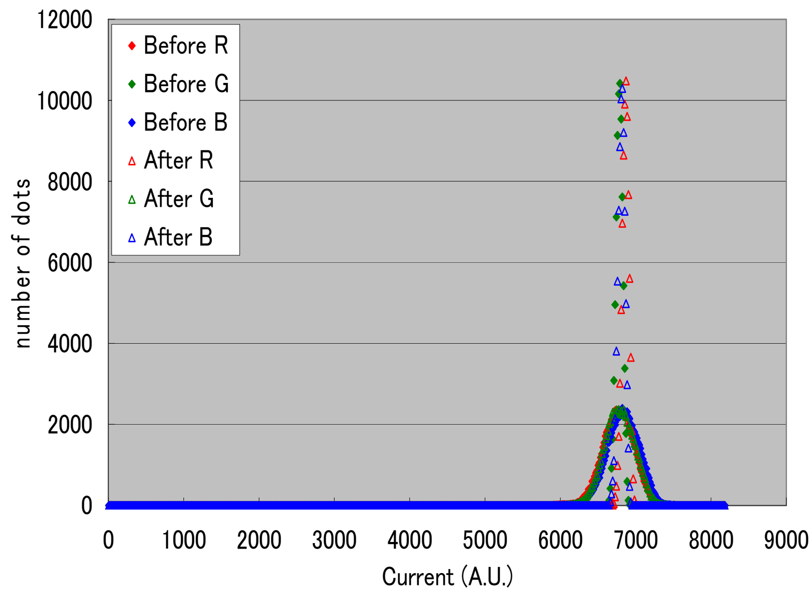


Fig. 129 Compensation accuracy at high current region

5.2 Fabrication of MILC TFT + color-by-white high color gamut OLED display for large OLED television manufacturing

By combining (1) white tandem OLED structure using BGRY spectrum, (2) Square –type RGBW pixel layout, (3) RGBW driving algorithm, which reduces power to half compared with normal RGB three pixel case, (4) High transmittance color filter with micro milling technology, (5) Scalable external compensation method (GMC method) and (6) Scalable TFT backplane (MILC method), he proved that the 100% NTSC AMOLED display can be designed with equivalent or lower display power than a commercial LCDs by showing 8-inch AMOLED display prototype. (Fig. 131)

		Color-by-white **(SID2007) [67]**	Color-by-white **(Tsujimura, IDW2008) [69]**	LCD (C080VW02, 2008)[73]
Color reproducibility		78% NTSC	100% NTSC	<72% NTSC
Power consumption	**8-inch**	-	1.90W	3.30W
	14.1-inch	16.0W	-	-
	32-inch (calculation)	82.4W	29.6W	51.5W

Fig. 130 Comparison of power consumption and color reproducibility for W-RGBW OLED and LCD

Fig. 131 8.1" 100% NTSC low-power AMOLED display prototype

6. Current technical issues and potential new technologies

6.1 Trend toward high resolution format

In small size display for mobile phone, very high resolution has become very popular. According to the subjective evaluation of image quality of actual 2.3-inch display prototype, it was reported that higher resolution gives better evaluation score, at least up to 700 ppi. [74] Also for the large television display, very high resolution displays such as 3840 ×2160 pixels (so called "4K display") are already in the market and 7680 ×4320 pixels (so called "8K display") are fabricated as prototype. [75] Higher resolution has become the major trend in display industry.

Color-by-white method discussed in chapter 3 has advantage over RGB-pixelation method in terms of resolution, because the accuracy of color filter alignment is better than the accuracy of a pixel formed by shadow mask method. [76] However, as the pixel density is very much increased like 4K-level, other factors also affects the display design. If diagonal size is 55-inch, a 4K display has 105[μm]×317 [μm] sub-pixel area. In case of 8K, 52[μm]×158 [μm]. An OLED sub-pixel region normally has several (4~8) transistors and (1~2) capacitors to compensate for the

luminous uniformity variation. Then the compensation circuitry occupies large portion of the sub-pixel area, which reduces the aperture ratio significantly if conventional bottom emission OLED structure is used. (Fig. 132) Low aperture ratio causes large impact on the display luminance lifetime and also causes image sticking issue.

To circumvent this issue, it is necessary to change the OLED structure from bottom emission to top emission. (Fig. 133) However, transparent electrode such as ITO has large resistivity, which causes significant voltage drop and is not suitable for large display driving. As an alternative, it would improve the voltage drop situation if via hole is made like Fig.134 so that the high resistance cathode is connected with low resistance metal lines. However creating a via hole means that shadow mask patterning is used. It would be nonsense to use shadow mask when mask-less feature is going to be enjoyed from production-yield point of view.

Possible solution for low resistive cathode would be to connect cathode electrode to somewhere low resistance. There are two examples illustrated in Fig. 135 and in Fig. 136. The former creates auxiliary wiring pattern by non-shadow-mask method like ink jet printing of metal layers [77] and latter connects the cathode electrode to counter substrate. [78] Such technologies will open the door for the ultra-high resolution AMOLED and would bring more attractive viewing experience to the customers.

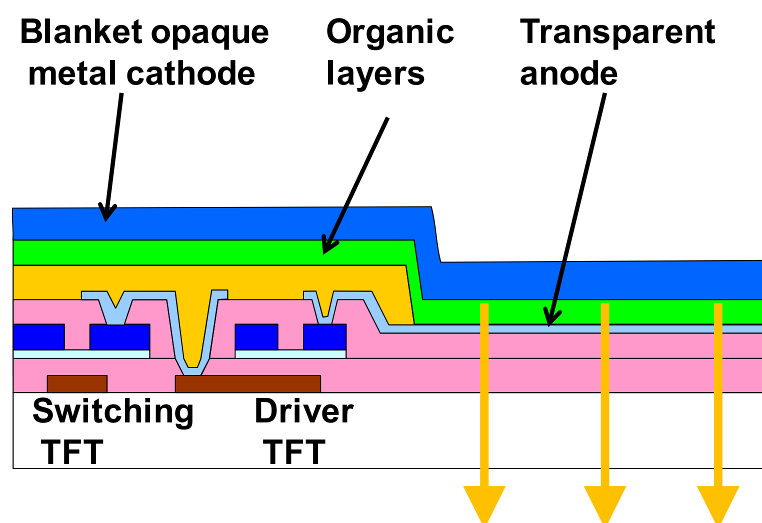


Fig. 132 Color-by-white OLED by bottom emission device

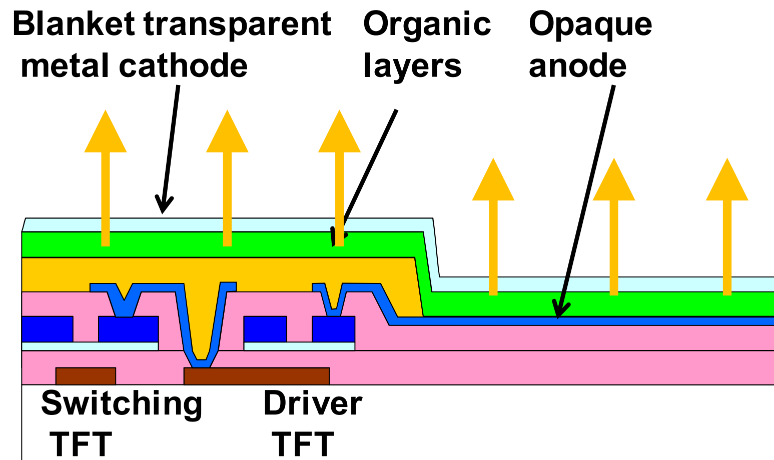


Fig. 133 Color-by-white OLED by conventional top emission device

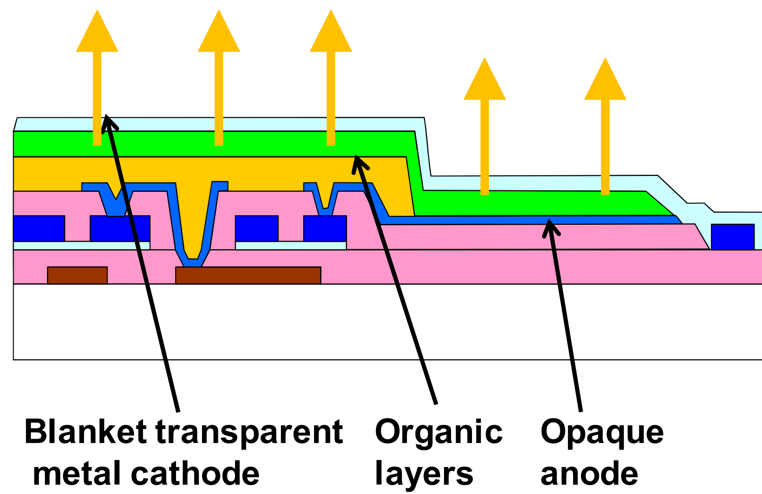


Fig. 134 Color-by-white OLED by via-hole connected cathode

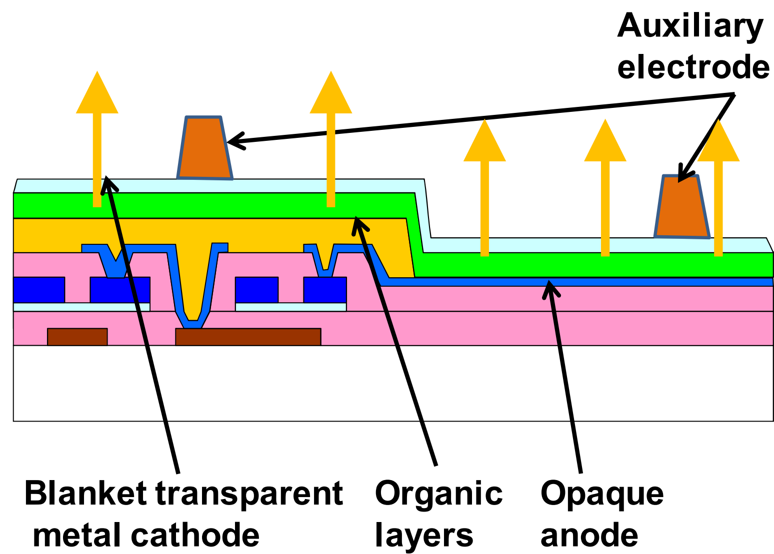


Fig. 135 Color-by-white OLED with auxiliary cathode electrode

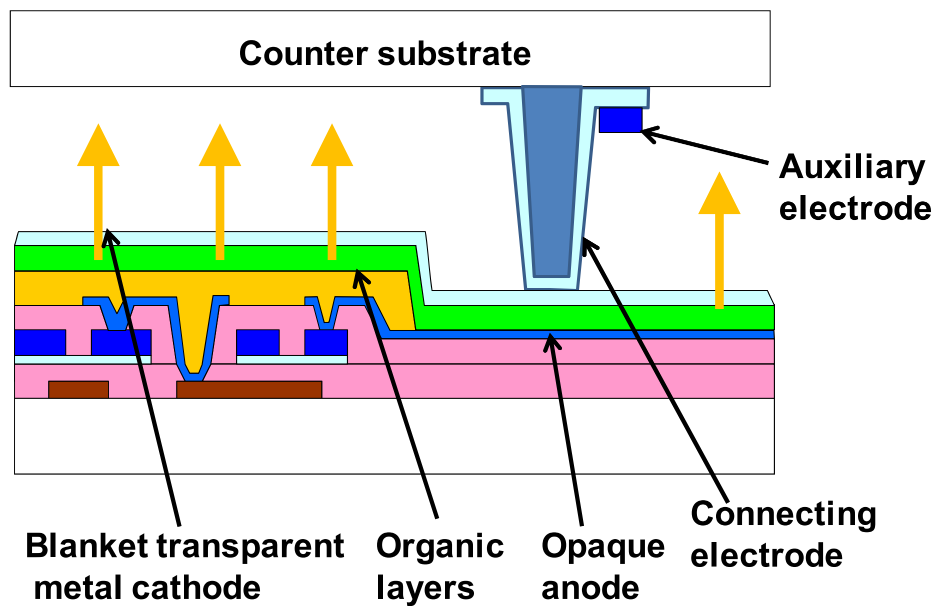


Fig. 136 Color-by-white OLED with counter-substrate-connected cathode

6.2 Trend toward cost reduction

For the cost reduction of a display, mother glass size expansion has been always used. For AMOLED manufacturing, generation-5 has been the limitation even after SLS-LTPS method [79] was applied to the TFT backplane. However, by using

color-by-white method and oxide TFT backplane [80] combination, substrate size restriction was very much relaxed and generation-8 production line has been fabricated to produce large low-cost high-performance AMOLED television displays. [30]

As the AMOLED television is penetrated into mass market, further substrate size expansion might happen. At the same time, there are different approaches to make cheaper AMOLED to happen.

One approach is to make OLED by roll-to-roll manner. Generation-5 equivalent roll-to-roll manufacturing line was introduced to produce low cost white OLED lighting panel. [81] [82] Also roll-to-roll TFT fabrication process is under development. [83] Combining both technology, cheaper AMOLED might happen in the future.

7. General conclusion

7.1 Summary of the thesis

By means of two prototype fabrication, there were several insights provided for large AMOLED display.

1. Proof of AMOLED driving by non-ELA-LTPS TFT

- Driving capability

It was widely believed that the poly-Si was the sole possible choice to drive AMOLED and amorphous Si TFT cannot drive it. [84][85] It was proven in the study that low mobility amorphous Si TFT has enough driving capability for large AMOLED TV. The first prototype triggered the non-ELA-LTPS TFT development, including amorphous Si, microcrystalline Si, metal-induced poly-Si, AMFC (alternate magnetic field crystallization), oxide TFTs.

- Instability

Large V_{TH} shift has been a major issue for amorphous silicon TFT to drive OLED. To cope with the TFT instabilities, combination of technologies, such as pixel-level compensation, current concentration reduction of TFT, high-durability driving method, dual-channel-TFT, AC driving, deposition recipe control, can significantly improve the situation.

- Structure

Pixel structure was studied for NMOS TFT devices for both common-anode and common-cathode configuration. The structure is

currently widely used in AMOLED TVs by oxide TFTs, having the same NMOS feature.

- Impact

As a result, Kyocera and Ortus Technology (JV by Casio and Toppan) successfully shipped a-Si-driven AMOLED product in the market. [86][87]

After my study, new TFT technologies with larger design flexibility have been appeared such as oxide TFTs, so amorphous-silicon-TFT-driven AMOLED has been disappeared. However approaches used for the study have been used in current AMOLED products, such as NMOS + common-cathode + tandem OLED structure (Fig. 50. Industry standard structure for state-of-art AMOLED TV. US7227304B2) and dual-channel TFT. [30]

Tsujimura received SID Special Recognition Award for this study [88] and the prototype was listed on the Display industry chronological timetable issued in 2003 by SID. [89]

2. Establishment of high manufacturability technology for large AMOLED TVs

- Production yield simulation model

As the display size becomes larger, the production yield is significantly reduced. To make large display manufacturing happen, technology with very low defect density must be chosen to fight with the conventional technology. Combination of "scalable" technologies should be chosen for large display manufacturing. ("Scalable" color-by-white OLED + "scalable" oxide TFT were chosen for the state-of-art OLED TV manufacturing, as suggested.)

- Concomitant of both large color gamut and low power consumption for high manufacturability color-by-white AMOLED.

Though it was believed industry-wide that color-by-white method could not achieve both color gamut and power consumption [65][66] (Discussed in 4.2.), the methodology and prototype presented in IDW2008 has proven that both can be simultaneously achieved. (High color gamut over 100% NTSC and lower power consumption than LCDs.) By adding spectrum component with large visual sensitivity significantly reduces the power consumption, much better than predicted in the past. (Fig. 114)

The technology was transferred to a manufacturer and applied to the generation-8 manufacturing of large AMOLED TV including 55-inch

[30].

Tsujimura received SID Fellow Award for this study. [90]

7.2 Conclusion based on the two concept trials

As a result of my study toward large size, OLED television more than 50-inch has been successfully launched and the color-by-white approach has been recognized as the mainstream technology for large OLED. The choice of color filter for color patterning was the right choice because color filter is mature technology, which promises the high yield manufacturing.

Fig. 137 shows the prediction of production yield loss, presented in FPD International 2009. [91] As color-by-white is a combination of mature process technologies, the production yield can be increased rapidly as shown in the "Top-runner technology" in Fig. 137. On the other hand, if "Newer technology" starts manufacturing, it has to start from the 1st year. Naturally, the yield of newer technology is much lower than the "Top-runner technology", which causes very high production cost. Therefore, newer technology needs to have tangible differentiation enough to beat "Top-runner", other than the manufacturing cost. As predicted, though several new methods have been proposed aiming to beat color-by-white, still there is no technology yet to replace it for large AMOLED TV.

RGBW approach decreases the aperture ratio of sub-pixel area due to additional white. In OLED case, as the display luminance is proportional to the current and is not very much affected by reduced aperture ratio, then OLED can fully enjoy the power reduction merit of RGBW. In LCD case, the aperture ratio loss reduces the merit of RGBW's power reduction, so RGBW method is more suitable for the OLED display. Though the merit of RGBW is limited in case of LCDs, the approach was adopted for actual LCDs recently. [92]

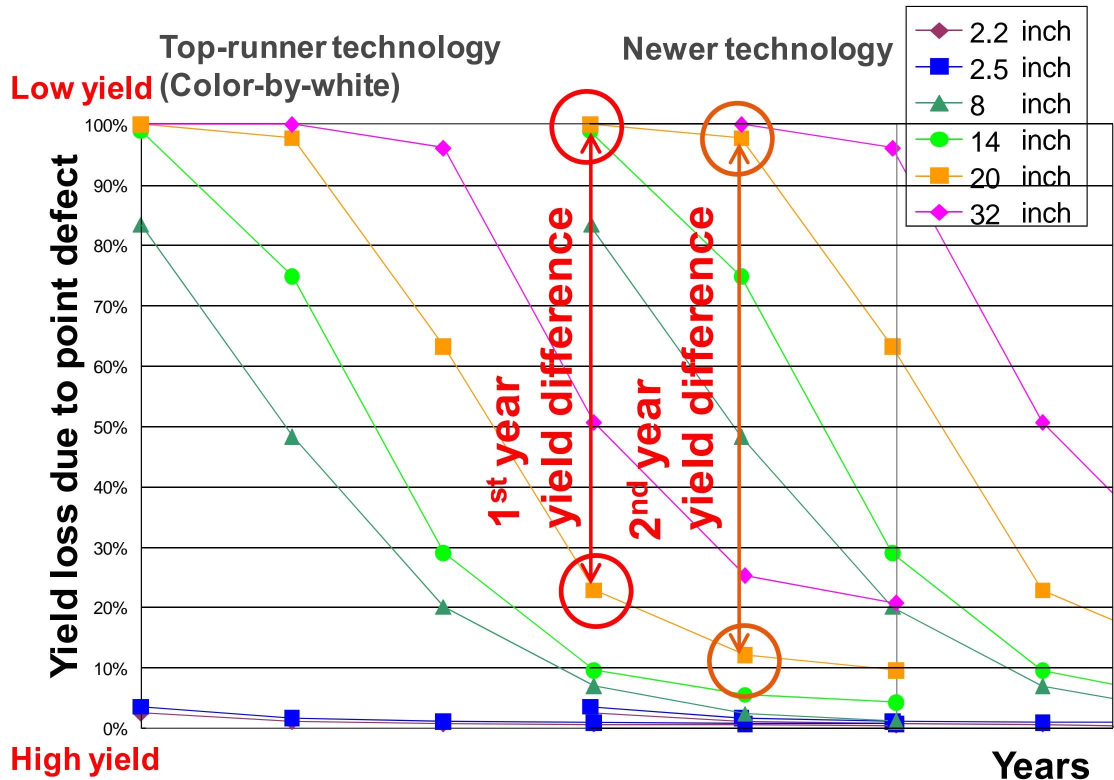


Fig. 137 Yield loss prediction presented in FPD International 2009.

In my first trial, shadow-masking color patterning method was used and in the second trial, color-by-white approach was used. Though first approach could achieve low power consumption due to highly efficient phosphorescent device, second approach could also achieve low power due to the use of color image science. Both case achieved 100% NTSC ratio, so color-by-white would be the better than the shadow-masking from the manufacturability point of view. In actual, several companies failed to make large OLED display manufacturing using shadow mask recently.

New technology targeting large display, such as inkjet and nozzle coating, have been proposed in the industry. As manufacturing using new technology would have to start from very low yield, so it is always very important to consider if the technology can make differentiation against conventional technology at low yield manufacturing condition.

Regarding the choice of TFT technology, amorphous silicon TFT was applied to the first prototype and MILC TFT was applied to the second. Amorphous silicon would be able to make around ten thousand hours lifetime at room condition, if multiple approaches are implemented. However, V_{TH} shift becomes larger when the

operational temperature is increased and the degraded TFT performance decreases the operational margin. When other technologies, such as oxide TFTs, MILC TFTs and solid-laser-crystallized microcrystalline TFTs exist, there is no need to stick to the use of amorphous silicon. Also due to the low mobility of amorphous silicon TFTs, TFT size in a pixel becomes very large that naturally increases the probability of inter-layer or intra-layer defects. Higher mobility technology should give better production yield.

As to the MILC technology used for the second prototype, residual Nickel can be a serious issue. Remained nickel tends to cause TFT leakage issue after driving stress. Nickel-free technologies, such as oxide TFTs or AMFC (alternalte-magnetic-field crystallization) would give better stability during operation.

Overall, the combination of color-by-white OLED and oxide TFT, which has been adopted for the industry can be regarded as the best for large OLED television so far.

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