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Low-power operating oxide thin-film transistors and circuits for wireless device application

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Abstract

This study was targeted at the development of a flexible passive-type RFID tag with monolithic antenna that can be operated by 13.56-MHz RFID reader. The RFID is expected as a platform to be equipped with sensors and connecting them to a network. The RFID-sensor fusion device will be attached to a variety of places thanks to its flexibleness. Such an RFID requires a technology to fabricate a power source, an antenna and electrical circuits on a flexible substrate.

In order to achieve the target, a-InGaZnO thin-film transistor was selected as an active device that constructs the RFID in terms of its advantages in low-temperature fabrication, characteristics and fabrication cost. The three element technologies were successfully developed in this study; (1) low-voltage operating a-InGaZnO thin-film transistor that can be used for wirelessly operating circuits, (2) rectifier that can convert 13.56-MHz radio wave into a DC power, and (3) logic gate that enables internal data-processing circuits to operate within the power supplied through the rectifier and with the frequency accepted by the reader terminal. With these threes studies, the feasibility of the flexible passive-type RFID tag was demonstrated. The main remaining issues, which will surely be solved, are further lowering of the fabrication temperature and the addition of the sensing function onto the flexible RFID platform.

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Contents

Chapter 1

Introduction

1.1 “Internet of Things” and RFID

In a coming era of the “Internet of Things (IoT)” variety of things are connected to the internet. According to Harvard Business Review November 2014 [1], the number of devices connecting to the internet is rapidly growing and it is estimated to be twice the number of present, 20 billion, in 2018. Furthermore, according to “T Sensors roadmap,” trillions of sensors per year will be connected to a network in 2021 “driven by emergence of sensor based smart systems fusing computing, communication and sensing” (Fig. 1.1) [2].

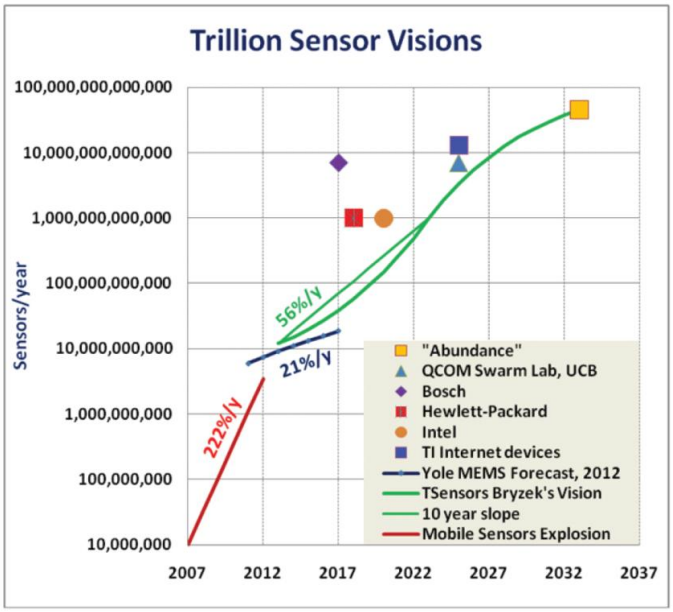


Fig. 1.1 Number of connected sensors (from *T Sensors Summit for Trillion Sensor Roadmap* (2013) [2]).

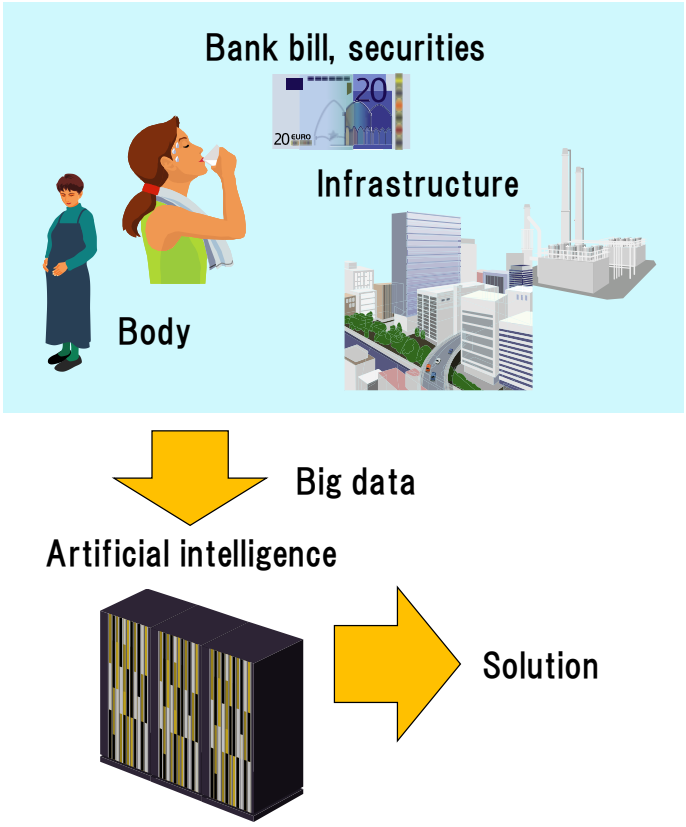


Fig. 1.2 Connected sensors and big data analysis for solving problems.

In such an era, the “big data” collected by the “connected sensors” are analyzed by an artificial intelligence to solve the problems in medical, healthcare, environmental and social sectors (Fig 1.2). The sensors are connected in wireless way and distributed to everywhere. Some of the sensors are light, thin and flexible and are attached on to a curved surface or a bending part of things and living bodies. A fusion of sensors with wireless power transmission, wireless communication and flexible technology are essential to actualize this vision.

Radio frequency identification (RFID) is one of the devices that can be used for the physical layer of the IoT. RFID is a small device that can communicate wirelessly with a terminal called reader. It contains ID information in an on-chip memory and responds

ID information when the reader accesses to it. There are two types of RFIDs; active type and passive type. The active type RFID includes a battery on it and thus it operates autonomously and also relatively long-distance wireless communication is possible. On the other hand, the passive type RFID does not have a battery. It generates power to operate itself from the electromagnetic wave transmitted by a reader terminal. The generated power is very small even when the RFID is put close to the reader. Therefore, the passive RFID are not able to be used for a long-distance communication. An RFID consists of an antenna and an IC chip (and also a battery if it is an active type) and the IC chip consists of a memory and a circuit to drive it. In addition, the passive RFID also has a circuit to generate the power for its operation from electromagnetic wave.

The RFID has been used for the management of things such as books in a library [3]. It has also been used for the traceability of foods and industrial products [4], for example the traceability of beef. Some company in the distribution industry stared to use RFID to improve the efficiency of the supply chain management [5]. Recently, RFID-sensor fusion system is attracting an attention for applications such as monitoring and controlling of environment and living bodies. Some groups started R&D to use RFID technology in "personal healthcare in smart environments" [6]. The RFID for such applications needs to be produced with low cost since a lot of sensors are required to collect so-called "big data" for the data analysis and some of the sensors for monitoring a living body are even disposables. The RFID further needs to be light, thin and flexible in order that it can be attached on to a curved surface or a bending part of things.

SENSIMED, a Swiss company spun-off of Swiss Federal Institute of Technology, has been developing a sensor-equipped contact lens called "Triggerfish®" [7-9]. It is

equipped with a strain sensor and it records ocular dimensional changes or intraocular pressure over 24 hours. In 2009, they obtained approval of Class IIa device CE-mark from European regulatory authorities and Triggerfish has been introduced into clinical management of a glaucoma patient [9]. In 2014, Google also announced that they have been working on R&D of a sensor-equipped contact lens [10, 11]. The sensor in their contact lens monitors glucose level in tear fluid hence people with diabetes can continuously check the glucose level in their body. These two contact-lens type devices are based on RFID technologies. The antenna, circuits and sensor are separately produced and then integrated onto a silicone based substrate. It is presumed that resistance to bending and production cost are still issues. This is because they are the issues in current RFID tag, in which antenna and IC are attached together by glue. There are also some other RFID based flexible sensors such as humidity sensor [12] and gas sensor [13] and so on. However, these sensors also have the same issues since antenna, circuits and sensors are not monolithically fabricated.

1.2 Flexible wireless communicating device focused in this study

Against this background, our group has been focused on a research of flexible wireless communicating sensor device based on RFID; a sheet device such as a plastic film equipped with sensing and communicating function. We especially focused on fabricating RFID and antenna monolithically and directly onto a substrate in order to solve the issues mentioned above. Such a wireless communicating device requires a technology to fabricate a power source, an antenna, electrical circuits and a sensor on a

flexible substrate.

Regarding the power source, there are two types of wireless communicating devices as already mentioned; active type and passive type. The active type device has a battery and it can transmit data using power from the battery. Therefore, the consumption power of the device can be as large as the battery permits. However, the device gets larger, thicker and heavier due to the on board battery and also the battery needs to be replaced periodically. On the other hand, the passive type device does not have battery. The power required to drive the device is wirelessly transmitted from a reader terminal. Therefore, the replacement of a battery is unnecessary. However, the consumption power of the device is limited to a small power that can be received wirelessly.

Regarding the antenna, it needs to be flexible and resistant to bending. The antenna itself of the some of the current RFID is already flexible. However, the durability is not enough since the antenna and IC chip are fabricated separately and are attached together by using glue. Furthermore, the attachment process increases the production cost of RFID tags.

Regarding the circuits, the consumption power needs to be smaller than the power supplied by an on board battery or a wireless power transmission from a reader terminal. At the same time, the circuits need to operate at the frequency that the reader terminal can accept.

In view of the above circumstances, this study was targeted at the development of the flexible passive-type RFID tag with monolithic antenna that can be operated by 13.56-MHz RFID reader. Though the RFID does not include sensors on it, it is equipped with the basic elements for the wireless communication and hence it is an adequate target for the first step. The passive-type operation was chosen since the

on-board battery is not suitable with the flexibleness and also the replacement of the battery is almost impossible when thousands of RFID tags are distributed. The antenna should be fabricated monolithically with the RFID circuit to increase the durability and also to reduce the production cost. The device should be operated by the 13.56-MHz RFID reader since this frequency band is most widely used for the wireless communication devices such as RFIDs and thus the reader is already in widespread use.

In order to achieve the target, we focused on the development of three element technologies in this study.

1. Low-voltage operating transistor that can be fabricated on a flexible substrate.
2. Rectifier that can convert 13.56-MHz radio wave into a DC power.
3. Logic gate that enables the internal data-processing circuits to operate within the power supplied through the rectifier and with the frequency accepted by the reader terminal.

The monolithic antenna was developed by other members of the research group and some results are reported in [14] (most of the results are not published yet). The circuit architecture is also developed by other members of the research group [15, 16].

1.3 Thin-film transistors

In the achievement of the flexible passive-type RFID tag, fabrication of transistors onto a flexible substrate with low-temperature (less than 150-200^{o}C) and low-cost process is the key. Furthermore, the transistors need to have high mobility (larger than ~10 cm^{2}/Vs) and need to be driven by low voltage (less than ~5 V) to achieve the low

power sufficient for wireless operation.

Thin-film transistor (TFT) is a suitable device for such an application. The transistors used for large scale integrated circuits (LSIs) are fabricated by using a semiconductor substrate (crystalline silicon in most cases) and the channel layer is fabricated "in" the substrate. On the other hand, TFT is a transistor fabricated "on" a substrate by using a deposited semiconductor material as a channel layer. It can be fabricated on a large-area substrate like a glass sheet and hence it is used for a driving device of active-matrix flat-panel displays. Amorphous silicon (a-Si) and poly-crystalline silicon (pc-Si) are the most widely used materials as the channel layer of a TFT. However, process temperatures above 300^{o}C for a-Si TFT [17-20] and above 450^{o}C for pc-Si TFT [21-23] are required in order to fabricate a TFT with good performance and reliability. Moreover, the mobility of the a-Si TFT, ~1 cm^2/Vs, is not high enough and the subthreshold slope (*SS*), larger than 200 mV/decade, is too large for the low-voltage operation. Therefore, these two types of TFTs are not suitable for fabricating on a flexible substrate such as a plastic film. An organic TFT using organic semiconductor, pentacene for example, as a channel layer is attracting an attention since it can be fabricated at room temperature [24-26]. However, at present, there are still some issues regarding the performance and stability.

In contrast to the TFTs mentioned above, a TFT using metal-oxygen compound semiconductor, especially amorphous metal-oxygen compound semiconductor, is much more suitable for the flexible passive-type RFID tag. It shows high performance with good stability even when the channel layer material is deposited by sputtering at room temperature [27-33]. Among the metal-oxygen compound semiconductors, amorphous indium-gallium-zinc complex oxide (a-InGaZnO) is the promising material in terms of

performance, reliability, fabrication process and fabrication cost. Therefore, a-InGaZnO was adopted as a channel layer of a TFT in this study. Table 1.1 summarizes properties of TFTs.

Table 1.1 Properties of TFTs.

Channel material	**a-Si**	**pc-Si**	**Organic**	**Oxide**
Process temperature (°C)	**~300**	**~450**	**~RT**	**~RT?**
Mobility (cm^2/Vs)	**~1**	**~100**	**~1**	**~10**
***SS* (mV/dec)**	**> 300**	**> 200**	**> 300**	**< 200**

1.4 a-InGaZnO and thin-film-transistor application

1.4.1 a-InGaZnO

a-InGaZnO TFT was proposed in 2004 [27] and since then it is widely studied at research institutes all over the world. One of the most distinctive characteristic of InGaZnO is the way conduction band is formed (Fig. 1.3). As is well known, the conduction band of covalent semiconductors such as silicon is formed by sp^3-orbitals. The sp^3-orbitals form a perfect tetrahedral network when the semiconductor is in the crystalline phase and hence the electron mobility is high. On the other hand, the network is imperfect when the semiconductor is in the amorphous phase and the overlaps between sp^3-orbitals are not sufficient. Therefore, the electron mobility is small. In contrast, as reported in [27], the conduction band of the InGaZnO is formed by *s*-orbitals of post-transition-metals, which are large spheres. Therefore, the overlap

between the *s*-orbitals is large enough even when the material is in the amorphous phase. Thus the electron mobility in a-InGaZnO is almost as large as that in the crystalline phase.

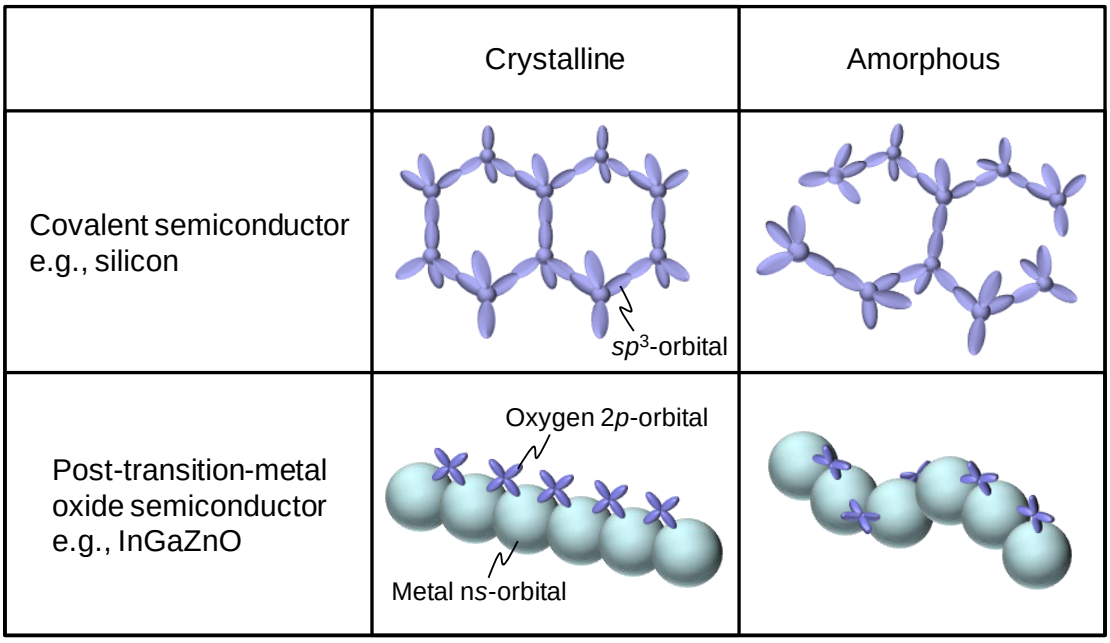


Fig. 1.3 Schematic orbital drawings of conduction band bottoms of covalent and post-transition-metal oxide semiconductor; crystalline phase on left and amorphous phase on right (reproduced from K. Nomura, *et al.*, *Nature* (2004) [27]).

1.4.2 Effect of material composition

It is reported in [34] that the phase of pure ZnO and In_2O_3 are crystalline even when they are deposited at room temperature and thus it is difficult to obtain amorphous phases for these materials. On the other hand, it is also reported in [34] that the phase of binary oxide compounds, such as Zn-In-O and Zn-Ga-O, deposited at room temperature are amorphous since mixing of cations having different ionic charges and sizes suppresses crystallization.

Indium and zinc ions increases electron mobility since unoccupied *s*-orbitals of these cations form electron transport paths in a-InGaZnO [34, 35]. On the other hand, the conductivity of an a-InGaZnO film reduces when the gallium ion content rate is high [34, 35]. This is because gallium ion suppresses the formation of oxygen vacancy and thus the generation of free electrons due to the strong binding power of Ga-O bond (the relation between oxygen vacancy and free electron will be explained later). It is also because gallium ion reduces electron mobility in a-InGaZnO. Gallium ion also plays a role in stabilizing the conductivity of an a-InGaZnO film; the conductivity of a gallium free film rapidly changes.

1.4.3 Effect of oxygen vacancy

One of the most important factors that determine the properties of the oxide semiconductors including a-InGaZnO is the oxygen vacancy. Oxygen in an oxide material tends to be less than the amount in the stoichiometry and the oxygen defect leaves two electrons at the vacancy (Fig. 1.4). When a non-bonding state of a metal cation is located close to the conduction band, those two electrons turn into free electrons and the vacancy turns into a donor with 2^+ positive charges and this vacancy acts as a trap state. Therefore, oxide semiconductors are basically n-type semiconductors and this is the reason for the difficulty of achieving p-type oxide semiconductors.

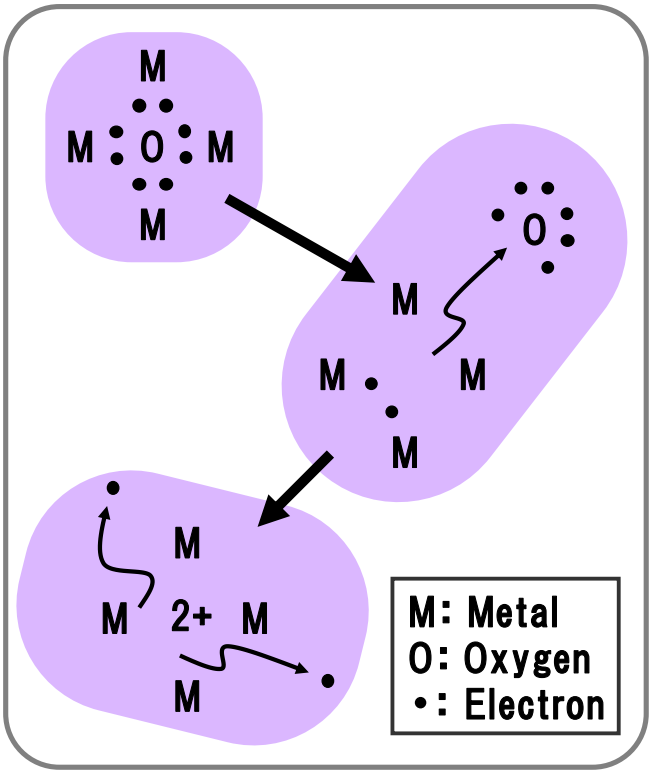


Fig. 1.4 Schematic drawings of carrier generation mechanism due to oxygen vacancy.

Controlling the properties of a-InGaZnO film regarding the oxygen vacancies is usually performed by combination of controlling of oxygen partial pressure (P_{O2}) during deposition of a-InGaZnO film and annealing after the deposition of the film. The main way to control the number of oxygen vacancies in an a-InGaZnO film is varying level of P_{O2} [36, 37]. An a-InGaZnO film is often deposited by RF or DC sputtering in a vacuum chamber and small amount of O_2 gas is introduced into the chamber during the sputtering. When P_{O2} is low, number of the oxygen vacancies is large and consequently free-electron carrier density (N_e) and number of trap states are large. Therefore, when the film is used as a channel layer of a TFT, turn on voltage (V_t) is low and *SS* is large.

In TFT application, the a-InGaZnO film is usually annealed after the deposition. An annealing in an atmosphere containing O_2 reduces oxygen vacancies and as a result, *SS*, electron mobility and bias stability of a TFT improves [28, 38].

Plasma treatment also affects on properties of an a-InGaZnO film [39, 40]. When an a-InGaZnO film is exposed to argon or other plasma, resistivity of the film decreases. It is presumed that the number of oxygen vacancies at the exposed surface increases due to the plasma damage [39]. In fact, although a TFT with plasma damaged channel layer showed a negative V_t and large *SS*, the effect of the damage disappeared when 30 nm of a-InGaZnO film from the exposed surface was wet etched [40]. In fabrication of back-channel-etch type TFT, in which source/drain electrodes are formed on top of an a-InGaZnO channel layer, exposure of the a-InGaZnO film to plasma is inevitable. This is because plasma etching is performed on the a-InGaZnO film in order to form the source/drain electrodes. Therefore, control of the plasma damage is a key technique in fabrication of back-channel-etch type TFT. One of the solutions to reduce the oxygen vacancies generated by the plasma damage is N_2O plasma treatment [41, 42].

1.4.4 Effect of hydrogen

Hydrogen also affects on resistivity or N_e of an a-InGaZnO film. As reported in [37], H_2 annealing at low temperature such as < 200^oC introduces free electrons into an a-InGaZnO film. H_2^+ ion implantation at room temperature also introduces free electrons. The calculation in [37] shows that the introduced H atoms always form O-H bonds and generate electrons; H (from outside) + O^{2-} (in a-InGaZnO) -> -OH^- (in a-InGaZnO) + e^-.

1.4.5 Effect of O_2 and H_2O adsorption

It is also reported that physical adsorption and desorption of O_2 and H_2O molecules on an a-InGaZnO film affects on properties of the film by charge transfer between the film and the molecules [43-45]. V_t of an a-InGaZnO TFT shifts to positive direction and *SS* of the TFT decreases when O_2 molecules are adsorbed and V_t shifts to negative direction and *SS* increases when O_2 molecules are desorbed [43, 45]. Therefore, it is presumed that N_e and trap states decrease when O_2 molecules are adsorbed and they increase when O_2 molecules are desorbed. On the other hand, the adsorption of H_2O molecules shifts V_t to negative direction and increases *SS* and the desorption of H_2O molecules shifts V_t to positive direction and decreases *SS* [44, 45] Therefore, it is presumed that N_e and trap states in an a-InGaZnO film and desorption of H_2O molecules reduces them.

1.4.6 Electronic structure

Not only the structure of the orbital network but also the electronic structure (i.e., density of states) of a-InGaZnO is very different from that of silicon [34, 37]. The various types of states in the band gap shown in Fig. 1.5 are generated by oxygen vacancies. The deep states (“deep levels” in Fig. 1.5) at the lower half of the band gap are basically occupied by electrons. Since those states are located at very deep place, they do not affect on the operation of the nMOS TFT. The states in the conduction band tail affect on the operation of the nMOS TFT. Therefore, in order to achieve good performance (i.e., high mobility, small *SS* and small hysteresis), densities of those shallow states need to be low. The most distinctive characteristics of the electronic structure is that there is a potential barrier in the conduction band at ~0.1 eV above conduction barrier minimum. This barrier leads to the unique dependence of the Hall

mobility on carrier density and temperature; the Hall mobility increases with increase in the carrier density and temperature

1.4.7 TFT application

From the basic understanding of a-InGaZnO mentioned above, the points in applying it to a channel layer of a TFT are summarized as follows.

1. Crystallinity of InGaZnO is not a big matter.
2. Oxygen vacancies in an a-InGaZnO film, H atoms in an a-InGaZnO film, O_2 molecules adsorbed on an a-InGaZnO film and H_2O molecules adsorbed on an a-InGaZnO film rule N_e and electronic structure of the a-InGaZnO film.

Therefore, we can use the amorphous phase of InGaZnO, which can be formed at low temperature, as a channel layer of a TFT. The control of oxygen vacancies, H atoms, O_2 molecules and H_2O molecules are important factors for the TFT characteristics such as off current (I_{off}), V_t, *SS*, on current (I_{on}) and reliability. The oxygen vacancies are controlled by P_{O2} during sputtering of a-InGaZnO, an annealing after the sputtering and plasma treatment. Amount of H atoms, O_2 molecules and H_2O molecules in or on an a-InGaZnO film are controlled by the exposure of the a-InGaZnO film to H_2, O_2 and H_2O during or after the TFT fabrication.

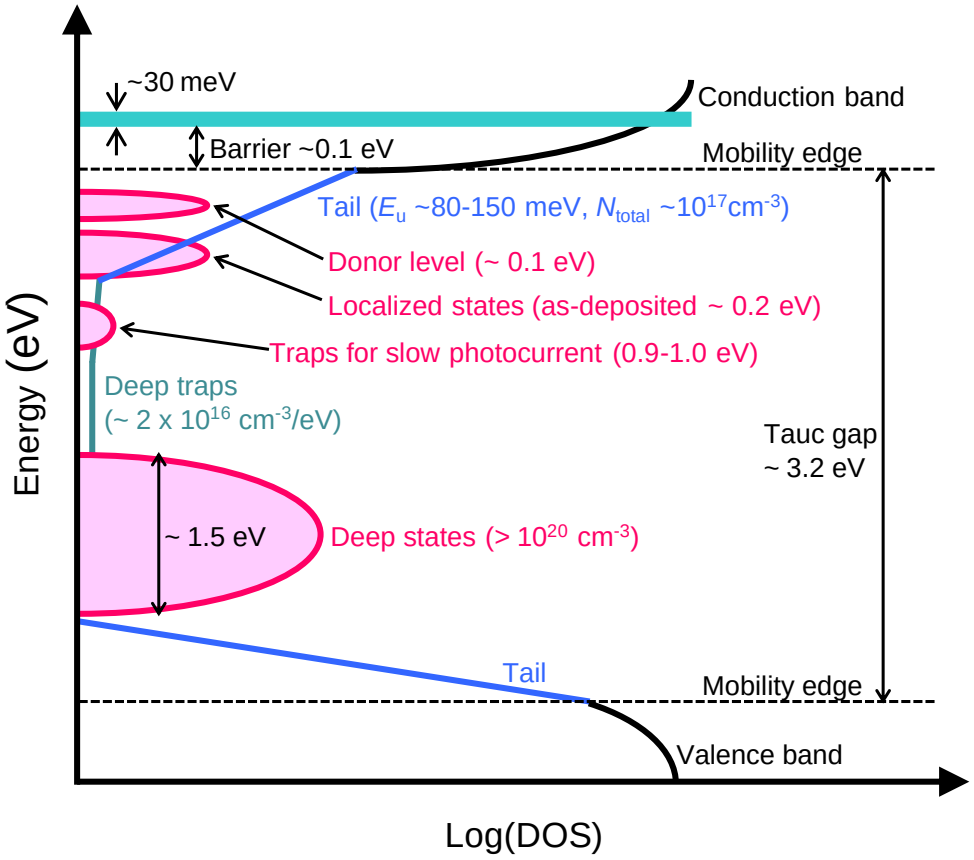


Fig. 1.5 Electronic structure (i.e., density of states (DOS)) of a-InGaZnO (reproduced from T. Kamiya *et al.*, *NPG Asia Mater.* (2010) [34], T. Kamiya *et al.*, *IEEE Trans. J. Disp. Tech.* (2009) [37]).

1.5 Issues in a-InGaZnO TFTs

As mentioned above, a-InGaZnO is a promising material for a channel layer of TFTs in terms of performance, reliability, fabrication process and fabrication cost. Active-matrix flat-panel displays using a-InGaZnO TFTs are already commercialized. However a-InGaZnO TFT still has some issues.

One of the big issues is the difficulty of achieving pMOS TFT. Oxide semiconductors are basically n-type semiconductors and it is difficult to achieve a p-type oxide semiconductor as already mentioned. The a-InGaZnO is not an exception and a pMOS

a-InGaZnO TFT good enough for circuit application is not available at present. Since we can not use CMOS inverter in an a-InGaZnO circuit, it is difficult to design a logic circuit operating at high frequency with low consumption power.

Another big issue is the difficulty of controlling V_t of a TFT. This also reduces the degrees of freedom in designing a circuit and makes it difficult to design a circuit operating at high frequency with low consumption power. V_t of a TFT can be shifted to negative direction by introducing oxygen vacancies by plasma treatment [39, 40] or by introducing H atoms by annealing or ion implantation [37] into an a-InGaZnO film. However, in some cases they increase trap states and deteriorate reliability of a TFT. Furthermore, as far as our knowledge, there is no way to shift V_t to positive direction by controlling property of an a-InGaZnO film itself. Although the dual gate structure (one under a channel layer and the other over the channel layer) or introduction of a negative charge into a gate insulator can shift V_t to positive direction, they increase fabrication process steps and hence increase fabrication cost.

The third big issue is the difficulty of ensuring the long-term reliability of a TFT [42, 46-48]. V_t of an a-InGaZnO TFT shift to positive direction when a positive bias is applied to a gate electrode for a period and shift to negative direction when a negative bias is applied. This is presumed to be caused by the charge trapping at the interface states between an a-InGaZnO layer and a gate insulator layer or the bulk trap states in the a-InGaZnO film. In some cases *SS* increases at the same time and this is presumed to be caused by the increase of interface trap states. The shifting of V_t accelerates when light is irradiated to an a-InGaZnO layer during negative bias application to a gate electrode. This phenomenon is caused by trapping of photo-generated holes. All these instability problems accelerate by increasing temperature during the tests. The most

widely used solution to improve the reliability of an a-InGaZnO TFT is the annealing at 250-350^{o}C. The annealing reduces the trap states at the interface or in the bulk and gives high enough reliability for some types of displays. However the annealing temperature is too high to apply it to flexible devices since, as far as our knowledge, the available plastic films for a substrate can only endure up to 150-200^{o}C. Therefore, we need to ensure the long-term reliability with annealing at less than 150^{o}C to achieve the flexible RFID.

1.6 Objective of this study

The objective of this study is development of the three element technologies listed blow to achieve the flexible passive-type RFID tag with monolithic antenna that can be operated by 13.56-MHz RFID reader.

1. Low-voltage operating transistor that can be fabricated on a flexible substrate.
2. Rectifier that can convert 13.56-MHz radio wave into a DC power.
3. Logic gate that enables the internal data-processing circuits to operate within the power supplied through the rectifier and with the frequency accepted by the reader terminal.

The RFID tag achieved with these technologies will be a basic device that has indispensable functions for a wireless sensor network.

1.7 Outline of this thesis

This thesis is regarding to the low-power operating oxide thin-film transistors and circuits for flexible wireless device application.

In chapter 1, the foresight of the connected devices, the necessity of the flexible passive-type RFID and the basics of oxide semiconductor (especially a-InGaZnO), are described.

In chapter 2, the concept, fabrication and experimental results of a low-voltage operating fully-depleted type a-InGaZnO TFT, which is proposed in this study, are described.

In chapter 3, the designing, fabrication and experimental results of a rectifier circuit using the above fully-depleted a-InGaZnO TFT are described. The rectifier circuit is targeted at the operation with 13.56-MHz band since this frequency band is widely used for wireless devices such as RFID.

In chapter 4, the designing, fabrication and experimental results of a capacitive-coupling type logic gate are described. The logic gate satisfies both the operation frequency and the consumption power required for the wireless operation of the RFID.

In chapter 5, the final chapter, conclusion and the foresight are described.

Chapter 2

Development of low-voltage operating a-InGaZnO TFT

2.1 Issues in conventional TFTs

TFTs should have high mobility, high uniformity and high stability with low temperature process, since they determine the performance of the devices. Moreover, TFTs need to operate at low voltage if circuits are driven by a battery or a wireless power transmission. For such low-voltage operation, namely to have high on/off ratio under low-voltage operation, TFTs with low I_{off}, small V_t and small *SS* are also essential.

However, conventional TFTs do not satisfy the above requirements simultaneously. Although hydrogenated a-Si TFTs have good uniformity over a large area, their *SS* is 300 mV/decade or larger and their stability under electrical stress is not sufficient [17-20]. pc-Si TFTs have high mobility and high stability [21-23]. Some of them with large crystal grains even have relatively small *SS* values, such as 200 mV/decade or smaller [22, 23]. However, high temperature (450^{o}C or above) annealing is necessary for impurity activation; this makes it difficult to fabricate poly-Si TFTs directly on a plastic substrate. Organic TFTs are being intensively studied as a next-generation technology. However, finding a means of raising both mobility and stability is still a challenge. Furthermore, the reported values of their V_t is as high as several to tens of volts and *SS* is larger than 300 mV/decade [24-26].

TFTs using amorphous oxide semiconductors such as InGaZnO [27-32], and Zn-Sn-O [33, 49] reportedly have good performance. These amorphous oxide TFTs operate as

nMOS TFTs with high mobility, high uniformity, high stability under electrical stress, V_t near 0 V, and relatively small *SS* (< 200 mV/decade). Furthermore, amorphous oxide semiconductors can be deposited by low-temperature (around room temperature) sputtering, which is suitable for a flexible substrate. By taking advantage of these features, high-performance low-voltage-operating TFTs on a large and flexible substrate might be able to be fabricated.

TFTs using polycrystalline oxide semiconductors such as Zn-O also show good performance [50-53]. However, as far as we know, amorphous oxide TFTs show better performance when the oxide channels are deposited by sputtering at room temperature. Therefore, we chose a-InGaZnO for the channel layer.

2.2 Proposal and designing of fully-depleted amorphous oxide TFTs

An on/off ratio during low-voltage operation can be increased by decreasing I_{off} and *SS*, and increasing I_{on}. In this study, we focused on decreasing I_{off} and *SS* [54, 55]. Since oxide semiconductors intrinsically have n-type features and TFTs operate as accumulation mode devices, the fully-depleted (FD) off state is suitable for a small I_{off} and a small *SS*. When an FD oxide TFT is turned off, in other words, when 0 V or a negative voltage is applied to a gate electrode, both the conduction and the valence bands bend upwards across the channel layer. Thus, a depletion layer, which is an insulator, is formed throughout the channel layer. Figure 2.1 shows the band diagram when the voltage applied to the gate electrode is slightly lower than the voltage where the current start to flow; i.e., slightly lower than the voltage where the subthreshold

region starts. Here, W_{dep} is the maximum width of the depletion layer, E_c, E_v, E_f, E_i are the energy level of the conduction band, valence band, Fermi level and intrinsic level, respectively, and φ_g is the potential gap between E_f and E_i, when the band is not bended.

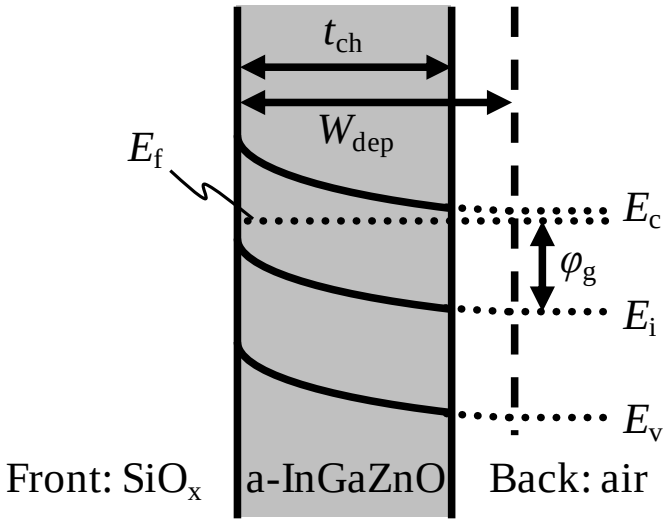


Fig. 2.1 Band diagram of a-InGaZnO in fully-depleted (FD) state.

To achieve FD state, t_{ch} (thickness of the channel layer) needs to be smaller than W_{dep} as in Fig. 2.1. According to the semiconductor theory, the hole accumulation should occur in a-InGaZnO when a negative voltage is applied to the gate electrode. However, in reality, the hole accumulation does not occur due to the subgap states in a-InGaZnO. It is reported in [37] and [56] that the subgap states occupy lower half of the bandgap (note that the tail of the subgap density of states crosses over the middle of the gap) and they are filled with electrons. The filled electrons in the subgap states prevent the hole accumulation because the amount of the states is estimated as to be two orders of magnitude larger than the holes that can be induced by the electric field form the gate

electrode. Therefore, E_f can exist only in the upper half of the bandgap. In other words, the width of the depletion layer maximizes when E_f reaches to the middle of the gap (i.e., E_i). Thus the condition to achieve the FD state is

$$t_{ch} < W_{dep} = \sqrt{\frac{4\varepsilon_0 \varepsilon_{InGaZnO} \phi_g}{qN_e}}, \tag{2.1}$$

therefore,

$$N_e t_{ch}^2 < \frac{4\varepsilon_0 \varepsilon_{InGaZnO} \phi_g}{q}. \tag{2.2}$$

Here, q is the elementary charge, N_e is a carrier density, ε_0 is the vacuum permittivity, $\varepsilon_{InGaZnO}$ is the relative permittivity of a-InGaZnO. The FD mode operation is achieved when $N_e t_{ch}^2$ is sufficiently small. Otherwise, the TFTs operate in a partially-depleted (PD) mode. We assumed $\varepsilon_{InGaZnO}$ = 10 [57]. Since the bandgap of a-InGaZnO is around 3.2 eV and the Fermi level is near the mobility edge of the conduction band [36, 37, 56], we assumed $\varphi_g \sim 3.2/2 = 1.6$ eV. Both the conduction and valence bands bend upwards across the channel layer when the FD a-InGaZnO TFTs are turned off. Thus, a depletion layer, which is an insulator, is formed throughout the channel layer. Most of the current in the FD a-InGaZnO TFTs flows at the back interface in the subthreshold region since the energy level of the conduction band is the lowest at the back interface as shown in Fig. 2.1.

Figure 2.2 shows the relationship between N_e and t_{ch} calculated from equation (2.2). The FD state is achieved when N_e and t_{ch} are sufficiently small to be in the gray region. Otherwise, a TFT operates in PD mode.

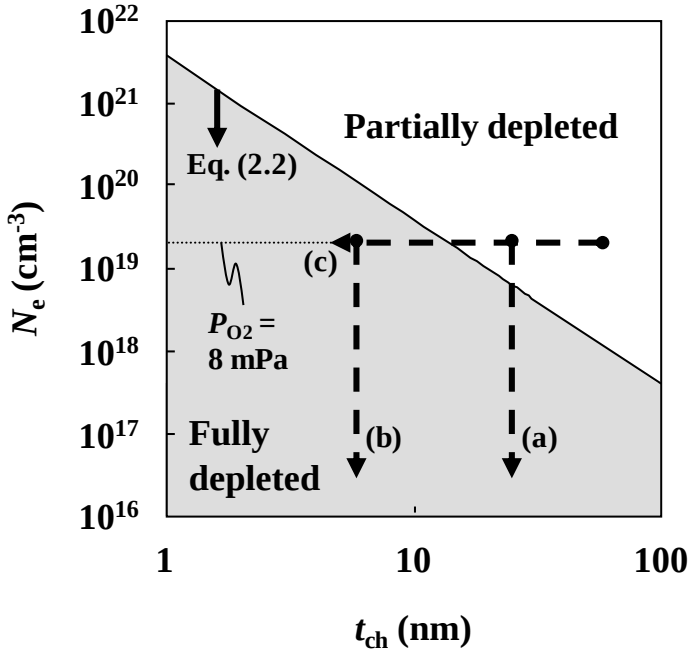


Fig. 2.2 Relationship between carrier density (N_e) and channel layer thickness (t_{ch}) calculated from equation (2.2).

2.3 Fabrication of sample TFTs

Inverted staggered (bottom gate, top contact; Fig. 2.3 (a)) and inverted coplanar (bottom gate, bottom contact; Fig. 2.3 (b)) structure TFTs were fabricated using a-InGaZnO as a channel layer. The inverted staggered TFTs were used to investigate effects of changing t_{ch}, P_{O2} during the sputtering of a-InGaZnO, a gate insulator formation process and gate insulator thickness. The inverted coplanar TFTs were used to investigate channel length (L) dependence.

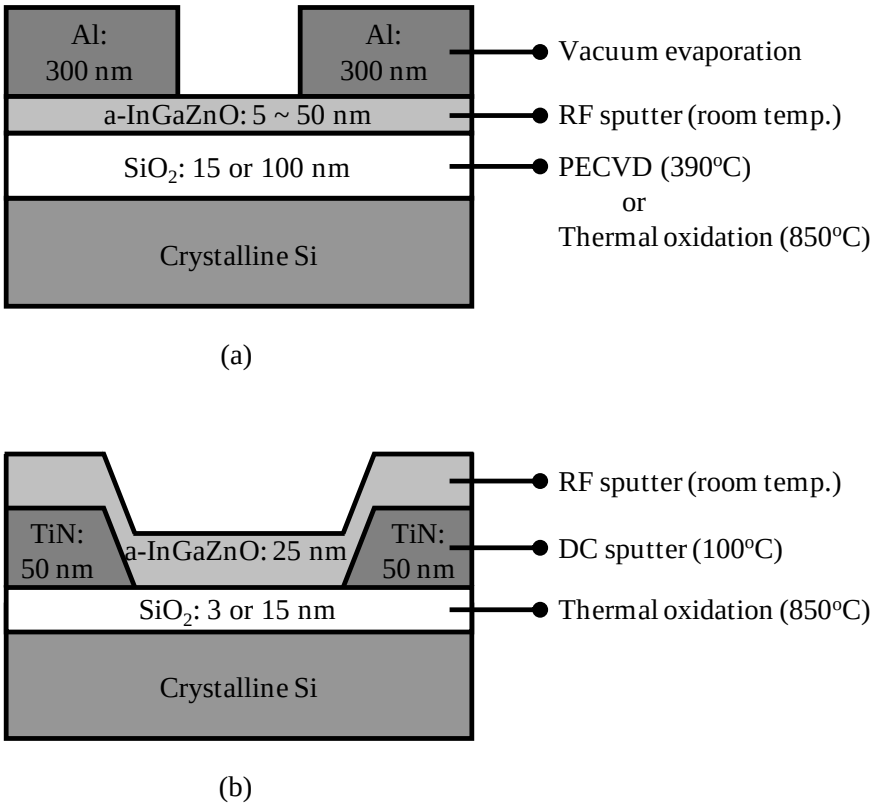


Fig. 2.3 Cross-sectional views of sample TFTs; (a) inverted staggered (bottom gate, top contact) type and (b) inverted coplanar (bottom gate, bottom contact) type.

In a fabrication of the inverted staggered TFT, a 100-nm-thick SiO_2 was deposited by plasma enhanced chemical vapor deposition (PECVD) at 390°C, or a 10 to 200-nm thick thermal SiO_2 was formed at around 850°C as a gate insulator on a crystalline Si (c-Si), which acts as a gate electrode. Then, an a-InGaZnO channel layer was deposited by radio-frequency (RF) magnetron sputtering at room temperature. t_{ch} was varied from 5 to 50 nm, and P_{O2} was varied from 8 to 70 mPa. After that, 300-nm-thick Al electrodes were deposited on the a-InGaZnO channel layer through a shadow mask to form source/drain electrodes. Channel width (W) and L were 2000 μm and 100 μm, respectively.

In a fabrication of the inverted coplanar TFTs, a 3 or 15-nm-thick thermal SiO_2 was formed at 850^{o}C on a c-Si as a gate insulator. After that, a 50-nm thick TiN was deposited by sputtering and patterned by photolithography and wet etching to form source/drain electrodes. *L* was varied from 2 to 100 μm. Finally, an a-IGZO channel layer was deposited by RF magnetron sputtering at room temperature.

Although we need to use PECVD to form the gate insulator when we apply the TFTs to the flexible devices, we used the thermal SiO_2 for some of the TFTs in this feasibility study to focus on the effects from a-InGaZnO films. We also did not stack a passivation layer on an a-InGaZnO layer for the same reason. The TFTs were annealed at 125^{o}C in a controlled dry air atmosphere (the percentages of H_2 and H_2O were almost 0% and that of O_2 was 21%) after the fabrication and the electrical determinations of the TFTs were performed within the same atmosphere. Since the TFTs used in this study do not have a passivation layer, V_t and *SS* might vary, as mentioned above, if the atmosphere is not controlled due to the adsorption and desorption of the H_2O and O_2 molecules on an a-InGaZnO layer [43-45]. We chose a low annealing temperature such as 125^{o}C since it can be applied to the flexible devices in the future.

The crystallinity of InGaZnO films was evaluated by cross-sectional transmission electron microscope (TEM) observations. The TEM observations were performed after annealing at 125^{o}C. Figure 2.4 shows a cross-sectional TEM micrograph of an a-InGaZnO TFT. The InGaZnO on a 15-nm thick SiO_2/c-Si stack was 6-nm thick. The micrograph indicates that the InGaZnO remained amorphous even after the annealing at 125^{o}C. The interface between the a-InGaZnO and the SiO_2 was flat and smooth, which might be important for the small *SS*.

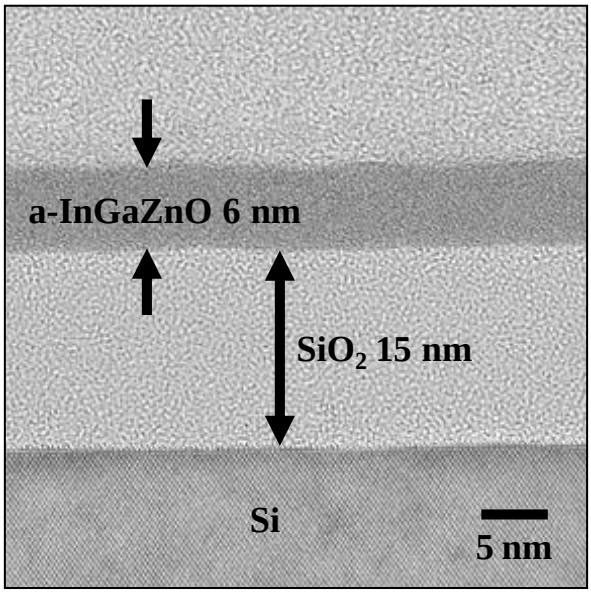


Fig. 2.4 Cross-sectional transmission electron microscope (TEM) micrograph of a-InGaZnO TFT after 125°C annealing.

2.4 Effect of annealing

The authors found that the annealing process was necessary to achieve the FD mode operation. Figure 2.5 shows the source-drain current (I_{ds}) versus source to gate voltage (V_{gs}) curves of three a-InGaZnO TFTs immediately after the fabrication and after the 125°C annealing. The differences among the three TFTs are P_{O2} during the sputtering of the a-InGaZnO layer, thus N_e, and t_{ch}. Before the annealing, TFT A and C had negative V_t and large *SS* while TFT B did not even show on/off behavior in the measured V_{gs} range. However, for all the TFTs, V_t shifted in the positive direction and *SS* decreased after the annealing. The negative V_t was larger when P_{O2} was smaller (i.e. N_e was larger) or t_{ch} was larger, namely when $N_e t_{ch}^2$, the left side of equation (2.2), was larger. This is

likely to be due to the less controllability of the bands near the backside of the channel by V_{gs}. The results indicate that there were excessive carriers that cause the negative V_t and trap states that cause the large *SS* before the annealing and they were reduced by the annealing.

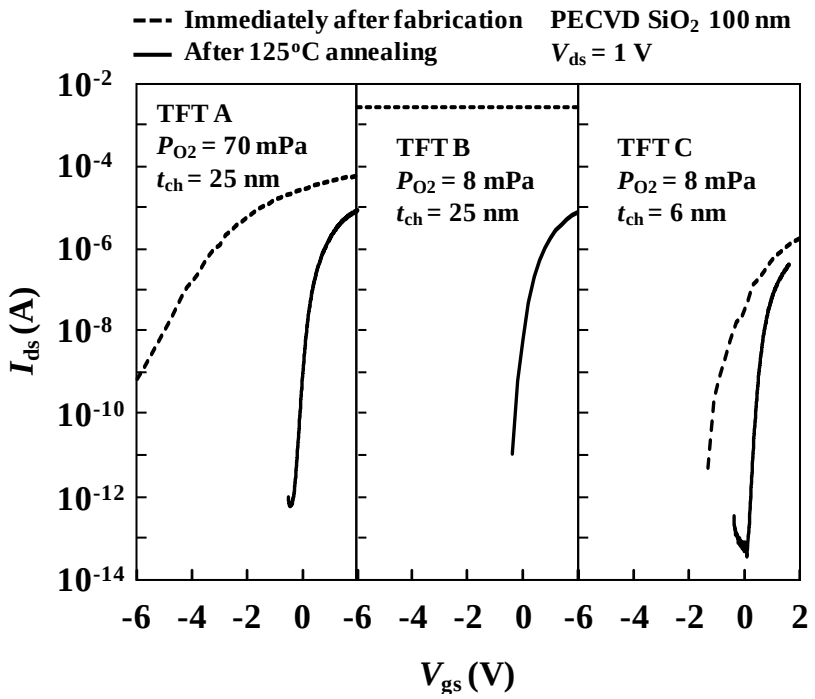


Fig. 2.5 I_{ds}-V_{gs} curves of a-InGaZnO TFTs immediately after fabrication and after 125°C annealing.

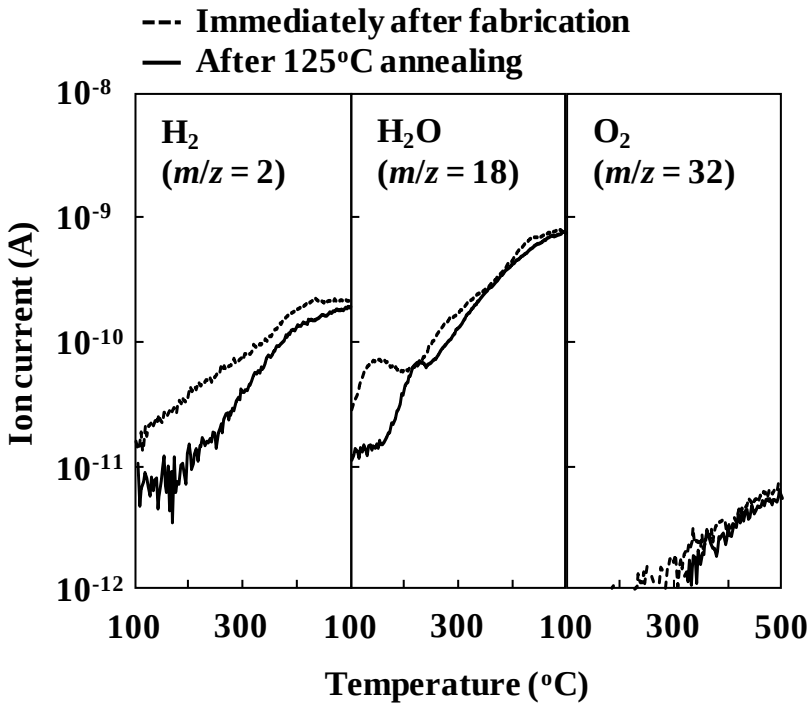


Fig. 2.6 Thermal desorption spectra of H_2, H_2O and O_2 from a-InGaZnO films immediately after deposition and after 3 hours of 125°C annealing.

One possible origin of these variations of the I_{ds}-V_{gs} curves is decreasing of oxygen vacancies, which serve as the electron donors, during the annealing. However, the main part of the oxidation of a-InGaZnO usually takes place at a higher temperature such as >300°C [37]. We evaluated the thermal desorption from a-InGaZnO films to investigate other origin. As shown in Fig. 2.6, more H_2 and H_2O were detected from an a-InGaZnO film immediately after the deposition than from an a-InGaZnO film after the 125°C annealing. Therefore, the H_2 and H_2O probably caused the negative V_t and the large *SS*. We presume that the origin of the H_2 is hydrogen incorporated in the a-InGaZnO film. Desorption of H^0 should reduce a free electron since introduction of H^0 generates a free electron [37, 58]. On the other hand, we presume that the origin of H_2O is the molecules adsorbed on or encapsulated in the a-InGaZnO film since the desorption of the H_2O

molecules reduces free electrons and trap states [44]. In addition to that, OH incorporated in the film but not bonding strongly with the metal cation might also be the origin of H_2O (note that the reaction to form H_2O from the OH bonding with the cation likely generates free electrons [37]). The less desorption from the annealed film even above 125^{o}C might be because the annealing time (3 hours) was long compared to the temperature sweep time (swept at 30^{o}C/minute).

2.5 Electrical characteristics of fabricated TFTs

2.5.1 Measurement conditions

The electrical characteristics of the a-InGaZnO TFT were evaluated by using a semiconductor parameter analyzer (Agilent 4156B). The TFTs were put under dry air atmosphere (the amount H_2 and H_2O was almost 0% and that of O_2 was fixed at 21%) during the electrical measurement. This is to avoid the exposure of a-InGaZnO channel layer to H_2, H_2O and O_2 since these molecules affect on N_e, which is an important parameter for the FD-TFTs.

2.5.2 Dependence on oxygen partial pressure

Oxygen vacancies generate carrier electrons in oxide semiconductors. Therefore, N_e can be reduced by increasing P_{O2}. The transition from the PD to the FD mode by reducing N_e was confirmed with the samples in which N_e was reduced along the dashed arrows (a) and (b) in Fig. 2.2. t_{ch} was kept at 25 nm or 6 nm, and P_{O2} was varied from 8 mPa to 70 mPa. N_e was determined to be as around 2×10^{19} cm^{-3} when P_{O2} was 8 mPa, from Hall measurements. We could not determine N_e when P_{O2} was 20 mPa or larger

since it was lower than the detection limit of our equipment, which is ~ 10^{18} cm^{-3}. Therefore, the *SS* values are plotted against P_{O2} (not against N_e) in Fig. 2.7. *SS* decreased from 230 to 100 mV/decade by increasing P_{O2} (namely by reducing N_e) when t_{ch} is 25 nm, corresponding to the transition from the PD to the FD mode. On the other hand, when t_{ch} is 6 nm, *SS* was almost constant (~ 80 mV/decade) and independent of P_{O2} (or N_e), indicating that all the TFTs with 6-nm channel layer operated in the FD mode, as was expected from Fig. 2.2.

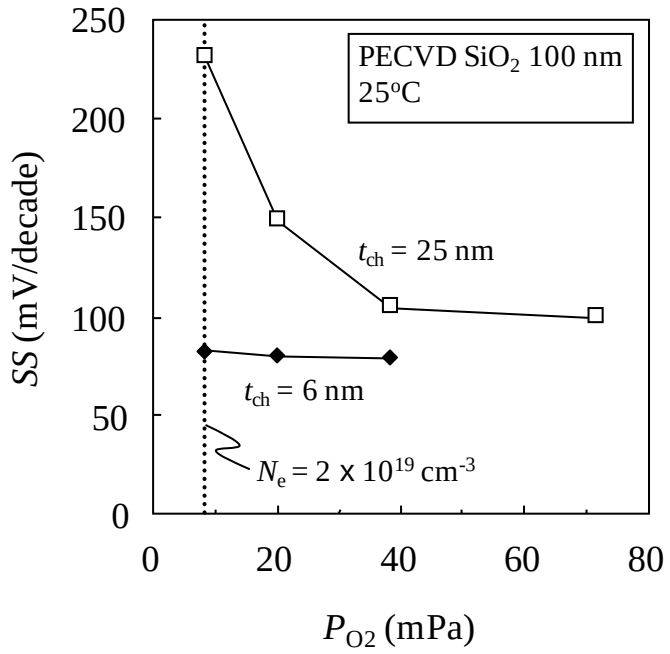


Fig. 2.7 Dependence of subthreshold slope (*SS*) on oxygen partial pressure (P_{O2}) measured at 25°C.

2.5.3 Dependence on thickness of a-InGaZnO layer

To confirm that the operating mode of a TFT changes from the PD to FD mode by reducing t_{ch}, we prepared samples in which t_{ch} was reduced along the dashed arrow (a) in Fig. 2.2. In this experiment, N_e was kept at 2×10^{19} cm^{-3} and t_{ch} was varied from 75 nm to 5 nm. Figure 2.8 shows the dependence of I_{ds}-V_{gs} curve of TFTs on t_{ch}. When t_{ch} was larger than 75 nm, the TFTs did not turn off even when -50 V was applied to the gate electrode (this is the reason why we focused on the development of a low-voltage operating TFT). TFT turned off when t_{ch} was less than 50 nm, and switching characteristics improved with decreasing t_{ch} (-4 V was necessary to turn off the TFT with 50-nm channel). The *SS* values are summarized in Fig. 2.9. *SS* was over 1000 mV/decade when t_{ch} was 50 nm. It decreased with decreasing t_{ch} and asymptotically approached to 80 mV/decade, indicating the transition from the PD to FD mode.

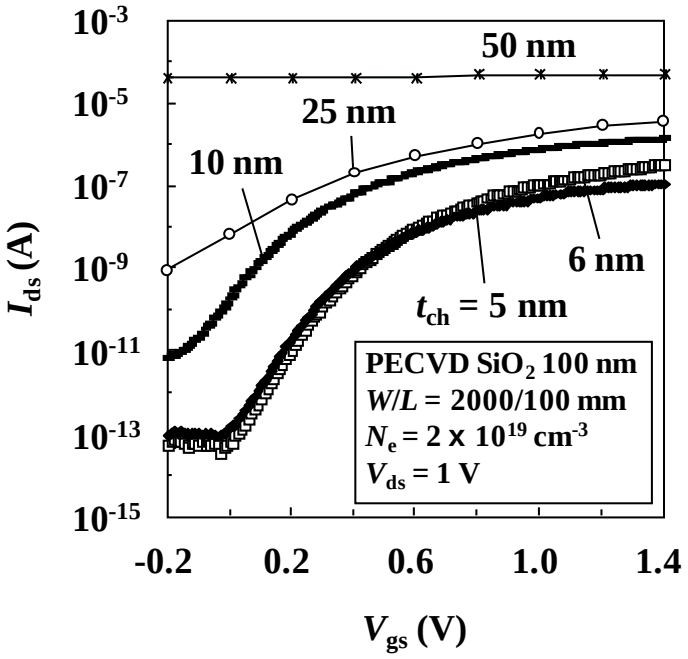


Fig. 2.8 I_{ds}-V_{gs} curves of a-InGaZnO TFTs with various channel layer thickness (t_{ch}) measured at 25^{o}C.

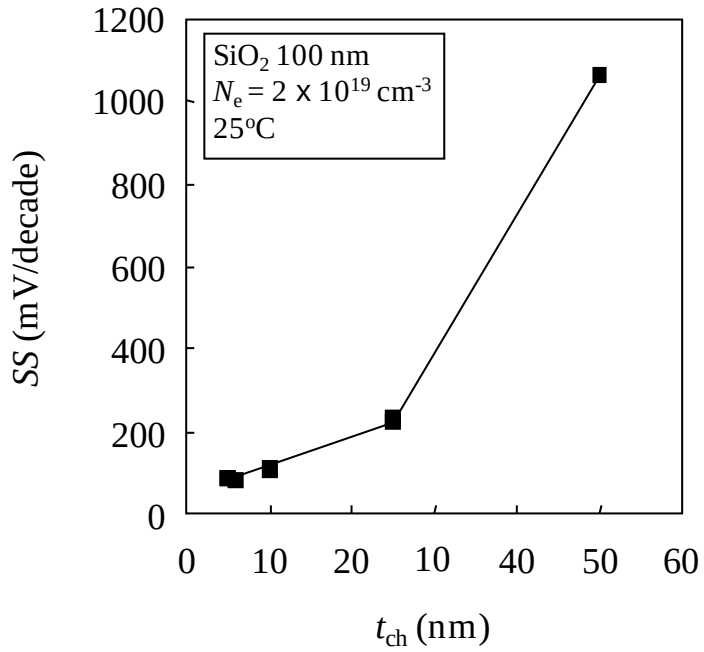


Fig. 2.9 Dependence of subthreshold slope (*SS*) on channel layer thickness (t_{ch}) measured at 25°C.

Table 2.1. Design parameters and *SS* at 25°C of fabricated TFTs.

No.	Gate insulator	P_{O2} (mPa)	t_{ch} (nm)	*SS* (mV/decade)	Fig. 2.5
1	PECVD SiO_2 100 nm	8	6	82	TFT C
2	PECVD SiO_2 100 nm	20	6	80	-
3	PECVD SiO_2 100 nm	38	6	79	-
4	PECVD SiO_2 100 nm	38	25	104	TFT A
5	PECVD SiO_2 100 nm	70	25	99	-
6	Thermal SiO_2 100 nm	8	6	83	-
7	Thermal SiO_2 100 nm	38	25	108	-

Table 2.1 lists P_{O2}, t_{ch} and *SS* of TFT A, C in Fig. 2.5, some TFTs in Fig. 2.7 and some other fabricated TFTs. All of these TFTs should operate in the FD mode based on equation (2.2). We found that TFTs with a 6-nm t_{ch} tend to have a smaller *SS* than those with a 25-nm t_{ch} and that TFTs with larger P_{O2} tend to have a smaller *SS*. The reason for these results will be discussed later.

2.5.4 Dependence on deposition method of gate insulator

We fabricated and evaluated TFTs with three types of gate insulators; 100-nm-thick PECVD-SiO_2 and 100- and 15-nm-thick thermal SiO_2. t_{ch} and N_e were kept at 6 nm and 2×10^{19} cm^{-3} respectively. I_{ds}-V_{gs} curves for the TFTs with the three gate insulators are plotted in Fig. 2.10. At 25°C, the TFTs with a 100-nm-thick PECVD-SiO_2 and with a 100-nm-thick thermal SiO_2 showed almost identical characteristics; *SS* ~ 82 mV/decade, $I_{off} < 10^{-17}$ A per 1-μm channel width (lower than the detection limit of our equipment), and on/off ratio ~ 10^7 for a 1.5-V V_{gs} swing. The TFT with a 15-nm-thick thermal SiO_2, which has a larger gate oxide capacitance, had superior characteristics; *SS* = 63 mV/decade, $I_{off} < 10^{-17}$ A per 1-μm channel width, and on/off ratio ~ 10^8 for a 1.5-V V_{gs} swing.

Though these TFTs showed good characteristics, I_{on} was not high enough compared to the value expected from the electron mobility in a-InGaZnO. We presume that the contact resistance between the Al source/drain electrode and a-InGaZnO channel layer is high when the a-InGaZnO film is thin as 6 nm. Therefore, we redesigned the structure of the TFT when we applied it to circuits.

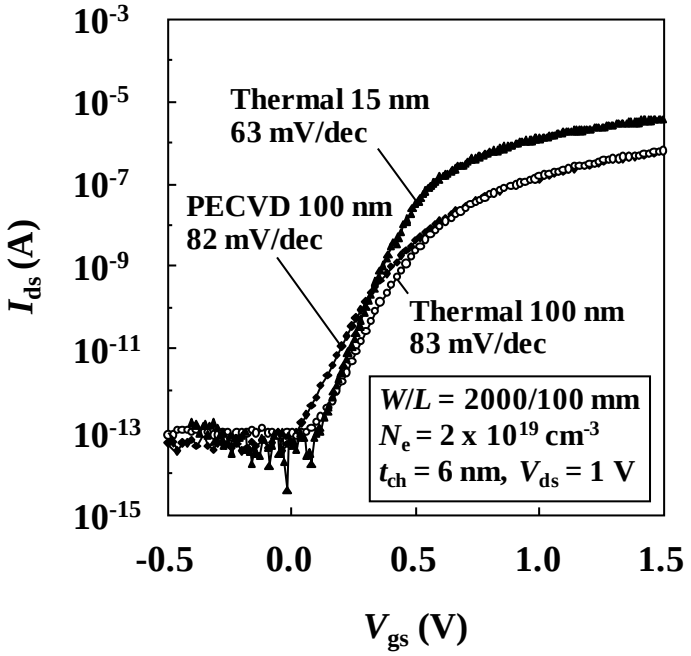


Fig. 2.10 I_{ds}-V_{gs} curves of a-InGaZnO TFTs with various SiO_2 gate insulators measured at 25°C.

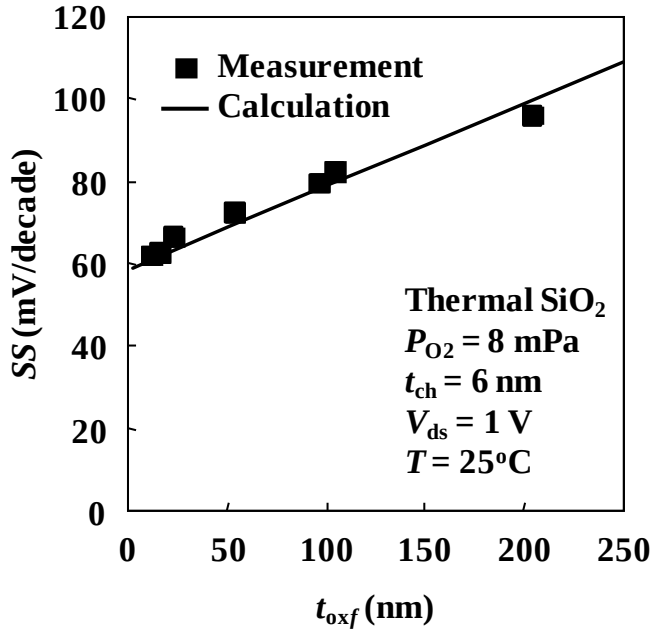


Fig. 2.11 Dependence of *SS* on t_{oxf} at 25°C. The linear curve is calculated data using equation (2.8) by substituting $C_{itf}+C_{itb}+2C_{sg}+2C_{fr} = 1.17\times10^{-4}$ F/m^2.

2.5.5 Dependence on thickness of gate insulator

We fabricated and evaluated TFTs with 11 to 204-nm-thick thermal SiO_2 gate insulators and 6-nm-thick a-InGaZnO channel layers. The smallest *SS* was 62 mV/decade when the thickness of the SiO_2 gate insulator (t_{oxf}) was 11 nm. As shown in Fig. 2.11, *SS* increased linearly with increase in t_{oxf}.

2.5.6 Dependence on operation temperature

Figure 2.12 shows the operation temperature dependence of *SS* of the TFT with a 15-nm-thick thermal SiO_2 gate insulator and a 6-nm-thick a-InGaZnO channel layer. The temperature of the TFT (*T*) was varied from -25 to 100°C. The *SS* increased linearly with increase in *T*.

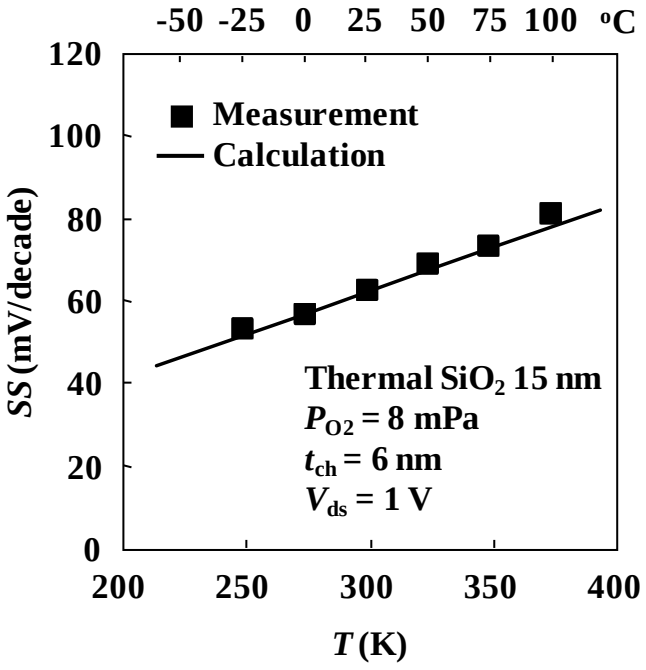


Fig. 2.12 Dependence of *SS* on *T*. The linear curve is calculated data using equation (2.8) by substituting $C_{itf}+C_{itb}+2C_{sg}+2C_{fr} = 1.17\times10^{-4}$ F/m^2.

2.5.7 Dependence on channel length

Dependence of characteristics of FD InGaZnO TFT on L were investigated by using inverted coplanar TFTs. L was varied from 100 μm down to 2 μm, while W, t_{ch} and N_e were kept at 1000 μm, 6 nm and 2×10^{19} cm^{-3}, respectively. Figure 2.13 plots the dependence of V_t, which is defined as V_{gs} where $I_{ds} = 5 \times 10^{-10}$ A, on L for TFTs with 15-nm and 3-nm-thick thermal SiO_2 gate insulators. V_t shifted to the negative direction as L decreased. It is considered that this dependence is due to the drain-induced barrier lowering effect in a-InGaZnO TFT. Figure 2.14 shows the dependence of SS on L. In contrast to V_t, SS was almost constant from L = 100 μm down to L = 2 μm, indicating that the FD a-InGaZnO TFT is scalable down to 2 μm or less.

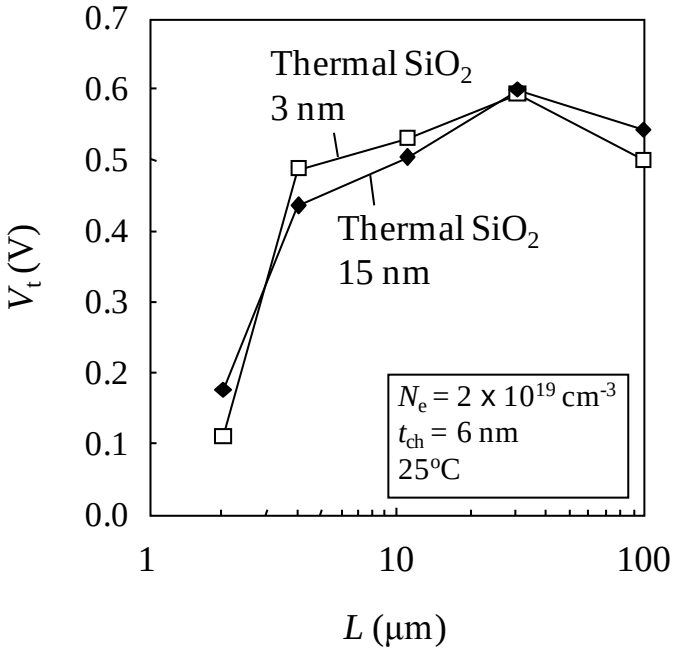


Fig. 2.13 Dependence of V_t on L.

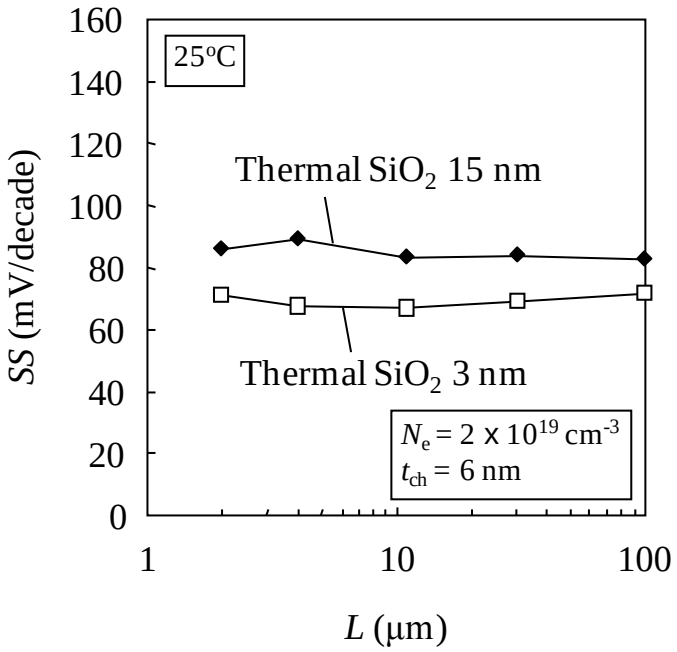


Fig. 2.14 Dependence of *SS* on *L*.

2.6 Discussion

2.6.1 *SS* of FD a-InGaZnO TFT

The above mentioned results indicate that the theoretical equation for *SS* should explain that *SS* (a) increases with increase in t_{ch}, (b) increases with decrease in P_{O2}, (c) increases linearly with increase in t_{oxf}, and (d) increases linearly with the increase in *T*.

We derived a theoretical equation for *SS* of FD a-InGaZnO TFT by starting from the equation developed for silicon on insulator (SOI) MOS transistor since the device structures are similar to each other. It has been reported that *SS* of SOI MOS transistor can be described as follows [59, 60];

$$SS_{ij} = \left(\frac{d \log_{10} I_{dj}}{dV_{gi}} \right)^{-1} = \log_e 10 \frac{kT}{q} \frac{dV_{gi}}{d\phi_j} \quad , \tag{2.3}$$

where I_{dj} is a drain current, V_{gi} is a gate voltage, k is the Boltzmann constant and φ_j is a surface potential. The subscript i indicates the gate that is operated and j indicates the surface where most of the current flows. These subscripts take on either f or b, where f corresponds to the front of the channel layer and b corresponds to the back of it. Most of the current in an FD a-InGaZnO TFT flows on the back surface in the subthreshold region because the potential in the channel layer is the lowest on the back surface as shown in Fig. 2.1. Therefore, we should consider $SS_{fb} = \log_e 10(kT/q)(dV_{gf}/d\varphi_b)$.

The FD a-InGaZnO TFT can be modeled using the equivalent circuit shown in Fig. 2.15, where C_{oxf}, C_{itf}, C_{itb}, C_{sg}, C_d and C_{fr} are the capacitances of the SiO_2 gate insulator, the interface traps at front and back surfaces, the subgap states [61] in half of the thickness of the amorphous semiconductor film ($t_{ch}/2$), the depleted semiconductor film and the fringe coupling. V_g, V_d and V_s are the gate, drain and source voltages. The relations between the variations in voltages applied to the electrodes (ΔV_g, ΔV_d, and ΔV_s) and the variations in the surface potentials ($\Delta\varphi_f$ and $\Delta\varphi_b$) are derived from the charge conservation law;

$$C_{oxf}\left(\Delta\phi_f - \Delta V_g\right) + \left(C_{itf} + C_{sg}\right)\Delta\phi_f + C_d\left(\Delta\phi_f - \Delta\phi_b\right) = 0\,, \tag{2.4}$$

$$C_{fr}\left(\Delta\phi_b - \Delta V_d\right) + C_{fr}\left(\Delta\phi_b - \Delta V_s\right) + \left(C_{itb} + C_{sg}\right)\Delta\phi_b + C_d\left(\Delta\phi_b - \Delta\phi_f\right) = 0\,. \tag{2.5}$$

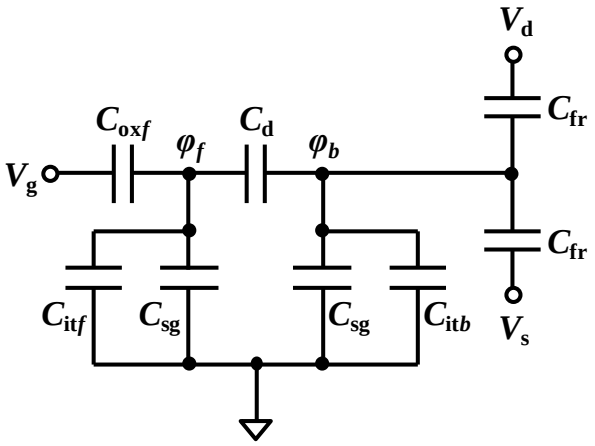


Fig. 2.15 Equivalent circuit model of FD a-InGaZnO TFT.

Here, we assume that the variation in the potential across the depleted semiconductor film is linear; i.e., the electric field across the film is constant. Considering that $\Delta V_d = \Delta V_s = 0$, the ΔV_g is derived from equations (2.4) and (2.5) as follows;

$$\Delta V_g = \left(1+\frac{2C_{fr}+C_{itb}+C_{sg}}{C_d}\right)\left(1+\frac{C_{itf}+C_{sg}}{C_{oxf}}+\frac{C_d}{C_{oxf}}\frac{2C_{fr}+C_{itb}+C_{sg}}{C_d+2C_{fr}+C_{itb}+C_{sg}}\right)\Delta\phi_b, \tag{2.6}$$

and by substituting equation (2.6) into (2.3),

$$SS_{fb} = \log_e 10\frac{kT}{q}\left(1+\frac{2C_{fr}+C_{itb}+C_{sg}}{C_d}\right)\left(1+\frac{C_{itf}+C_{sg}}{C_{oxf}}+\frac{C_d}{C_{oxf}}\frac{2C_{fr}+C_{itb}+C_{sg}}{C_d+2C_{fr}+C_{itb}+C_{sg}}\right). \tag{2.7}$$

Equation (2.7) explains that the *SS* is small when C_d and C_{oxf} are large while C_{fr}, C_{itf}, C_{itb} and C_{sg} are small. It also explains that the theoretical minimum for the *SS* is $\log_e 10(kT/q)$, which is 59.2 mV/decade at 25°C. The *SS* increases with decrease in C_d (= $\varepsilon_0\varepsilon_{InGaZnO}/t_{ch}$) or increase in C_{sg}, and therefore, with the increase in the t_{ch}. The result listed in Table 2.1, in which the FD TFTs with a 25-nm t_{ch} had a larger *SS* than the FD TFTs with a 6-nm t_{ch}, is understood from equation (2.7).

Using equation (2.7) and the result in Fig. 2.11, $2C_{fr}+C_{itb}+C_{sg} < C_d/99$ is derived when t_{ch} = 6 nm and t_{oxf} = 11-204 nm. Therefore, the terms in the first brackets of equation (2.7) are approximated to be 1 and the terms in the second brackets are approximated to be $1+(C_{itf}+C_{itb}+2C_{sg}+2C_{fr})/C_{oxf}$. From these assumptions, equation (2.7) is rewritten as

$$\begin{aligned} SS_{fb} &= \log_e 10\frac{kT}{q}\left(1+\frac{C_{itf}+C_{itb}+2C_{sg}+2C_{fr}}{C_{oxf}}\right) \\ &= \log_e 10\frac{kT}{q}\left\{1+\frac{\left(C_{itf}+C_{itb}+2C_{sg}+2C_{fr}\right)t_{oxf}}{\varepsilon_0\varepsilon_{SiO2}}\right\} \end{aligned}, \tag{2.8}$$

where ε_{SiO2} is the relative permittivity of SiO_2. Equation (2.8) indicates that a very small *SS* such as 62 mV/decade was obtained since $C_{itf}+C_{itb}+2C_{sg}+2C_{fr} << C_{oxf}$ was satisfied. It also indicates that *SS* increases linearly with increase in t_{oxf} and *T*. The reason for the smaller *SS* with larger P_{O2} listed in Table 2.1 is explained by equation (2.8) since the number of sub gap states, thus $2C_{sg}$, should be smaller when P_{O2} is larger. The measured *SS* in both Figs. 2.11 and 2.12 followed equation (2.8) when $C_{itf}+C_{itb}+2C_{sg}+2C_{fr}$ = 1.17×10^{-4} F/m^2, suggesting that equations (2.7) and (2.8) well explain the dependence on t_{oxf} and *T*. According to [61], the density of the states around E_f, which is located

near E_c, is $10^{17} \sim 10^{18}$ $cm^{-3}eV^{-1}$, thus $6 \times 10^{10} \sim 6 \times 10^{11}$ $cm^{-2}eV^{-1}$ when t_{ch} = 6 nm. If we assume that the value is similar in our a-InGaZnO film, $C_{itf}+C_{itb}+2C_{sg}$ is calculated to be $9.6\times10^{-5} \sim 9.6\times10^{-4}$ F/m^2 for t_{ch} = 6 nm, and thus, it is likely that $C_{itf}+C_{itb}+2C_{sg}$ accounts for a large portion of $C_{itf}+C_{itb}+2C_{sg}+2C_{fr}$.

In summary, equation (2.8) explains the experimental results; *SS* (a) increases with increase in t_{ch}, (b) increases with decrease in P_{O2}, (c) increases linearly with increase in t_{oxf}, and (d) increases linearly with increase in T.

Based on the experimental results and equation (2.8), to achieve an FD a-InGaZnO TFT with small *SS*, $N_e t_{ch}^2$ needs to be made sufficiently small to satisfy the condition for the FD mode operation. Furthermore, C_d and C_{oxf} need to be made large while C_{itf}, C_{itb}, C_{sg} and C_{fr} need to be made small, by annealing, to make *SS* even smaller.

2.6.2 I_{ds} and V_{th} of FD a-InGaZnO TFT

We need to consider the adequacy of applying the semiconductor theory to oxide TFTs to discuss I_{ds} and threshold voltage (V_{th}). For an n-type field effect transistor (FET), I_{ds} in linear region is described as equation (2.9), I_{ds} in saturation regions is described as equation (2.10) and V_{th} is described as equation (2.11) [62]

$$I_{ds} = \mu C_0 \frac{W}{L}\left(V_{gs} - V_{th}\right)V_{ds}, \tag{2.9}$$

$$I_{ds} = \frac{1}{2}\mu C_0 \frac{W}{L}\left(V_{gs} - V_{th}\right)^2, \tag{2.10}$$

$$V_{th} = V_{fb} + 2\phi_g + \frac{\sqrt{4\varepsilon_s q N_a \phi_g}}{C_0}, \tag{2.11}$$

Here, μ is the electron mobility, C_0 is the gate insulator capacitance per unit area, V_{fb} is the flat-band voltage, φ_g is the difference between the Fermi level and the intrinsic level, ε_s is the permittivity of the semiconductor and N_a is the acceptor charge per unit volume. Equations (2.9) to (2.11) are derived for FETs using inversion layer as a channel (most Si FETs). However, oxide TFTs are n-type FETs using an accumulation layer as a channel. Hence, we cannot use this set of equations for oxide TFTs.

Equations (2.9) and (2.10) are derived by performing an integral on right side of equation (2.12) from $V = 0$ to $V = V_{ds}$.

$$I_{ds} = \mu \frac{W}{L} \int_0^{V_{ds}} \{-Q_{ch}(V)\} dV . \tag{2.12}$$

Here, V is the voltage in source-to-drain direction at the channel, $Q_{ch}(V)$ is the electron charge in the channel per unit area. For inversion layer, $Q_{ch}(V)$ is described as

$$\begin{aligned} Q_{ch}(V) &= Q_s - Q_d \\ &= -C_0(V_{gs} - V_{fb} - \phi_s) + \sqrt{2\varepsilon_s q N_a (2\phi_g + V)} \\ &= -C_0(V_{gs} - V_{fb} - 2\phi_g - V) + \sqrt{2\varepsilon_s q N_a (2\phi_g + V)} \end{aligned} , \tag{2.13}$$

where $Q_s = -C_0(V_{gs}-V_{fb}-\varphi_s)$ is the total charge per unit area, $Q_d = -\{2\varepsilon_s q N_a(2\varphi_g+V)\}^{1/2}$ is the depletion charge per unit area, and φ_s is the surface potential.

To obtain equations for accumulation layer channel, we need to modify equation (2.13). For inversion channel, $\varphi_s = 2\varphi_g+V$, where $2\varphi_g$ is the potential that the inversion

layer start to appear (it is assumed that φ_s does not depend on V_{gs} while an inversion layer exists). For the accumulation channel, we modify it to $\varphi_s = V$ since an accumulation layer starts to appear when $\varphi_s = 0$ (it is also assumed that φ_s does not depend on V_{gs} while an accumulation layer exists). Also, we modify Q_d to 0 since a depletion layer does not exist when the accumulation layer does. Therefore, equation (2.13) is modified to

$$\begin{aligned} Q_{ch}(V) &= Q_s \\ &= -C_0(V_{gs} - V_{fb} - \phi_s). \\ &= -C_0(V_{gs} - V_{fb} - V) \end{aligned} \tag{2.14}$$

By placing equation (2.14) into equation (2.12), we obtain

$$I_{ds} = \mu C_0 \frac{W}{L}(V_{gs} - V_{fb})V_{ds} - \frac{V_{ds}^2}{2}. \tag{2.15}$$

When $V_{ds} << V_{gs}$-V_{fb} (linear region), equation (2.15) is rewritten as

$$I_{ds} = \mu C_0 \frac{W}{L}(V_{gs} - V_{fb})V_{ds}. \tag{2.16}$$

When $V_{ds} = V_{gs}$-V_{fb}, I_{ds} reaches a maximum (equation (2.17)) and it does not increase further when $V_{ds} > V_{gs}$-V_{fb} (saturation region).

$$I_{ds} = \frac{1}{2}\mu C_0 \frac{W}{L}(V_{gs} - V_{fb})^2. \tag{2.17}$$

If we define V_{th} as

$$V_{th} = V_{fb}, \tag{2.18}$$

equations (2.16) and (2.17) are described in the same manner as equations (2.9) and (2.10).

These results indicate that we can use equations (2.9), (2.10), and the idea of linear/saturation region as first-order approximation for designing or analyzing oxide TFT circuits; i.e., using a Si model for a simulation in the following chapters is a good approach. Furthermore, although the description of V_{th} is different from that of Si FETs, we can also derive V_{th} by extrapolating I_{ds}-V_{gs} curves, as in the same way as in the analysis of Si FET characteristics. These understandings are particularly important for designing and analyzing analogue circuits such as a rectifier.

However, to be precise, the above consideration is valid and equations (2.14)-(2.18) are good approximations when the number of the donors, i.e., number of oxygen vacancies in the case of oxide semiconductors, in the semiconductor layer is not very large. The accumulation layer disappears when the conduction band is flat. However, in n-type semiconductor, the channel is not yet cut off because electrons still exist. Electrons disappear when the band is bended upward throughout the semiconductor layer. Therefore, the channel is completely cut off when W_{dep} is equal to t_{ch}. When this condition is satisfied around the source, $V_{gs} = V_{th}$, $V = 0$ (source voltage), and $Q_{ch}(V) = 0$. Since $W_d = \{2\varepsilon_s(-\varphi_s+V)/(qN_d)\}^{1/2}$, we obtain $\varphi_s = -(qN_d t_{ch}^2)/(2\varepsilon_s)$, where N_d is the donor charge per unit volume. Also, $Q_d = qN_d W_{dep} = qN_d t_{ch}$. Therefore, equation (2.13) is modified to

$$
\begin{aligned}
Q_{\mathrm{ch}}(V) &= Q_{\mathrm{s}} - Q_{\mathrm{d}} \\
&= -C_0\left(V_{\mathrm{th}} - V_{\mathrm{fb}} - \phi_{\mathrm{s}}\right) - q N_{\mathrm{d}} t_{\mathrm{ch}} \\
&= -C_0\left(V_{\mathrm{th}} - V_{\mathrm{fb}} + \frac{q N_{\mathrm{d}} {t_{\mathrm{ch}}}^2}{2\varepsilon_{\mathrm{s}}}\right) - q N_{\mathrm{d}} t_{\mathrm{ch}} \\
&= -C_0\left(V_{\mathrm{th}} - V_{\mathrm{fb}} + \frac{q N_{\mathrm{d}} {t_{\mathrm{ch}}}^2}{2\varepsilon_{\mathrm{s}}} + \frac{q N_{\mathrm{d}} t_{\mathrm{ch}}}{C_0}\right)
\end{aligned}
\quad . \tag{2.19}
$$

Since $Q_{\mathrm{ch}}(0) = 0$, we obtain

$$
V_{\mathrm{th}} = V_{\mathrm{fb}} - \frac{q N_{\mathrm{d}} {t_{\mathrm{ch}}}^2}{2\varepsilon_{\mathrm{s}}} - \frac{q N_{\mathrm{d}} t_{\mathrm{ch}}}{C_0} . \tag{2.20}
$$

We believe that this is a precise description of V_{th} for oxide TFTs. It is understood that V_{th} shift to negative direction as N_{d} or t_{ch} increases. When N_{d} and t_{ch} is too large, oxide TFTs do not turn off. In our FD oxide TFTs, N_{d} and t_{ch} are designed to be sufficiently small.

It is difficult to describe donor-origin I_{ds} analytically when V_{gs} is between V_{th} and V_{fb}. However, it is easily derived when $V_{\mathrm{gs}} = V_{\mathrm{fb}}$ (no depletion or accumulation layer). In this situation, the channel is treated as a simple two-terminal resistance and I_{ds} is described as

$$
I_{\mathrm{ds}} = q N_{\mathrm{d}} \mu V_{\mathrm{ds}} t_{\mathrm{ch}} \frac{W}{L} . \tag{2.21}
$$

When $V_{\mathrm{gs}} > V_{\mathrm{fb}}$, I_{ds} is the sum of right side of equation (2.16) and (2.21) for linear

region (equation (2.22)) and that of equation (2.17) and (2.21) for saturation region (equation (2.23)).

$$I_{ds} = \mu C_0 \frac{W}{L}\left(V_{gs} - V_{fb}\right)V_{ds} + q N_d \mu V_{ds} t_{ch} \frac{W}{L}, \tag{2.22}$$

$$I_{ds} = \frac{1}{2}\mu C_0 \frac{W}{L}\left(V_{gs} - V_{fb}\right)^2 + q N_d \mu V_{ds} t_{ch} \frac{W}{L}. \tag{2.23}$$

We believe that these are precise descriptions of I_{ds} for oxide TFTs.

2.6.3 Operation frequency of FD a-InGaZnO TFT

Here, we discuss the maximum operation frequency (f_m) of the FD a-InGaZnO TFT. There are two finite times, T_d and T_c, that determine f_m. T_d is the time taken by the fastest electron injected from the source electrode to drift in the channel toward the drain electrode. T_c is the time taken for the capacitance between the gate and the channel to be charged. A signal cannot be transmitted before T_d because even the fastest electron cannot reach the drain electrode before T_d. The operation with the frequency between $1/(2T_d)$ and $1/(2T_c)$, where I_{ds} is not yet at a steady state, is called non-quasi-static operation [63]. The operation with the frequency lower than $1/(2T_c)$, where I_{ds} is already at a steady state, is called quasi-static operation. In non-quasi-static operation, the output voltage of a TFT is smaller than the expected voltage, i.e., V_{ds} in linear region and V_{ds}-V_{th} in saturation region, and it shrinks as the frequency increases. On the other hand, in quasi-static operation, the output voltage is the expected voltage and does not depend on the frequency.

When an FD a-InGaZnO TFT is turned on, electrons are injected from the source electrode to the channel and they drift toward the drain electrode due to the horizontal electric field generated by the effective horizontal voltage applied to the channel. The effective horizontal voltage is V_{ds} in linear region and V_{gs}-V_{th} in saturation region. Therefore, a TFT operating in the saturation region has a smaller effective horizontal voltage and determines f_m of a circuit when $V_{ds} = V_{gs} = V_{in}$, where V_{in} is an input voltage. T_d of a TFT operating in the saturation region is described as

$$T_d \sim \frac{L}{\mu(V_{gs} - V_{th})/L} = \frac{L^2}{\mu(V_{gs} - V_{th})}. \tag{2.24}$$

Therefore, f_m for non-quasi-static operation (f_{mnqs}) is

$$f_{mnqs} = \frac{1}{2T_d} \sim \frac{\mu(V_{gs} - V_{th})}{2L^2}. \tag{2.25}$$

Quasi-static operation is analyzed as follows. Since overlap lengths between the gate electrode and the source/drain electrodes (OL) are comparable to L in bottom-gate/top-contact structure, the TFT structure used for a circuit in this study, a TFT's gate-source capacitance (C_{gs}) cannot be ignored. Therefore, T_c is the time to draw out the electrons charged at both the gate-channel capacitance (C_{gc}) and C_{gs} to the drain electrode. The total capacitance is

$$C_{gs} + C_{gc} = \frac{\varepsilon_{SiO2}\varepsilon_0}{t_{oxf}} W(L + OL), \tag{2.25}$$

where ε_{sio2} is the relative permittivity of SiO_2.

In the AC circuit theory, f_m for quasi-static operation, i.e. the unity-gain frequency ($f_{mqs} = 1/(2T_c)$), is described as a frequency where the gain of the transistor is equal to 1. Here, the gain is defined as the ratio between the output current and the input current. In FETs, input current is the gate current (I_g) and output current is I_{ds}. They are described as

$$I_g = j\omega(C_{gs} + C_{gc})V_{gs} = j2\pi f(C_{gs} + C_{gc})V_{gs}, \tag{2.27}$$

$$I_{ds} = g_m V_{gs}, \tag{2.28}$$

where j is the imaginary unit, ω is angular rate, f is frequency, and g_m is the transconductance. In saturation region,

$$g_m = \frac{\partial I_{ds}}{\partial V_{gs}} = \frac{\mu \varepsilon_{SiO2} \varepsilon_0}{t_{oxf}} \frac{W}{L}(V_{gs} - V_{th}), \tag{2.29}$$

therefore,

$$\begin{aligned} \frac{|\Delta I_{ds}|}{|\Delta I_g|} &= \frac{g_m \Delta V_{gs}}{2\pi f(C_{gs} + C_{gc})\Delta V_{gs}} \\ &= \frac{\frac{\mu \varepsilon_{SiO2} \varepsilon_0}{t_{oxf}} \frac{W}{L}(V_{gs} - V_{th})}{2\pi f \frac{\varepsilon_{SiO2} \varepsilon_0}{t_{oxf}} W(L + OL)}, \\ &= \frac{\mu(V_{gs} - V_{th})}{2\pi f L(L + OL)} \end{aligned} \tag{2.30}$$

Since $f = f_{mqs}$ when $|\Delta I_{ds}|/|\Delta I_g| = 1$,

$$f_{mqs} = \frac{\mu(V_{gs} - V_{th})}{2\pi L(L + OL)}. \tag{2.31}$$

We estimated f_{mqs} for several cases by using equation (2.31) as shown in Fig. 2.16. For the a-InGaZnO TFTs fabricated on a flexible sheet substrate, the minimum value for L and OL would be around 1 μm due to the process technology for large area and flexible substrates. If we use 1 μm process and 10 V is supplied as V_{in}, μ around 0.2 cm^2/Vs is necessary for achieving 13.56-MHz operation, around 15 cm^2/Vs is necessary for 900-MHz operation, and around 40 cm^2/Vs is necessary for 2.45-GHz operation; 13.56-MHz, 900-MHz and 2.45-GHz bands are widely used in existing wireless applications. When 20 V is supplied for V_{in}, 0.1 cm^2/Vs is necessary for 13.56-Hz operation, 7 cm^2/Vs is necessary for 900-MHz operation, and 20 cm^2/Vs is necessary for 2.45-GHz operation.

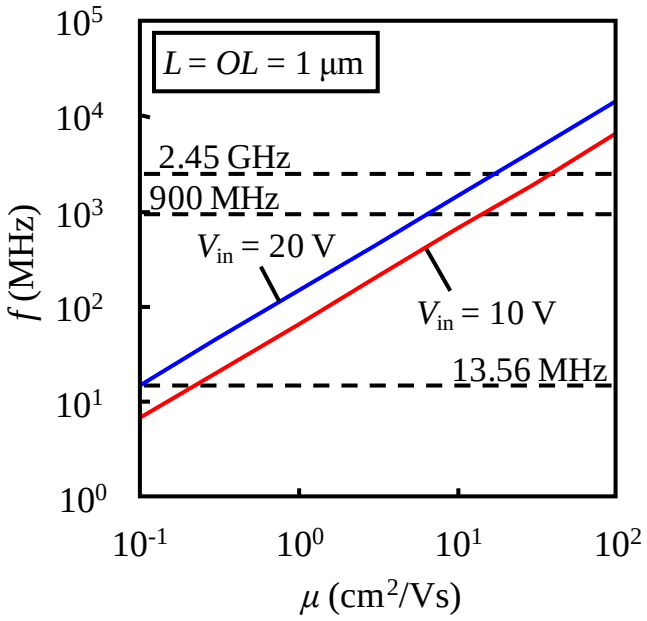


Fig. 2.16 Calculated maximum operation frequency of FD a-InGaZnO TFT.

Chapter 3

Development of four-TFT rectifier circuit

3.1 Issues in conventional rectifier circuits

In the case of wirelessly transmitting signals and power, a rectifier is required for converting alternating current (AC) into direct-current (DC). Although one can design a rectifier by using p-n or Schottky diodes [64], we did not choose these devices in this study since they require additional fabrication steps and materials, which increase manufacturing cost of an oxide TFT circuit. Rectifiers constructed from oxide TFTs have been reported [65, 66]. However, wireless input with HF (13.56-MHz) band and higher frequencies has not been rectified yet. This is required since HF band and higher frequencies can transmit signals and power over a distance and can deal with large-volume information. Furthermore, DC output voltage and power of a rectifier must be larger than a voltage and power required for driving logic circuits on the oxide RFID (~ 5 V and ~2 mW). Therefore, in this study we focused on a full-wave rectifier rather than a half-wave rectifier [67].

In this chapter, a full-wave rectifier achieving the above requirements by using amorphous a-InGaZnO TFTs will be explained. The FD a-InGaZnO TFTs were used here in anticipation of fabricating a low-power-consumption logic circuits together with the rectifier.

3.2 Designing of four-TFT rectifier circuit

3.2.1 Circuit configuration

A circuit diagram of fabricated four-TFT full-wave rectifier is shown in Fig. 3.1. TFT1 and TFT2 act as switches, TFT3 and TFT4 act as diodes, C_1 (= 200 pF) acts as a voltage smoothing capacitor, and R_1 represents subsequent circuits (we assumed it as 2 Mohm). Upper and lower halves are mirror symmetrical with respect to horizontal plane. LA and LB are input terminals, OUTP is an output terminal for positive voltage, and OUTN is an output terminal for negative voltage. When the antenna coil connected to LA and LB receives wireless input, the differential AC voltage is generated and applied to LA and LB; the AC voltages at LA (V_{LA}) and LB (V_{LB}) are described as $V_{LA} = V_{in}\sin(2\pi ft)$ and $V_{LB} = -V_{in}\sin(2\pi ft)$, where t is time here. The arrows indicate the current path when a positive voltage is applied to LA and a negative voltage is applied to LB.

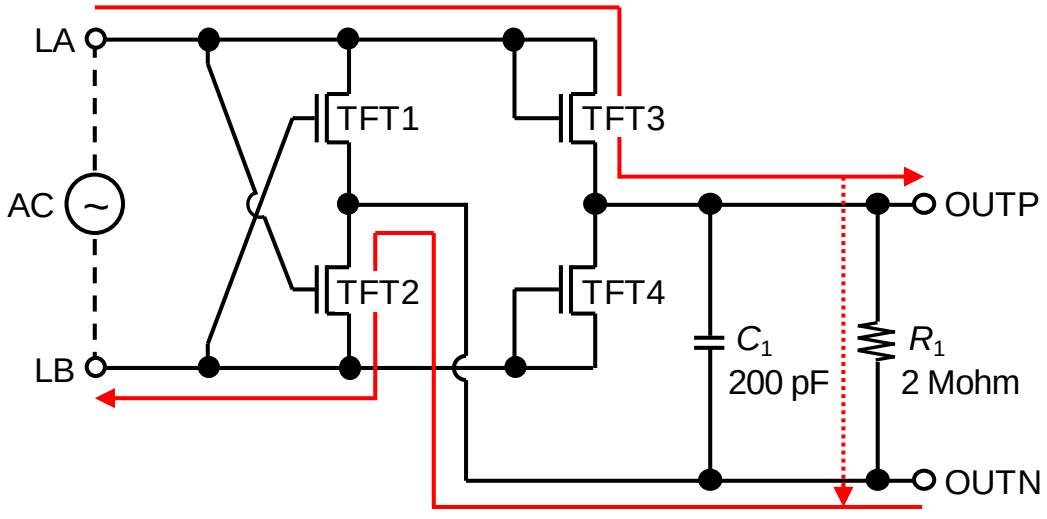


Fig. 3.1 Schematic view of four-TFT rectifier. C_1 is smoothing capacitor and R_1 is load resistance.

TFT1 and TFT2 are switch connected and rectify negative inputs. When V_{in} is applied to LA and $-V_{in}$ is applied to LB, TFT2 turns on and LB is connected to OUTN. Therefore, the voltage at OUTN (V_{outn}) is $-V_{in}$. The voltage drop across the drain-to-source of TFT2 is small since it operates in the linear region; i.e., V_{gs} is always larger than V_{ds}. On the other hand, LA is disconnected from OUTN since TFT1 is turned off.

TFT3 and TFT4 are diode connected, i.e. the gate is connected to the drain, and rectify a positive input. They turn on and operate in the saturation region when a voltage larger than V_{th} is applied as V_{gs} and V_{ds}. This means that they have a larger voltage drop ($= V_{th}$) than the switch connected TFTs. When V_{in} ($> V_{th}$) is applied to LA, TFT3 turns on and LA is connected to OUTP. The voltage at OUTP (V_{outp}) is V_{in}-V_{th}. On the other hand, LB is disconnected from OUTP since TFT4 is turned off.

3.2.2 Simulation

A circuit simulation was conducted before making photo masks in the circuit designing step. We used SmartSpice from Silvaco for the circuit simulator and the model for the pc-Si TFT (LEVEL 36) since there was no model for oxide TFTs in SmartSpice. The model was modified to fit with characteristics of a fabricated a-InGaZnO TFT. Virtuso from Cadence was used for the mask layout and 5 layers of masks were made; gate layer (M1), channel layer, source/drain layer (M2), contact hole between M1 and M2, and contact hole for pads.

A pc-Si TFT shows larger μ and I_{ds} compared to an a-InGaZnO TFT. Furthermore, V_{th} of a pc-Si TFT and V_{th} of an a-InGaZnO TFT are not the same. Taking account of these two points, the parameters relating to μ and V_{th} were adjusted to fit the calculated I_{ds}-V_{gs}

curves to measured I_{ds}-V_{gs} curves. We could manage to make the difference of I_{ds} between simulation and measurement to less than 10% as shown in Fig. 3.2.

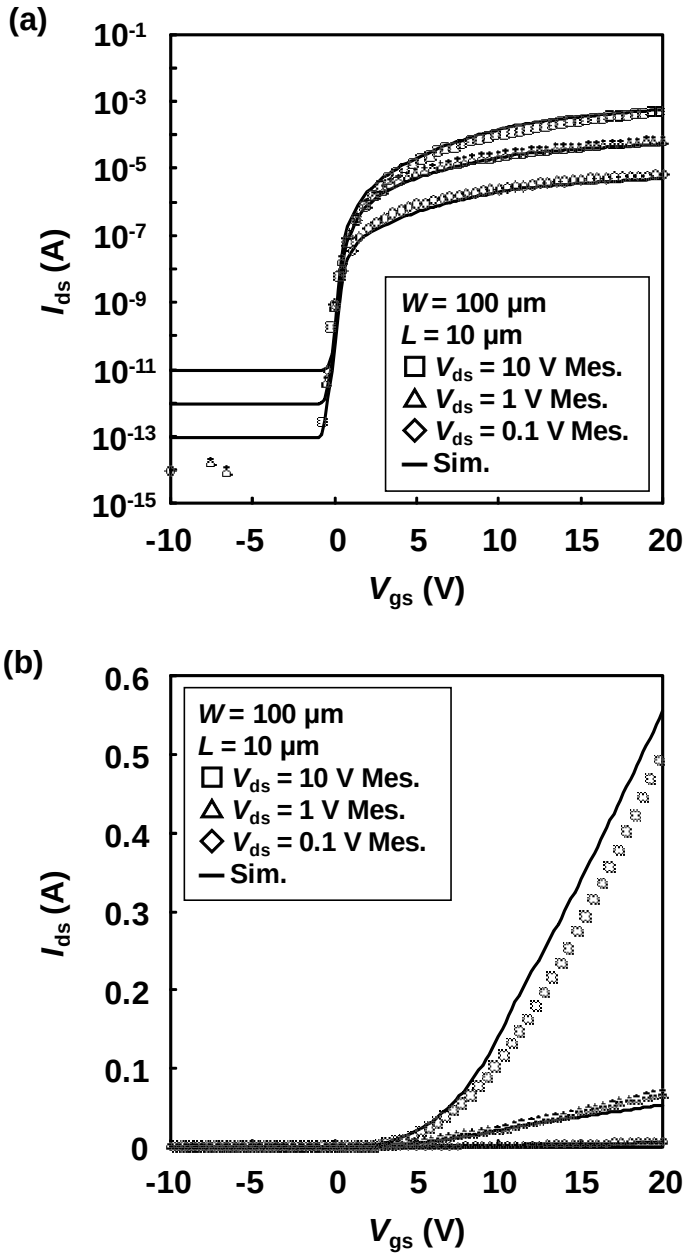


Fig. 3.2 Measured and simulated I_{ds}-V_{gs} curves; (a) log scale and (b) linear scale.

We performed a circuit simulation of the four-TFT rectifier using this modified TFT model. 13.56-MHz input was rectified and DC voltages were obtained for V_{outp} and V_{outn} as shown in Fig. 3.3. The output voltages were time-averaged (smoothed) by C_1, and therefore, the values were around $2/\pi$ of the peak value; $V_{outp} \sim (2/\pi)(V_{in}-V_{th})$ and $V_{outn} \sim -(2/\pi)V_{in}$.

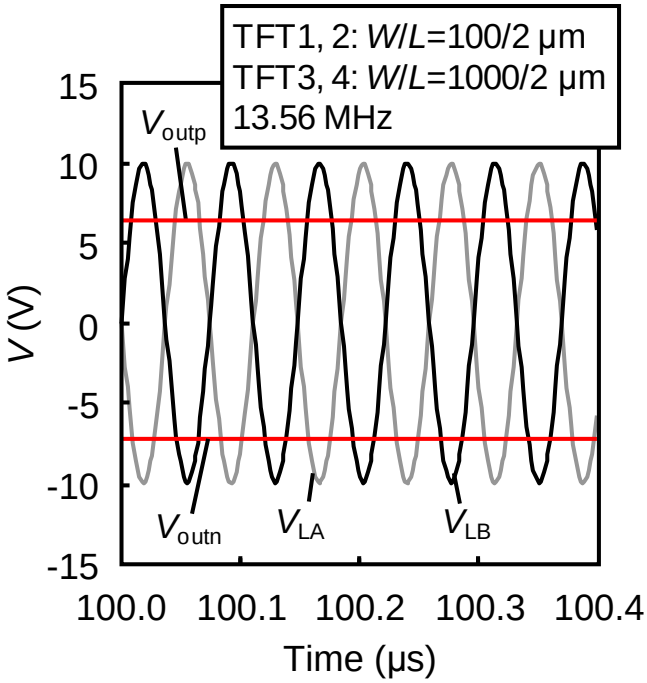


Fig. 3.3 Simulated full-wave rectifying characteristics of four-TFT a-InGaZnO rectifier for 13.56-MHz input.

3.2.3 Redesigning of FD a-InGaZnO TFT and its fabrication process for circuit application

We redesigned FD a-InGaZnO TFT and its fabrication process for circuit application. The TFTs were fabricated on a glass substrate and their structure was modified to the bottom-gate/top-contact type structure shown in Fig. 3.4. The fabrication process is as follows.

Gate electrode formation:

a 70-nm thick Mo layer was deposited on a glass substrate by electron beam evaporation and then patterned by dry etching.

Gate insulator formation:

a 100-nm thick SiO_2 layer was deposited at 300^{o}C by plasma enhanced chemical vapor deposition (we used SiO_2 deposited at a high temperature in this work to study a feasibility of the rectifier).

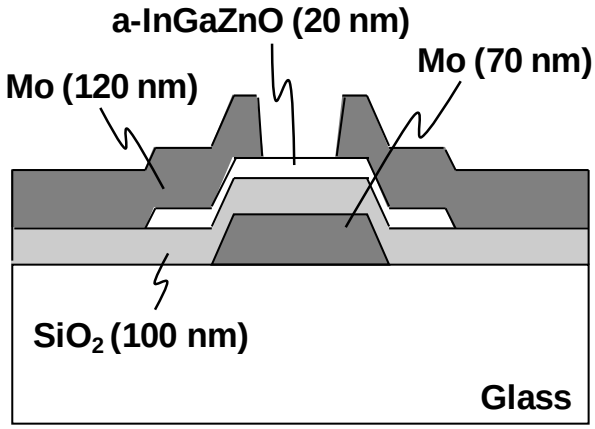


Fig. 3.4 Schematic cross-section of bottom-gate/top-contact FD a-InGaZnO TFT for circuit application.

Channel layer formation:

a 20-nm thick a-InGaZnO layer was deposited by RF magnetron sputtering at room temperature and then patterned by wet etching.

Contact hole formation:

SiO_2 layer was wet etched.

Source/drain electrode formation:

a 120-nm thick Mo layer was deposited by electron beam evaporation and then patterned by dry etching.

Annealing:

a fabricated TFT was annealed at 125^{o}C in dry air.

The cross-sectional transmission electron micrograph of a part of a fabricated a-InGaZnO TFT is shown in Fig. 3.5. The 20-nm InGaZnO remained amorphous even after the fabrication processes. A top view of a fabricated four-TFT a-InGaZnO rectifier is shown in Fig. 3.6. *L* of all four TFTs is 2 μm, *W* of TFT1 and TFT2 is 100 μm, that of TFT3 and TFT4 is 1000 μm, and *OL* of all four TFTs is 2 μm.

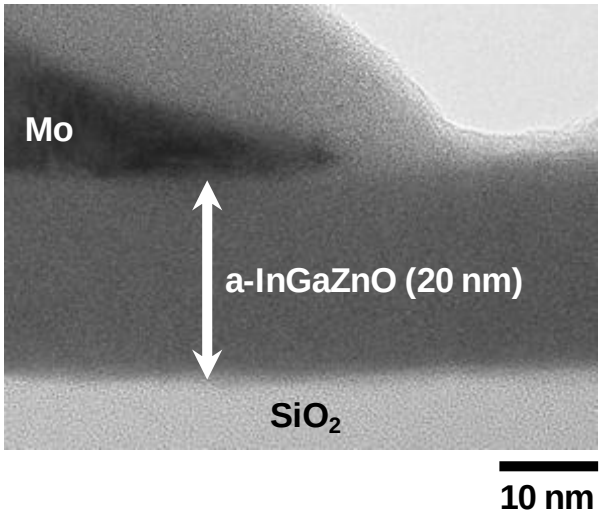


Fig. 3.5 Cross-sectional transmission electron micrograph of a-InGaZnO TFT.

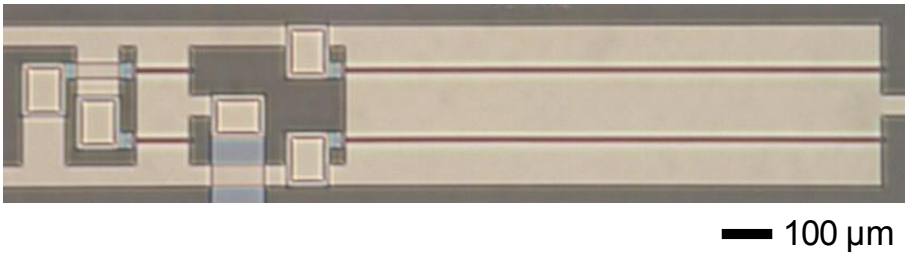


Fig. 3.6 Top view of fabricated four-TFT a-InGaZnO rectifier.

3.3 Electrical characteristics of fabricated four-TFT rectifier circuit

3.3.1 Characteristics of TFT

The transfer characteristics of a fabricated a-InGaZnO TFT are shown in Fig. 3.7. The TFT had field effect mobility (μ_{fe}) of 15.1 cm^2/Vs, I_{off} of $< 10^{-15}$ A/μm, *SS* of 160 mV/decade, on/off ratio of $> 10^{10}$. The small I_{off} and the small *SS* were obtained due to the FD structure. I_{on} was as high as the value expected from μ_{fe}. As shown in Fig. 3.8, the static characteristic had no kink effect.

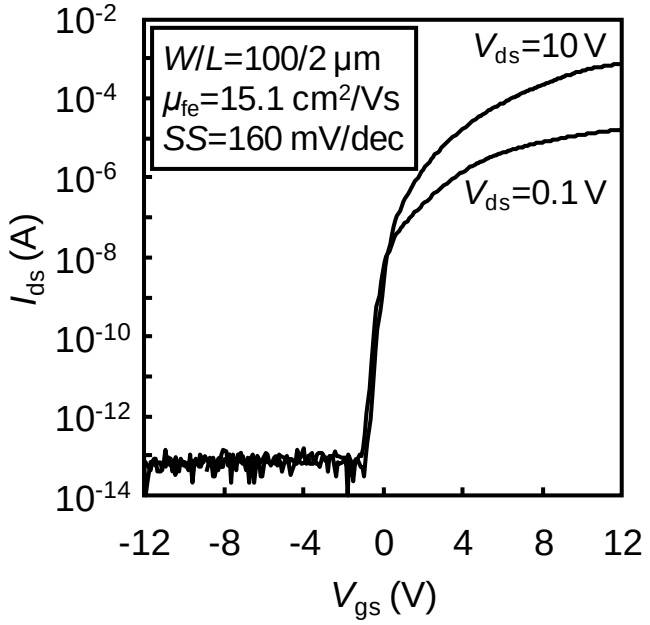


Fig. 3.7 Transfer characteristic of fabricated a-InGaZnO TFT.

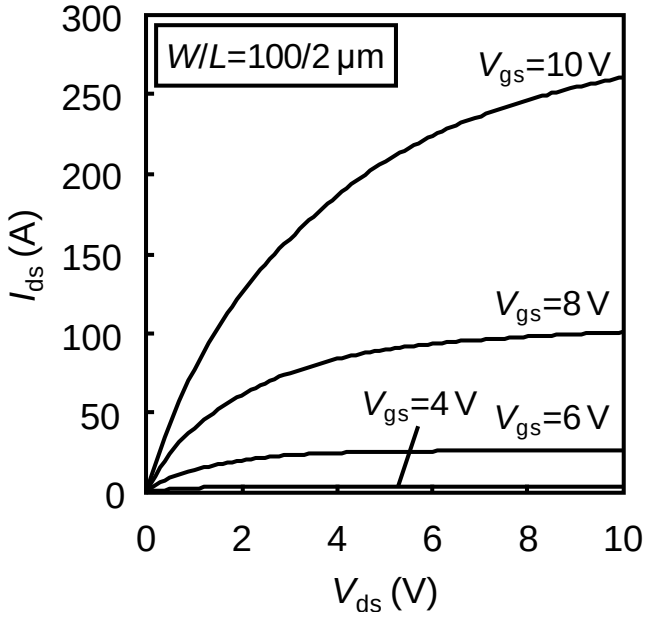


Fig. 3.8 Static characteristic of fabricated a-InGaZnO TFT.

3.3.2 Comparison with simulation

In the wired measurement, a rectifier was driven by AC voltages from a pulse generator. The AC voltages are inputted into LA and LB of the rectifier. The waveforms obtained when V_{in} was 10 V (i.e., 20-V peak to peak) and f was 13.56 MHz are plotted in Fig. 3.9. DC voltages with small ripples were obtained for V_{outp} and V_{outn}. A differential between the two output voltages, V_{outp}-V_{outn} ~ 13 V, is the voltage supplied to subsequent circuits. $|V_{outp}|$ had an 8% (0.5 V) smaller value than the simulation while $|V_{outn}|$ had almost the same value (see Fig. 3.3). We presume that the difference is due to small differences in V_{th} and I_{ds} between an actual TFT and a TFT in the simulation.

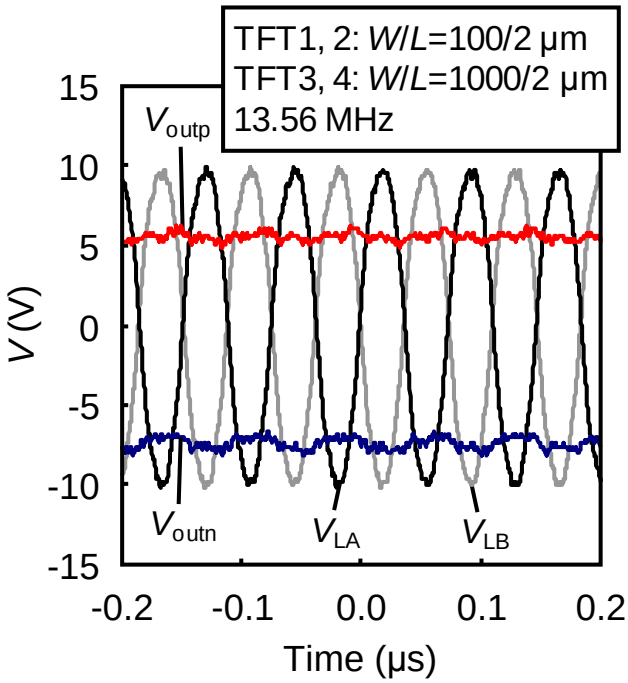


Fig. 3.9 Measured full-wave rectifying characteristics of four-TFT a-InGaZnO rectifier for 13.56-MHz wired input.

3.3.3 Dependence on input voltage

The dependence of V_{outp} and $|V_{outn}|$, which are time averaged over the ripples, on V_{in} is shown in Fig. 3.10. V_{outp} was around $(2/\pi)(V_{in}-V_{th})$ (V_{th} of the TFT was ~2 V) and $|V_{outn}|$ was around $(2/\pi)V_{in}$ as explained in the previous section.

3.3.4 Dependence on input frequency

The dependences of time-averaged values of V_{outp} and V_{outn} on f are shown in Fig. 3.11. Both V_{outp} and V_{outn} had peak values at around 0.1 MHz when C_1 = 200 pF. C_1 did not work as a smoothing capacitor when f was lower than 0.1 MHz presumably because the cutoff frequency of the RC circuit is around 0.1 MHz.

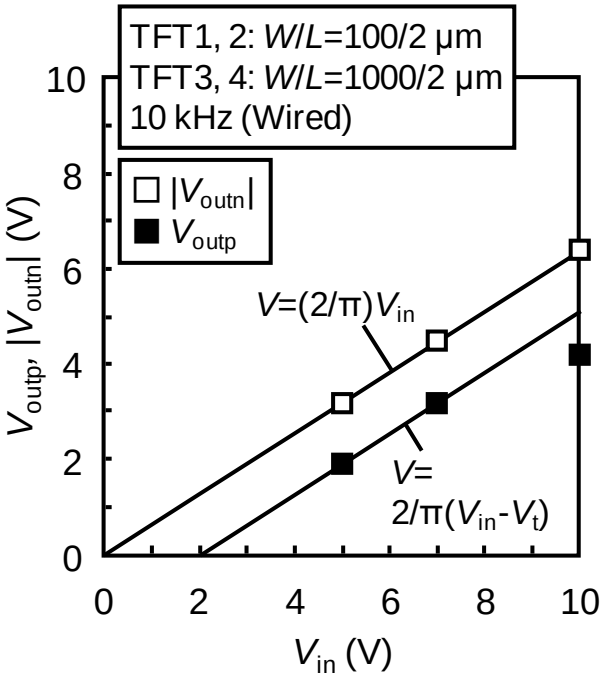


Fig. 3.10 Positive and negative output voltage dependences of four-TFT a-InGaZnO rectifier on input amplitude.

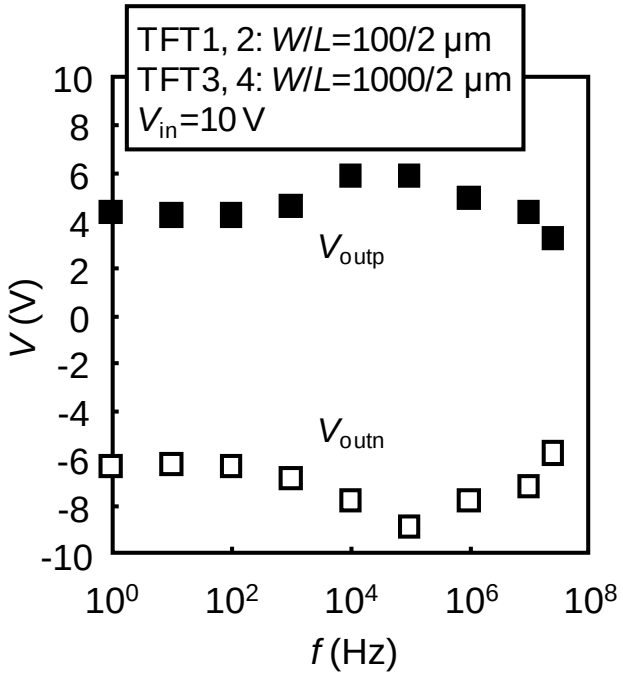


Fig. 3.11 Positive and negative output voltage dependences of four-TFT a-InGaZnO rectifier on input frequency.

3.3.5 Wireless operation and dependence on power transmission distance

The experimental setup for measuring wireless voltage rectification is shown in Fig. 3.12. The a-InGaZnO rectifier was connected to a resonance capacitor (C_2), a 3-turn antenna coil, C_1 and R_1. We used a commercial RFID reader with input power of 200 mW and the AC frequency of 13.56 MHz. We varied the distance between the antenna coil and the reader (d). Measured wireless rectifying characteristics at d = 60 mm are shown in Fig. 3.13. For V_{outp}, the obtained waveforms agreed well with those of the wired measurement. However, V_{outn} was not obtained (the reason will be discussed later). The dependences of V_{in} and V_{outp} on d are shown in Fig. 3.14. V_{in} and

V_{outp} had the maximum values (18 V and 12 V, respectively) when d was around 30 mm. V_{outp} was lager than 5 V when d was 5-65 mm; i.e, circuits on the oxide RFID can be operated in this distance range. The generated power was around 70 μW at this distance range. We will discuss this dependence on the distance later.

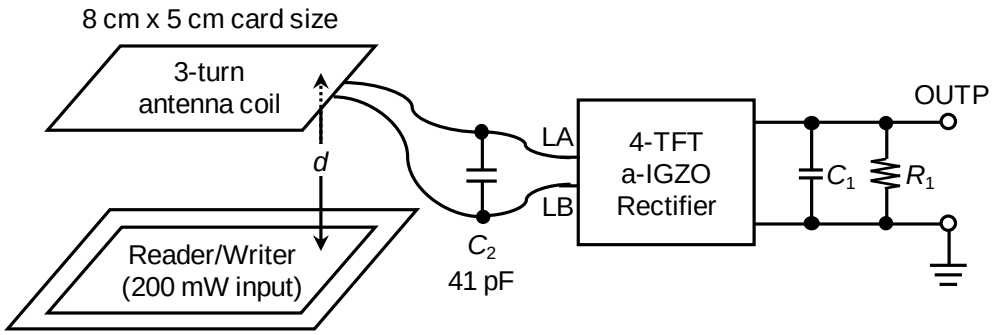


Fig. 3.12 Experimental setup for measuring wireless voltage rectification. C_1 is smoothing capacitor, C_2 is resonance capacitor and R_1 is load resistance.

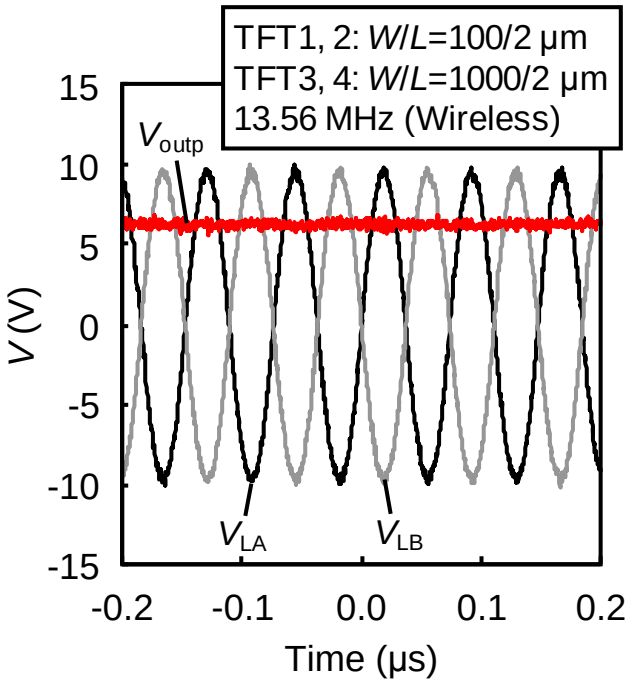


Fig. 3.13 Measured full-wave rectifying characteristics of four-TFT a-InGaZnO rectifier for 13.56-MHz wireless input.

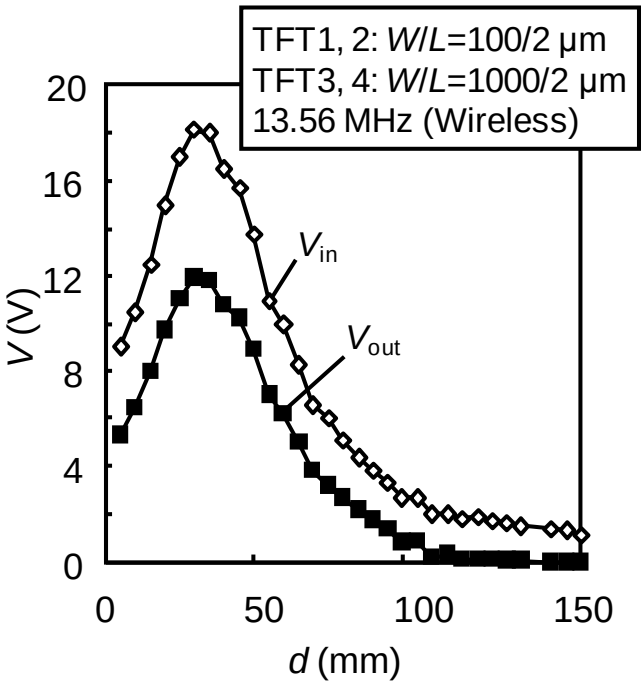


Fig. 3.14 Dependence of input amplitude and output voltage on distance between antenna coil and reader.

3.4 Discussion

3.4.1 Output voltage

To avoid degrading output voltage of the rectifier, leakage current of TFTs must be small enough. If the leakage current at TFT1 (see Fig 3.1) is not small enough, the absolute value of V_{outn} decreases. Therefore, TFT1 must have small I_{ds} when V_{gs} is 0 V and V_{ds} is $2V_{in}$; note that $-V_{in}$ is applied to LB and the gate of TFT1, V_{in} is applied to LA, and V_{outn} is $-V_{in}$. On the other hand, if the leakage current at TFT4 is not small enough, V_{outp} decreases. Therefore, TFT4 must have small I_{ds} when V_{gs} is 0 V and V_{ds} is $2V_{in}$-V_{th}, likewise TFT1; note that $-V_{in}$ is applied to LB and the gate of TFT4, and V_{outp} is V_{in}-V_{th}.

As shown in Fig. 3.7, a FD a-InGaZnO TFT has a leakage current smaller than 50 pA/μm at V_{gs} = 0 V (this value does not depend on V_{ds} since this is subthreshold current). Therefore, a channel resistance at V_{gs} = 0 V of TFT1 (W = 100 μm) is larger than 4 Gohm (= V_{ds}/I_{ds} = 20 V/5 nA), and that of TFT4 (W = 1000 μm) is larger than 400 Mohm. Since these values are over 200 times larger than the load resistance, namely resistance of subsequent circuits, the degradation of V_{outp} and V_{outn} due to the leakage current can be ignored.

3.4.2 Operation frequency

Here, we discuss f_m of the oxide TFT rectifier. As mentioned in chapter 2, there are two finite times, T_d and T_c, that determine f_m. The operation with the frequency between $1/(2T_d)$ and $1/(2T_c)$, where I_{ds} is not yet at a steady state, is called non-quasi-static operation [63]. The operation with frequency lower than $1/(2T_c)$, where I_{ds} is already at a steady state, is called quasi-static operation.

It is calculated from equation (2.25) as $T_d \sim 330$ ps for the FD a-InGaZnO TFT used

in this study by substituting L = 2 μm, μ_{fe} = 15 cm^2/Vs, V_{gs} = V_{in} = 10 V, and V_{th} = 2 V. Therefore, f_{mnqs} is ~1.5 GHz. It is also calculated from equation (2.31) as f_{mqs} = 240 MHz since OL = 2 μm. Therefore, our rectifier can rectify up to ~1.5 GHz in non-quasi-static operation and up to 240 MHz in quasi-static operation. As the experimental results show, this is sufficient for 13.56-MHz operation.

3.4.3 Reason for non-full-wave rectification in wireless operation

V_{outn} was not obtained in Fig. 3.13 as already explained. We analyzed the reason and found out that the gate insulators of TFT1 and TFT2 have broken down. This is because a large AC voltage was applied between the gate electrode and the channel of those TFTs. The AC voltage is the voltage applied between LA and LB (= $2V_{in}$) and the maximum value of V_{in} was 18 V as shown in Fig. 3.13. Therefore, 36-V AC voltage oscillating at 13.56 MHz was applied between the gate electrode and the channel of TFT1 and TFT2. To avoid the brake down of the gate insulator, the rectifier needs to be equipped with a circuit to regulate V_{in}. Otherwise, we should use a half-wave rectifier (only TFT3 and TFT4) with accepting the output power decreasing by half.

3.4.4 Distance dependence in wireless operation

As mentioned above, V_{in} and V_{outp} took peak values when d was around 30 mm and they decreased with increase in d when d was larger than 30 mm. This dependence results from a mixture of two phenomena.

The first phenomenon is the decrease of the coupling factor (κ) between the two coils, the one on the reader side and the one on the RFID side, with the increase in d. When κ is 1, 100% of the magnetic flux generated by the reader coil passes through the RFID coil. On the other hand, when κ is 0, 0% of the magnetic flux generated by the reader

coil passes through the RFID coil. Therefore, the power transmission efficiency decreases with the increase in d. κ depends not only the distance between the two coils but also on the size, shape and number of turns in the coils and the angle between the two coils.

The other phenomenon is the variation of the resonant frequency (f_r) of the two LC circuits; one is the reader coil with the internal capacitor (C_{reader}) and the other is the 3-turn antenna coil with C_2 in Fig. 3.12. When the two coils are coupled to each other, f_r of the two coils are written as follows;

$$f_{r1} = \frac{1}{2\pi\sqrt{(L_1 + M)C_{reader}}}, \tag{3.1}$$

$$f_{r2} = \frac{1}{2\pi\sqrt{(L_2 + M)C_2}}, \tag{3.2}$$

where subscript 1 denotes reader side, subscript 2 denotes RFID side and L is inductance. M is mutual inductance between the two coils and it is written as follows;

$$M = \kappa\sqrt{L_1 L_2}. \tag{3.3}$$

Therefore, when κ is large, thus M is large, f_{r1} and f_{r2} vary largely from the target

frequency (13.56 MHz in our case) and the power transmission efficiency decreases. Since κ is large when d is small, as mentioned above, the efficiency degrades as d decreases.

The situation as a result of the two phenomena is schematically shown in Fig. 3.15 (note that this is not an accurate calculation). The heights of the curves decrease as d increases due to the decrease in κ. When $d = 0$, $f_r \sim 11.5$ MHz and hence the efficiency at 13.56 MHz is around 30%. When d takes a medium value, $f_r \sim 12.5$ MHz and the efficiency at 13.56 MHz takes the maximum value of around 45%. When d takes a large value, $f_r \sim 15$ MHz and the efficiency at 13.56 MHz takes a low value of around 8%.

In summary, V_{in} and V_{outp} take peak values at a certain d as a result of two phenomena; (1) the power transmission efficiency decreases as d increases since κ decreases, and (2) the power transmission efficiency decreases as d decreases since f_r departs from 13.56 MHz.

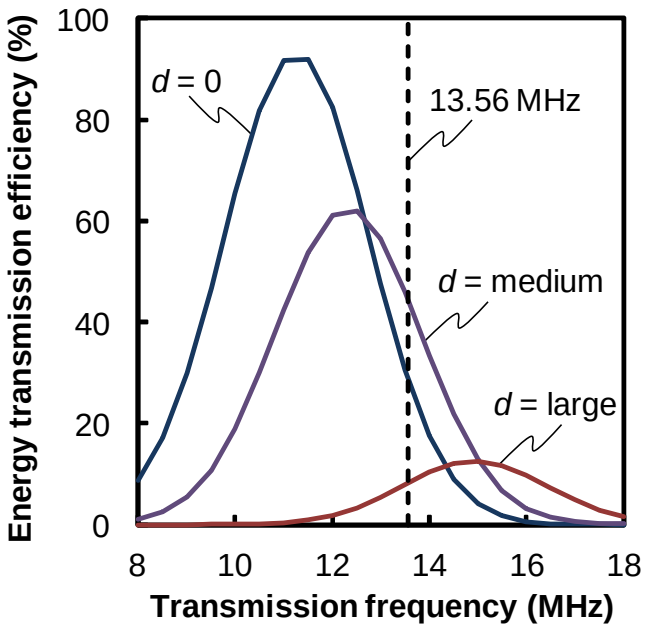


Fig. 3.15 Schematic view of dependence of energy transmission efficiency on transmission frequency and distance (d) between two coils.

Chapter 4

Development of low-power operating logic circuit

4.1 Issues in conventional logic gates

4.1.1 Requirements for logic circuits

The a-InGaZnO RFID needs to adapt to the existing infrastructure, namely a reader terminal conformable to ISO15693. The reader terminal can send 4 W at maximum and it can read the signal from the RFID when the frequency is higher than ~1 kHz.

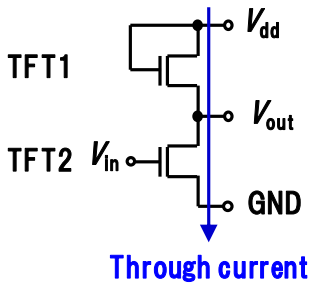
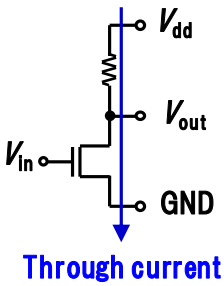
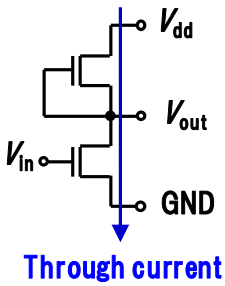
With the conversion efficiency of a-InGaZnO TFT rectifier discussed in the previous chapter, 1.4 mW can be generated at maximum. For an RFID using a-InGaZnO TFT, logic circuit part consist of around 500 logic gates and thus the consumption power of a logic gate needs to be smaller than 2.8 μW. Therefore a logic gate needs to be operated at a frequency higher than 1 kHz with consumption power lower than 2.8 μW.

Though CMOS inverter is used in LSIs consist of bulk silicon transistors, it can not be used in oxide-TFT circuits since there are no high performance pMOS transistors at present. Since a-InGaZnO TFT is an nMOS TFT, logic gates need to be formed by using only nMOS TFTs. Unlike silicon, it is not easy to control precisely the resistivity of a part of an a-InGaZnO film on a substrate or V_t of selected a-InGaZnO TFTs on a substrate. Although it is known that the resistivity can be lowered or the V_t can be shifted toward negative direction by using proton implantation [37], the process is expensive and hence it is not appropriate to adopt such an option for RFID application. Therefore, we need to form a logic circuit by using nMOS inverters that uses the

a-InGaZnO films with identical resistivity or V_t for the load and the drive TFTs. There are three types of such nMOS inverters that are already known; diode-connected type inverter, resistance-load type inverter and active-load type inverter (Table 4.1).

In this study, we first fabricated ring oscillators using diode-connected type inverters and their consumption power and operation frequency were measured. By using this result, we then estimated the consumption power and operation frequency of ring oscillators using resistance-load type and active-load type inverters. Since all three types of ring oscillators did not satisfy the requirements, we proposed a novel type of inverter and ring oscillator.

Table 4.1. Conventional logic gates.

Type	Diode-connected	Resistance-load	Active-load
Circuit diagram			
Issue	Large consumption current	Low operation frequency	Low operation frequency

4.1.2 Fabrication of ring oscillator using diode connected-type inverter

Ring oscillator is a circuit connecting odd number of inverters in series. The output of the *n*th stage inverter is inputted into (*n*+1)th stage and the output of the last stage is

inputted into the first stage. During the operation, the logical negation of the input into the first stage is outputted from the last stage after some finite delay time. This signal is inputted into the first stage and hence the input and output of all inverters oscillate. 5-stage ring oscillators consist of diode connected type inverters shown in Fig. 4.1 were fabricated in this study.

A simulation was conducted with SmartSpice before fabricating the 5-stage ring oscillator. Fig. 4.2 is the result when the channel width of the drive-TFT (W_{drive}) is 100 μm, the channel width of the load-TFT (W_{load}) is 10 μm and L of the both TFTs are 10 μm. The delay time for 1-stage (T_{delay}) and the oscillation frequency (f = 1/(2 x T_{delay} x 5-stage)) are plotted versus supply voltage (V_{dd}).

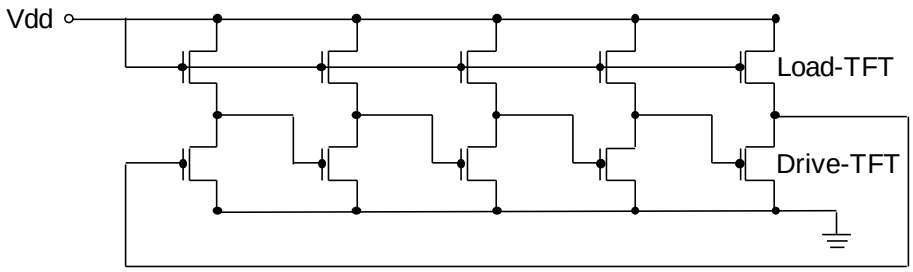


Fig. 4.1 Circuit diagram of 5-stage ring oscillator consist of diode connected type inverters.

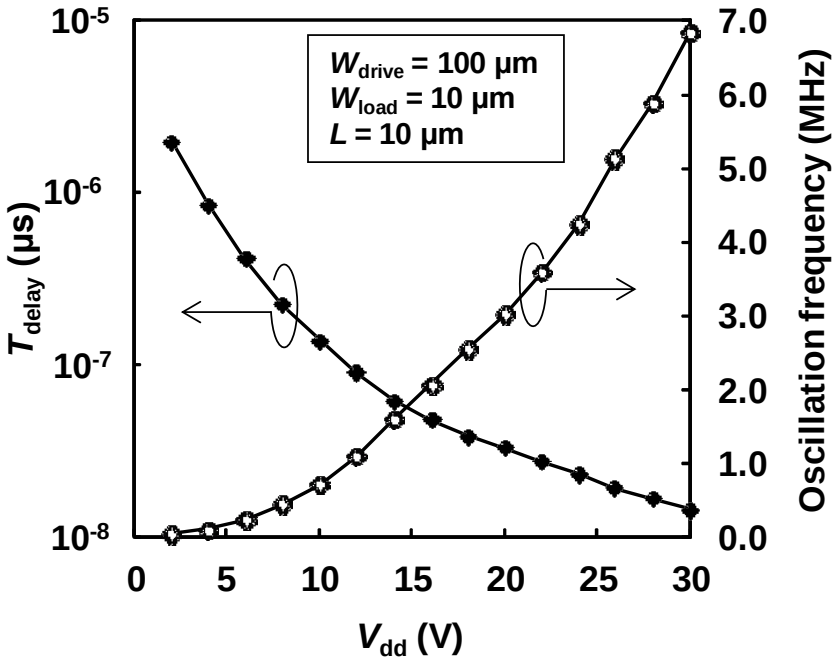


Fig. 4.2 Simulated T_{delay} and oscillation frequency of 5-stage ring oscillator consist of diode connected type inverters.

In case of diode connected type inverter, if W_{drive} and W_{load} were not designed properly, the gain (V_{out}/V_{in}) is small and the ring oscillator does not oscillate. However, as shown in Fig. 4.2, it showed an oscillation when W_{drive}/W_{load} was around 10. Furthermore, T_{delay} decreased and the oscillation frequency increased with the increase in V_{dd}. Using these results, 5 types of ring oscillators with W_{drive}/W_{load} = 100/1, 100/3, 100/10, 100/30, 100/50 μm were fabricated.

DC characteristics of the diode-connected type inverters were shown in Fig. 4.3. V_{dd} was fixed at 15 V and V_{in} was swept from -15 V to 20 V. On/off characteristics was steeper when W_{load} was small and the gain was large (G_{max} in the figure is the maximum gain with each inverters). V_{out} is derived from multiplying V_{dd} by a ratio of the channel

resistance of the drive-TFT (R_{drive}) and the sum of R_{drive} and the channel resistance of the load-TFT (R_{load}) as shown by equation (4.1).

$$V_{out} = \frac{V_{dd} R_{drive}}{R_{load} + R_{drive}} . \tag{4.1}$$

When V_{in} is "low," R_{load} is small enough compared to R_{drive} and thus $V_{out} = V_{dd}$ regardless of W_{drive}/W_{load}. On the other hand, when V_{in} is "high," R_{drive}/R_{load} decreases with increase in W_{drive}/W_{load} and therefore, V_{out} decreases.

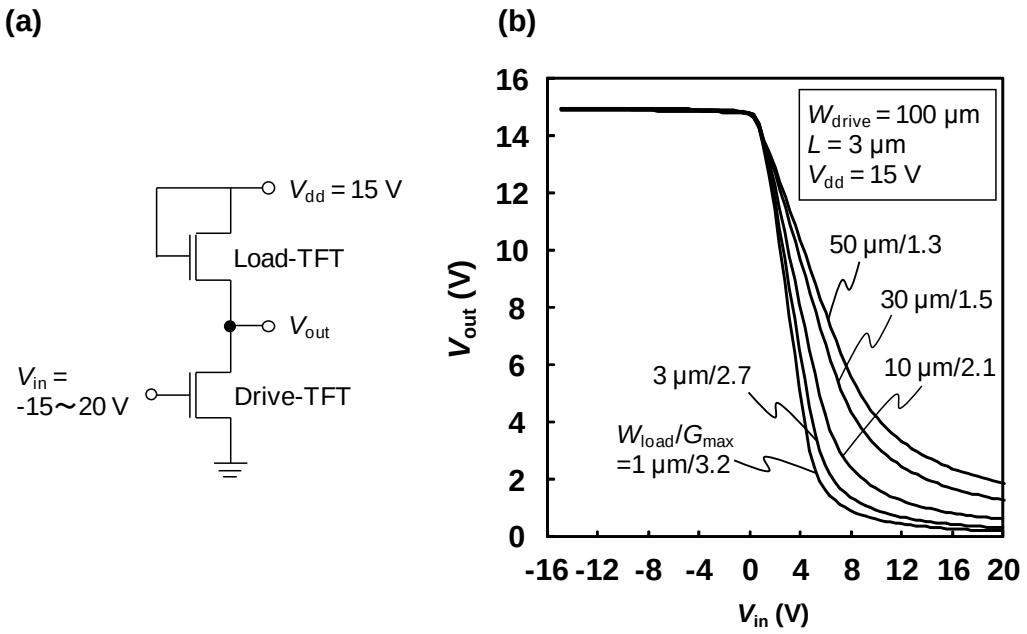


Fig. 4.3 (a) Circuit diagram and (b) DC characteristics of the diode-connected type inverters.

Figures 4.4 and 4.5 show the measurement data of the fabricated ring oscillators. Figure 4.4 shows the dependence on W_{load} and it indicates that T_{delay} decreases as W_{load} increases. Since the ring oscillators with W_{load} = 1 and 50 μm did not show oscillation, Fig. 4.4 only shows the results for W_{load} = 3, 10, 30 μm. Figure 4.5 shows dependence on L and OL. It indicates that T_{delay} decreases as L or OL decreases. Within this investigation, the smallest T_{delay} of 15 ns and the largest oscillation frequency of 6.8 MHz were obtained when W_{drive} = 100 μm, W_{load} = 30 μm, L = OL = 2 μm and V_{dd} = 22 V.

T_{delay} decreases with increase in the current and increases with increase in the parasitic capacitance as understood from equation (4.2), where α is constant, C_{para} is parasitic capacitance and $I_{through}$ is through current.

$$T_{delay} = \alpha \frac{C_{para}}{I_{through}} = \alpha C_{para} \frac{R_{load} + R_{drive}}{V_{dd}}. \quad (4.2)$$

This should be the reason for small T_{delay} with large W_{load}, small L and small OL. The ring oscillator with W_{load} = 1 μm did not show oscillation because the resistance of the load TFT was too high and the current was not enough. On the other hand, the ring oscillator with W_{load} = 50 μm did not show oscillation because the gain of an inverter was not enough as shown in Fig. 4.3. Though G_{max} = 1.3 (larger than 1), it might be smaller than 1 at the operation point of the ring oscillator.

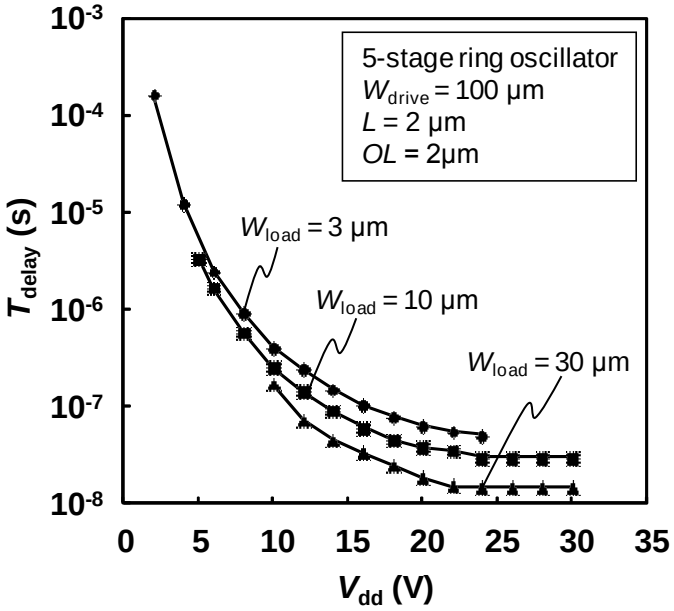


Fig. 4.4 Measured characteristics of 5-stage ring oscillator consist of diode connected type inverters: dependence of T_{delay} on W_{load}.

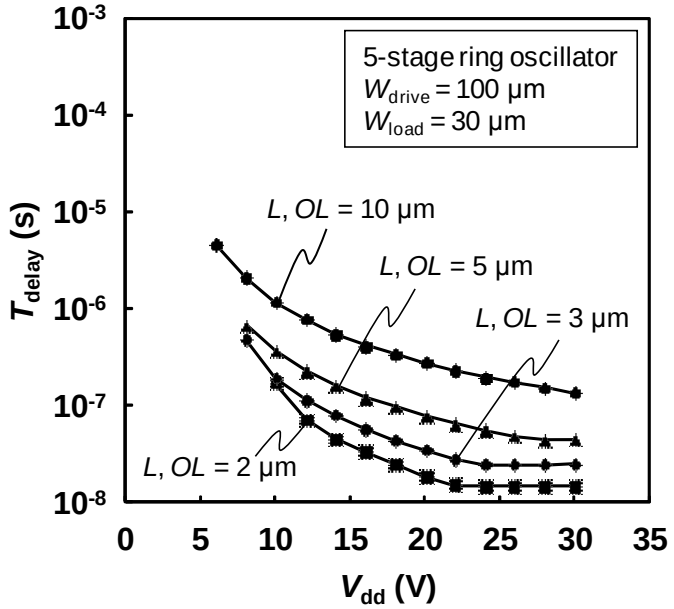


Fig. 4.5 Measured characteristics of 5-stage ring oscillator consist of diode-connected type inverters: dependence of T_{delay} on L and OL.

4.1.3 Estimation of consumption current and frequency of 11 stage ring oscillator consist of diode-connected type inverters

By using the above results, a relation between the oscillation frequency of an 11-stage ring oscillator and the consumption power of the one logic gate was calculated by using equation (4.3).

$$f_{11} = f_5 \frac{5}{11}. \tag{4.3}$$

Here, f_{11} is the frequency of the 11-stage ring oscillator and f_5 is the frequency of 5-stage ring oscillator.

The boundary conditions are as follows; the minimum sizes of *W*, *L* and *OL* are 2 μm and the maximum sizes of *W* and *L* are 100 μm. 2 μm is the limitation of the contact aligner used in this study. The maximum size of *W* and *L* should be as small as possible since it determines the chip size of the RFID.

As shown in Fig. 4.6, the ring oscillators could not achieve the required specifications. The frequency was high enough but the consumption power was too large.

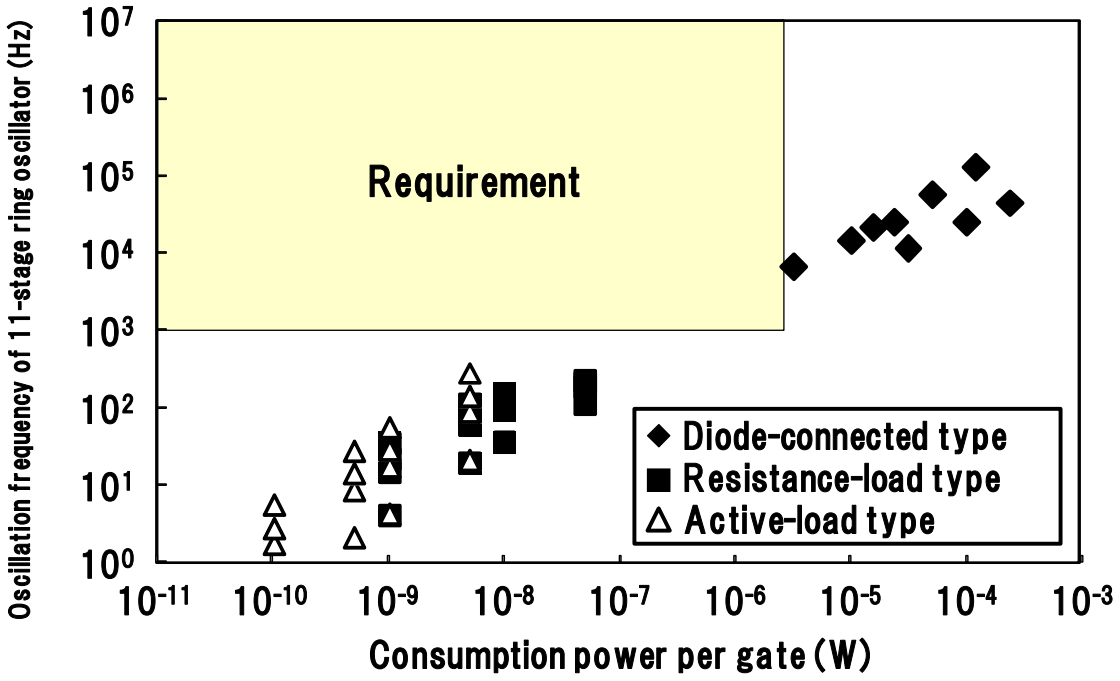


Fig. 4.6 Relation between oscillation frequency of 11-stage ring oscillator and consumption power per gate.

4.1.4 Estimation of consumption current and frequency of 11 stage ring oscillator consist of resistance-load type inverters

The frequency of a ring oscillator using the resistance-load type inverters was also calculated by using equation (4.4).

$$f = \frac{I}{\sum_{i=1}^{2}\left(C_{\mathrm{OLd}i}\Delta V_{\mathrm{OLd}i} + C_{\mathrm{ch}i}\Delta V_{\mathrm{ch}i} + C_{\mathrm{OLs}i}\Delta V_{\mathrm{OLs}i}\right)} \times \frac{1}{2(11-1)}. \tag{4.4}$$

Here, i is the number of TFT in Table 4.1, C_{OLd}, C_{ch}, C_{OLs} are the capacitances of the overlap on drain side, channel, overlap on source side and ΔV_{OLd}, ΔV_{ch}, ΔV_{OLs} are the

differences between the maximum and the minimum voltages applied to the capacitances during one cycle of oscillation. It is determined by the gate-channel capacitance, the parasitic capacitances and the voltage applied to those capacitances. *I* is through current and was calculated from an I_{ds}-V_{gs} curve of a fabricated a-InGaZnO TFT with W = 100 μm and L = 2 μm. The consumption current of a logic gate was also calculated from the I_{ds}-V_{gs} curve.

As shown in Fig. 4.6, this type of ring oscillators also could not achieve the required specs. The consumption power was small enough but the frequency was too low.

4.1.5 Estimation of consumption current and frequency of 11 stage ring oscillator consist of active-load type inverters

The relation between the frequency and the consumption power of a ring oscillator using the active-load type inverters was also calculated by using equation (4.4) and the I_{ds}-V_{gs} curve. As shown in Fig. 4.6, the frequencies of this type of ring oscillators were also too low.

In summary, there is a trade off between the frequency and consumption power of a ring oscillator and it can not be solved with the conventional inverters. Therefore, a novel inverter is needed to achieve the a-InGaZnO RFID.

4.2 Proposal and designing of capacitive-coupling logic gate

The consumption current of diode-connected type inverter was too large because the gate voltage of the load TFT is always V_{dd}. On the other hand, the switching speed of the active-load type inverter was too small because the gate voltage of the load TFT is

0 V and $I_{through}$ was small. Therefore, if the gate voltage of the load TFT can be controlled at the medium voltage, $I_{through}$ also takes medium value (Fig. 4.7) and it solves the trade-off problem.

To achieve the medium gate voltage, we proposed a novel inverter named "capacitive-coupling type inverter" (Fig. 4.8). The gate electrode of the load TFT of this inverter is floating and its voltage is determined by the capacitive coupling between the source electrode (V_{out} is applied) and drain electrode (V_{dd} is applied) (Fig. 4.9). The voltage of the floating gate (V_{fg}) is designed with equation (4.5).

$$V_{fg} = \frac{V_{out}OL_s + V_{dd}OL_d}{OL_s + OL_d}. \tag{4.5}$$

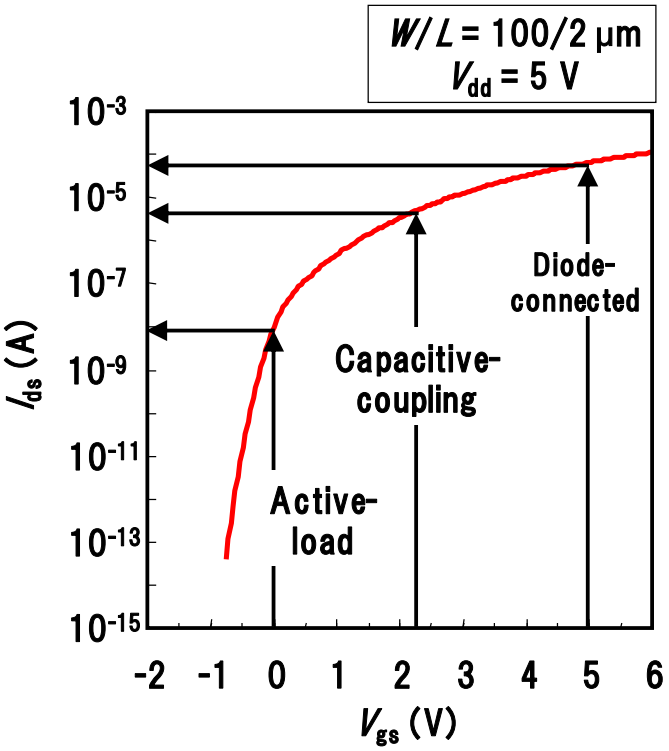


Fig 4.7 I_{ds}-V_{gs} curve of TFT1 of inverter.

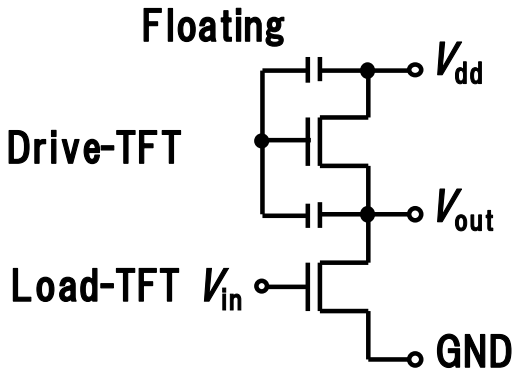


Fig. 4.8 Circuit diagram of capacitive-coupling type inverter.

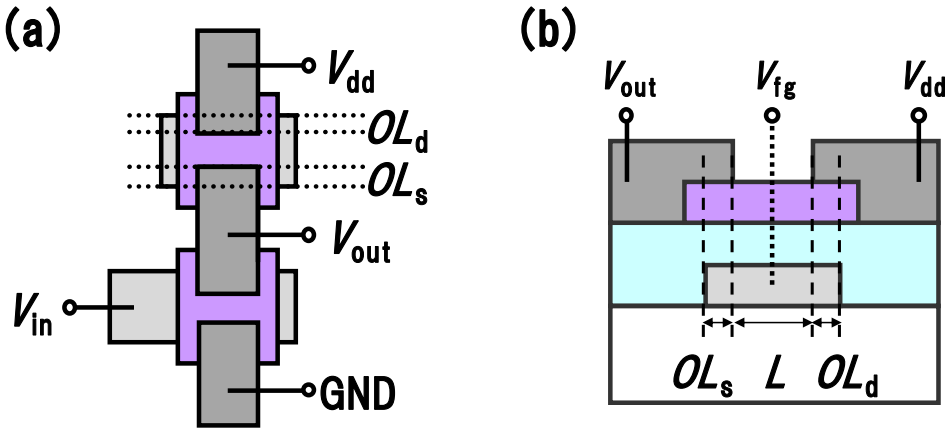


Fig. 4.9 (a) Top view of capacitive-coupling type inverter and (b) cross-sectional view of TFT1 (load TFT).

4.3 Electrical characteristics of fabricated capacitive-coupling type logic circuits

4.3.1 DC characteristics of inverter circuit

Capacitive-coupling type inverter was fabricated and its characteristic was compared with the diode-connected type and active-load type inverters. Figure 4.10 shows the $I_{through}$-V_{in} curves of three types of inverters. The capacitive-coupling type inverter had the medium $I_{through}$ as expected in the previous section. Thus, a medium consumption current is expected. Figure 4.11 shows the on/off switching characteristic of the three types of inverters. The capacitive-coupling type inverter had better switching characteristic than the diode-connected type and thus it should show an oscillation when a ring oscillator is fabricated using this inverter.

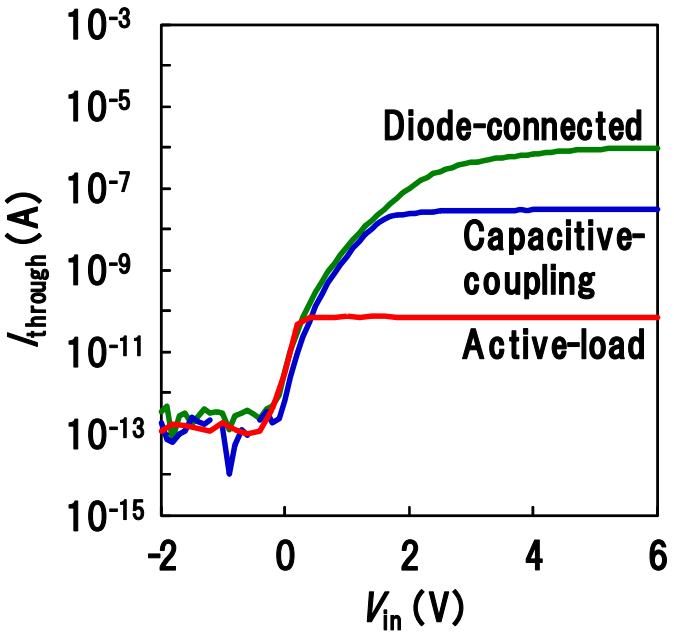


Fig. 4.10 $I_{thorugh}$-V_{in} curves of three types of inverters.

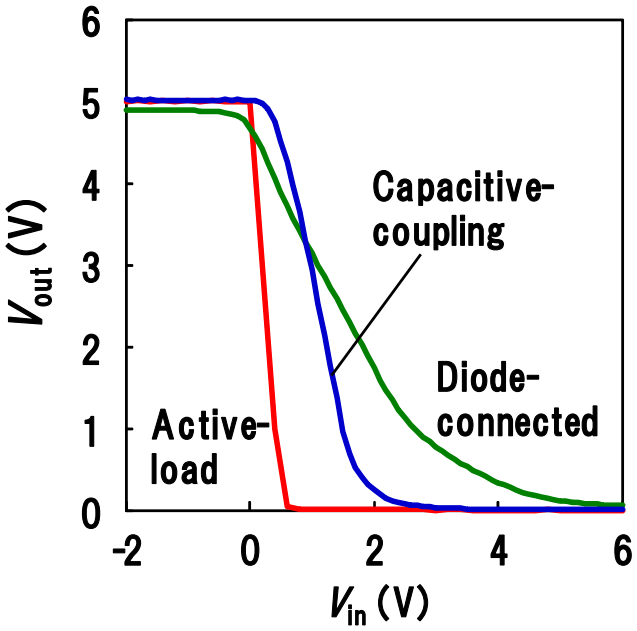


Fig. 4.11 On/off switching characteristic of the three types of inverters.

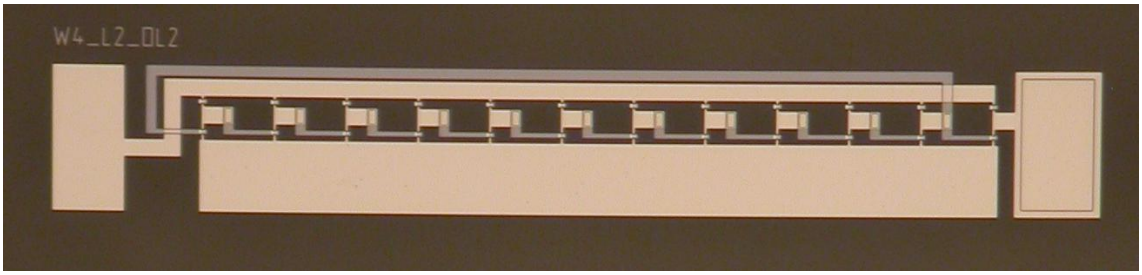


Fig 4.12 Microscopic image of the ring oscillator consists of capacitive-coupling type inverters.

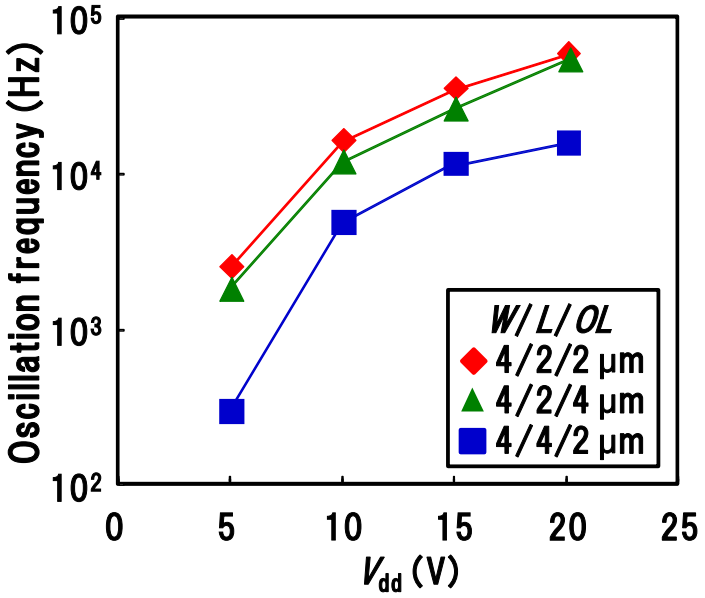


Fig. 4.13 Dependence of oscillation frequency on V_{dd}, L and OL.

4.3.2 AC characteristics of ring oscillator circuit

11-stage ring oscillators consist of the capacitive-coupling type inverters were fabricated. Figure 4.12 is a microscopic image of the ring oscillator. Figure 4.13 shows the dependence of the frequency on V_{dd}, L and OL. W was fixed at 4 μm. The frequency increased with the increase in V_{dd} since the V_{fg} of the load TFT and thus $I_{through}$ increased. It decreased with the increase in L since $I_{through}$ decreased and C_{para} increased. It also decreased with the increase in OL since C_{para} increased. All these results are explained by equation (4.4).

The capacitive-coupling type 11-stage ring oscillators with several sizes of load and drive TFTs were fabricated and the relation between their frequency and the consumption current for one inverter was measured. The boundary conditions are; the minimum sizes of W, L and OL are 2 μm and the maximum sizes of W and L are

100 μm. 2 μm is the limitation of the contact aligner used in this study. The maximum size of *W* and *L* should be as small as possible since it determines the chip size of the RFID. As was expected, the capacitive-coupling type ring oscillators successfully achieved the requirement for the a-InGaZnO RFID (Fig. 4.14).

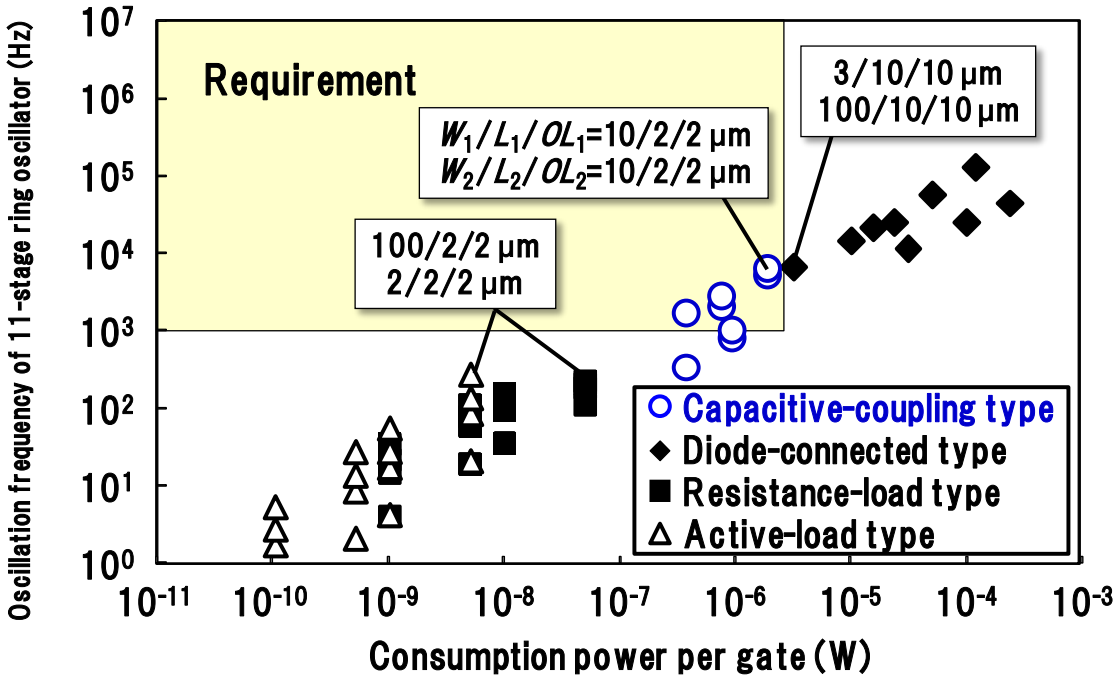


Fig. 4.14 Relation between oscillation frequency of 11-stage ring oscillator and consumption power per gate.

4.4 Discussion

The target for the consumption current was < 2.8 μW and the target for the oscillation frequency was > 1 kHz. The capacitive-coupling type ring oscillator achieved 1.9 μW and 5.7 kHz respectively.

Furthermore, the small size of the capacitive-coupling type inverter leads to the small size of the RFID chip. Assuming replacing conventional type logic gates, which are diode-connected type, resistance-load type and active-load type, with the capacitive-coupling type logic gates, the chip size decreases from 3.5 mm x 3.5 mm to 2.5 mm x 2.5 mm (~50% decrease). Though it has no merit at this stage since the size of antenna coil is 35 mm x 50 mm, the decrease in the size will reduce the chip cost by ~50% when the size of the antenna coil is reduced to 2.5 mm x 2.5 mm.

In order to meet the ISO15693 standard formally, the communication frequency needs to be higher than 26 kbps. Therefore, the internal oscillation frequency of the RFID needs to be higher than 26 kbps (5.7 kbps at the moment). It is expected to increase up to 150 kbps by introducing the following modifications; (1) improvement of the rectifier circuit, (2) reduction of the C_{para} in the ring oscillator, (3) reduction of the stages of the ring oscillator down to 5 stages, (4) reduction of the channel length of the TFTs down to 1 μm.

Chapter 5

Conclusion

5.1 Conclusion

We studied on low-power operating a-InGaZnO TFTs and circuits for flexible RFID application and developed (1) low-voltage operating a-InGaZnO TFT, (2) 13.56-MHz band rectifier circuit and (3) high-frequency and low-power operating logic gate, which are indispensable to flexible RFID application.

1. We discussed the development of a low-voltage operating a-InGaZnO TFT, which is suitable for low-power circuits on a flexible substrate, in chapter 2. We proposed a fully-depleted (FD) type a-InGaZnO TFT and demonstrated 1.5-V operation of it. This TFT utilizes the fully-depleted state for the off state of an nMOS TFT that uses an accumulation layer as a channel layer. We also proposed the operation model and the designing strategy of the TFT. Thanks to the fully-depleted state, a small off current (I_{off}) and a small subthreshold slope (*SS*) were achieved; the smallest *SS*, 62 mV/decade, was close to the theoretical limit of *SS* for a FET. We analyzed the dependence of TFT characteristics on (a) the thickness of the channel layer (t_{ch}), (b) oxygen partial pressure during the sputtering of a-InGaZnO (P_{O2}), (c) the type of the gate insulator, (d) the thickness of the gate insulator (t_{oxf}), (e) operation temperature (*T*) and (f) the length of the channel (*L*). By using the result of these analyses, we then discussed the operation mechanism of the FD

a-InGaZnO TFT and proposed theoretical expressions for *SS*, I_{sd} and V_{th} of the TFT. Furthermore, we estimated the maximum operation frequency (f_m) of the FD a-InGaZnO TFT. We achieved a TFT promising for a flexible wireless communicating devices.

2. We discussed the development of a four-TFT rectifier, which is necessary for wireless power and data transmission, in chapter 3. We developed a four-TFT rectifier that operates with 13.56-MHz band, which is the frequency band widely used for wireless devices such as RFID. We developed a simulation model of an a-InGaZnO TFT based on a model for poly-crystalline silicon TFT and designed the rectifier circuit by using this model. We modified the structure and the fabrication process of the FD a-InGaZnO TFT in order to apply it to a circuit. We fabricated the four-TFT rectifier and demonstrated the wired operation up to 25 MHz and the wireless operation at 13.56 MHz. We discussed the dependence of the output voltage (V_{out}) on (a) the input voltage (V_{in}), (b) the input frequency and (c) the transmittance distance (*d*).

3. We discussed the development of a high-frequency and low-power operating logic gate, which is necessary for a wireless operation with a reader terminal compliant with ISO/IEC 15693 standard, in chapter 4. Degree of freedom in designing an a-InGaZnO TFT circuit is low since, unlike Si FETs, pMOS is not available and V_{th} control is not easy. Therefore, forming RFID logic circuits that satisfy both the frequency and the consumption power with conventional logic gates is not easy. Against this background, we proposed a novel logic gate called

"capacitive-coupling type" and demonstrate an operation with the required frequency and the consumption power using the FD a-InGaZnO TFTs.

As stated above, we studied on the elemental technologies regarding low-voltage operating a-InGaZnO TFT and circuits required for flexible passive-type RFID tag and demonstrated the feasibility of the device.

5.2 Future prospects

In order to put the flexile passive-type RFID into a practical use, there are several issues to be solved.

1. Reduction of process temperature.

   The process temperatures of most of the fabrication processes for a-InGaZnO TFT are low enough to use a flexible sheet such as a plastic film as a substrate. However, at present, over 300^{o}C is used in the gate insulator formation process and thus the reduction of the temperature for this process is a challenge. The process temperature needs to be reduced down to 150-200^{o}C in order for the flexible substrate to endure through the process. It should be achieved by reducing the temperature during the PECVD or sputtering of the insulator film. Though we fabricated some prototypes, a simple reduction of the temperature resulted in degradation of *SS* and bias stability of a TFT. Therefore a technology development is necessary. Regarding other process steps, we used 125^{o}C for the annealing. In a

flat-panel display application, annealing at a temperature higher than 300^{o}C is necessary in order to ensure the bias stability. However, the annealing temperature required for the RFID application can be much lower since the operation time of the circuit is much shorter (less than 1 s per reading operation), the operation voltage is lower (~5 V) and, unlike in a display, there are no back light that accelerates degradation of a TFT during a bias application. In fact, the circuits and RFID did not show degradation during the evaluation, which was performed intermittently for a few hours. We believe that the annealing at 125-150^{o}C is enough for the RFID application.

2. Introduction of a passivation layer.

   Although we did not deposit a passivation layer on an a-InGaZnO layer in this study, it is required in a practical application. This is because the property of an a-InGaZnO TFT is affected by gases in atmosphere as mentioned in chapter 1. The challenge is that the passivation layer needs to be deposited at low temperature such as 150-200^{o}C since we need to use a flexible sheet as a substrate. Furthermore, the passivation layer needs to be deposited without giving damage on a back surface of the a-InGaZnO layer. Otherwise it increases C_{itb} in equation (2.7) and therefore *SS* increases. One candidate is a SiO_2 film deposited at low temperature by PECVD. Within our trial, it did not increase *SS* of a TFT. However, it absorbed H_2O in atmosphere and V_t of a TFT shifted in negative direction as time passed. Therefore, we need another idea to prevent the absorption of H_2O. Adding nitrogen in the passivation film (SiON) might be a good idea.

3. Reduction of a gas permeability of flexible substrate.

   Gases such as H_2O, O_2 and H_2 passing through a flexible substrate also affect on the property of an a-InGaZnO TFT. Therefore, reduction of a gas permeability of a flexible substrate is also a challenge. Adding a protection layer such as a metal layer or SiN layer might be a good solution.

4. Improvement of the accuracy of lithography on flexible substrate.

   Accuracy of the lithography on a flexible substrate is not high at present due to the roughness and expansion/contraction. Therefore, improvement the process of the substrate is a challenge.

5. Demonstration of the flexible passive-type RFID operating within the specification compliant with ISO/IEC 15693 standard.

   The operation of the a-InGaZnO RFID using conventional logic gates was already demonstrated [15, 16]. However, the internal operation frequency is around 50 Hz and hence it must be increased up to tens of kHz. It is already estimated to be achievable by using the capacitive-coupling type logic gate developed in this study along with reduction of the channel length down to 1 μm. It needs to be demonstrated as soon as possible.

6. Addition of the sensing function on to the flexible RFID.

   To make the flexible RFID tag to more useful device, addition of the function such as sensing is required. This fits with the concept of “Internet of Things (IoT)” or “Trillion Sensors Universe.” A physical or chemical sensor compatible with

a-InGaZnO TFT is required in order to achieve it.

Abbreviations

AC:	alternating current
a-Si:	amorphous silicon
DC:	direct current
DOS:	density of states
FD:	fully depleted
FET	field effect transistor
HF:	high frequency (13.56 MHz)
IC:	integrated circuit
ID:	identification
IoT:	internet of things
LSI:	large scale integration
MOS:	metal oxide semiconductor
nMOS:	n-channel metal oxide semiconductor
pc-Si:	polycrystalline silicon
PD:	partially depleted
PECVD:	plasma enhanced chemical vapor deposition
pMOS:	p-channel metal oxide semiconductor
RF:	radio frequency
RFID:	radio-frequency identification
SOI:	silicon on insulator
TEM:	transmission electron microscopy
TFT:	thin-film transistor

Symbols

b (subscript):	denotes back side of channel layer
C_0:	gate insulator capacitance per unit area
C_1:	voltage smoothing capacitor
C_2:	resonance capacitor
C_{ch}	capacitance of channel
C_d:	capacitance of depleted semiconductor film
C_{fr}:	capacitance of fringe coupling
C_{gc}:	gate-channel capacitance
C_{gs}:	gate-source capacitance
C_{itb}:	capacitance of interface traps back surface
C_{itf}:	capacitance of interface traps front surface
C_{OLd}	capacitances of overlap on drain side
C_{OLs}	capacitances of overlap on source side
C_{oxf}:	capacitances of SiO_2 gate insulator,
C_{para}:	parasitic capacitance
C_{reader}:	internal resonance capacitor in RFID reader
C_{sg}:	capacitance of subgap states
d:	distance between antenna coil and reader
E_c:	energy level of conduction band
E_v:	energy level of valence band
E_f:	energy level of Fermi level
E_i:	energy level of intrinsic level

f: frequency

f (subsctipt): denotes front side of channel layer

f_{11}: frequency of 11-stage ring oscillator

f_5: frequency of 5-stage ring oscillator

f_m: maximum operation frequency

f_{mnqs}: maximum operation frequency for non-quasi-static operation

f_{mqs}: maximum operation frequency for quasi-static operation

f_r: resonant frequency

f_{r1}: resonant frequency of reader side LC circuit

f_{r2}: resonant frequency of RFID side LC circuit

G_{max}: the maximum gain of inverter

g_m: transconductance of TFT

i (subscript): denotes gate that is operated

I: current

I_{dj}: drain current at surface where most of current flows

I_{ds}: source-drain current

I_g: gate current

I_{off}: off current

I_{on}: on current

$I_{through}$: through current of inverter

j (subscript): denotes surface where most of current flows

k: Boltzmann constant

L: channel length

L_1 inductance of reader side coil

L_2: inductance of RFID side coil

LA: input terminal of rectifier

LB: input terminal of rectifier

M: mutual inductance between the two coils

M1: gate layer

M2: source/drain layer

N_a: acceptor charge per unit volume

N_d: donor charge per unit volume

N_e: free-electron carrier density

OUTP: output terminal of rectifier for positive voltage

OUTN: output terminal of rectifier for negative voltage

OL: overlap length between gate electrode and source/drain electrodes

Q: amount of charge that needs to be charged and discharged in logic gate during oscillation

q: elementary charge

Q_{ch}: electron charge in the channel per unit area

Q_d: depletion charge per unit area

Q_s: total charge per unit area

R_{drive}: resistance of drive-TFT

R_{load}: resistance of load-TFT

R_1: resistance of circuits connecting to rectifier

SS: subthreshold slope

SS_{fb}: SS when front gate is operated and most of current flows at back side of channel layer

T_d: time taken by the fastest electron injected from source electrode to drift in channel toward drain electrode

T_c: time taken for capacitance between gate and channel to be charged

t_{oxf}: thickness of front side SiO_2 gate insulator

T_{delay}: delay time for 1-stage of ring oscillator

T: operation temperature

t_{ch}: thickness of the channel layer

ΔV_{ch} difference between maximum and minimum voltages applied to C_{ch} during one cycle of oscillation

V_t: turn on voltage; denotes (1) V_{gs} where I_{ds} reaches certain value or (2) V_{th} depending on context

V_{gs}: source to gate voltage

V_{th}: threshold voltage

V_d: drain voltage

ΔV_d: variation in V_d

V_g: gate voltage

ΔV_g: variation in V_g

ΔV_{OLd} difference between maximum and minimum voltages applied to C_{OLd} during one cycle of oscillation

ΔV_{OLs} difference between maximum and minimum voltages applied to C_{OLs} during one cycle of oscillation

V_s: source voltage

ΔV_s: variation in V_s

V_{in}: input voltage

V_{fb}: flat-band voltage

V_{outn}: voltage at OUTN

V_{outp}: voltage at OUTP

V_{LA}: voltage at LA

V_{LB}: voltage at LB

V_{dd}: supply voltage

V_{fg}: voltage of floating gate

W_{drive}: channel width of drive-TFT

W_{load}: channel width of load-TFT

W_{dep}: maximum width of depletion layer

P_{O2}: oxygen partial pressure

ε_0: vacuum permittivity

$\varepsilon_{InGaZnO}$: relative permittivity of a-InGaZnO

ε_s: permittivity of semiconductor

ε_{sio2}: relative permittivity of SiO_2

κ: coupling factor

φ_b: surface potential at back surface of channel layer

$\Delta\varphi_b$: variation inφ_b

φ_f: surface potential at front surface of channel layer

$\Delta\varphi_f$: variation inφ_f

φ_g: potential gap between E_f and E_i

φ_j: surface potential at surface where most current flows

φ_s: surface potential

μ: electron mobility

μ_{fe}: field effect mobility

ω: angular rate

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[1] H. Kurata, K. Otsuga. Y. Sasago, T. Arigane, T. Kawamura, T. Kobayashi, Y. Ikeda, A. Sato, K. Korakai, S. Noda. M.Shimizu, O. Tsuchiya and K. Furusawa, "Self-boosted charge injection for 90-nm-node 4-Gb multilevel AG-AND flash memories programmable at 16 MB/s," *2004 Symposium on VLSI Circuit* (*VLSI Circ.*), 5.4, Honolulu, USA, 2004.

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Patents

Registered

As lead inventor: 5 inventions are registered as Japanese patents and 18 inventions are registered as foreign patents.

As secondary (or after) inventor: 2 inventions are registered as Japanese patents and 2 inventions are registered as foreign patents.

Pending

As lead inventor: 6 inventions are patent-pending in Japan and 6 inventions are patent-pending in foreign countries.

As secondary (or after) inventor: 9 inventions are patent-pending in Japan and 14 inventions are patent-pending in foreign countries.

Part of this study was reported in journal papers [4], [5], international conferences [7], [8], [9], [10],[16] and journal [1].

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