論文 / 著書情報
Article / Book Information

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Title(English)	Low-Power and Low-Jitter Frequency Synthesizers for High-Speed Wireless Communications
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Thesis Outline

Low-Power and Low-Jitter Frequency Synthesizers for High-Speed Wireless Communications

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The thesis is divided into 7 chapters. Chapter 1 discusses an evolution to the era of internet-of-everything which requires the development of low-cost high-performance frequency synthesizer that consumes low power for future portable devices. In Chapter 2, a design guide of the basic conception of oscillators and phase-locked loop to achieve low-integrated-noise are summarized. Chapter 3 describes the design of low-noise oscillators with a constant-current-control in Class-C VCO and a design guide for oscillators for mm-wave frequency generations. Chapter 4 discusses the design of a sub-sampling mm-wave PLL using sub-harmonic injection-locked architecture for low-power and low-jitter integer-N mm-wave PLL. Chapter 5 discusses the design a near-mm-wave fractional-N PLL using frequency and reference doubler for achieving low-jitter performance in a mm-wave fractional-N PLL. Chapter 6 describes an all-digital phase-locked loop in a digitized sub-sampling architecture that achieves low-jitter performance. Chapter 7 summarizes the thesis and future work.