論文 / 著書情報
Article / Book Information

題目(和文)	高速無線通信に向けた低消費電力かつ低ジッタ周波数シンセサイザの研究
Title(English)	Low-Power and Low-Jitter Frequency Synthesizers for High-Speed Wireless Communications
著者(和文)	SIRIBURANONT
Author(English)	Teerachot Siriburanon
出典(和文)	学位:博士(学術), 学位授与機関:東京工業大学, 報告番号:甲第10248号, 授与年月日:2016年3月26日, 学位の種別:課程博士, 審査員:岡田 健一,松澤 昭,益 一哉,高木 茂孝,伊藤 浩之,滝波 浩二
Citation(English)	Degree:Doctor (Academic), Conferring organization: Tokyo Institute of Technology, Report number:甲第10248号, Conferred date:2016/3/26, Degree Type:Course doctor, Examiner:,,,,,
学位種別(和文)	博士論文
Category(English)	Doctoral Thesis
種別(和文)	論文要旨
Type(English)	Summary

（博士課程）
Doctoral Program

論 文 要 旨

THESIS SUMMARY

専攻： Department of	Physical Electronics 専攻	申請学位（専攻分野）： Academic Degree Requested	博士 Doctor of (Philosophy)
学生氏名： Student's Name	Teerachot Siriburanon	指導教員（主）： Academic Advisor(main)	Prof. Kenichi Okada
		指導教員（副）： Academic Advisor(sub)	Prof. Akira Matsuzawa

要旨（英文 800 語程度）
Thesis Summary (approx.800 English Words)

Due to congestion frequency band below 5GHz, utilizing mm-wave frequency bands, e.g., 28GHz or 60GHz bands, which offer larger bandwidth is one of the most promising solution to obtain several tens of Gbps wireless communication. To allow such high-speed communication, frequency synthesizers which offer low-integrated phase noise are required. The issues for such high frequency phase-locked loops are high in-band phase noise and high power consumption. High-performance phase locked loop has been reported using technology node more than 28nm. However, in more advanced technology nodes, i.e. less than 28nm, leakage currents and supply scaling challenges the design of analog building blocks which would result in performance degradation. Therefore, the design of all-digital phase-looked loop (AD-PLL) gains significant attention to both industries and academia.

This dissertation presents a study of low-power low-integrated phase noise frequency synthesizers for high-speed wireless communication to support future demands. The thesis describes architecture considerations and key building blocks to obtain both low-integrated phase noise, and low power consumption for mm-wave integer-N phase locked loop (PLL), mm-wave fractional-N PLL, and all-digital PLL. Chapter 1 discusses an evolution to the era of the internet-of-everything which requires the development of low-cost high-performance frequency synthesizers that consumes low-power consumption for the use in future portable devices. In Chapter 2, the design guide and basic conception of oscillators and phase-locked loop to achieve low-integrated phase noise are summarized. Chapter 3 describes the design of low-noise oscillators with a constant-current-control in Class-C VCO and a design guide for oscillators for mm-wave frequency generations. Traditional class-C VCO offers good current efficient but the performance variation due to the gate bias of cross-coupled pair could alter the performance significantly. In Chapter 3.1, constant-controlled bias circuit for class-C VCO is proposed. It shows more robust phase noise performance over a variation of current consumption. Chapter 3.2 discusses the development of 20GHz VCO based on push-push topology. It utilizes an inductor at the cross-coupled tail transistors which offers higher output impedance and acting as a tail filtering which provide better immunity to maintain high quality factor of the main oscillators.

Chapter 4, for 60-GHz applications, a sub-sampling integer-N frequency synthesizer in a sub-harmonic injection-locked architecture is implemented. The design and analysis of the injection-locked frequency divider (ILFD) using dual-step-mixing architecture are analyzed and compared with traditional single-step mixing ILFD which shows twice larger locking range due to less attenuation factor to the injection efficiency. Moreover, the design optimization of the tank of the 60GHz quadrature injection-locked oscillator (QILO) is described to maintain oscillation under low power consumption. As a result, it can support 16QAM with the baseband tracking bandwidth of 400kHz. In Chapter 5, to serve future 5G mobile communication, a 28-GHz fractional frequency synthesizer using a frequency doubler and reference doubler is developed which results to the state-of-the-art performance for fractional-N PLLs with frequency more than 20GHz. The circuit implementation and phase noise consideration are also discussed in details. In Chapter 6, it describes the development of a voltage-domain all-digital PLL using digital sub-sampling architecture instead of using traditional time-to-digital converters. By using gain amplifier, the gain of sub-sampling phase detector is furthered enhanced which results in higher resolution in phase digitization and higher loop gain. This results in a narrow-range TDC with extremely fine resolution. Unlike traditional bang-bang phase detector or coarse-resolution TDC, this works can achieve low in-band phase noise with wider loop bandwidth for integer-N AD-PLL. Chapter 7 summarizes this thesis and future research direction is described. Voltage-domain or hybrid time/voltage phase digitization shows capability for future high-performance all-digital phase-locked loop that consume low power consumption.

In this dissertation, we have presented sub-sampling technique in mm-wave PLLs and all-digital PLL. Sub-sampling techniques offers high loop gain and high resolution in digital architecture. This results in comparable performance to the state-of-the-art mm-wave PLLs and integer-N AD-PLL as described in Chapter 4 and Chapter 6. Moreover, to further push the performance, reference doubler can be used as described in Chapter 5. Additionally, the design optimization for high performance building blocks, i.e., voltage-controlled oscillators, high speed injection-locked frequency dividers, and quadrature injection-locked oscillators are described in Chapter 3 and Chapter 4. In the future, higher performance PLL would require the development of reference clock multiplier that extends possible bandwidth and lower quantization noise from the TDC in an AD-PLL. Moreover, a more robust operation of fine and coarse phase detection should be addressed.

備考 ： 論文要旨は、和文 2000 字と英文 300 語を 1 部ずつ提出するか、もしくは英文 800 語を 1 部提出してください。
Note : Thesis Summary should be submitted in either a copy of 2000 Japanese Characters and 300 Words (English) or 1copy of 800 Words (English).

注意：論文要旨は、東工大リサーチリポジトリ(T2R2)にてインターネット公表されますので、公表可能な範囲の内容で作成してください。
Attention: Thesis Summary will be published on Tokyo Tech Research Repository Website (T2R2).