論文 / 著書情報
Article / Book Information

題目(和文)	革新的なFPGAアクセラレータのための効率的な開発基盤
Title(English)	Efficient Development Infrastructure for Innovative FPGA Accelerators
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Category(English)	Doctoral Thesis
種別(和文)	論文要旨
Type(English)	Summary

（博士課程）
Doctoral Program

論 文 要 旨

THESIS SUMMARY

専攻： Department of	計算工学 専攻	申請学位（専攻分野）： Academic Degree Requested	博士 （工学） Doctor of
学生氏名： Student's Name	小林 諒平	指導教員（主）： Academic Advisor(main)	吉瀬 謙二
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要旨（英文 800 語程度）
Thesis Summary (approx.800 English Words)

Computer systems have been continuously improved throughout the years, and they tend to employ fabrics such as FPGAs and GPUs to accelerate some computing tasks that normally run on general-purpose CPUs. FPGA-based accelerators can achieve higher performance and better power efficiency than implementations on CPUs and GPUs because designers can implement circuits that realize application-specific pipelined hardware and data supply systems. A lot of companies and research institutes have given considerable attention to FPGAs, and from now on the hybrid computing model based on CPUs, GPUs and FPGAs seriously begins in order to try to build innovative computer systems.

To exploit the remarkable potentials of FPGA-based accelerators, it is truly necessary to consider how to build them. In other words, designers have to pay attention to an appropriate FPGA device, hardware design, and implementation depending on application characteristics. Another obstacle is to need long simulation time for circuit behavior verification. For development of FPGA accelerators, it is usually repeated that Hardware Description Language (HDL) based circuit design and the circuit behavior verification. However, designing large-scale circuits leads to long Register Transfer Level (RTL) simulation time, which means that traditional RTL simulators cannot finish the circuit behavior verification within a realistic time frame. Besides, FPGAs have become larger and larger due to transistor scaling and stacking, and it enables implementation of larger hardware on FPGAs. However the simulation time is also larger, and that is why high-speed simulation environments are required.

This thesis presents a novel infrastructure supporting efficient development of FPGA-based accelerators. The proposed infrastructure shows how to build high-performance FPGA-based accelerators targeting fundamental applications and enables high-speed RTL simulation to verify whether or not a designed accelerator works as intended.

The first contribution of this work is to propose a high performance FPGA-based accelerator for 2D stencil computation. In the last several decades, stencil computation has been accelerated by using multicore microprocessors and GPUs. However, sustained performance is limited due to memory bandwidth restriction, and also because the computation kernel has small arithmetic intensity. To address this problem, I propose a high performance architecture for 2D stencil computation employing multiple small FPGAs. In this architecture, the data set is divided into multiple blocks and each block is assigned to each FPGA, which means that the data set is stored in FPGA internal memory instead of in an external DRAM. This also means that the according to this architecture, the number of connected FPGAs scales with the size of the data set. The proposed stencil computation hardware was implemented with HDL, and I confirmed that the developed hardware accurately worked. The evaluation result shows that the proposed accelerator achieves even better power efficiency than a typical GPU.

The second contribution of this work is to propose an FPGA-based sorting accelerator, which combines the sorting network and the merge sorter tree. The proposed sorting hardware is customizable by means of tuning design parameters. I also provide an analytical model that accurately estimates the sorting performance depending on the hardware configuration. In other words, designers can estimate sorting accelerator performance in advance and can implement the best one that fulfills cost and performance constraints. I also propose a data compression mechanism for the sorting accelerator to mitigate memory bandwidth limitation. Similar to the stencil-computation accelerator, I developed the proposed sorting accelerator with HDL, and confirmed that the developed hardware actually achieved the estimated performance and higher performance than a typical desktop computer. In order to allow every designer to easily and freely use

this accelerator, the RTL source code is released as an open-sourced hardware.

Finally I summarized important points for the efficient development infrastructure of FPGA-based accelerators according to the two previous contributions. For development of FPGA accelerators, designers implement logic circuits with HDL and verify the circuit behavior. However, designing large-scale circuits leads to long RTL simulation time, which means that traditional RTL simulators cannot finish the circuit behavior verification within a realistic time frame. To address this problem, I propose a high-speed RTL simulator employing two prior studies. I evaluated it in terms of the RTL simulation speed by using the designs of the two proposed accelerators, and confirmed that it could do the RTL simulation much faster than a commercial one. Also, I discussed that the findings obtained from the development of the two FPGA-based accelerators are useful in other hardware platforms and computation kernels.