論文 / 著書情報
Article / Book Information

題目(和文)	
Title(English)	Charge Trapping Characteristics of MAHOS Capacitor Structures with High-k Dielectric Materials as Charge Trapping Layers
著者(和文)	RifaiAbdulloh
Author(English)	Abdulloh Rifai
出典(和文)	学位:博士（工学）, 学位授与機関:東京工業大学, 報告番号:甲第10027号, 授与年月日:2015年12月31日, 学位の種別:課程博士, 審査員:中村 吉男,史 蹟,小林 能直,村石 信二,三宮 工
Citation(English)	Degree:, Conferring organization: Tokyo Institute of Technology, Report number:甲第10027号, Conferred date:2015/12/31, Degree Type:Course doctor, Examiner:,,,,
学位種別(和文)	博士論文
Type(English)	Doctoral Thesis

The Dissertation Committee for Tokyo Institute of Technology certifies that this is the approved version of the following dissertation:

Charge Trapping Characteristics of MAHOS Capacitor Structures with High-κ Dielectric Materials as Charge Trapping Layers

Committee:

Supervisor: _____

(Yoshio Nakamura)

Charge Trapping Characteristics of MAHOS Capacitor Structures with High-κ Dielectric Materials as Charge Trapping Layers

by

Abdulloh Rifai

(11D51284)

Dissertation

Presented to Department of Metallurgy and Ceramics Science

Faculty of Graduate School of Science and Engineering

of Tokyo Institute of Technology

in Partial Fulfillment

of the Requirements

for the Degree of

Doctor of Engineering

Tokyo Institute of Technology

December 2014

Contents

Chapter 1
Introduction

In this chapter, the basics of non-volatile memory will be described and the role of high-κ dielectric materials as tunneling layer, blocking layer, and charge trapping layer in memory structures will be reviewed. Current status on utilizing high-κ dielectric materials as charge trapping layers will be discussed. Motivation of this research will be stated. Issue and challenges in this field of research will be identified. Strategy to solve the issue is proposed and the chapter is ended by stating our research purposes which would be the centerpiece of our work.

1.1 The Basics of Non-Volatile Memory

Based on data loss due to disconnected power supply, memory device can be classified into two groups, including volatile memory and non-volatile memory, as shown in Figure 1.1. Volatile memory, such as SRAM and DRAM, is memory that requires power to maintain the stored information. A volatile memory typically has a worst case retention time of less than a second. Non-volatile memory is memory that has the ability to maintain data when the circuit power supply is turned off. Non-volatile memories have two major application, including code applications and data applications[1]. For code applications, non-volatile memories store the program and operating system and process it by microprocessor or microcontroller. Non-volatile memory integration in logic systems allows software updates, stores identification codes, or reconfigures the system on the field. In this sense, non-volatile memory devices are widely used in several fields, such as in the computer environment, on the computer network equipments, and in the automotive electronics. In the computer environment, non-volatile memory stores and updates the operation system in PC BIOS and harddisk drives, in almost all peripherals such as printers and DVD–readers, and in

most add-on boards such as video and sound cards. On computer network equipments, non-volatile memory upgrades the software in modems, interface cards and network routers. In the automotive electronics field, non-volatile memories are used in vital function such as engine control units (ECUs) and global positioning systems (GPS). For data applications, non-volatile memories are used as data storage where data files for document, audio and video files are recorded and read sequentially. This is to create storing elements like memory boards or solid-state hard disks, made by Flash memory arrays, which are configured to create large size memories.

Flash EEPROM, which is a type of non-volatile memory, can be electrically programmed and erased. There are some variants of Flash, but in current production, Flash memory is dominated by two types, including NAND Flash, which is oriented toward data - block storage applications, and NOR Flash, which is suited for code and word addressable data storage. Flash memory devices are mainly charge-based where charge can be injected into or removed from a critical region of a device and the presence or absence of the charge can be sensed. Charge-based memory was invented by Sze and Kahng at Bell Labs in 1967[1]. The program/erase state is defined via adding charges to and removing charges from the charge-storage layer respectively. Charge-based memory is compatible with the complementary metal-oxide-semiconductor (CMOS) technology, and easy to be integrated with current fabrication process.

Figure 1.2 shows the cross-section of a floating-gate memory transistor which is the first generation of charge-based memory structure. The floating-gate memory consists of a polysilicon layer formed within the gate insulators, tunneling layer and blocking layer, between the normal gate electrode (the control gate) and the channel. The amount of charge is injected on the floating gate during programming. Since the floating gate is completely surrounded by insulators, it retains charge for a long period of time independent of whether

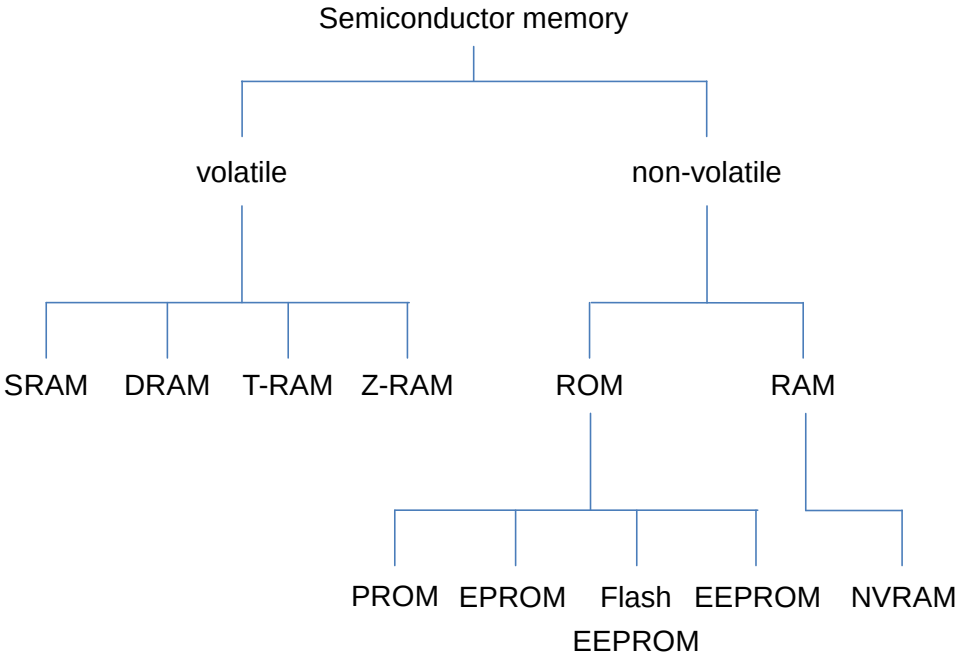


Figure 1.1 Classification of semiconductor memory.

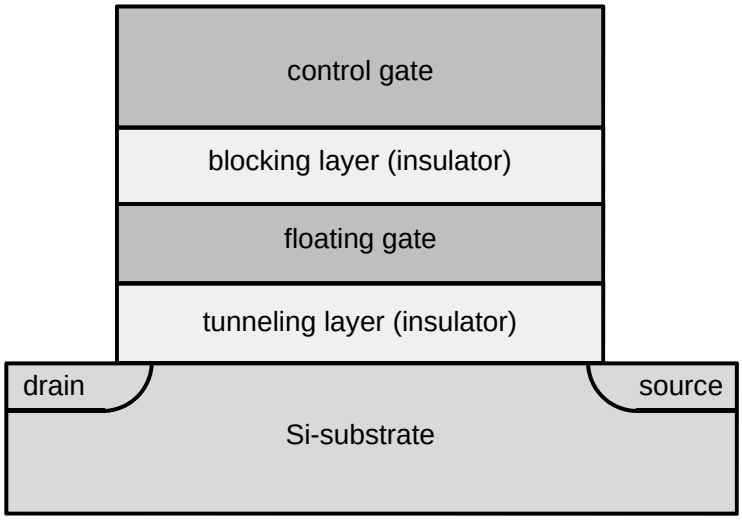


Figure 1.2 The structure of charge-based memory transistor.

the circuit power supply voltage is present.

To understand the nature of the charge-based memory device, we need to consider the energy levels involved. Figure 1.3 shows the band structure for a simple charge-based memory device. The n-type poly-Si floating gate is embedded within insulators and isolated from the exit or entry of charge by the high – energy barrier. These barriers, which are much greater than the thermal energy, provide nonvolatile retention of the charge. The amount of charge stored on the floating gate can be changed by changing the potential of the floating gate relative to the potential on the opposite side of either SiO_2 layer until some conduction mechanism is invoked that can overcome or tunnel through the barrier. Two common conduction mechanisms are channel hot – electron (CHE) injection and Fowler – Nordheim (FN) tunneling.

The process of writing or storing data into a charge-based memory involves two operations, including initializing the state of the cells which means that all of the cells are cleared to a “one” state and programming the cells to “zero” or left at “one” in accord with the input data signals. Figure 1.4 shows the relative relationship of the erase and program states in terms of the resulting current – voltage characteristics. Erasing moves the threshold voltage in a negative direction while writing moves the threshold voltage in a positive direction.

There are two parameters that describe reliability of a nonvolatile memory cell, including retention and endurance[1]. Retention defines the elapsed time between data storage and the first erroneous readout of the data. There are three factors that can impact the retention properties, which are defects associated with materials, details of device geometry, and aspects of circuit design. Each of these three factors can result in the addition or removal of charge to/from the floating gate. The processes involved in writing or reading non-volatile memory cells results in stresses that eventually degrade the properties of the memory or

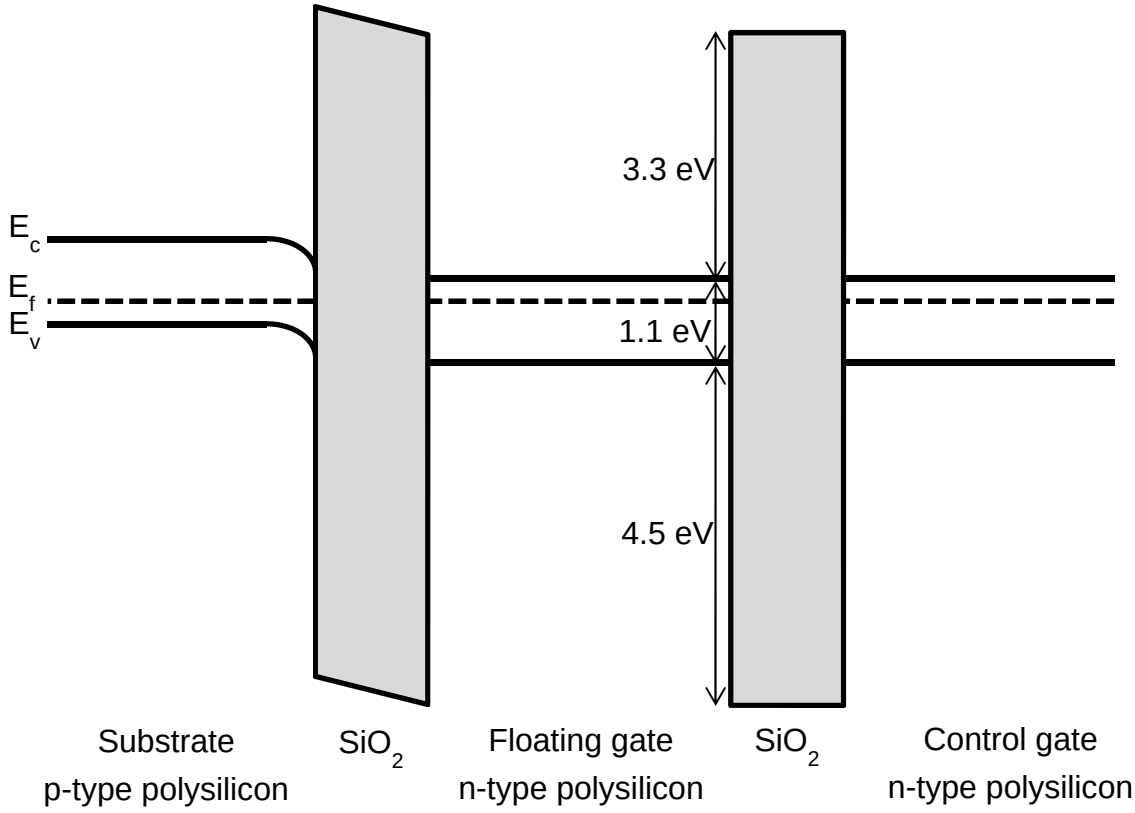


Figure 1.3 Energy band diagram for a typical charge-based memory structure.

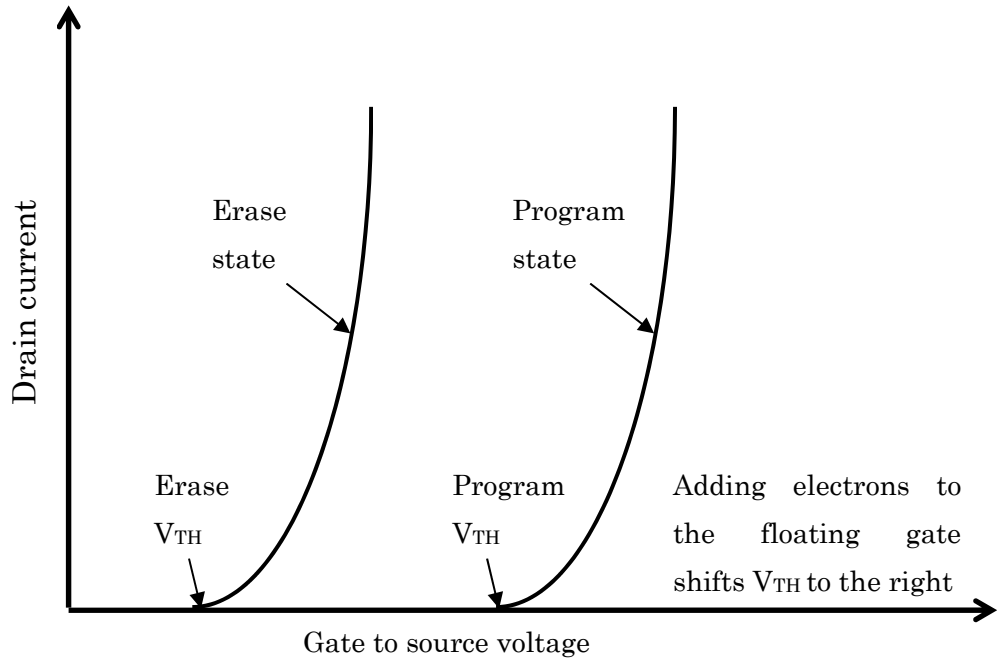


Figure 1.4 The current – voltage characteristics of erase state and program state.

disturb the contents of the memory. The ability of a device to withstand stresses is called endurance which is quantified as a minimum number of erase – write cycles or write – read cycles that the non-volatile memory chips can be expected to survive.

1.2 The Role of High-κ Dielectric Materials in Non-Volatile Memory

The use of high-κ dielectric materials in electronic devices, such as metal-oxide-semiconductor field effect transistors (MOSFETs) is prompted by the need of new gate insulators to replace SiO_2 in future generation of MOSFETs in order to meet the attempt to reduce the device dimensions by following Moore's law. Due to higher dielectric constant, with the same equivalent oxide thickness (EOT) with SiO_2, high-κ dielectric materials can be thicker without reducing the device performance.

In recent development of floating gate structure for non-volatile memory application, high-κ dielectric has been investigated as tunneling layer replacing SiO_2, blocking layer, and charge trapping layer.

1.2.1 High-κ Dielectric Materials as Blocking Layer

The first generation flash memory uses SiO_2 as blocking layer. As the flash memory's dimension is continually scaled down, the use of SiO_2 become unacceptable due to the large tunneling current through SiO_2. Since the erase speed for this type of SONOS devices is determined by the competition of the direct band-to-band tunneling current through a tunnel oxide and the unwanted Fowler-Nordheim tunneling current through a blocking oxide, the tunnel oxide thickness is fundamentally required to be less than 2 nm for a stable erase operation. Therefore, numerous attempts have been tried to replace thermal oxides by new dielectrics or related new structures.

As the blocking oxide layer, high-κ dielectrics proportionally reduced the electric field across the blocking oxide with its dielectric constant. Therefore, electron injection from

the gate during erase can be effectively suppressed, which will generally in turn enhance the erase speed. In addition, using a physical thicker blocking layer film minimizes the electron leaking out to the gate during retention. Materials with high-κ dielectric constants can be seen in Figure 1.5[3]. There are some good candidate dielectrics to replace SiO_2, including Al_2O_3 and rare earth oxides, such as Gd-based dielectric (Gd_2O_3 and Al-doped Gd_2O_3), La-based dielectric (La_2O_3 and $LaAlO_x$), and Y-based dielectric (Y_2O_3 and Y_xAl_yO)[4-7].

Al_2O_3 has some favourable properties, including a wide band gap, high dielectric constant ($\kappa \sim 9$) which is higher than SiO_2 ($\kappa \sim 3.9$), good thermodynamic stability on Si up to high temperatures, and amorphous under the condition of interest. Fast program/erase operation by Fowler – Nordheim (FN) tunneling has been achieved by utilizing Al_2O_3 as blocking layer in SANOS structure which consist of $Si/Al_2O_3/Si_3N_4/SiO_2/Si$[4]. In addition, this structure achieves longer data retention and realizes lower voltage programming. Faster operation speed has also been obtained by using Al_2O_3 as blocking layer. However, due to its dielectric constant, Al_2O_3 is not suitable as long-term solution. Gd-based dielectric shows a superior charge retention property and an improved operation speed[5]. La-based dielectric is considered as blocking layer due to its relatively large conduction band offset and high dielectric constant[6]. Its properties provide faster program speed, wider threshold voltage window, more robustness to voltage stress, and has a better retention properties under temperature below 120^{o}C. Y_2O_3 is also potential as blocking layer due to its strongest affinity for oxygen, no humidity absorption, and no magnetic characteristic. However Y_2O_3 has poor thermal property and relaatively small band gap, ~6 eV. The optimized Y*x*Al*y*O film shows lower interface-state density, lower bulk charge-trapping density, higher dielectric constant, and smaller gate leakage, due to the suppressed interlayer and good thermal property ascribed to appropriate Y and Al contents in the thin film[7].

1.2.2 High-κ Dielectric Materials as Tunneling Layer

SiO_2 is used as tunneling layer in the first generation of flash memory and SONOS. SiO_2 is chosen because it can be thermally grown on Si substrate, has the largest band gap among dielectric materials, and make a good contact with Si with best interface quality as well as least oxide traps, thus lowest leakage current. Considering reliability degradation issue, thermal SiO_2 is still the best option as tunneling layer. For the next generation flash memory, it is required that memory devices have thinner tunneling oxide to achieve higher program/erase speeds and lower operating voltages. However, SiO_2 as tunneling layer suffers from retention problem due to direct tunneling leakage through the thin tunnel oxide.

To solve the retention issue, a band-gap engineered ONO tunneling dielectric was proposed to replace the traditional SiO_2 in SONOS structure since the ultra-thin nitride which is less than 2 nm has negligible charge trapping[8]. This concept is demonstrated by a multilayer structure of SONONOS with the ultra-thin O1/N1/O2 structure as a tunneling dielectric, N2 as the charge storage layer, and O3 as the blocking oxide. The ultra-thin ONO structure suppresses direct tunneling at low electric field during retention, while it allows efficient hole tunneling erase at high electric field due to the band offset. The ONO tunneling dielectric serves as an efficient hole tunneling barrier for SONOS, and it is much more reliable and practical. Therefore, this SONOS offers fast hole tunneling erase, while it is immune to the retention problem of the conventional SONOS.

Another option to solve the retention issue due to tunneling layer scaling is to utilize a novel multilayer tunnel barrier which consists of a two-layer dielectrics stack with a low-κ/high-κ combination or three-layer dielectric stack with low-κ/high-κ/low-κ combination in symmetric form that allows for either lower voltage or higher speed programming due to the increased current-voltage (I-V) slope[9]. The stack can be regarded as a VARIable Oxide Thickness (VARIOT) dielectric. The thicker physical thickness of the

stack offers better retention as compared to the EOT layer at low biases.

1.2.3 High-κ Dielectric Materials as Charge Trapping Layer

In 1990s, the performance and reliability of non-volatile memory (NVM) was enhanced by appplying silicon-oxide-nitride-oxide-silicon (SONOS) technology in which thin Si_3N_4 film was used as charge trapping layer replacing the conducting polysilicon floating-gate electrode[10]. Si_3N_4 film in SONOS device improved endurance since a single defect will not cause the discharge of the memory. In SONOS memory, the charges are stored in isolated sites within the Si_3N_4 dielectric. To suppress short-channel effects, it is required to scale down the charge-trapping layer to <6 nm. However, this becomes issue since the charge trapping deteriorates when the Si_3N_4 is made thinner. Very little charge trapped in a 2 nm Si_3N_4 layer in SONOS. In addition, the high temperature retention also gets worse when the Si_3N_4 is thin because of the higher trap energy in the oxide/Si_3N_4/oxide, arising from quantum confinement.

The dielectric constant of Si_3N_4, $\kappa \sim 7$, is not so high that it also faces issues related to the the continual down-scaling of cell size and reduction of operating voltage. Various high-κ dielectrics with higher κ value have been widely investigated as charge trapping layer to solve these issues. With higher dielectric constant, high-κ dielectrics allow a higher electric field over the tunnel dielectric and results in enhanced program/erase speed. For charge trapping layer, crystalline high-*k* dielectrics is preferable than amorphous one, for example, tetragonal and cubic ZrO_2, have theoretical *k*-values of 46.6 and 36.8, respectively, which are much higher than their amorphous-phase counterpart, so they will be beneficial to enhance memory performance[11].

In addition, high-κ dielectrics should have a larger conduction-band offset with respect to the tunnel dielectric to get better charge retention. Another drawback of Si_3N_4 as charge trapping layer in SONOS structure is it has small conduction band discontinuity at the

Si_3N_4/SiO_2 interface, which causes the charge leak out from the shallow trap levels of Si_3N_4. To overcome this problem, high-*k* dielectric materials, such as ZrO_2, HfO_2, and Ta_2O_5 are promising candidates to replace a Si_3N_4 film as the charge trapping layer of SONOS memory devices since they have a larger conduction-band offset as shown in Figure 1.6[12]. By using such high-*k* dielectric films, charge trapping characteristics can be improved since they have sufficient densities of trap states and deep trap energy levels which give rise to better data retention.

1.3 Background of the Research

1.3.1 Motivation of the Research

The development of the next generation charge-based non-volatile memory requires the memory device to be scaled down without deteriorating the charge trapping characteritics of the device and to be able to achieve fast programming/erasing speed with low programming voltage and good retention for over 10 years. The scaling projection for charge-based non-volatile memory devices can be found in the International Technology Roadmap for Semiconductor (ITRS) documents. The ITRS scaling projection has been used by researchers as a guideline for further improvement in the field of non-volatile memory. Table 1.1 and Table 1.2 show the ITRS scaling projection for charge trapping NAND flash and NOR flash, respectively. The memory devices will progressively scaled down beyond 25 nm technology.

Thermally grown SiO_2 is still the best choise as tunneling layer since amorphous SiO_2 is an excellent insulator with very few electronic defects and it forms an excellent interface with Si. As tunneling layer, its thickness cannot be reduced to less than 3 nm because because the charge will tunnel across it by direct tunneling mechanism. Instead of SiO_2, the ONO structure which consists of $SiO_2/Si_3N_4/SiO_2$ stack is used as tunneling layer since it

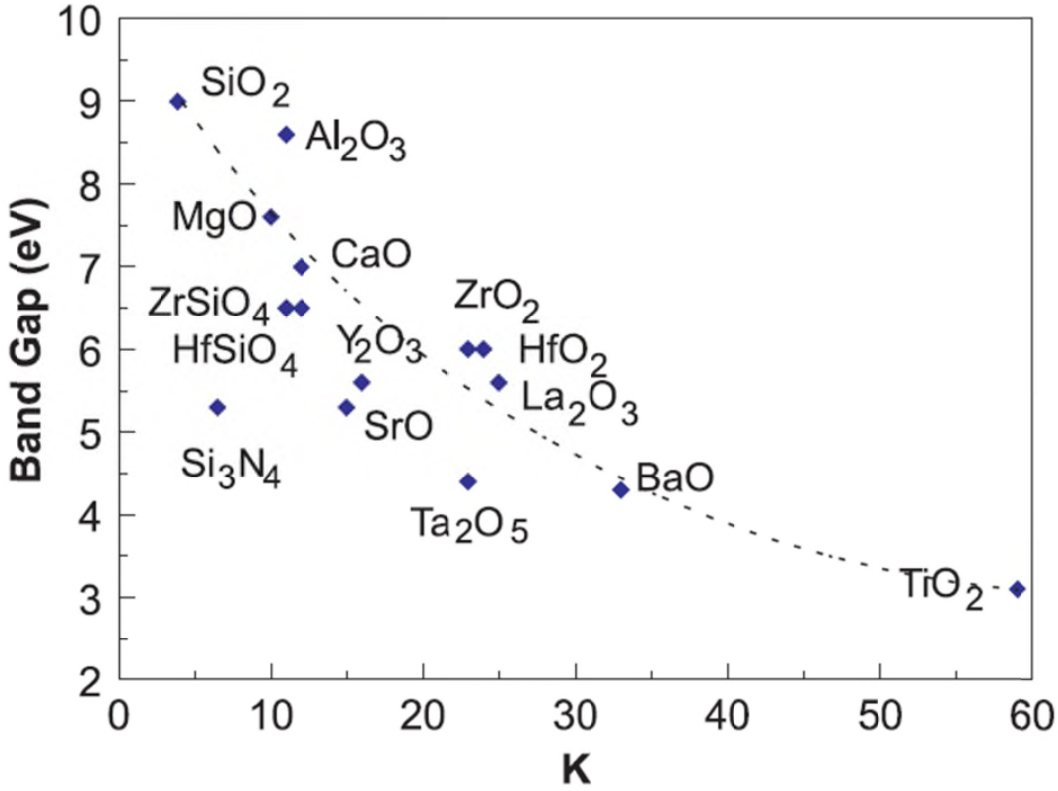


Figure 1.5 Static dielectric constant vs. band gap for candidate gate oxides[3].

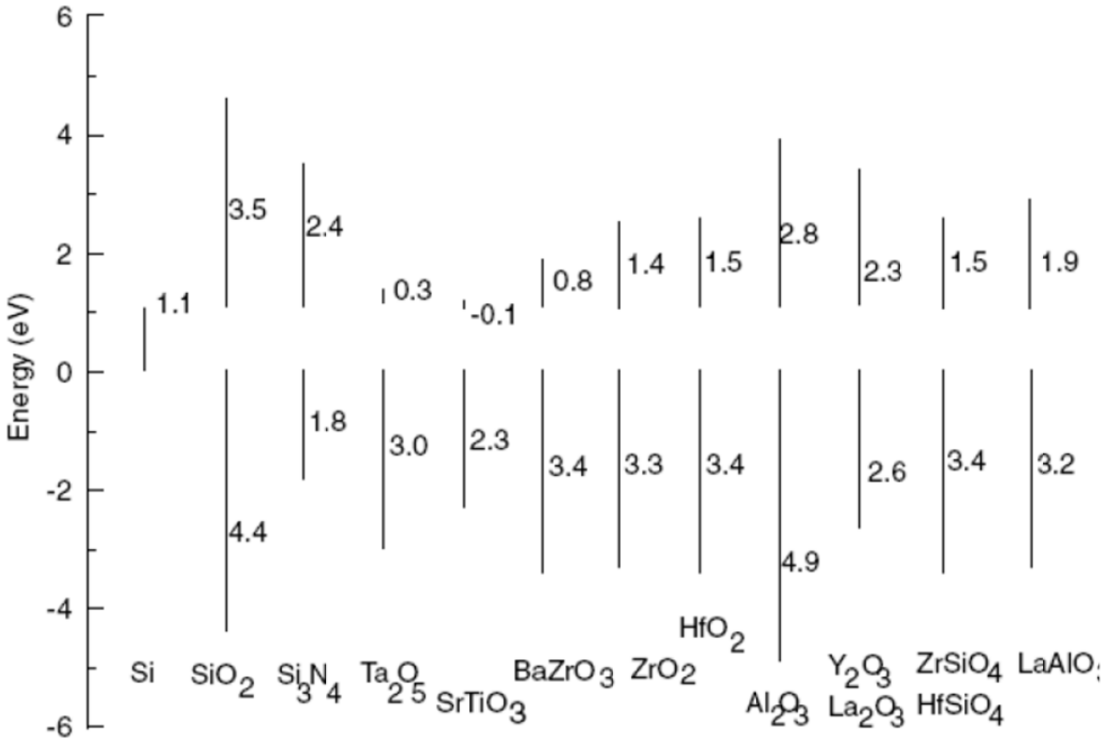


Figure 1.6 Band alignments of high-κ dielectrics[12].

Table 1.1 International Technology Roadmap for Semiconductors (ITRS) scaling projections for charge trapping NAND flash[13].

Year of Production	2012	2013	2014	2015	2016	2024
Charge trapping NAND Flash (MANOS or Barrier Engineering)						
NAND Flash poly 1/2 Pitch (nm)	25	22	20	19	18	8
Cell size – area factor a in multiples of F^2 SLC/MLC	4.0/1.3	4.0/1.3	4.0/1.0	4.0/1.0	4.0/1.0	4.0/1.0
Tunnel dielectric material	SiO_2 or ONO	SiO_2 or ONO	SiO_2 or ONO	SiO_2 or ONO	SiO_2 or ONO	SiO_2 or ONO
Tunnel dielectric thickness EOT (nm)	3 – 4	3 – 4	3 – 4	3 – 4	3 – 4	3 – 4
Blocking dielectric material	Al_2O_3	Al_2O_3	Al_2O_3	Al_2O_3	Al_2O_3	Al_2O_3
Blocking dielectric thickness EOT (nm)	6 – 8	6 – 8	6	6	6	5
Charge trapping layer material	SiN	SiN	SiN	SiN	SiN/high-κ	SiN/high-κ
Charge trapping layer thickness (nm)	5 – 7	5	4 – 6	4 – 6	4 – 6	3 – 4
Gate material	Metal	Metal	Metal	Metal	Metal	Metal
Highest W/E voltage (V)	15 – 17	15 – 17	15 – 17	15 – 17	15 – 17	15 – 17
Endurance (erase/write cycles)	10×10^5	10×10^4	10×10^4	10×10^4	10×10^4	10×10^4
Non-volatile data retention (years)	10 – 20	10 – 20	10 – 20	10 – 20	5 – 10	5 – 10
Maximum number of bits per cell (MLC)	3	3	4	4	4	4

Table 1.2 International Technology Roadmap for Semiconductors (ITRS) scaling projections for charge trapping NOR flash[13].

Year of Production	2012	2013	2014	2015	2016	2024
Charge trapping NOR Flash (SONOS/NROM)						
SONOS/NROM technology node, F (nm)	35	32	28	25	22	10
SONOS/NROM cell size – area factor a in multiples of F^2	7 – 8	7 – 8	7 – 8	8 – 9	8 – 9	9 – 10
Cell size (per bit) – area factor a in multiples of F^2 SLC/MLC	3.7/1.9	3.7/1.9	3.7/1.9	4.3/2.2	4.3/2.2	4.8/2.4
Gate length L_g, physical (nm)	100	100	90	90	80	60
Tunnel oxide thickness (nm)	4.5	4	4	4	4	3.5
Charge trapping layer thickness (nm)	4 – 6	4 – 6	4 – 6	4 – 5	4 – 5	4
Blocking (top) dielectric material EOT (nm)	6 – 8	6 – 8	6 – 8	5 – 7	5 – 7	5 – 7
Highest W/E voltage (V)	6 – 8	6 – 8	5 – 7	5 – 7	5 – 7	4 – 6
I_{read} (μA)	17 – 22	15 – 20	14 – 19	13 – 18	12 – 17	6 – 10
Endurance (erase/write cycles)	10×10^5	10×10^5	10×10^5	10×10^6	10×10^6	
Non-volatile data retention (years)	10 – 20	10 – 20	10 – 20	10 – 20	10 – 20	10 – 20
Maximum number of bits per cell (physical 2-bit/cell + MLC)	2 – 4	2 – 4	2 – 4	4	4	4

suppresses direct tunneling at low electric field during retention and allows efficient hole tunneling erase at high electric field. Al_2O_3 is used as blocking layer due to good thermodynamic stability on Si up to high temperatures, higher dielectric constant of 9, and a wide band gap. The thickness of Al_2O_3 is projected to be reduced to 5 nm in 2024. As charge trapping layer, Si_3N_4 is used since the charges are stored in isolated sites within the Si_3N_4 dielectric and it provides good endurance. The thickness of charge trapping layer is projected to be scaled down to about 4 – 6 nm in the next few years and 3 – 4 nm in 2024 and it has been reported that Si_3N_4 as charge trapping layer faces issues related to the the continual down-scaling of cell size. Therefore, high-κ dielectric material is considered to replace Si_3N_4.

1.3.2 Current Status of Research utilizing High-κ Dielectric Materials as Charge Traping Layers

Many non-volatile memory structures have been prepared with high-κ dielectric materials as charge trapping layer in various kinds of structures, such as SOHOS device, MHOS device, MONOS device, MOHOS device etc. Different kinds of methods have been used to deposit materials, including chemical vapour deposition, reactive magnetron sputtering, atomic layer deposition, etc. Charge trapping characteristics, including program/erase characteristic, endurance characteristics, and retention characteristics have been reported.

The polysilicon–oxide–high-κ–oxide–silicon (SOHOS) structure with high-κ dielectrics as charge trapping layer have been investigated. Compared to the conventional SONOS devices, the SOHOS structure, with HfO_2 as the charge-storage layer, demonstrates a superior charge-storage capability at low voltages, faster programming, and less over-erase problems compared to the conventional SONOS devices. However, it suffers from a poorer charge-retention capability than the SONOS one. On the other hand, The SOHOS structure with Al_2O_3 as the charge-storage layer results in an improved charge-retention performance,

but at the expense of a slower programming speed. By adding a small amount of Al to HfO_2 to form HfAlO, the SOHOS structure with HfAlO as the charge trapping layer combines the advantages of both HfO_2 and Al_2O_3, such as fast programming speed and good charge-retention capability[14]. In this structure, electron trapped in the bulk of the HfAlO layer, rather than negative charge trapping at the tunnel oxide/high-*k* interface, since the charge-storage capability depends on the HfAlO thickness.

The charge trapping and tunneling characteristics of the metal-hafnium-oxide-semiconductor (MHOS) structure capacitors with HfO_2 layer as charge trapping layer have been investigated and compared with those of metal-nitride-oxide-semiconductor (MNOS) structure capacitors[15]. It is reported that at the same trap layer thickness, the MHOS capacitors showed a larger memory window than the MNOS capacitors. The ultrathin HfO_2 trap layer with a thickness of 2 nm stored almost the same charges with Si_3N_4 layer with a thickness of 7 nm. These results show that the HfO_2 layer has better charge trapping efficiency than the Si_3N_4 layer. The MNOS capacitors faces scaling-down issue due to the increase of tunneling current. On the other hand, in MHOS capacitor the gate leakage current due to tunneling was reduced significantly by stacking the HfO_2 trap layer on thin SiO_2 tunnel layer.

In 2008, MONOS memory devices which has the structure of TaN/HfLaON/ $Hf_{1-x-y}N_xO_y/SiO_2/Si$ was fabricated and the nitrogen composition dependence of the characteristics was studied by Yang *et al.*[16]. Lower program/erase voltages and better high temperature retention can be achieved with using a higher *k* $Hf_{1-x-y}N_xO_y$ dielectric as charge trapping layer. To investigate how nitride composition alters the characteristics, its composition in the $Hf_{1-x-y}N_xO_y$ was varied. By increasing the N composition in the $Hf_{1-x-y}N_xO_y$ trapping layer, both the memory window and high-temperature retention can be enhanced. Another MONOS memory device fabricated to improve both the retention time

and the programming speed was a memory structure based on the band engineering considerations of HfO_2 for the tunneling and blocking layer and Ta_2O_5 for the charge storage layer[17]. It was observed that the device with HfO_2 which has low charge barrier height and Ta_2O_5 which has deep-trap energy level and proper band offset alignments was able to achieve faster programming and better retention performance simultaneously. The retention decay rate of this device is improved by a factor more than three as compared to the conventional SONOS type devices.

In 2008, a novel charge-trap-engineered flash NVM device was proposed with the structure of p-Si/SiO_2/$LaAlO_3$/HfON/Si_3N_4/$LaAlO_3$/SiO_2/metal, combining a 5 nm Si_3N_4 with a 0.9 nm equivalent oxide thickness (EOT) layer of HfON, within double-barrier and double-tunnel layers. This device shows good retention and a large memory window. At 150 °C and ±16 V program/erase, the device showed a program/erase speed of 100 μs, an initial ΔV_{th} window of 5.6 V and extrapolated 10 year retention of 3.8 V. These results are much better than those of a control charge trap flash device with a single Si_3N_4 trapping layer, which had a smaller initial ΔV_{th} and poorer 10-year retention.

In 2010, a cubic ZrO_2 film was investigated as the charge-trapping layer for nonvolatile memory formed by annealing of amorphous ZrON [11]. The memory with a nitrogen-stabilized cubic ZrO_2 film shows promising performance in terms of 3.81 V hysteresis memory window by ± 7 V program/erase voltage and 1.98 V flat-band voltage shift by programming at +7 V for 10 ms. Improved performance is mainly due to the greatly enhanced *k*-value of 32.8 and the increased trapping sites provided by grain boundaries.

Rare-earth oxides such as Tb_2O_3 and Y_2O_3 have attracted much interest in research for complementary metal oxide semiconductor (CMOS) applications of high-*k* materials and are attractive candidates for the trapping layer memory because of good thermodynamic stability, their large energy band gaps, a large conduction band offset with regard to silicon, and high

dielectric constants. A metal-oxide-high-κ-oxide-silicon (MOHOS) memory structure with high-κ Tb_2O_3 charge-trapping layer has been investigated[18]. The device annealed at 800 °C exhibited large threshold voltage shift, with memory window of 1.41 V operated at V_g = 8 V at 0.1 s, good data retention with charge loss of 10% measured time up to 10^4 s and at 85 °C, and good endurance characteristics with program/erase cycles up to 10^5 due to charge trapping at deep trap level. This crystalline Tb_2O_3 has a high dielectric constant of 11.8. Another rare earth oxides, Y_2O_3, with a high dielectric constant of 18, a high conduction band offset over 2 eV, and a low lattice mismatch with silicon, was used as charge trapping layer in SONOS memory device[19]. This memory device exhibited large threshold voltage shift, good data retention with charge loss of ~4% measured time up to 10^4 s at room temperature, and good endurance characteristics with program/erase cycles up to 10^5 because of the higher probability for trapping charge carriers.

Among various high-*k* dielectrics, ternary compounds also have been investigated as charge trapping layer in memory devices, such as $SrTiO_3$ with its high dielectric constant of 140 and $BaTiO_3$ with its high dielectric constant of higher than 100. $SrTiO_3$ has zero band-offset with respect to silicon which is desirable as charge trapping layer for memories to improve the program/erase speeds and retention property. Huang, et al incorporated nitrogen in $SrTiO_3$ resulted in more charges trap in the band gap through substitution of oxygen by nitrogen[20]. This nitrided $SrTiO_3$ has higher dielectric constant. Ti silicate between the CTL and SiO_2 can be suppressed by nitrogen passivation. The device with nitrided $SrTiO_3$ showed a larger memory window, higher program/erase speeds and good retention properties with charge loss of 38% after 10^4 s. Another ternary compound used as charge trapping layer is $BaTiO_3$ which has negative band offset with respect to Si, so it has a large barrier height relative to SiO_2. Huang et al reported that the isovalent substitution of Ti with Zr in $BaTiO_3$ in Zr-doped $BaTiO_3$ has been demonstrated to have higher program speed at low gate voltage, a

lower leakage current than $BaTiO_3$ while maintaining a comparable dielectric constant, better endurance, and good data retention with charge loss of 6.4% at 150°C for 10^4 s)[21]. Zr-doped $BaTiO_3$ exhibited higher charge-trapping efficiency and higher density of traps.

1.3.3 Issues and Challenges of Research utilizing High-κ Dielectric Materials as Charge Traping Layers

High-κ dielectrics are highly considered for CTM upon continually scaling down of the dimensions of flash memory. The using of high-κ dielectrics makes it possible for continual down-scaling of the cell size due to the advantage of using high-κ dielectrics which is the high-κ dielectrics can have a thicker physical thickness than silicon dioxides for the same equivalent oxide thickness (EOT). As charge trapping layers, high-κ dielectrics have to answer some challenges. High-κ dielectrics should have sufficient densities of trap states and deep trap energy levels which give rise to better data retention. High-κ dielectrics also should have a wide conduction band offset with respect to the tunneling oxide to prevent the charge leak out from the shallow trap levels in high-κ dielectrics. In addition, high-κ dielectrics have to possess good thermodynamic stability and good compatibility with current semiconductor technologies.

To fabricate the device structure beyond 25 nm technology for electronic purposes, the roughness among layers and the uniformity of the thickness also become major concern. The capability of fabrication technology to deposit semiconductor materials on top of one another with virtually no interface traps is necessary.

To explain the charge trapping characteristic in memory devices, it is essential to evaluate the energy band parameters of each layer in the structure, including the band gap and barrier heights, which include valence band offset (VBO) and conduction band offset (CBO). Some works on the study of charge trapping characteristics evaluated the interfacial barriers using the bulk parameters of solids which can be misleading since the bulk parameters may

not necessarily reflect the properties of thin films.

In our preliminary works, it is found that as-deposited capacitor structure with amorphous high-κ as charge trapping layer did not trap electrons during inversion step, but it trap holes during accumulation step in capacitance – voltage (C – V) measurement. The charge trapping in high-κ is related to the presence of the electronic defects. This issue of charge trapping should be explained after evaluating the device structures and energy band parameters.

1.4 What to Propose and the Purpose of the Research

To fulfil the requirements of the next generation of non-volatile memory devices, which are low programming voltage, low leakage current, and good retention characteristics for over 10 years, high-κ Al_2O_3/HfO_2 nanolaminates as charge trapping layer in metal gate electrode – Al_2O_3 – high – SiO_2 – p-type Si substrate (MAHOS) structure is proposed. By utilizing nanolaminates as charge trapping layer, heterojunction formed between two dissimilar semiconductors is created to get unique properties provided by the difference in energy gap, which can be seen in Figure 1.7. HfO_2 is believed to have deep trap level and has smaller conduction and valence band offset with respect to Si substrate, so the charges can be trapped with lower programming voltage and faster erase speed can be achieved. Al_2O_3 is used to modulate charge trapping distribution. Since it has wider bandgap and band offset with respect to Si than those of HfO_2, it is hoped that the retention properties can be improved.

Before explaining the charge trapping characteristics in the device structure, the evaluation of the microstructure and chemical state is also proposed to answer the device fabrication issue. In addition, the measurement of energy band parameters will be conducted to to analyze the charge transport mechanisms across the semiconductor structure.

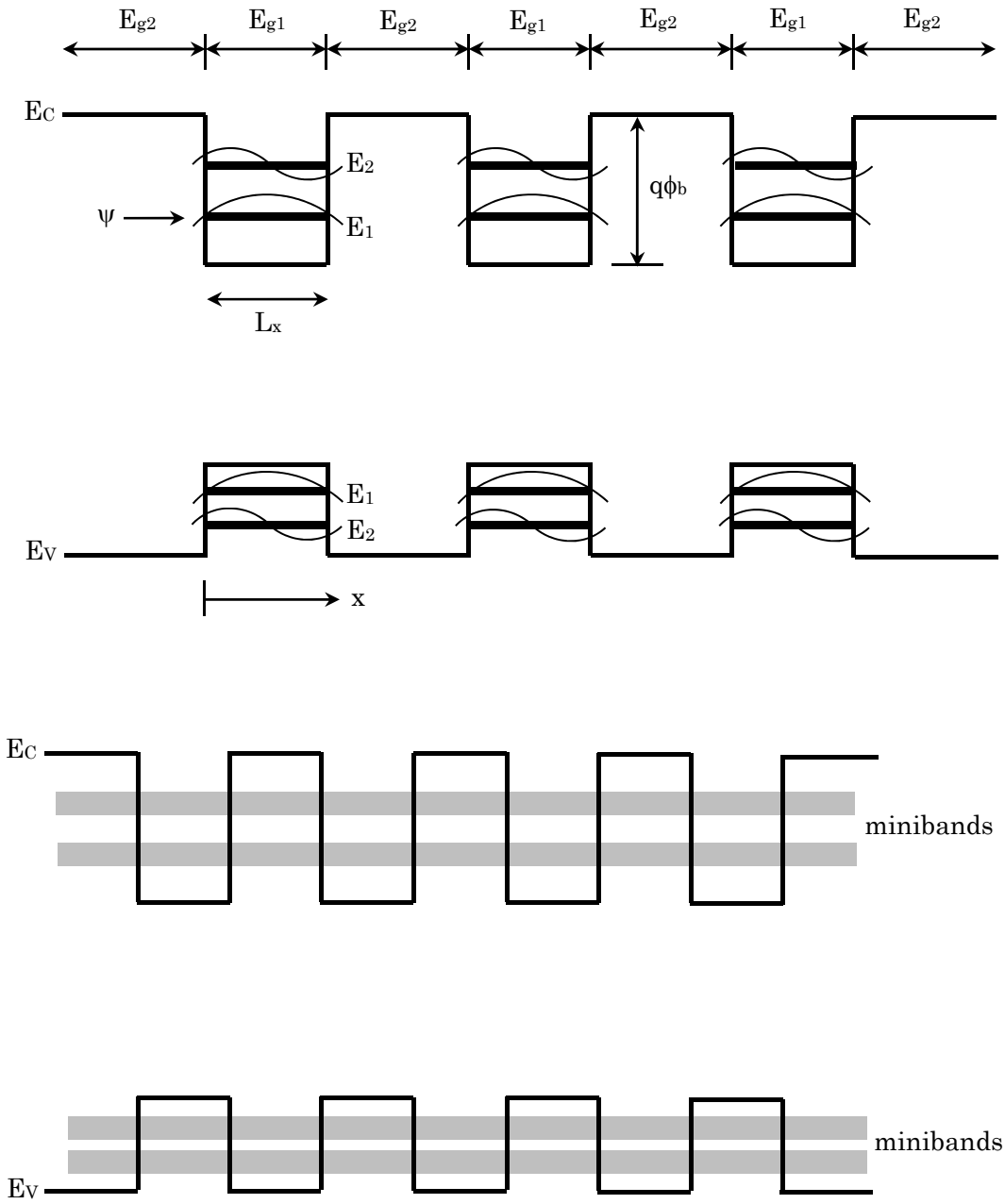


Figure 1.7 Energy-band diagrams for (a) heterostructure with multiple quantum wells and (b) heterostructure superlattice[22].

By considering the background discussed in the previous section which includes the motivation, current status, and challenges, the main goal of this research is to investigate the charge trapping characteristics in the MAHOS capacitor structure with high-κ dielectric nanolaminates and high-κ dielectrics as charge trapping layer for non-volatile memory application beyond 25 nm technology.

To achieve the main goal, this research is divided into four works based on their specific objectives mentioned as follow:

1. To fabricate and to evaluate the MAHOS capacitor structures by high resolution transmission electron microscopy (HR-TEM), x-ray photoelectron spectroscopy (XPS), and auger electron spectroscopy (AES). (Chapter 2)
2. To investigate the energy band parameters, including bandgap, valence band offset, and conduction band offset, of materials in the MAHOS capacitor structures by reflection electron energy-loss spectroscopy (REELS) and x-ray photoelectron spectroscopy (XPS). (Chapter 3)
3. To investigate the memory fuction of the as-deposited MAHOS capacitor structures by inductance – capacitance – resistance (LCR) meter and semiconductor analyzer system. (Chapter 4)
4. To investigate the memory fuction of the annealed MAHOS capacitor structures by inductance – capacitance – resistance (LCR) meter and semiconductor analyzer system. (Chapter 5)

1.5 Thesis Organization

This Dissertation consists of 6 chapters, including:

Chapter 1: “Introduction”. The basic of non-volatile memory is described and the role of high-κ dielectric materials for non-volatile memory application is reviewed. The background

of this research which includes the motivation, current status of the research, and some challenges is described. The research purpose which would be the centerpiece of our work is stated.

Chapter 2: “Device Fabrication and Structural Properties Characterizations”. The fabrication of MAHOS capacitor structures for non-volatile memory application, which involves Radio Corporation America (RCA) cleaning, rapid thermal oxidation (RTO), atomic layer deposition (ALD), rapid thermal annealing (RTA), and thermal evaporation, is explained. The microstructures of the MAHOS capacitor structures, which also include the interface and roughness, is evaluated by high-resolution transmission electron microscope (HRTEM). The chemical states and the binding energy of materials in the structure are evaluated by x-ray photoemission spectroscopy (XPS) and auger electron spectroscopy (AES).

Chapter 3: “Energy Band Alignment of the MAHOS Memory Capacitors”. The energy band parameters, such as band gap, valence band offset (VBO) and conduction band offset (CBO) are obtained from experimental results. The energy band gap of materials is observed by reflection energy electron loss spectroscopy (REELS) and the VBO and CBO are obtained from the x-ray photoelectron spectroscopy (XPS) spectra. The energy band alignment of each MAHOS structure is drawn. The effect of the dipole formation on the band structure at semiconductor/semiconductor interfaces is also explained.

Chapter 4: “Charge Trapping in Capacitor Structures with As-deposited High-κ Dielectric Materials as Charge Trapping Layers”. The charge trapping properties of as-deposited MAHOS capacitor structures are explained by evaluating, leakage current density – electric field characteristics, high frequency (1 MHz) capacitance – voltage (C – V) characteristics. The neutral flatband voltage is analyzed. The charge transport mechanism is explained by considering energy band diagram of the structures.

Chapter 5: “Charge Trapping in Capacitor Structures with Annealed High- Dielectric

Materials as Charge Trapping Layers". The charge trapping characteristics of annealled MAHOS capacitor structures are investigated from high frequency (1 MHz) capacitance – voltage (C – V) measurement results. The charge transport mechanism is analyzed from leakage current density measurement. The energy band diagram of the capacitor structures is also considered in explaining the charge injection. The difference in charge trapping characteristics between as-deposited MAHOS structures and annealed MAHOS structures is discussed.

Chapter 6: "Conclusions dan Recommendation for Future Works". This chapter concludes the whole research works and states some reccommendation for future works.

References

[1] Brewer, J.; Gill, M. Nonvolatile Memory Technologies with Emphasis on Flash: A Comprehensive Guide to Understanding and Using NVSM Devices; IEEE Press: Piscataway, NJ, USA, 2008.

[2] D.Khang and S.M.Sze. A floating gate and its application to memory devices. Bell Sys.Tech.j., vol.46, p.1288, 1967.

[3] John Robertson. Band offsets of wide-band-gap oxides and implications for future electronic devices. J. Vac. Sci. Technol. B 18, 1785 (2000).

[4] Lee, C.H.; Hur, S.H.; Shin, Y.C.; Choi, J.H.; Park, D.G.; Kim, K. Charge trapping device structure of SiO_2/SiN/high-k dielectric Al_2O_3 for high-density flash memory. Appl. Phys. Lett. 2005, 86.

[5] Pu, J.; Chan, D.S.; Kim, S.-J.; Cho, B.J. Aluminum-doped gadolinium oxides as blocking layer for improved charge retention in charge-trap-type nonvolatile memory devices. IEEE Trans. Electron Devices 2009, 56, 2739–2745.

[6] He, W.; Pu, J.; Chan, D.S.; Cho, B.J. Performance improvement in charge-trap flash memory using lanthanum-based high-k blocking oxide. IEEE Trans. Electron Devices 2009, 56, 2746–2751.

[7] Huang, X.D.; Liu, L.; Xu, J.P.; Lai, P.T. Improved performance of yttrium-doped Al2O3 as inter-poly dielectric for flash-memory applications. IEEE Trans. Device Mater. Rel. 2011, 13, 490–494.

[8] Lue, H.-T.; Wang, S.-Y.; Lai, E.-K.; Shih, Y.-H.; Lai, S.-C.; Yang, L.-W.; Chen, K.-C.; Ku, J.; Hsieh, K.-Y.; Liu, R.; *et al*. BE-SONOS: A bandgap engineered SONOS with excellent performance and reliability. In *Proceedings of IEEE International IEDM Technical Digest Electron Devices Meeting*, Washington, DC, USA, 5 December 2005; pp. 547–550.

[9] Govoreanu, B.; Blomme, P.; Rosmeulen, M.; van Houdt, J.; de Meyer, K. VARIOT: A novel multilayer tunnel barrier concept for low voltage nonvolatile memory devices. *IEEE Electron Device Lett.* 2003, *24*, 99–101.

[10] White, M.H.; Adams, D.A.; Bu, J. On the go with SONOS. *IEEE Circuits Devices Mag.* 2000, *16*, 22–31.

[11] Wu, Y.H.; Chen, L.L.; Wu, J.R.; Wu, M.L.; Lin, C.C.; Chang, C.H. Nonvolatile memory with nitrogen-stabilized cubic-phase ZrO_2 as charge-trapping layer. *IEEE Electron Device Lett.* **2010**, *31*, 1008–1010.

[12] J. Robertson. High dielectric constant gate oxides for metal oxide Si transistors. Rep. Progress in Physics, vol. 69, pp. 327 – 390, 2006.

[13] International Technology Roadmap for Semiconductors: Process Integration, Devices and Structures. **2009**. http://www.itrs.net/Links/2009ITRS/Home2009.htm.

[14] Tan, Y.N.; Chim, W.K.; Choi, W.K.; Joo, M.S.; Byung, J.C. Hafnium aluminum oxide as charge storage and blocking-oxide layers in SONOS type nonvolatile memory for high-speed operation. *IEEE Trans. Electron Devices* **2006**, *53*, 654–662.

[15] You, H.-W.; Cho, W.-J. Charge trapping properties of the HfO2 layer with various thicknesses for charge trap flash memory applications. Appl. Phys. Lett. 2010, 96, 093506:1–093506:3.

[16] Yang, H.J.; Cheng, C.F.; Chen, W.B.; Lin, S.H.; Yeh, F.S.; McAlister, S.P.; Chin, A. Comparison of MONOS memory device integrity when using $Hf_{1-x-y}N_xO_y$ trapping layers with different N compositions. *IEEE Trans. Electron Devices* **2008**, *55*, 1417–1423.

[17] Wang, X.; Liu, J.; Bai, W.; Kwong, D.-L. A novel MONOS-type nonvolatile memory using high-*k* dielectrics for improved data retention and programming speed. *IEEE Trans. Electron Devices* **2004**, *51*, 597–602.

[18] Pan, T.-M.; Jung, J.-S.; Chen, F.-H. Metal-oxide-high-k-oxide-silicon memory structure incorporating a Tb_2O_3 charge trapping layer. *Appl. Phys. Lett.* **2010**, *97*, 012906:1–012906:3.

[19] Pan, T.-M.; Yeh, W.-W. High-performance high-*k* Y_2O_3 SONOS-type flash memory. *IEEE Trans. Electron Devices* **2008**, *55*, 2354–2360.

[20] Huang, X.D.; Lai, P.T.; Liu, L.; Xu, J.P. Nitrided $SrTiO_3$ as charge-trapping layer for nonvolatile memory applications. *Appl. Phys. Lett.* **2011**, *98*.

[21] Huang, X.D.; Sin, J.K.O.; Lai, P.T. Improved Charge-Trapping Characteristics of $BaTiO_3$ by Zr Doping for Nonvolatile Memory Applications. *IEEE Electron Device Lett.* **2013**, *34*, 499–501.

[22] S. M. Sze and Kwok K. Ng. Physics of Semiconductor Devices, Third Edition. 2007. John Wiley & Sons, Inc.

Chapter 2

Device Fabrication and Structural Properties Characterizations

In chapter 2, the experimental procedures on the fabrication of the MAHOS capacitor structures will be described. The process flow of the device fabrication, including Radio Corporation America (RCA) cleaning, rapid thermal oxidation (RTO), atomic layer deposition (ALD), rapid thermal annealing (RTA), and thermal evaporation, will be explained. The microstructures and the chemical states of the MAHOS capacitor structures will be evaluated. Structural properties of the devices were characterized by high-resolution transmission electron microscope (HRTEM) and chemical states of the devices are characterized by x-ray photoemission spectroscopy (XPS) and auger electron spectroscopy (AES).

2.1 Design Consideration of MAHOS Capacitor Structures

In this research, the MAHOS capacitor structure was designed as memory structure for non-volatile memory application. For this application, the MAHOS capacitor structures consists of Aluminum as gate electrode, Al_2O_3 as blocking oxide, high-κ dielectric materials as charge trapping layer, SiO_2 as tunneling layer, and p-type Silicon substrate. For tunneling oxide and blocking oxide, the energy barriers for electrons (Φe) and holes (Φh) at the metal gate/oxide and Si/oxide interfaces must be sufficiently high to suppress the tunneling effect[1]. It is required that the potential barrier at each band is higher than 1 eV to inhibit conduction by the Schottky emission of electrons or holes into the oxide bands[2]. SiO_2 was selected as tunneling oxide since it is an excellent insulator with amorphous structure, large band gap of about 8.9 eV with high barriers for both electrons and holes, and very few electronic defects[3,4]. SiO_2 is thermally grown on Si substrate with excellent interface with Si. High-κ

dielectric Al_2O_3 is used as blocking oxide. Using high-κ dielectric materials as blocking oxide increases the electric field across the tunnel oxide and charge-storage layers and decreases the electric field across the blocking oxide layer at the same time which results in increase in the program and erase speeds and improve the retention characteristics[5,6,7]. For charge trapping layer, high-κ dielectric materials were used since they have electronic defects which can trap charges due to possessing ionic bonding and high coordination number[8,9,10]. In this research, we will compare the charge trapping characteristics in Al_2O_3 single layer, the mixture of high-κ dielectric Al_2O_3 and HfO_2, and the nanolaminate structure of HfO_2/Al_2O_3. The nanolaminate structure as charge trapping layer created heterojunction structure with multiple quantum well.

The MAHOS capacitor structures prepared in this works are shown in table 2.1. The structures were prepared by applying certain methods to make sure that the high quality MAHOS structures can be fabricated. The process flow of the MAHOS capacitor fabrication is shown in figure 2.1. In this chapter, the MAHOS structures are evaluated by HRTEM, XPS, and AES.

2.2 Fabrication of MAHOS Capacitor Structures

2.2.1 RCA Cleaning Process

The Radio Corporation America (RCA) cleaning process is a standard set of silicon wafer cleaning in semiconductor manufacturing which needs to be performed before high temperature processing steps, such as thermal oxidation to grow SiO_2 and structure deposition[11,12]. Based on the purposes, there are three steps in RCA cleaning process, including the removal of organic contaminants (organic clean), the removal of thin SiO_2 layer (oxide strip), and the removal of ionic contamination (ionic clean).

Table 2.1 The MAHOS Capacitor Structures

The MAHOS Structure	RTA	Sample name
Al gate/Al_2O_3 (20 nm)/SiO_2 (3 nm)/p-type Si	no	A1
	yes	A2
Al gate/Al_2O_3 (10 nm)/HfAlO (10 nm)/SiO_2 (3 nm)/p-type Si	no	HA1
	yes	HA2
Al gate/Al_2O_3 (10 nm)/HfO_2 (2 nm)/ [HfO_2 (2 nm)/Al_2O_3 (2 nm)]$_2$/SiO_2 (3 nm)/p-type Si	no	NA1
	yes	NA2
Al gate/Al_2O_3 (10 nm)/HfO_2 (1 nm)/ [HfO_2 (1 nm)/Al_2O_3 (1 nm)]$_4$/SiO_2 (3 nm)/p-type Si	no	NB1
	yes	NB2

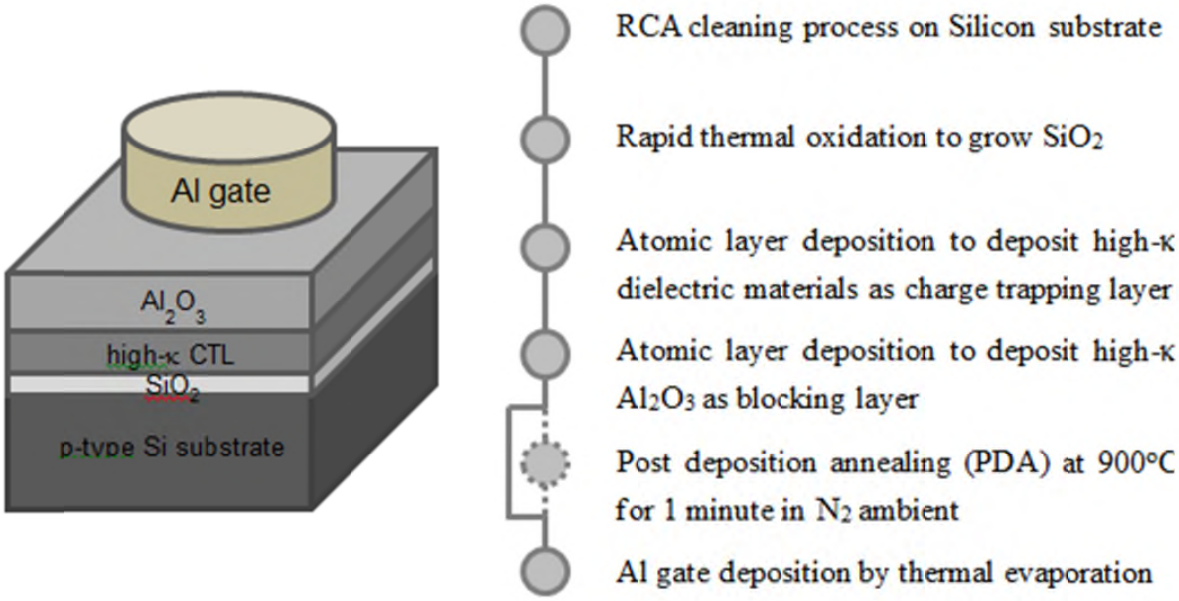


Figure 2.1 Process flow of the fabrication of the MAHOS capacitor structure.

For three different purposes, three chemical mixtures, including organic clean mixture, oxide strip mixture, and ionic clean mixture, are prepared. Organic clean mixture has to be made less than 45 minutes prior to being used. The mixture consists of 5 parts of DI water, 1 part of hydrogen peroxide (H_2O_2, 30%), and 1 part of ammonium hydroxide (NH_4OH, 28%). The solutions are poured into the beaker and stirred with clean teflon rod. The beaker is placed into the temperature-controlled water bath and the hotplate is adjusted to maintain the solution temperature at 50^{o}C. Oxide strip mixture consists of 30 parts of DI water and 1 part of hydrofluoric acid (HF, 49%). The solutions are poured into propylene beaker. Ionic clean mixture consists of 6 parts of DI water, 1 part of hydrogen peroxide (H_2O_2, 30%), and 1 part of hydrochloric acid (HCl, 37%). The solutions are poured into the beaker and the beaker is placed into the temperature-controlled water bath.

To clean the silicon wafer, the wafer is placed in teflon basket. Then, it is submerged in the organic clean solution for 10 minutes and heated to 50^{o}C. The basket with silicon wafer is removed from the bath and rinsed in the DI water for 1 minute. Then, the basket with wafer is submerged in the oxide strip solution for 15 seconds. After that, it is removed from the bath and rinsed in the DI water for 1 minute. Last, the basket with wafer is submerged in the ionic clean solution for 10 minutes and heated to 50^{o}C. The basket is removed from the bath and rinsed wafer in the DI water for 1 minute. Then, the basket is removed from the DI water and the silicon wafer is blown dry with nitrogen.

In our work, p-type silicon (100) wafers with a resistivity of 15 – 25 Ω.cm were used. RCA cleaning process was done on all Si substrates prior to thin film deposition.

2.2.2 Rapid Thermal Processing (RTP)

In this research, rapid thermal processing (RTP) was applied to grow high quality tunneling oxide, SiO_2, by rapid thermal oxidation (RTO) in O_2 and N_2 ambient and to anneal

the capacitor structures by rapid thermal annealing in N_2 ambient before Al gate electrode deposition was done.

When the SiO_2 is grown on Si substrate by thermal oxidation process, the oxidation process influences the distribution of impurities in the bulk of silicon and at the Si/SiO_2 interface. Since the movement of impurities affects the device size and its electrical properties, it is important to control and minimize the effects of oxidation on the impurity profile. This can be achieved by controlling the oxidation temperature precisely and reducing the thermal budget of the heat cycle required for an oxide film growth[13,14]. In this case, the conventional furnace oxidation has a limitation because its inertia to temperature transition will result in a higher thermal budget than that required for oxidation. Decreasing the duration of these transitions can reduce the thermal budget considerably. Rapid thermal processing (RTP) offers a process with smaller thermal budget so it can reduce the effects of oxidation on the impurity profile, as shown in figure 2.2.

During RTP, the silicon wafer is rapidly heated from room temperature to a high processing temperature ($T > 800^oC$) with temperature transition rates range from 10 to $350^oC/s$, compared with about $0.1^oC/s$ for furnace processing. The wafer is held at high temperature for a short time, varies from 1s to 5 minutes and then cooled down rapidly to a low temperature. By rapid heating and rapid cooling down, RTP reduces the ramp-up and ramp-down durations. Due to its superior process and operational flexibility, RTP is commonly used in semiconductor device manufacturing fabrications and is suitable to grow thin oxide films with thickness less than 40 nm, where a precise temperature control and short oxidation times are important[15,16].

An RTP system is single-wafer furnace, only one wafer is in the chamber and processed. A schematic cross-section of RTP system which is a single wafer rapid thermal

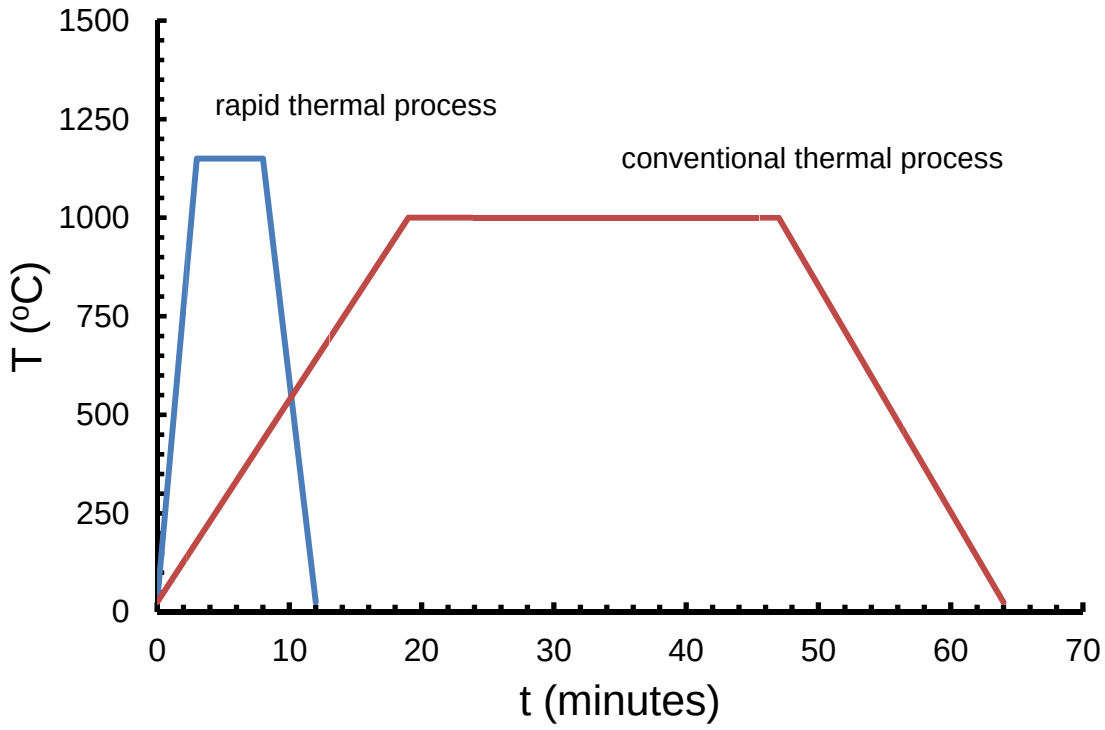


Figure 2.2 The thermal budget reduction in rapid thermal processing.

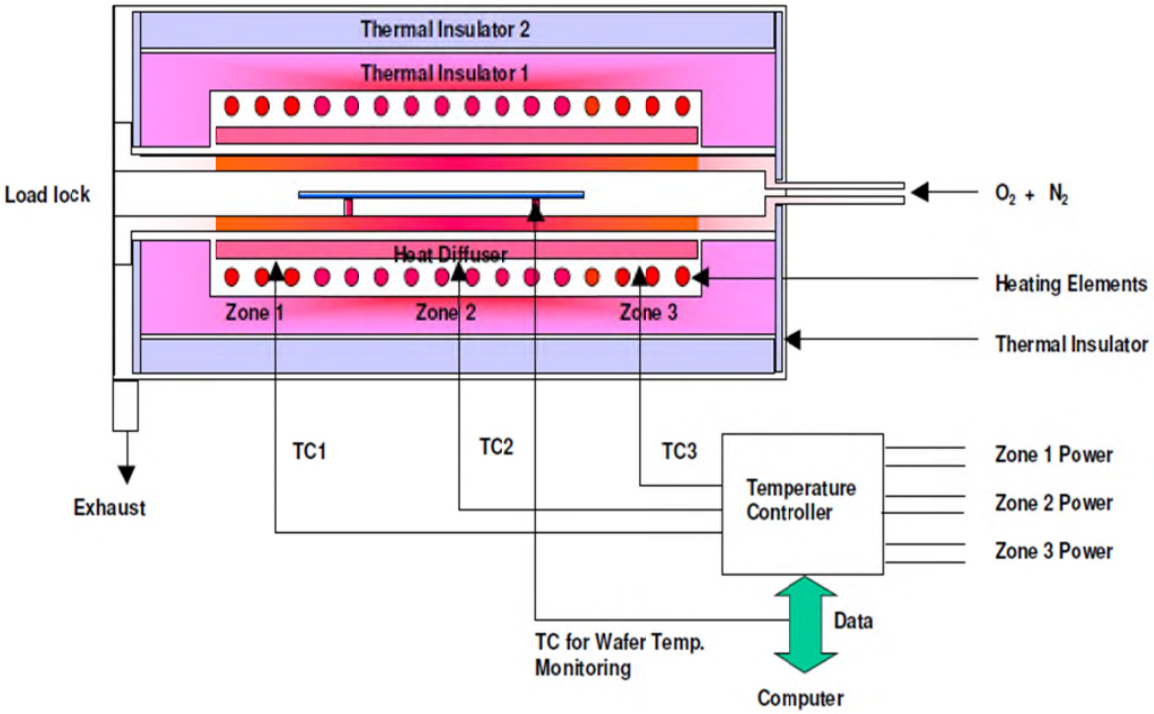


Figure 2.3 A schematic cross-section of single wafer rapid thermal furnace (SWRTF).

furnace (SWRTF) is shown in Fig. 2.3. The heat source is typically an array of tungsten halogen lamps in an optical system.

After RCA cleaning process, high quality tunneling layer, SiO_2, was grown on p-type Si substrate by RTO in O_2 ambient with a design thickness of 3 nm. RTA was done on the structure after charge trapping layer and blocking layer deposition in N_2 ambient. The RTP parameters for thermal oxidation and post deposition annealing can be seen in table 2.2.

2.2.3 Atomic Layer Deposition (ALD)

Atomic layer deposition (ALD) is a chemical gas phase thin film deposition method in which thin film is grown through sequential saturative surface reactions that are realized by pulsing the two (or more) precursors into the reactor alternatively, one at a time, separated by purging or evacuation steps[17]. The reactions in ALD are saturative which makes the film growth self-limiting that, in turn, gives the method a number of advantages. The self-limiting growth ensures that each cycle deposits the same amount of material on all surfaces independent of the precursor dose received as long as the dose is high enough to saturate the reactions. As a consequence, the ALD method offers excellent large area uniformity and conformality. In addition, film thicknesses are accurately controlled simply by the number of deposition cycles applied. This makes it also straightforward to tailor film composition at an atomic layer level. Preparation of multicomponent and multilayer materials is further facilitated by the fact that process temperature windows are often reasonably wide so that binary processes are easy to combine.

Successful utilization of ALD is dependent on two factors, including proper precursors and fast and efficient reactors. The precursors must be volatile enough to ensure efficient transportation for saturating the surface reactions. The precursors and the surface species formed thereof do not decompose thermally on their own to maintain atomic level accuracy in film thickness control and uniformity. The precursor dosed onto the substrate

should react rapidly with the surface species left from the previous precursor pulse to achieve fast saturation in each reaction step. Another related requirement is that the reactions should be complete to provide high film purity. Precursors should not etch the material formed during the deposition process. The by-products formed in the surface exchange reactions should be unreactive so that they can be easily purged away from the reactor.

In our research, the high-κ trapping layers, including Al_2O_3, HfAlO, and (HfO_2/Al_2O_3) nanolaminates and Al_2O_3 blocking layer were deposited on SiO_2/p-type Si substrate by ALD. The designed thickness of charge trapping layer and blocking layer for each MAHOS structures can be seen in Table 2.2. High-κ Al_2O_3 and HfO_2 were deposited at a substrate temperature of 300^oC by using tri-methylaluminium [$Al(CH_3)_3$] and hafnium tetrachloride ($HfCl_4$) precursors, respectively. The precursor temperatures were 23^oC for $Al(CH_3)_3$ and 185^oC for $HfCl_4$. The H_2O was used as an oxidant precursor.

Flow-type reactor was used in this research. The first precursor gas was introduced into the process chamber and produces a monolayer of gas on the wafer surface. A second precursor of gas was then introduced into the chamber reacting with the first precursor to produce a monolayer of film on the wafer surface. There are two fundamental mechanisms during atomic layer deposition, including chemisorption saturation process and sequential surface chemical reaction process.

In air, H_2O vapor is adsorbed on most surfaces, forming a hydroxyl group. The hydroxyl group form $Si\text{-}O\text{-}H_{(s)}$ with SiO_2. After placing the substrate in the reactor, for Al_2O_3 deposition, trymethyl aluminum, $Al(CH_3)_3$ (TMA) is pulsed into the reaction chamber. TMA reacts with the adsorbed hydroxyl groups, producing methane as the reaction product.

$$Al(CH_3)_{3(g)} + :Si\text{-}O\text{-}H_{(s)} \rightarrow :Si\text{-}O\text{-}\ Al(CH_3)_{2(s)} + CH_{4(g)}$$

TMA reacts with the adsorbed hydroxyl groups until the surface is passivated. TMA does not react with itself, terminating the reaction to one layer which causes the uniformity of

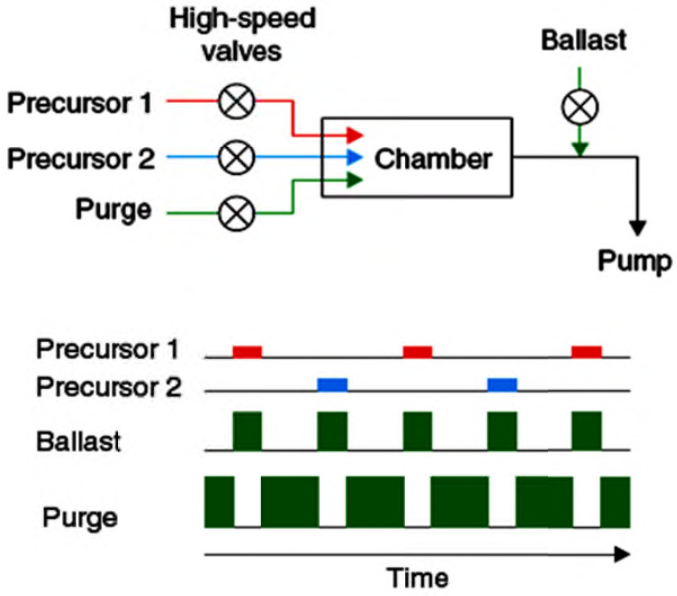


Figure 2.4 (a) A schematic diagram of atomic layer deposition (ALD) system and (b) Gas flow as a function of time in ALD system.

ALD. The excess of TMA is pumped away with the methane reaction product. After the TMA and methane reaction product is pumped away, water vapor (H_2O) is pulsed into the reaction chamber. H_2O reacts with the dangling methyl groups on the new surface forming aluminum oxygen (Al-O) bridges and hydroxyl surface groups, waiting for a new TMA pulse. Methane is also the product after this reaction.

$$2H_2O_{(g)} + :Si\text{-}O\text{-}\ Al(CH_3)_{2(s)} \rightarrow :Si\text{-}O\text{-}\ Al(OH)_{2(s)} + 2CH_{4(g)}$$

The reaction product, methane, is pumped away. Excess H_2O vapor does not react with the hydroxyl surface groups which cause perfect passivation to one atomic layer. One TMA and one H_2O vapor pulse form one cycle.

For HfO_2 deposition, hafnium tetrachloride, $HfCl_4$ (HTC) was used as precursor with H_2O as oxidant precursor. One HTC and one H_2O vapor pulse form one cycle. There are two reaction steps in one cycle, including

$$HfCl_{4(g)} + 2{:}Si\text{-}O\text{-}H_{(s)} \rightarrow :(Si\text{-}O)_2\text{-}HfCl_{2(s)} + 2HCl_{(g)}$$

$$2H_2O_{(g)} + :(Si\text{-}O)_2\text{-}HfCl_{2(s)} \rightarrow :(Si\text{-}O)_2\text{-}Hf(OH)_{2(s)} + 2HCl_{(g)}$$

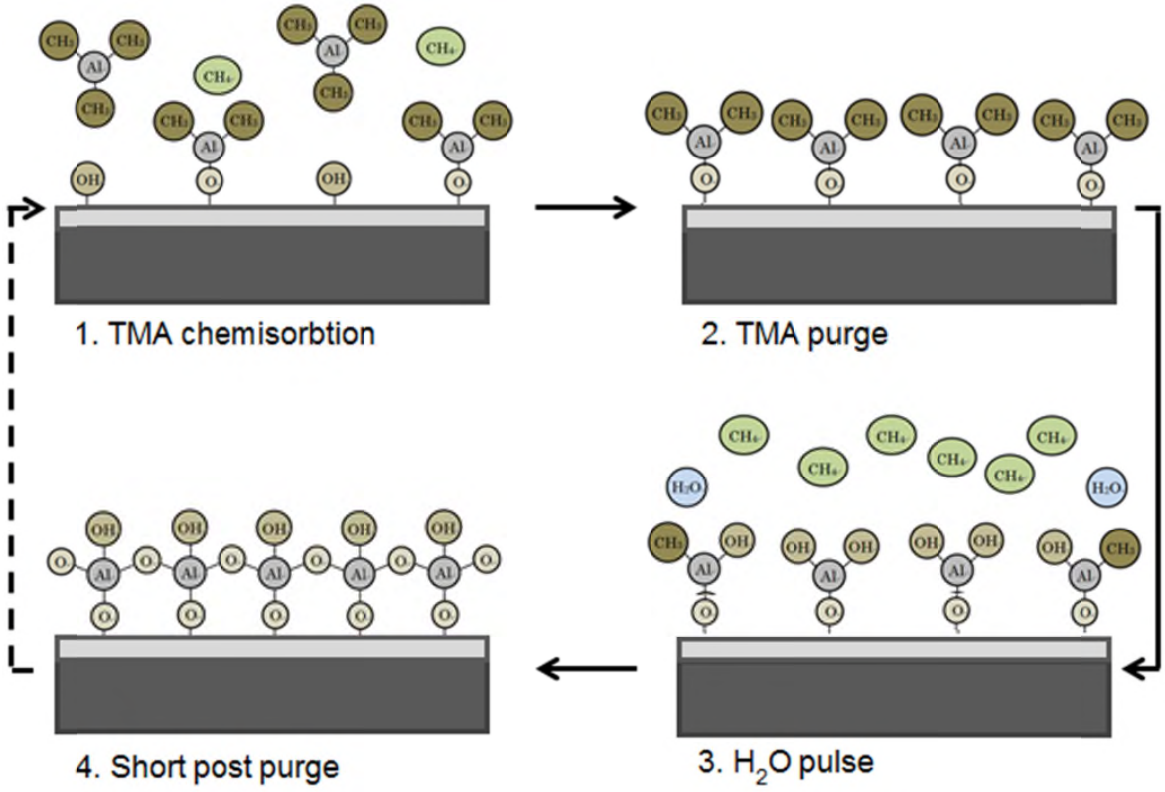


Figure 2.5. Two reaction steps in one cycle during Al_2O_3 deposition process by ALD.

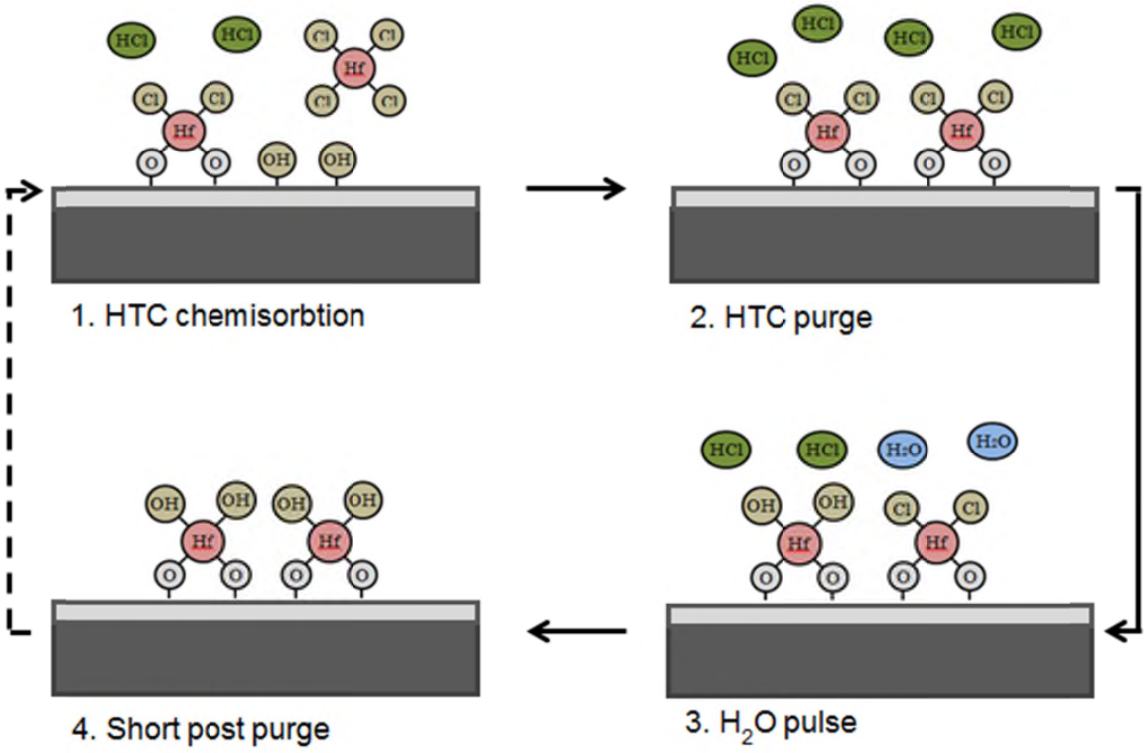


Figure 2.6. Two reaction steps in one cycle during HfO_2 deposition process by ALD.

2.2.4 Thermal Evaporation

Evaporation is based on the concept that there exists a finite “vapor pressure” above any material. Thermal evaporation is a simple physical vapor deposition method comprises evaporating source materials in a vacuum chamber below 1×10^{-6} torr (1.3×10^{-4} Pa) and condensing the evaporated particles on a substrate. Resistive heating is most commonly used for the deposition of thin films. The temperature of the source material is raised in an open boat or suspended on a wire so that the material evaporates or sublimes onto the substrate. The resistively heated wire or boat, generally made of high temperature or refractory metals such as W, Mo, or Ta and they must not react adversely with the evaporant. Crucibles of quartz, graphite, alumina, beryllia, boron-nitride, or zirconia are used with indirect heating. The refractory metals are evaporated by electron-beam deposition since simple resistive heating cannot evaporate high melting point materials.

In this work, thermal evaporation was used to deposit Al as gate electrode in the MAHOS structure. Shadow mask was put on the structure to get the individual gate area of 3.14×10^{-4} cm^2. The deposition rate was controlled to be nm/minutes with the design thickness of 200 nm.

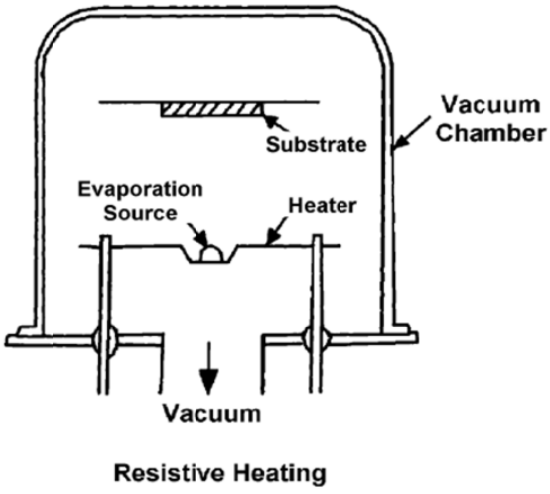


Figure 2.7. Schematic diagram of resistive heating thermal evaporation.

Table 2.2 Experimental Parameters of the MAHOS Capacitor Structure Fabrication

A. Rapid Thermal Oxidation (RTO)	
Oxidation temperature ($T_{oxidation}$)	
Oxidation time ($t_{oxidation}$)	
Base pressure (P_{base})	
Working pressure ($P_{working}$)	
Gas flows	
B. Atomic Layer Deposition (ALD)	
Substrate temperature ($T_{substrate}$)	
Precursor for Al_2O_3	
Precursor for HfO_2	
Oxidant precursor	
Working pressure ($P_{working}$)	
C. Post Deposition Annealing (PDA) or RTA	
Oxidation temperature ($T_{oxidation}$)	
Oxidation time ($t_{oxidation}$)	
Base pressure (P_{base})	
Working pressure ($P_{working}$)	
Gas flows	
D. Thermal Evaporation of Al	
Base pressure (P_{base})	
Working pressure ($P_{working}$)	
Working power	
Deposition rate and Gas flows	

2.3 Structural Properties and Chemical States of the MAHOS Capacitor Structures

Observing the microstructure image and analyzing the chemical states of the MAHOS capacitor structures is important not only to evaluate all processes involved in the structure fabrication but also to explain the relationship between their structural properties, energy band alignment, and charge trapping characteristics. This part explains the basic principle of the characterization methods used to evaluate the microstructure and chemical state of the structures.

2.3.1 Structural Properties Characterized by HRTEM

a. Basic Principle of Structural Observation by HRTEM

In a transmission electron microscope (TEM) (Fig. 1.1), a thin specimen is irradiated with an electron beam of uniform current density. The acceleration voltage is about 300 kV. Electrons are emitted in the electron gun by field emission. A three- or four-stage condenser-lens system permits variation of the illumination aperture and the area of the specimen illuminated. The electron intensity distribution behind the specimen is imaged with a lens system, composed of three to eight lenses, onto a fluorescent screen. The image can be recorded digitally via a fluorescent screen coupled by a fiber-optic plate to a CCD camera.

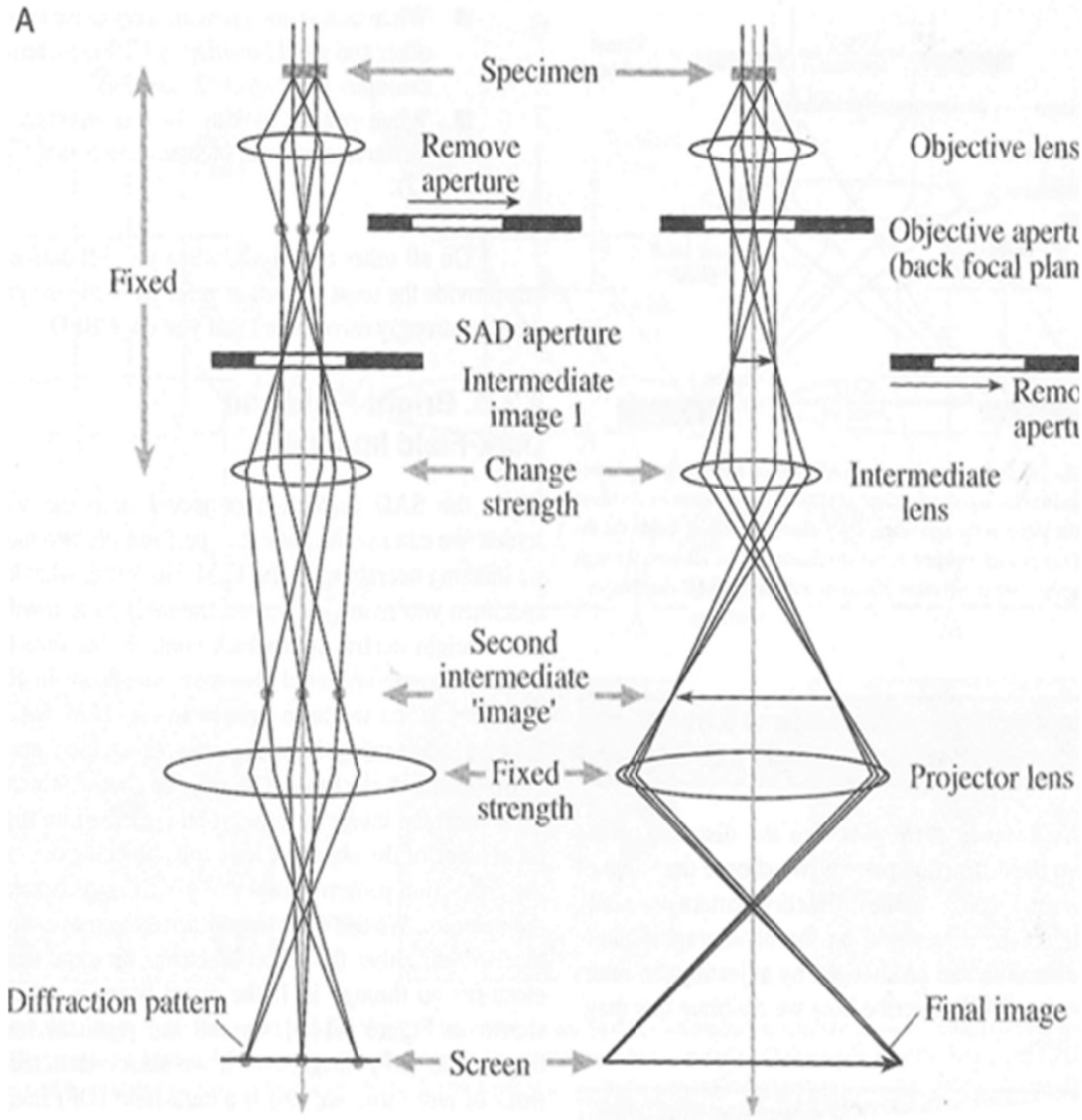
b. TEM Sample Preparation and Observation

Electrons interact strongly with atoms by elastic and inelastic scattering. The specimen must therefore be very thin, typically of the order of 5–100 nm depending on the density and elemental composition of the object and the resolution desired. Special preparation techniques are needed.

2.3.2 Chemical State Identification by XPS and AES

a. Chemical Bonding Observation by X-ray Photoelectron Spectroscopy (XPS)

Material characterization by XPS is conducted with a special form of photoemission which is the ejection of an electron from a core level by an X-ray photon of energy hv. The



Diffraction Pattern Image

Figure 2.8 Schematic diagram of the XPS process, showing photoionization of an atom by the ejection of a 1s electron

energy of the emitted photoelectrons is then analysed by the electron spectrometer and the data presented as a graph of intensity versus electron energy. The kinetic energy (E_K) of the electron is the experimental quantity measured by the spectrometer which is dependent on the photon energy of the X-rays. The binding energy of the electron (EB) is the parameter which identifies the electron specifically, both in terms of its parent element and atomic energy level. The relationship between the parameters involved in the XPS experiment is

$$E_B = \mathrm{hv} - E_K - W$$

where hv is the photon energy, E_K is the kinetic energy of the electron, and W is the spectrometer work function. The photoemission process is shown schematically in Figure 1.2, where an electron from the K shell is ejected from the atom (a 1s photoelectron). The photoelectron spectrum will reproduce the electronic structure of an element quite accurately since all electrons with a binding energy less than the photon energy will feature in the spectrum, as shown in figure 2.8.

Sample characterization by XPS was carried out by PHI 5000 VersaProbe II Scanning XPS Microprobe equipped with Al Kα (1486.6 eV) x-ray source. The high resolution spectra were collected with the pass energy of 23.5 eV and at a photoelectron take off angle of 90^o relative to the sample surface. The energy scale was calibrated by setting the binding energy of Ar 2p at 241.82 eV. The core level spectra were fitted by asymmetric Gaussian-Lorentzian sum function with a fixed spin orbit splitting. The Shirley background was added before fitting the peaks.

b. Chemical State Identification by Auger Electron Spectroscopy (AES)

In material characterization by auger electron spectroscopy (AES), a specimen is irradiated with electrons and core electrons are ejected in the same way that an X-ray beam will cause core electrons to be ejected in XPS. The difference between AES and XPS is that in the case of electron irradiation the secondary electrons contain no analytical information –

although those of low energy are very useful for imaging purposes as in scanning electron microscopy. However, once an atom has been ionized it return to its ground state.

The core hole, for example a K shell vacancy, may be filled by an electron from a higher level, the $L_{2,3}$ level in Figure 1.4. In order to conform with the principle of the conservation of energy, another electron must be ejected from the atom, e.g., another $L_{2,3}$ electron in the schematic of Figure 1.4. This electron is termed the $KL_{2,3}L_{2,3}$ Auger electron. The kinetic energy of a $KL_{2,3}L_{2,3}$ Auger electron is approximately equal to the difference between the energy of the core hole and the energy levels of the two outer electrons, $EL_{2,3}$

$$E_{KL_{2,3}L_{2,3}} = E_K - E_{L_{2,3}} - E_{L_{2,3}}$$

It is the kinetic energy of this Auger electron ($E_{KL_{2,3}L_{2,3}}$) that is the characteristic material quantity irrespective of the primary beam composition (i.e., electrons, X-rays, ions) or its energy. For this reason Auger spectra are always plotted on a kinetic energy scale. The use of a finely focused electron beam for AES enables us to achieve surface analysis at a high spatial resolution.

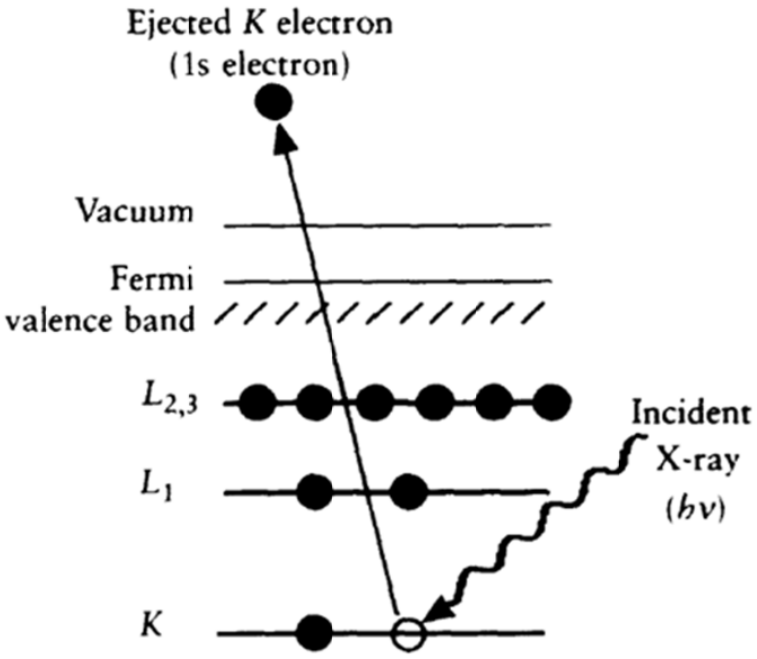


Figure 2.9 Schematic diagram of the XPS process, showing photoionization of an atom by the ejection of a 1s electron

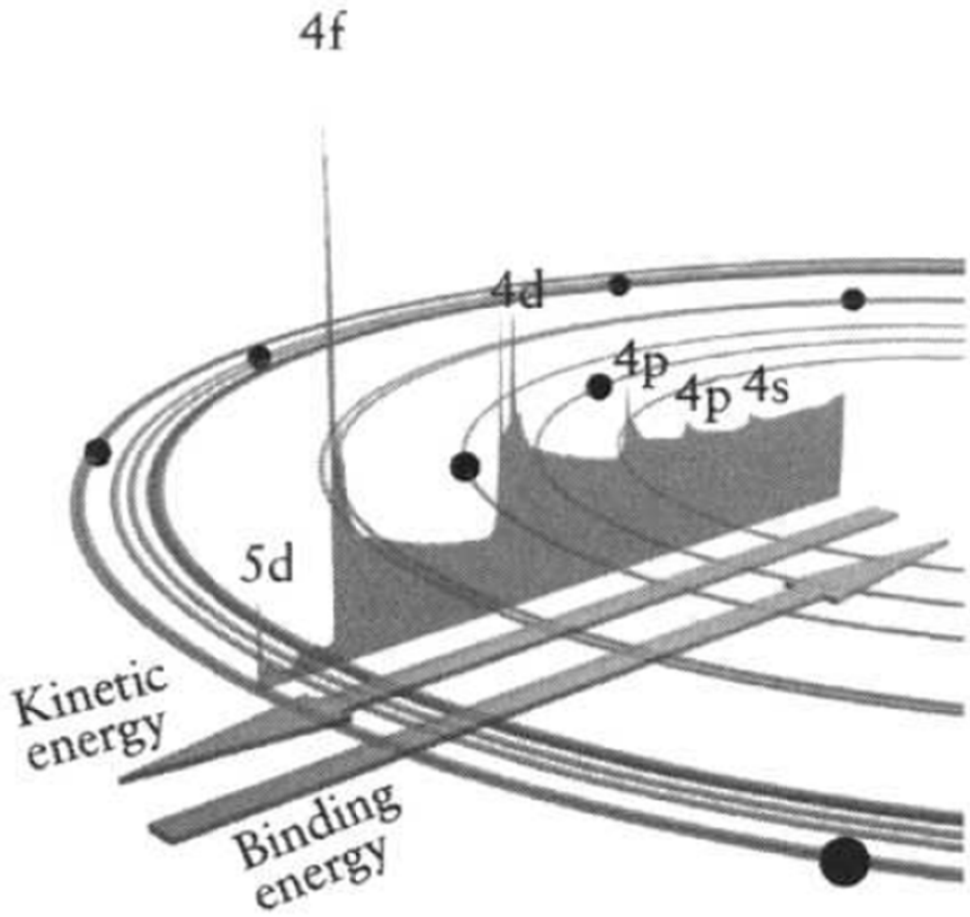


Figure 2.10 Schematic diagram of the XPS process, showing photoionization of an atom by the ejection of a 1s electron

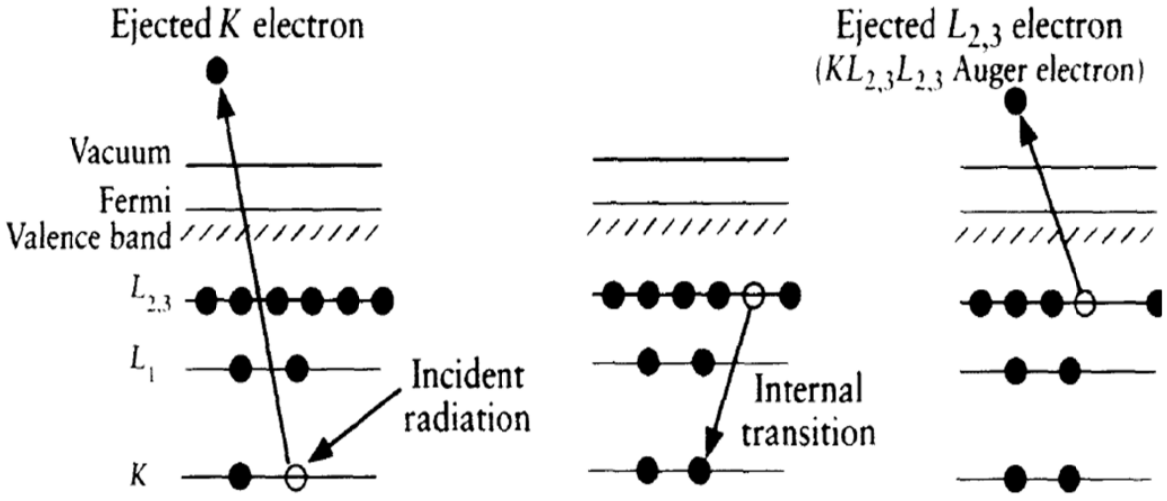


Figure 2.11 Relaxation of the ionized atom of Figure 1.2 by the emission of a $KL_{2,3}L_{2,3}$ Auger electron

2.4 Structural Properties and Chemical States of the MAHOS Capacitor Structures

2.4.1 SiO_2 Grown on p-type Si Substrate

Figure R2.1 – R2.4 shows cross sectional HRTEM images of the MAHOS capacitor structure with as-deposited Al_2O_3, HfAlO, $(HfO_2/Al_2O_3)_4/HfO_2$ nanolaminates, and $(HfO_2/Al_2O_3)_2/HfO_2$ nanolaminate as charge trapping layers. From the figures, high quality SiO_2 can be grown by thermal rapid oxidation after RCA cleaning on p-type Si substrate. The interface of thermally grown SiO_2 and Si has the roughness of about 1 – 2 monolayers of Si atoms. This high quality interface of SiO_2 and Si substrate is required in electronic structures since the carriers induced by the gate are induced within Angstroms of the Si-oxide interface. High quality interface guarantees that the number of interface defects can be minimized because the amorphous SiO_2 is able to configure its interface bonding.

Good interface condition between SiO_2 and Si is also confirmed by XPS spectra of Si 2p at the interface observed from 3 nm SiO_2/p-type Si, as shown in Figure R2.5, which can be deconvoluted into two peaks, including Si $2p_{SiO2}$ and Si $2p_{p\text{-type Si}}$. The core level spectra of Si 2p were fitted by a nonlinear Gaussian-Lorentzian line shape with a fixed spin orbital splitting between Si $2p_{1/2}$ and Si $2p_{3/2}$ to be 0.6 eV and an area ratio of 1 to 2[18]. The Si $2p_{SiO2}$ peak and Si $2p_{p\text{-type Si}}$ peak are located at 103.504 eV and 98.96 eV, respectively. The peak locations of Si $2p_{SiO2}$ and Si $2p_{p\text{-type Si}}$ are similar with those of bulk phases as also shown in Figure R2.5. The bulk Si $2p_{SiO2}$ of 40 nm SiO_2/p-type Si and the bulk of Si $2p_{p\text{-type Si}}$ of p-type Si substrate are located at 103.485 eV and 98.98 eV, respectively. The binding energy difference between the Si 2p and O 1s core levels of SiO_2 is about 429.5 ± 0.02 eV for both 40 nm SiO_2/p-type Si and 3 nm SiO_2/p-type Si structures. Binding energy (BE) and FWHM values of the Si 2p and O 1s high resolution spectra for each sample can be seen in Table 2.3. These results show that the bands of SiO_2 and Si substrate for the 3 nm SiO_2/Si system are flat (flat band condition) in thermodynamic equilibrium.

Table 2.3 Binding energy (BE) and FWHM values of the Si 2p and O 1s high resolution spectra.

Sample (Phase)	Si 2p		O 1s		δ(Si2p – O1s) (eV)
	BE (eV)	FWHM (eV)	BE (eV)	FWHM (eV)	
40 nm SiO_2/Si (SiO_2)	103.485	1.291	532.9739	1.338	429.489
3 nm SiO_2/Si (SiO_2)	103.500	1.281	533.0229	1.377	429.519
3 nm SiO_2/Si (Si)	98.957	0.52			
p-type Si(Si)	98.983	0.775			

2.4.2 Al_2O_3 as Charge Trapping Layer in Al/Al_2O_3/SiO_2/Si Structure and as Blocking Layer in MAHOS Structures

Al_2O_3 was deposited as charge trapping layer in Al/Al_2O_3/SiO_2/Si structure and as blocking layer in all MAHOS structures with the same deposition parameters. As-deposited Al_2O_3 has amorphous structure as confirmed by HRTEM results. The amorphous Al_2O_3 partially transformed into crystalline Al_2O_3 after rapid thermal annealing at 800^{o}C in N_2 ambient. The actual thickness of Al_2O_3 in as-deposited and annealed Al/Al_2O_3/SiO_2/p-type Si is ~15.4 nm and ~13.2 nm, respectively, which is close to the designed one, which is 15 nm. On the other hand, the actual thickness of Al_2O_3 blocking oxide in the MAHOS structures with HfAlO and Al_2O_3/HfO_2 nanolaminates as charge trapping layers is ~ 10 ± 1 nm. The actual thickness is similar with the designed one and shows that deposition by ALD method provides good constrain of thickness.

Figure R2.6 and Figure R2.7 show the high resolution Al 2p and O1s spectra of Al_2O_3 obtained by XPS. The charge build-up happened during x-ray irradiation on Al_2O_3 and shifted the peak to lower binding energy. To correct the peak position due to charging effect on insulator material, the peak was corrected by using Ar 2p peak at 241.82. The binding

energy of the components Al $2p_{3/2}$ and Al $2p_{1/2}$ were fitted by fitting the experimental data using a doublet with SOS of 0.41 eV and branching ratio of 2/1[18]. The binding energy (BE), FWHM, area, and area ratio of the O 1s and Al 2p high resolution spectra of as-deposited and annealed Al_2O_3 blocking layers can be seen in Table 2.4 – 2.7. The average position of the Al $2p_{3/2}$ peak is determined to be 74.64 ± 0.03 eV and 74.60 ± 0.03 eV for amorphous Al_2O_3 and crystalline Al_2O_3, respectively. The peak location of Al 2p at 74.60 eV confirms the formation of Al_2O_3. The average position of the O 1s peaks is determined to be 531.53 ± 0.02 eV and 531.51 ± 0.05 eV for amorphous Al_2O_3 and crystalline Al_2O_3, respectively. The core level difference of O1s and Al 2p is 456.87 ± 0.02 eV and 456.92 ± 0.06 eV for amorphous

Table 2.4 Binding energy (BE) and FWHM values of the Al 2p and O 1s high resolution spectra of as-deposited Al_2O_3 blocking layers in the MAHOS structures.

Sample	Al 2p		O 1s		d (Al2p - O1s)
	BE (eV)	FWHM (eV)	BE (eV)	FWHM (eV)	
A1	74.6679	1.613	531.5179	1.919	456.85
HA1	74.6529	1.595	531.5449	1.922	456.892
NA1	74.6219	1.587	531.5109	1.917	456.889
NB1	74.7749	1.578	531.5149	1.906	456.851

Table 2.5 Binding energy (BE) and FWHM values of the Al 2p and O 1s high resolution spectra of annealed Al_2O_3 blocking layers in the MAHOS structures.

Sample	Al 2p		O 1s		d (Al2p - O1s)
	BE (eV)	FWHM (eV)	BE (eV)	FWHM (eV)	
HA2	74.6249	1.613	531.5399	1.91	456.915
NA2	74.5729	1.649	531.5559	1.934	456.983
NB2	74.5839	1.604	531.4519	1.903	456.868

Table 2.6 The area of the Al 2p and O 1s high resolution spectra and the area ratio of Al 2p and O 1s of as-deposited Al_2O_3 blocking layers in the MAHOS structures.

Sample	Area of Al2p	Area of O1s	Ratio O:Al
A1	6101.138	28533.76	4.676793084
HA1	5087.759	24110.20	4.738864400
NA1	5062.822	24130.65	4.766244991
NB1	5184.789	25832.86	4.982432265

Table 2.7 The area of the Al 2p and O 1s high resolution spectra and the area ratio of Al 2p and O 1s of annealed Al_2O_3 blocking layers in the MAHOS structures.

Sample	Area of Al2p	Area of O1s	Ratio O:Al
HA1	5239.330	24514.970	4.6790277
NA1	5052.693	24085.150	4.7667947
NB1	5132.986	23386.060	4.5560342

Al_2O_3 and crystalline Al_2O_3, respectively.

2.4.3 $Al_2O_3/SiO_2/Si$ Interface in $Al/Al_2O_3/SiO_2/Si$ Structure

From the HRTEM images of as-deposited and annealed $Al/Al_2O_3/SiO_2/Si$ structures, high quality interface of Al_2O_3/SiO_2 interface is obtained with small roughness of less than 0.4 nm and without silicate formation even after annealing. The high resolution XPS spectra of Al 2p and Si 2p were evaluated at $Al_2O_3/SiO_2/Si$ interface in as-deposited structure, as shown in Figure R2.8. The binding energy (BE) and FWHM values of Al $2p_{Al2O3}$, Si $2p_{SiO2}$ and Si $2p_{Si}$ is shown in Table 2.8. The Si 2p spectra of SiO_2 layer and Al 2p spectra of Al_2O_3 layer are put together as comparison. The Si 2p peak is deconvoluted into 3 peaks, belongs to SiO_2, p-type Si substrate, and Si 2p peak in between 2 peaks. The Al 2p peak is deconvoluted into 2 peaks, belongs to Al_2O_3 at higher binding energy and Al 2p peak at lower binding

Table 2.8 The binding energy (BE) and FWHM values of Al $2p_{Al2O3}$, Si $2p_{SiO2}$ and Si $2p_{Si}$ at $Al_2O_3/SiO_2/Si$ interface in sample A1

Sample	Si 2p of SiO_2		Si 2p of Si		Al 2p of Al_2O_3		$E_{CL(i)}^{SiO2} - E_{CL(i)}^{Al2O3}$
	BE (eV)	FWHM	BE (eV)	FWHM	BE (eV)	FWHM	
A1 (Al_2O_3)					74.668	1.613	
A1 (Al_2O_3/SiO_2/Si int 1)	103.037	1.985	98.995	0.921	75.829	1.722	27.198
A1 (Al_2O_3/SiO_2/Si int 2)	103.145	1.757	98.933	0.904	75.987	1.696	27.158

energy. Since in HRTEM, there is no interlayer observed between Al_2O_3 and SiO_2, the other peak of Al 2p and Si 2p were detected as the peaks which represent the interface of Al_2O_3/SiO_2. The position of Al $2p_{Al2O3}$ at interface shifts to higher binding energy while the position of Si $2p_{SiO2}$ at interface shifts to lower binding energy. The peak shifts in Al 2p and Si 2p is due to internal electric field generation at $Al_2O_3/SiO_2/Si$ interface. This phenomenon will be explained in detail in chapter 3.

2.4.4 HfAlO Layer and [Al_2O_3/HfO_2] Nanolaminate Structures

The HRTEM images of HfAlO layer and [Al_2O_3/HfO_2] nanolaminates in MAHOS structures are shown in Figure R2.2 – Figure R2.4. The as-deposited HfAlO layer is basically nanolaminate structures since each Al_2O_3 monolayer and HfO_2 monolayer were deposited periodically until the total thickness of 10 nm was obtained. Since the thickness of monolayer is very thin, the nanolaminate appears as single layer of HfAlO. The thickness of HfAlO layer is observed to be ~10 nm. On the other hand, the nanolaminate structure of sample NA1 and NB1 can be observed. The thickness of one Al_2O_3 and HfO_2 layer in sample NA1 is observed to be 0.85 nm and 1.05 nm, respectively. In sample NB1, the thickness of one Al_2O_3 and HfO_2 layer is found to be 1.8 nm and 2.1 nm, respectively. The roughness at Al_2O_3/HfO_2

interface is found to be less than 0.5 nm. High-κ dielectric in as-deposited MAHOS structure has amorphous phase.

After annealing at 800^{o}C in N_2 ambient for one minutes, amorphous high-κ dielectric transforms into crystalline phase. In sample NA2 and NB2, the nanolaminate structure, which are [1 nm HfO_2/1 nm Al_2O_3]$_4$/1 nm HfO_2 and [2 nm HfO_2/2 nm Al_2O_3]$_2$/2 nm HfO_2, broke up and Al_2O_3 mix with HfO_2 in the middle of nanolaminate structure. The CTL structure of annealed sample became HfO_2/HfAlO/HfO_2.

The high resolution XPS peaks of Al 2p and Hf 4f of sample HA1, sample NA1, and sample NB1 at Al_2O_3/HfAlO interface and Al_2O_3/HfO_2 interface were obtained by removing or sputtering the upper layer, Al_2O_3 blocking layer by using Ar gas. The binding energy of the components Hf $4f_{7/2}$ and Al $4f_{5/2}$ were fitted by fitting the experimental data using a doublet with SOS of 1.68 eV and branching ratio of 4/3. Figure R2.9 shows the Al 2p and Hf 4f peaks of as-deposited Al_2O_3/[HfO_2/Al_2O_3]$_2$/HfO_2/SiO_2/p-type Si capacitor structure at the Al_2O_3/HfO_2 interface with different depth levels. The binding energy (BE) of Si 2p, Hf 4f, and Al 2p in sample HA1, NA1, and NB1 and the energy distance between different core level (CL) at interface in sample HA1, NA1, and NB1 are shown in Table 2.9 and 2.10, respectively. Figure R2.9 (a), (b), and (c) represent Al_2O_3/HfO_2 interface which are close to Al_2O_3 blocking layer, in the middle of nanolaminates, and close to SiO_2/p-type Si, respectively. To fit the experimental data, the Al 2p peak is deconvoluted into 2 peaks which belong to Al^{3+} or Al-O bonding of Al_2O_3 and Al-Al bonding, respectively. The Hf 4p peak is deconvoluted into 4 peaks which belong to the bonding of Hf-O of HfO_2 and Hf-Hf bonding, respectively. Loss feature of Hf metal is also found at the energy of about 23 eV. The Al 2p and Hf 4f peaks are shifted to higher binding energy from 74.39 eV to 74.86 eV and from 17.36 eV to 17.85 eV, respectively. However, the binding energy difference between Al 2p and Hf 4f peaks are constant which is ~57 eV. The binding energy shift of Al 2p and Hf 4f is

Table 2.9 The binding energy (BE) of Si 2p, Hf 4f, and Al 2p in sample HA1, NA1, and NB1.

Sample	$t_{sputtering}$ (min)	Si 2p of SiO_2	Si 2p of Si	Hf 4f	Al 2p of Al_2O_3
		BE (eV)	BE (eV)	BE (eV)	BE (eV)
HA1 (Al_2O_3/HfAlO)	2.7			17.4969	74.4769
HA1 (Al_2O_3/HfAlO/SiO_2/Si)	4.8	103.211	98.933	18.7139	75.6239
NA1 (Al_2O_3/HfO_2)	2.7			17.6579	74.6159
NA1 (Al_2O_3/HfO_2/SiO_2/Si)	4.5	103.232	98.901	18.6989	75.5979
NB1 (Al_2O_3/HfO_2 int. 1)	1.8			17.3599	74.3879
NB1 (Al_2O_3/HfO_2 int. 2)	2.1			17.5959	74.6119
NB1 (Al_2O_3/HfO_2 int. 3)	3			17.8469	74.8599
NB1 (Al_2O_3/HfO_2/SiO_2/Si)	5.1	103.051	98.848	18.5129	75.3799

Table 2.10 The energy distance between different ore leel (CL) at interface in sample HA1, NA1, and NB1.

Sample	$t_{sputtering}$ (min)	$E_{CL(i)}^{Si} - E_{CL(i)}^{Hf}$	$E_{CL(i)}^{SiO2} - E_{CL(i)}^{Hf}$	$E_{CL(i)}^{Al2O3} - E_{CL(i)}^{Hf}$
HA1 (Al_2O_3/HfAlO)	2.7			56.98
HA1 (Al_2O_3/HfAlO/SiO_2/Si)	4.8	80.2191	84.497	56.91
NA1 (Al_2O_3/HfO_2)	2.7			56.958
NA1 (Al_2O_3/HfO_2/SiO_2/Si)	4.5	80.2021	84.533	56.899
NB1 (Al_2O_3/HfO_2 int. 1)	1.8			57.028
NB1 (Al_2O_3/HfO_2 int. 2)	2.1			57.016
NB1 (Al_2O_3/HfO_2 int. 3)	3			57.013
NB1 (Al_2O_3/HfO_2/SiO_2/Si)	5.1	80.3351	84.538	56.867

due to the dipole formation in HfO_2/Al_2O_3 interface. Figure R2.10 shows the Al 2p and Hf 4f peaks of sample HA1, NA1, and NB1, respectively, at certain depth level whichis close to SiO_2/p-type Si. The Al 2p and Hf 4f peaks shifted to higher binding energy for HfO_2/Al_2O_3 nanolaminate with thicker period. The binding energy difference between Al 2p and Hf 4f peaks is similar, ~57 eV. This result shows different structure of HfO_2/Al_2O_3 nanolaminate and different magnitude of dipole formation does not change the barrier height between HfAlO or HfO_2 and Al_2O_3.

After annealing, amorphous high-κ films transform into crystalline high-κ films and the CTL structure of NA2 and NB2 sample became HfO_2/HfAlO/HfO_2. The high resolution XPS peaks of Al 2p and Hf 4f of sample HA2, sample NA2, and sample NB2 were obtained at the positions which are in the middle of nanolaminates, and close to SiO_2/p-type Si, shown in Figure R2.11 and Figure R2.12, respectively. The binding energy (BE) of Si 2p, Hf 4f, and Al 2p in sample HA2, NA2, and NB2 and the energy distance between different ore leel (CL) at interface in sample HA2, NA2, and NB2 are shown in Table 2.11 and 2.12, respectively. At the position which is in the middle of nanolaminates, the binding energy of Al 2p and Hf 4f for sample NA2 and NB2 are determined to be ~74.55 ± 0.02 eV and 17.49 ± 0.03 eV, respectively. These peak positions are similar with those in HfAlO layer and indicate that the observed layer is HfO_2/HfAlO with more dominant crystalline HfAlO layer. At the position which is close to SiO_2/p-type Si, the binding energy of Al 2p and Hf 4f for sample NA2 and NB2 shifted to higher binding energy and are found to be ~74.91 ± 0.01 eV and 17.92 ± 0.03 eV, respectively. On the other hand, the binding energy of Al 2p and Hf 4f for sample HA2 are determined to be ~74.49 eV and 17.56 eV, respectively. These results indicate that position, the observed layer in sample NA2 and NB2 is crystalline HfAlO/HfO_2 with more dominant HfO_2 and that in sample HA2 is crystalline HfAlO layer. The binding energy difference between Al 2p and Hf 4f peaks for all samples is ~57 eV.

Table 2.11 The binding energy (BE) of Si 2p, Hf 4f, and Al 2p in sample HA2, NA2, and NB2.

Sample	$t_{sputtering}$ (min)	Si 2p of SiO_2	Si 2p of Si	Hf 4f	Al 2p of Al_2O_3
		BE (eV)	BE (eV)	BE (eV)	BE (eV)
HA2 (Al_2O_3/HfAlO)	2.7			17.5689	74.5559
HA2 (Al_2O_3/HfAlO/SiO_2/Si)	4.5	103.20	98.973	18.7029	75.6319
NA2 (HfO_2/HfAlO)	2.1			17.5199	74.5669
NA2 (HfAlO/HfO_2)	2.7			17.8939	74.9049
NA2 (HfAlO/HfO_2/SiO_2/Si)	4.2	103.163	98.956	18.7409	75.6719
NB2 (HfO_2/HfAlO)	2.1			17.4679	74.5379
NB2 (HfAlO/HfO_2)	3			17.9479	74.9269
NB2 (HfAlO/HfO_2/SiO_2/Si)	4.2	103.214	98.904	18.7859	75.7221

Table 2.12 The energy distance between different core level (CL) at interface in sample HA2 NA2, and NB2.

Sample	$t_{sputtering}$ (min)	$E_{CL(i)}^{Si} - E_{CL(i)}^{Hf}$	$E_{CL(i)}^{SiO2} - E_{CL(i)}^{Hf}$	$E_{CL(i)}^{Al2O3} - E_{CL(i)}^{Hf}$
HA2 (Al_2O_3/HfAlO)	2.7			56.987
HA2 (Al_2O_3/HfAlO/SiO_2/Si)	4.5	80.2701	84.496	56.929
NA2 (HfO_2/HfAlO)	2.1			57.047
NA2 (HfAlO/HfO_2)	2.7			57.011
NA2 (HfAlO/HfO_2/SiO_2/Si)	4.2	80.2151	84.422	56.931
NB2 (HfO_2/HfAlO)	2.1			57.07
NB2 (HfAlO/HfO_2)	3			56.979
NB2 (HfAlO/HfO_2/SiO_2/Si)	4.2	80.1181	84.428	56.9362

2.4.5 High-κ/SiO_2/Si Structure and Its Interface

The high resolution XPS peaks of Si $2p_{(SiO2)}$, Si $2p_{(p\text{-type Si})}$, Al 2p, and Hf 4f of as-deposited and annealed MAHOS structures at $Al_2O_3/HfO_2/SiO_2$/Si interface were also observed and their binding energy differences were evaluated. The data can be found in Table 2.9 – 2.12. The binding energy of Si 2p peak of SiO_2 for all samples is determined to be ~103.20 ± 0.04 eV, which is shifted to lower binding energy compared to that of SiO_2 thick film and SiO_2 thin film on p-type Si substrate which is found to be ~103.50 eV. The binding energy shift of Si 2p of SiO_2 is due to dipole formation at HfO_2/SiO_2/Si structure. On the other hand, the binding energy of Si 2p of Si substrate is found to be ~98.95 ± 0.05 eV. Comparing to the binding energy of Al 2p and Hf 4f at Al_2O_3/HfO_2 interface, the Al 2p and Hf 4f peaks at high-κ/SiO_2/Si interface has higher binding energy due to dipole formation at HfO_2/SiO_2 interface which are determined to be ~75.61 ± 0.02 eV and ~18.70 ± 0.02 eV for as-deposited structures and ~75.69 ± 0.04 eV and ~18.74 ± 0.04 eV for annealed structures, respectively. The binding energy difference between Al 2p and Hf 4f, Si 2p and Hf 4f, and Si 2p and Al 2p are found to be ~56.9 ± 0.02 eV, ~84.52 ± 0.02 eV, and ~27.63 ± 0.04 eV for as-deposited MAHOS structures and ~56.9 ± 0.02 eV, ~84.46 ± 0.04 eV, and ~27.5 ± 0.04 eV for annealed MAHOS structures, respectively.

2.5 Summary

In chapter 2, the design consideration of capacitor structures, experimental procedures on the fabrication of the MAHOS capacitor structures, and structure characterization have been described. The process flow of the device fabrication, including Radio Corporation America (RCA) cleaning, rapid thermal oxidation (RTO), atomic layer deposition (ALD), rapid thermal annealing (RTA), and thermal evaporation, has been explained. The microstructures and the chemical states of the MAHOS capacitor structures were evaluated

by high-resolution transmission electron microscope (HRTEM) and x-ray photoemission spectroscopy (XPS).

From the MAHOS structure evaluation discussed in this chapter, we can summarize some important points:

1. The MAHOS capacitor structures have been successfully prepared, by using certain fabrication methods which are common in semiconductor fabrication industry to make sure that the devices have good quality and are suitable for electronic applications.
2. From cross-sectional HRTEM images, all structures possess high quality interface with small roughness less than 5 Angstrom and uniform thickness. The natural SiO_2 and defects can be removed by RCA cleaning completely and high quality SiO_2 can be grown by rapid thermal oxidation. This is indicated by good interface of SiO_2/Si with the roughness of about 1 – 2 monolayers of Si and uniform thickness of SiO_2. The excellent uniformity of Al_2O_3 and HfO_2 deposited by ALD proves that the ALD method offers good control of thickness with good uniformity.
3. The Al 2p and Hf 4f peaks are shifted to higher binding energy. However, the binding energy difference between Al 2p and Hf 4f peaks are constant which is ~57 eV. The binding energy shift of Al 2p and Hf 4f is due to the dipole formation in HfO_2/Al_2O_3 interface. Different structure of HfO_2/Al_2O_3 nanolaminate and different magnitude of dipole formation does not change the barrier height between HfAlO or HfO_2 and Al_2O_3.
4. After annealing, amorphous high-κ films transform into crystalline high-κ films and the CTL structure of NA2 and NB2 sample became HfO_2/HfAlO/HfO_2. The XPS measurement at high-κ/SiO_2/Si interface shows that the observed layer close to SiO_2/Si in sample NA2 and NB2 is crystalline HfAlO/HfO_2 with more dominant HfO_2 and that in sample HA2 close to SiO_2/Si is crystalline HfAlO layer.

References

[1] Tuo-Hung Hou, Chungho Lee, Venkat Narayanan, Udayan Ganguly, and Edwin Chihchuan Kan. Design Optimization of Metal Nanocrystal Memory—Part II: Gate-Stack Engineering. IEEE Transactions on Electron Devices, vol. 53, no. 12, December 2006.

[2] S. M. Sze and Kwok K. Ng. Physics of Semiconductor Device, Third Edition. 2007. John Wiley & Sons, Inc.

[3] J. L. Alay and M. Hirose. The valence band alignment at ultrathin SiO_2/Si interfaces. Journal of Applied Physics **81**, 1606 (1997).

[4] J. Robertson. High dielectric constant oxides. Eur. Phys. J. Appl. Phys. **28**, 265–291 (2004).

[5] Sangmoo Choi, Myungjun Cho, and Hyunsang Hwang. Improved metal–oxide–nitride–oxide–silicon-type flash device with high-k dielectrics for blocking layer. Journal Of Applied Physics Volume 94, Number 8 (2003).

[6] Jong Kyung Park, Youngmin Park, Seok-Hee Lee, Sung Kyu Lim, Jae Sub Oh, Moon Sig Joo, Kwon Hong, and Byung Jin Cho. Mechanism of Date Retention Improvement by High Temperature Annealing of Al_2O_3 Blocking Layer in Flash Memory Device. Japanese Journal of Applied Physics 50 (2011) 04DD07.

[7] Chang-Hyun Lee, Sung-Hoi Hur, You-Cheol Shin, Jeong-Hyuk Choi, Dong-Gun Park, and Kinam Kim. Charge-trapping device structure of SiO_2/SiN/high-k dielectric Al_2O_3 for high-density flash memory. Applied Physics Letters **86**, 152908 (2005).

[8] Keith P. McKenna and Alexander L. Shluger. Electron and hole trapping in polycrystalline metal oxide materials. Proc. R. Soc. A. rspa(2010)0518.

[9] T. Sugizaki, M. Kohayashi, M. Ishidao, H. Minakata, M. Yamaguchi, Y. Tamura, Y. Sugiyama, T. Nakanishi, and H. Tanaka. Novel Multi-bit SONOS Type Flash Memory

Using a Highk Charge Trapping Layer. 2003 Symposium on VLSl Technology Digest of Technical Papers.

[10] D. Misra and N. A. Chowdhury. Charge Trapping in High-κ Gate Dielectrics: A Recent Understanding. ECS Transactions, 2 (1) 311-328 (2006).

[11] W. Kern. (1990). The Evolution of Silicon Wafer Cleaning Technology. Journal of the Electrochemical Society 137 (6): 1887–1892.

[12] M. Itano, F. W. Kern, M. Miyashita, T. Ohmi. (1993). Particle Removal from Silicon Wafer Surface in Wet Cleaning Process. IEEE Transactions on Semiconductor Manufacturing 6 (3): 258.

[13] M. J. Hartt and A. G. R. Evans. Rapid Thermal Processing in Semiconductor Technology. Semicond. Sci. Technol. 3 (1988) 421-436.

[14] A. T. Fiory. Methods in Rapid Thermal Annealing. Proceedings of RTP 2000, Eighth International Conference on Advanced Thermal Processing of Semiconductors (Gaithersburg, Md., Sept. 20 - 22, 2000), pp. 15-25.

[15] Youngseok Lee, Woongkyo Oh, Vinh Ai Dao, Shahzada Qamar Hussain, and Junsin Yi. Ultrathin Oxide Passivation Layer by Rapid Thermal Oxidation for the Silicon Heterojunction Solar Cell Applications. International Journal of Photoenergy Volume 2012, Article ID 753456, 5 pages.

[16] R. Gunawan, M.Y.L. Jung, E.G. Seebauer, R.D. Braatz. Optimal Control of Rapid Thermal Annealing in a Semiconductor Process. Journal of Process Control 14 (2004) 423–430.

[17] A.L. Helms, Jr., R.B. Herring, C. Porter, A. Starner: Solid State Technology, 42, No. 11 (1999), 83.

[18] Alexander V. Naumkin, Anna Kraut-Vass, Stephen W. Gaarenstroom, and Cedric J. Powell. NIST X-ray Photoelectron Spectroscopy Database. 2012.

Figure of Results

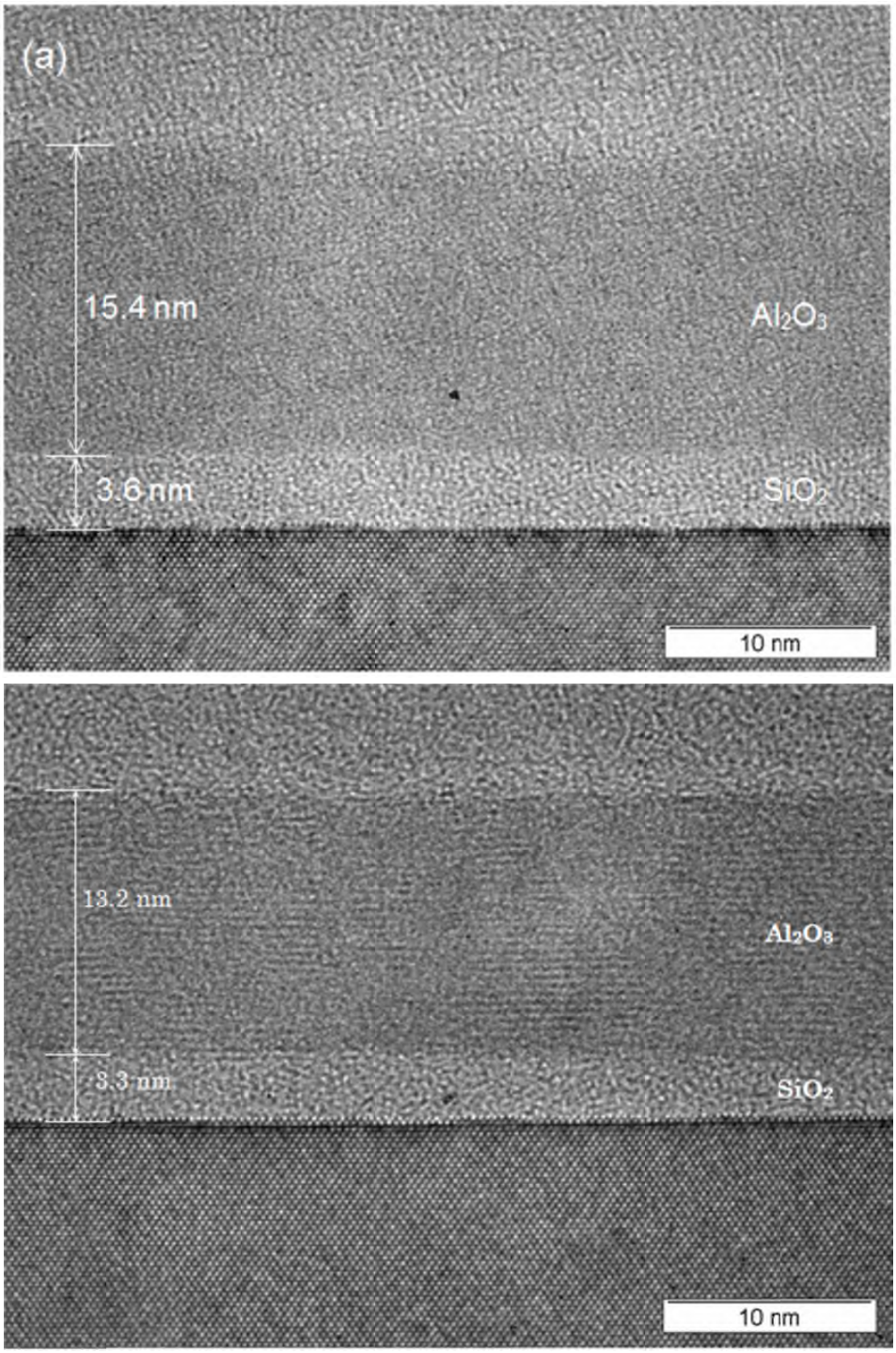


Figure R2.1 HRTEM image of (a) as-deposited Al_2O_3/SiO_2/p-type Si capacitor structure and (b) Al_2O_3/SiO_2/p-type Si capacitor structure annealed at 900^{o}C for 1 minute in N_2 ambient.

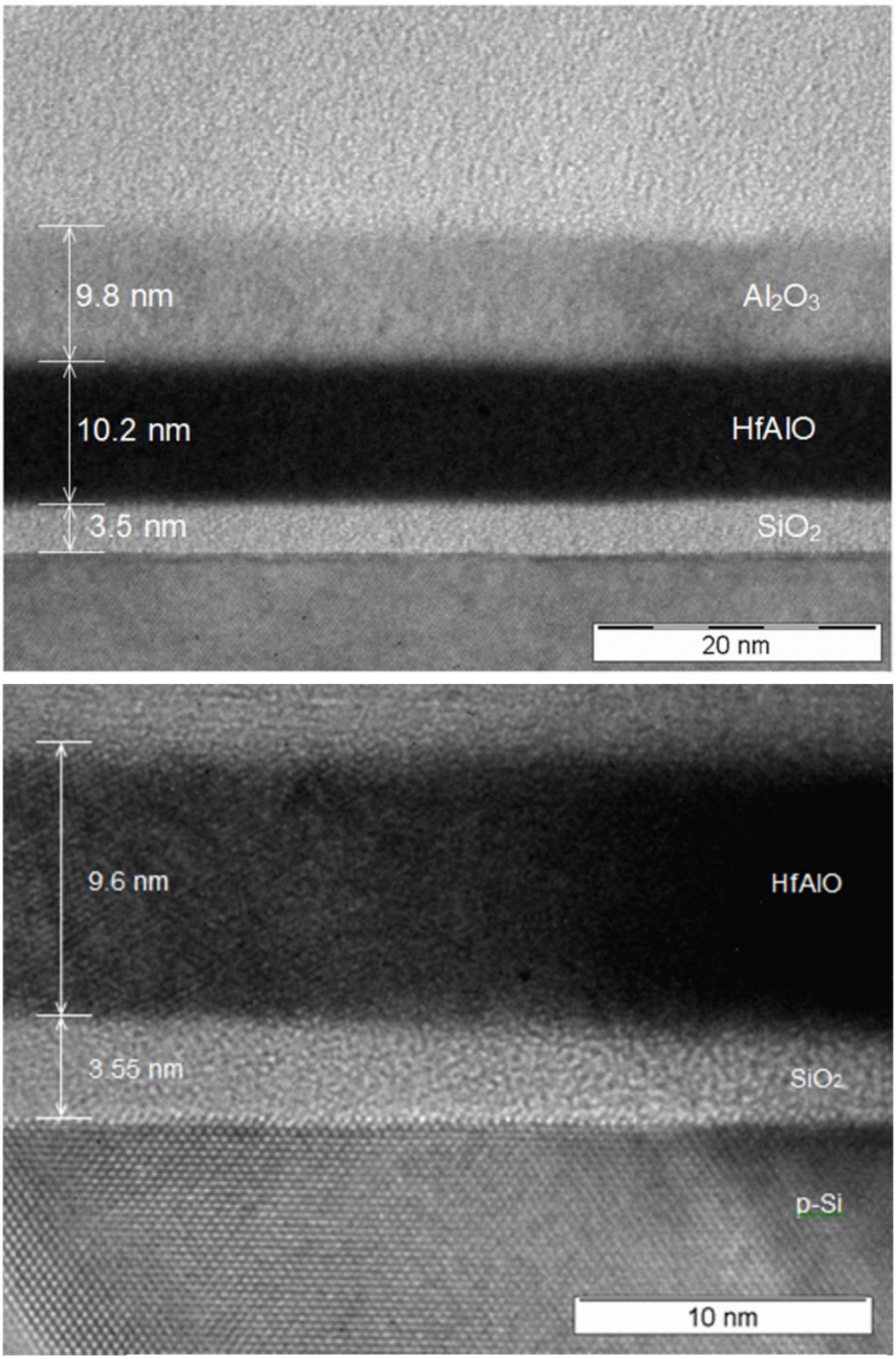


Figure R2.2 HRTEM image of (a) as-deposited Al_2O_3/HfAlO/SiO_2/p-type Si capacitor structure and (b) Al_2O_3/ HfAlO/SiO_2/p-type Si capacitor structure annealed at 900^oC for 1 minute in N_2 ambient.

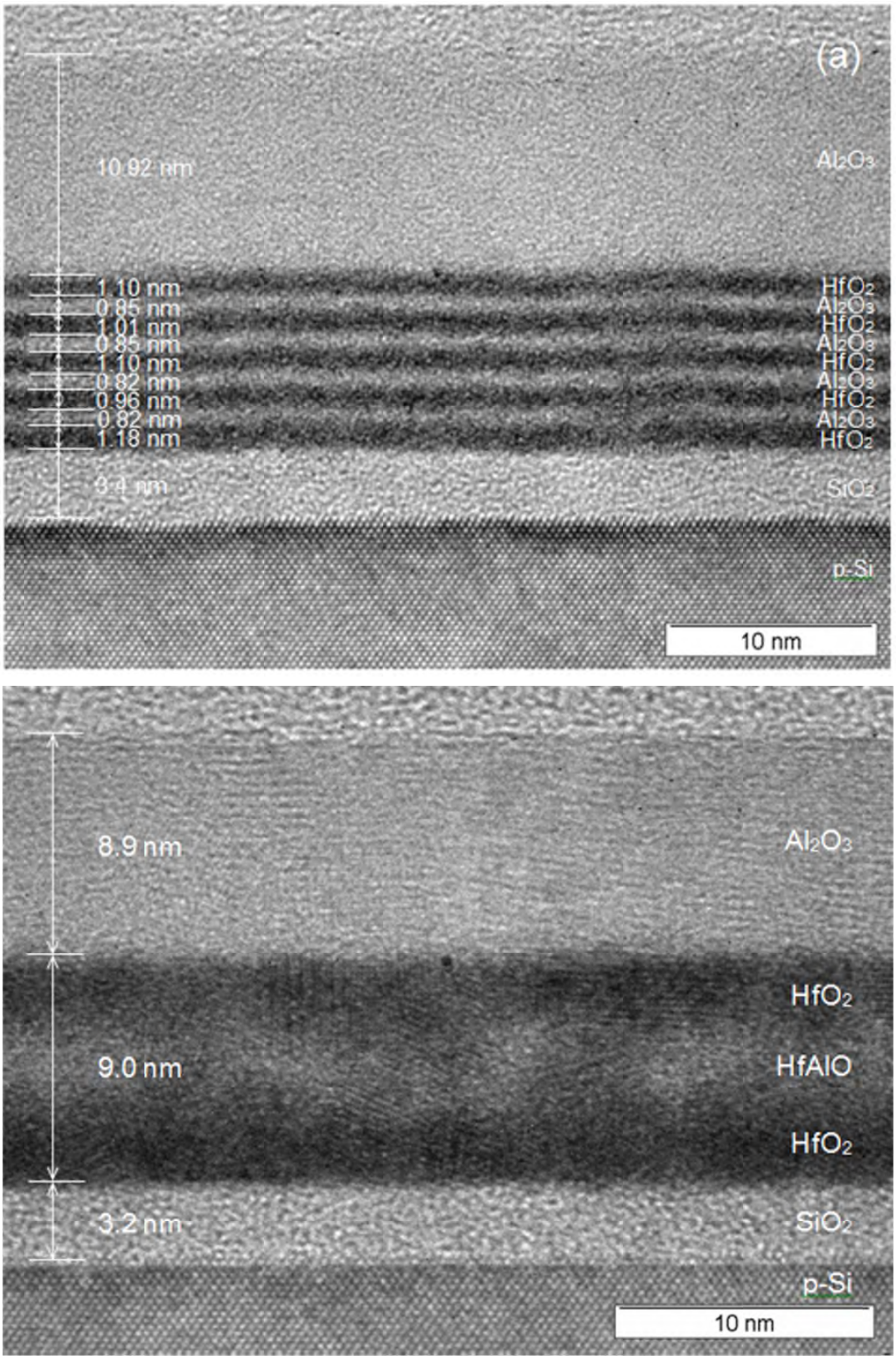


Figure R2.3 HRTEM image of (a) as-deposited $Al_2O_3/[HfO_2/Al_2O_3]_4/HfO_2/SiO_2$/p-type Si capacitor structure and (b) $Al_2O_3/[HfO_2/Al_2O_3]_4/HfO_2/SiO_2$/p-type Si capacitor structure annealed at 800^oC for 1 minute in N_2 ambient.

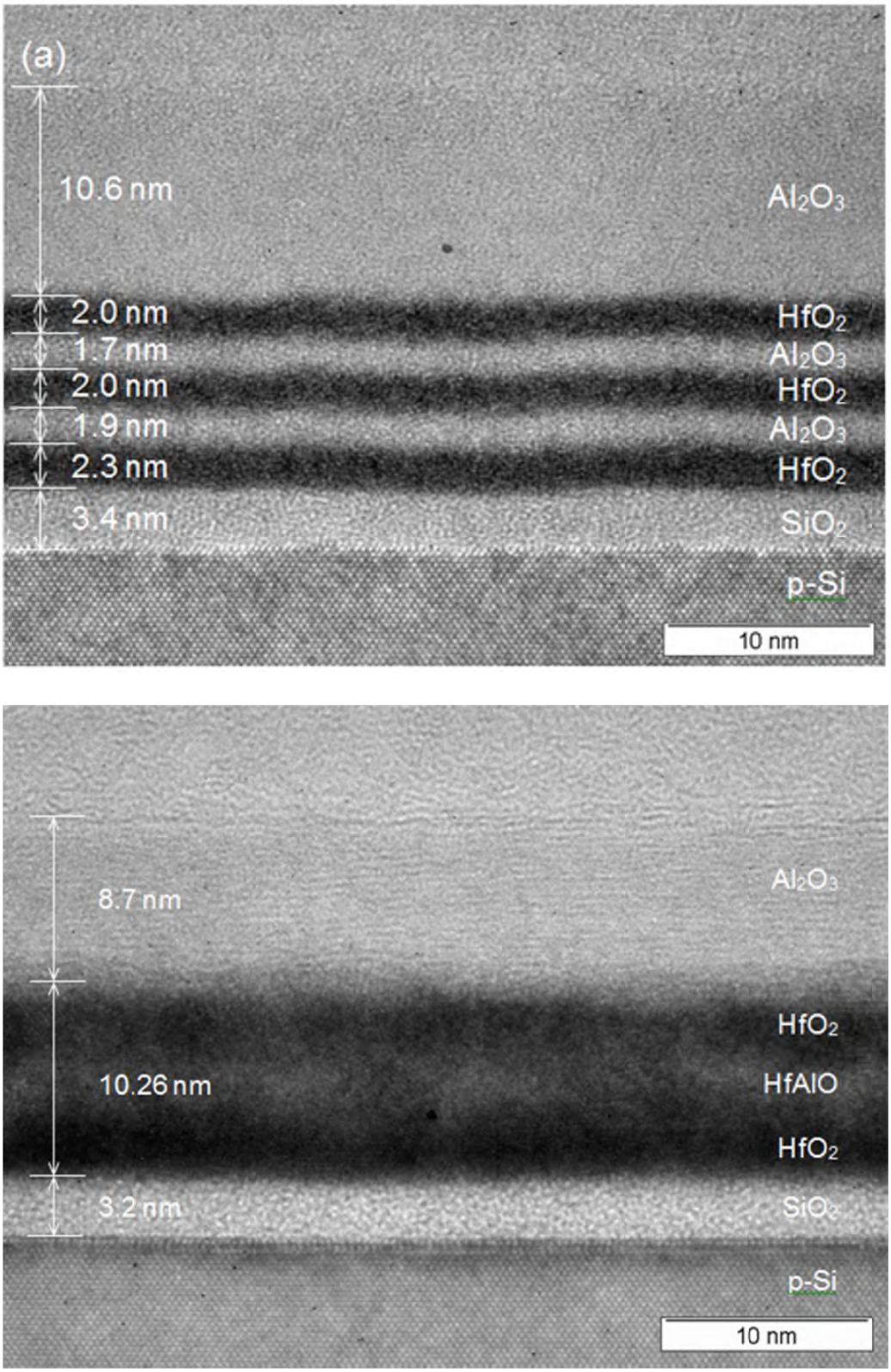


Figure R2.4 HRTEM image of (a) as-deposited $Al_2O_3/[HfO_2/Al_2O_3]_2/HfO_2/SiO_2$/p-type Si capacitor structure and (b) $Al_2O_3/[HfO_2/Al_2O_3]_2/HfO_2/SiO_2$/p-type Si capacitor structure annealed at 800^oC for 1 minute in N_2 ambient.

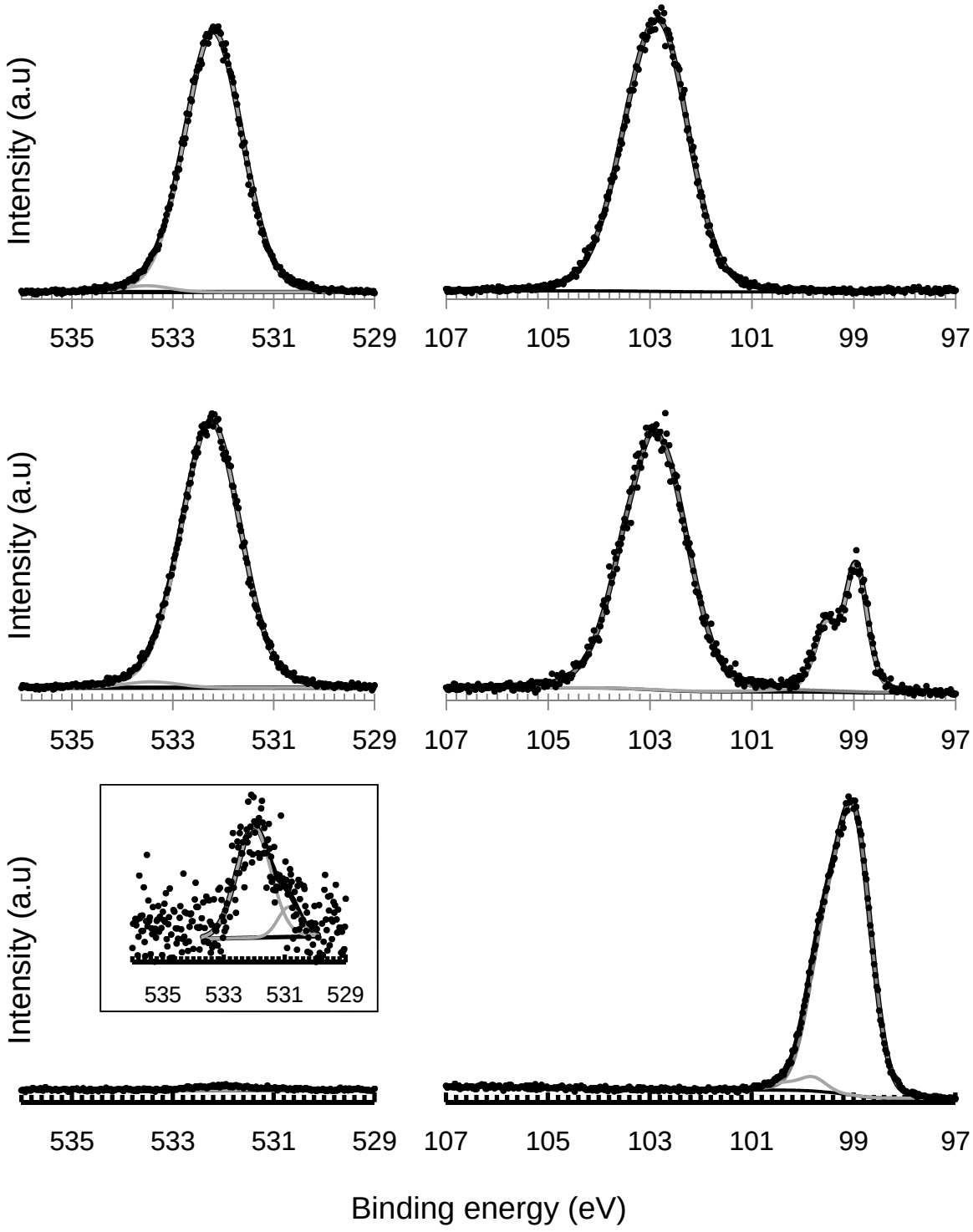


Figure R2.5 The O 1s and Si 2p peaks of (a) bulk SiO_2 of 40 nm SiO_2/p-type Si, (b) SiO_2 and Si at the interface of 3 nm SiO_2/p-type Si, and (c) bulk p-type Si of 3 nm SiO_2/p-type Si after removing SiO_2 layer by sputtering.

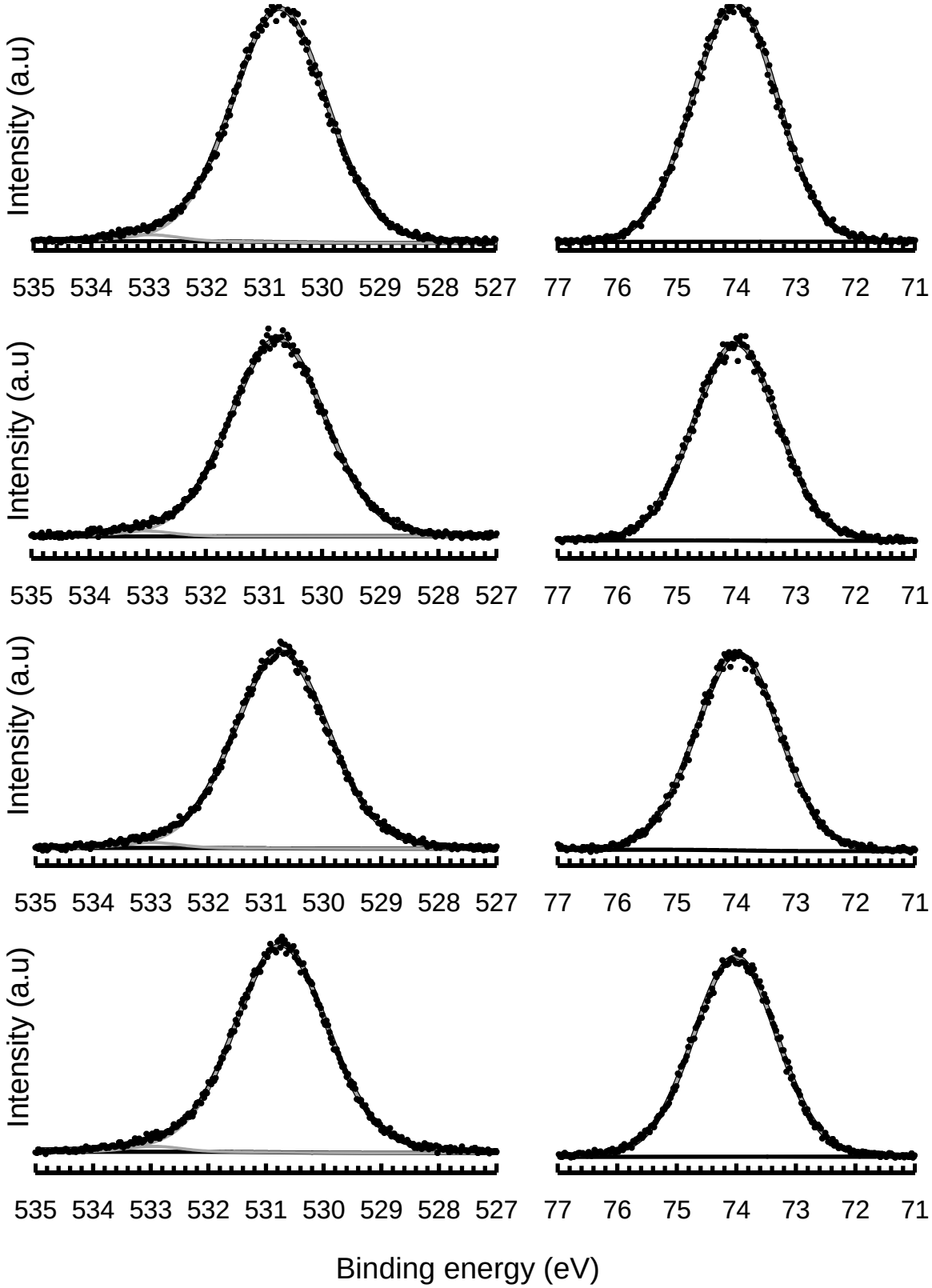


Figure R2.6 The O 1s and Al 2p peaks of Al_2O_3 blocking layers of as-deposited (a) Al_2O_3/SiO_2/p-type Si, (b) Al_2O_3/HfAlO/SiO_2/p-type Si, (c) $Al_2O_3/[HfO_2/Al_2O_3]_4/HfO_2/SiO_2$/p-type Si, and (d) $Al_2O_3/[HfO_2/Al_2O_3]_2/HfO_2/SiO_2$/p-type Si capacitor structure.

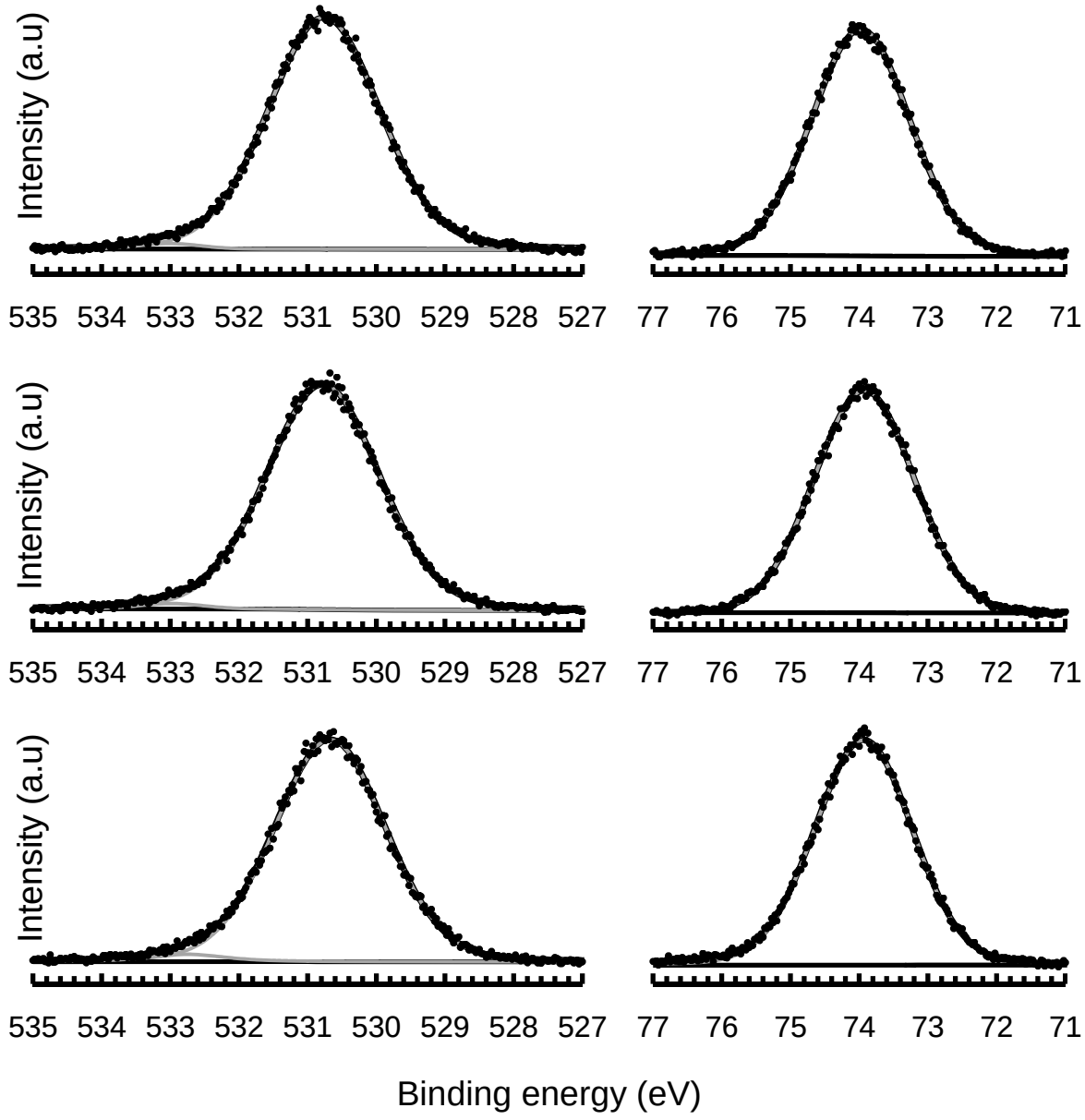


Figure R2.7 The O 1s and Al 2p peaks of Al_2O_3 blocking layers of annealed (a) Al_2O_3/HfAlO/SiO_2/p-type Si, (b) Al_2O_3/[HfO_2/Al_2O_3]$_4$/HfO_2/SiO_2/p-type Si, and (c) Al_2O_3/[HfO_2/Al_2O_3]$_2$/HfO_2/SiO_2/p-type Si capacitor structure.

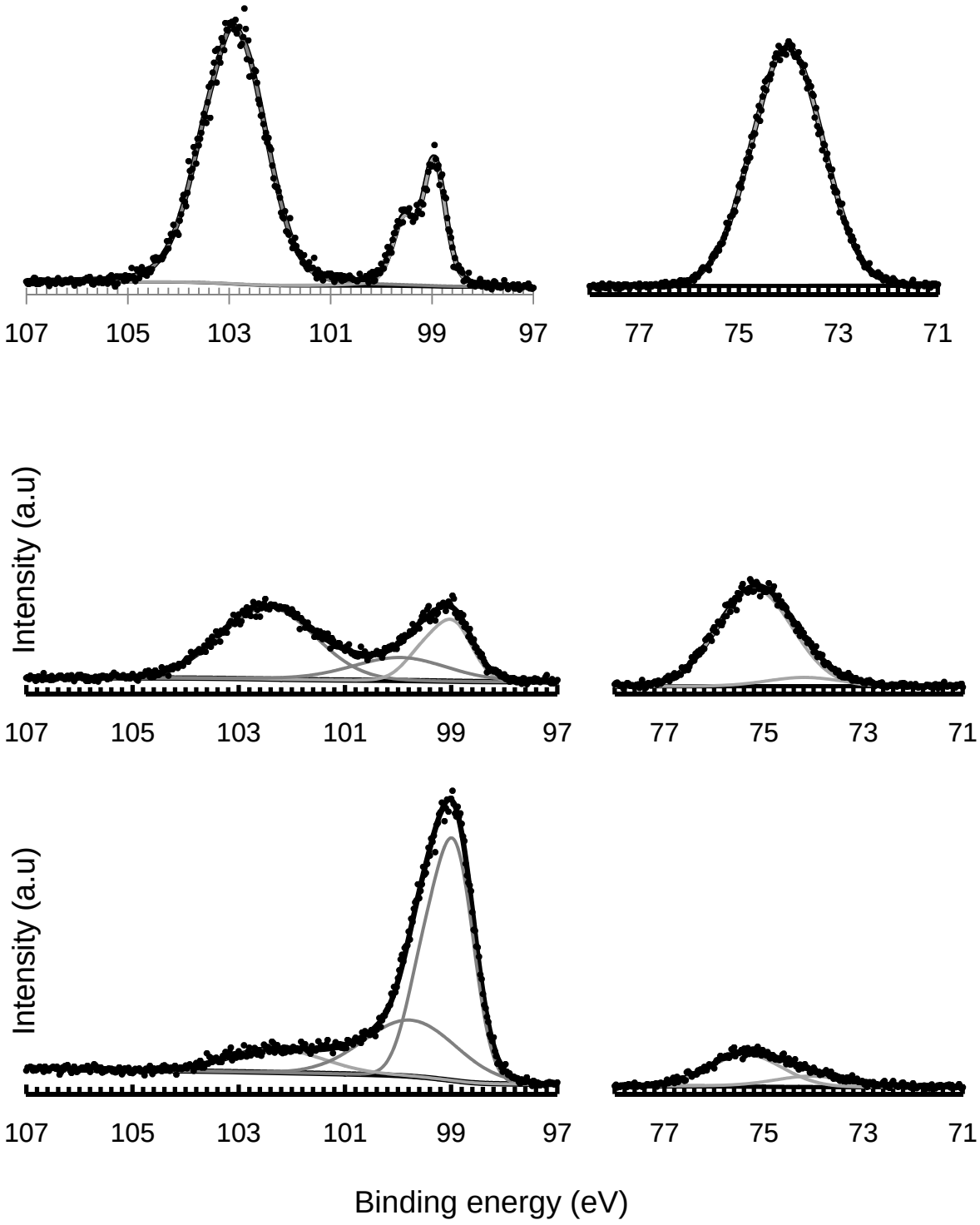


Figure R2.8 The Si 2p and Al 2p peaks of (a) 3 nm SiO_2/p-type Si and Al_2O_3 bulk,

(b) Al_2O_3/SiO_2/p-type Si interface after etching 1, and

(c) Al_2O_3/SiO_2/p-type Si interface after etching 2.

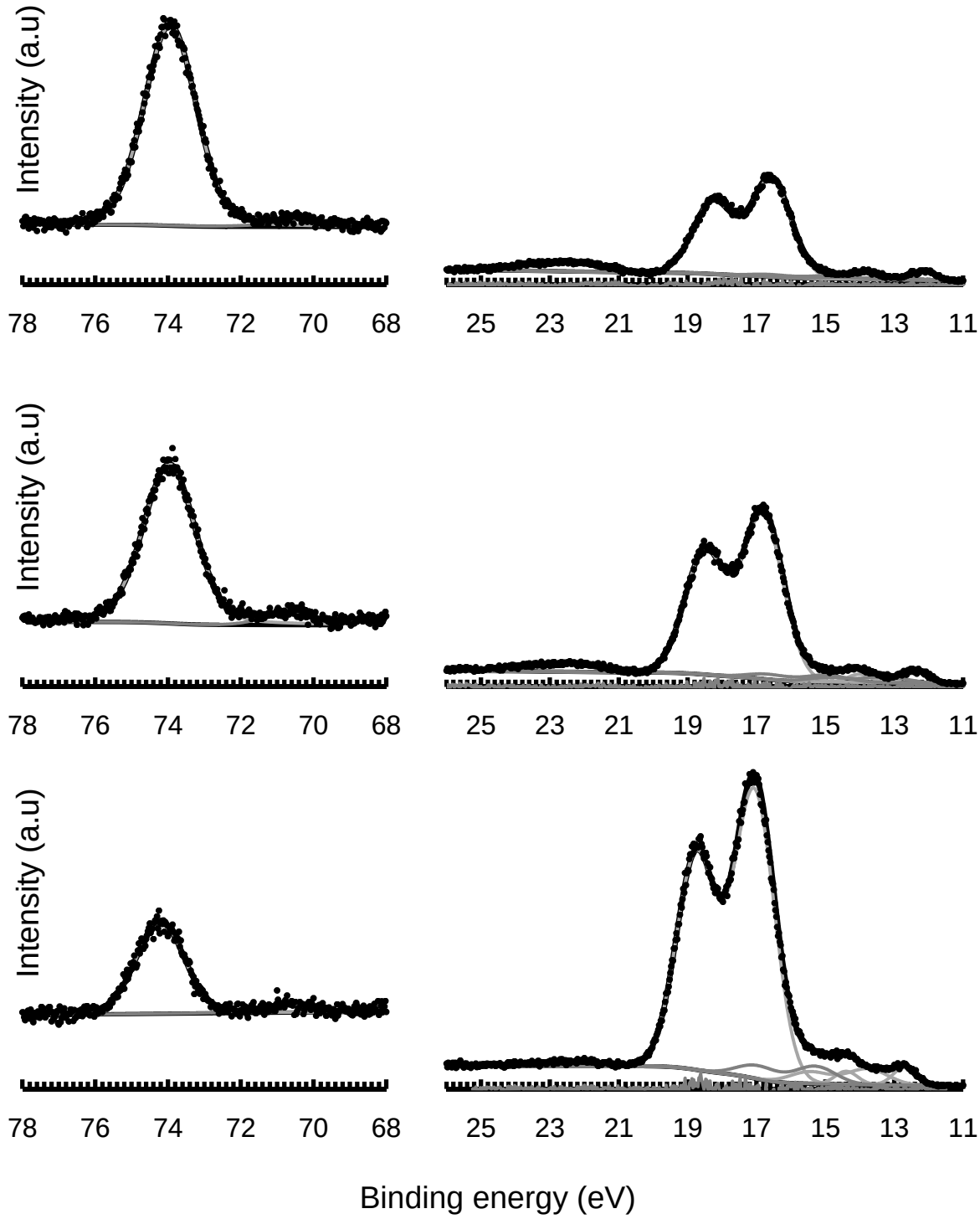


Figure R2.9 The Al 2p and Hf 4f peaks of the Al_2O_3/HfO_2 interface of as-deposited $Al_2O_3/[HfO_2/Al_2O_3]_2/HfO_2/SiO_2$/p-type Si capacitor structure at different depth levels.

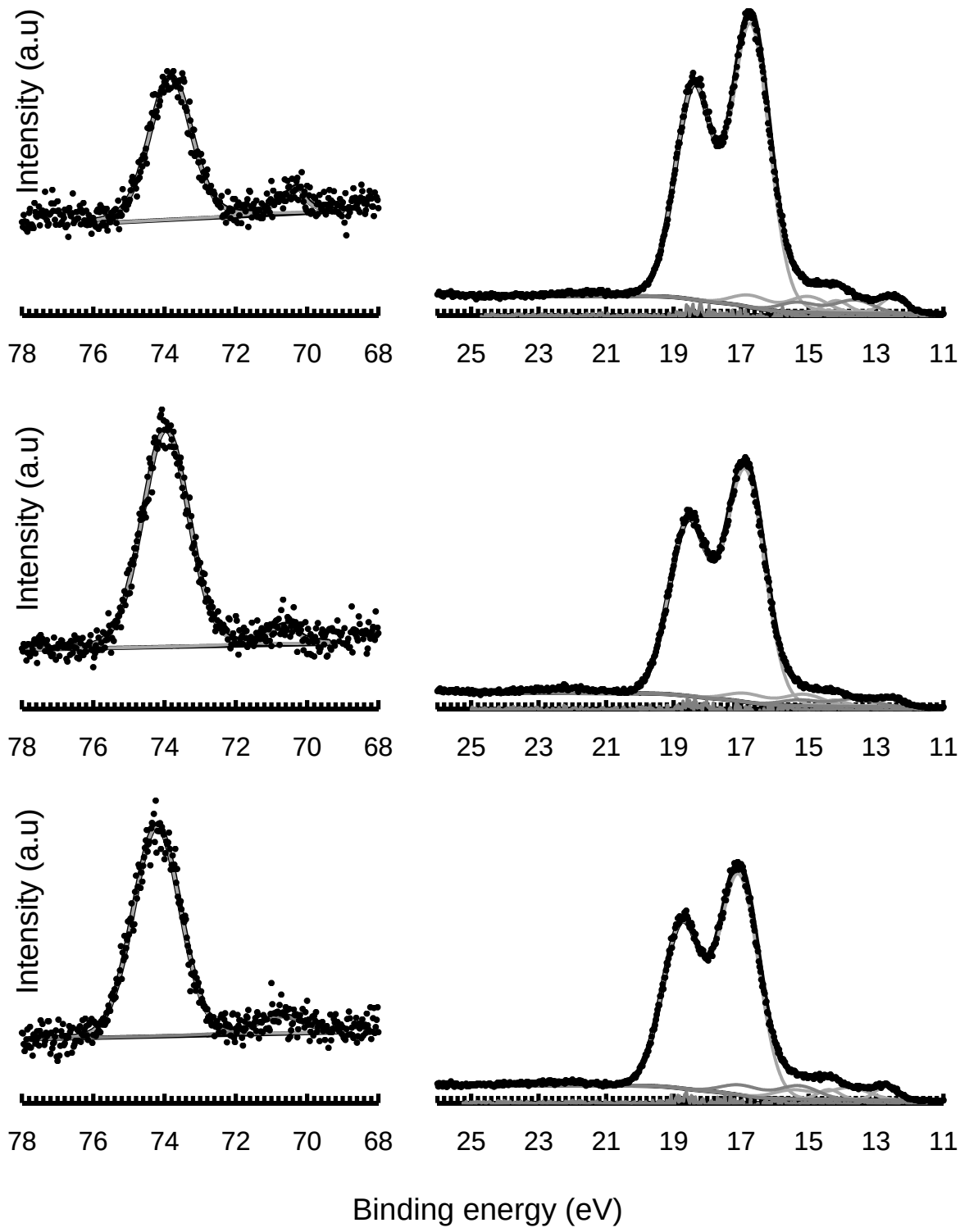


Figure R2.10 The Al 2p and Hf 4f peaks of the Al_2O_3/HfO_2 interface of as-deposited

(a) Al_2O_3/10 nm HfAlO/SiO_2/p-type Si capacitor structure,

(b) Al_2O_3/[1 nm HfO_2/1 nm $Al_2O_3]_4$/1 nm HfO_2/SiO_2/p-type Si capacitor structure, and

(c) Al_2O_3/[2 nm HfO_2/2 nm $Al_2O_3]_2$/2 nm HfO_2/SiO_2/p-type Si capacitor structure.

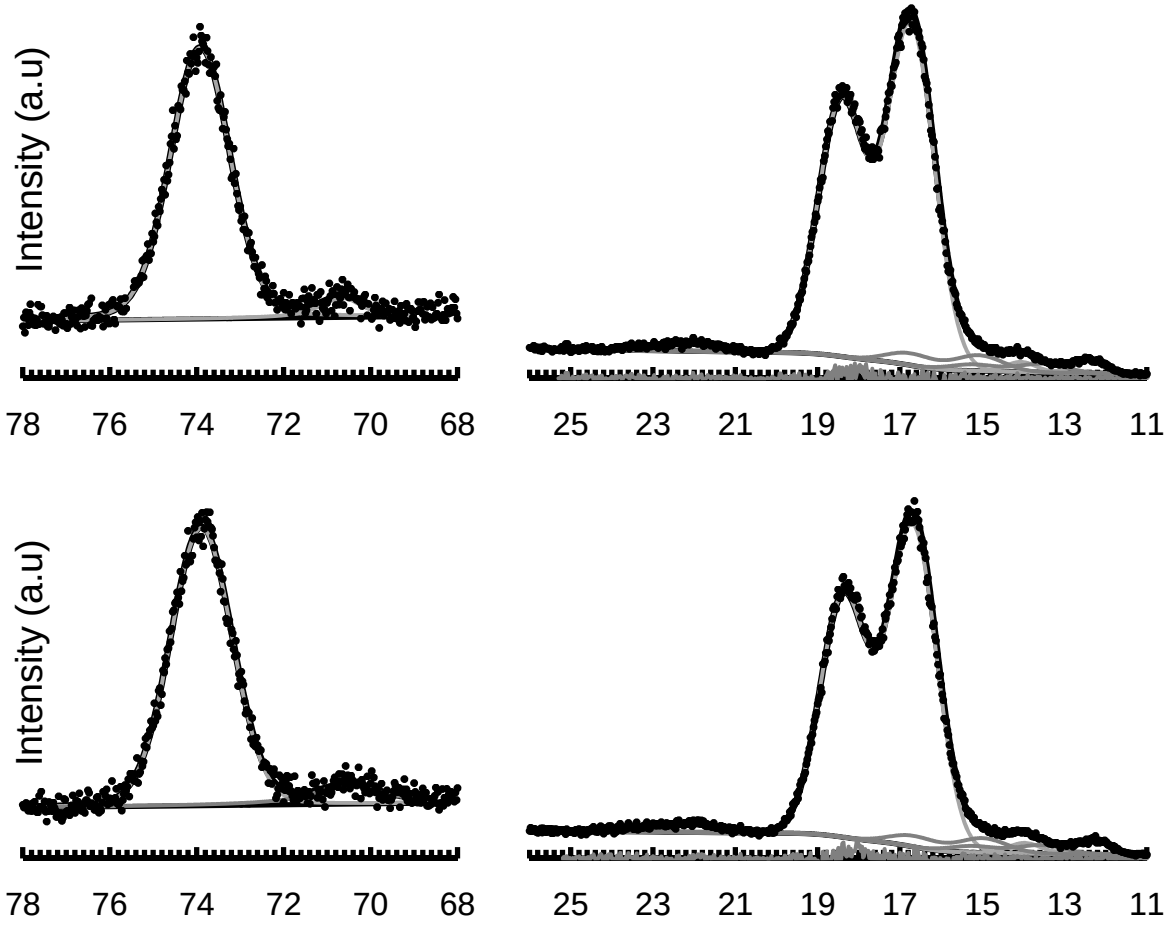


Figure R2.11 The Al 2p and Hf 4f peaks of annealed

(a) Al_2O_3/[1 nm HfO_2/1 nm Al_2O_3]$_4$/1 nm HfO_2/SiO_2/p-type Si capacitor structure, and

(b) Al_2O_3/[2 nm HfO_2/2 nm Al_2O_3]$_2$/2 nm HfO_2/SiO_2/p-type Si capacitor structure.

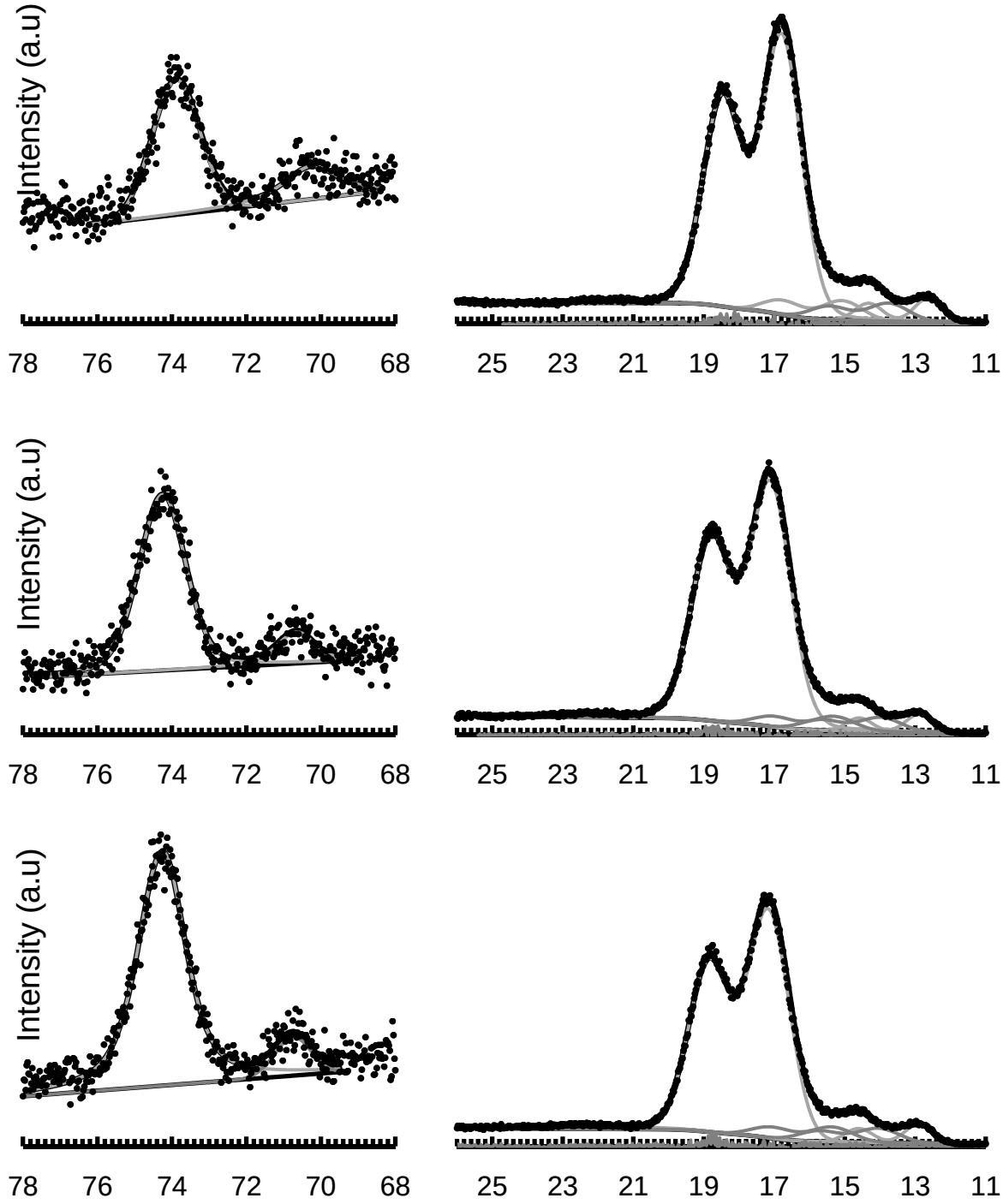


Figure R2.12 The Al 2p and Hf 4f peaks of annealed

(a) Al_2O_3/10 nm HfAlO/SiO_2/p-type Si capacitor structure,

(b) Al_2O_3/[1 nm HfO_2/1 nm Al_2O_3]$_4$/1 nm HfO_2/SiO_2/p-type Si capacitor structure, and

(c) Al_2O_3/[2 nm HfO_2/2 nm Al_2O_3]$_2$/2 nm HfO_2/SiO_2/p-type Si capacitor structure

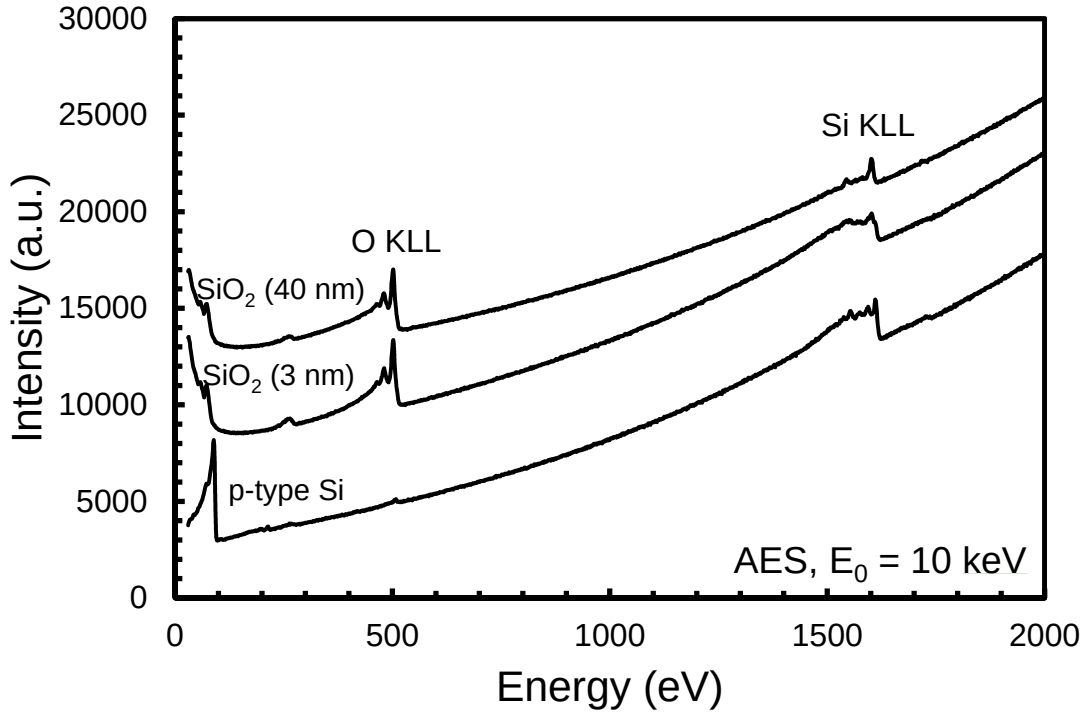


Figure R2.13 AES Spectra of SiO_2 of SiO_2 (40 nm), SiO_2/Si interface of SiO_2 (3nm) thermally grown on p-type Si, and Si of p-type Si

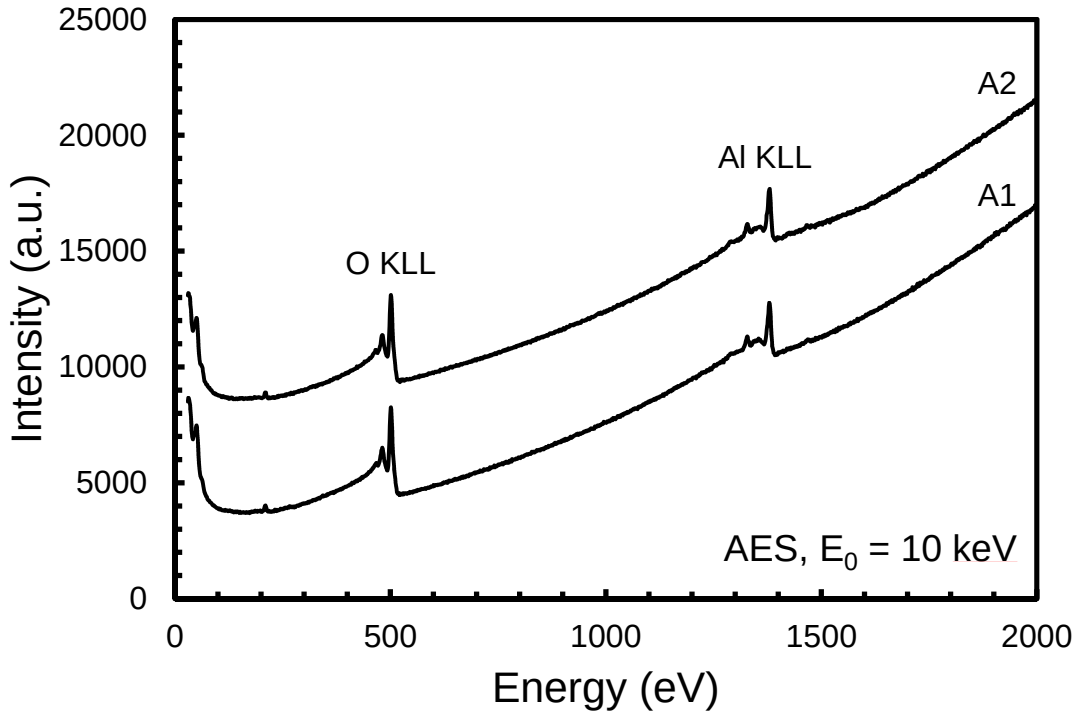
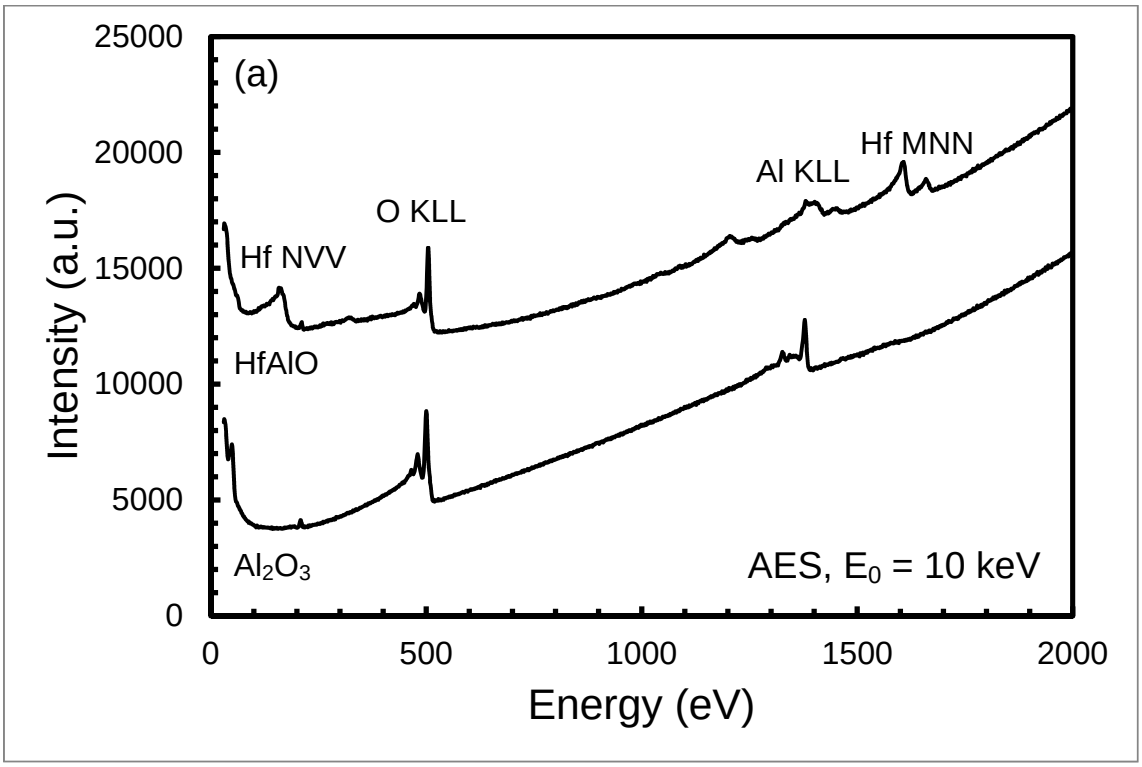


Figure R2.14 AES Spectra of as-deposited Al_2O_3/SiO_2/p-type Si capacitor structure andAl_2O_3/SiO_2/p-type Si capacitor structure annealed at 900^{o}C for 1 minute in N_2 ambient.



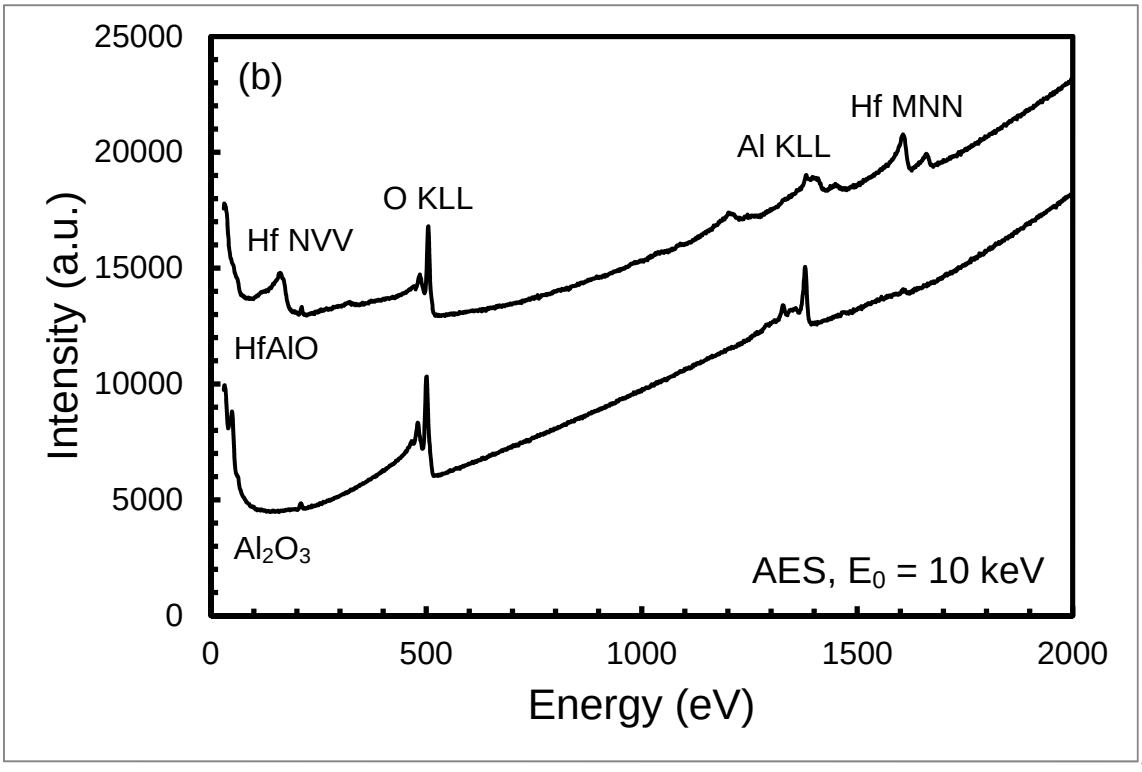
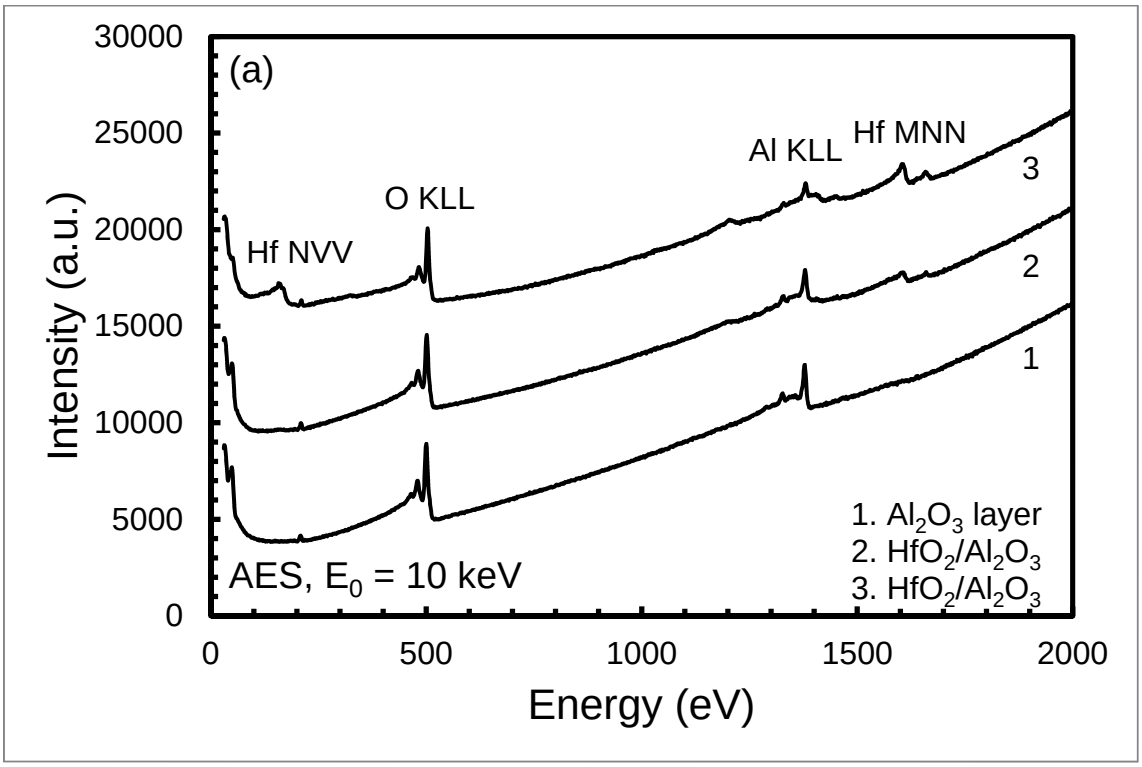


Figure R2.15 AES Spectra of (a) as-deposited Al_2O_3/HfAlO/SiO_2/p-type Si capacitor structure and (b) Al_2O_3/ HfAlO/SiO_2/p-type Si capacitor structure annealed at 900^oC for 1 minute in N_2 ambient.



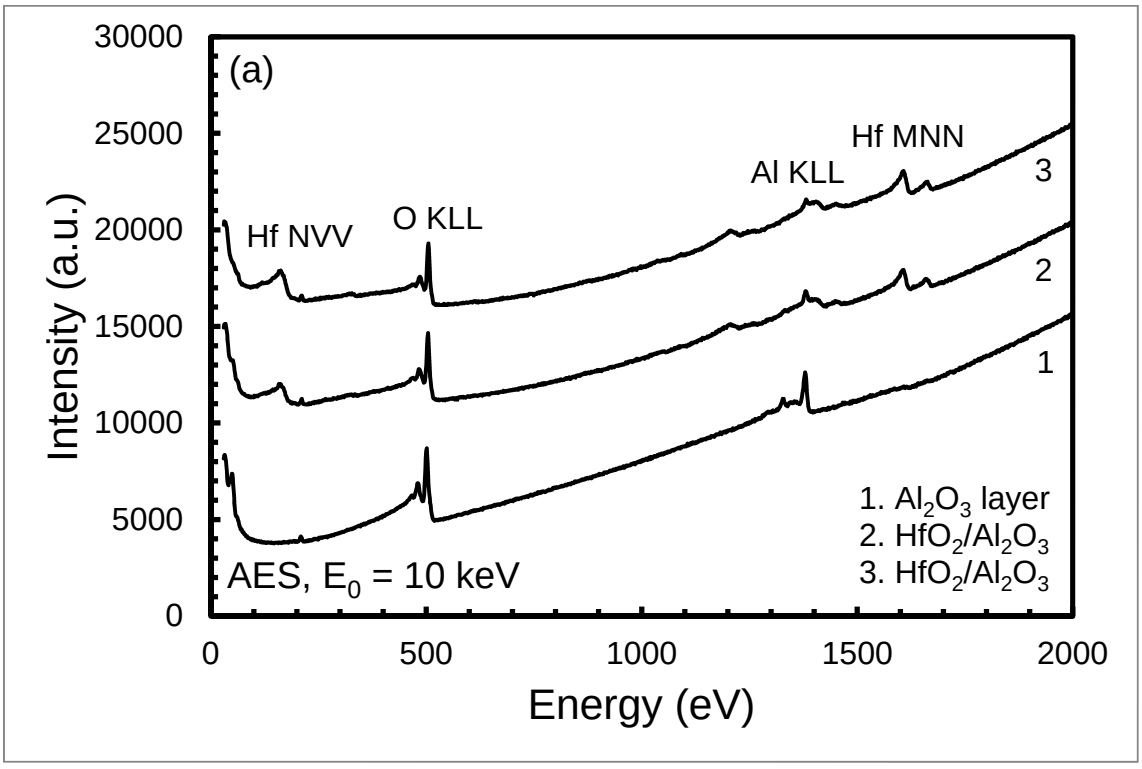
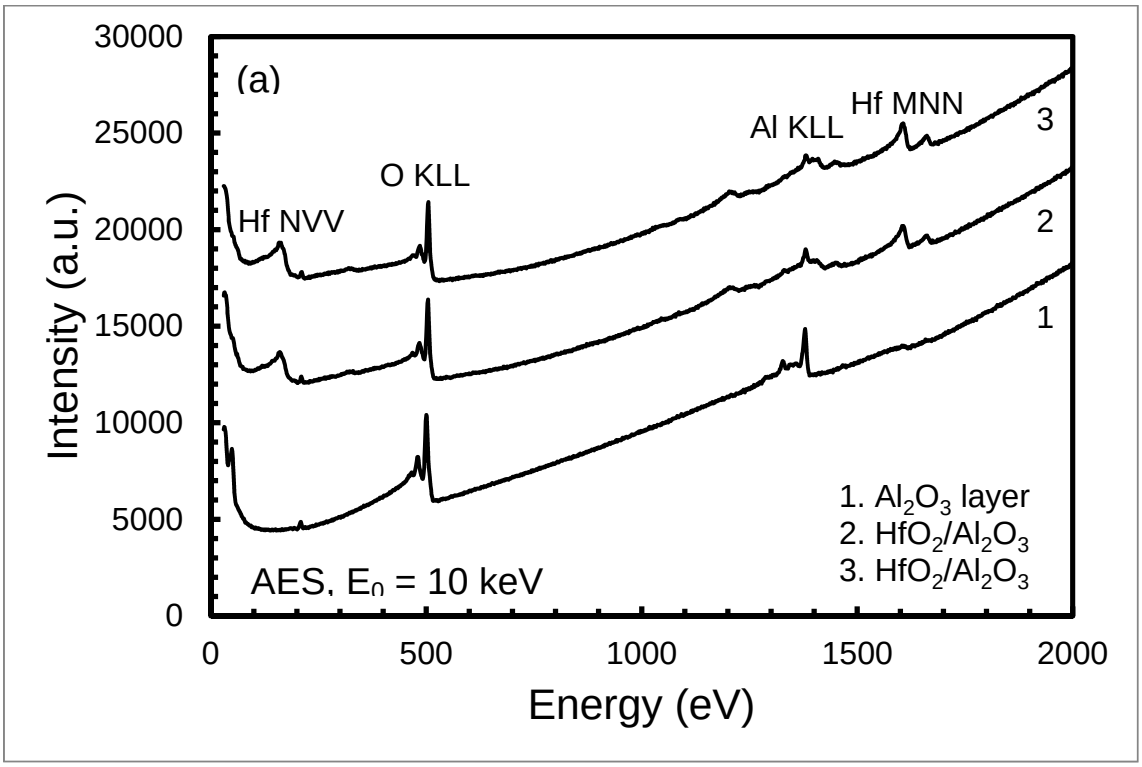


Figure R2.16 AES Spectra of (a) as-deposited $Al_2O_3/[HfO_2/Al_2O_3]_4/HfO_2/SiO_2$/p-type Si capacitor structure and (b) $Al_2O_3/[HfO_2/Al_2O_3]_4/HfO_2/SiO_2$/p-type Si capacitor structure annealed at 800^{o}C for 1 minute in N_2 ambient.



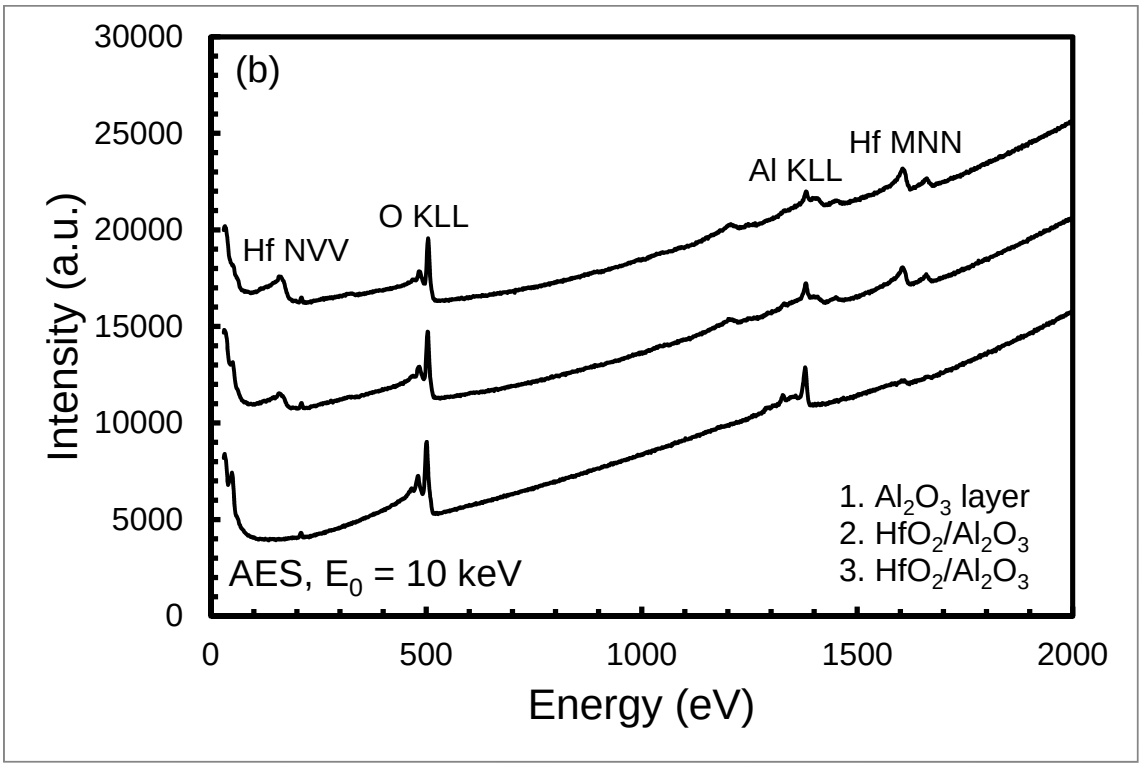


Figure R2.17 AES Spectra of (a) as-deposited $Al_2O_3/[HfO_2/Al_2O_3]_2/HfO_2/SiO_2$/p-type Si capacitor structure and (b) $Al_2O_3/[HfO_2/Al_2O_3]_2/HfO_2/SiO_2$/p-type Si capacitor structure annealed at 800^oC for 1 minute in N_2 ambient.

Chapter 3

Energy Band Alignment of the MAHOS Memory Capacitors

In chapter 3, the energy band alignment for each MAHOS structure is constructed. The energy band parameters, such as band gap, valence band offset (VBO) and conduction band offset (CBO) are extracted from experimental results. The energy band gap of materials observed by reflection energy electron loss spectroscopy (REELS) is shown and the method to determine VBO and CBO from the x-ray photoelectron spectroscopy (XPS) spectra is explained. The effect of the dipole formation on the band structure at semiconductor/semiconductor interfaces is also explained.

3.1 Background

In designing capacitor or transistor structures for non-volatile memory application, the band gap and barrier heights, which include valence band offset (VBO) and conduction band offset (CBO), represent the parameters of primary importance for the selection of materials. Some previous works on the study of charge trapping characteristics evaluated the interfacial barriers using the bulk parameters of solids[1,2]. However, the bulk parameters used may not necessarily reflect the properties of thin films. As shown in Figure 3.1, which is the reported data for thin films obtained from optical measurements, the band gap of thin films are different from those of bulk materials which depends of the type of binding and the phase of materials[3].

Such an erroneousness in barrier heights and energy band gap of materials leads to large inaccuracy in the evaluation of the charge tunneling and to a largely undefined metal–silicon work function difference (ϕ_{ms}). Therefore the knowledge of energy band parameters and barrier heights is needed to analyze the charge transport mechanisms across the semiconductor structure.

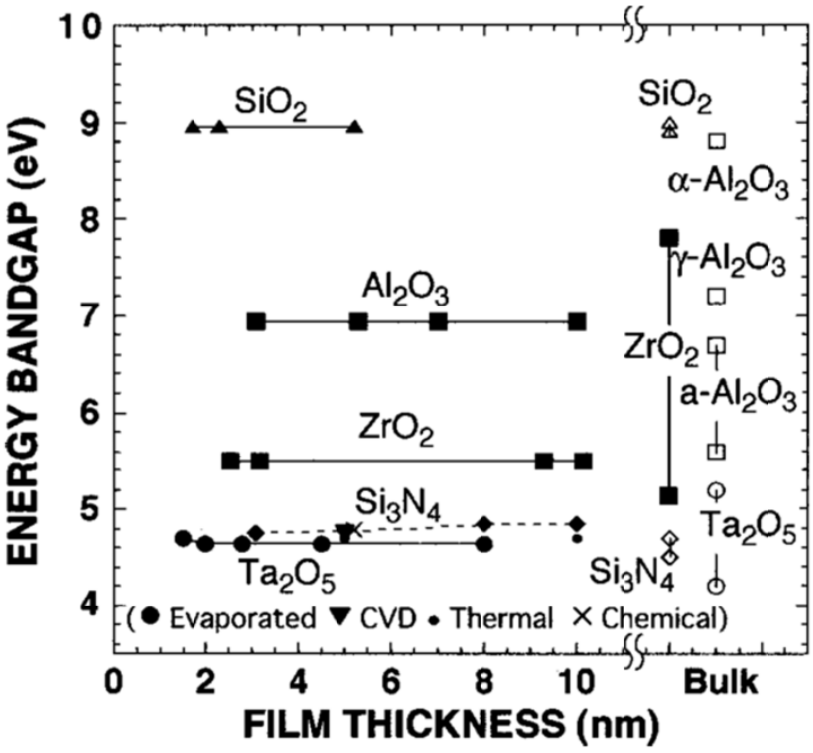


Figure 3.1 Energy band gap of gate dielectrics vs film thickness.

3.2 Energy Band Parameter Measurement by AES-REELS and XPS

3.2.1 Energy Band Diagram at the Interface between Two Materials

Energy parameters including valence band offset (VBO) and conduction band offset (CBO) are determined by applying Kraut's method [4]. The interface between a semiconductor and a metal, another semiconductor, or vacuum creates the disruption of a perfect crystal lattice which is generally accompanied by a deviation of the charge distribution near the interface from that deeper in the bulk semiconductor. As a consequence, Poisson's equation predicts a spatially varying electrostatic potential V_{BB}^{X} which bends all of the bands or energy levels by the same amount as a function of distance away from the interface. Figure 3.2 (a) shows energy band diagram at an interface with the energy of a core level E_{CL}^{X}, the valence-band maximum E_{V}^{X}, and the conduction-band minimum E_{C}^{X} in the bulk (b) and at an interface (i) with either a metal, semiconductor &, insulator, or vacuum. Binding energy E_B is measured with respect to the Fermi level E_F (E_B = 0). The band gap E_{G}^{X}, position of the

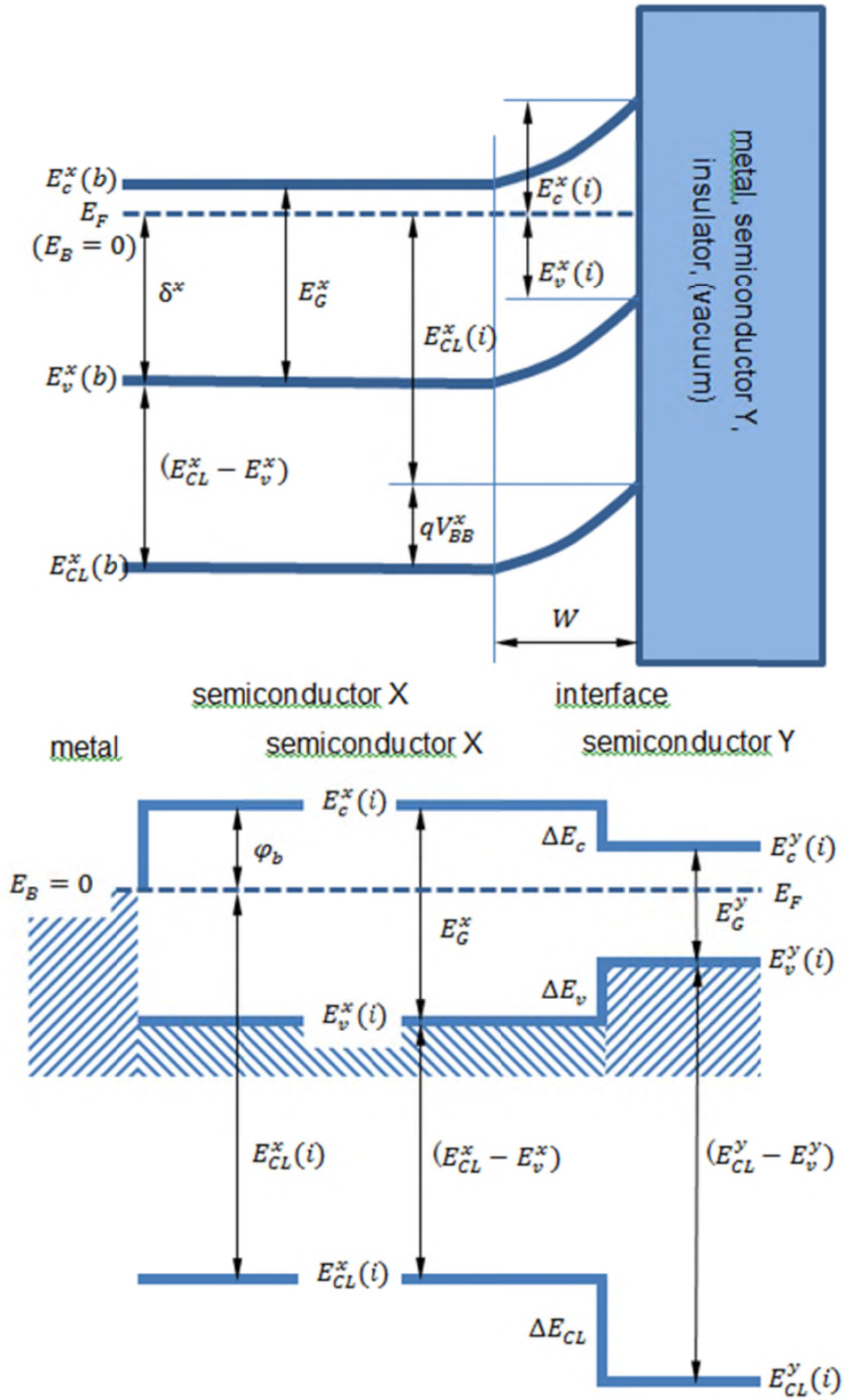


Figure 3.2 (a) Energy band diagram at an interface between a semiconductor and vacuum, metal, insulator, or a another semiconductor; (b) Schematic flat-band diagram at a metal-semiconductor or heterojunction interface.

Fermi level in the bulk relative to the valence-band edge δ^X, band-bending potential E_{BB}^X and depletion-layer width W are also shown in Figure 3.2(a). Given an XPS measurement of the position of the core level $E_{CL}^X(i)$ at the interface and the binding-energy difference ($E_{CL}^X - \mathrm{E}_V^X$) between core level E_{CL}^X and the valence-band maximum E_V^X it follows from Fig. 1(a) that the position of the conduction-band minimum at the interface is given by

$$\mathrm{E}_C^X(\mathrm{i}) = (\mathrm{E}_{CL}^X - \mathrm{E}_V^X) + \mathrm{E}_G^X - E_{CL}^X(i)$$

the position of the conduction-band minimum at the interface is given by

$$\mathrm{E}_C^X(\mathrm{i}) = (\mathrm{E}_{CL}^X - \mathrm{E}_V^X) + \mathrm{E}_G^X - E_{CL}^X(i)$$

and the band-bending potential V_{BB}^X at a surface or interface is given by

$$\mathrm{qV}_{BB}^X = (\mathrm{E}_{CL}^X - \mathrm{E}_V^X) + \delta^X - E_{CL}^X(i)$$

The energy levels defined in Figure 3.2 (a) as measured within the 20 A XPS sampling depth are shown in Figure 3.1 (b) for a heterojunction interface and for a metal-semiconductor interface. The Schottky-barrier height $\varphi_b = \mathrm{E}_C^X(\mathrm{i})$ at the metal-semiconductor interface is given by Eq. (1) and the valence-band discontinuity $\Delta\mathrm{E}_V$ at the heterojunction interface is given by

$$\Delta\mathrm{E}_V = (\mathrm{E}_{CL}^Y - \mathrm{E}_V^Y) - (\mathrm{E}_{CL}^X - \mathrm{E}_V^X) - \Delta\mathrm{E}_{CL}$$

$\Delta\mathrm{E}_{CL} = E_{CL}^Y(i) - E_{CL}^X(i)$. The effect of interface states is to shift the potential within the sampled region on both sides of an interface by the same constant value. Thus, any potential shift due to interface states or other sources of band bending cancel.

3.2.2 Energy Band Parameter Determination

There are several methods to determine the band gap of materials, including optical measurement[5-7], electron energy-loss spectroscopy (EELS)[8-10], O1s energy loss spectra of XPS[3,11,12], and reflection electron energy-loss spectroscopy (REELS)[13-15]. In this work, REELS was used because it provides faster analysis and accurate results with simple sample preparation.

By using REELS, Auger electrons passing through a solid can excite the modes of collective oscillation of conduction electrons such as plasmon and electron–hole interband transition. Transitions, between occupied and unoccupied states, are caused by the electric field caused by photons. Band-to-band transition is interpreted as electronic transition from a bound state (either valence or core) to an unoccupied state located in the conduction band. In compacted dielectric materials, the energy loss for the plasmon excitation is generally much larger than that for the excitation from the top of the valence band to the bottom of the conduction band. Therefore, the energy band gap can be determined from the onset of the energy-loss spectrum defined by linearly extrapolating the segment of maximum negative slope to the background level.

In this work, samples were bombarded with a focused low-energy electron beam of 1 keV, the probe current of 10 nA, the dwell time of 20 ms, and the probe diameter of 10 μm. The energy distribution of the reflected electrons was measured. From the zero-loss peak of all samples, the resolution of low-loss region spectra observation is about 0.9 eV, as shown in Figure 3.3.

3.2.3 Valence band offset measurement

A variety of other techniques have been used to measure band offsets in semiconductor heterojunctions. Most of these technique can be divided into two categories, including optical techniques[16-18], in which optical absorption, photoluminescence, or photoluminescence excitation spectra from quantum-well or superlattice structures are analyzed with the band offsets as fitted parameters, and electrical technique[19-21], in which either the conduction or the valence band offset is extracted from measurements, such as C-V or I-V characteristics, on electrical device structures.

The determination of band offsets by XPS has a number of advantages over other band-offset measurement techniques. Unlike many optical and electrical methods for

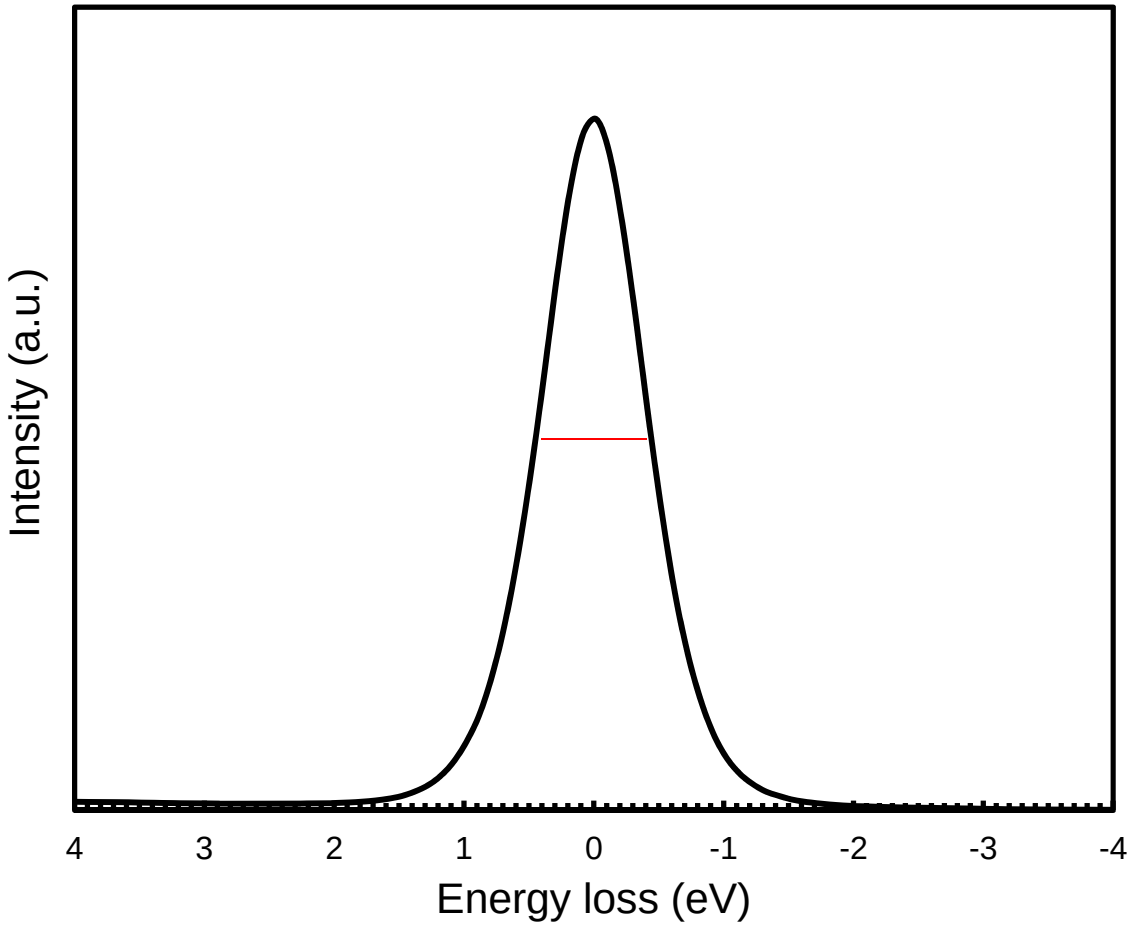


Figure 3.3 Zero Loss Peak (ZLP) observed by REELS determines the resolution of the measurement.

determining band offset, the XPS provide a direct measurement of the band offset, so that interpretation of the experimental results is fairly straightforward. In addition, the XPS technique is well suited to the study of novel material systems, since the structures required are very simple, and fabrication of functional electrical devices is not necessary.

In this work, x-ray photoelectron spectroscopy (XPS) was used to measure band offset values for MAHOS capacitor structures. In XPS, a sample is exited using x-rays, photons with energies ranging approximately from 100 eV to 10,000 eV, and the energy spectrum of electrons photoexited from the sample is measured. In our experiments we have used an Al Kα x-ray source, yielding photons with energy hv = 1486.6 eV. The energy spectrum of the

photoexited electrons yields a profile of the electronic density of states in the sample, modulated by a photoelectric cross section. By XPS, the separation between two core level peaks and between a core level peak and the valence band maximum can be measured quite precisely. The relatively high energy resolution available in XPS allows core energy separations to be measured within ± 0.02 – 0.03 eV, and core level energy to valence band maximum binding energies can be obtained to within ± 0.04 – 0.05 eV.

3.3 Band Gap of Materials in the MAHOS Capacitor Structures

3.3.1 Band Gap of SiO_2 in SiO_2/p-type Si Structures

Figure R3.1 shows the REELS low loss spectra of SiO_2, from the SiO_2 layer with the thickness of 40 nm and 3 nm thermally grown on p-type Si substrate. The band gap of SiO_2 in 40 nm SiO_2/Si structure appears at ~8.9 ± 0.05 eV which is the onset of the energy-loss spectrum represents band-to-band transition from a bound state to an unoccupied state. From the REELS low loss spectra of 3 nm SiO_2/Si structure, it is found that the spectra of SiO_2 is overlap with that of Si substrate since the depth penetration in SiO_2 layer is about 3 nm. However, the bandgap of SiO_2 can still be obtained at ~8.9 ± 0.05 eV. This result shows how to get the bandgap of thin layer on another layer.

The bandgap value of SiO_2, which is in good agreement with other values obtained from other references[3,8,22], shows that this measurement result is valid. The band gap of ultrathin SiO_2 has also been evaluated by applying ab initio model conducted by other researchers[23,24]. The result shows band gap of SiO_2 did not begin to decrease until there were fewer than three monolayers of oxide. Estimates of the changes in the associated conduction and valance band offsets for these systems indicated that a minimum of 7 Å of SiO_2 is required to obtain bulk properties. This indicates that within two monolayers of the Si channel interface, oxygen atoms do not have the full arrangement of oxygen neighbors and

therefore cannot form the full band gap that exists within the ‘‘bulk’’ of the SiO_2 film. The local energy gap in SiO_2 is directly related to the number of O second nearest neighbors, for a given O atom. The last row of O atoms which is next to the Si substrate by definition cannot have the full six nearest neighbor O atoms. The second row of O atoms from the Si interface is thus the first layer of O atoms that have the required six second-nearest neighbor O atoms. Based on the density of state calculation the valence band of SiO_2 consists mainly of O p states and the conduction band consists of Si 4s and Si 3p.

By observing the low-loss spectra of 3 nm SiO_2 on p-type Si substrate with a primary energy of 1 keV, the low loss spectrum of SiO_2 is overlap with the low loss spectrum of Si which can be identified from their plasmon loss peak. The plasmon peak of SiO_2 is observed at ~22.5 eV with a shoulder at ~12 eV, while the plasmon peak of Si is located at ~17.1 eV.

3.3.2 Band Gap of Al_2O_3 in MAHOS Structures

The band gap values for as-deposited and annealed Al_2O_3 of the MAHOS structure with Al_2O_3 as charge trapping layer were measured to be 6.7 ± 0.1 eV and 6.9 ± 0.1 eV, respectively, as shown in figure R3.2. The low band gap of as-deposited Al_2O_3 is associated with low density and low atomic coordination with the Al coordination closer to 4 and O coordination closer to 2.67[25]. After rapid thermal annealing at 900°C, crystallization of Al_2O_3 occurs and its band gap increases. The increase in the band gap value in Al_2O_3 which become 6.9 eV is associated with the metastable crystalline phase of γ-Al_2O_3. From the density of state calculation the valence band of Al_2O_3 consists mainly of O p states and the conduction band of mainly Si 4s and Si 3p. The plasmon peak is located at ~22.6 eV for as-deposited Al_2O_3. The plasmon peak is shifted to higher energy-loss after annealing.

The band gap of blocking oxide layer, which is Al_2O_3, in other MAHOS structures with HfAlO and Al_2O_3/HfO_2 nanolaminates as charge trapping layers were also observed by REELS, as shown in figure R3.3, R3.4, and R3.5, respectively. The spectra shows similar

results with the band gap values of as-deposited and annealed Al_2O_3 were measured to be 6.7 ± 0.1 eV and 6.9 ± 0.1 eV, respectively.

3.3.3 Band Gap of HfAlO and HfO_2 in MAHOS Structures

Figure R3.3 shows the REELS low-loss region of the MAHOS structures with HfAlO as charge trapping layers, before and after annealing. The band gap of as-deposited and annealed HfAlO appears to be 5.9 eV and 6.0 eV, respectively. The band gap difference between amorphous and crystalline HfAlO is related to the density and atomic coordination number of the layer. From the density of state of HfAlO, the valence band of HfAlO consists mainly of O p states and the conduction band consists of Hf 4d states. As we observed from HRTEM images the HfO_2/Al_2O_3 nanolaminate structures in sample NA1 and NB1 were broken after annealing at high temperature and transform into HfAlO in the middle part of the layer. As shown in figure R3.4 and R3.5, the band gap of HfAlO appear to be 6.0 eV, which is similar with the sample with HfAlO as charge trapping layer. From the REELS low-loss region of the structures with Al_2O_3/HfO_2 nanolaminates as charge trapping layers (figure R3.4 and R3.5), the band gap of HfO_2 was obtained which appears to be 5.8 eV and 5.9 eV, respectively.

3.4 Band Alignment in MAHOS Capacitor Structures

3.4.1 Band Alignment of SiO_2 in SiO_2/p-type Si Structures

Figure R3.6 shows the energy distance between core level (CL) and valence band maximum (VBM) of Si substrate, SiO_2/Si interface, and SiO_2 layer which are used for VBO calculation of SiO_2 with respect to Si substrate. The CL and VBM of each component are summarized in Table 3.1 The binding energy difference between Si 2p CL and VBM of p-type Si ($E_{Si\ 2p}^{Si} - E_{VBM}^{Si}$), the CL difference between SiO_2 and Si at the interface ($E_{CL(i)}^{Si} - E_{CL(i)}^{oxide}$), and the binding energy difference between Si 2p CL and VBM of SiO_2 ($E_{CL}^{Si} - E_{VBM}^{Si}$)

Table 3.1 Binding energy (BE) of the Si 2p and VBM values in SiO_2, Si substrate, and at SiO_2/p-type Si interface.

Sample	Si 2p of SiO_2		Si 2p of Si		$E_{CL}^{Si} - E_{VBM}^{Si}$	$E_{CL}^{oxide} - E_{VBM}^{oxide}$	$E_{CL(i)}^{Si} - E_{CL(i)}^{oxide}$
	BE (eV)	VBM (eV)	BE (eV)	VBM (eV)			
40 nm SiO_2/Si	103.48	4.7			98.78		
3 nm SiO_2/Si	103.50	4.7	98.96	0.2	98.8	98.76	4.54
p-type Si			98.98	0.2		98.78	

are calculated to be 98.78 eV, 4.54 eV, and 98.78 eV, respectively. By applying Kraut's method, the VBO at SiO_2/p-type Si interface is found to be ~4.5 eV, which is in agreement with other references[3,26]. The valence band spectra of 3 nm SiO_2/p-type Si structure are also shown in figure 3.9. The VBM of SiO_2 and VBM of Si at SiO_2/p-type Si interface are found to be 4.7 eV and 0.2 eV, respectively. From this result, the VBO at SiO_2/p-type Si interface also can be obtained which is 4.5 eV. The VBM of SiO_2 and VBM of Si at the interface are similar with those at SiO_2 and Si bulk phases. It is also reported previously that the binding energy of Si $2p_{SiO2}$ and Si $2p_{p\text{-type Si}}$ at SiO_2/p-type Si interface which are determined to be ~103.50 ± 0.02 eV and ~98.98 ± 0.02 eV are similar with those of bulk phases. These results show that the bands of SiO_2 and Si substrate for the 3 nm SiO_2/Si system are flat (flatband condition) in thermodynamic equilibrium. In addition, valence band offset in flatband condition can be determined by measuring the VBM difference between two materials since XPS measurement is done by using Fermi level's spectrometer as reference [27,28].

By considering the finite-oxide/semi-infinite-semiconductor contact, gap states exist on the surface of SiO_2 and at the SiO_2/Si interface. The space charges in the SiO_2 are sufficiently small to be neglected since SiO_2 has wide band gap of 8.9 eV. Thus charge transfer among the surface gap states on the surface of SiO_2, the interfacial gap states at the

SiO_2/Si interface, and space charges of Si substrate induce the electric potential distribution and the alignment of Fermi levels of SiO_2 and Si substrate is built. Since the magnitudes of gap states at the surface of SiO_2 and the SiO_2/Si interface are small enough to be negligible, the Fermi level of SiO_2 is aligned to the bulk Fermi level of Si substrate without electron transfer between SiO_2 and Si substrate and without band bends of SiO_2 and Si substrate. The energy band diagram of 3 nm SiO_2/p-type Si structure is shown in Figure 3.4. The CBO at SiO_2/p-type Si interface is calculated to be 3.5 eV. The band gap of p-type Si is set to be 1.1 eV.

3.4.2 Band Alignment of MAHOS Structures in Flatband Condition

As stated previously, valence band offset (VBO) can be determined by measuring the difference between VBM of two materials. As shown in Figure R3.7 – R3.13, the VBM of

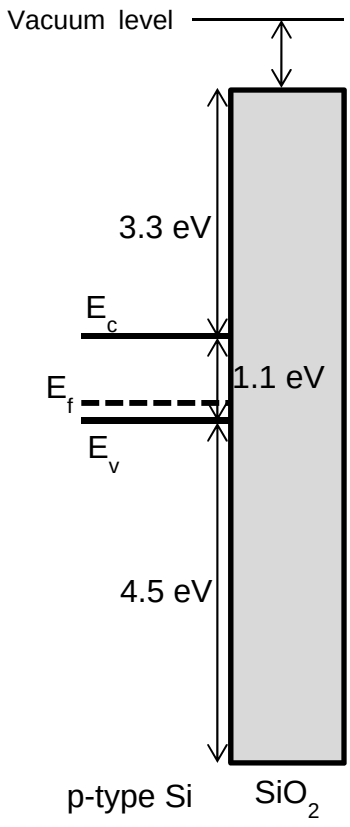


Figure 3.4 The schematic band diagram of 3 nm SiO_2/p-type Si structure in thermodynamic equilibrium.

as-deposited and annealed Al_2O_3 were obtained and are found to be ~3.1 eV. It is known that theVBM of Si is ~0.2 eV. Therefore, the VBO of Al_2O_3 with respect to Si substrate is found to be ~2.9 eV and the CBO of Al_2O_3 with respect to Si substrate is obtained to be ~2.7 eV. The VBM of Al_2O_3 was also obtained from $Al_2O_3/SiO_2/Si$ interface, as shown in Table 3.2. The VBO at flatband condition cannot be obtained directly since there is dipole formation at $Al_2O_3/SiO_2/Si$ interface which involve three layers.

Figure R3.8, Figure R3.9, and Figure R3.10 show the energy distance between core level (CL) and valence band maximum (VBM) in Al_2O_3 blocking layer, at Al_2O_3/HfAlO interface and Al_2O_3/HfAlO/SiO_2/Si interface of sample HA1, and Al_2O_3/HfO_2 interface and $Al_2O_3/HfO_2/SiO_2$/Si interface of sample NA1 and NB1, respectively. The observed value of each CL and VBM in sample HA1, NA1, and NB1 are summarized in Table 3.4. The binding energy distance among Si 2p, Hf 4f, and Al 2p at Al_2O_3/HfAlO interface and

Table 3.2 Binding energy (BE) of the Si 2p and VBM values in Al_2O_3 and Si substrate at Al_2O_3/SiO_2/p-type Si interface.

Sample	Si 2p of SiO_2		Si 2p of Si		Al 2p of Al_2O_3	
	BE (eV)	VBM (eV)	BE (eV)	VBM (eV)	BE (eV)	VBM (eV)
A1 (Al_2O_3 BO)					74.6679	3.1
A1 (Al_2O_3/SiO_2/Si interface)	103.027		98.995	0.2	75.8289	4.25
A1 (Al_2O_3/SiO_2/Si interface)	103.145		98.933	0.2	75.9869	4.4

Table 3.3 The energy distance between core level (CL) and valence band maximum (VBM) and between different CL at interface in sample A1.

Sample	$E_{CL}^{Si} - E_{VBM}^{Si}$	$E_{CL}^{Al2O3} - E_{VBM}^{Al2O3}$	$E_{CL(i)}^{Si} - E_{CL(i)}^{Al2O3}$	$E_{CL(i)}^{SiO2} - E_{CL(i)}^{Al2O3}$
A1 (Al_2O_3 BO)		71.5679		
A1 (Al_2O_3/SiO_2/Si interface)	98.795	71.5789	23.1661	27.198
A1 (Al_2O_3/SiO_2/Si interface)	98.733	71.5869	22.9461	27.158

Al_2O_3/HfAlO/SiO_2/Si interface in sample HA1 and Al_2O_3/HfO_2 and Al_2O_3/HfO_2/SiO_2/Si interface in sample NA1 and NB1 are shown in Table 3.5. For annealed samples, the energy distance between CL and VBM in Al_2O_3 blocking layer, at Al_2O_3/HfAlO interface and Al_2O_3/HfAlO/SiO_2/Si interface of sample HA2, and HfO_2/HfAlO or HfAlO/HfO_2 interface and HfAlO/HfO_2/SiO_2/Si interface of sample NA2 and NB2, are shown in Figure R3.11, Figure R3.12, and Figure R3.13, respectively. The observed value of each CL and VBM and the binding energy distance among Si 2p, Hf 4f, and Al 2p at Al_2O_3/HfAlO interface and Al_2O_3/HfAlO/SiO_2/Si interface in sample HA2 and HfO_2/HfAlO or HfAlO/HfO_2 interface and HfAlO/HfO_2/SiO_2/Si interface in sample NA2 and NB2 are shown in Table 3.6 and Table 3.7, respectively. The binding energy difference between CL and VBM is a material constant before and after interface formation. From the results, it is found that the energy distance between CL and VBM of HfAlO and HfO_2 in MAHOS structures, as-deposited and annealed samples, at different interfaces is ~14.70 ± 0.02 eV and ~14.75 ± 0.02 eV, respectively. At Al_2O_3/HfAlO interface or Al_2O_3/HfO_2 interface, even though the binding energy of Al 2p and Hf 4f are shifted to higher energy as a function of depth level from the surface, the energy distance between Al 2p and Hf 4f ($E_{CL(i)}^{Al2O3} - E_{CL(i)}^{Hf}$) is ~56.99 ± 0.03 eV. At Al_2O_3/HfAlO/SiO_2/Si or Al_2O_3/HfO_2/SiO_2/Si interface, the energy distance between Al 2p and Hf 4f ($E_{CL(i)}^{Al2O3} - E_{CL(i)}^{Hf}$) is ~56.89 ± 0.02 eV which is less than that at HfAlO or Al_2O_3/HfO_2 interface due to the dipole formation at HfAlO/SiO_2/Si or HfO_2/SiO_2/Si interface.

The VBO of HfAlO with respect to Al_2O_3 layer is obtained by applying Kraut's method with $E_{CL}^{Al2O3} - E_{VBM}^{Al2O3}$ is ~71.58 ± 0.02 eV, $E_{CL(i)}^{Al2O3} - E_{CL(i)}^{HfAlO}$ is ~56.99 ± 0.03 eV and $E_{CL}^{HfAlO} - E_{VBM}^{HfAlO}$ is ~14.70 ± 0.02 eV. It is measured to be 0.10 ± 0.03 eV, which means the VBO of HfO_2 with respect to Si substrate is 2.8 eV. By considering the band gap of as-deposited and annealed HfAlO which are 5.9 eV and 6.0 eV, respectively, the CBO of HfAlO with respect to Si substrate are 2.0 eV and 2.1 eV, respectively.

Table 3.4 The binding energy (BE) of Si 2p, Hf 4f, and Al 2p in sample HA1, NA1, and NB1.

Sample	$t_{sputtering}$ (min)	Si 2p of SiO_2	Si 2p of Si		Hf 4f		Al 2p of Al_2O_3
		BE (eV)	BE (eV)	VBM (eV)	BE (eV)	VBM (eV)	BE (eV)
HA1 (Al_2O_3/HfAlO)	2.7				17.4969	2.8	74.4769
HA1 (Al_2O_3/HfAlO/SiO_2/Si)	4.8	103.211	98.933	0.2	18.7139	4	75.6239
NA1 (Al_2O_3/HfO_2)	2.7				17.6579	2.9	74.6159
NA1 (Al_2O_3/HfO_2/SiO_2/Si)	4.5	103.232	98.901	0.2	18.6989	3.95	75.5979
NB1 (Al_2O_3/HfO_2 int. 1)	1.8				17.3599	2.6	74.3879
NB1 (Al_2O_3/HfO_2 int. 2)	2.1				17.5959	2.85	74.6119
NB1 (Al_2O_3/HfO_2 int. 3)	3				17.8469	3.1	74.8599
NB1 (Al_2O_3/HfO_2/SiO_2/Si)	5.1	103.051	98.848	0.2	18.5129	3.75	75.3799

Table 3.5 The energy distance between core level (CL) and valence band maximum (VBM) and between different CL at interface in sample HA1, NA1, and NB1.

Sample	$t_{sputtering}$ (min)	$E_{CL}^{Si} - E_{VBM}^{Si}$	$E_{CL}^{Hf} - E_{VBM}^{Hf}$	$E_{CL(i)}^{Si} - E_{CL(i)}^{Hf}$	$E_{CL(i)}^{SiO2} - E_{CL(i)}^{Hf}$	$E_{CL(i)}^{Al2O3} - E_{CL(i)}^{Hf}$
HA1 (Al_2O_3/HfAlO)	2.7		14.6969			56.98
HA1 (Al_2O_3/HfAlO/SiO_2/Si)	4.8	98.733	14.7139	80.2191	84.497	56.91
NA1 (Al_2O_3/HfO_2)	2.7		14.7579			56.958
NA1 (Al_2O_3/HfO_2/SiO_2/Si)	4.5	98.701	14.7489	80.2021	84.533	56.899
NB1 (Al_2O_3/HfO_2 int. 1)	1.8		14.7599			57.028
NB1 (Al_2O_3/HfO_2 int. 2)	2.1		14.7459			57.016
NB1 (Al_2O_3/HfO_2 int. 3)	3		14.7469			57.013
NB1 (Al_2O_3/HfO_2/SiO_2/Si)	5.1	98.648	14.7629	80.3351	84.538	56.867

Table 3.6 The binding energy (BE) of Si 2p, Hf 4f, and Al 2p in sample HA2, NA2, and NB2.

Sample	$t_{sputtering}$ (min)	Si 2p of SiO_2	Si 2p of Si		Hf 4f		Al 2p of Al_2O_3
		BE (eV)	BE (eV)	VBM (eV)	BE (eV)	VBM (eV)	BE (eV)
HA2 (Al_2O_3/HfAlO)	2.7				17.5689	2.85	74.5559
HA2 (Al_2O_3/HfAlO/SiO_2/Si)	4.5	103.20	98.973	0.2	18.7029	4	75.6319
NA2 (HfO_2/HfAlO)	2.1				17.5199	2.8	74.5669
NA2 (HfAlO/HfO_2)	2.7				17.8939	3.15	74.9049
NA2 (HfAlO/HfO_2/SiO_2/Si)	4.2	103.163	98.956	0.2	18.7409	4.0	75.6719
NB2 (HfO_2/HfAlO)	2.1				17.4679	2.75	74.5379
NB2 (HfAlO/HfO_2)	3				17.9479	3.2	74.9269
NB2 (HfAlO/HfO_2/SiO_2/Si)	4.2	103.214	98.904	0.2	18.7859	4.05	75.7221

Table 3.7 The energy distance between core level (CL) and valence band maximum (VBM) and between different CL at interface in sample HA2 NA2, and NB2.

Sample	$t_{sputtering}$ (min)	$E_{CL}^{Si} - E_{VBM}^{Si}$	$E_{CL}^{Hf} - E_{VBM}^{Hf}$	$E_{CL(i)}^{Si} - E_{CL(i)}^{Hf}$	$E_{CL(i)}^{SiO2} - E_{CL(i)}^{Hf}$	$E_{CL(i)}^{Al2O3} - E_{CL(i)}^{Hf}$
HA2 (Al_2O_3/HfAlO)	2.7		14.7189			56.987
HA2 (Al_2O_3/HfAlO/SiO_2/Si)	4.5	98.773	14.7029	80.2701	84.496	56.929
NA2 (HfO_2/HfAlO)	2.1		14.7199			57.047
NA2 (HfAlO/HfO_2)	2.7		14.7439			57.011
NA2 (HfAlO/HfO_2/SiO_2/Si)	4.2	98.756	14.7409	80.2151	84.422	56.931
NB2 (HfO_2/HfAlO)	2.1		14.7179			57.07
NB2 (HfAlO/HfO_2)	3		14.7479			56.979
NB2 (HfAlO/HfO_2/SiO_2/Si)	4.2	98.704	14.7359	80.1181	84.428	56.9362

The VBO of HfO_2 with respect to Al_2O_3 layer is obtained by applying Kraut's method with $E_{CL}^{Al2O3} - E_{VBM}^{Al2O3}$ is ~71.58 ± 0.02 eV, $E_{CL(i)}^{Al2O3} - E_{CL(i)}^{HfO2}$ is ~56.99 ± 0.03 eV and $E_{CL}^{HfO2} - E_{VBM}^{HfO2}$ is ~14.75 ± 0.02 eV. It is measured to be 0.15 ± 0.03 eV, which means the VBO of HfO_2 with respect to Si substrate is 2.75 eV. By considering the band gap of as-deposited and annealed HfO_2 which are 5.8 eV and 5.9 eV, respectively, the CBO of HfO_2 with respect to Si substrate are 1.95 eV and 2.05 eV, respectively. The band gap, valence band offset, and conduction band offset of each layer are summarized in Table 3.8 and Table 3.9. The band alignments of each structure in flatband condition are shown in Figure 3.5 – Figure 3.8.

Table 3.8 The Energy Band Parameters of Materials in the as-deposited MAHOS Capacitor Structures.

Offset	Sample	VBO	CBO
SiO_2/Si	S1	4.5 eV	3.3 eV
Al_2O_3/Si	A1	2.9 eV	2.7 eV
HfAlO/Si	HA1	2.8 eV	2.0 eV
HfO_2/Si	NA1	2.75 eV	1.95 eV
HfO_2/Si	NB1	2.75 eV	1.95 eV

Table 3.9 The Energy Band Parameters of Materials in the annealed MAHOS Capacitor Structures.

Offset	Sample	VBO	CBO
Al_2O_3/Si	A2	2.9 eV	2.9 eV
HfAlO/Si	HA2	2.8 eV	2.1 eV
HfO_2/Si	NA2	2.75 eV	2.05 eV
HfO_2/Si	NB2	2.75 eV	2.05 eV

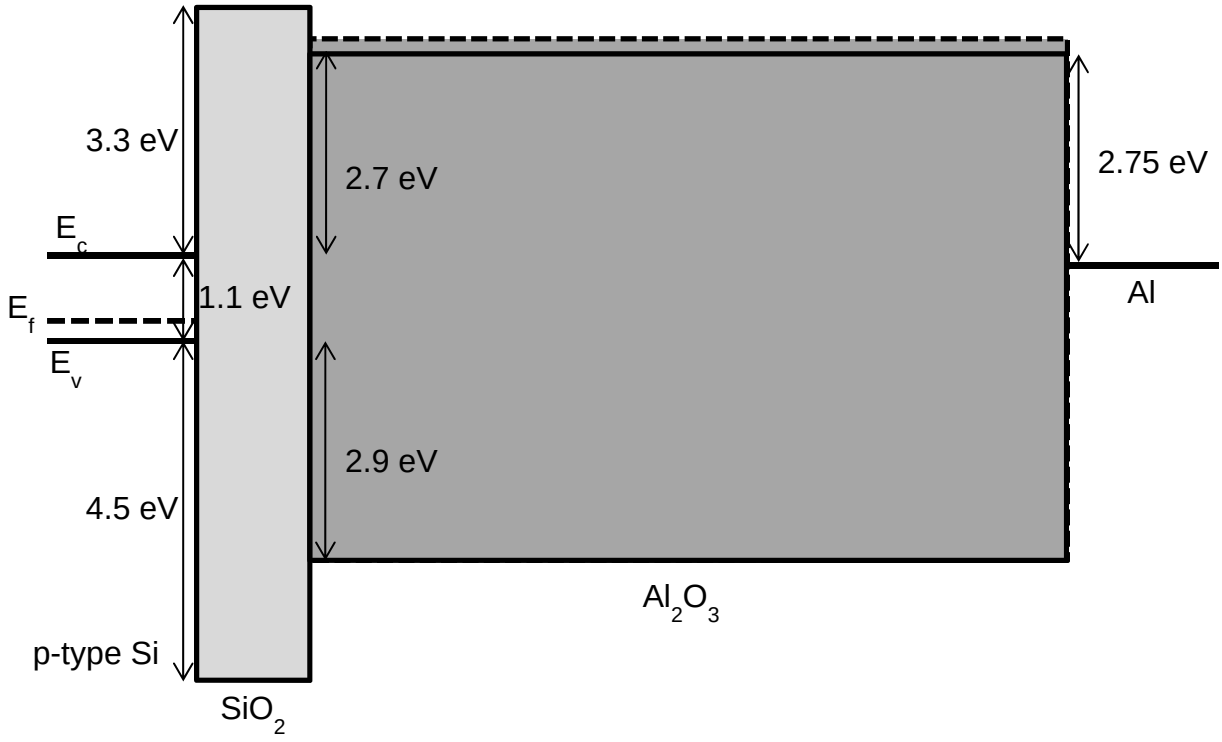


Figure 3.5 The band diagram of as-deposited (solid line) and annealed (dashed line) $Al/Al_2O_3/SiO_2$/p-type Si structure under the flat-band condition.

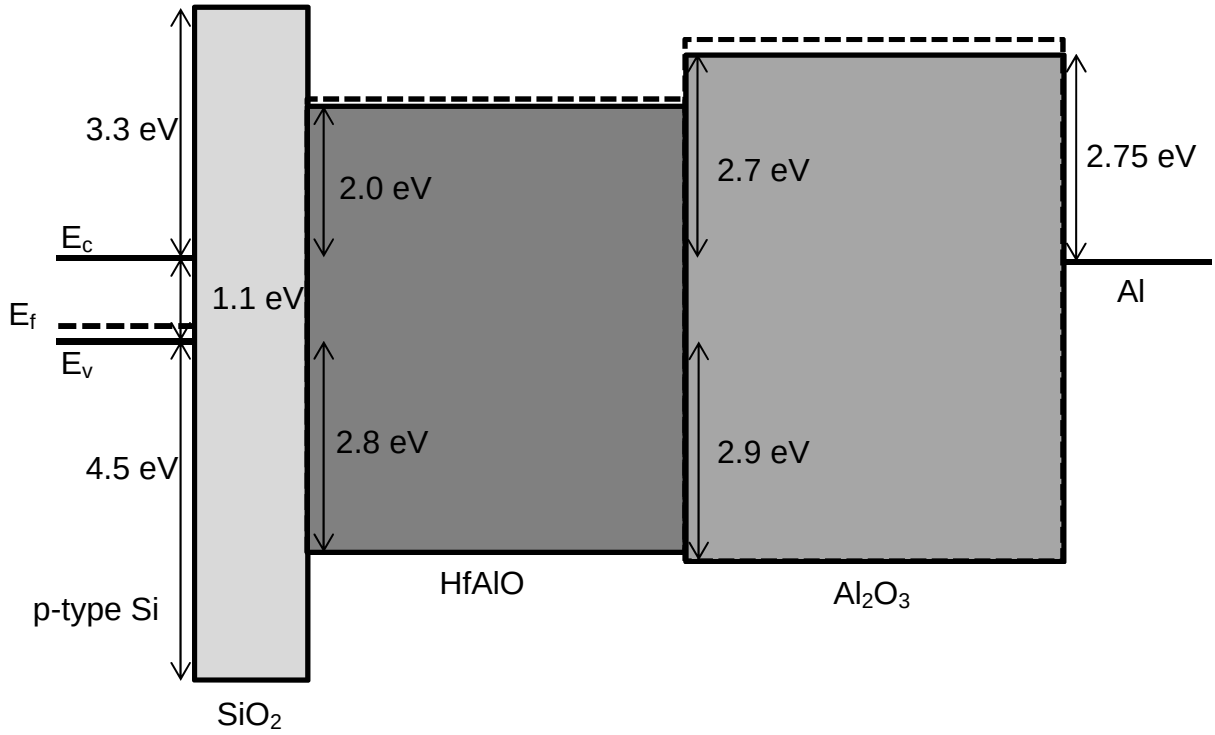


Figure 3.6 The band diagram of as-deposited (solid line) and annealed (dashed line) $Al/Al_2O_3/HfAlO/SiO_2$/p-type Si structure under the flat-band condition.

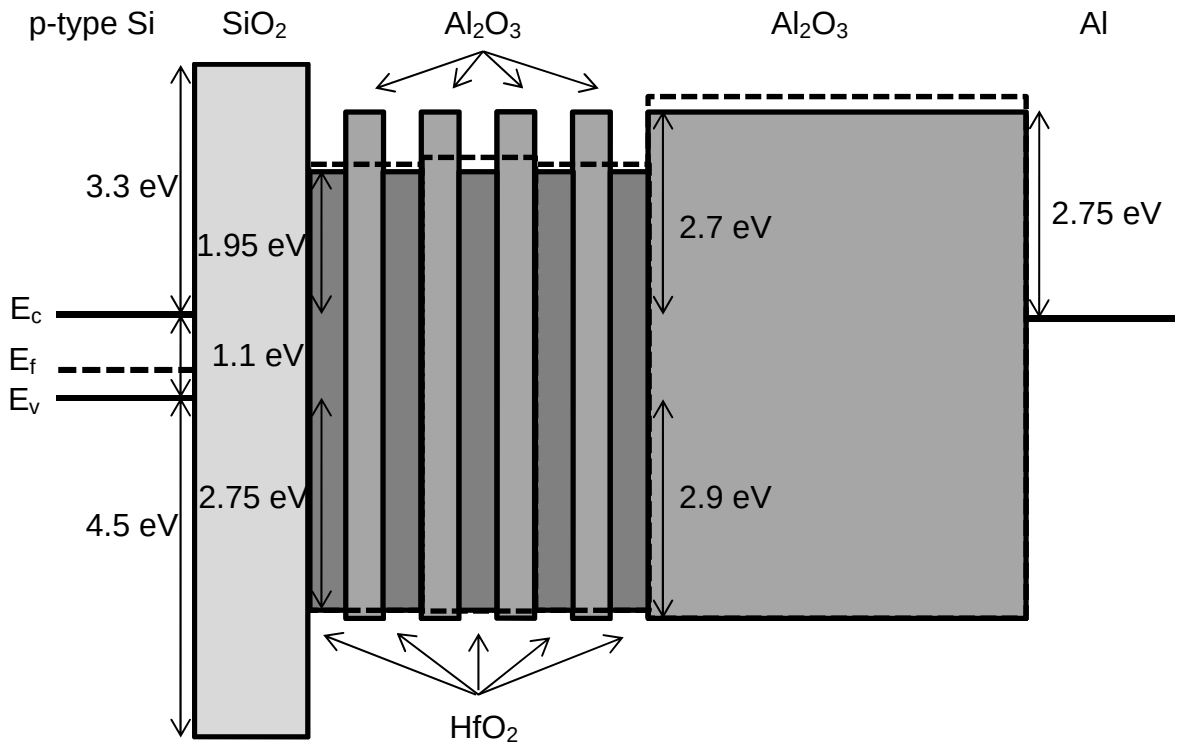


Figure 3.7 The band diagram of as-deposited (solid line) and annealed (dashed line) $Al/Al_2O_3/[HfO_2/Al_2O_3]_4/HfO_2/SiO_2$/p-type Si structure under the flat-band condition.

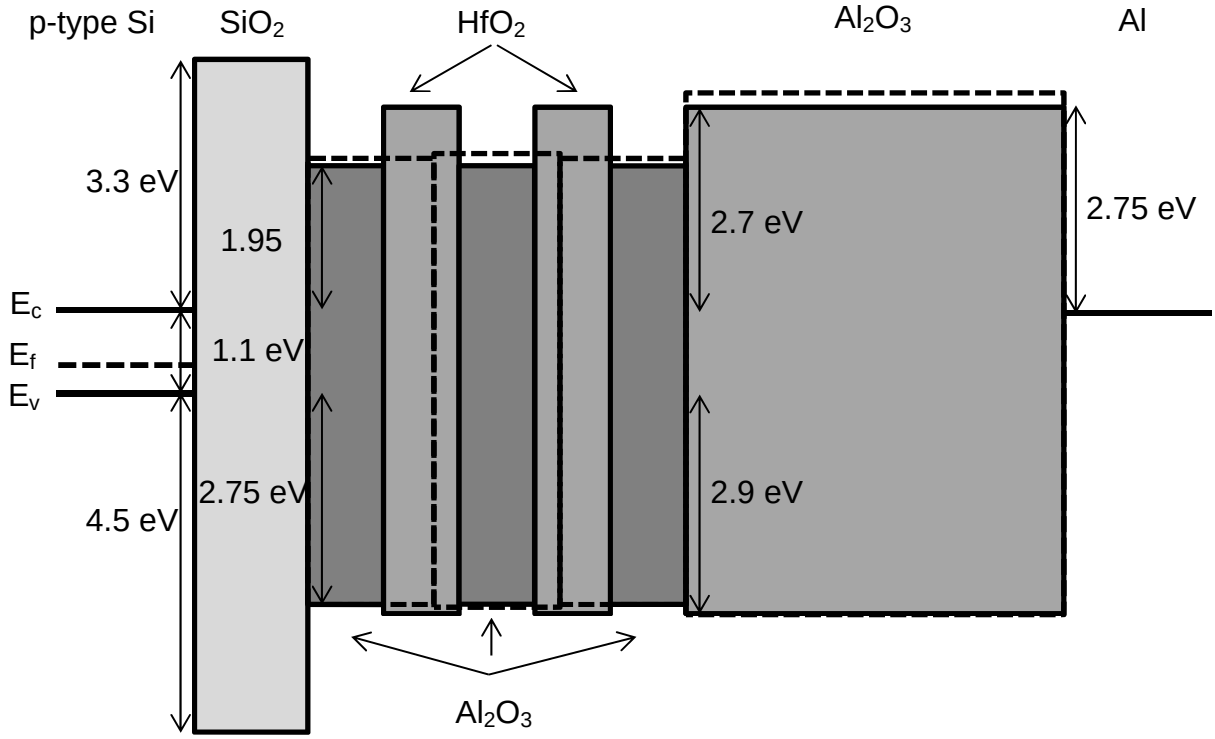


Figure 3.8 The band diagram of as-deposited (solid line) and annealed (dashed line) $Al/Al_2O_3/[HfO_2/Al_2O_3]_2/HfO_2/SiO_2$/p-type Si structure under the flat-band condition.

3.4.3 Band Alignment of High-κ Oxide in Contact with High-κ Oxide in Thermodynamic Equilibrium

The band alignment of high-κ oxide in contact with high-κ oxide is constructed using the concepts of interfacial or surface gap states and charge neutrality level (CNL). The CNL plays a role which is similar to the Fermi level. The band alignment of Al_2O_3/HfO_2 stack will be described as an example. The Fermi levels of Al_2O_3/HfO_2 stack are consistent in thermodynamic equilibrium. The alignment of Fermi levels in the structure is built by charge transfer among the surface gap states on the surface of Al_2O_3, the interfacial gap states at Al_2O_3/HfO_2, and the surface gap states on the surface of HfO_2.

The CNL of Al_2O_3 with energy gap of 8.8 eV and HfO_2 with energy gap of 6.0 eV is reported to be 5.5 eV and 3.7 eV above the valence band edge, respectively[26]. By considering the electron affinity of Al_2O_3 and HfO_2 which is 1 eV and 2.5 eV[26], respectively, the CNL of Al_2O_3 and HfO_2 is 4.3 eV and 4.8 eV measured from the vacuum level, respectively. Figure 3.14 shows the schematic energy band structure of HfO_2 and Al_2O_3 with finite thickness before contact to each other and it is assumed that in this case the CNL of HfO_2 is also lower than the CNL of Al_2O_3. Based on measurement results by REELS, the band gap of Al_2O_3 and HfO_2 is set to be 6.7 eV and 5.8 eV, respectively. For finite-HfO_2 on finite-Al_2O_3, gap state exists at the Al_2O_3/HfO_2 interface. The density of gap states lying in the band gap of HfO_2 and Al_2O_3 cannot be negligible. The contact of finite-HfO_2 on finite-Al_2O_3 follows same fundamental principle as semiconductor/semiconductor contact. When Al_2O_3 is in contact with HfO_2, electron will transfer from Al_2O_3 to HfO_2 in order to balance the Fermi levels of HfO_2 and Al_2O_3 stack since the CNL of HfO_2 is lower than that of Al_2O_3. There are positive charges on the Al_2O_3 side, while equal negative charges on the HfO_2 side. An electrical dipole is induced between HfO_2 and Al_2O_3 stacks. As a consequence, the energy bands of Al_2O_3 stack bend upward as shown in Figure 3.9.

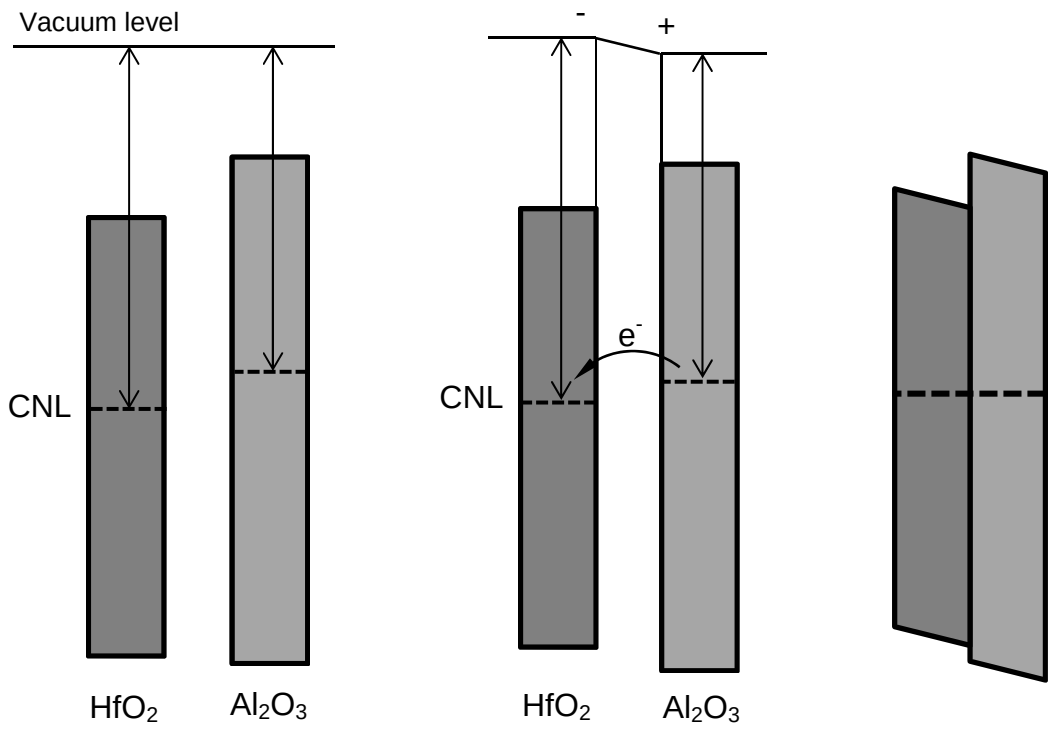


Figure 3.9 The schematic band diagram of a separated HfO_2 and Al_2O_3, the effect of charge transfer between HfO_2 and Al_2O_3, and Al_2O_3/HfO_2 structure in thermodynamic equilibrium.

The NB1 sample with the structure of $Al_2O_3/[HfO_2/Al_2O_3]_4/HfO_2/SiO_2$/p-type Si substrate was sputtered for 1.8, 2.1, and 3.0 minutes and the peak of Al 2p of Al_2O_3 and Hf 4f HfO_2 were obtained at three different depth levels. As summarized in Table 3.5, the Al 2p of Al_2O_3 shifted to lower binding energy and suggested that the band of Al_2O_3/HfO_2 bends upward at the depth level which is close to Al_2O_3 blocking layer.

3.4.4 Band Alignment of High-κ Oxide in Contact with SiO_2/p-type Si Structures in Thermodynamic Equilibrium

It is suggested that there is a minimum thickness of SiO_2, so the the dipole formation at high-κ oxide/SiO_2 interface in high-κ oxide/SiO_2/p-type Si structure will not be affected by Si substrate. The minimum thickness of SiO_2 observed at high-κ oxide/SiO_2/p-type Si was about 5 nm[29]. When the thickness of SiO_2 is more than 5 nm, internal electric field is generated at high-κ oxide/SiO_2 interface in high-κ oxide/SiO_2/p-type Si structure. In case of HfO_2/SiO_2 interface, by considering the CNL of HfO_2 which is 4.8 eV from vacuum level, the

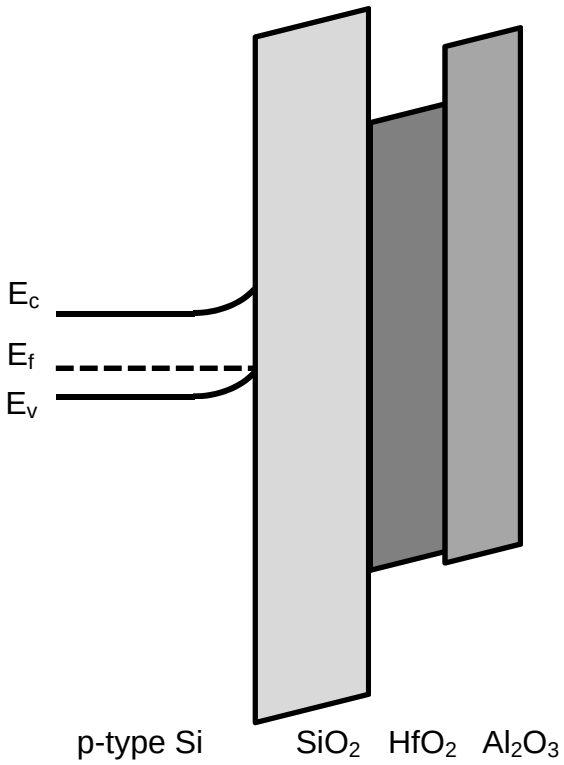


Figure 3.10 The band alignment of $Al_2O_3/HfO_2/SiO_2$/p-type Si structure in thermodynamic equilibrium.

CNL of HfO_2 will be higher than the Fermi level of SiO_2/p-type Si structures. Therefore, there will be positive charges on HfO_2 side and negative charges on SiO_2 side. Electrical dipole is induced between HfO_2 and SiO_2 and the energy band of HfO_2/SiO_2 bends downward. This band bending is indicated by the energy difference of Si 2p of SiO_2 and Si 2p of Si which is higher than the energy difference of Si 2p of SiO_2 and Si 2p of Si in SiO_2/Si structure.

In high-κ oxide/SiO_2/Si structure with thickness of SiO_2 lower than 5 nm, as in this work, the energy difference of Si 2p of SiO_2 and Si 2p of Si in high-κ oxide/SiO_2/p-type Si structure is lower than that of in SiO_2/p-type Si structure which is reported to be about 4.3 eV for all MAHOS structures, while the energy difference of Si 2p of SiO_2 and Si 2p of Si in SiO_2/p-type Si structure is reported to be 4.5 eV. This result suggests that the dipole formed at high-κ oxide/SiO_2 is affected by p-type Si substrate. In this case, the alignment of Fermi levels are built by charge transfer among the surface gap states on the surface of high-κ oxide, the interfacial gap states at high-κ oxide/SiO_2 and SiO_2/Si interfaces, and the space charges of

Si substrate. As summarized in Table 3.5 for as-deposited MAHOS structures and Table 3.7 for annealed MAHOS structures, all results suggest that the energy band of high-κ oxide /SiO_2 bends upward which means there are positive charges in SiO_2/p-type Si stack. Figure 3.10 shows the band alignment of Al_2O_3/HfO_2/SiO_2/p-type Si structure in thermodynamic equilibrium by taking the result for sample NB1 as an example.

3.5 Summary

In this chapter, the energy band parameters, including bandgap, valence band offset (VBO), and conduction band offset (CBO) of materials in as-deposited and annealed MAHOS structures with Al_2O_3, HfAlO, $[HfO_2/Al_2O_3]_4/HfO_2$ nanolaminates, and $[HfO_2/Al_2O_3]_2/HfO_2$ nanolaminates as as charge trapping layer has been investigated by reflection electron energy-loss spectroscopy (REELS) and x-ray photoelectron spectroscopy (XPS). The band alignment in flatband condition was constructed. The band alignment of high-κ oxide in contact with high-κ oxide and high-κ oxide in contact with SiO_2/p-type Si substrate were evaluated by considering the concepts of interfacial or surface gap states and charge neutrality level (CNL).

From all results discussed in this chapter, we can summarize some important points:

1. The bandgap measurement by REELS in this work is valid and provides fast and accurate results as indicated by bandgap measurement of SiO_2 in 40 nm SiO_2/p-type Si and 3 nm SiO_2/p-type Si with the bandgap value of about 8.9 eV. The bandgap of material depend on its phase and structure, e.g. the band gap of Al_2O_3 is 6.7 eV for amorphous and 6.9 eV for crystalline which is different from the bulk one which is 8.8 eV. The bandgap of HfAlO is found to be slightly higher than that of HfO_2.
2. It is confirmed that the energy distance between core level (CL) and valence band maximum (VBM) is constant for a material. The valence band offset (VBO) can be

determined by measuring the VBM difference of two materials since it is found that at flatband condition the CL and VBM position are the same for SiO_2 and p-type Si at bulk and interface.

3. The distance between Al 2p and Hf 4f is constant at Al_2O_3/HfO_2 and $HfAlO/HfO_2$ interfaces even though its CL position shifts as a function of depth level. The CL position shifts of Al 2p and Hf 4f is due to dipole formation at Al_2O_3/HfO_2 and $HfAlO/HfO_2$ interfaces.
4. The band alignment in high-κ oxide in contact with SiO_2/p-type Si structure thermodynamical equilibrium is affected by Si substrate. The alignment of Fermi levels are built by charge transfer among the surface gap states on the surface of high-κ oxide, the interfacial gap states at high-κ oxide/SiO_2 and SiO_2/Si interfaces, and the space charges of Si substrate.

References

[1] Yan Ny Tan, Wai Kin Chim, Wee Kiong Choi, Moon Sig Joo, and Byung Jin Cho. Hafnium Aluminum Oxide as Charge Storage and Blocking-Oxide Layers in SONOS-Type Nonvolatile Memory for High-Speed Operation. IEEE Transactions on Electron Devices, Vol. 53, No. 4, April 2006.

[2] S. Maikap, H. Y. Lee, T-Y. Wang, P-J. Tzeng, C. C. Wang, L. S. Lee, K. C. Liu, J-R. Yang, and M-J. Tsai. Charge Trapping Characteristics of Atomic-Layer-Deposited HfO_2 Films with Al_2O_3 as a Blocking Oxide for High-Density Non-Volatile Memory Device Applications. Semicond. Sci. Technol. 22 (2007) 884–889.

[3] Seiichi Miyazaki. Photoemission Study of Energy-Band Alignments and Gap-State Density Distributions for High-κ Gate Dielectrics. Journal of Vacuum Science & Technology B 19, 2212 (2001).

[4] E. A. Kraut, R. W. Grant, J. R. Waldrop, and S. P. Kowalczyk. Precise Determination of the Valence-Band Edge in X-Ray Photoemission Spectra: Application to Measurement of Semiconductor Interface Potentials. Physical Review Letters, Volume 44, Number 24, 16 June 1980.

[5] Eunah Kim, Zhong-Tao Jiang, and Kwangsoo No. Measurement and Calculation of Optical Band Gap of Chromium Aluminum Oxide Films. Jpn. J. Appl. Phys. 39 4820 (2000).

[6] Kaupo Kukli, Jaan Aarika, Aleks Aidlaa, Oksana Kohana, Teet Uustarea, Väino Sammelselg. Properties of tantalum oxide thin films grown by atomic layer deposition. Thin Solid Films Volume 260, Issue 2, 15 May 1995, Pages 135–142.

[7] Modaffer A. Mohammed. Correlation between Thickness, Grain Size and Optical Band Gap of CdI2 Film. Eng. & Tech. Journal,Vol.27, No. 6, 2009.

[8] Jucheol Park, Sung Heo, Jae-Gwan Chung, Heekoo Kim, Hyung Ik Lee, Kihong Kim,

Gyeong-Su Park. Bandgap measurement of thin dielectric films using monochromated STEM-EELS. Ultramicroscopy 109 (2009) 1183–1188.

[9] H Amari, HY Zhang, L Geelhaar, C Chèze, M J Kappers, and T Walther. Nanoscale EELS analysis of elemental distribution and bandgap properties in AlGaN epitaxial layers. Journal of Physics: Conference Series 326 (2011) 012039.

[10] M. Stöger-Pollach. Optical properties and bandgaps from low loss EELS: Pitfalls and solutions. Micron Volume 39, Issue 8, December 2008, Pages 1092–1110.

[11] M. L. Huang, Y. C. Chang, C. H. Chang, and T. D. Lin. Energy-band parameters of atomic-layer-deposition Al_2O_3/InGaAs heterostructure. Applied Physics Letters 89, 012903 (2006).

[12] H. Y. Yu, M. F. Li, B. J. Cho, C. C. Yeo, M. S. Joo, D.-L. Kwong, J. S. Pan, C. H. Ang, J. Z. Zheng, and S. Ramanathan. Energy gap and band alignment for $(HfO_2)_x(Al_2O_3)_{1-x}$ on (100) Si. Applied Physics Letters 81, 376 (2002).

[13] H. Jin, S. K. Oh, and H. J. Kang. Band alignment in ultrathin Hf–Al–O/Si interfaces. Applied Physics Letters 87, 212902 (2005).

[14] Hua Jin, Suhk Kun Oh, Hee Jae Kang, and Sven Tougaard. Electronic properties of ultrathin HfO_2, Al_2O_3, and Hf–Al–O dielectric films on Si(100) studied by quantitative analysis of reflection electron energy loss spectra. Journal of Applied Physics 100, 083713 (2006).

[15] M. L. Huang, Y. C. Chang, Y. H. Chang, T. D. Lin, J. Kwo, and M. Hong. Energy-band parameters of atomic layer deposited Al_2O_3 and HfO_2 on $In_xGa_{1-x}As$. Applied Physics Letters 94, 052106 (2009)

[16] C. L. Chang, L. P. Rokhinson, and J. C. Sturm. Direct optical measurement of the valence band offset of $p^+Si_{1-x-y}Ge_xC_y/p^-Si(100)$ by heterojunction internal photoemission. Appl. Phys. Lett. 73, 3568 (1998).

[17] P. M. Young, E. Runge, M. Ziegler, and H. Ehrenreich. Optical absorption and exciton linewidths of $Zn_{1-x}Cd_xSe$ quantum wells. Phys. Rev. B 49, 7424 (1994).

[18] D. Vignauda and F. Mollot. Conduction band offset in the $Al_xGa_yIn_{1-x-y}P/Ga_{0.52}In_{0.48}P$ system as studied by luminescence spectroscopy. Journal of Applied Physics, Volume 93, Number 1, (2003).

[19] S. Khorram, C. H. Chern, and K. L. Wang. Measurement of Valence Band Offset in Strained Ge_xSi_{1-x}/Si Heterojunctions. MRS Proceedings, Volume 220, 1991.

[20] J.-L.P.J. van der Steen, R.J.E. Hueting, G.D.J. Smit, T. Hoang, J. Holleman, J. Schmitz. Valence Band Offset Measurements on Thin Silicon-on-Insulator MOSFETs. IEEE Electron Device Letters, Volume:28, Issue: 9, Sept. 2007. 821 – 824.

[21] T. van Hemert, B.K. Kemaneci, R.J.E. Hueting, D. Esseni, M.J.H. van Dal, J. Schmitz. Extracting the conduction band offset in strained FinFETs from subthreshold-current measurements. Solid-State Device Research Conference (ESSDERC), 2011 Proceedings, 275 – 278.

[22] Eric Bersch, Sylvie Rangan, and Robert Allen Bartynski. Band offsets of ultrathin high-κ oxide films with Si. Physical Review B 78, 085114 (2008).

[23] Shaoping Tang, Robert M Wallace, Alan Seabaugh, Dominic King-Smith. Evaluating the minimum thickness of gate oxide on silicon using first-principles method. Applied Surface Science, Volume 135, Issues 1–4, September 1998, 137–142.

[24] J. B. Neaton, D. A. Muller, and N. W. Ashcroft. Electronic Properties of the Si/SiO2 Interface from First Principles. Phys. Rev. Lett. 85, 1298 (2000).

[25] D. Liu, S. J. Clark, and J. Robertson. Oxygen vacancy levels and electron transport in Al_2O_3. Applied Physics Letters 96, 032905 (2010)

[26] John Robertson. Band offsets of wide-band-gap oxides and implications for future electronic devices. Journal of Vacuum Science & Technology B 18, 1785 (2000).

[27] Y. C. Chang, M. L. Huang, K. Y. Lee, Y. J. Lee, T. D. Lin, M. Hong, J. Kwo, T. S. Lay, C. C. Liao, and K. Y. Cheng. Atomic-layer-deposited HfO_2 on $In_{0.53}Ga_{0.47}As$: Passivation and energy-band parameters. Applied Physics Letters 92, 072901 (2008).

[28] H. Y. Yu, M. F. Li, B. J. Cho, C. C. Yeo, M. S. Joo, D.-L. Kwong, J. S. Pan, C. H. Ang, J. Z. Zheng, and S. Ramanathan. Energy gap and band alignment for $(HfO_2)_x$ $(Al_2O_3)_{1-x}$ on (100) Si. Applied Physics Letters 81, 376 (2002).

[29] Li Qiang Zhu, Koji Kita, Tomonori Nishimura, Kosuke Nagashio, Sheng Kai Wang, and Akira Toriumi. Observation of Dipole Layer Formed at High-κ Dielectrics/SiO_2 Interface with X-ray Photoelectron Spectroscopy. Applied Physics Express 3 (2010) 061501.

Figures of Results

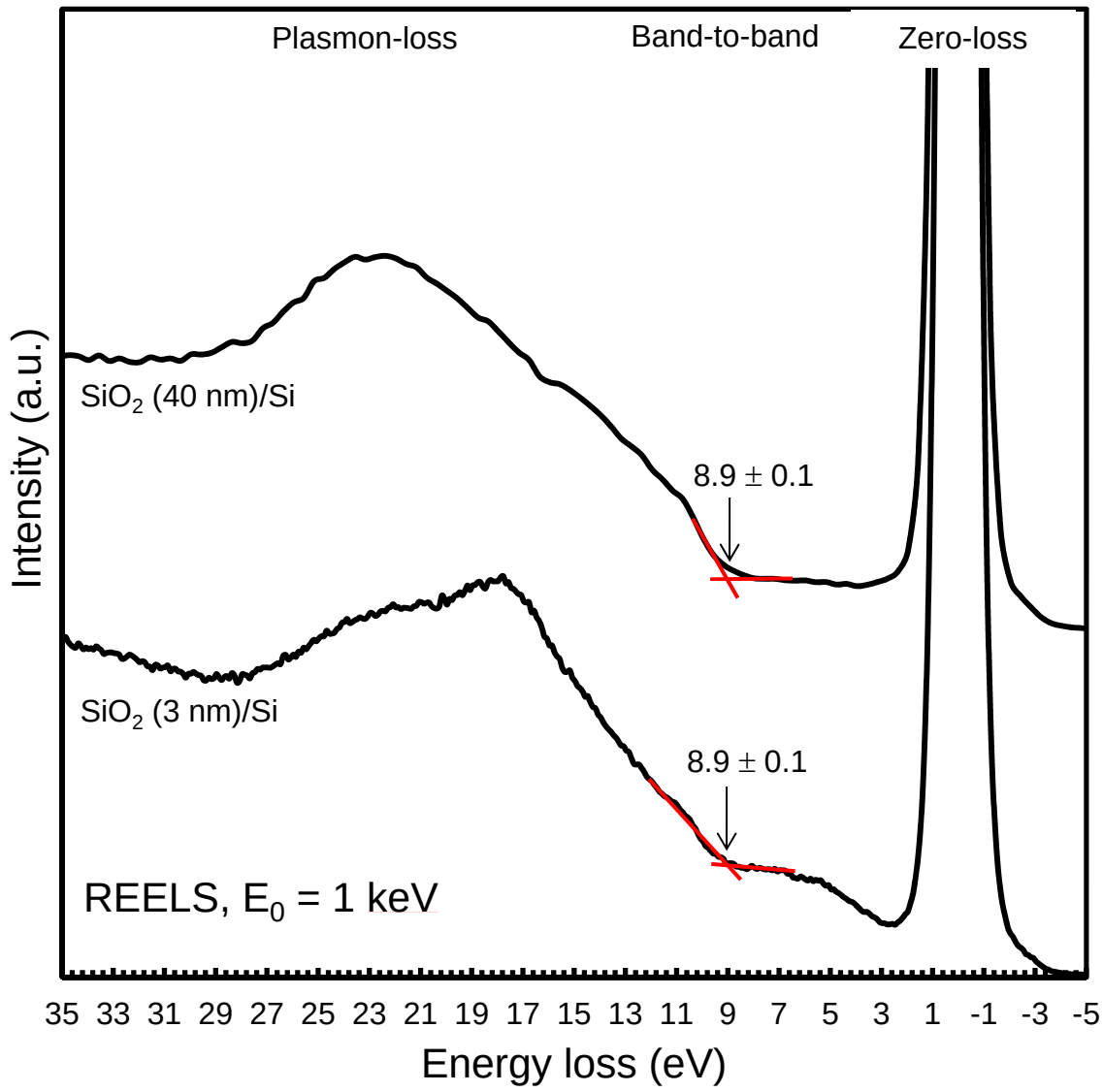


Figure R3.1 The low-loss region of REELS spectra of SiO_2 (t = 3 nm) grown on p-type Si and SiO_2 (t = 3 nm) grown on p-type Si.

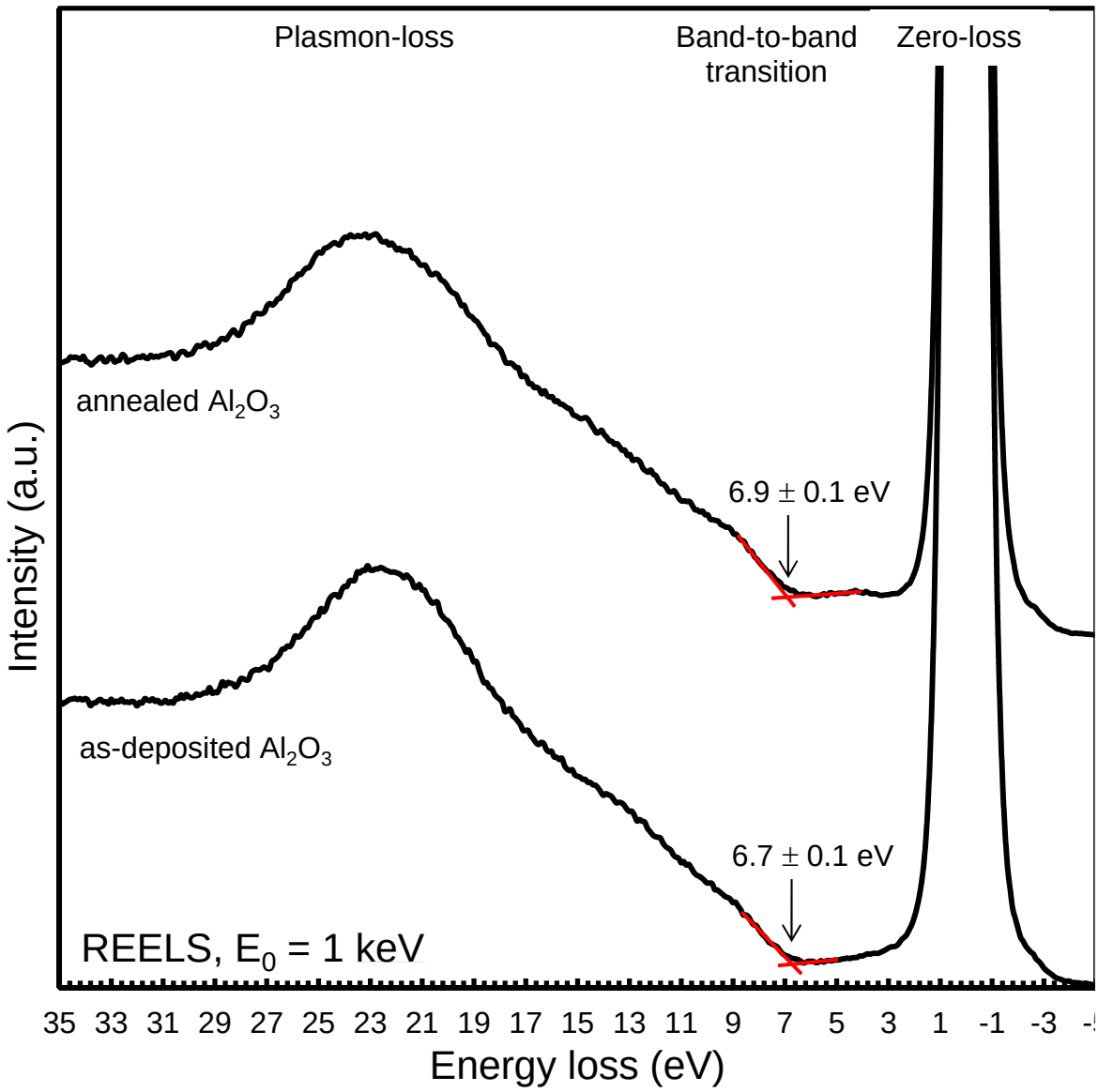


Figure R3.2 The low-loss region of REELS spectra of Al_2O_3 from as-deposited and annealed Al_2O_3/SiO_2/p-type Si capacitor structure.

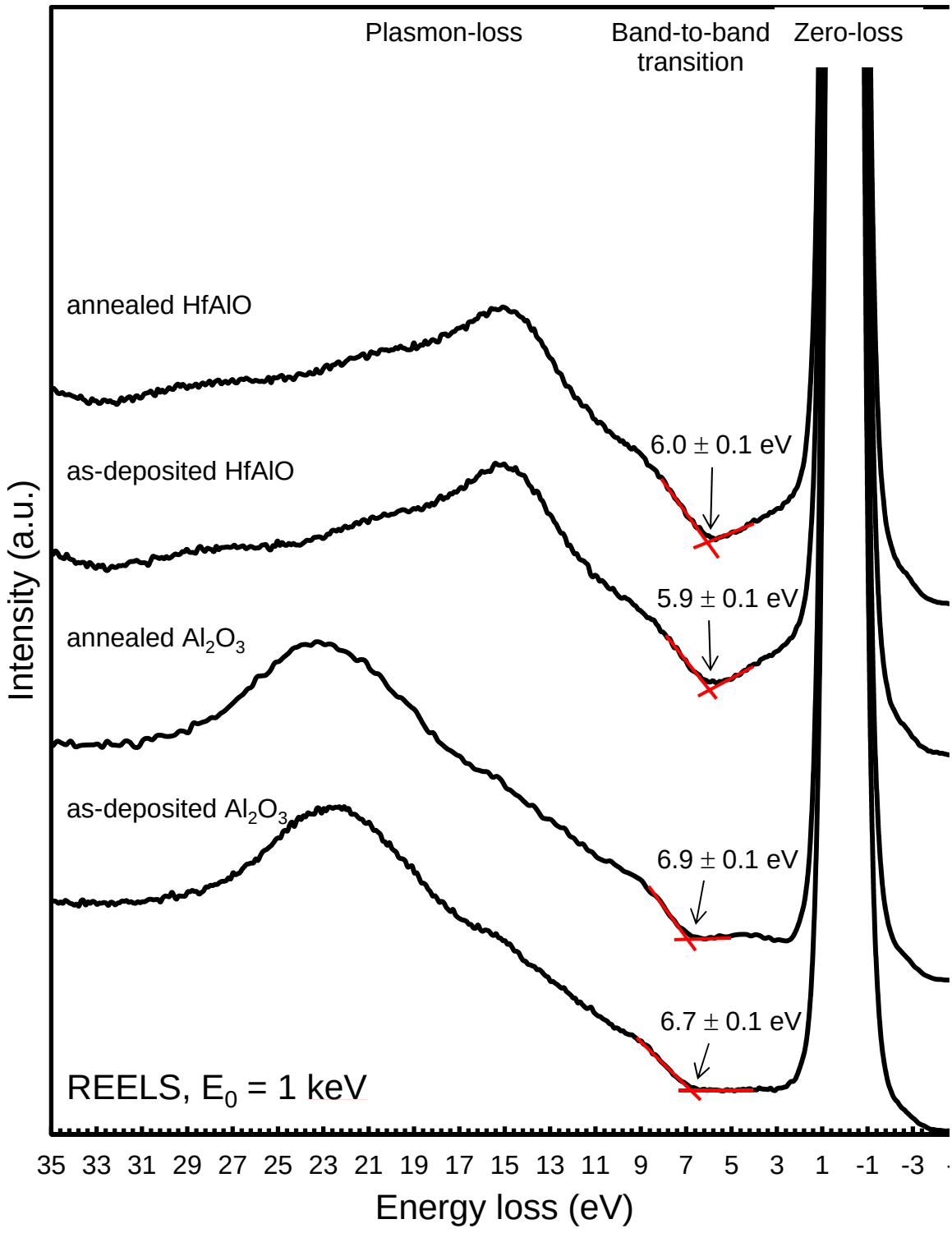


Figure R3.3 The low-loss region of REELS spectra of Al_2O_3 and HfAlO from as-deposited and annealed Al_2O_3/ HfAlO/SiO_2/p-type Si capacitor structure.

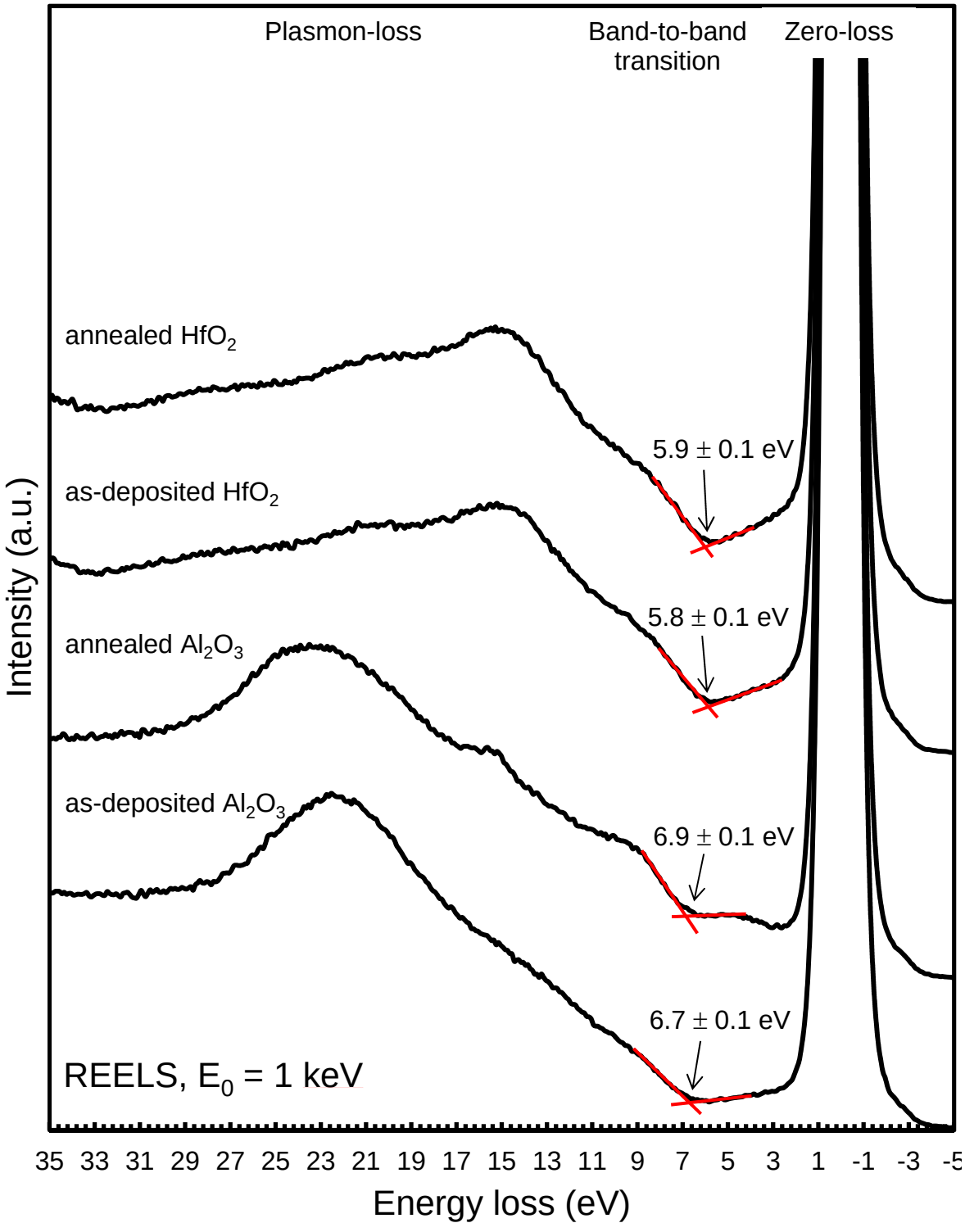


Figure R3.4 The low-loss region of REELS spectra of Al_2O_3 and HfO_2 from as-deposited $Al_2O_3/[HfO_2/Al_2O_3]_4/HfO_2/SiO_2$/p-type Si capacitor structure and Al_2O_3 and HfAlO from annealed $Al_2O_3/[HfO_2/Al_2O_3]_4/HfO_2/SiO_2$/p-type Si capacitor structure.

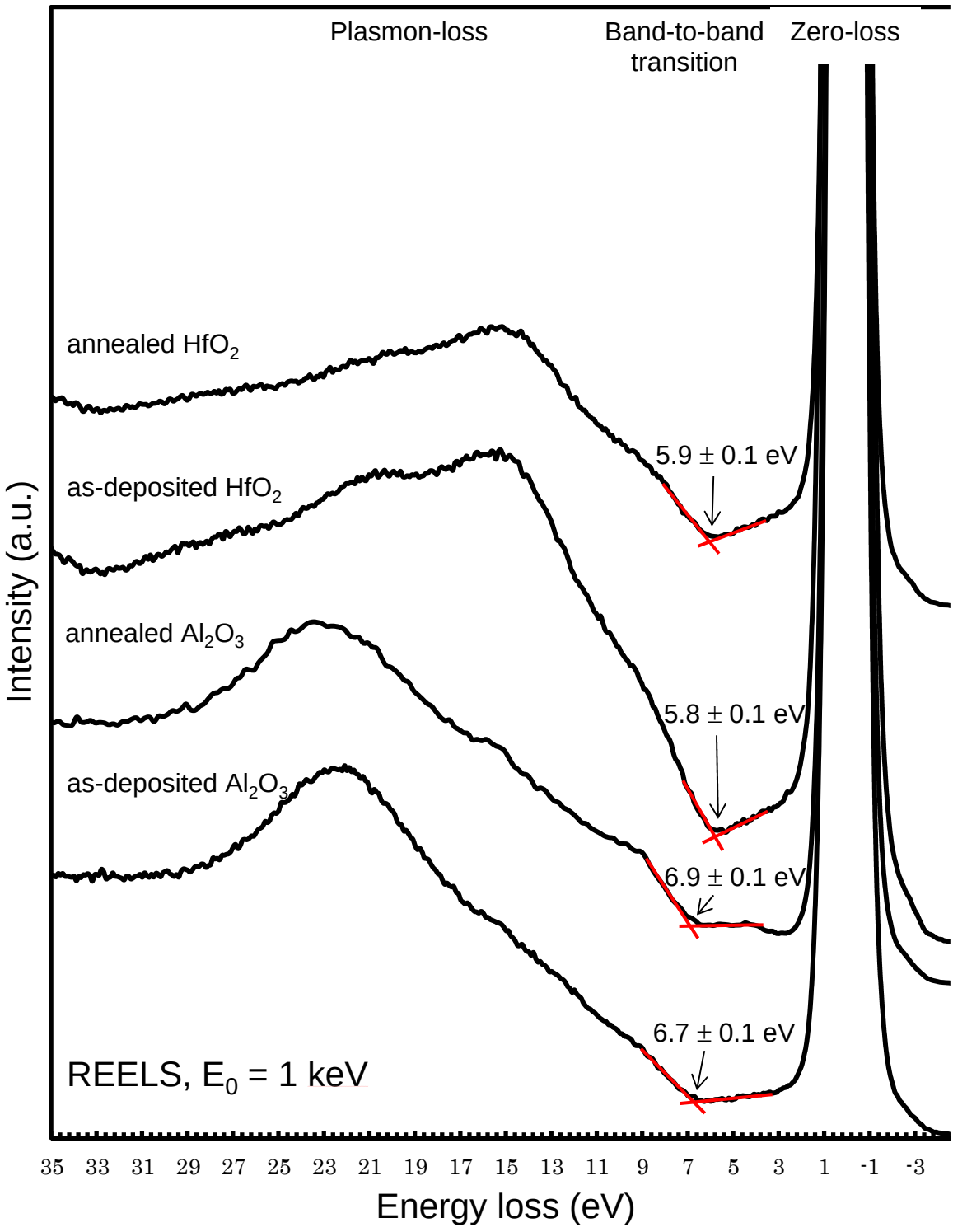


Figure R3.5 The low-loss region of REELS spectra of Al_2O_3 and HfO_2 from as-deposited $Al_2O_3/[HfO_2/Al_2O_3]_2/HfO_2/SiO_2$/p-type Si capacitor structure and Al_2O_3 and HfAlO from annealed $Al_2O_3/[HfO_2/Al_2O_3]_2/HfO_2/SiO_2$/p-type Si capacitor structure.

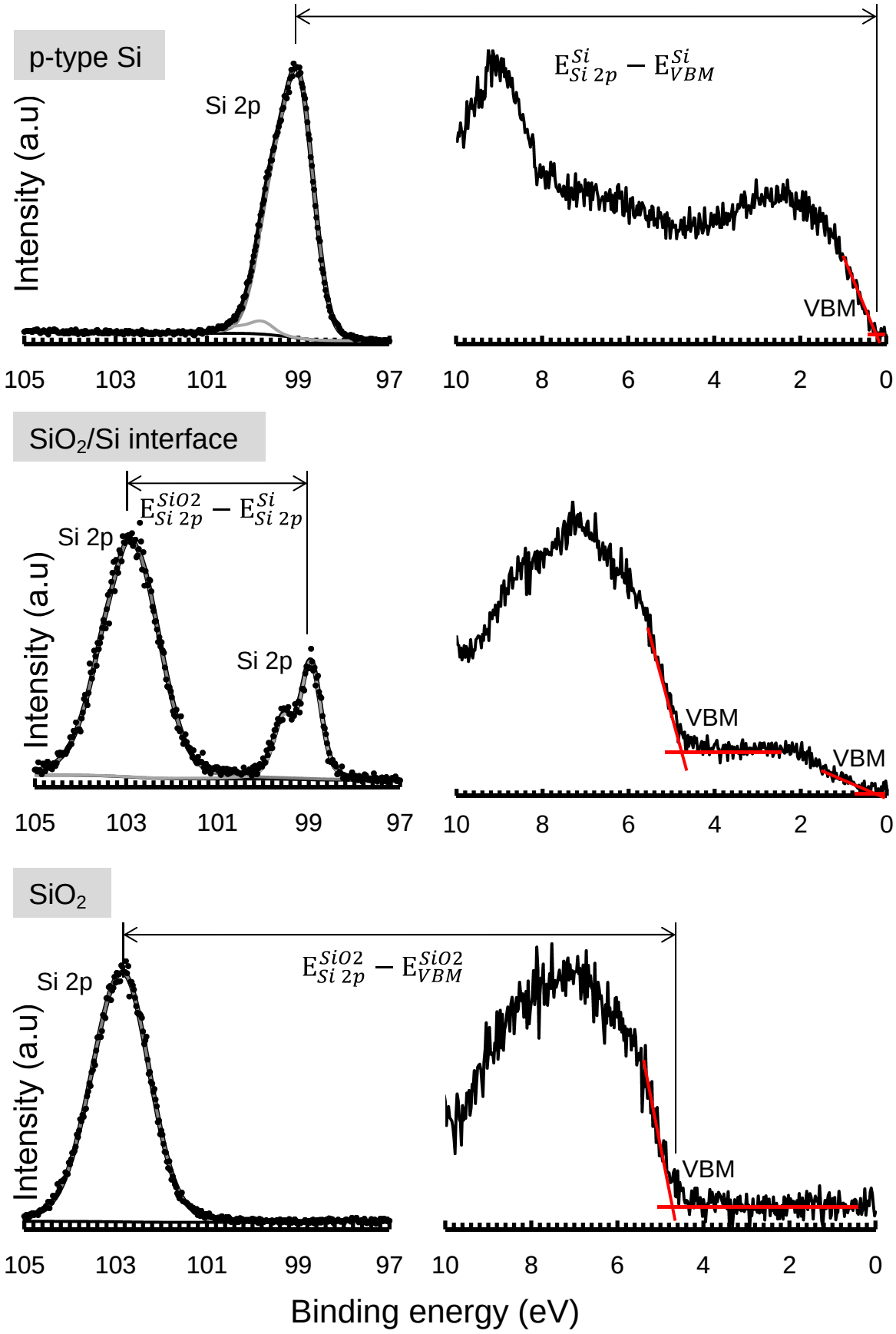


Figure R3.6 The energy distance between Si 2p CL and VBM of Si of Si substrate, Si 2p CL of SiO_2 and Si 2p CL of Si at SiO_2/Si interface, and Si 2p CL of VBM of Si O_2 of SiO_2 layer.

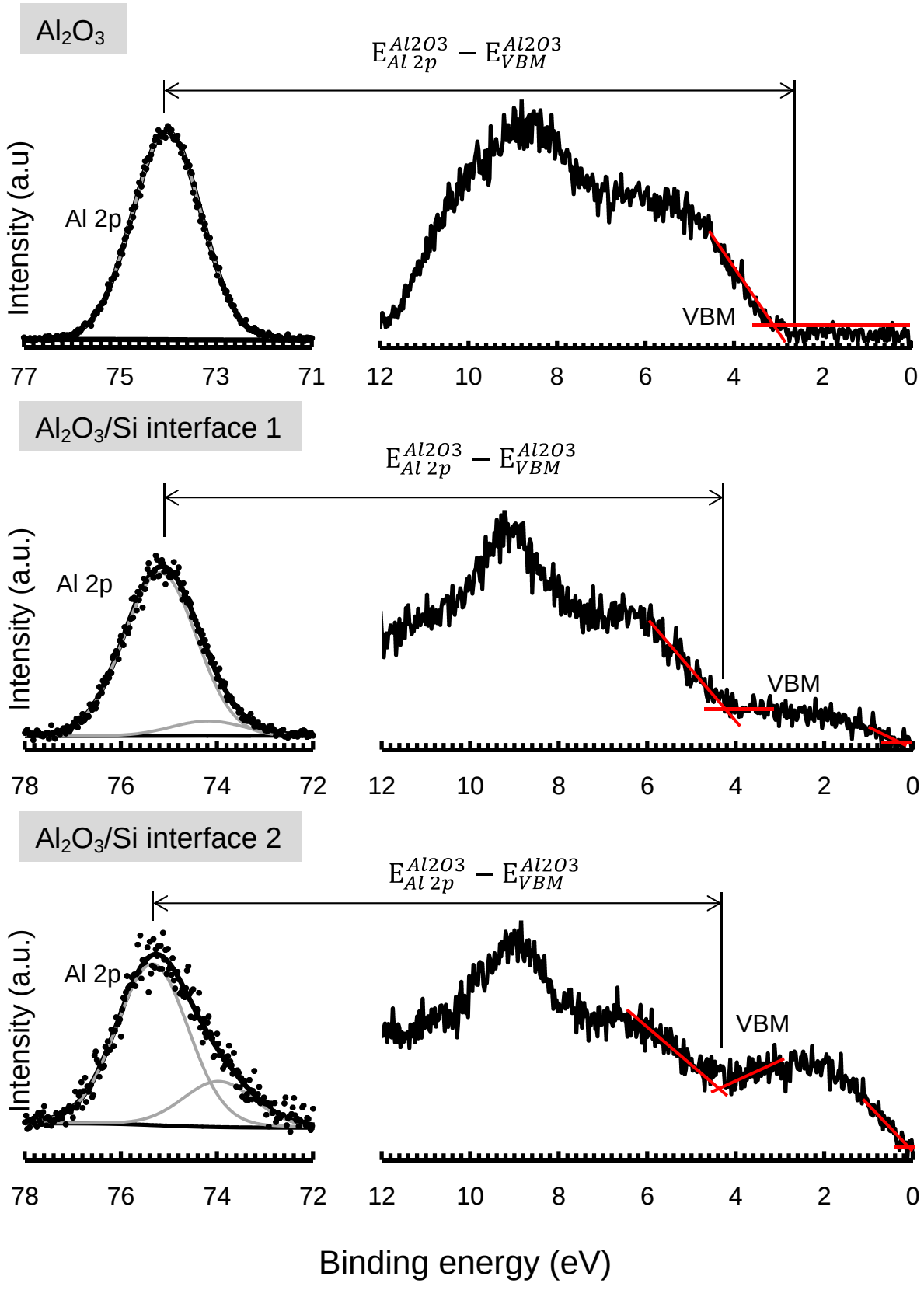


Figure R3.7 The energy distance between Al 2p CL and VBM of Al_2O_3 in Al_2O_3 blocking layer, at Al_2O_3/SiO_2 interface 1, and at Al_2O_3/SiO_2 interface 2 of sample A1.

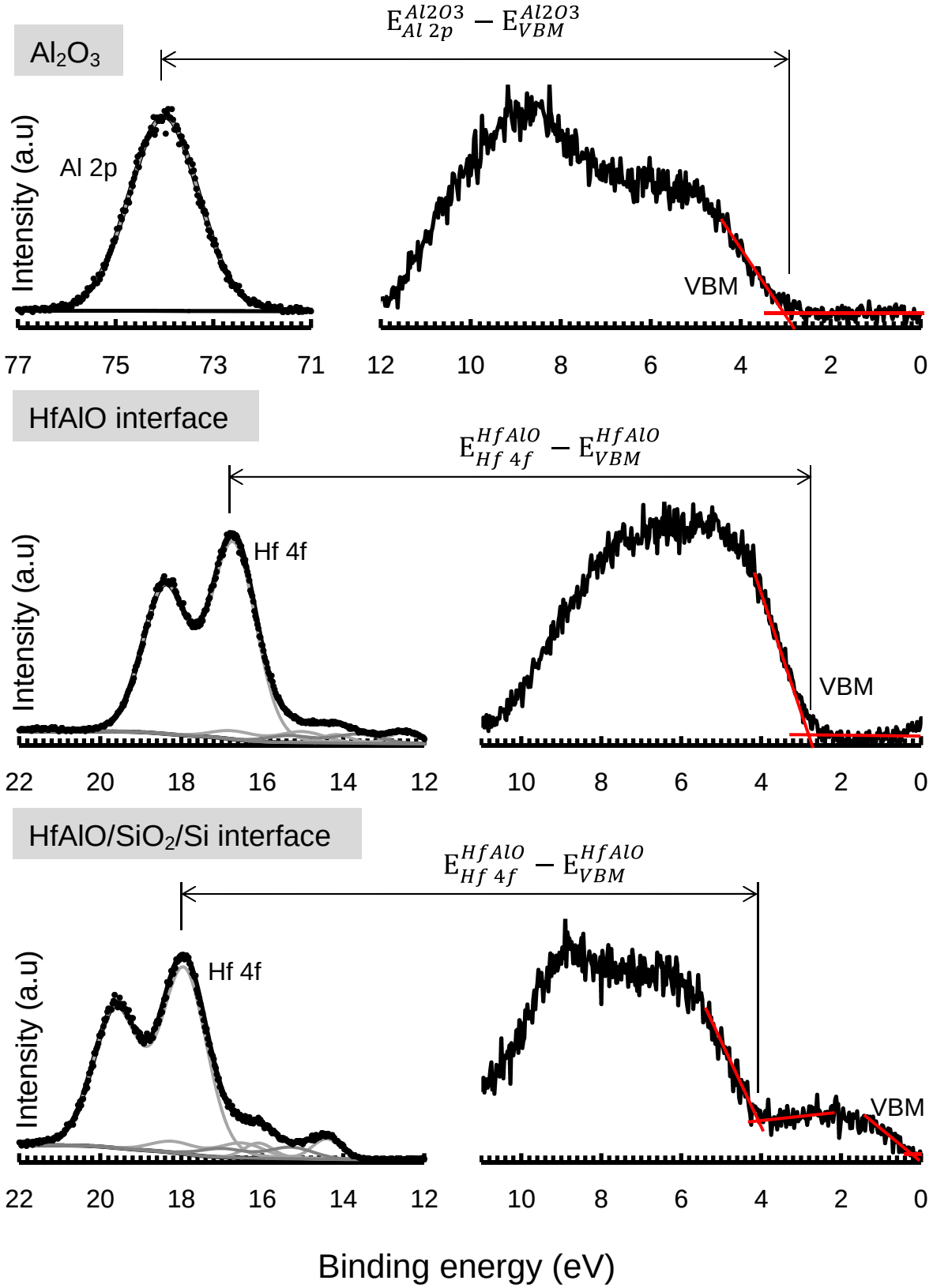


Figure R3.8 The energy distance between Al 2p CL and VBM of Al_2O_3 in Al_2O_3 blocking layer, Hf 4f CL and VBM of HfAlO at HfAlO layer, and Hf 4f CL and VBM of HfAlO at HfAlO/SiO_2/Si interface of sample HA1.

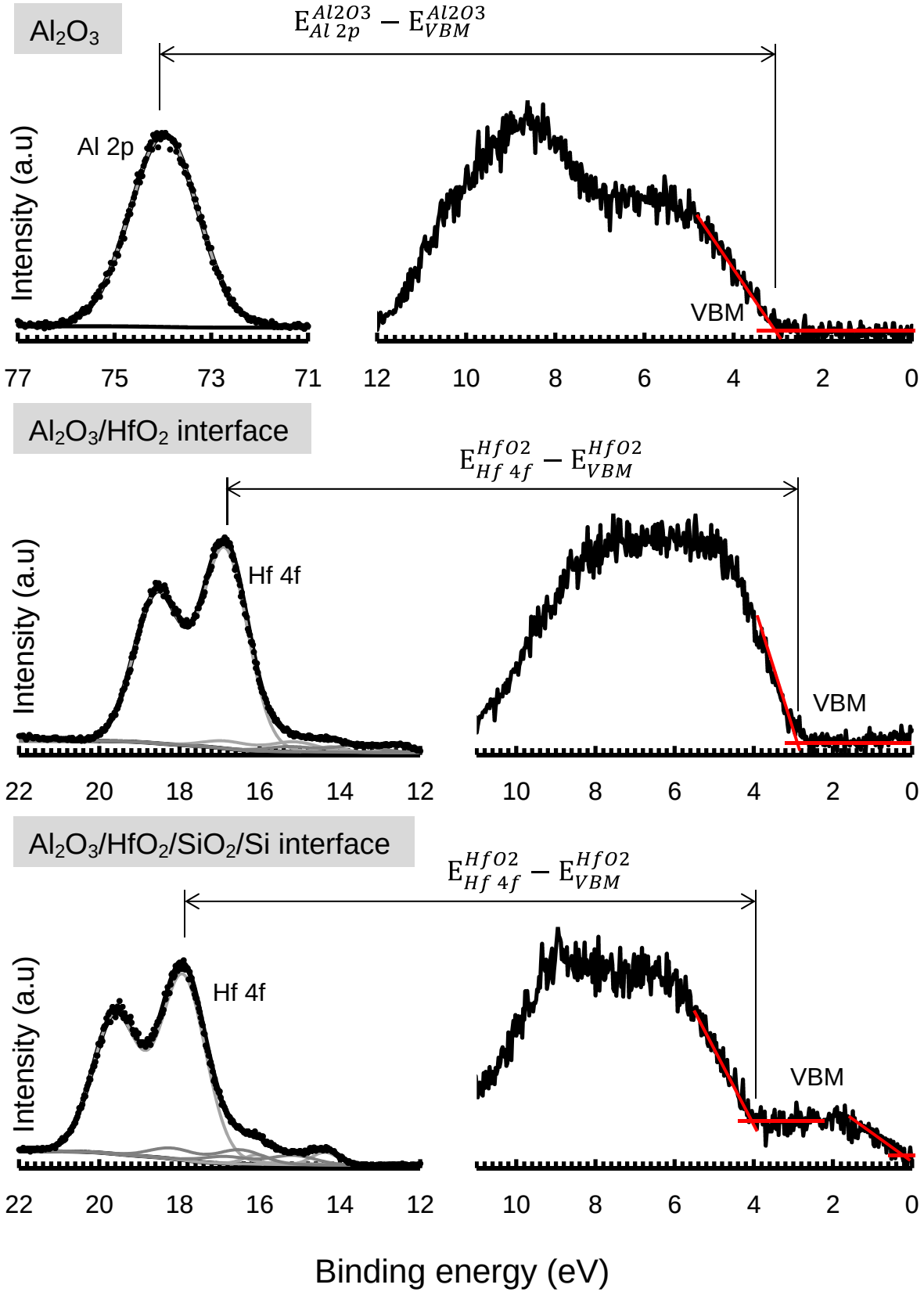
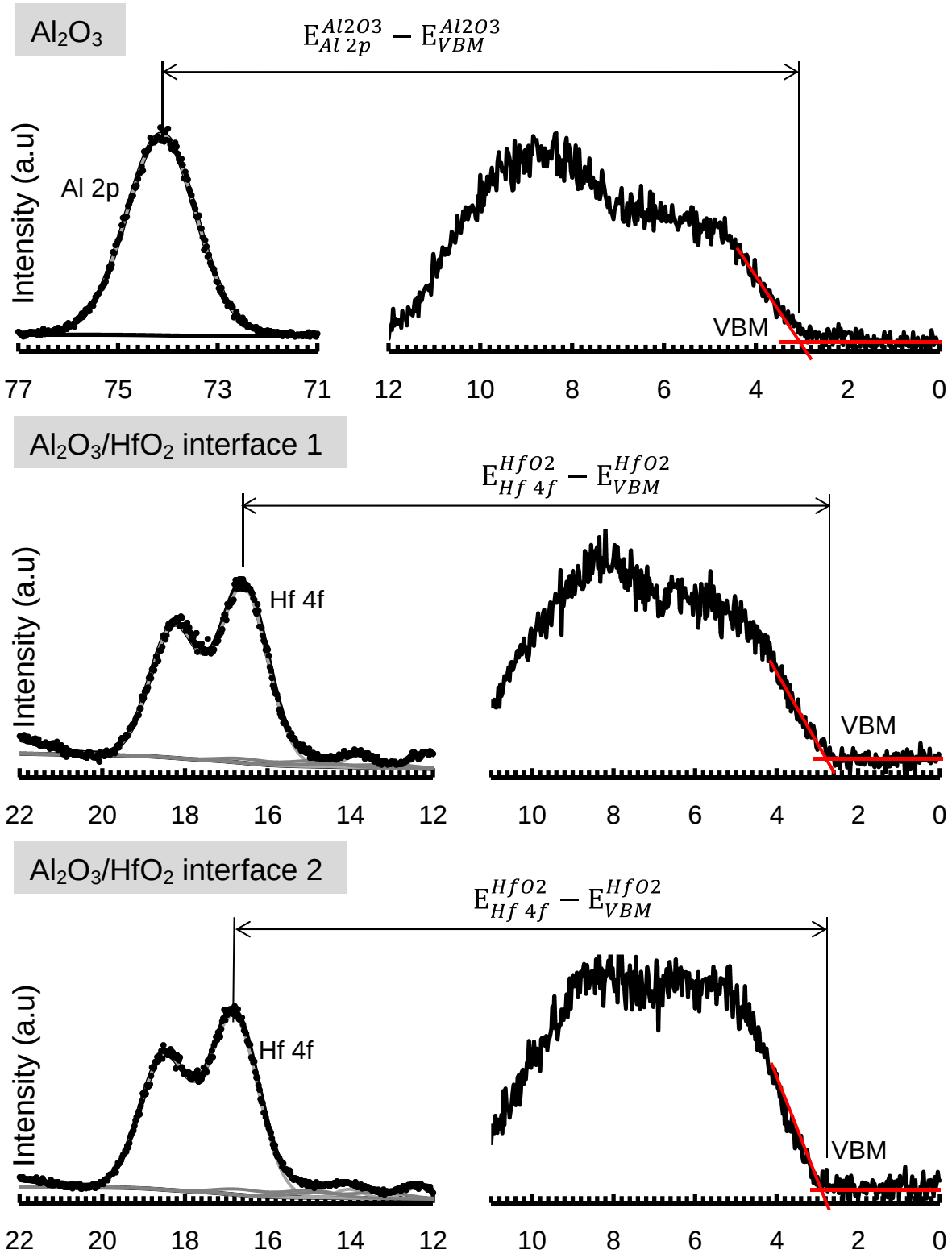


Figure R3.9 The energy distance between Al 2p CL and VBM of Al_2O_3 in Al_2O_3 blocking layer, Hf 4f CL and VBM of HfO_2 at Al_2O_3/HfO_2 interface, and Hf 4f CL and VBM of HfO_2 at $Al_2O_3/HfO_2/SiO_2/Si$ interface of sample NA1.


Al2O3
$E_{Al\ 2p}^{Al2O3} - E_{VBM}^{Al2O3}$
Intensity (a.u)
Al 2p
VBM
77
75
73
71
12
10
8
6
4
2
0
Al2O3/HfO2 interface 1
$E_{Hf\ 4f}^{HfO2} - E_{VBM}^{HfO2}$
Intensity (a.u)
Hf 4f
VBM
22
20
18
16
14
12
10
8
6
4
2
0
Al2O3/HfO2 interface 2
$E_{Hf\ 4f}^{HfO2} - E_{VBM}^{HfO2}$
Intensity (a.u)
Hf 4f
VBM
22
20
18
16
14
12
10
8
6
4
2
0

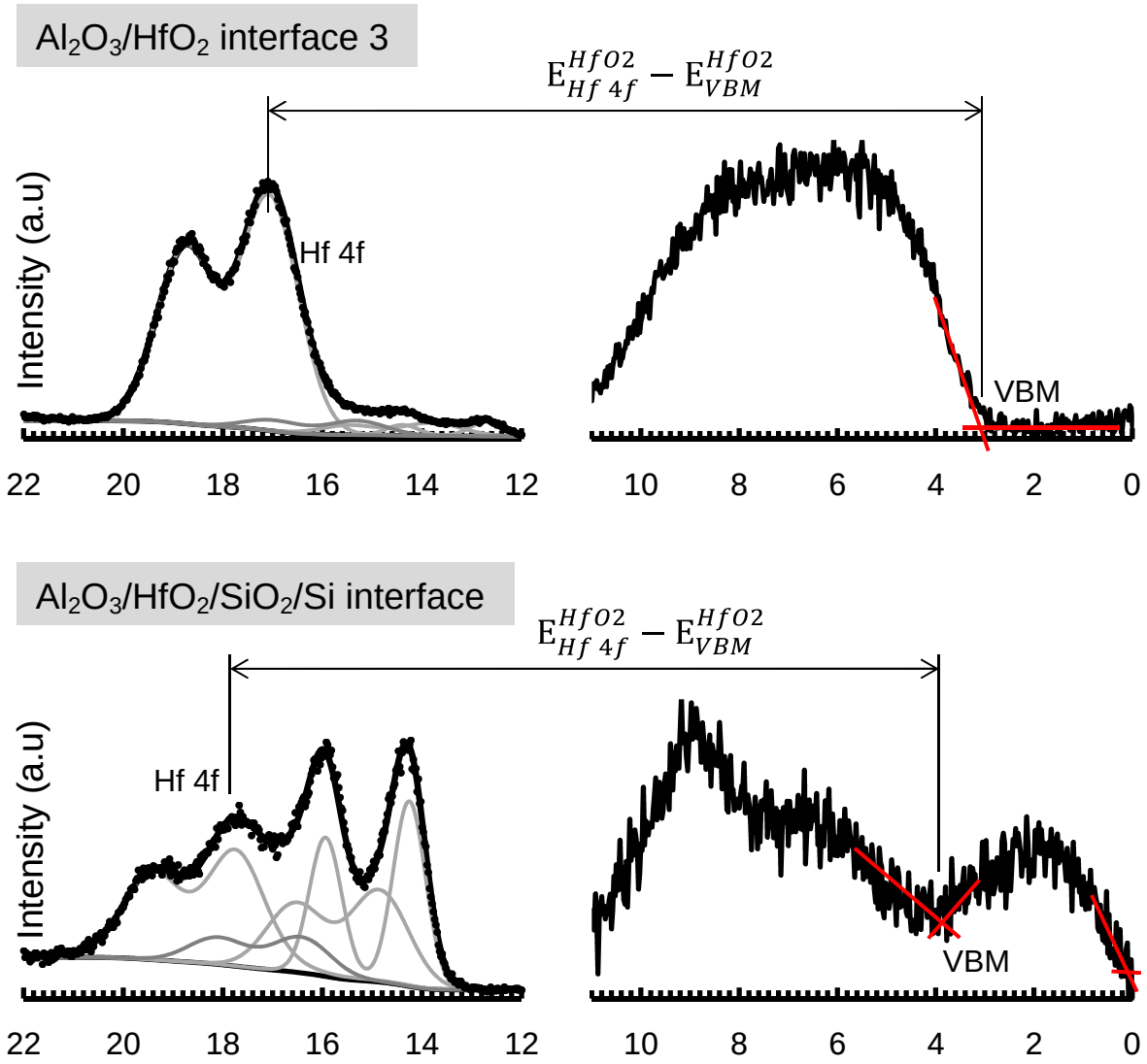


Figure R3.10 The energy distance between Al 2p CL and VBM of Al_2O_3 in Al_2O_3 blocking layer, Hf 4f CL and VBM of HfO_2 at Al_2O_3/ HfO_2 interface 1, Hf 4f CL and VBM of HfO_2 at Al_2O_3/ HfO_2 interface 2, Hf 4f CL and VBM of HfO_2 at Al_2O_3/ HfO_2 interface 3, and Hf 4f CL and VBM of HfO_2 at Al_2O_3/HfO_2/SiO_2/Si interface of sample NB1.

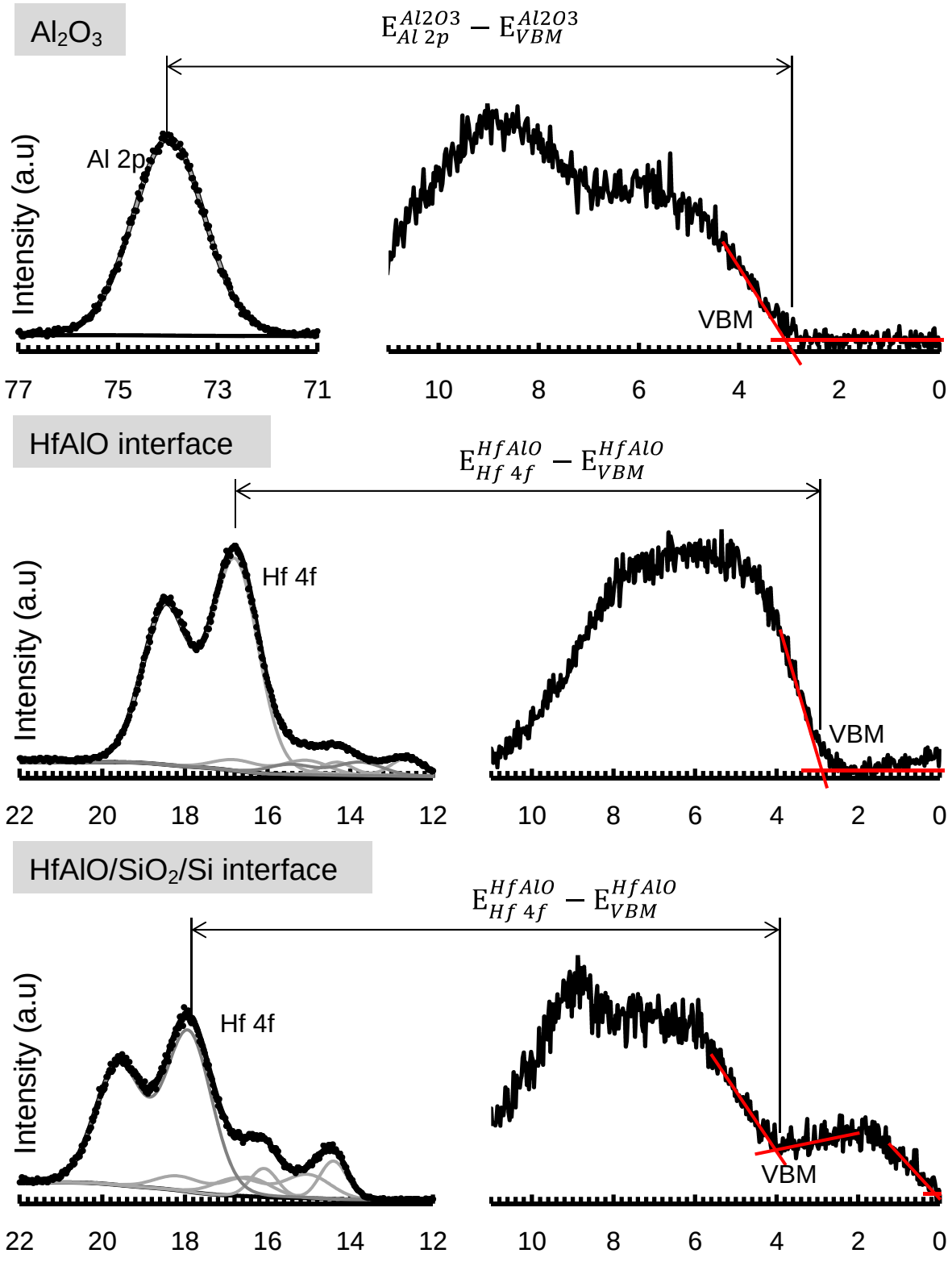
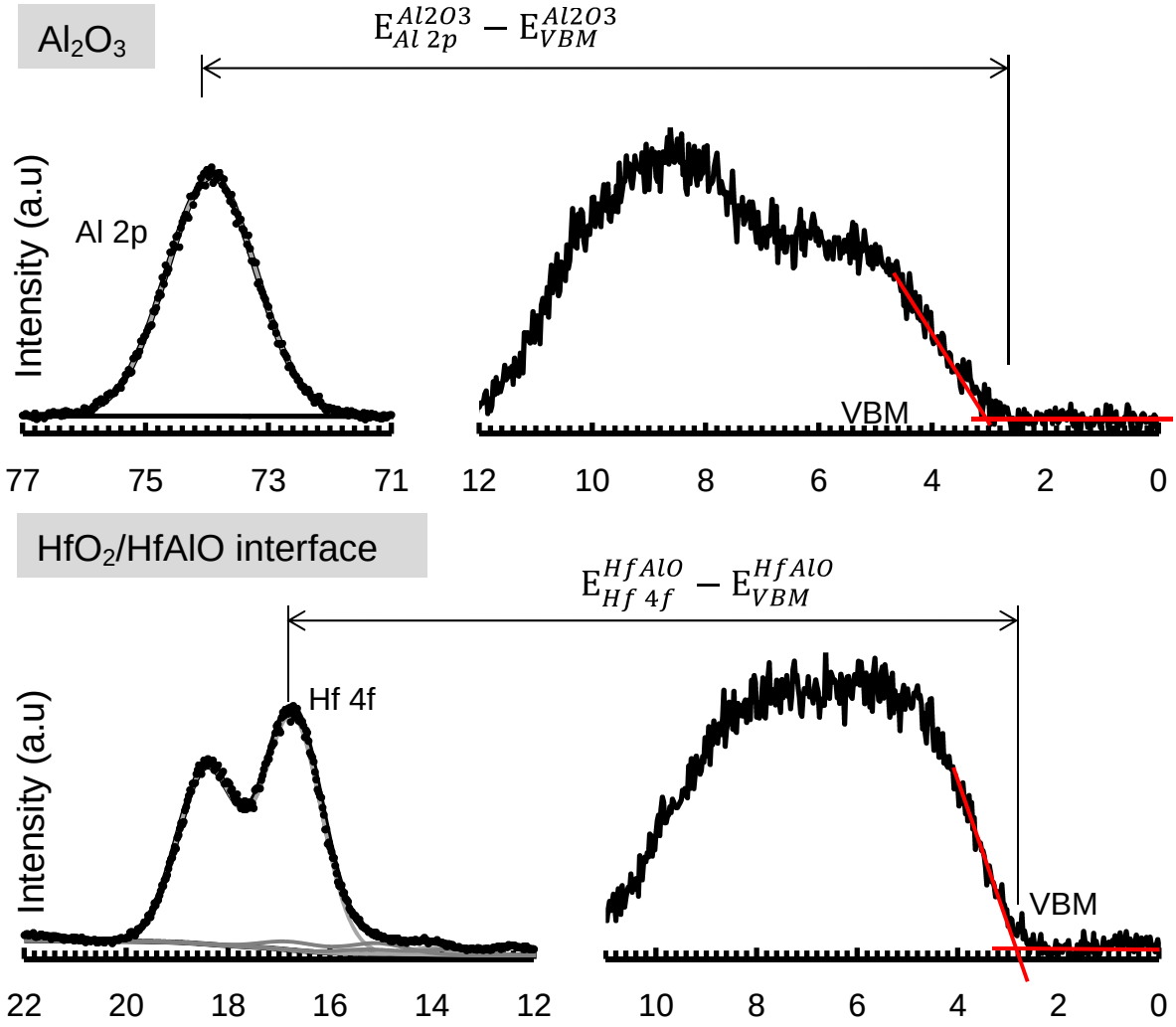


Figure R3.11 The energy distance between Al 2p CL and VBM of Al_2O_3 in Al_2O_3 blocking layer, Hf 4f CL and VBM of HfAlO at Al_2O_3/ HfAlO interface, and Hf 4f CL and VBM of HfAlO at Al_2O_3/ HfAlO/SiO_2/Si interface of sample HA2.


Al2O3
$E_{Al\ 2p}^{Al2O3} - E_{VBM}^{Al2O3}$
Intensity (a.u)
Al 2p
VBM
77
75
73
71
12
10
8
6
4
2
0
HfO2/HfAlO interface
$E_{Hf\ 4f}^{HfAlO} - E_{VBM}^{HfAlO}$
Hf 4f
Intensity (a.u)
VBM
22
20
18
16
14
12
10
8
6
4
2
0

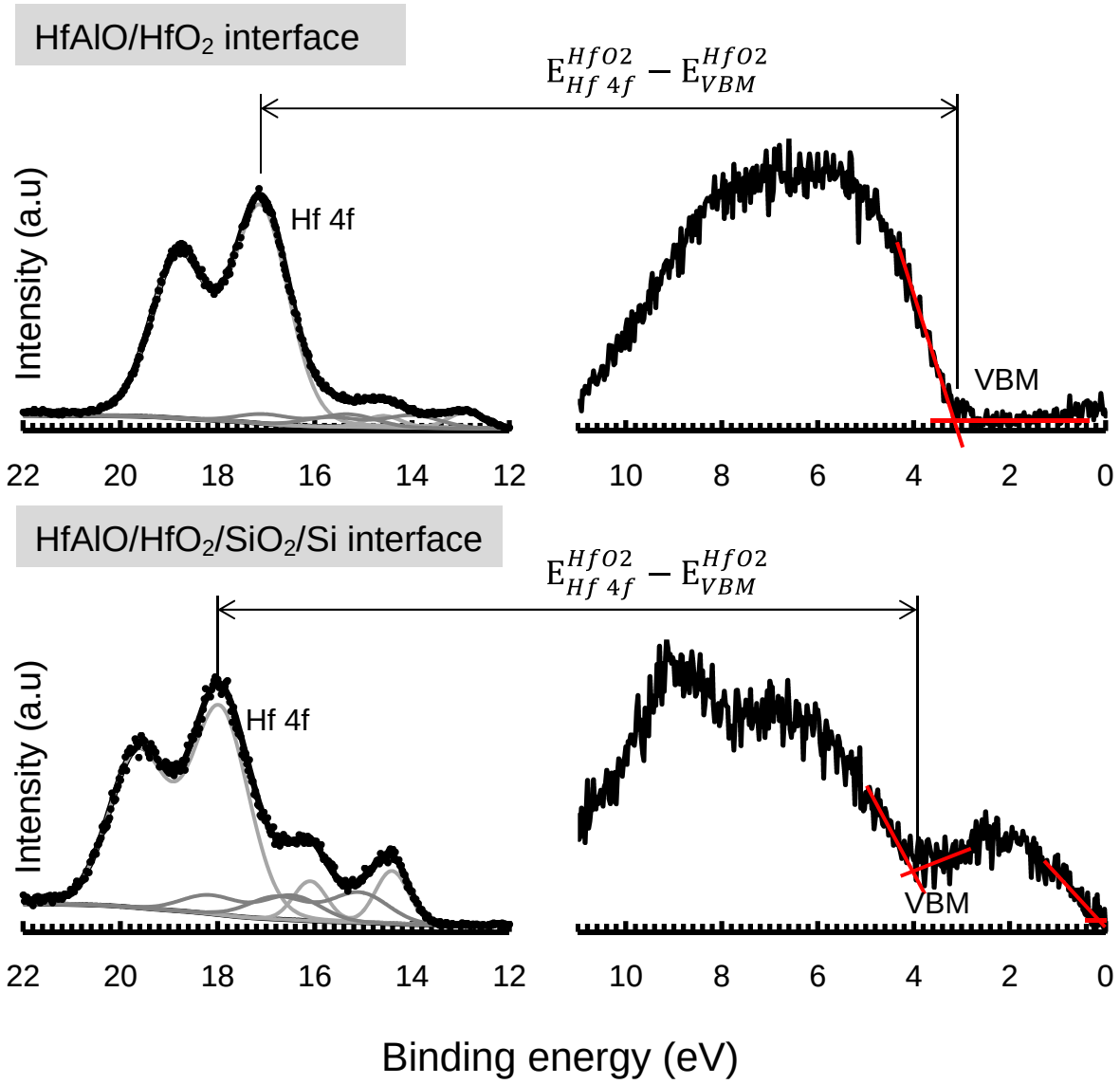
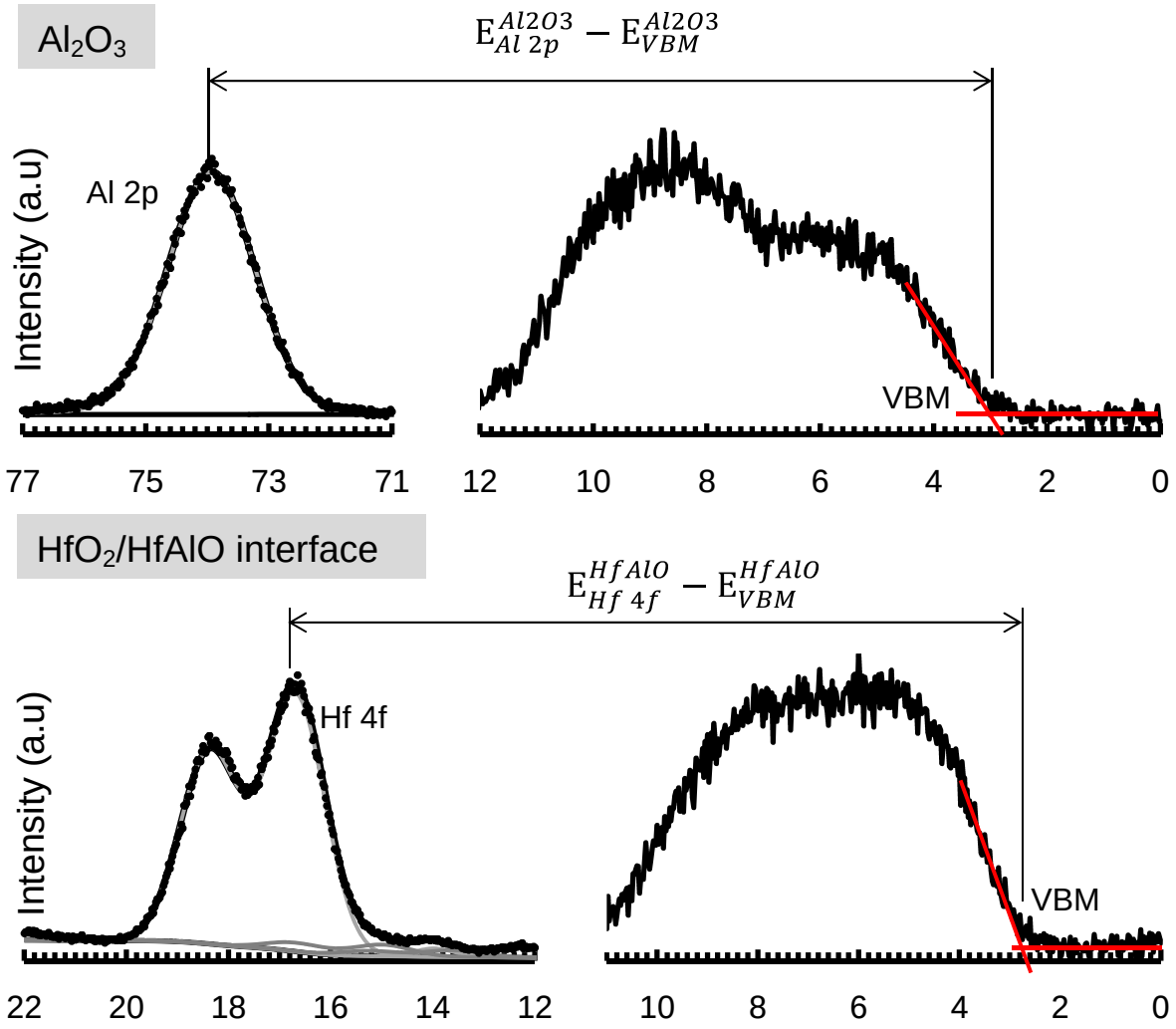


Figure R3.12 The energy distance between Al 2p CL and VBM of Al_2O_3 in Al_2O_3 blocking layer, Hf 4f CL and VBM of HfAlO at Al_2O_3/ HfAlO interface, Hf 4f CL and VBM of HfO_2 at Al_2O_3/HfO_2 interface, and Hf 4f CL and VBM of HfO_2 at Al_2O_3/HfO_2/SiO_2/Si interface of sample NA2.


Al2O3
$E_{Al\ 2p}^{Al2O3} - E_{VBM}^{Al2O3}$
Intensity (a.u)
Al 2p
VBM
77
75
73
71
12
10
8
6
4
2
0
HfO2/HfAlO interface
$E_{Hf\ 4f}^{HfAlO} - E_{VBM}^{HfAlO}$
Intensity (a.u)
Hf 4f
VBM
22
20
18
16
14
12
10
8
6
4
2
0

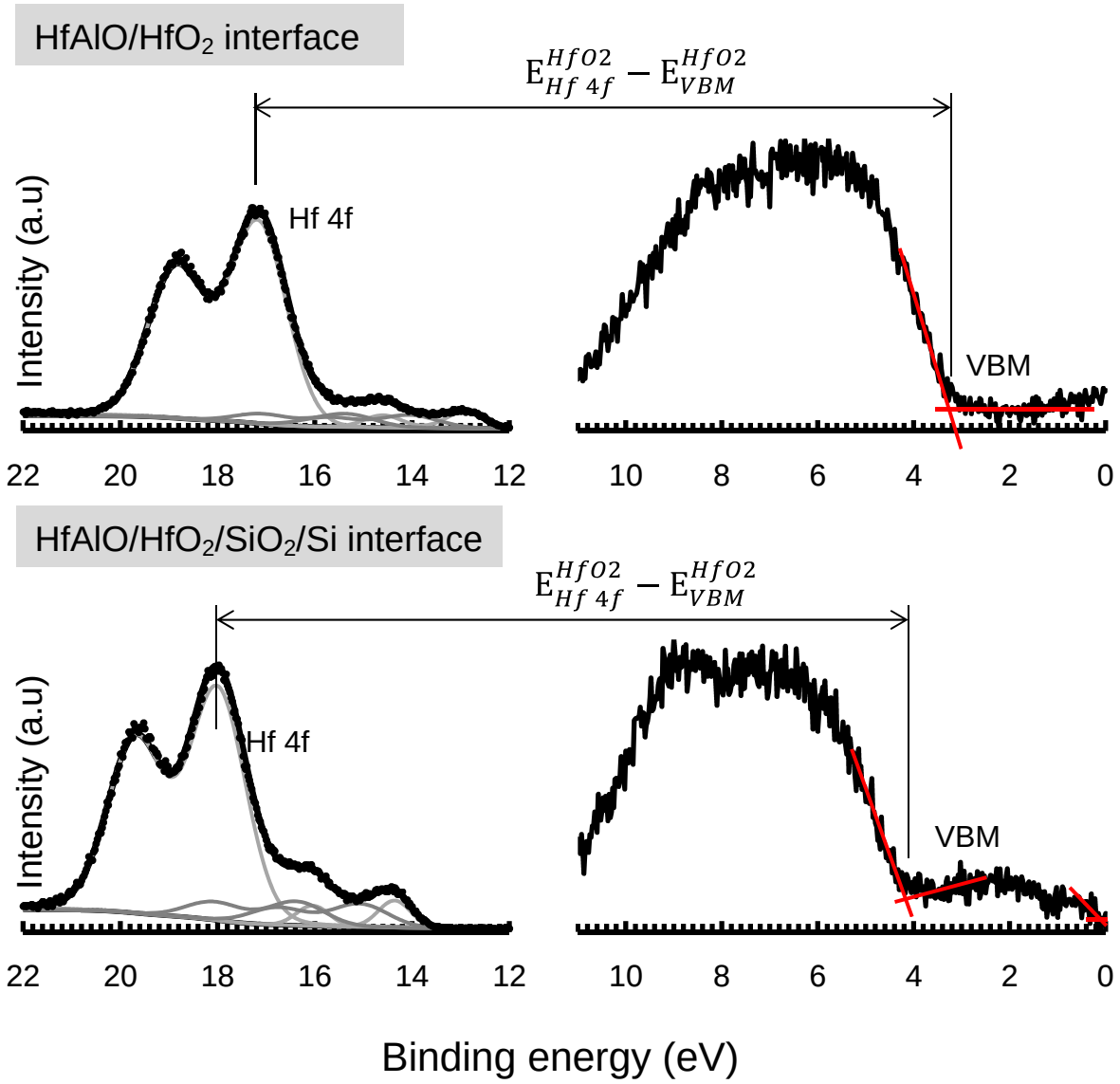


Figure R3.13 The energy distance between Al 2p CL and VBM of Al_2O_3 in Al_2O_3 blocking layer, Hf 4f CL and VBM of HfAlO at Al_2O_3/ HfAlO interface, Hf 4f CL and VBM of HfO_2 at Al_2O_3/HfO_2 interface, and Hf 4f CL and VBM of HfO_2 at Al_2O_3/HfO_2/SiO_2/Si interface of sample NB2.

Chapter 4

Charge Trapping in Capacitor Structures with as-deposited High-κ Dielectric Materials as Charge Trapping Layers

In chapter 4, the charge trapping characteristics in as-deposited MAHOS capacitor structures with heterostructure of Al_2O_3/HfO_2 nanolaminates as charge trapping layers (CTL) are observed by inductance – capacitance – resistance (LCR) meter and semiconductor analyzer system. The mechanism of charge trapping is explained by considering the energy band structures of MAHOS capacitors. Before discussing the charge trapping characteristics, the properties of Boron-doped p-type Silicon are evaluated, including the dopant concentration, electron concentration, and Fermi level with respect to the intrinsic Fermi level. The neutral flatband voltage of samples is determined by applying the calculation C_{FB} method. The neutral flatband voltage shift which is influenced by the dipole formation in high-κ/SiO_2 interface is also discussed.

4.1 Introduction

4.1.1 Background on Using Al_2O_3/HfO_2 Nanolaminates as Charge Trapping Layer

As stated in chapter 1, one of the main purposes of this research work is to investigate the charge trapping characteristics of the MAHOS structures, which consist of metal gate electrode – Al_2O_3 – high-κ dielectric – SiO_2 – p-type Si substrate, with Al_2O_3/HfO_2 nanolaminates as CTL. Their charge trapping characteristics are compared with the MAHOS structures with Al_2O_3 and the mixture of Al_2O_3 and HfO_2 as charge trapping layers. By using Al_2O_3/HfO_2 nanolaminates as charge trapping layer, heterojunction formed between two dissimilar semiconductors is created to get unique properties provided by the difference in energy gap. HfO_2 has deep trap level and has smaller conduction and valence band offset

with respect to Si substrate, so the charges can be trapped with lower programming voltage and faster erase speed can be achieved.[1-3] However, HfO_2 shows poor retention characteristics with very large charge loss.[4] Al_2O_3 is used to modulate charge trapping distribution. Since it has wider bandgap and band offset with respect to Si than those of HfO_2, it is hoped that the retention properties can be improved.[1]

From the results, it is observed whether the structure with Al_2O_3/HfO_2 nanolaminates as CTL can fulfil the requirements of the next generation of non-volatile memory devices, which are low programming voltage, low leakage current, and good retention characteristics for over 10 years. The charge trapping characteristics in the MAHOS structures is evaluated by carrying out high frequency (1 MHz) C – V measurement. Their leakage current density is observed by analyzing the current density when stress voltage is applied on the capacitor structure.

4.1.2 Charge Injection Mechanism by Fowler – Nordheim Tunneling

In the framework of quantum mechanics, the solutions of the Schrodinger equation represent a particle. The continuous nonzero nature of these solutions, even in classically forbidden regions of negative energy, implies an ability to penetrate these forbidden regions and a probability of tunneling from one classically allowed region to another[5]. The concept of tunneling through a potential barrier applies well to MOS structures with thin oxide. Figure 4.1 shows the energy-band diagram of a MOS structure with negative bias applied to the metal electrode with respect to the p-doped silicon substrate. The probability of electron tunneling depends on either the distribution of occupied states in the injecting material or the shape, height, and width of the barrier. Using a free-electron gas model for the metal and the Wentzel–Kramers–Brillouin (WKB) approximation for the tunneling probability, one obtains the following expression for current density [6]:

$$J = \frac{q^3 F^2}{16\pi^2 h^2 \Phi_B} \exp\left[-4(2m_{ox}^*)^{\frac{1}{2}}\Phi_B^{\frac{3}{2}}/3hqF\right] \quad (4.1)$$

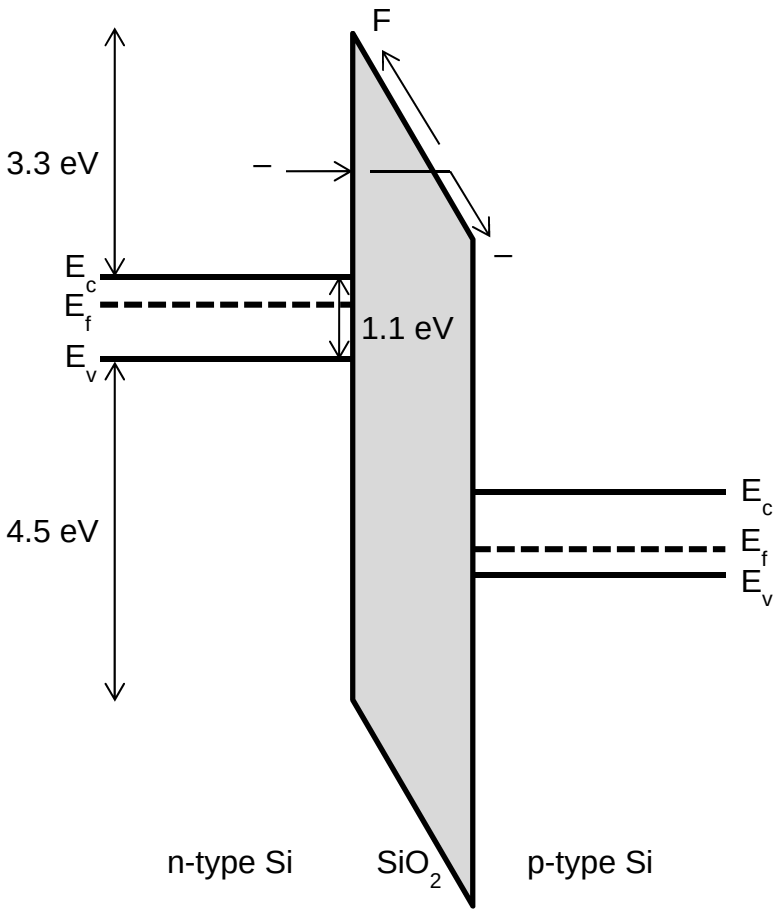


Figure 4.1 Fowler – Nordheim tunneling through a potential barrier in a MOS structure.

where Φ_B is the barrier height, m_{ox}^* is the effective mass of the electron in the forbidden gap of the dielectric, h is the Planck's constant, q is the electronic charge, and F is the electric field through the oxide.

The F-N mechanism is widely used in NVM, particularly in EEPROM. With a relatively thick oxide (20 – 30 nm) one must apply a high voltage (20 – 30 V) to have an appreciable tunnel current. With thin oxides, the same current can be obtained by applying a much lower voltage. An optimum thickgness is chosen in present devices, which use the tunneling phenomenon to tradeoff between performance constraints (programming speed, power consumption, etc.) and reliability concerns. There are three main reasons for this choice:

a. Tunneling is a pure electrical mechanism.

b. The involved current level is quite low and thus allows the internal generation of supply voltages needed for all operations.

c. It allows one to obtain the time to program (<1 ms) 12 orders of magnitude shorter than retention time (>10 *y*), which is a fundamental request for all NVM technologies.

The exponential dependence of tunnel current on the oxide-electric field causes some critical problems of process control because very small variation of oxide thickness among the cells in a memory array produces a great difference in programming or erasing currents. Bad quality oxides are rich of interface and bulk traps, and trap-assisted tunneling is made possible since the equivalent barrier height seen by electrons is reduced and tunneling requires a much lower oxide field than 10 MV/cm. The oxide defects must be avoided to control program/erase characteristics and to have good reliability. Frequent program and erase operations induce an increase of trapped charge in the oxide. This affects the barrier height, which is lower in the case of positive and higher in the case of negative trapping, respectively, thus increasing or decreasing the tunnel currents.

The classic theory is based on the assumption that electrons, as well as holes, at the semiconductor surface can be treated as a three-dimensional gas of free particles with a Boltzmann distribution of energy. But when the silicon surface is inverted or accumulated (which are the usual conditions during tunnel injection in MOS devices), these particles are confined into a narrow potential well, so the quantum-mechanics laws require their motion perpendicular to the interface to be quantized. Thus, the correct treatment is a two-dimensional quantum-mechanical gas. Briefly, the results of this treatment are as follows.[7]

a. The barrier height is voltage dependent and is lower than the classical one.

b. The oxide field is lower than the classical one due to a much greater voltage drop in the

silicon substrate.

It is possible to rewrite (1) in the simplest form

$$J = A.F^2 \exp[-B/F] \quad (4.2)$$

and to use A and B as functions of the electric field, which include quantum effects. This approach is quite satisfactory in a lot of cases but leads to different values of and depending on the injecting electrode and on device polarization.

4.2 Measurement Methods

4.2.1 High Frequency (1 MHz) Capacitance – Voltage (C – V) Characteristics Measurement

The high frequency (1 MHz) capacitance – voltage (C – V) characteristics were measured by LCR meter Agilent 4284 A. The small-signal, high frequency capacitance of the specimen is measured as a function of a ramped voltage applied between the metal gate and the silicon substrate. The surface carrier concentration, flatband capacitance, and flatband voltage are calculated from the capacitance and voltage data.

Charge trapping characteristics is measured based on the flatband voltage shift which is the difference between the flatband voltage after applying sweeping gate voltage and neutral flatband voltage. Since electron trapping is expected in charge-trap memory, the C – V measurement is carried out by applying the sweeping gate voltage from inversion to accumulation in order to trap electrons for programming purpose, then applying the sweeping gate voltage from accumulation to inversion in order to remove the electrons from charge trapping layer for erasing purpose. To observe the electron trapping in charge trapping layer as a function of gate voltage, the sweeping gate voltage from inversion or positive voltage, with the voltage of 2 V – 15 V, to accumulation or negative voltage with the voltage of -2 V is applied. Then, the sweeping gate voltage from accumulation or negative voltage, with the

voltage of -2 V – -15 V, to inversion or positive voltage with the voltage of 3 V is applied. The flatband voltage shifts are determined and are plotted as a function of the gate voltage.

4.2.2 Leakage Current Density Measurement

Current-voltage (I-V) measurements can indicate the conduction mechanism. A sweep voltage with a fixed voltage step of 0.1 V and a step delay time is applied to the device under investigation. Leakage current density as a function of stress voltage is measured by HP4156C semiconductor analyzer system. For one sample, the leakage current density is measured under positive sweep voltage from 0 – 35 V on several devices. The leakage current density is also measured under negative sweep voltage from 0 – -35 V.

4.3 Determination of Dopant Concentration, Electron Concentration, and Fermi Level of p-type Silicon Substrate

4.3.1 Dopant Concentration

The substrate dopant concentration (N_D) can be obtained from the measurement of differential capacitance as a function of gate bias. The dopant profile from a capacitance measurement can only be obtained when the profile is closely related to the free carrier charge concentration flowing in response to the ac gate voltage. Dopant concentration cannot be obtained accurately in either accumulation or inversion. However, it can be obtained accurately in depletion, where the free carrier concentration depends strongly on dopant impurity concentration.

The ionized dopant concentration is obtained from the slope of a ($1/C^2$) versus V_G curve, where C is the capacitance measured in depletion at gate bias V_G. An expression for the ionized dopant impurity concentration at the depletion layer edge is derived by assuming that the interface traps have a negligible influence.[8]

The doping concentration is calculated as follows,

$$N_D = \frac{2}{q\varepsilon_s A^2\left(\frac{\Delta 1/C^2}{\Delta V_G}\right)} \quad (4.3)$$

where N_D is substrate dopant concentration, q is electron charge (1.60219×10^{-19} C), A is gate area (cm^2), ε_s is permittivity of the substrate material (F/cm), V_G is gate voltage (V), and C is measured capacitance (F).

The substrate dopant concentration (N_D) is related to the reciprocal of the slope of the $1/C^2$ vs. V_G curve. A positive slope will give a negative N_D for acceptors, whereas a negative slope gives a positive N_D for donors.

Figure 4.2 shows the C – V characteristics of as-deposited $Al/Al_2O_3/HfAlO/SiO_2$/ p-type Si structure under the sweep voltage from 2 V to -2 V. From this measurement, the $1/C^2$ as a function of V_G is obtained and the slope $\left(\frac{\Delta 1/C^2}{\Delta V_G}\right)$ is observed to be 0.159512 $pF^{-2}.V^{-1}$, as shown in Figure 4.3. By using equation (4.3), the dopant concentration is calculated to be 7.6672×10^{14} cm^{-3}. By using the Standard Practice for Conversion Between Resistivity and Dopant Density for Boron-Doped[9], it is found that the Si-substrate with the

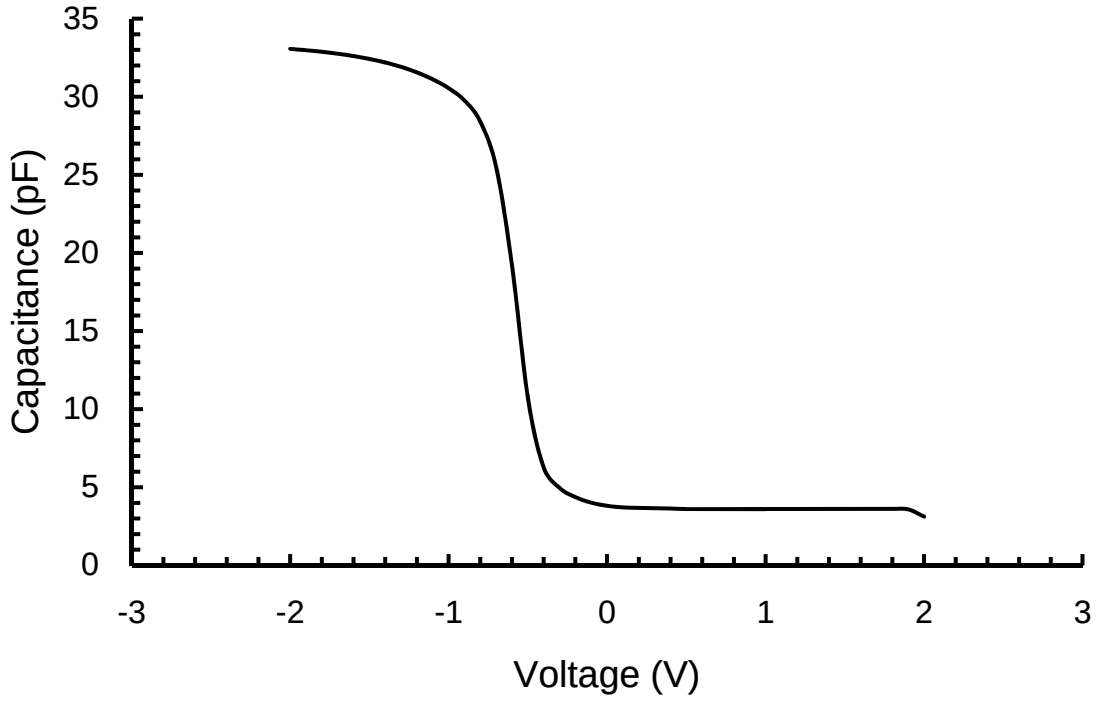


Figure 4.2. Measured C – V characteristics for as-deposited $Al/Al_2O_3/HfAlO/SiO_2$/p-type Si structure.

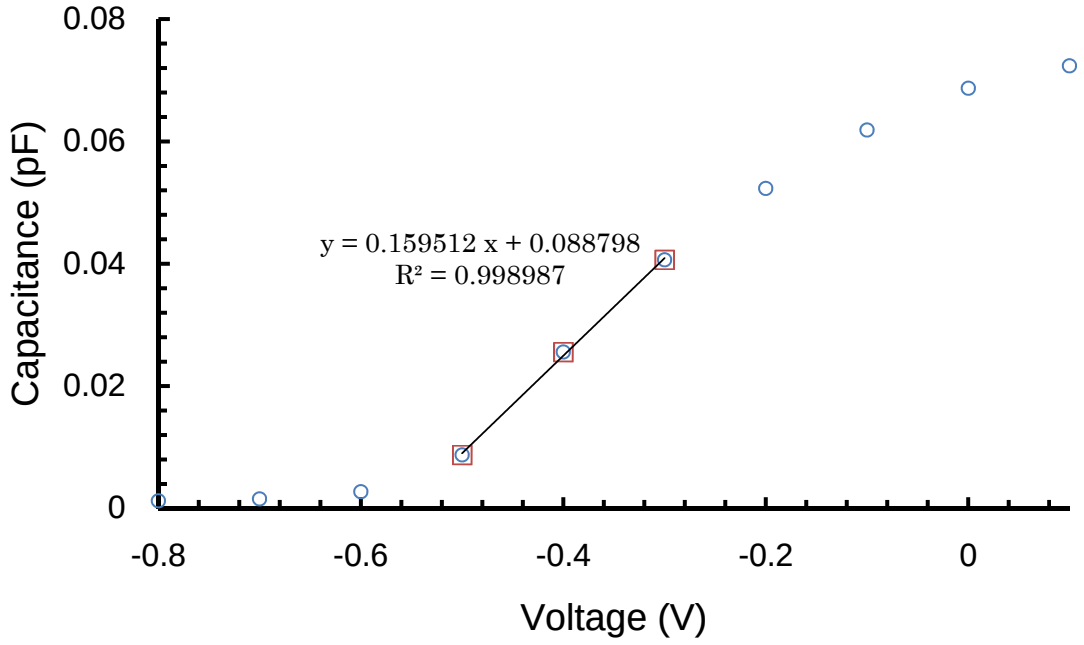


Figure 4.3. Linear parts of measured $1/C^2(V_G)$ characteristics for as-deposited $Al/Al_2O_3/HfAlO/SiO_2$/p-type Si structure.

dopant concentration of 7.6672×10^{14} cm^{-3} has the resistivity of 17.7 Ω.cm. The dopant concentration calculation is also done on $Al/Al_2O_3/HfAlO/SiO_2$/ p-type Si and $Al/Al_2O_3/[Al_2O_3/HfO_2]_4/HfO_2/SiO_2$/ p-type Si structures. The dopant concentrations and resistivities are shown in Table 4.1. These results are valid because the Si subtrate that we use is Boron-doped p-type Si substrate with the resistivity between 15 – 25 Ω.cm.

Table 4.1 The dopant concentrations and resistivities measured on several devices

Sample	$\frac{\Delta 1/C^2}{\Delta V_G}$ ($pF^{-2}.V^{-1}$)	N_D (cm^{-3})	R (Ω.cm)
A1	0.158153	7.733051×10^{14}	17.2
A1	0.15788	7.746472×10^{14}	17.2
HA1	0.15951	7.667167×10^{14}	17.2
HA1	0.16831	7.266471×10^{14}	18.1
NA1	0.15497	7.891985×10^{14}	16.8
NA1	0.165263	7.400357×10^{14}	17.9

4.3.2 Carrier Concentrations and the Fermi Level at Equilibrium

The Si substrate is doped with Boron which is an acceptor or a p-type material. Therefore the equilibrium hole concentration (p_0) equals the dopant concentration (N_D) which is 7.64×10^{14} cm^{-3}. To find the equilibrium electron concentration, the Law of Mass Action can be used, which is

$$n_0 = \frac{n_i^2}{p_0} \tag{4.4}$$

It is known that the Silicon intrinsic carrier concentration (n_i) is 1.08×10^{10} cm^{-3}.[10, 11] It is found that the electron concentration is 1.5267×10^5 cm^{-3}. To find the Fermi level with respect to the intrinsic Fermi level, the expression that links the hole concentration to the intrinsic Fermi level (E_i) and the intrinsic carrier concentration (n_i).

$$p_0 = n_i exp\left(\frac{E_i - E_F}{kT}\right) \tag{4.5}$$

$$E_i - E_F = kT\ ln\left(\frac{p_0}{n_i}\right)$$

$$E_F = E_i - 0.289\ eV$$

It is found that the Fermi level of p-type Si substrate with the dopant concentration of 7.64×10^{14} cm^{-3} is 0.289 eV below the intrinsic Fermi level or 0.261 above the valence band edge of silicon substrate.

4.4 Neutral Flatband Voltage Determination

4.4.1 Flatband Voltage Calculation

Two materials share the same free electron level at the interface when they are brought into contact because at the interface of two materials, an electron that is free from the crystal field of one material is also free from the crystal field of the other material. Metal such as aluminum has smaller work function than that of silicon, so the flatband condition is reached by applying a negative gate voltage, called the flatband voltage, with respect to the

silicon substrate. Flatband voltage (V_{FB}) in semiconductor is an important parameter in the MOS (metal-oxide-semiconductor) structure and it influences the threshold voltage (V_T), which is the fundamental parameter of any MOS device[12]. The V_{FB} voltage is the gate voltage required to make the energy bands in the semiconductor flat up to the semiconductor-dielectric interface, as schematically shown in Figure 4.4. The V_{FB} voltage is given by the well known formula:

$$V_{FB} = \phi_{MS} - \frac{Q_{eff}}{C_{OX}} \tag{4.6}$$

where ϕ_{MS} is contact potential difference in MOS structure [V], Q_{eff} is the equivalent oxide charge per unit area at the oxide-silicon interface [C/cm^2], and C_{OX} is the oxide capacitance per unit area, for an oxide film of thickness t_{ox} and permittivity ε_{ox} [F/cm^2].

The relative importance of the ϕ_{MS} and Q_{eff} values for the value of V_{FB} with time, as new technology is being introduced. The better control of the technological process is achieved, hence lower Q_{eff} values are typically obtained. By applying current technology in MOS structure fabrication, the Q_{ox}/q at the Si – SiO_2 interface can be controlled to below

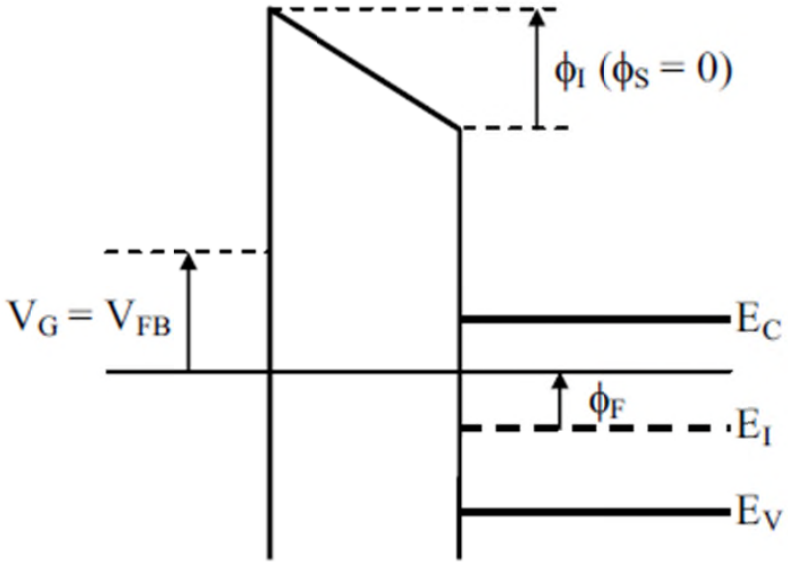


Figure 4.4 Band diagram of the MOS structure for the flat-band state in semiconductor ($\phi_S = 0$).

10^{10} cm^{-2} with the contribution to the V_{fb} is less than 50 mV for thin gate oxides below 20 nm. Therefore, the flatband voltage is mainly determined by the work function difference ϕ_{ms}.

The V_{FB} voltage has a great practical importance, so it is necessary to determine its value accurately. The methods of the flat-band voltage V_{FB} determination can be divided into three groups, including computational and graphical both based on $C(V_G)$ characteristic measurement of MOS structure and photoelectric method, in which the light is a medium.

In our works, flatband voltage is calculated by applying "calculation C_{FB} method". In this method the experimental $C(V_G)$ characteristic measured on MOS structure and the value of the C_{FB} capacitance obtained by appropriate calculations is needed. The C_{FB} value is defined as [12]:

$$C_{FB} = \frac{C_{OX} \cdot C_{sFB}}{C_{OX} + C_{sFB}} \tag{4.7}$$

where, C_{sFB} is semiconductor surface capacitance [F/cm^2].

The C_{sFB} value is calculated as follows

$$C_{sFB} = \frac{\varepsilon_s \cdot \varepsilon_0}{L_D} \tag{4.8}$$

where ε_s is electric permittivity of the semiconductor, ε_0 is electric permittivity of the vacuum [F/cm], and L_D is Debye's length [cm].

The L_D value can be expressed:

$$L_D = \sqrt{\frac{kT\varepsilon_s\varepsilon_0}{q^2 N_D}} \tag{4.9}$$

where k is Boltzmann's constant [J/K], T is temperature [K], q is electron charge [C], and N_D is doping concentration [1/cm^3].

Finally, having measured $C(V_G)$ characteristic and having calculated C_{FB} value (using the same parameters of the structure) the V_{FB} value is given by the corresponding value of the gate voltage V_G for C_{FB} capacitance. Figure 4.5 shows a schematic illustration of this method.

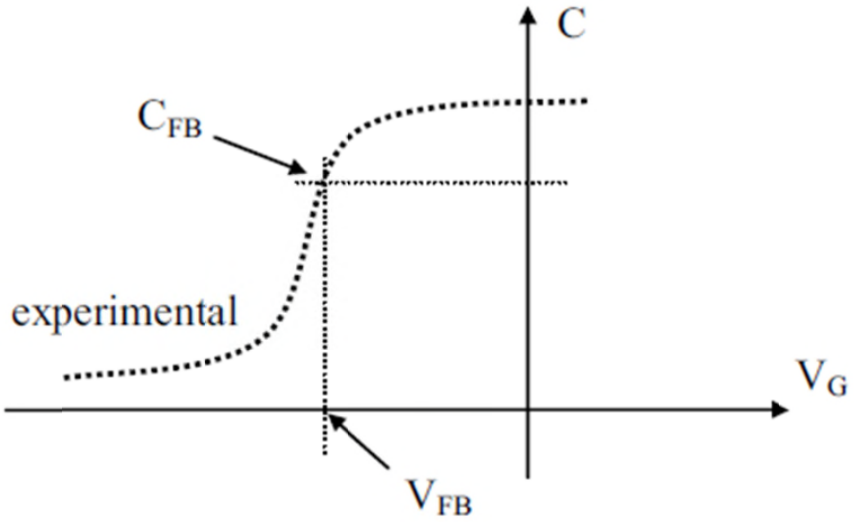


Figure 4.5 The C_{FB} value placed on experimental $C(V_G)$ characteristic indicates the gate voltage $V_G = V_{FB}$ for flat-band state in semiconductor.

4.4.2 Neutral Flatband Voltage in As-deposited MAHOS Capacitor Structures

Since the MAHOS structures, which consists of aluminum gate electrode/Al_2O_3/ high-κ/SiO_2/p-type Si, use high-κ dielectric materials as charge trapping layers, the flatband voltage in flatband condition is referred as neutral flatband voltage, V_{nfb}, to distinguish it with that after charge injection. The qV_{nfb} of as-deposited MAHOS structures is shown in Table 4.2. qV_{nfb} means the amount of energy gained by the charge of a single electron move across an electric potential difference of V_{nfb}. The binding energy of Al $2p_{3/2}$ of Al_2O_3 blocking oxide and the distance between the binding energy of Al $2p_{3/2}$ and the qV_{nfb} are

Table 4.2 The qV_{nfb} of the as-deposited MAHOS structure and the core level of Al $2p_{3/2}$ of Al_2O_3 blocking oxide in the MAHOS structure.

Sample	qV_{nfb} (eV)	CL Al $2p_{3/2}$ (eV)	CL Al $2p_{3/2}$ – V_{nfb} (eV)
A1	-0.531	73.891	74.422
HA1	-0.543	73.876	74.419
NA1	-0.648	73.845	74.493
NB1	-0.415	73.998	74.413

also shown in the table. It is found that in as-deposited MAHOS structures, the distance between the binding energy of Al $2p_{3/2}$ and the qV_{nfb} is similar for all structures which is 74.45 ± 0.04 eV. This result shows that the V_{nfb} is influenced by the structure and dipole formation at the interface between layers.

All MAHOS structures use Al_2O_3 as blocking oxide with the thickness of 10 nm, except sample A1 which use Al_2O_3 as charge trapping layer with the thickness of 15 nm. The layer of Al_2O_3 in as-deposited samples has amorphous structure. Therefore, the binding energy of Al $2p_{3/2}$ relative to the Fermi edge of the Al_2O_3 has to be similar. However, since the work function of semiconductor or oxide cannot be determined from a photoemission spectrum of semiconductor alone, what can be obtained from the initial spectrum is some highest kinetic energy corresponding to the VBM and a lowest kinetic energy which is zero.[13] The measured binding energy of core level shifts because the Fermi level pinning and band bending which is due to dipole formation at the interface between two high-κ dielectric layers and the interface between high-κ dielectric layer and SiO_2/Si occurs. This result is indicated by similar magnitude of shift in the binding energy of Al $2p_{3/2}$ of Al_2O_3 blocking oxide and qV_{nfb} with similar difference between the binding energy of Al $2p_{3/2}$ and the qV_{nfb} for all as-deposited MAHOS structures with the accuracy of 0.04 eV. Therefore, the neutral flatband voltage of as-deposited MAHOS structures given can be written as follow

$$V_{fb} = (\phi_m - \phi_s) - E_{dipole} = \phi_{ms} - E_{dipole} \quad (4.10)$$

4.5 Charge Trapping in As-deposited MAHOS Capacitor Structures

The high frequency (1 MHz) C – V characteristics of as-deposited Al/Al_2O_3/SiO_2/ p-type Si capacitor structure (sample A1) under sweep gate voltage from inversion to accumulation and under sweep gate voltage from accumulation to inversion are shown in Figure R4.1 and Figure R4.2, respectively. Its flatband voltage as a function of sweep gate

voltage is shown in Figure R4.3. Small flatband voltage shift (ΔV_{FB}) of 0.18 V is observed after applying the gate voltage (V_G) of 6 V. The flatband shift increase as the gate voltage increase with the ΔV_{FB} of 0.36 V after applying the V_G of 14 V. After applying the gate voltage of -12 V, the ΔV_{FB} slightly decreases to 0.3 V from the initial ΔV_{FB} of 0.36 V. The ΔV_{FB} decreases significantly after applying the gate voltage of -13, -14, and -15 V. The ΔV_{FB} becomes -0.87 V after applying the V_G of -15 V.

Figure R4.4, Figure R4.7, and Figure R4.10 shows the high frequency (1 MHz) C – V characteristics of as-deposited Al_2O_3/HfAlO/SiO_2/p-type Si structure (sample HA1), Al/ Al_2O_3/[HfO_2/Al_2O_3]$_4$/HfO_2/SiO_2/p-type Si structure (sample NA1), and Al/Al_2O_3/[HfO_2/ Al_2O_3]$_2$/HfO_2/SiO_2/p-type Si structure (sample NB1) under sweep gate voltage from inversion to accumulation, respectively, while Figure R4.5, Figure R4.8, and Figure R4.11 are under sweep gate voltage from accumulation to inversion, respectively. The flatband voltage as a function of sweep gate voltage is shown in Figure R4.6, Figure R4.9, and Figure R4.12. The V_{FB} of sample HA1, NA1, and NB1 starts to shift to positive value after applying the V_G of 7 V, 6 V, and 5 V with the ΔV_{FB} of 0.29 V, 0.63 V, and 0.42 V, respectively. The V_{FB} of the samples increases significantly up to the V_G of 10 V. The ΔV_{FB} of sample HA1, NA1, and NB1 after applying the V_G of 15 V are 2.1 V, 2.63 V, and 2.82 V, respectively. Under sweep gate voltage from accumulation to inversion, V_{FB} decreases with small ΔV_{FB} from the initial ΔV_{FB} of 2.1 V to 0.86 V, 2.63 V to 1.08 V, and 2.82 V to 0.88 V for sample HA1, NA1, and NB1, respectively, under the V_G of -11 V. By increasing the negative V_G, the positive ΔV_{FB} is reduced significantly and the ΔV_{FB} becomes negative.

Flatband voltage as a function of gate voltage of sample A1, HA1, NA1, and NB1 under sweeping voltage from inversion to accumulation is shown in Figure R4.13 to compare the value of ΔV_{FB} in each sample. It is observed that the ΔV_{FB} of sample A1 < ΔV_{FB} of sample HA1 < ΔV_{FB} of sample NA1 < ΔV_{FB} of sample NB1. These results show that the

MAHOS structures with Al_2O_3/HfO_2 nanolaminates as CTL trap more electrons than the structures with Al_2O_3 and HfAlO single layer as CTL. Compared to the structure with Al_2O_3 as CTL, the structure with HfAlO as CTL traps more electrons since it is a mixture with HfO_2. The MAHOS structure with $[Al_2O_3$ (2 nm)/HfO_2 (2 nm)$]_2$/ HfO_2 (2 nm) as CTL traps more electrons than the structure with $[Al_2O_3$ (1 nm)/HfO_2 (1 nm)$]_2$/ HfO_2 (1 nm) since thicker HfO_2 in nanolaminate provides more sites to trap electrons. On the other hand, Al_2O_3 layer in nanolaminate prevents charge injection to the next HfO_2 layer since it has higher conduction band offset with respect to silicon substrate. The electron trapping into the CTL in the MAHOS structures which occurs under the V_G of about 5 V shows that the injection mechanism of electron is due to Fowler – Nordheim (F – N) tunneling. By this mechanism, electrons from Si substrate tunnel through triangular barrier of SiO_2. The F – N tunneling can be identified by measuring leakage current density as a function of sweep voltage which is discussed in the next sub chapter.

Flatband voltage as a function of gate voltage of sample A1, HA1, NA1, and NB1 under sweeping voltage from accumulation to inversion is shown in Figure R4.14. In all MAHOS structures, under the V_G of -3 V to about -11 V, the ΔV_{FB} decreases slightly which indicates detrapping of electrons from CTL to silicon substrate. Under the V_G of $\geq$ -12 V, ΔV_{FB} reduces significantly which indicates the injection of holes into the CTL in the MAHOS structures. Under more negative V_G, ΔV_{FB} becomes negative which means more holes are injected into CTL. These results show that the mechanism of erasing involves two charge transport which are electron detrapping and hole injection by F – N tunneling through tunnel oxide. Holes can be captured in the trap sites of CTL under high negative V_G since the valence band offset (VBO) of SiO_2 is higher than the conduction band offset (CBO) of SiO_2 with respect to Si substrate. Therefore, higher electric field is necessary so that holes can tunnel through triangular barrier by F – N tunneling. In case of hole trapping into CTL of

MAHOS structures, it is observed that the V_G of -15 V, the $-\Delta V_{FB}$ of sample A1 < $-\Delta V_{FB}$ of sample HA1 < $-\Delta V_{FB}$ of sample NA1 < $-\Delta V_{FB}$ of sample NB1 which show that the MAHOS structures with Al_2O_3/HfO_2 nanolaminates as CTL trap more holes than the structures with Al_2O_3 and HfAlO single layer as CTL.

4.6 Leakage Current Measurement in As-deposited MAHOS Capacitor Structures

The mechanism of charge transport in the MAHOS capacitor structure when the gate bias is applied can be identified by carrying out the leakage current measurement. Figure R4.15 – R4.18 shows the leakage current density as a function of sweep voltage of the sample A1, HA1, NA1, and NB1 respectively. For each sample, the measurement is conducted by measuring the leakage current density under the positive sweep voltage from 0 V – 35 V on one device and measuring the leakage current density under the negative gate voltage from 0 V – -35 V on different device.

The behavior of the current – voltage characteristics has two regions for dielectric materials. The current is due to thermally generated carriers in the low field region where electric field, E < 10^5 V/cm. When a large electric field is applied across an oxide layer, a significant electron or hole tunneling can take place. In order to analyze the conduction mechanism of MAHOS structures in the higher field region, the experimental J-E curves were fitted by Fowler – Nordheim tunneling models. $\ln(J/E^2)$ is plotted as a function of 1/E, which is known as a Fowler-Nordheim plot. E is the oxide electrical field and is given by,[14]

$$E_{ox} = \frac{\left[V_G - \frac{(\phi_m - \chi_s)}{q} - \psi_s\right]}{t_{ox}} \qquad (4.11)$$

The plot of $\ln J/E_{ox}^2$ vs $1/E_{ox}$ of sample A1, HA1, NA1, and NB1 under the positive sweep voltage and the negative sweep voltage are shown in the Figure R4.19 – R.22,

respectively. The linear region shows the FN tunneling. Linear fitting prove the FN tunneling is the main charge transport mechanism under certain electric field. Electron injection from the gate electrode into the charge trapping layer in the MAHOS structures with high-κ dielectric materials as CTL is schematically indicated in Figure R4.23 – R4.26.

4.7 Summary

In this chapter, the charge trapping characteristics in as-deposited MAHOS capacitor structures with heterostructure of Al_2O_3/HfO_2 nanolaminates as charge trapping layers (CTL) has been investigated by inductance – capacitance – resistance (LCR) meter. The mechanism of charge trapping has been explained by considering the leakage current density as a function of sweep voltage measured by semiconductor analyzer system and considering the energy band structures of MAHOS capacitors.

Some important points are summarized below from all results discussed in this chapter,

1. The neutral flatband voltage in the as-deposited MAHOS structures is not only depends on the work function difference between metal and semiconductor, but also is affected by the dipole formation at the interface between high-κ materials and between high-κ dielectric with SiO_2/Si stack. The influence of dipole formation is indicated by the similar shift in the binding energy of Al $2p_{3/2}$ and neutral flatband voltage.
2. As-deposited MAHOS capacitor structures with heterostructure of Al_2O_3/HfO_2 nanolaminates as CTL trap more electron than the structures with Al_2O_3 and HfAlO as CTL.
3. The main charge transport mechanism for charge trapping is Fowler – Nordheim (F – N) tunneling mechanisms as indicated by leakage current density measurement and linear fitting with F – N tunneling equation.

References

[1] Yan Ny Tan, Wai Kin Chim, Wee Kiong Choi, Moon Sig Joo, and Byung Jin Cho. Hafnium Aluminum Oxide as Charge Storage and Blocking-Oxide Layers in SONOS-Type Nonvolatile Memory for High-Speed Operation. IEEE Transactions on Electron Devices, Vol. 53, no. 4, April 2006.

[2] Hee-Wook You and Won-Ju Cho. Charge trapping properties of the HfO_2 layer with various thicknesses for charge trap flash memory applications. Appl. Phys. Lett. 96, 093506 (2010).

[3] S. Maikap, H. Y. Lee, T-Y. Wang, P-J. Tzeng, C. C. Wang, L. S. Lee, K. C. Liu, J-R. Yang, and M-J. Tsai. Charge trapping characteristics of atomic-layer-deposited HfO_2 films with Al_2O_3 as a blocking oxide for high-density non-volatile memory device applications. Semicond. Sci. Technol. 22 (2007) 884–889.

[4] T. Sugizaki, M. Kohayashi, M. Ishidao, H. Minakata, M. Yamaguchi, Y. Tamura, Y. Sugiyama, T. Nakanishi, and H. Tanaka. Novel Multi-bit SONOS Type Flash Memory Using a High-k Charge Trapping Layer. Symposium on VLSl Technology Digest of Technical Papers. 2003.

[5] P. Pavan, R. Bez, P. Olivo, amd E. Zanoni. Flash Memory Cells - An Overview. Proc. IEEE 1997, 85, 1248–1271.

[6] M. Lenzlinger and E. H. Snow. Fowler‐Nordheim Tunneling into Thermally Grown SiO_2. J. Appl. Phys. 40, 278 (1969).

[7] J. Sune, P. Olivo, and B. Ricco. Quantum-mechanical modeling of accumulation layers in MOS structures. IEEE Trans. Electron Devices, vol. 39, no. 7, pp. 1732–1739, 1992.

[8] E. H. Nicollian and J. R. Brews. MOS Physics and Technology. Bell Telephone Laboratories, Inc. 1982. USA.

[9] Annual Book of ASTM Standards, Volume 10.05: Electronics. Standard Practice for

Conversion Between Resistivity and Dopant Density for Boron-Doped, Phosphorus-Doped, and Arsenic-Doped Silicon.

[10] Martin A. Green. Intrinsic concentration, effective densities of states, and effective mass in silicon. Journal of Applied Physics 67, 2944 (1990).

[11] A. B. Sproul and M. A. Green. Improved value for the silicon intrinsic carrier concentration from 275 to 375 K. Journal of Applied Physics 70, 846 (1991).

[12] K. Piskorski and H. M. Przewlocki. The methods to determine flat-band voltage VFB in semiconductor of a MOS structure. MIPRO 2010, May 24-28, 2010, Opatija, Croatia.

[13] Rudy Schlaf. Calibration of Photoemission Spectra and Work Function Determination.

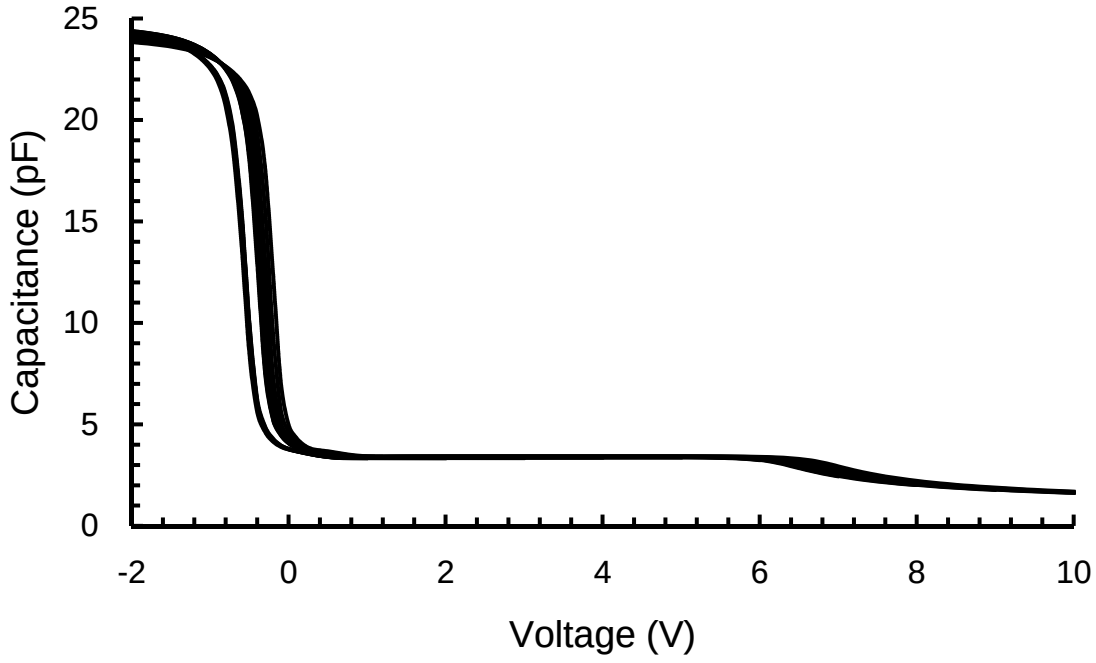


Figure R4.1 High frequency (1 MHz) C – V characteristics of as-deposited Al/Al_2O_3/SiO_2/ p-type Si capacitor structure under sweep gate voltage from inversion to accumulation.

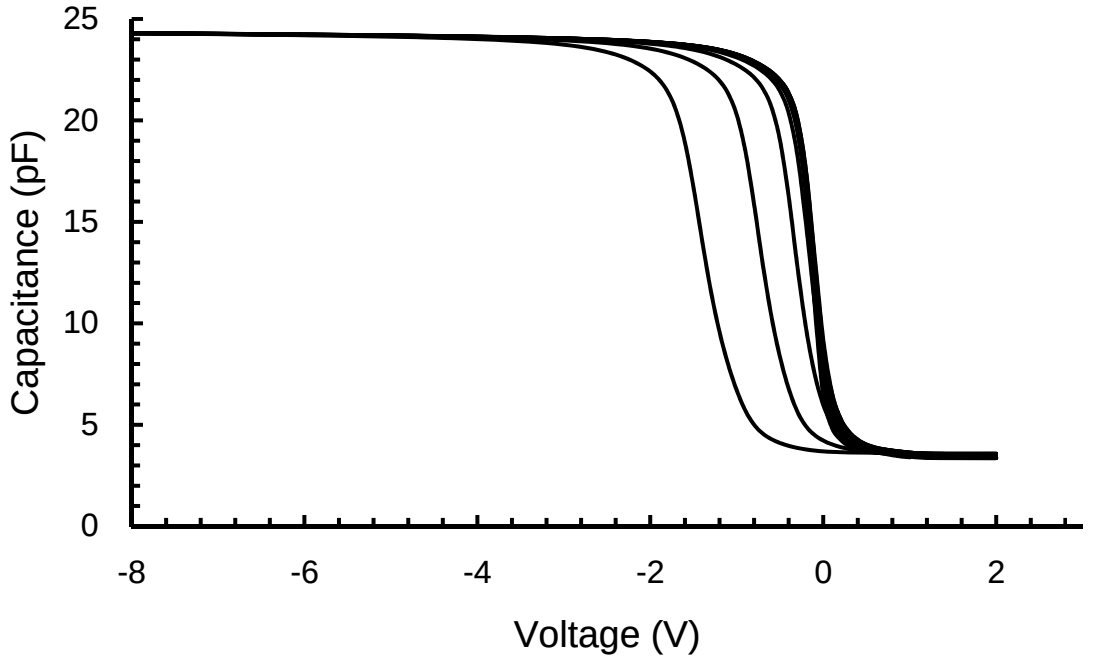


Figure R4.2 High frequency (1 MHz) C – V characteristics of as-deposited Al/Al_2O_3/SiO_2/ p-type Si capacitor structure under sweep gate voltage from accumulation to inversion.

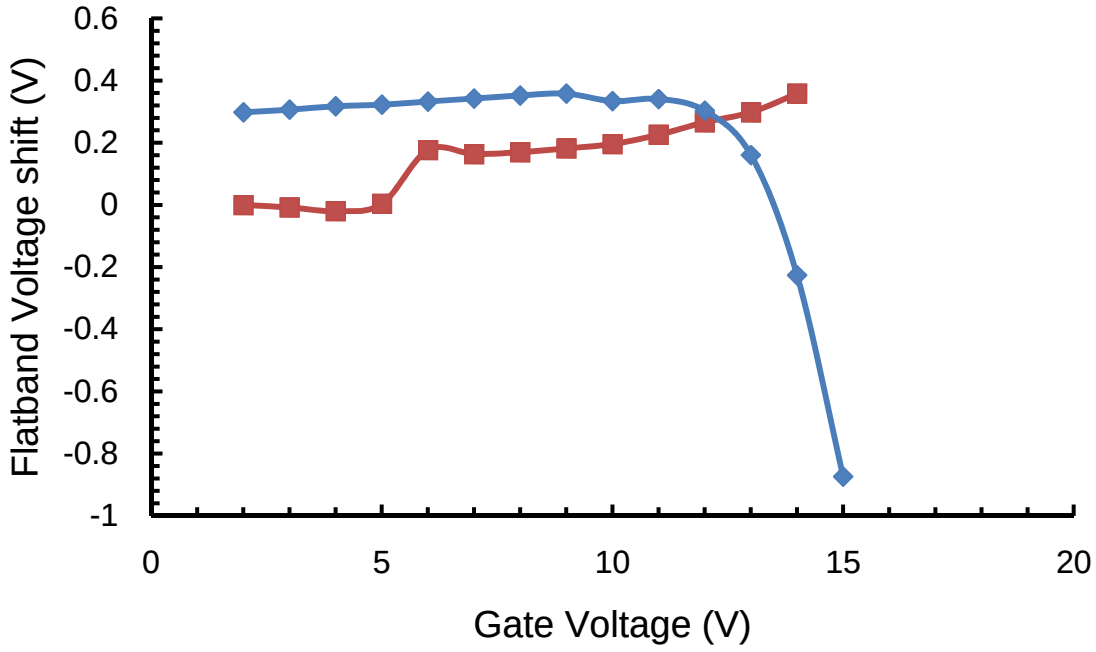


Figure R4.3 Flatband voltage as a function of sweep gate voltage of as-deposited $Al/Al_2O_3/SiO_2/$ p-type Si capacitor structure.

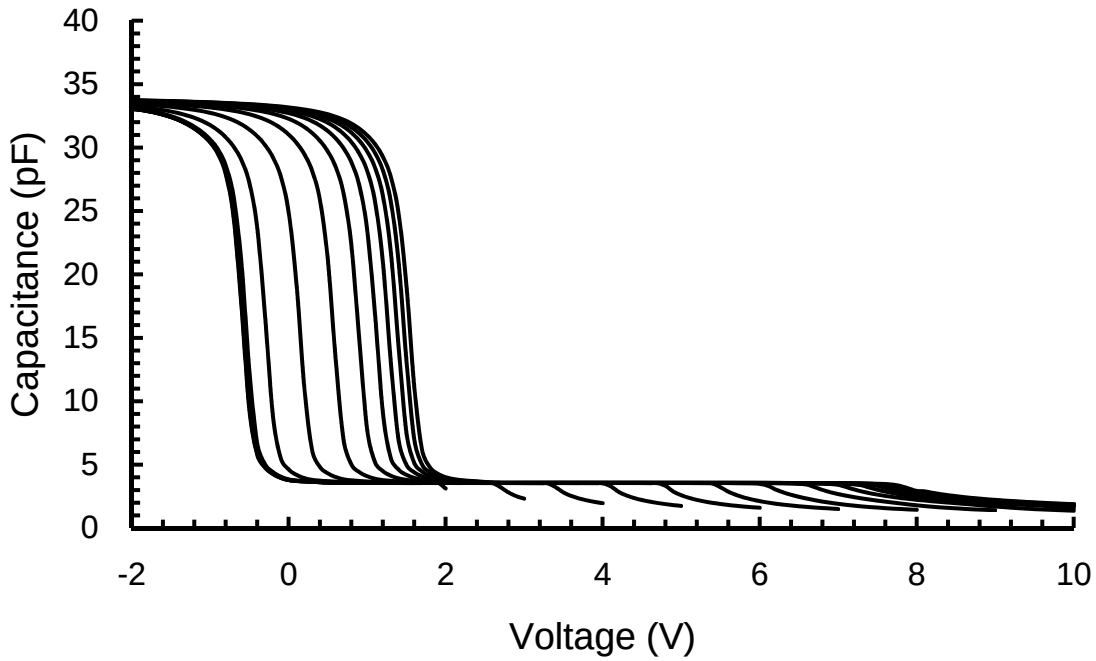


Figure R4.4 High frequency C – V characteristics of as-deposited $Al_2O_3/HfAlO/SiO_2$/p-type Si under sweep gate voltage from inversion to accumulation.

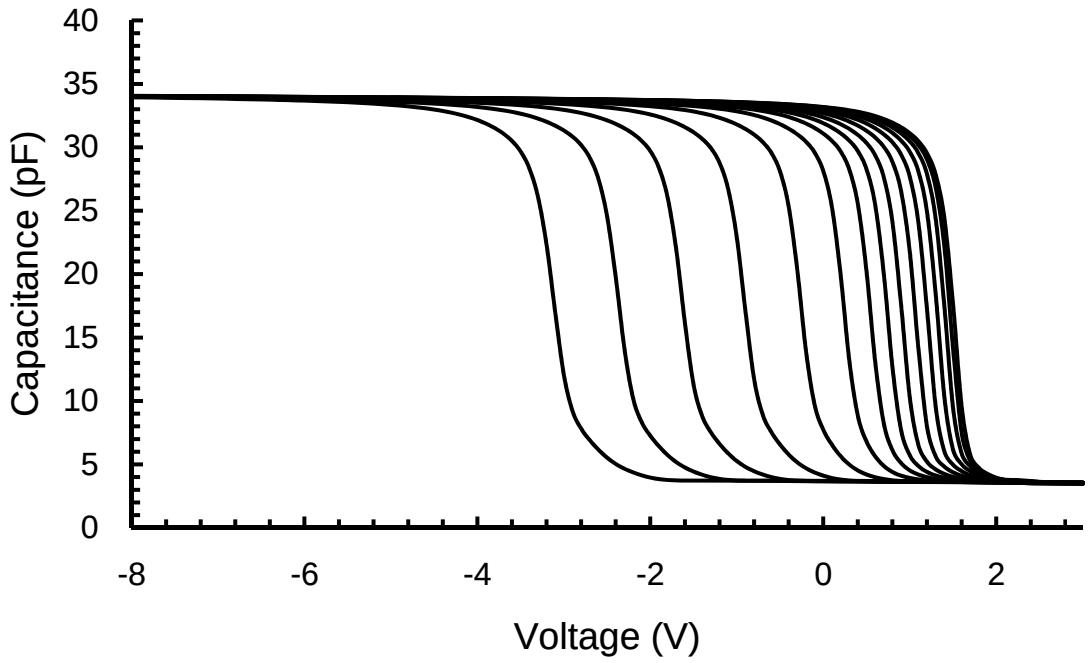


Figure R4.5 High frequency C – V characteristics of as-deposited Al_2O_3/HfAlO/SiO_2/p-type Si under sweep gate voltage from inversion to accumulation.

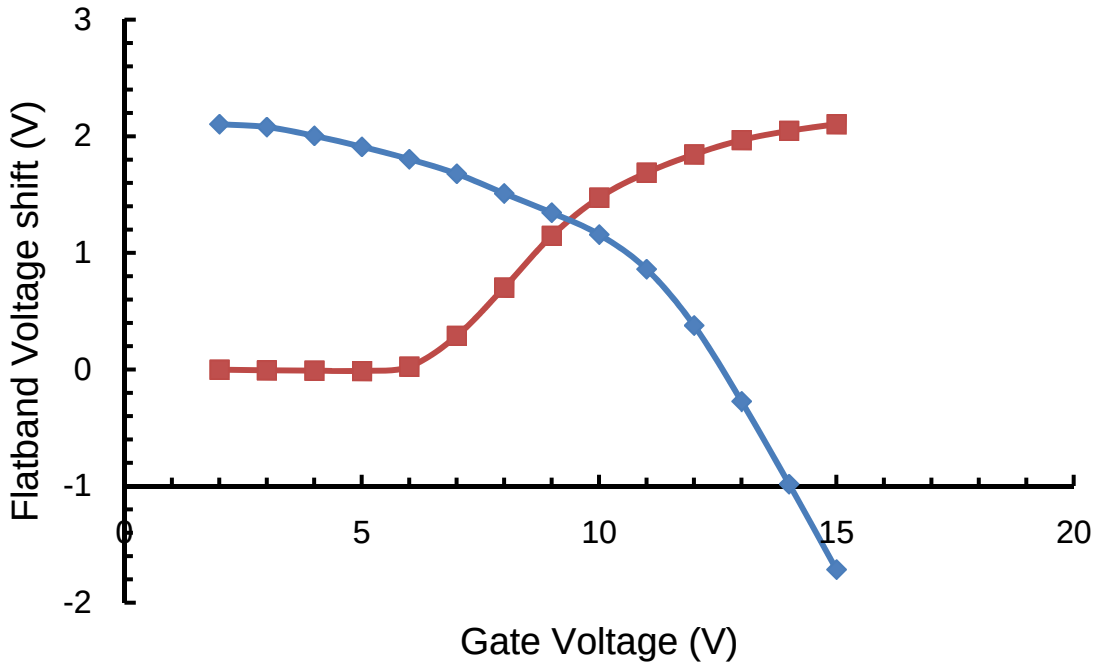


Figure R4.6 Flatband voltage as a function of sweep gate voltage of as-deposited Al_2O_3/HfAlO/SiO_2/p-type Si capacitor structure.

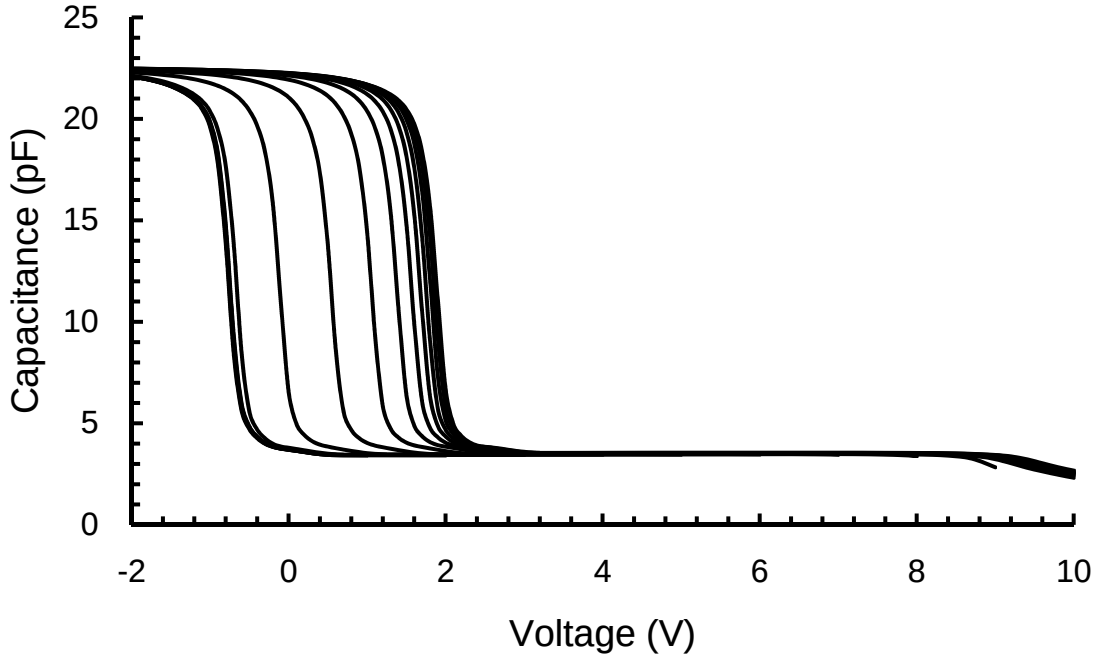


Figure R4.7 High frequency C – V characteristics of as-deposited Al/Al_2O_3/[HfO_2/ Al_2O_3]$_4$/HfO_2/SiO_2/p-type Si under sweep gate voltage from inversion to accumulation.

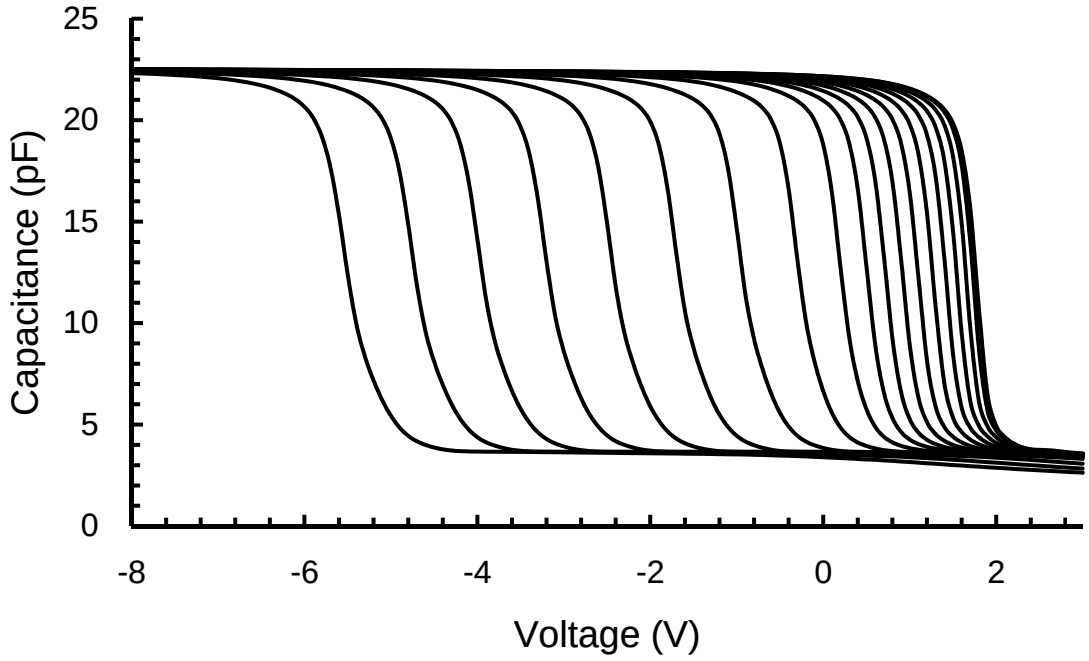


Figure R4.8 High frequency C – V characteristics of as-deposited Al/Al_2O_3/[HfO_2/ Al_2O_3]$_4$/HfO_2/SiO_2/p-type Si under sweep gate voltage from inversion to accumulation.

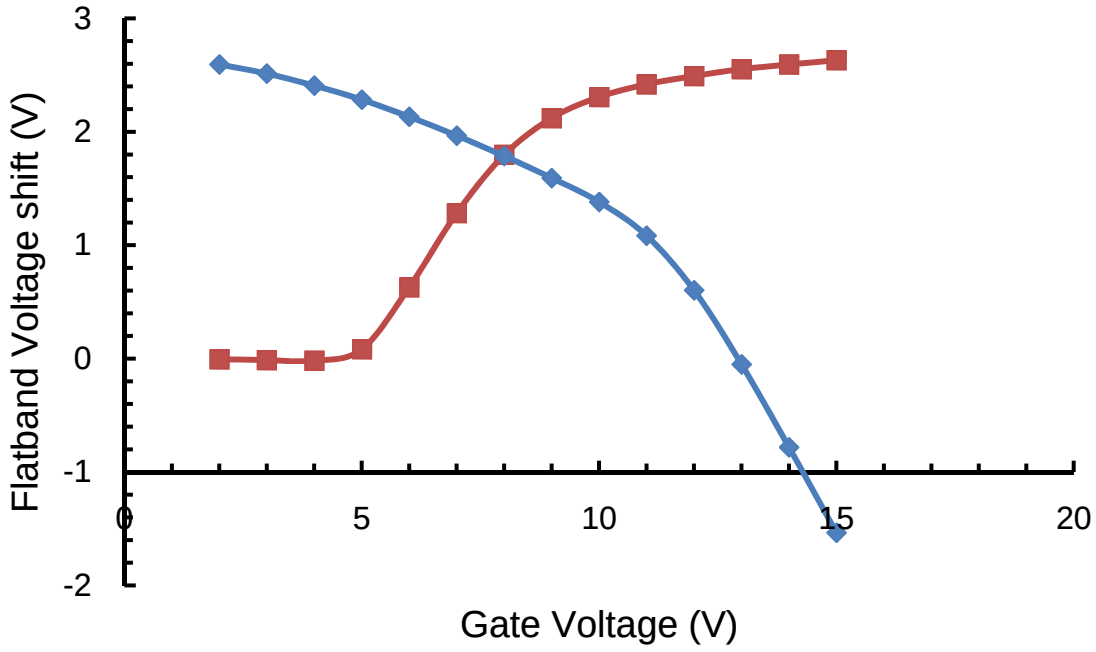


Figure R4.9 Flatband voltage as a function of sweep gate voltage of as-deposited $Al/Al_2O_3/[HfO_2/Al_2O_3]_4/HfO_2/SiO_2$/p-type Si capacitor structure.

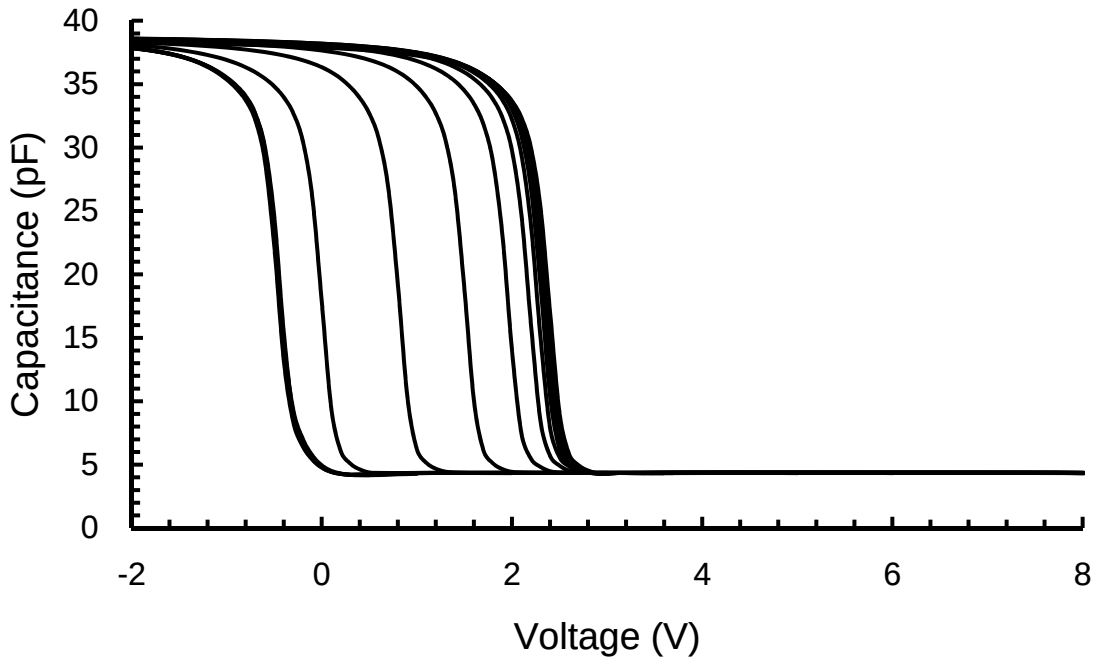


Figure R4.10 High frequency C – V characteristics of as-deposited $Al/Al_2O_3/[HfO_2/Al_2O_3]_2/HfO_2/SiO_2$/p-type Si under sweep gate voltage from inversion to accumulation.

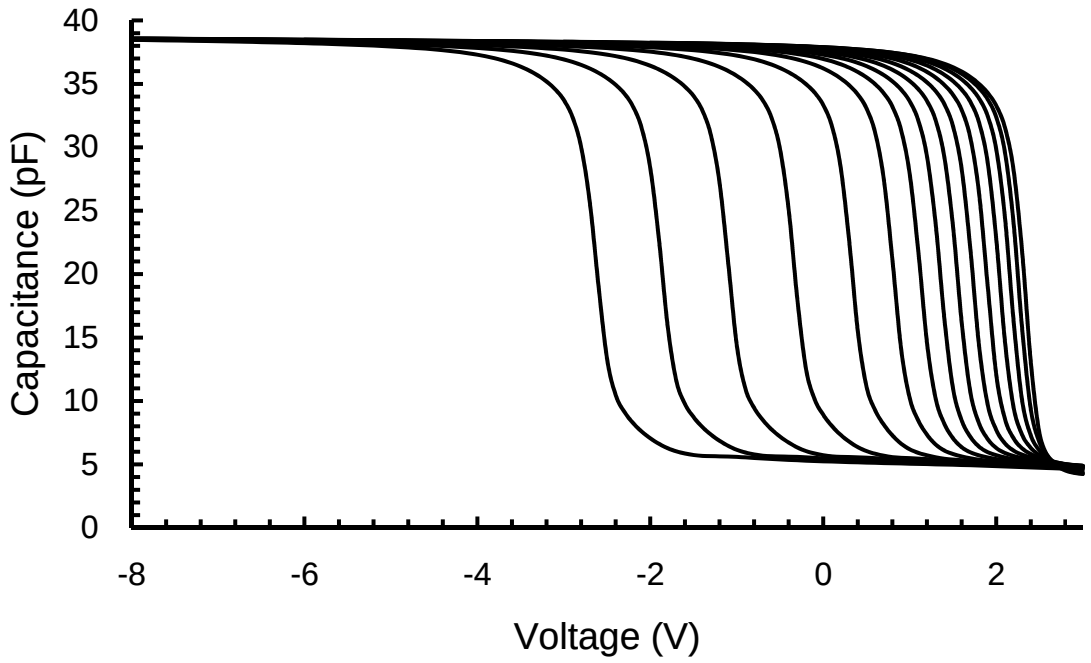


Figure R4.11 High frequency C – V characteristics of as-deposited Al/Al_2O_3/[HfO_2/Al_2O_3]$_2$/HfO_2/SiO_2/p-type Si under sweep gate voltage from accumulation to inversion.

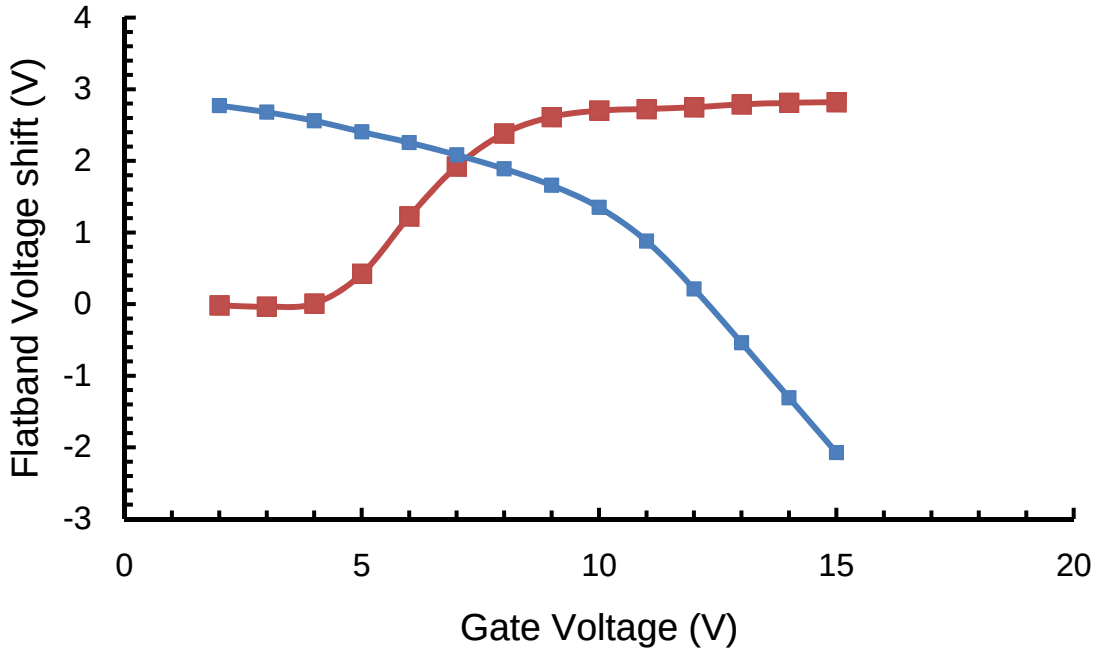


Figure R4.12 Flatband voltage as a function of sweep gate voltage of as-deposited Al/Al_2O_3/[HfO_2/Al_2O_3]$_2$/HfO_2/SiO_2/p-type Si capacitor structure.

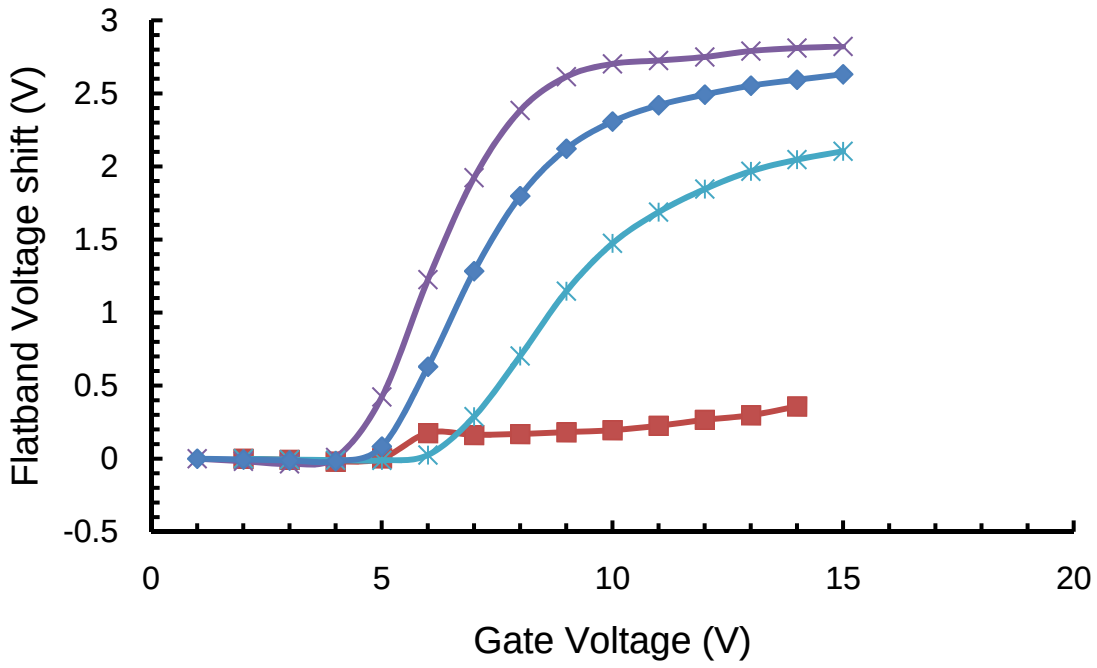


Figure R4.13 Flatband voltage as a function of sweep gate voltage of sample A1, HA1, NA1, and NB1 under sweeping voltage from inversion to accumulation.

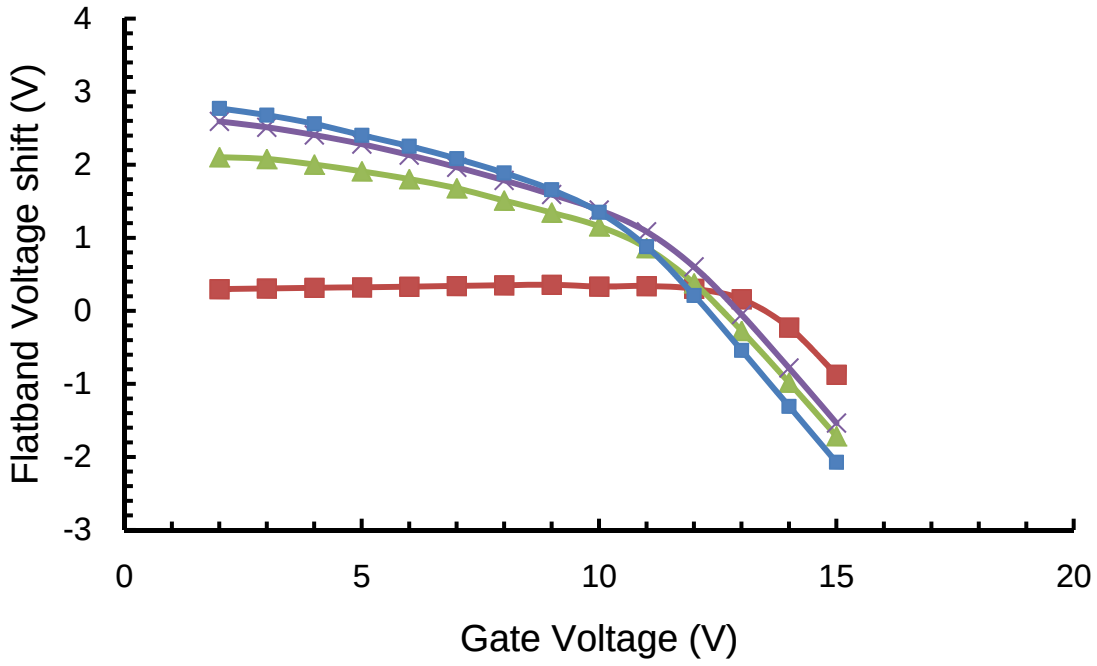


Figure R4.14 Flatband voltage as a function of sweep gate voltage of sample A1, HA1, NA1, and NB1 under sweeping voltage from accumulation to inversion.

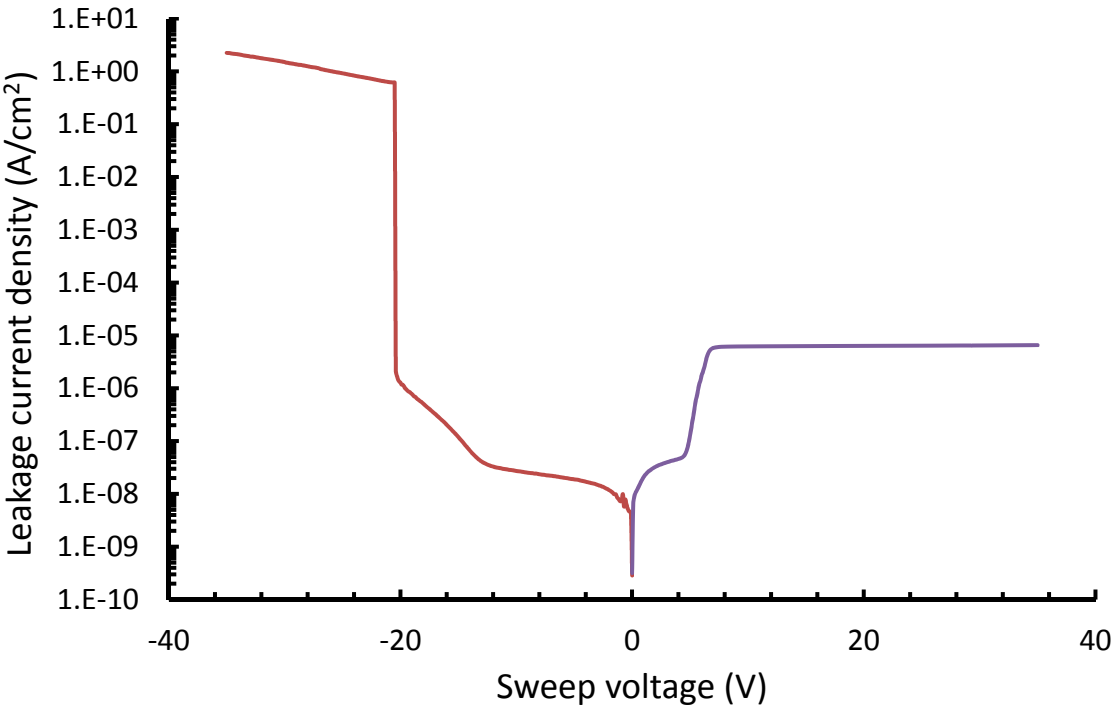


Figure R4.15 Leakage current density as a function of sweep voltage of as-deposited $Al/Al_2O_3/SiO_2$/p-type Si capacitor structure.

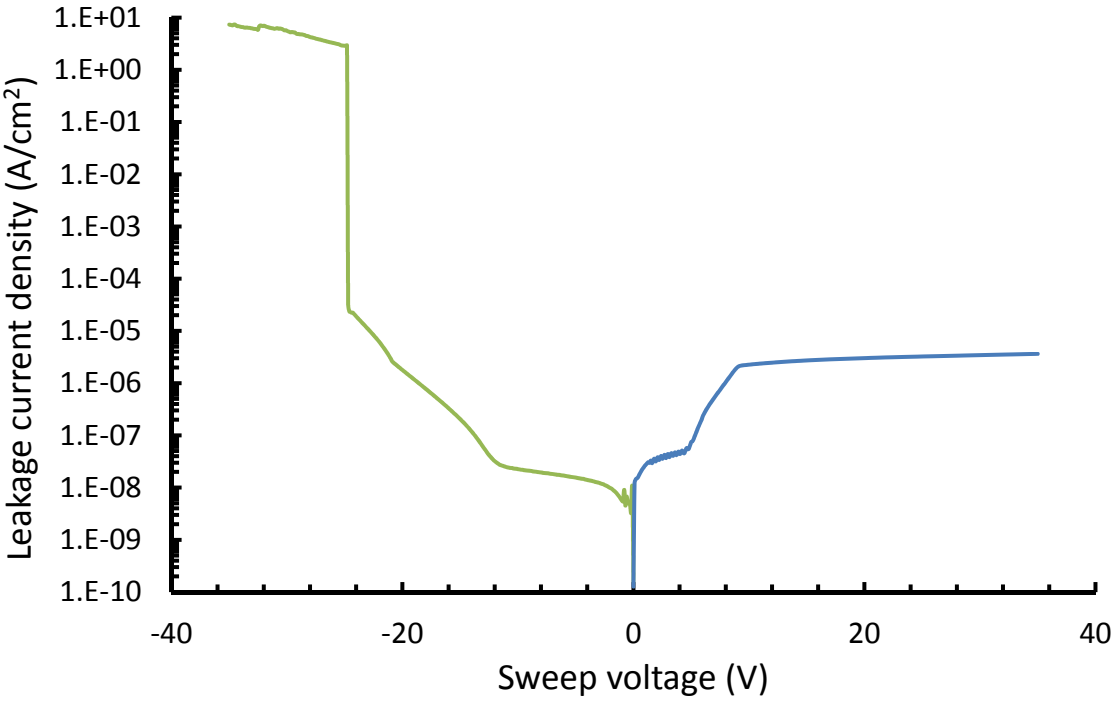


Figure R4.16 Leakage current density as a function of sweep voltage of as-deposited $Al_2O_3/HfAlO/SiO_2$/p-type Si capacitor structure.

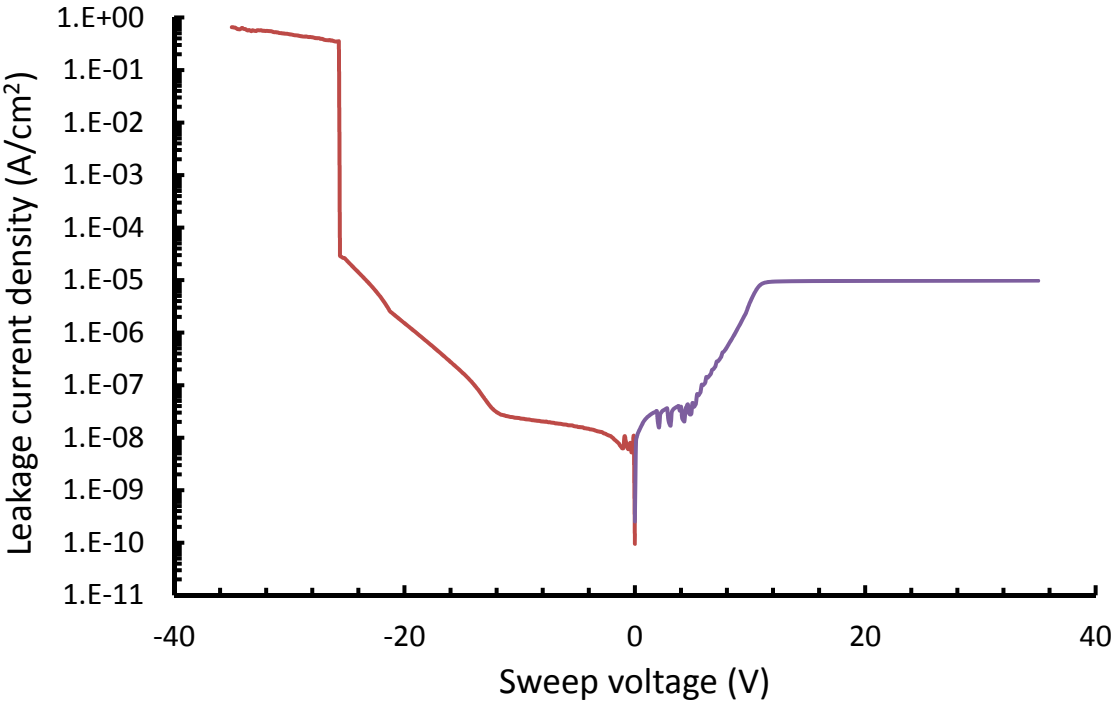


Figure R4.17 Leakage current density as a function of sweep voltage of as-deposited $Al/Al_2O_3/[HfO_2/Al_2O_3]_4/HfO_2/SiO_2$/p-type Si capacitor structure.

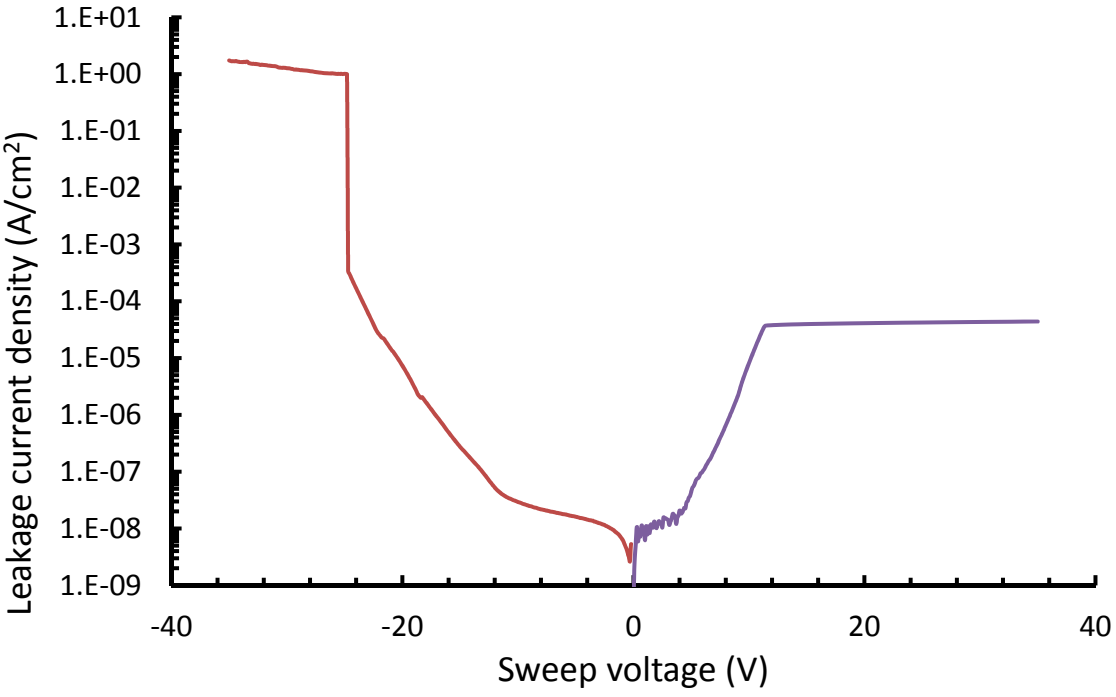


Figure R4.18 Leakage current density as a function of sweep voltage of as-deposited $Al/Al_2O_3/[HfO_2/Al_2O_3]_2/HfO_2/SiO_2$/p-type Si capacitor structure.

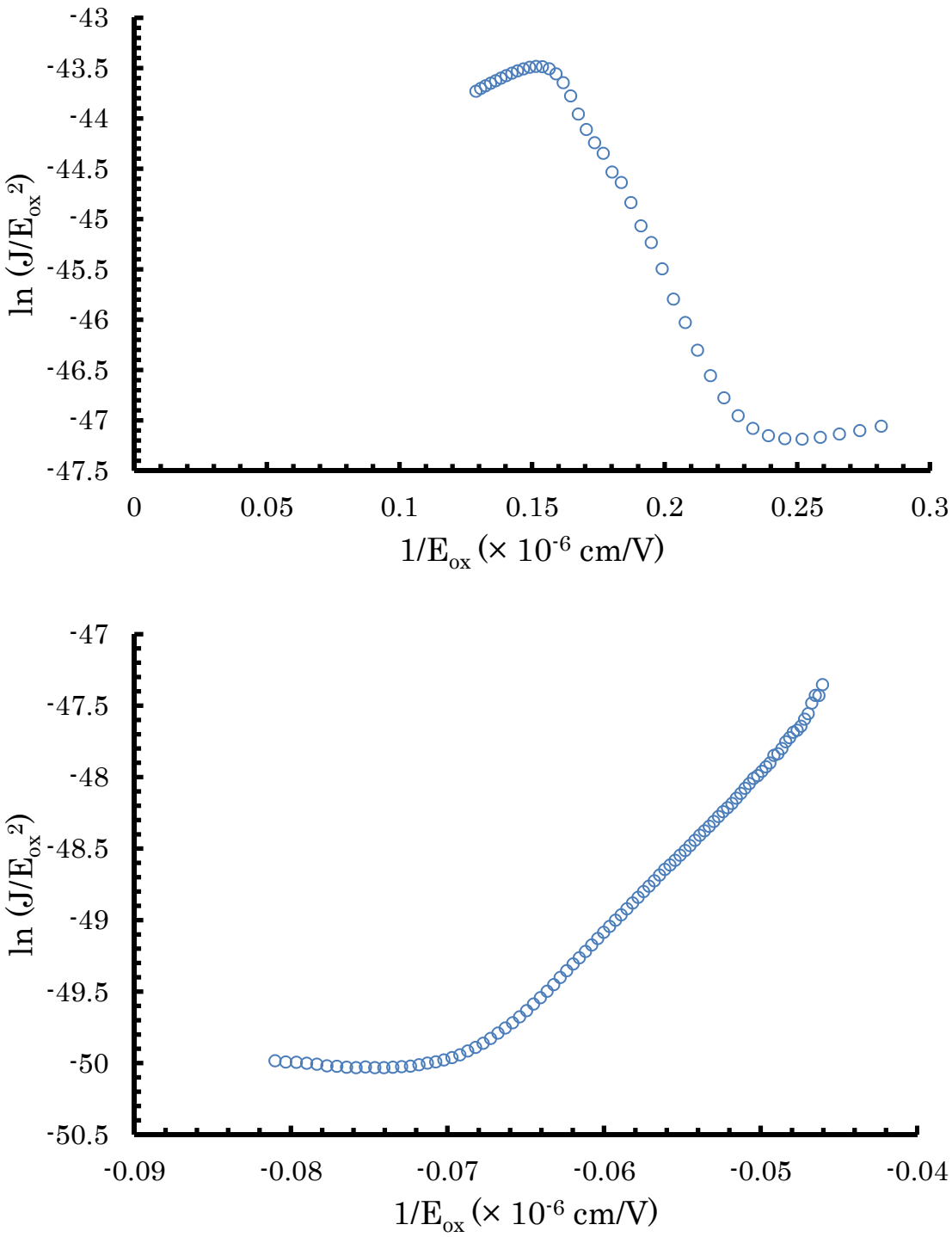


Figure R4.19 $\ln J/E_{ox}^2$ vs $1/E_{ox}$ of as-deposited $Al/Al_2O_3/SiO_2$/p-type Si capacitor structure under the positive sweep voltage (top) and the negative sweep voltage (bottom). The linear region shows the FN tunneling.

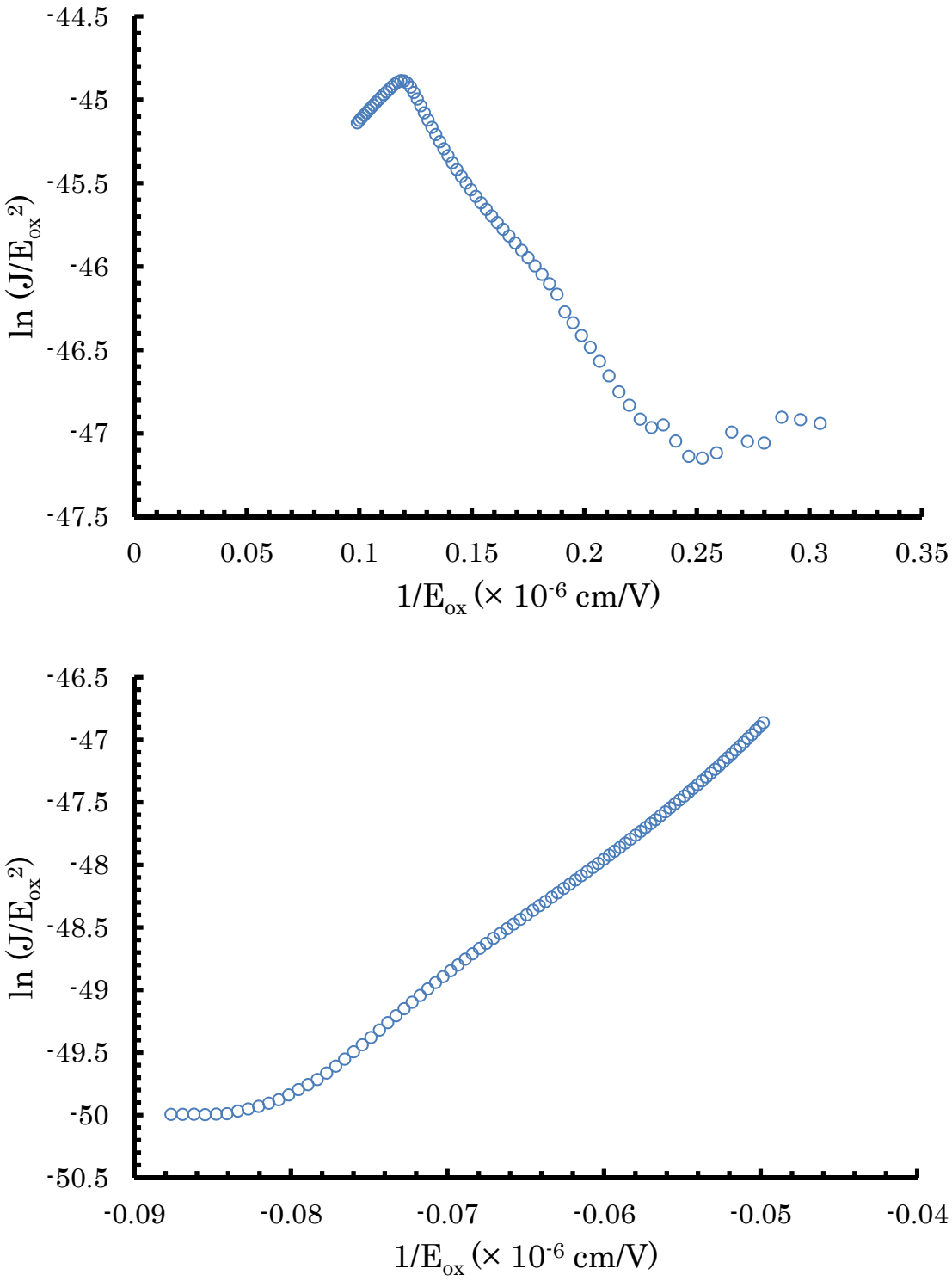


Figure R4.20 $\ln J/E_{ox}^2$ vs $1/E_{ox}$ of as-deposited $Al/Al_2O_3/HfAlO/SiO_2$/p-type Si capacitor structure under the positive sweep voltage (top) and the negative sweep voltage (bottom). The linear region shows the FN tunneling.

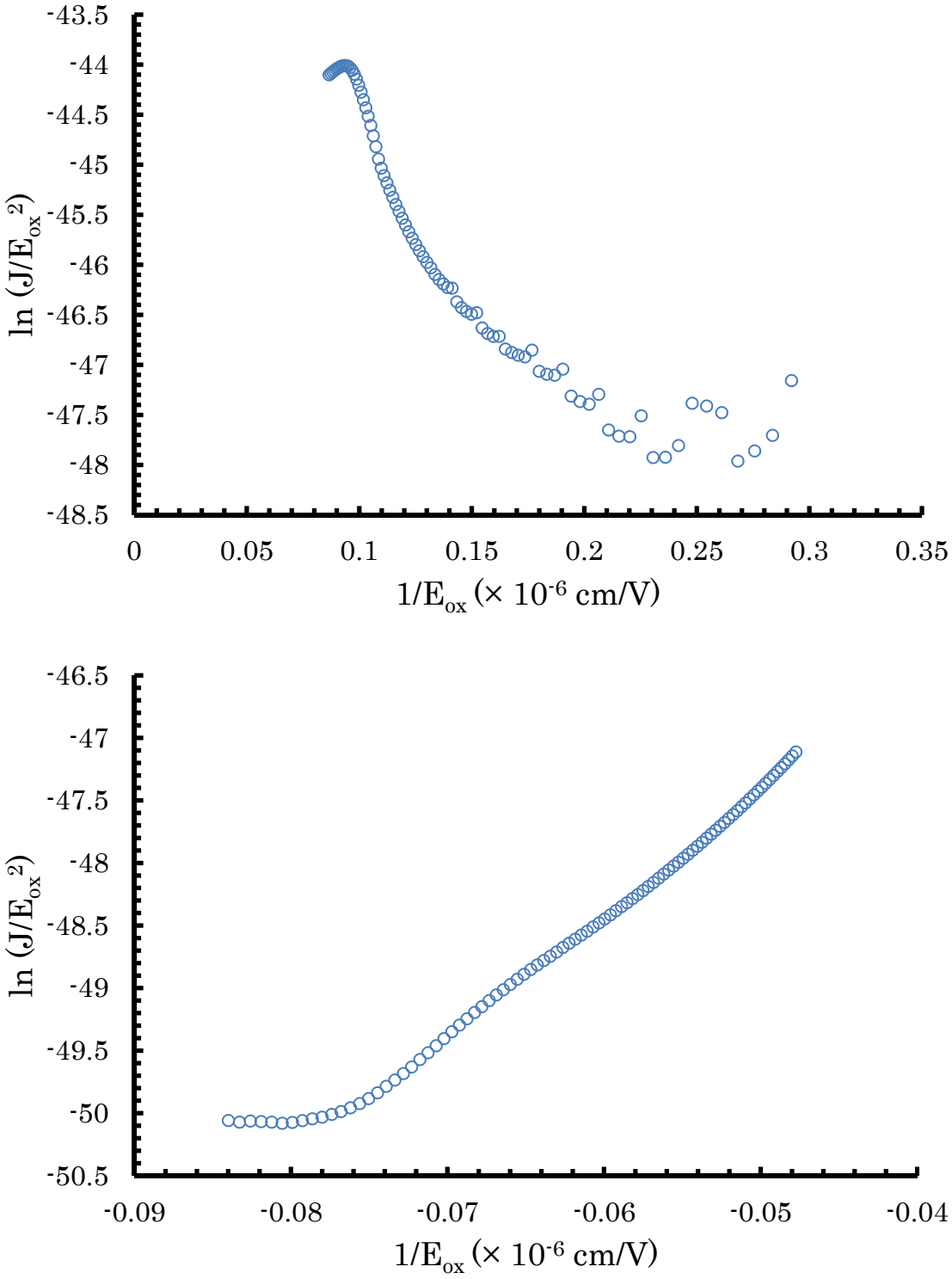


Figure R4.21 $\ln J/E_{ox}^2$ vs $1/E_{ox}$ of as-deposited $Al/Al_2O_3/[HfO_2/Al_2O_3]_4/HfO_2/SiO_2$ /p-type Si capacitor structure under the positive sweep voltage (top) and the negative sweep voltage (bottom). The linear region shows the FN tunneling.

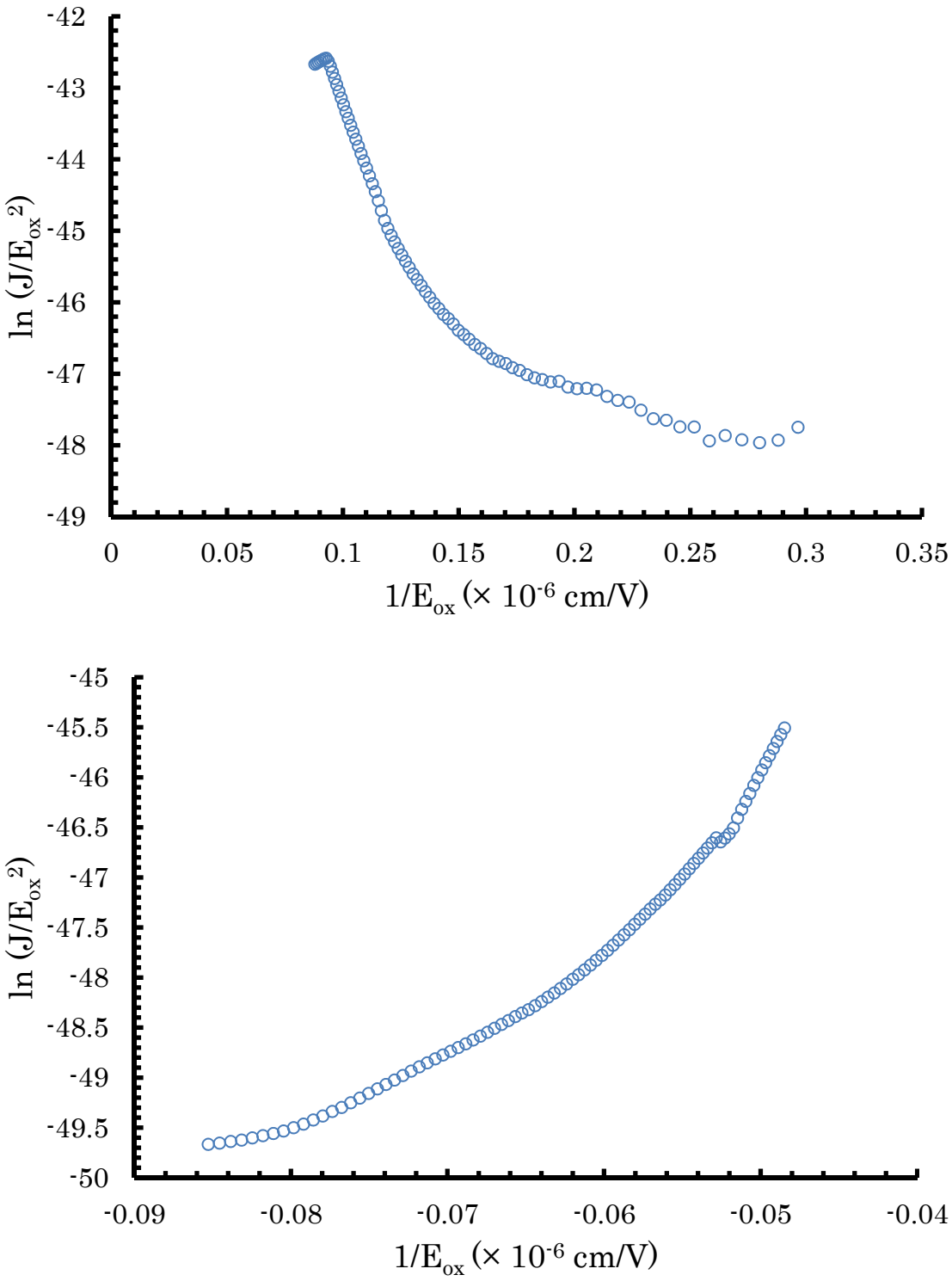


Figure R4.22 ln J/E_{ox}^2 vs $1/E_{ox}$ of as-deposited $Al/Al_2O_3/[HfO_2/Al_2O_3]_2/HfO_2/SiO_2$ /p-type Si capacitor structure under the positive sweep voltage (top) and the negative sweep voltage (bottom). The linear region shows the FN tunneling.

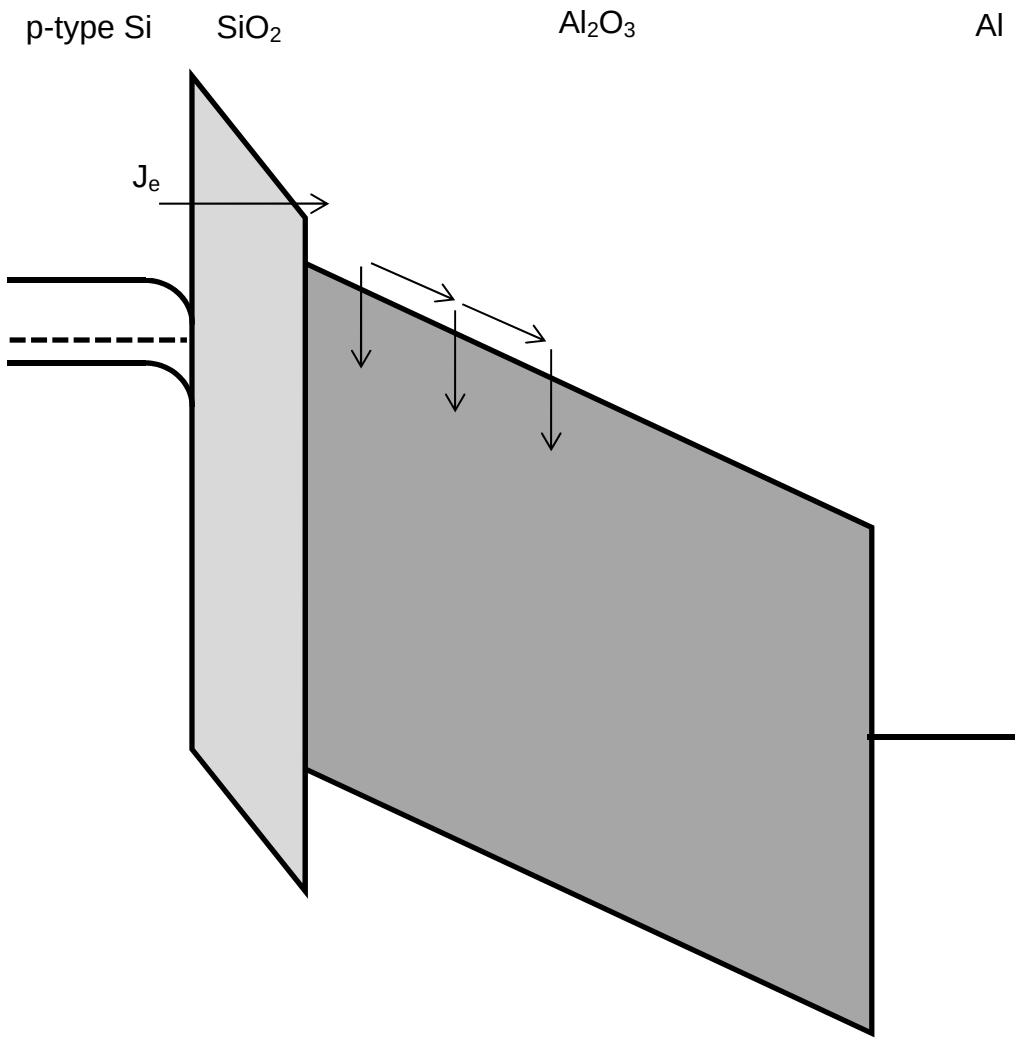


Figure R4.23 The band diagram of as-deposited $Al/Al_2O_3/SiO_2$/p-type Si capacitor structure under the positive V_G of 6 V.

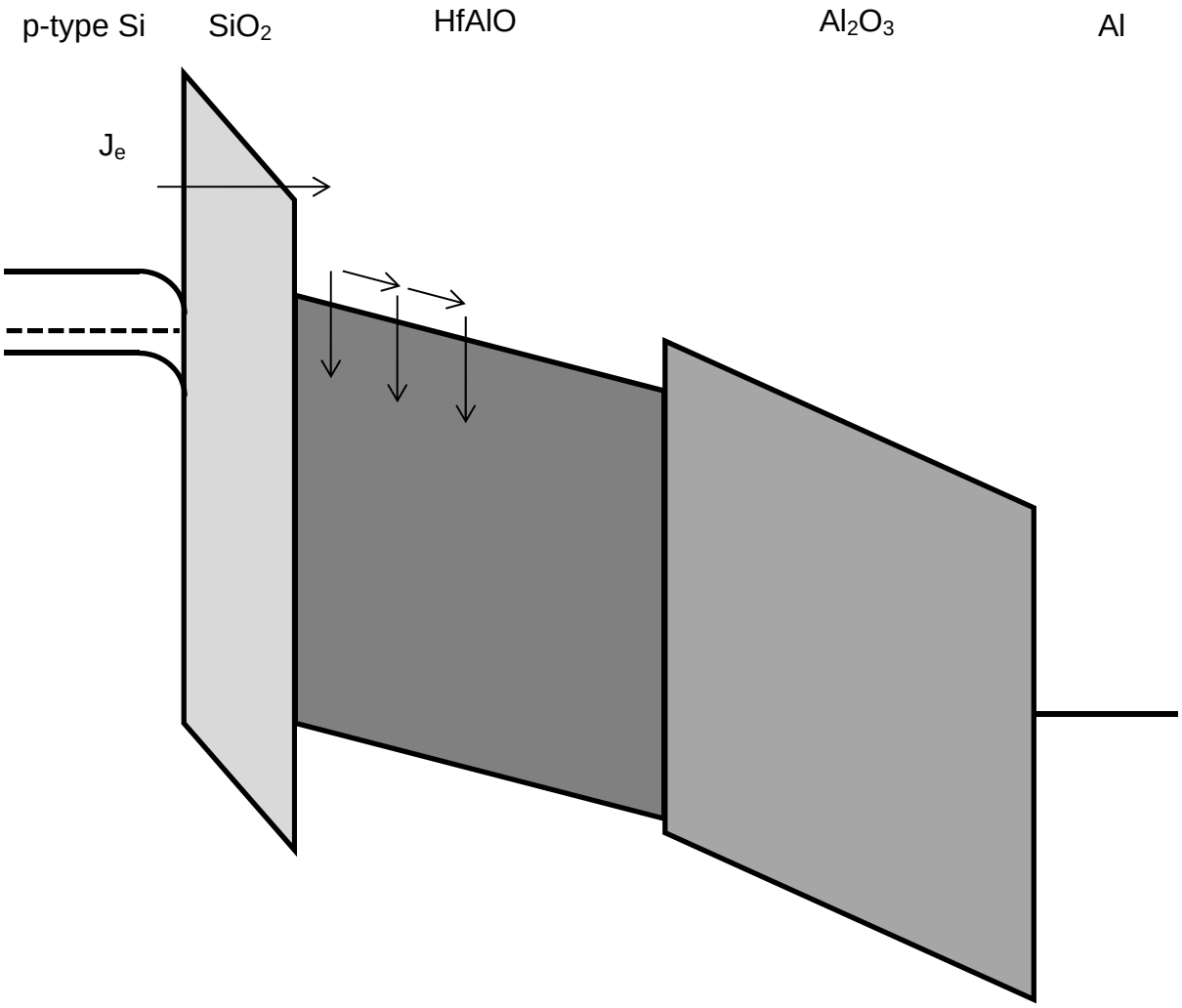


Figure R4.24 The band diagram of as-deposited $Al/Al_2O_3/HfAlO/SiO_2$/p-type Si capacitor structure under the positive V_G of 6 V.

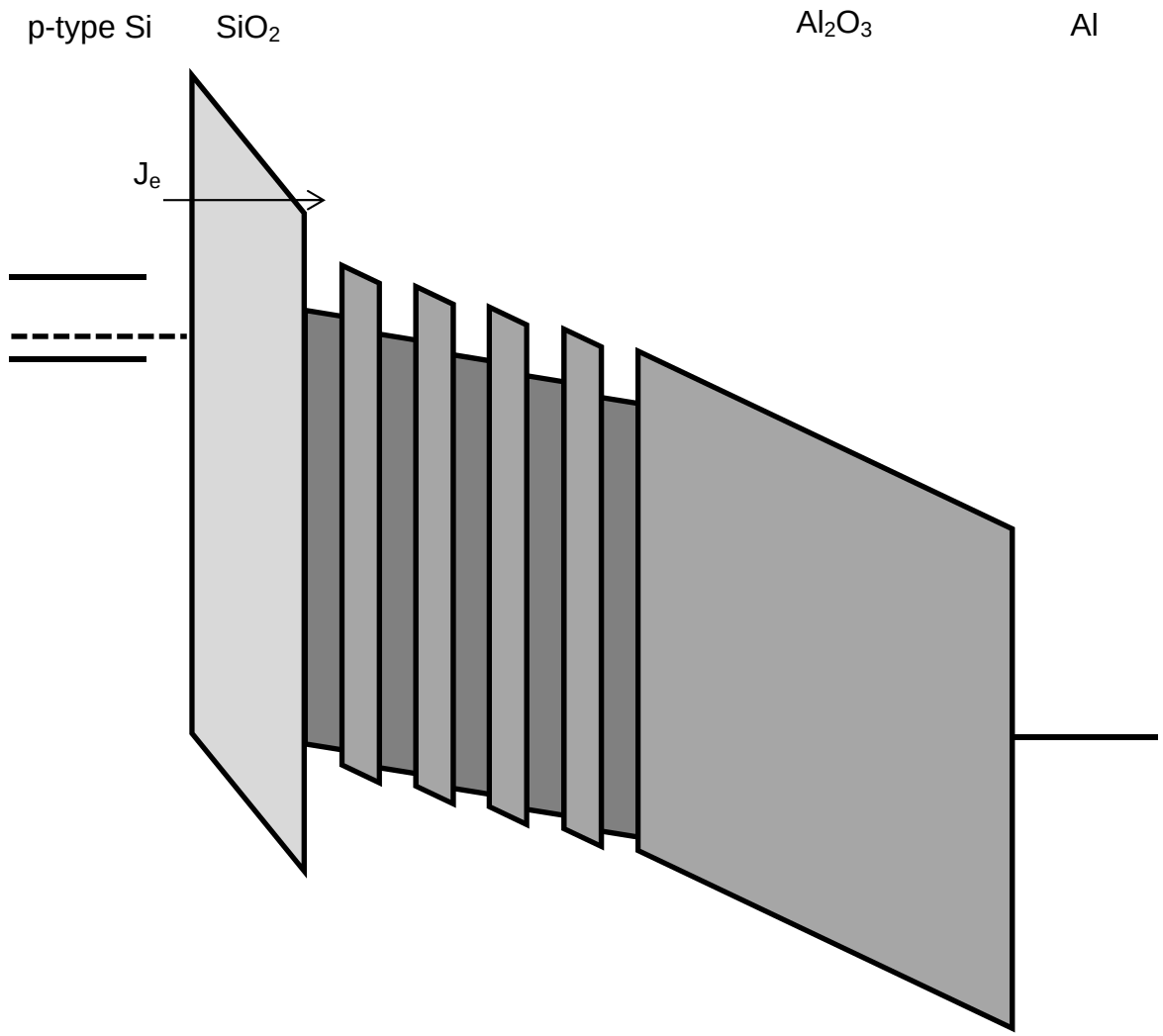


Figure R4.25 The band diagram of as-deposited Al/Al_2O_3/[Al_2O_3/HfO_2]$_4$/HfO_2/SiO_2/p-type Si capacitor structure under the positive V_G of 6 V.

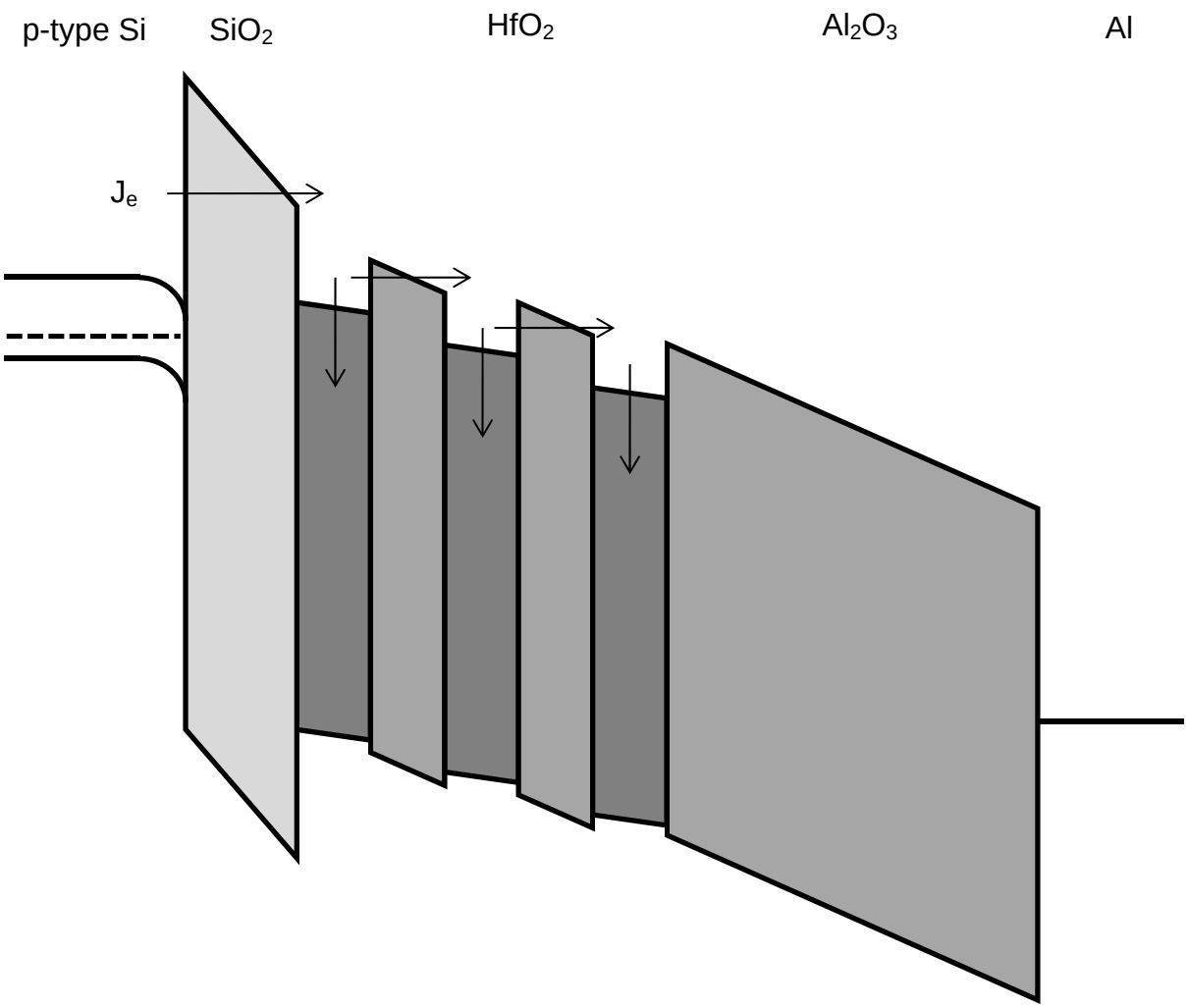


Figure R4.26 The band diagram of as-deposited $Al/Al_2O_3/[Al_2O_3/HfO_2]_2/HfO_2/SiO_2$/p-type Si capacitor structure under the positive V_G of 6 V.

Chapter 5

Charge Trapping in Capacitor Structures with Annealed High-κ Dielectric Materials as Charge Trapping Layers

The amorphous high-κ dielectric materials which are used as charge trapping layer (CTL) and blocking oxide (BO) in the MAHOS capacitor structures turn into crystalline phase after rapid thermal annealing (RTA). In this chapter, the charge trapping characteristics in annealed MAHOS structures are observed by LCR meter. Their leakage current densities are measured by semiconductor analyzer system. The mechanism of charge trapping is explained by considering the energy band structures of MAHOS capacitors which is studied previously. The neutral flatband voltage of samples is determined and its shift is also discussed.

5.1 Introduction

Device fabrication conditions, such as deposition methods, precursor for deposition, and annealing condition influence the atomic and electronic structures of the gate stack.[1] After annealing at high temperature, amorphous high-κ dielectric materials in memory structures will transform into crystalline phase which contains and generates defects, including step edges and dislocations. These defects induce discrete electronic states in the band gap that can be filled with electrons. The dimensionality and position of the defects affect their trapping capacity.[2] Line defects and grain boundaries are the dominant trapping centers in real oxide. On the other hand, point defects play only a minor role as electron traps due to their small abundance and low storage capacity. The large potential of extended defects to trap electrons has been demonstrated in a recent theoretical work by Shluger et al.[3] The study on energy spatial distribution of electron traps throughout the stack of SiO_2/high-κ dielectric revealed that the postdeposition annealing in N_2 has different impacts

on the electron traps in different energy regions.[4]

For the application of non-volatile memory, the structure is patterned and source and drain are implanted on silicon substrate. Source and drain have to be activated at high temperature of about 1000^{o}C. Therefore, understanding the charge trapping characteristics of annealed MAHOS structures is important.

5.2 Measurement Methods

Similar with the measurement methods in the previous chapter, the charge trapping characteristics is observed from the flatband voltage shift measured by carrying out the high frequency (1 MHz) capacitance – voltage (C – V) measurement using LCR meter, Agilent 4284 A. The surface carrier concentration which is calculated in the previous chapter is used to measure the flatband capacitance since the same p-type Si substrate is used. To analyze charge trapping characteristics, the sweeping gate voltage from inversion, with the voltage of 2 V – 15 V, to accumulation, with the voltage of -2 V, is applied in order to trap electrons for programming purpose. Then, the sweeping gate voltage from accumulation, with the voltage of -2 V – -15 V, to inversion, with the voltage of 3 V, is applied in order to remove the electrons from charge trapping layer and inject holes from silicon substrate into CTL for erasing purpose. The flatband voltage shifts are determined and are plotted as a function of the positive and negative gate voltage.

To understand charge transport mechanism in annealed MAHOS structures, current-voltage (I-V) measurements were carried out. Leakage current density as a function of sweep voltage is observed by HP4156C semiconductor analyzer system by applying a sweep voltage with a fixed voltage step of 0.1 V and a step delay time to the device. The leakage current density under positive sweep voltage from 0 – 35 V and under negative stress voltage from 0 – -35 V is investigated.

5.3 Neutral Flatband Voltage in Annealed MAHOS Capacitor Structures

Flatband voltage is calculated by applying "calculation C_{FB} method" explained in the previous chapter in which the experimental $C(V_G)$ characteristic measured on MOS structure and the value of the C_{FB} capacitance is obtained and the V_{FB} value is given by the corresponding value of the gate voltage V_G for C_{FB} capacitance.

The qV_{nfb}, the binding energy of Al $2p_{3/2}$ of Al_2O_3 blocking oxide, and the distance between the binding energy of Al $2p_{3/2}$ and the qV_{nfb} of annealed MAHOS structures are shown in Table 5.2. qV_{nfb} is defined as the amount of energy gained by the charge of a single electron which move across an electric potential difference of V_{nfb}. In annealed MAHOS structures, the distance between the binding energy of Al $2p_{3/2}$ and the qV_{nfb} is similar for all structures which is 72.99 ± 0.08 eV. In this case, the data of sample NB2 is ignored since the sample is probably damaged as also indicated by the charge trapping characteristic results.

If only the work function difference between metal and semiconductor is consider, the neutral flatband voltage will be negative since aluminum has smaller work function than that of silicon. However, after annealing, the V_{nfb} shifts to the positive side for all samples which is different in case of the V_{nfb} of as-deposited samples which have negative V_{nfb}. After annealing, the dipole relaxation occurs in the interface of high-κ dielectrics and line

Table 5.1 The neutral flatband voltage (qV_{nfb}) of the MAHOS structure and the core level of Al $2p_{3/2}$ of Al_2O_3 blocking oxide in the MAHOS structure.

Sample	qV_{nfb} (eV)	CL Al $2p_{3/2}$ (eV)	CL Al $2p_{3/2}$ – qV_{nfb} (eV)
A2	0.7219	73.777	73.0555
HA2	0.7805	73.848	73.0675
NA2	0.887	73.800	72.913
NB2	0.1379	73.807	73.6691

defects such as grain boundary is formed in the crystalline high-κ films. The defects in the crystalline high-κ structures affect the V_{nfb} of annealed MAHOS structures.

5.4 Charge Trapping in Annealed MAHOS Capacitor Structures

The charge trapping characteristics in annealed MAHOS capacitor sructures was studied by carrying out the high frequency C – V measurements. The C – V characteristics of annealed $Al/Al_2O_3/SiO_2$/p-type Si structure (sample A2), annealed $Al/Al_2O_3/HfAlO/SiO_2$/ p-type Si structure (sample HA2), and $Al/Al_2O_3/[HfO_2/Al_2O_3]_2/HfO_2/SiO_2$/p-type Si structure (sample NB1) under sweep gate voltage from inversion to accumulation are shown in Figure R5.1, Figure R5.4, and Figure R5.7, respectively, while their C – V characteristics under sweep gate voltage from accumulation to inversion are shown in Figure R5.2, Figure R5.5, and Figure R5.8, respectively. The flatband voltage as a function of sweep gate voltage of sample A2, sample HA2, and sample NA2 are shown in Figure R5.3, Figure R5.6, and Figure R5.9, respectively.

Positive ΔV_{FB} indicates electron trapping in the CTL of MAHOS structures which is expected for programming of non-volatile memory. The V_{FB} of sample A2, HA2, and NA2 initiate to shift to positive value after applying the V_G of 5 V with the ΔV_{FB} of 0.28 V, 0.49 V, and 0.58 V, respectively. The V_{FB} of sample A2, HA2, and NA2 increases significantly from the VG of 5 V up to 7 V for sample A2 and up to 9 V for sample HA2 and NA2. The ΔV_{FB} of sample A2, HA2, and NA2 after applying the V_G of 15 V are 1.89 V, 3.71 V, and 3.78 V, respectively. Under sweep gate voltage from accumulation to inversion, V_{FB} decreases. ΔV_{FB} decreases from the initial ΔV_{FB} of 1.73 V to -4.3 V, 3.68 V to -3.79 V, and 3.68 V to -4.03 V for sample A2, HA2, and NA2, respectively, under the V_G of -14 V. Sample A2, HA2, and NA2 can be completely erased when ΔV_{FB} becomes zero after applying the gate voltage of -9.6 V, -10.4 V, and -10.2 V. Erase mechanism is by detrapping of electrons from CTL to Si

substrate and hole injection from Si substrate to CTL. In case of as-deposited MAHOS structures, detrapping of electrons and injection of holes can be distinguished from two different slopes in ΔV_{FB} as a function of V_G. For annealed MAHOS structures, it is difficult to distinguish between detrapping of electrons and injection of holes from the slope in in ΔV_{FB} as a function of V_G even though initially the small decrease of ΔV_{FB} is observed under small V_G.

In case of sample NB2, it is expected that the sample also traps electrons under the positive V_G with large ΔV_{FB} and traps holes under the negative V_G with large ΔV_{FB}. The C – V characteristics of sample NB2 under sweep gate voltage from inversion to accumulation and under sweep gate voltage from accumulation to inversion are shown in Figure R5.10 and Figure R5.11, respectively. Its flatband voltage as a function of sweep gate voltage is shown in Figure R5.12. Very small increase of ΔV_{FB} is observed under the positive V_G which occurs in two steps from 0 V to 0.07 V after applying the positive V_G of 4 V and from 0.07 V to 0.22 V after applying the positive V_G of 10 V. Under the positive V_G of 5 V to 8 V, there is no increase in ΔV_{FB}. The two steps of ΔV_{FB} increase indicates two HfO_2 layers which is separated by AlHfO layer. Under the negative V_G, ΔV_{FB} starts to decrease from 0.22 V to 0.20 V under the the V_G of -7 V. ΔV_{FB} decreases to 0.17 V under the the V_G of -8 V. There is no decrease in ΔV_{FB} under higher negative V_G than -8 V. This result seems to be anomalous since HfAlO is capable to traps electrons.

To compare the value of ΔV_{FB} in each sample, flatband voltage as a function of gate voltage of sample A2, HA2, and NA2 under sweeping voltage from inversion to accumulation is shown in Figure R5.13. By considering only these three samples, it is observed that the ΔV_{FB} of sample A2 < ΔV_{FB} of sample HA2 < ΔV_{FB} of sample NA2. These results show that the annealed MAHOS structures with HfO_2/HfAlO/HfO_2 nanolaminates as CTL trap more electrons than the structures with Al_2O_3 and HfAlO single layer as CTL. The

structure with HfAlO as CTL traps more electrons compared to the structure with Al_2O_3 as CTL since it is a mixture with HfO_2 which provides more trap sites.

Flatband voltage as a function of gate voltage of sample A2, HA2, and NA2 under sweeping voltage from accumulation to inversion is shown in Figure R5.14. In case of hole trapping into CTL of MAHOS structures, it is observed that under the V_G of -15 V, the $-\Delta V_{FB}$ of sample A2 < $-\Delta V_{FB}$ of sample HA12 < $-\Delta V_{FB}$ of sample NA2 which show that the MAHOS structures with HfO_2/HfAlO/HfO_2 nanolaminates as CTL trap more holes than the structures with Al_2O_3 and HfAlO single layer as CTL.

In annealed MAHOS structures, including in sample A2, HA2, and NA2, more charges can be trapped in the CTL than that in as deposited MAHOS structures. Postdeposition annealing (PDA) at different temperatures changes the microstructure of high-κ layers significantly which affect the properties of electron traps.[5] In annealed MAHOS structures, line defects and grain boundaries are the dominant trapping centers, while in as-deposited MAHOS structures point defects are the sites for charge traps.

5.5 Leakage Current Density in Annealed MAHOS Capacitor Structures

The leakage current measurement provides information on how charges transport in annealed capacitor structures. The measurement is conducted by measuring the leakage current density under the positive sweep voltage from 0 V – 35 V on one device and measuring the leakage current density under the negative gate voltage from 0 V – -35 V on different device. The leakage current density as a function of sweep voltage of sample A2, HA2, NA2, and NB2 are shown in Figure R4.15 – R4.18, respectively. From the results it can be observed that electron injection occurs when the V_G is ≥ 5 V. For sample A2, between the V_G of 5 V – 9 V, tunneling mechanism is based on F – N tunneling. For sample HA2, NA2,

and NB2, different mechanisms of tunneling also occur. Hole injection can be observed at the V_G of about 11 V, when holes tunnel through SiO_2 by F – N tunneling mechanism.

At large electric field, a significant electrons or holes tunnel through SiO_2 layer. SiO_2 has good thermal stability and its phase remains amorphous. Therefore, the common mechanism tunneling through thin SiO_2 layer is F – N tunneling where charges tunnel through triangular barrier at high electric fields. The experimental J-E curves were fitted by F – N tunneling model. The plot of $\ln J/E_{ox}^2$ vs $1/E_{ox}$ of sample A2, HA2, NA2, and NB2 under the positive sweep voltage and the negative sweep voltage are shown in the Figure R5.19 – R5.22. Under the positive sweep voltage, the plot of $\ln J/E_{ox}^2$ vs $1/E_{ox}$ of sample HA2, NA2, and NB2 do not fit the F – N tunneling model. Since the the charge trapping layer and blocking oxide of annealed MAHOS structures are crystalline, the charge trapped in the grain boundary may leak to the metal gate by charge transport via grain boundary. Based on the study of the surface of HfO_2 layer by conductive atomic force microscopy (CAFM), it was revealed that HfO_2 with polycrystalline structure has deeper paths that correspond to the grain boundaries, which is typical for HfO_2 samples annealed at high temperatures.[6] In HfO_2 films, the charge transport occurs primarily through the grain boundaries.[7] The study on the leakage current through the poly-crystalline HfO_2 found that grain boundaries have higher density of defects than grains.[8]

5.6 Summary

The charge trapping characteristics in annealed MAHOS capacitor structures has been observed by measuring the ΔV_{FB} in the structures from high frequency (1 MHz) C – V characteristics. The neutral flatband voltage in annealed MAHOS capacitor structures is discussed. The mechanism of charge transport is explained by analyzing the leakage current density as a function of sweep voltage measured by semiconductor analyzer system.

Based on the discussion in this chapter, some important points can be summarized,

1. The neutral flatband voltage in the annealed MAHOS structures strongly affected by the electronic defects in the crystalline high-κ dielectric materials. The work function difference between aluminum and silicon substrate contributes to the negative value in determining V_{FB}. However, it is found that all annealed samples have positive V_{FB}.
2. Annealed MAHOS capacitor structures with heterostructure of HfO_2/HfAlO/HfO_2 trap more charges than the structure with Al_2O_3 and HfAlO as CTL. In general, annealed MAHOS capacitor structures trap more charges than the as-deposited structure since defects such as grain boundaries induce discrete electronic states in the band gap that can be filled with charges.
3. The charge transport mechanism from Si substrate through SiO_2 tunneling layer is F – N tunneling mechanism. However, charges that trapped in the defects in polycristalline high-κ may leak through defects to the metal gate.

References

[1] D. Misra and N. A. Chowdhury. Charge Trapping in High-κ Gate Dielectrics: A Recent Understanding. ECS Transactions, 2 (1) 311-328 (2006).

[2] B. Govoreanu, D.Wellekens, L. Haspeslagh, J. De Vos, and J. Van Houdt. Investigation of the low-field leakage through high-κ interpoly dielectric stacks and its impact on nonvolatile memory data retention. IEDM Tech. Dig., 2006, pp. 206–209.

[3] K. P. McKenna and A. L. Shluger. Electron-trapping polycrystalline materials with negative electron affinity. Nature Mater. 7, 859 (2008).

[4] Xue Feng Zheng, Wei Dong Zhang, Bogdan Govoreanu, Daniel Ruiz Aguado, Jian Fu Zhang, and Jan Van Houdt. Energy and Spatial Distributions of Electron Traps Throughout SiO2/Al2O3 Stacks as the IPD in Flash Memory Application. IEEE

Transactions on Electron Devices, vol. 57, No. 1, January 2010.

[6] V. Iglesias, M. Porti, M. Nafría, X. Aymerich, P. Dudek, T. Schroeder, and G. Bersuker. Correlation between the nanoscale electrical and morphological properties of crystallized hafnium oxide-based metal oxide semiconductor structures. Appl. Phys. Lett. 97, 262906 (2010).

[7] V. Iglesias, M. Porti, M. Nafria, X. Aymerich, P. Dudek, and G. Bersuker. Dielectric breakdown in polycrystalline hafnium oxide gate dielectrics investigated by conductive atomic force microscopy. J. Vac. Sci. Technol. B 29, 01AB02 (2011).

[8] Onofrio Pirrotta, Luca Larcher, Mario Lanza, Andrea Padovani, Marc Porti, Montserrat Nafría, and Gennadi Bersuker. Leakage current through the poly-crystalline HfO2: Trap densities at grains and grain boundaries. Journal of Applied Physics 114, 134503 (2013).

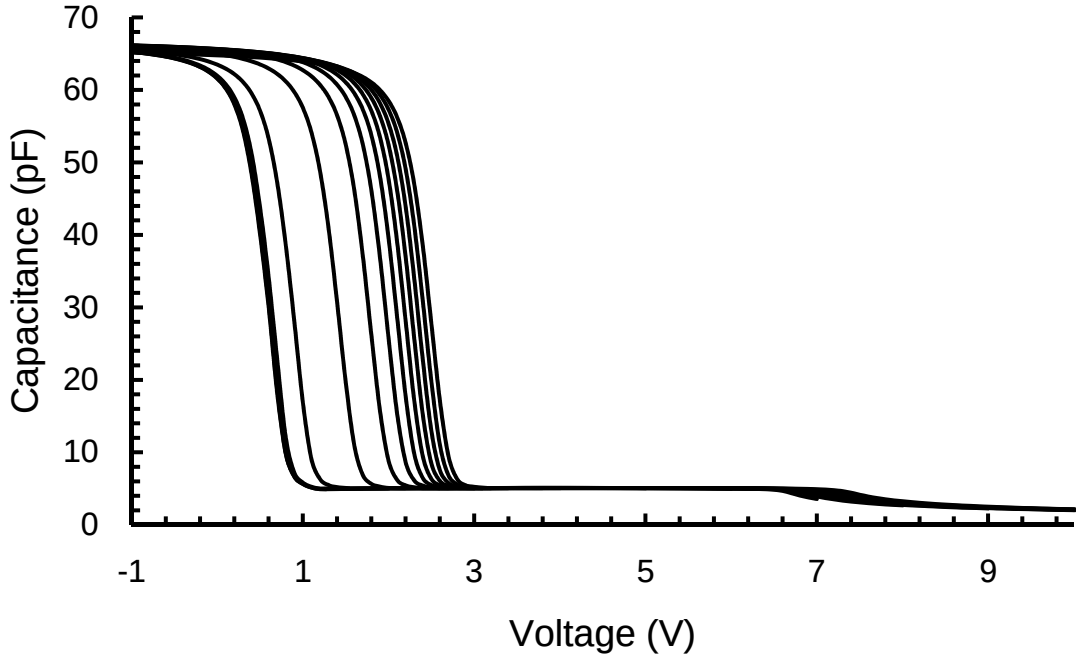


Figure R5.1 High frequency (1 MHz) C – V characteristics of annealed $Al/Al_2O_3/SiO_2/$ p-type Si capacitor structure under sweep gate voltage from inversion to accumulation.

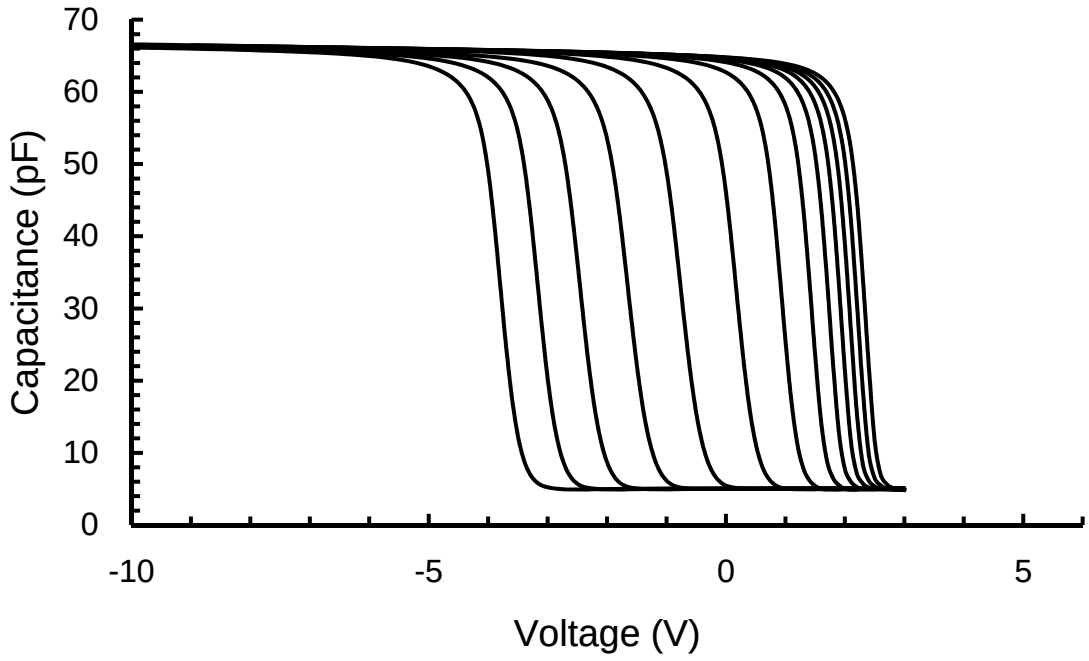


Figure R5.2 High frequency (1 MHz) C – V characteristics of annealed $Al/Al_2O_3/SiO_2/$ p-type Si capacitor structure under sweep gate voltage from accumulation to inversion.

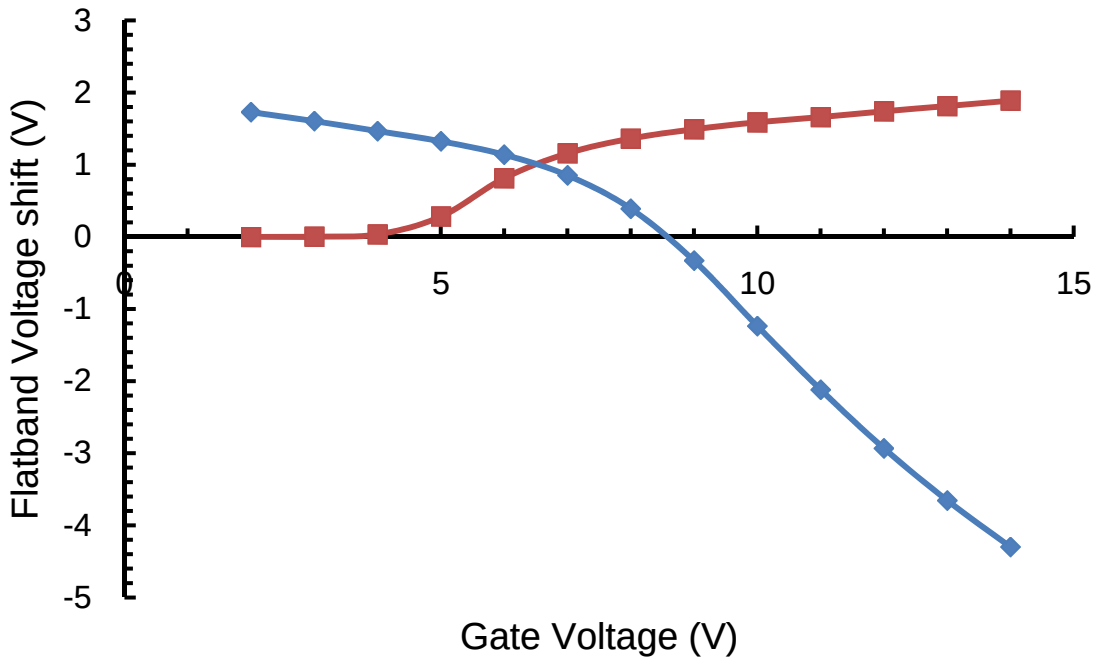


Figure R5.3 Flatband voltage as a function of sweep gate voltage of annealed $Al/Al_2O_3/SiO_2$/p-type Si capacitor structure.

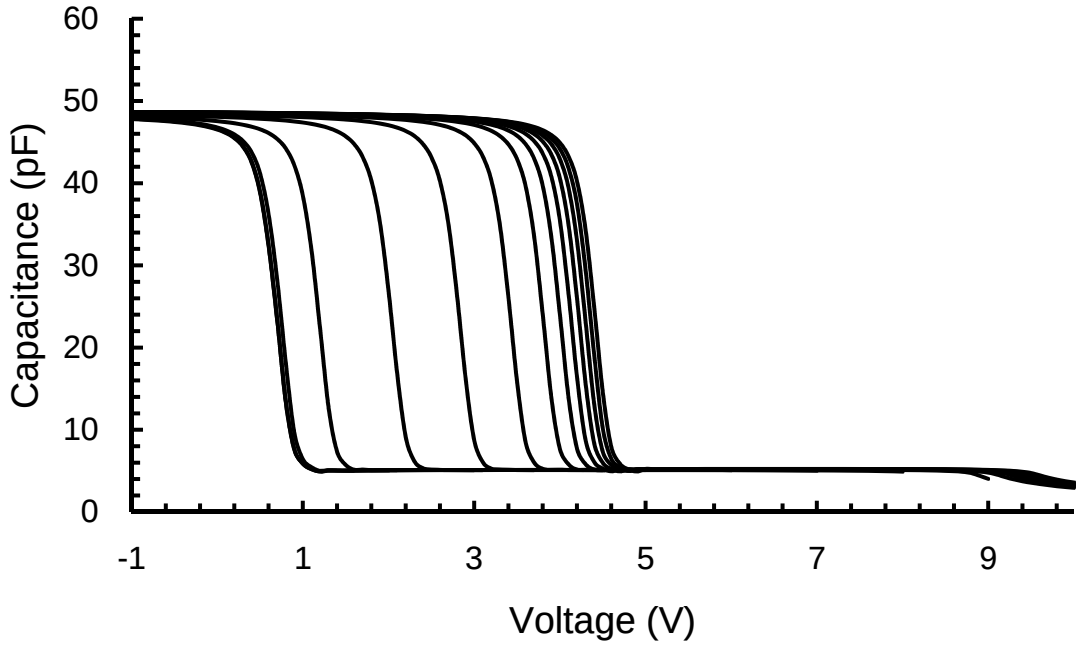


Figure R5.4 High frequency C – V characteristics of annealed $Al_2O_3/HfAlO/SiO_2$/p-type Si under sweep gate voltage from inversion to accumulation.

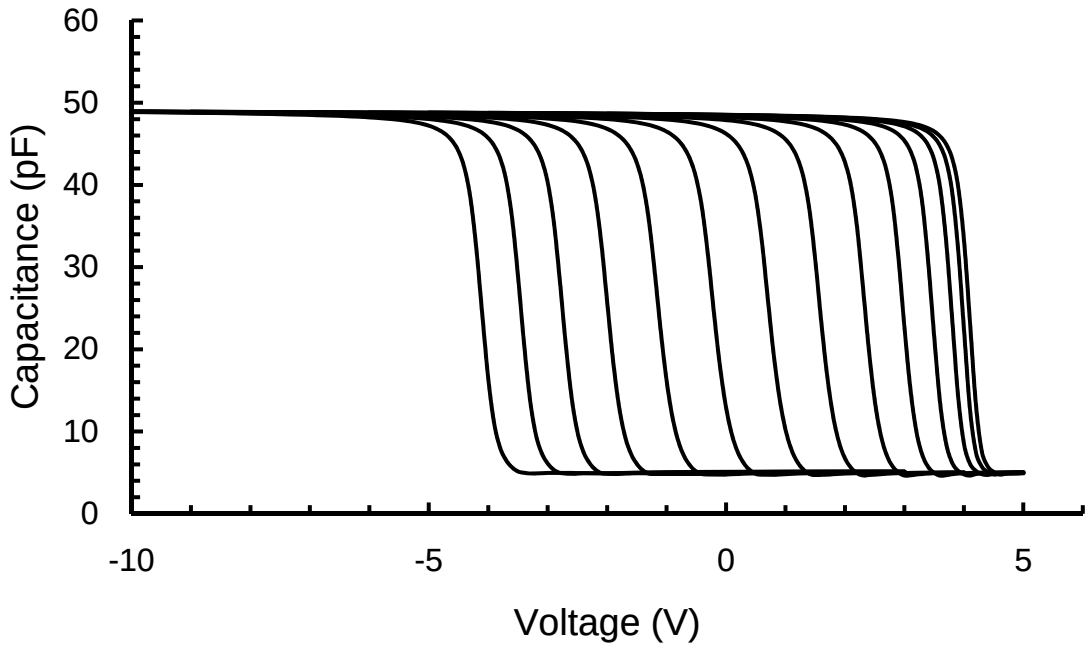


Figure R5.5 High frequency C – V characteristics of annealed Al_2O_3/HfAlO/SiO_2/p-type Si under sweep gate voltage from inversion to accumulation.

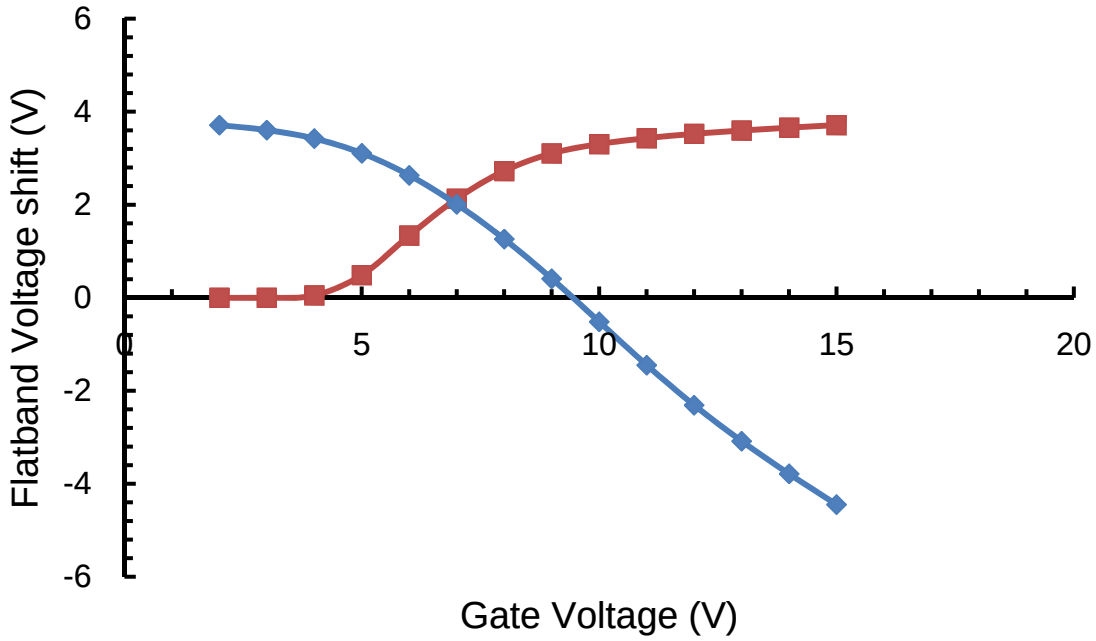


Figure R5.6 Flatband voltage as a function of sweep gate voltage of annealed Al_2O_3/HfAlO/SiO_2/p-type Si capacitor structure.

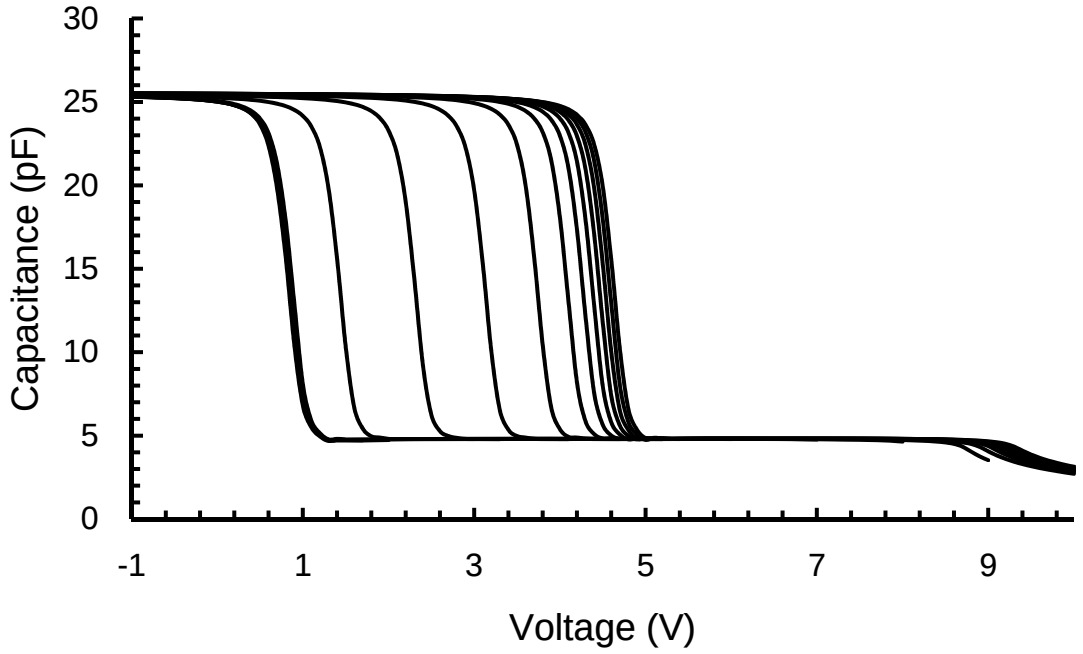


Figure R5.7 High frequency C – V characteristics of annealed Al/Al_2O_3/[HfO_2/ Al_2O_3]$_4$/HfO_2/SiO_2/p-type Si under sweep gate voltage from inversion to accumulation.

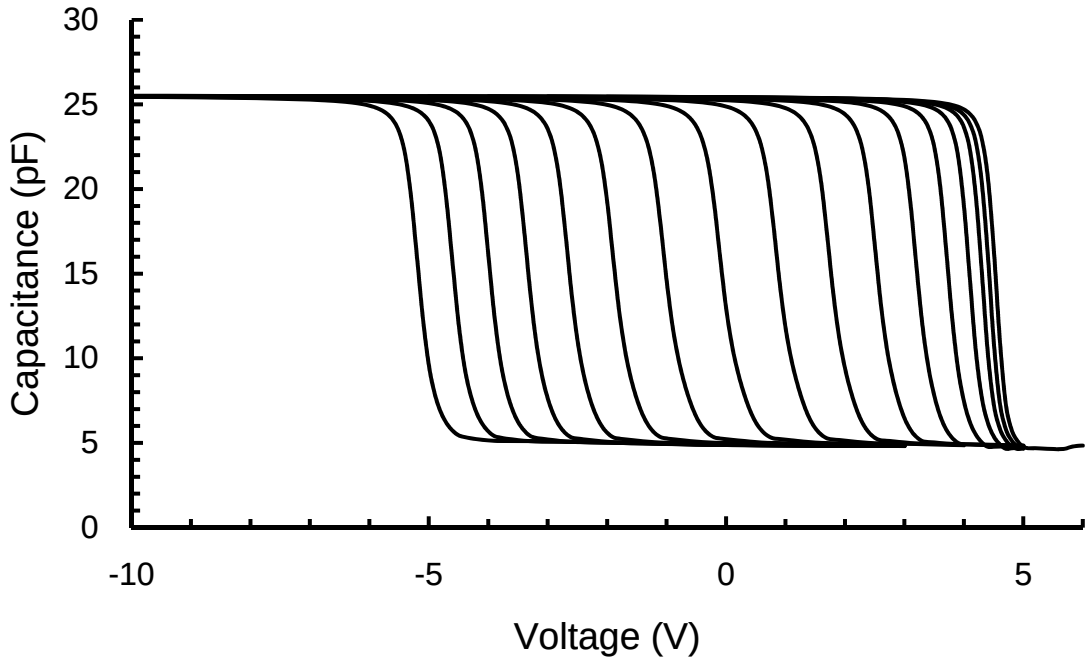


Figure R5.8 High frequency C – V characteristics of annealed Al/Al_2O_3/[HfO_2/ Al_2O_3]$_4$/HfO_2/SiO_2/p-type Si under sweep gate voltage from inversion to accumulation.

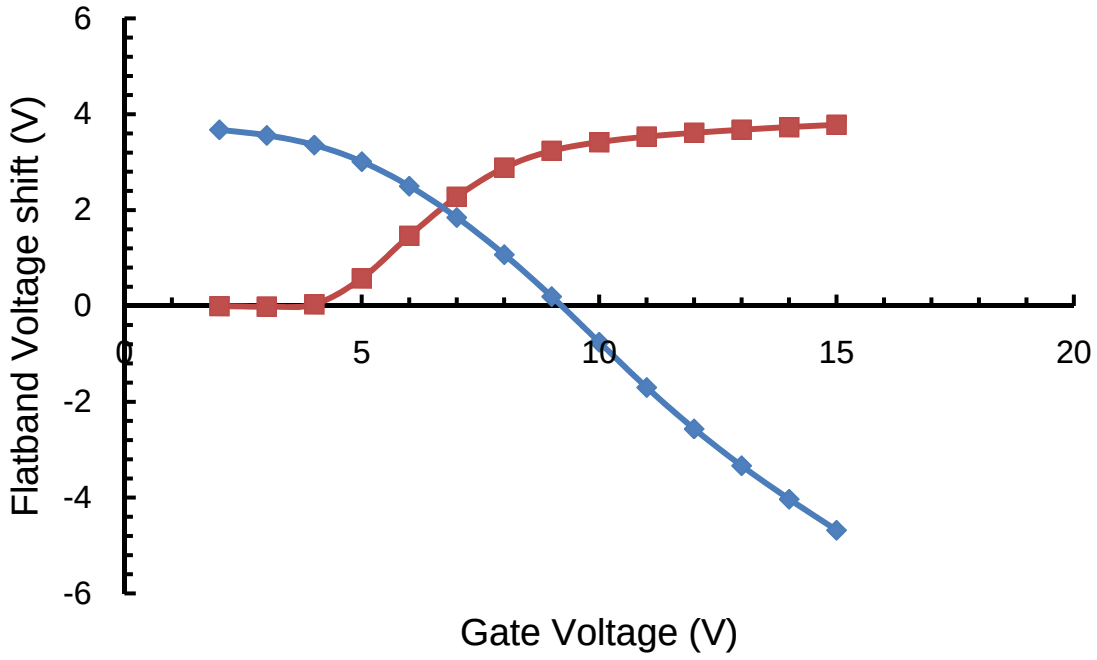


Figure R5.9 Flatband voltage as a function of sweep gate voltage of annealed $Al/Al_2O_3/[HfO_2/Al_2O_3]_4/HfO_2/SiO_2$/p-type Si capacitor structure.

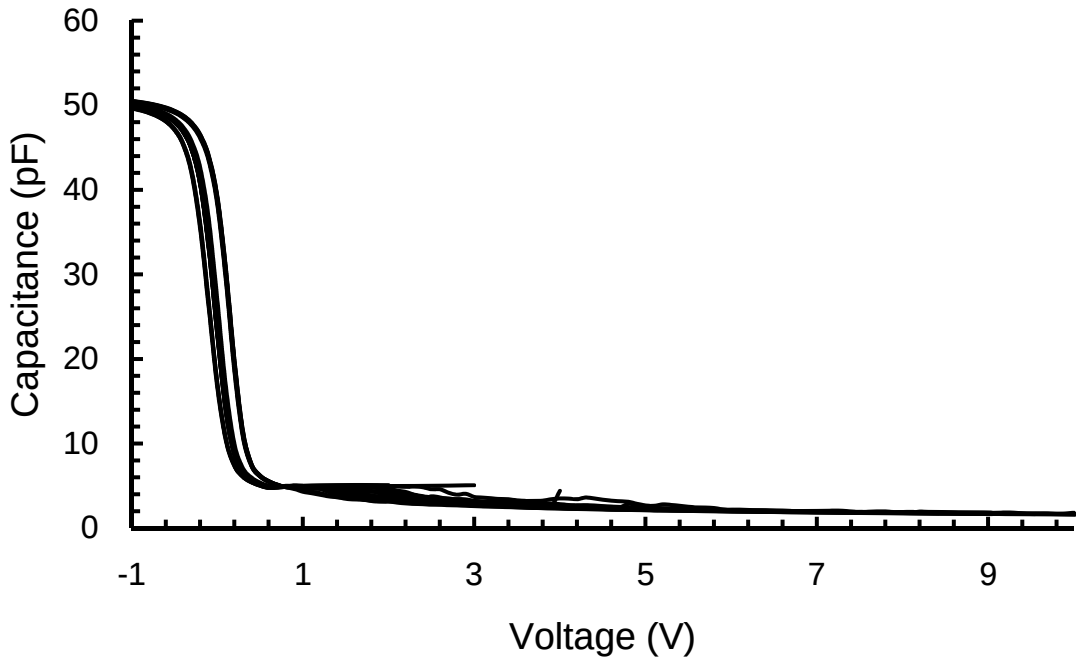


Figure R5.10 High frequency C – V characteristics of annealed $Al/Al_2O_3/[HfO_2/Al_2O_3]_2/HfO_2/SiO_2$/p-type Si under sweep gate voltage from inversion to accumulation.

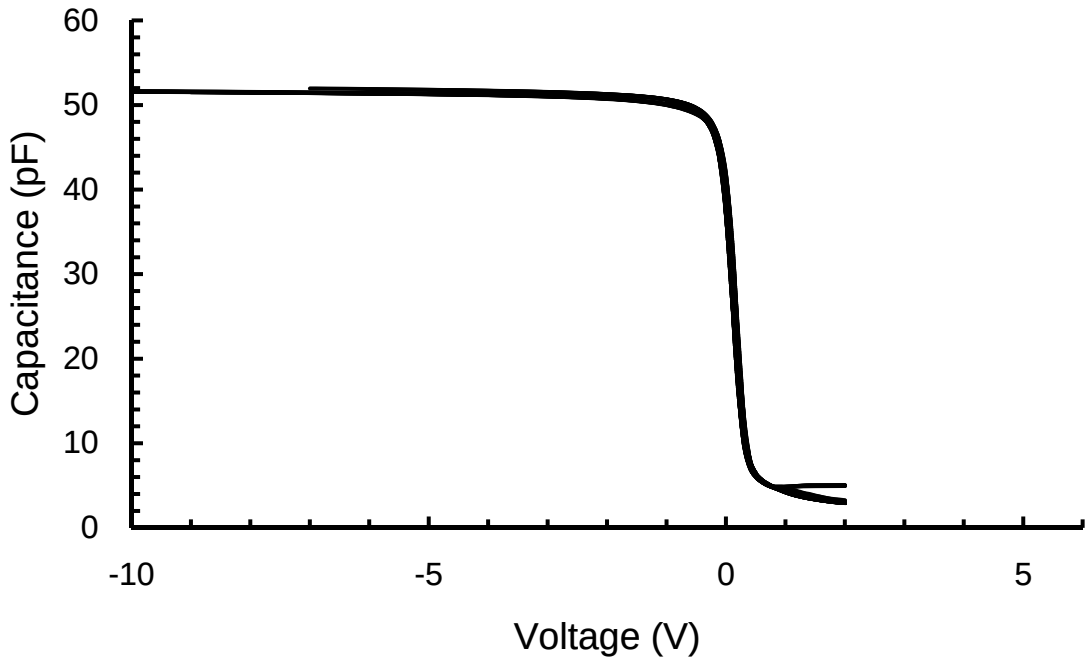


Figure R5.11 High frequency C – V characteristics of annealed Al/Al_2O_3/[HfO_2/ Al_2O_3]$_2$/HfO_2/SiO_2/p-type Si under sweep gate voltage from accumulation to inversion.

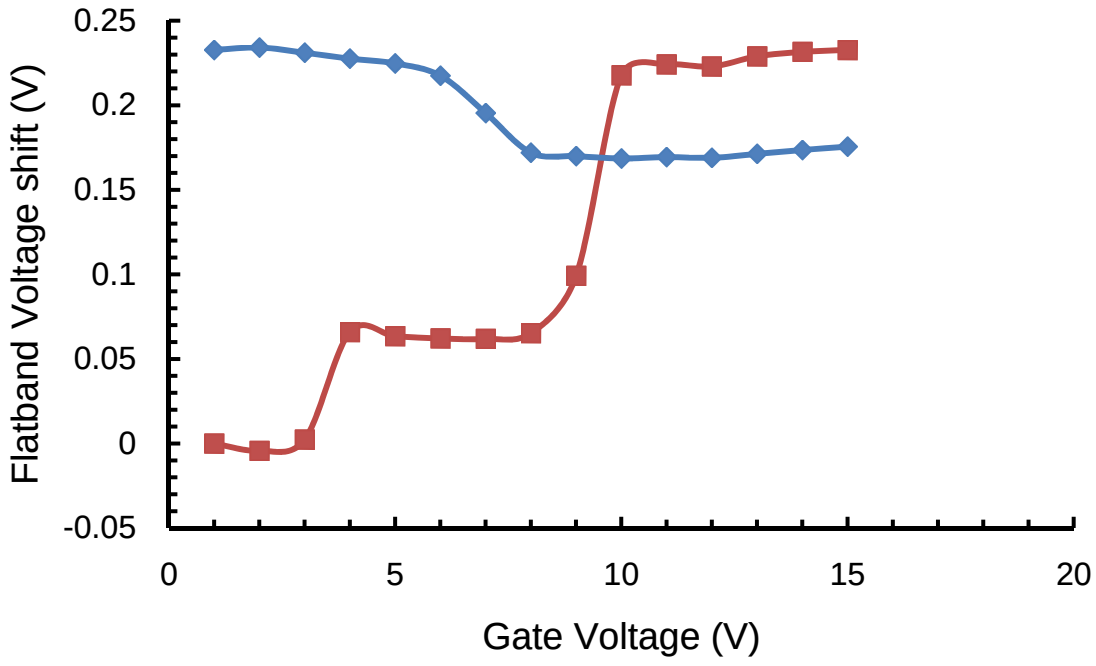


Figure R5.12 Flatband voltage as a function of sweep gate voltage of annealed Al/Al_2O_3/[HfO_2/Al_2O_3]$_2$/HfO_2/SiO_2/p-type Si capacitor structure.

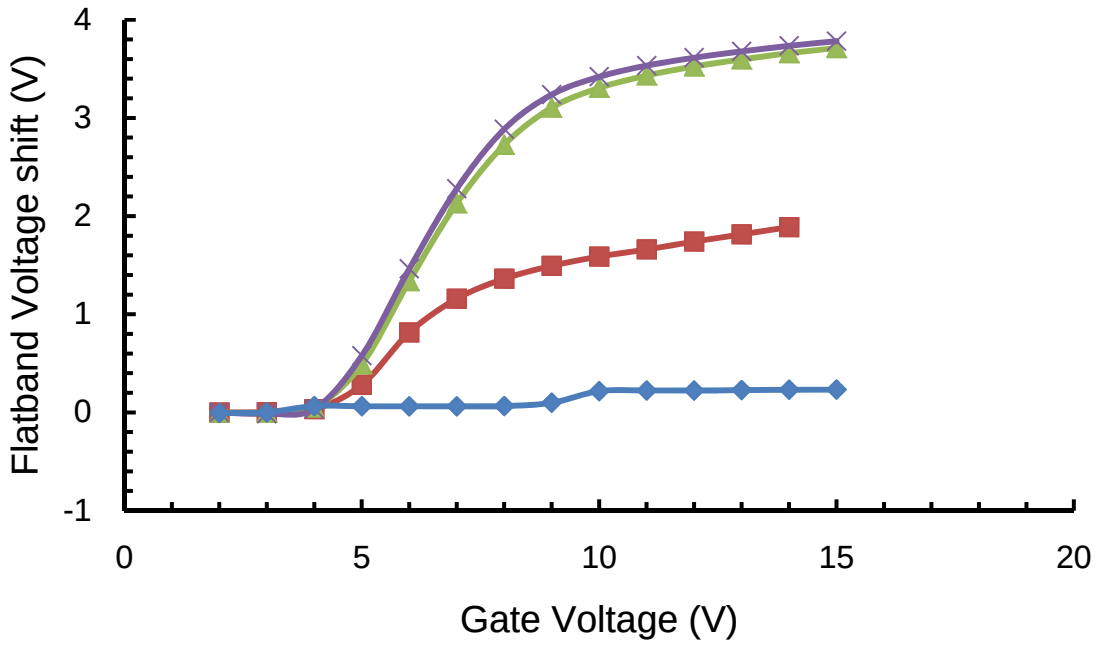


Figure R5.13 Flatband voltage as a function of sweep gate voltage of sample A2, HA2, NA2, and NB2 under sweeping voltage from inversion to accumulation.

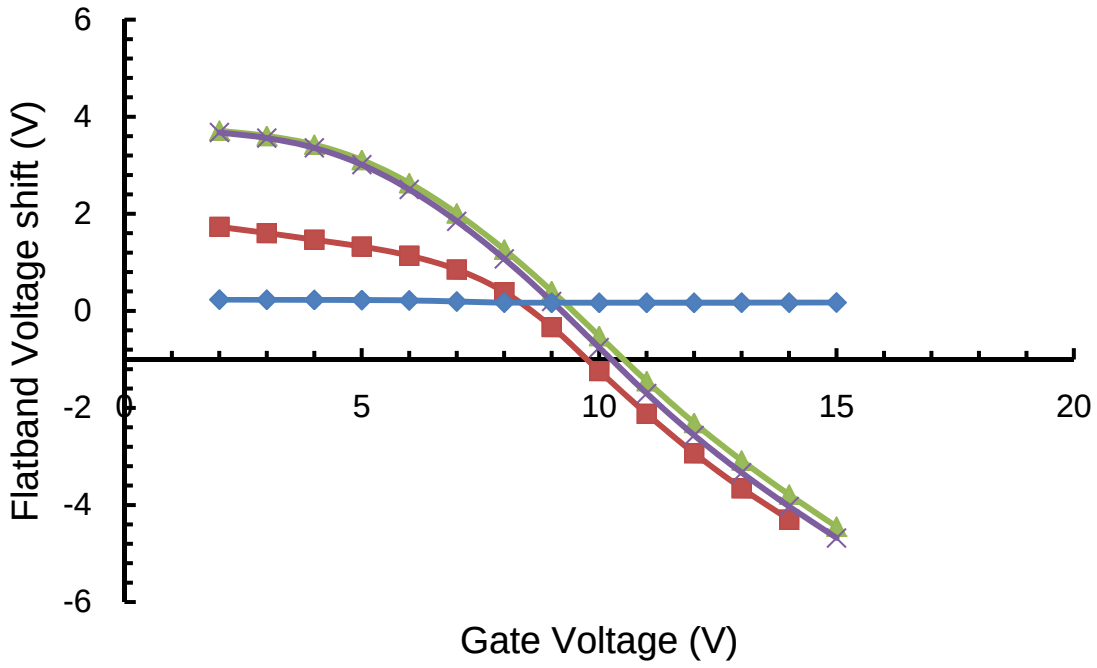


Figure R5.14 Flatband voltage as a function of sweep gate voltage of sample A1, HA1, NA1, and NB1 under sweeping voltage from accumulation to inversion.

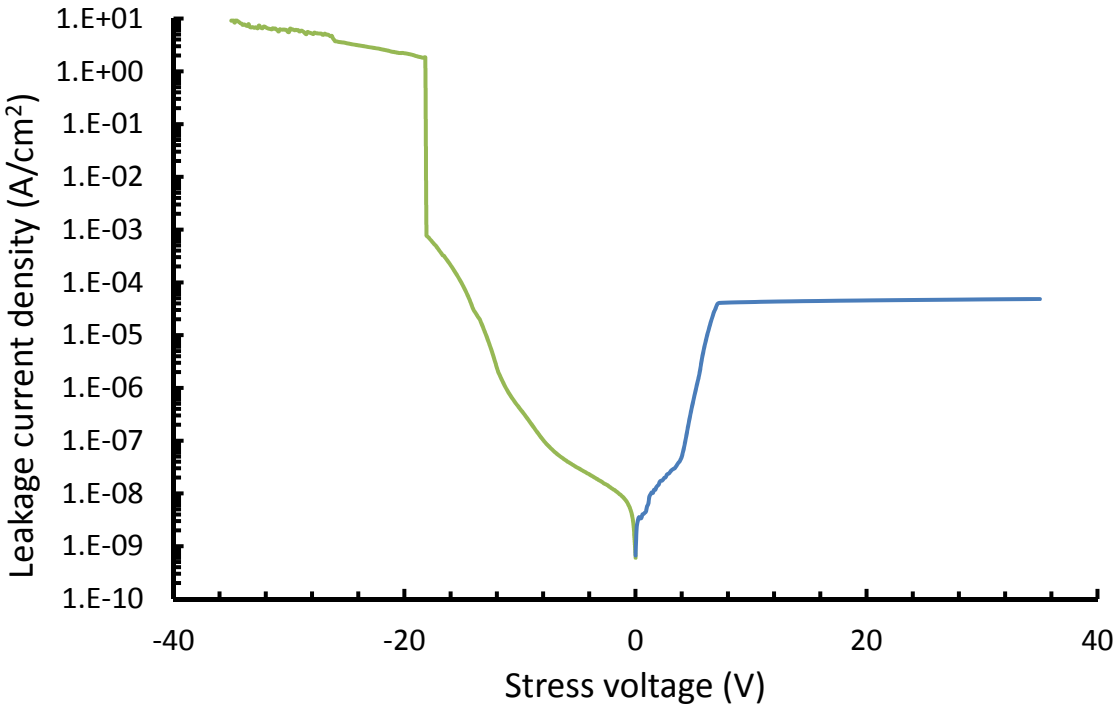


Figure R5.15 Leakage current density as a function of sweep voltage annealed $Al/Al_2O_3/SiO_2/$ p-type Si capacitor structure.

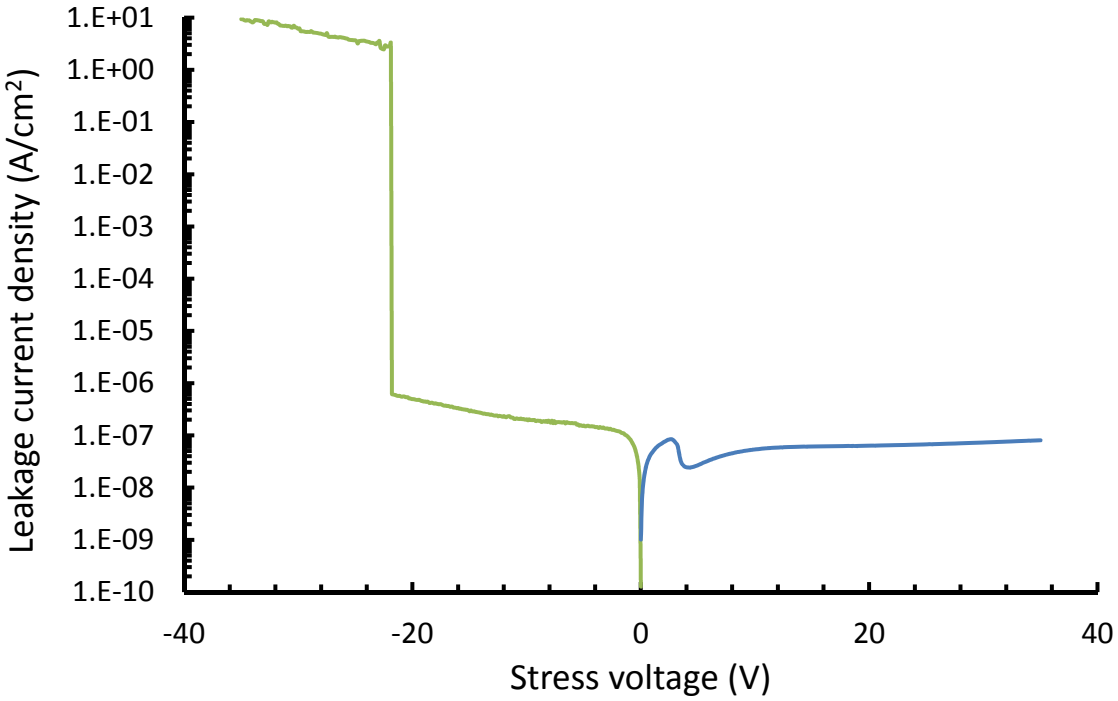


Figure R5.16 Leakage current density as a function of sweep voltage annealed $Al_2O_3/HfAlO/SiO_2$/p-type Si capacitor structure.

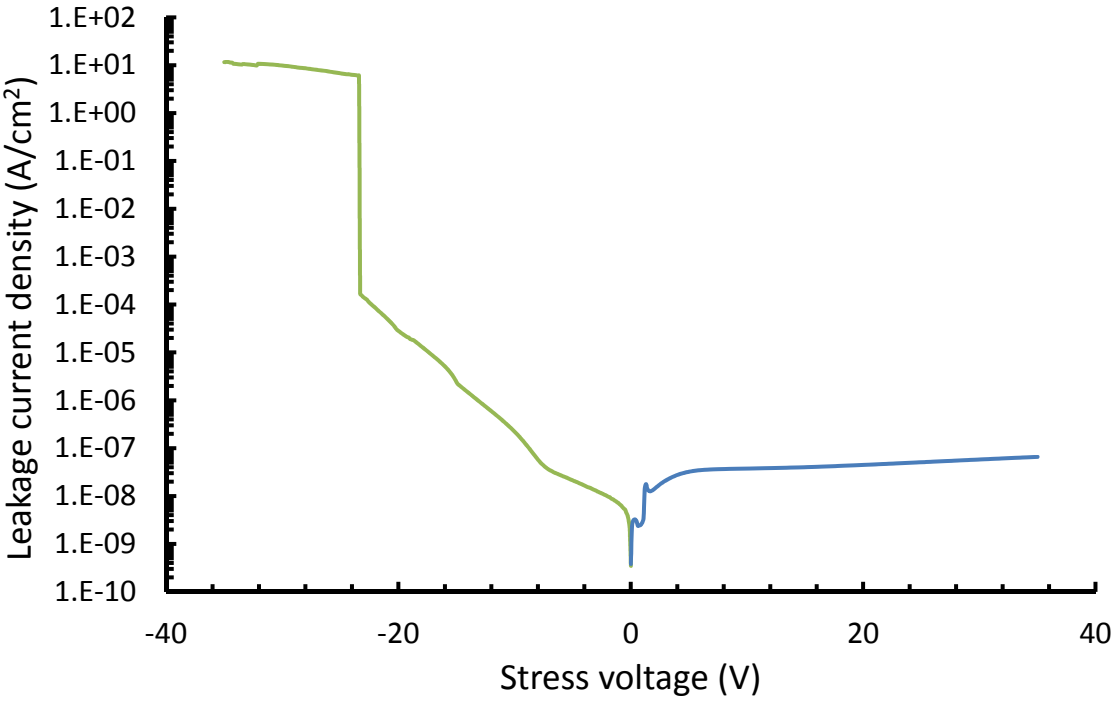


Figure R5.17 Leakage current density as a function of sweep voltage annealed $Al/Al_2O_3/[HfO_2/Al_2O_3]_4/HfO_2/SiO_2$/p-type Si capacitor structure.

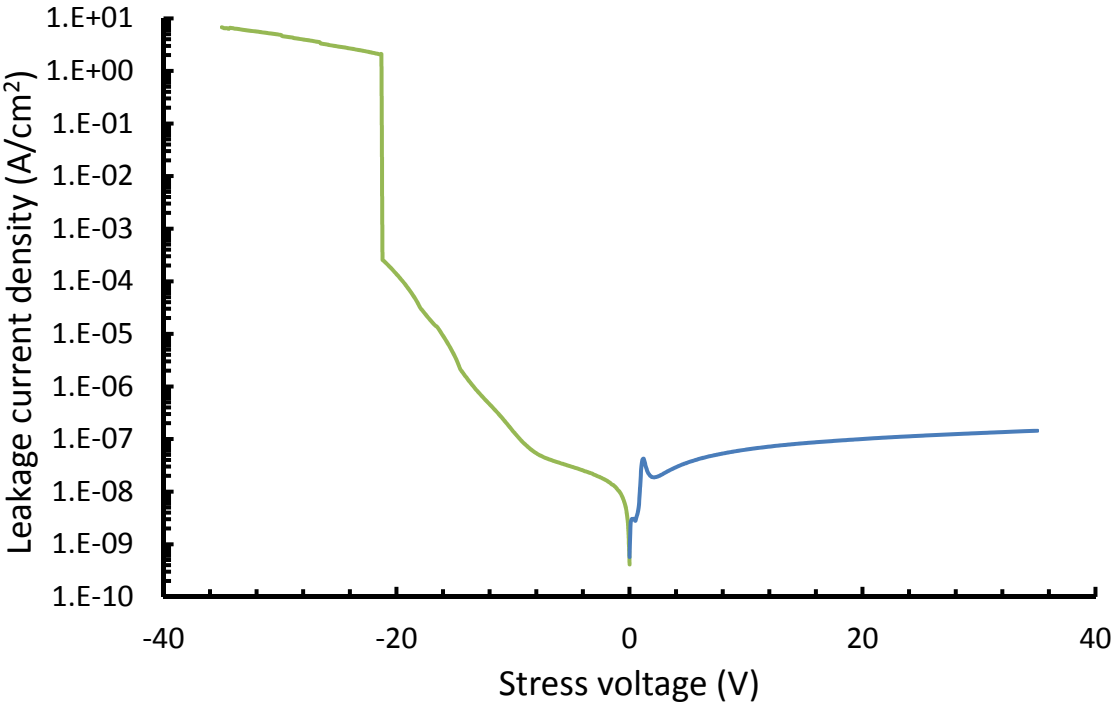


Figure R5.18 Leakage current density as a function of sweep voltage annealed $Al/Al_2O_3/[HfO_2/Al_2O_3]_2/HfO_2/SiO_2$/p-type Si capacitor structure.

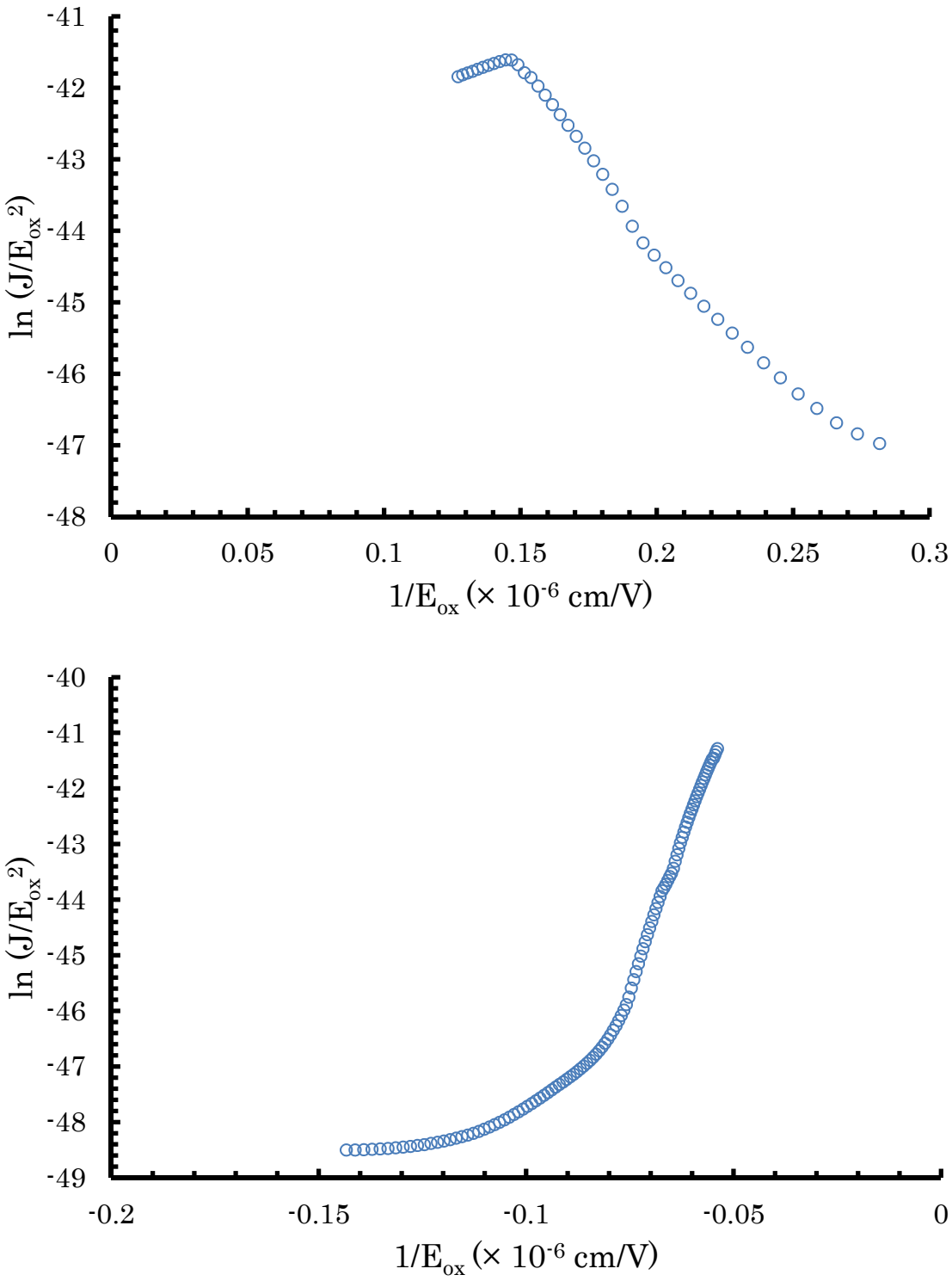


Figure R4.19 $\ln J/E_{ox}^2$ vs $1/E_{ox}$ of annealed $Al/Al_2O_3/SiO_2$/p-type Si capacitor structure under the positive sweep voltage (top) and the negative sweep voltage (bottom).

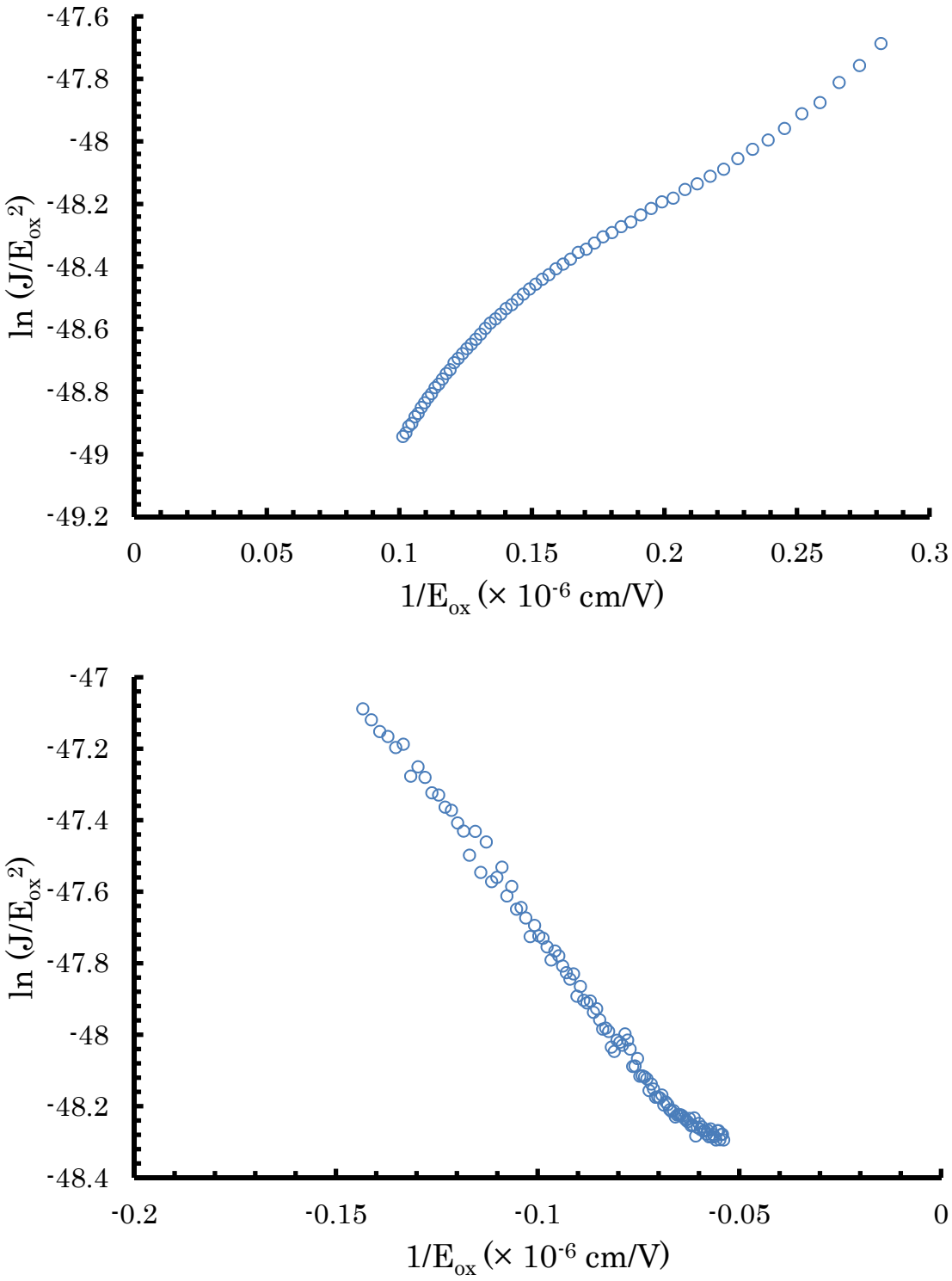


Figure R4.20 $\ln J/E_{ox}^2$ vs $1/E_{ox}$ of annealed $Al/Al_2O_3/HfAlO/SiO_2$/p-type Si capacitor structure under the positive sweep voltage (top) and the negative sweep voltage (bottom).

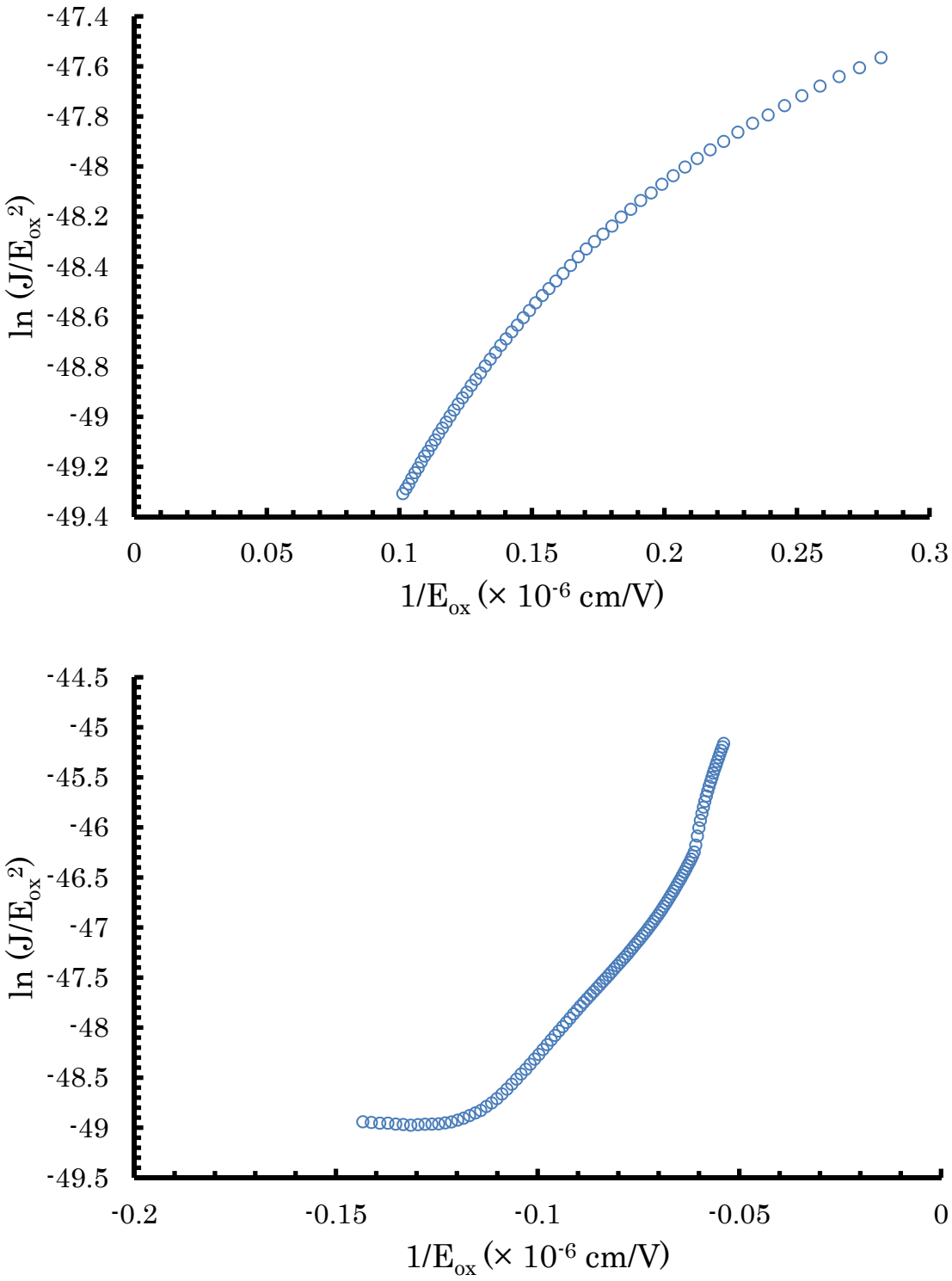


Figure R4.21 $\ln J/E_{ox}^2$ vs $1/E_{ox}$ of annealed $Al/Al_2O_3/[HfO_2/Al_2O_3]_4/HfO_2/SiO_2$ /p-type Si capacitor structure under the positive sweep voltage (top) and the negative sweep voltage (bottom).

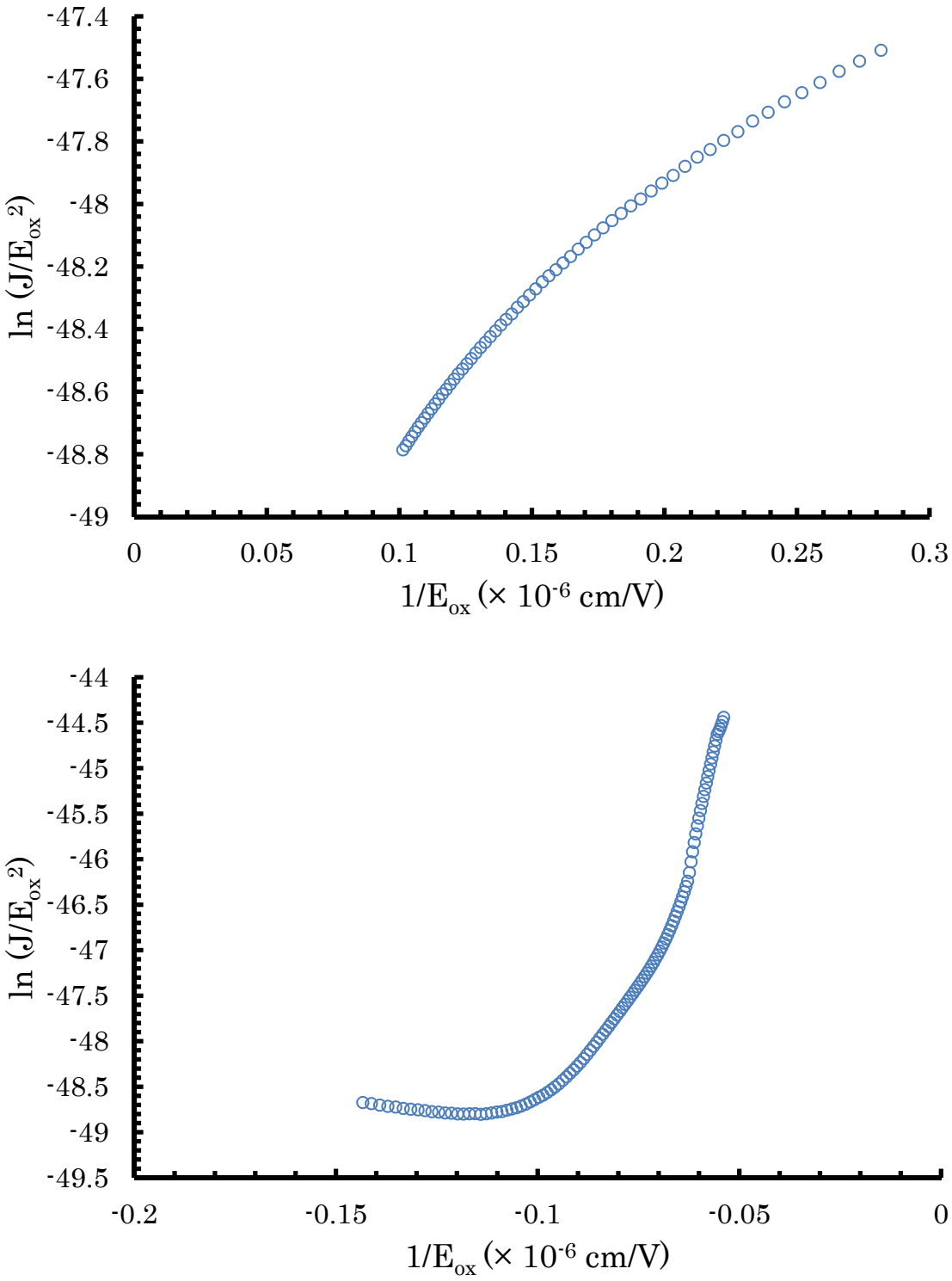


Figure R4.22 ln J/E_{ox}^2 vs $1/E_{ox}$ of annealed $Al/Al_2O_3/[HfO_2/Al_2O_3]_2/HfO_2/SiO_2$ /p-type Si capacitor structure under the positive sweep voltage (top) and the negative sweep voltage (bottom). The linear region shows the FN tunneling.

Chapter 6
Conclusions and Recommendations for Future Works

In this dissertation, the MAHOS capacitor structures which consist of Al gate electrode, Al_2O_3 blocking oxide, high-κ dielectric charge trapping layer, SiO_2 tunneling layer, and p-type Silicon substrate were fabricated. Our focus of study was investigating the charge trapping characteristics in the charge trapping characteristics in the MAHOS capacitor structure with high-κ Al_2O_3/HfO_2 nanolaminates and high-κ Al_2O_3 and HfAlO as charge trapping layer for non-volatile memory application. The high-κ Al_2O_3/HfO_2 nanolaminates was proposed as charge trapping layer since heterojunction formed between two dissimilar semiconductors provide unique properties due to the difference in energy band structures. To realized the main goal, a series of research works was carried out, including fabrication of the MAHOS capacitor structures and evaluation of their structural properties, observation of their energy band parameters which are energy bandgap, valence band offset, and conduction band offset, investigation of charge trapping characteristics and the mechanism of charge transport in as-deposited MAHOS capacitor structures, and investigation of charge trapping characteristics and the mechanism of charge transport in annealed MAHOS capacitor structures. These works are concluded and the recommendations for future works are stated.

6.1 Conclusions

In fabricating the MAHOS capacitor structures, design of the structures and structural paramaters such as thickness for each layer were considered in such a way that the MAHOS structures would be suitable for non-volatile memory application. The methods of the structure fabrication which are suitable for electronic applications and common in semiconductor fabrication industry are utilized, including Radio Corporation America (RCA) cleaning, rapid thermal oxidation (RTO), atomic layer deposition (ALD), rapid thermal annealing (RTA) for annealed structures, and thermal evaporation. The structural properties of the MAHOS structures, including the microstructure and the chemical states were evaluated by high-resolution transmission electron microscope (HRTEM) and x-ray photoemission spectroscopy (XPS). From cross-sectional HRTEM images, it is observed that all MAHOS capacitors could be fabricated

with good quality structures, including good interface between layers and excellent uniformity of thickness. The natural SiO_2 can be removed by RCA cleaning and high quality SiO_2 can be grown by RTO with good interface between of SiO_2/Si, small roughness of about 1 – 2 monolayers of Si and uniform thickness of SiO_2. Al_2O_3 and HfO_2 were deposited by ALD with good control of thickness and good uniformity. The phase of high-κ dielectric in as-deposited MAHOS structures is amorphous. After annealing, amorphous high-κ films transformed into crystalline high-κ films and the heterostructure of $[Al_2O_3/HfO_2]_4/HfO_2$ and $[Al_2O_3/HfO_2]_2/HfO_2$ became HfO_2/HfAlO/HfO_2. From XPS measurement, it is observed that in Al_2O_3/HfO_2 nanolaminate structure, from the surface of blocking oxide to the part close to SiO_2/Si stack, the Al 2p and Hf 4f peaks are shifted to higher binding energy, but the binding energy difference between Al 2p and Hf 4f peaks are constant which is ~57 eV. This indicates that the binding energy shift of Al 2p and Hf 4f is due to the dipole formation in HfO_2/Al_2O_3 interface. In annealed MAHOS structures with nanolaminates as CTL, the XPS measurement at high-κ/SiO_2-/Si interface shows that the observed layer close to SiO_2/Si in sample NA2 and NB2 is crystalline HfAlO/HfO_2 with more dominant HfO_2 and that in sample HA2 close to SiO_2/Si is crystalline HfAlO layer.

Before observing charge trapping characteristics, the energy band parameters, including energy bandgap, valence band offset (VBO), and conduction band offset (CBO) of materials in as-deposited and annealed MAHOS structures have been observed by reflection electron energy-loss spectroscopy (REELS) and x-ray photoelectron spectroscopy (XPS). By REELS, it is confirmed that the bandgap value of SiO_2 is 8.9 eV. The bandgap of material depend on its phase and structure, e.g. the band gap of Al_2O_3 is 6.7 eV for amorphous and 6.9 eV for crystalline which is different from the bulk one which is 8.8 eV, while the band gap of amorphous and crystalline HfO_2 are 5.8 eV and 5.9 eV, respectively and the band gap of amorphous and crystalline HfAlO appear to be 5.9 eV and 6.0 eV, respectively. By XPS measurement, it is found that VBO can be determined by measuring the VBM difference of two materials since it is found that at flatband condition the CL and VBM position are the same for SiO_2 and p-type Si at bulk and interface. The band alignment in high-κ oxide in contact with SiO_2/p-type Si structure in thermodynamical equilibrium is affected by Si substrate. The alignment of Fermi levels are built by charge transfer among the surface gap states on the surface of high-κ oxide, the interfacial gap states at high-κ oxide/SiO_2 and SiO_2/Si interfaces, and the space charges of Si

substrate. From REELS and XPS results, the band alignment in flatband condition was constructed. The band alignment of high-κ oxide in contact with high-κ oxide and high-κ oxide in contact with SiO_2/p-type Si substrate were also evaluated by considering the concepts of interfacial or surface gap states and charge neutrality level (CNL).

Charge trapping characteristics of as-deposited MAHOS structures has been observed by measuring the high frequency (1 MHz) capacitance – voltage (C – V) characteristics using inductance – capacitance – resistance (LCR) meter. Under the sweep gate voltage from inversion to accumulation, the MAHOS structures with Al_2O_3/HfO_2 nanolaminates as CTL trap more electrons than the structures with Al_2O_3 and HfAlO single layer as CTL. The structure with HfAlO as CTL traps more electrons compared to the structure with Al_2O_3 as CTL since it is a mixture with HfO_2. The MAHOS structure with [Al_2O_3 (2 nm)/HfO_2 (2 nm)]$_2$/ HfO_2 (2 nm) as CTL traps more electrons than the structure with [Al_2O_3 (1 nm)/HfO_2 (1 nm)]$_2$/ HfO_2 (1 nm) since thicker HfO_2 in nanolaminate provides more sites to trap electrons and Al_2O_3 layer has higher conduction band offset with respect to silicon substrate prevents charge injection to the next HfO_2 layer. Under the sweep gate voltage from accumulation to inversion, electron detrapped and hole injection by F – N tunneling through tunnel oxide occurred. The mechanism of charge transport in as-deposited MAHOS capacitor structures was identified by carrying out the leakage current measurement. Electrons or holes tunnel through SiO_2 layer when a large electric field is applied across an oxide layer. The experimental J-E curves were fitted by Fowler – Nordheim tunneling models in which $\ln(J/E^2)$ is plotted as a function of 1/E. Linear fitting prove the FN tunneling is the main charge transport mechanism under certain electric field.

After rapid thermal annealing in N_2 ambient at 1000^{o}C, the amorphous high-κ delectrics in MAHOS capacitor structures transform into polycrystalline structure. The charge trapping characteristics was observed based on high frequency (1 MHz) C – V measurement. The charge transport mechanism was analyzed from leakage current density as a function of sweep voltage. Annealed MAHOS structure with HfO_2/HfAlO/HfO_2 nanolaminates as charge trapping layer traps more charges than the structure with Al_2O_3 and HfAlO single layer as CTL. Polycrystalline structures provide trap sites such as grain boundaries and become dominant trapping centers in CTL. As a result, annealed MAHOS capacitor structures trap more charges than the as-deposited structures. Based on the leakage current density study, the charge transport mechanism from Si substrate through SiO_2 tunneling layer is F – N tunneling mechanism. However, charges that

trapped in the defects in polycrystalline high-κ may leak through defects to the metal gate.

6.2 Recommendations

High-κ nanolaminates such as $[HfO_2/Al_2O_3]/HfO_2$ structures have potential to be applied as charge trapping layer in non-volatile memory devices. To further study the possibility of utilizing high-κ nanolaminates as charge trapping layer, there are some recommendations that need to be consider from the point of view of material selection and fabrication condition.

As blocking layer, SiO_2 is ideal because it has high conduction band offset (CBO) and valence band offset (VBO) with respect to Si substrate and has amorphous structure with good thermal stability. However, the use of SiO_2 as blocking oxide prevents further miniaturization of the device since the dielectric constant is only 3.9. Based on International Technology Roadmap for Semiconductors (ITRS) scaling projections for charge trapping NAND flash, Al_2O_3 is recommended to be used as blocking oxide until 2024. The main problem is usually the crystalline phase of Al_2O_3 is gamma-phase which has lower band gap of 6.9 eV than alpha-phase with band gap of 8.8 eV. The possibility of transforming amorphous Al_2O_3 into alpha-phase Al_2O_3 needs to be studied.

In order to reduce leakage through blocking oxide, several annealing techniques need to be consider such as furnace anneal in oxygen at 800^{o}C, ozone anneal at 450^{o}C combined with furnace oxygen anneals, and rapid thermal anneal (RTA) at 800^{o}C in N_2O.

$[HfO_2/Al_2O_3]/HfO_2$ nanolaminates structure provide unique properties due to heterojunction with different energy gap formed between two dissimilar semiconductors. However, the nanolaminates structure break after annealing. $[HfO_2/Al_2O_3]/HfO_2$ nanolaminates can be applied in memory structure which does not required annealing at high temperature.