T2R2 東京科学大学 リサーチリポジトリ
Science Tokyo Research Repository

論文 / 著書情報
Article / Book Information

題目(和文)	
Title(English)	Charge Trapping Characteristics of MAHOS Capacitor Structures with High-k Dielectric Materials as Charge Trapping Layers
著者(和文)	RifaiAbdulloh
Author(English)	Abdulloh Rifai
出典(和文)	学位:博士（工学）, 学位授与機関:東京工業大学, 報告番号:甲第10027号, 授与年月日:2015年12月31日, 学位の種別:課程博士, 審査員:中村 吉男,史 蹟,小林 能直,村石 信二,三宮 工
Citation(English)	Degree:, Conferring organization: Tokyo Institute of Technology, Report number:甲第10027号, Conferred date:2015/12/31, Degree Type:Course doctor, Examiner:,,,,
学位種別(和文)	博士論文
Category(English)	Doctoral Thesis
種別(和文)	論文要旨
Type(English)	Summary

Powered by T2R2 (Science Tokyo Research Repository)

（博士課程）
Doctoral Program

論 文 要 旨

THESIS SUMMARY

専攻： Department of	材料工学	専攻	申請学位（専攻分野）： Academic Degree Requested	博士 Doctor of	（工学）
学生氏名： Student's Name	Abdulloh RIFAI		指導教員（主）： Academic Advisor(main)		中村吉男
			指導教員（副）： Academic Advisor(sub)		

要旨（英文 800 語程度）
Thesis Summary（approx.800 English Words ）

High-κ dielectric materials are projected to be used as charge trapping layer (CTL) for non-volatile memory application to meet the challenges of cell size continual down-scaling and operating voltage reduction. High-κ dielectric materials are beneficial to enhance memory performance since they contain electronic defects at certain levels in their bandgap. In addition, with higher dielectric constant, they allow a higher electric field over the tunnel dielectric which results in enhanced program/erase speed. In our research, we fabricated metal - Al_2O_3 - high-κ dielectric materials - SiO_2 - p-type Si (MAHOS) capacitor structures with aluminum as metal gate electrode, Al_2O_3 as blocking oxide (BO), and Al_2O_3, HfAlO, and HfO_2/Al_2O_3 nanolaminates (NL) as CTL and investigated their memory characteristics. Nanolaminates as CTL were proposed since heterojunction formed between two dissimilar semiconductors is created to get unique properties provided by the difference in energy gap.

The MAHOS structures were successfully fabricated with the process flow of the device fabrication including Radio Corporation America (RCA) cleaning, rapid thermal oxidation (RTO), atomic layer deposition (ALD), post-deposition annealing (PDA), and thermal evaporation. As observed from cross-sectional high resolution transmission electron microscope (HRTEM) images, the MAHOS structures have good interface between layers and excellent uniformity of thickness. The as-deposited CTL and BO are amorphous. After PDA, amorphous Al_2O_3 layer in $Al/Al_2O_3/SiO_2$/p-type Si transformed into highly-textured crystalline Al_2O_3. On the other hand, amorphous $[Al_2O_3/HfO_2]_4/HfO_2$ and $[Al_2O_3/HfO_2]_2/HfO_2$ charge trapping layer and Al_2O_3 blocking oxide transformed into polycrystalline HfO_2/HfAlO/HfO_2 and polycrystalline Al_2O_3, respectively.

The energy band alignment of the as-deposited and annealed MAHOS structures were constructed by considering energy band parameters of materials, including energy bandgap, valence band offset (VBO), and conduction band offset (CBO), based on the measurement of the band parameters by reflection electron energy-loss spectroscopy (REELS) and x-ray photoelectron spectroscopy (XPS). The bandgap of material depend on its coordination number and phase, e.g. the band gap of Al_2O_3 is 6.7 eV for amorphous and 6.9 eV for crystalline which is different from the bulk one which is 8.8 eV, while the band gap of amorphous and crystalline HfO_2 are 5.8 eV and 5.9 eV, respectively and the band gap of amorphous and crystalline HfAlO appear to be 5.9 eV and 6.0 eV, respectively. The binding energy shifts in the structures as observed by XPS indicate that band bending occurs due to the alignment of Fermi levels which are built by charge transfer among the surface gap states on the surface of high-κ oxide, the interfacial gap states at high-κ oxide/SiO_2 and SiO_2/Si interfaces, and the space charges of Si substrate. From the schematic band diagrams of the structures, it is suggested that more negative charges are present on HfO_2-side which also means there are more negative charges in HfO_2/Al_2O_3 nanolaminates, causing upward band bending in the middle part of the structures.

Charge trapping characteristics of as-deposited and annealed MAHOS structures were observed and the mechanism of charge injection was explained. Under the sweep gate voltage from inversion to accumulation, the MAHOS structures with Al_2O_3/HfO_2 nanolaminates as CTL trap more electrons than the structures with Al_2O_3 and HfAlO single layer as CTL with the memory window of 2.4 V under the gate voltage of 8 V. Larger memory window in the structures with Al_2O_3/HfO_2 nanolaminates as CTL is due to the nature of heterojunction where HfO_2 in nanolaminates traps electrons while Al_2O_3, with larger conduction band offset with respect to silicon, modulates charge trapping distribution. Under the sweep gate voltage from accumulation to inversion, electrons detrapped and holes injected. The mechanism of charge transport in the structures was identified by carrying out the leakage current measurement. The experimental J-E curves were fitted by Fowler - Nordheim tunneling model in which $\ln(J/E^2)$ is plotted as a function of 1/E. Linear fitting prove the FN tunneling is the main charge transport mechanism under certain electric field. On the other hand, annealed MAHOS structure with HfO_2/HfAlO/HfO_2 nanolaminates as CTL traps more charges than the structure with Al_2O_3 and HfAlO single layer as CTL with the memory window of 2.9 V under the gate voltage

of 8 V. Moreover, annealed MAHOS capacitor structures trap more charges than the as-deposited structures. PDA changes the microstructure of high-κ layers significantly which affect the properties of electron traps. In annealed MAHOS structures, line defects and grain boundaries are the dominant trapping centers, while in as-deposited MAHOS structures point defects are the sites for charge traps. Based on the leakage current density study, the charge transport mechanism from Si substrate through SiO_2 tunneling layer is F - N tunneling mechanism. Charges that trapped in the defects in polycrystalline high-κ may leak through defects to the metal gate.

In short, their memory properties of MAHOS capacitor structures with Al_2O_3, HfAlO, and HfO_2/Al_2O_3 nanolaminates NL as CTL have been studied with also considering their microstructures and energy band alignment of the structures. It has been proven that due to the unique properties of heterojunction with different energy gap formed between two dissimilar semiconductors, $[HfO_2/Al_2O_3]_x/HfO_2$ nanolaminates provide wider memory window at relatively low voltage. Therefore, $[HfO_2/Al_2O_3]_x/HfO_2$ nanolaminates have potential to be applied as charge trapping layers in NVM structures.

備考 : 論文要旨は、和文 2000 字と英文 300 語を 1 部ずつ提出するか、もしくは英文 800 語を 1 部提出してください。
Note : Thesis Summary should be submitted in either a copy of 2000 Japanese Characters and 300 Words (English) or 1copy of 800 Words (English).

注意：論文要旨は、東工大リサーチリポジトリ（T2R2）にてインターネット公表されますので、公表可能な範囲の内容で作成してください。
Attention: Thesis Summary will be published on Tokyo Tech Research Repository Website (T2R2).