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論 文 要 旨

THESIS SUMMARY

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学生氏名： Student's Name	Ahmed Awad	指導教員（主）： Academic Advisor(main)	Prof.Atsushi Takahashi
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要旨（英文 800 語程度）
Thesis Summary (approx.800 English Words)

As advanced technology nodes continue scaling down into sub-16nm regime, optical micro-lithography, wherein, an Integrated Circuit (IC) is patterned layer by layer through a pixelated mask, becomes more vulnerable to wafer image distortions and lithographic process variations. This turns out into pattern fidelity and overall lithographic yield degradation. Since Next Generation Lithography (NGL) is still not mature, the industry relies heavily on Resolution Enhancement Techniques (RETs), wherein, Optical Proximity Correction (OPC) with 193nm immersion lithography is dominant in the foreseeable future.

OPC algorithms have been well established both in literature and commercial tools to improve pattern fidelity and mask robustness against process variations. However, to keep pace with advanced technology nodes shrinkage, OPC algorithms are getting more aggressive to preserve acceptable pattern fidelity onto the silicon. Consequently, complex mask solutions are generated which turns out into mask data volume explosion, and thus, mask manufacturing cost increase. Furthermore, the need to shorten OPC computation time is often scarified in favor of maximizing pattern fidelity. As a result, long computation time is required to cover the huge number of mask shapes needed in realistic industrial cases.

This dissertation proposes an OPC engine methodology whose purpose is to find a highly manufacturable mask solution for a target pattern circuitry with high pattern fidelity and high robustness against process variations within a short computation time.

First of all, a novel intensity estimation model is proposed to estimate the wafer image for the mask of interest within a short time with exploiting the intensity information extracted from some reference mask. This is achieved through adaptively compensating the reference mask intensity information with exploiting an observed relation between intensity and local mask density. Overall, this results in significant shortening of OPC computation time (whose dominant part is typically wafer image computation).

Thereafter, pattern fidelity under process variations improvement techniques are proposed. This includes OPC adjustment steps guided by the proposed intensity estimation model. Such adjustments include Two-segment shifting, corner hammering, assisting features insertion, and input intensity tuning to increase intensity slope for less process variations. Adjustment dimensions are heuristically determined following regression based functions in such a way that the intensity impact induced by feature adjustment is included in the OPC response for other features. This turns out into accelerating the algorithm convergence in terms of maximizing pattern fidelity and robustness against process variations.

To reduce mask manufacturing cost with preserving acceptable pattern fidelity under process variations, post-OPC mask adjustments are proposed. Such adjustments are guided through a cluster-based linearly interpolated intensity error modeling included in the OPC recipe along with an error prediction model. The purpose of such models is to keep the algorithm effective in terms of pattern fidelity and robustness against process variations with respecting mask constraints for higher mask manufacturability.

The proposed OPC methodology has been examined on the public benchmarks which represent the most challenging M1 layer and compared with recently published algorithms. The proposed algorithm outperforms the state-of-art algorithms on both small and large scale benchmarks in terms of pattern fidelity under process variations. Furthermore, it has been found as 2X faster than the fastest algorithm among the state-of-art. Finally, the proposed methodology reduces significantly the number of mask design rule violations, which turns out into higher mask manufacturability when compared with other algorithms.

備考 ： 論文要旨は、和文 2000 字と英文 300 語を 1 部ずつ提出するか、もしくは英文 800 語を 1 部提出してください。
Note : Thesis Summary should be submitted in either a copy of 2000 Japanese Characters and 300 Words (English) or 1copy of 800 Words (English).