

論文 / 著書情報
Article / Book Information

題目(和文)	線形化技術を用いた高速オープンループパイプラインアナログ - デジタル変換器の研究
Title(English)	Study of High-Speed Open-Loop Pipeline Analog-to-Digital Converters Using Linearization Techniques
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出典(和文)	学位:博士（学術）, 学位授与機関:東京工業大学, 報告番号:甲第10355号, 授与年月日:2016年9月20日, 学位の種別:課程博士, 審査員:松澤 昭,益 一哉,高木 茂孝,岡田 健一,伊藤 浩之,塚本 三六
Citation(English)	Degree;, Conferring organization: Tokyo Institute of Technology, Report number:甲第10355号, Conferred date:2016/9/20, Degree Type:Course doctor, Examiner:,,,,,
学位種別(和文)	博士論文
Category(English)	Doctoral Thesis
種別(和文)	論文要旨
Type(English)	Summary

論文要旨

THESIS SUMMARY

専攻 :	Physical Electronics	専攻
Department of		
学生氏名 :	Yu Lilan	
Student's Name		

申請学位 (専攻分野) :	博士 (Philosophy)
Academic Degree Requested	Doctor of
指導教員 (主) :	Akira Matsuzawa
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要旨 (英文 800 語程度)

Thesis Summary (approx.800 English Words)

This thesis presents a design strategy for high-speed and low-power pipeline analog-to-digital converters (ADCs) in advanced process. To realize high-speed pipeline ADC with relatively low power consumption, open-loop structure is competitive. However, the nonlinearity issue of open-loop residue amplifier in pipeline ADC limits the ADC resolution. This research is to find solutions for enhancing the linearity of open-loop amplifier. Thus, high-speed and low-power pipeline ADCs with moderate resolution can be realized. The developed open-loop pipeline ADCs provide evidence of the effectiveness of these solutions in advanced process.

Chapter 1 sets the background of this research. The function and necessity of data converters in electrical systems are introduced. Along with the development of complementary metal-oxide-semiconductor (CMOS) technology, the effective gate length is continuing to scale down. The intrinsic gain of transistor reduces along with the scaling down, which increases the design difficulty for analog circuits. On the other hand, high-speed and low-power ADC is highly required in several applications. Thus, finding solutions to design high-speed and low-power ADC in advanced process is the main theme of this research.

In Chapter 2, ADC design considerations and difficulties in advanced CMOS technology are discussed. Based on the discussion, pipeline ADC is selected as a competitive candidate to realize high speed and moderate resolution by a single core with relatively low power consumption. Comparing with Conventional closed-loop amplification and interpolation-based amplification, open-loop structure has the best power efficiency because it has no requirement of high DC-gain, sufficient phase margin, and dual path. However, the issue of nonlinearity needs to be suppressed. In consequence, high speed and low power open-loop pipeline ADC with moderate resolution can be achieved. The purpose of this research is to push the boarder of pipeline ADC to higher resolution and sampling rate.

In Chapter 3, the concept, circuit implementation as well as the simulation results of the proposed open-loop amplifier with linearization technique is introduced. A conventional common source amplifier is used as one of the single stage amplifier. Its gain is decreasing while the input amplitude becomes larger. Another single stage amplifier utilizes local feedback loop to obtain a gain with reversed nonlinearity, whose gain will increase while the input amplitude becomes larger. By cascading two single stage amplifiers with reversed nonlinearity, the product of the two reversed-nonlinear gain becomes flat. The proposed open-loop amplifier is able to support a 9-bit resolution while conventional one only supports 6 bits.

In Chapter 4, a 9-bit 1.8-GS/s 44-mW pipeline ADC using linearized open-loop amplifiers is introduced. With the high-linearity open-loop amplifier, giga-hertz sampling rate and moderate resolution are realized with a relatively low power consumption of 44 mW. CDAC gain calibration is proposed to obtain the accurate stage gain. Top-plate sampling timing for double sampling is also proposed to further enhance the power efficiency of the residue amplifier. With these techniques, this ADC achieves the lowest FoM of 83 fJ/c.-s. among pipelined ADCs who do not need off-chip nonlinearity calibration for the residue amplifiers. The proposed linearization technique relaxes the nonlinearity issue of the open-loop amplifier while maintaining its advantages, proved that it is an efficient technique in advanced CMOS technology.

In Chapter 5, a time-domain linearization technique for dynamic amplifier is introduced. The idea is adding an input amplitude dependent value to compensate the nonlinearity. However, adding an input dependent value into the differential current is difficult. Thus, the compensation is carried out in time domain, because the gain of a dynamic amplifier is also proportional to the amplification time. The second order nonlinearity of input transistors is utilized to detect the input amplitude. The small difference under different input amplitude is amplified by a local positive feedback loop. The feedback signal controls the tail current as well as the amplification time. Therefore, the gain is adjusted according to the input amplitude and the gain is compensated to be flat. Comparing with conventional dynamic amplifier, the linearity is improved to be able to support a resolution of 9 bits, while conventional dynamic amplifier can only support 6-bit resolution.

In Chapter 6, a 9-bit 500-MS/s 6.0-mW dynamic pipeline ADC using time-domain linearized dynamic amplifiers is introduced. Besides the linearization technique for dynamic amplifier, common mode calibration, stage gain calibration and self-clocking techniques are employed. An inverter threshold-voltage based calibration is used to match the output common mode voltage of dynamic amplifier to that of references. CDAC attenuation is utilized to calibrate the stage gain automatically. To further improve the power efficiency, the global clock tree is replaced by local self-triggered clock. With these techniques, a full dynamic pipeline ADC is developed which achieves the world best SNDR of 50.5 dB and FoMs of 157 dB among dynamic pipeline ADCs.

Finally, the conclusion of this research is drawn in Chapter 7. The comparison with all other ADCs and the future works related to this research topic are discussed.

備考：論文要旨は、和文 2000 字と英文 300 語を 1 部ずつ提出するか、もしくは英文 800 語を 1 部提出してください。

Note : Thesis Summary should be submitted in either a copy of 2000 Japanese Characters and 300 Words (English) or 1 copy of 800 Words (English).

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