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Title(English)	Low-Power Noise Shaping Techniques in a Successive Approximation Register Analog-to-Digital Converter
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Thesis outline

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This thesis presents a study of low power noise shaping techniques in a successive approximation register (SAR) analog-to-digital converter (ADC). Meanwhile, low power noise shaping techniques are applied into the design of a sigma delta modulator.

Chapter 1 discusses the background of this research. With the scaling of the process and power supply, the SAR ADC can achieve ultra-high speed and very low power. However, the resolution of a SAR ADC is restrained by non-ideal effects. The noise shaping technique can provide a solution to improve the resolution. However, the noise shaping is usually based on an operational amplifier (opamp), which is not power efficient. Meanwhile, the design of an opamp with high gain and high bandwidth is becoming more and more difficult when the process is scaled. Therefore, a power efficient and scaling friendly noise shaping technique, called fully passive noise shaping (FPNS), is proposed in this thesis.

In Chapter 2, fundamental concept of quantizers and quantization noise is presented. Quantization noise in a SAR ADC may decide the final resolution of the SAR ADC. To reduce the quantization noise is very important. With the help of noise shaping, the quantization noise can be reduced. The resolution of the SAR ADC can be improved by the introduction of noise shaping effect into the SAR ADC. The realization of noise shaping in a SAR ADC is related to the quantization noise in the SAR ADC. So, the quantization noise in different SAR ADC architecture is reviewed in this chapter.

In Chapter 3, some traditional noise shaping SAR ADCs, which are based on opamps, are briefly reviewed. However, there are many disadvantages to realize noise shaping by an opamp. Therefore, a 1^{st} order FPNS SAR ADC by charge-redistribution is proposed to solve the issues by an opamp. The basic architecture and operation principle of a SAR ADC are maintained by the proposed technique. As a result, all the advantages of a SAR ADC will pass into the proposed fully passive noise shaping SAR ADC. Meanwhile, the detailed operation sequences and detailed circuit information are shown in this chapter. To verify the proposal, a prototype is designed in a 65-nm CMOS process. The measurement results show that a 58-dB SNDR is achieved based on an 8-bit CDAC at 50-MS/s sampling frequency. It consumes 120.7 μW power from a 0.8-V supply and achieves a Walden FoM of 14.8-fJ per conversion step.

In Chapter 4, an improved fully passive noise shaping, a 2^{nd} order FPNS SAR ADC, is introduced. 1^{st} order FPNS has limited noise shaping effect. Meanwhile, 1^{st} order noise shaping may suffer from idle cycle which is not expected effect. Thus, a 2^{nd} order FPNS SAR ADC, which can solve the issues of 1^{st} FPNS and improves the noise shaping effect, is presented in this chapter. The detailed realization information is shown and detailed circuit design is illustrated. To verify the proposal, a prototype is designed in a 65-nm CMOS process. The measurement results show that a 64.9-dB SNDR is achieved based on an 8-bit CDAC at 64-MS/s sampling frequency. It consumes 252.9-μW power from a 1-V supply and achieves a Walden FoM of 10.9 fJ per conversion step.

In Chapter 5, a 3^{rd} order sigma delta modulator with the 1^{st} order FPNS SAR ADC as quantizer is introduced. Only one opamp is used to realize the 3^{rd} order noise shaping effect, which can save power.

By the proposed technique, the potential instability issue is also solved. This chapter is focused on the architecture level analysis about the realization of the proposed single-opamp third-order sigma delta modulator. An opamp is shared to realize 2^{nd} order noise shaping while an additional 1^{st} order noise shaping is realized by the FPNS SAR ADC. A passive adder is also explained in order to realize an addition before the quantizer.

In Chapter 6, the detailed circuit design of the proposed 3^{rd} order sigma delta modulator is presented. The circuit information of an opamp is illustrated. Also, the concept and circuit realization of a data weighted averaging technique used to calibrate the mismatch of CDAC is introduced. A prototype is developed in a 65-nm CMOS process and is measured to verify the power efficiency. The sigma delta modulator gives a 75-dB SNDR with a signal bandwidth of 100 kHz and a sampling clock of 3.2 MHz. The prototype dissipates 45.8 μW with a Walden FoM of 50 fJ/conv.-step when analog supply is 0.7 V and digital supply is 0.85 V.

Finally, the conclusion of this research is drawn in Chapter 7. The future prospects of low power fully passive noise shaping techniques and the future works related to this research topic are discussed.