論文 / 著書情報
Article / Book Information

題目(和文)	
Title(English)	A study on in-situ formation of HfNx gate stack structure with bilayer gate insulator utilizing ECR plasma sputtering
著者(和文)	AtthiNithi
Author(English)	Nithi Atthi
出典(和文)	学位:博士（工学）, 学位授与機関:東京工業大学, 報告番号:甲第10342号, 授与年月日:2016年9月20日, 学位の種別:課程博士, 審査員:大見 俊一郎,宗片 比呂夫,筒井 一生,渡辺 正裕,飯野 裕明
Citation(English)	Degree:, Conferring organization: Tokyo Institute of Technology, Report number:甲第10342号, Conferred date:2016/9/20, Degree Type:Course doctor, Examiner:,,,,
学位種別(和文)	博士論文
Category(English)	Doctoral Thesis
種別(和文)	要約
Type(English)	Outline

Outline of Doctoral Thesis

A study on in-situ formation of HfN_x gate stack structure with bilayer gate insulator utilizing ECR plasma sputtering

Nithi Atthi

Department of Electronics and Applied Physics
Interdisciplinary Graduate School of Science and Engineering

Supervisor: Associate Professor Shun-ichiro Ohmi

Chapter 1 Introduction

Metal gate/high-κ gate insulator (MG/HK) stacks are necessary to suppress short-channel effects and high leakage current (J_g) even for three-dimensional (3-D) metal-insulator-semiconductor field-effect transistors (MISFETs). With the scaling of MISFETs, the equivalent oxide thickness (EOT) should be decreased. However, the formation of interfacial layer (IL) with relatively low-dielectric constant of oxide-based high-κ gate insulator such as HfO_2 has prevented EOT scaling. Therefore, hafnium nitride (HfN_x) gate insulator (I) is promising material to suppress IL formation at HfN_x/Si interface due to the absent of the oxygen atom in HfN_x film.

It was reported that higher nitrogen (N) concentration, such as Hf_3N_4 or higher, would be required for EOT scaling below 0.5 nm due to the increase of the N concentration would lead to higher dielectric constant. However, the directly deposited nitride gate insulator with high N concentration on Si substrate severely degrades the interface properties at high-κ/Si interface. Therefore, nitride-based IL especially HfN_x IL with low N concentration is required to improve the quality of high-κ/Si interface. Furthermore, the contamination and the oxidation during ex-situ Al gate electrode (G) deposition were found to degrade the electrical properties such as mobility.

In this dissertation, bilayer HfN_x (I) with in-situ formed metallic HfN_x (G) utilizing electron-cyclotron-resonance (ECR) plasma sputtering was purposed. The ECR plasma sputtering is used to realize in-situ deposition of HfN_x gate stacks to suppress contamination and oxidation at MG/HK interface, so that the excellent properties of HfN_x gate stacks such as EOT of 0.5 nm or below, low J_g and high mobility are expected to be obtained.

Chapter 2 Fabrication and characterization methods

To fabricate the MIS-diode with bilayer HfN_x gate insulator, p-Si(100) and p-Si(110) substrates (N_A: $1x10^{15}$ cm^{-3}) were cleaned by sulfuric peroxide mixture (SPM) and diluted hydrofluoric acid (DHF). Then, 0.9 nm-thick HfN_x IL with different Ar/N_2 gas flow ratio of 20/8 sccm (N_2: 28.8%, 0.20 Pa), 16/12 sccm (N_2: 44%, 0.20 Pa) and 12/16 sccm (N_2: 57%, 0.20 Pa) were deposited on p-Si(100) by using ECR plasma sputtering (JSW AFTY: AFTEX-3400). The μ-wave/RF power was 500/400W.

The 1.7 nm-thick $HfN_{1.3}$ (I) layer was in-situ deposited on HfN_x IL with Ar/N_2 gas flow ratio of 8/20 sccm (N_2: 71%, 0.20 Pa). The μ-wave/RF power was 500/500W. Then, 10 nm-thick metallic $HfN_{0.5}$ gate electrode (G) was in-situ deposited on $HfN_{1.3}$ (I).

The post-metallization annealing (PMA) before Al deposition called PMA1 process was carried out in both N_2 and $N_2/4.9\%H_2$ ambient (1 SLM) by silicon-wafer-covering (SWC) process utilizing rapid thermal annealing (RTA) system. The 40 nm-thick Al contact layer was ex-situ evaporated on HfN_x gate stacks of the samples with and without $HfN_{0.5}$ (G). Al contact layer was patterned by H_3PO_4:HNO_3 mixed solution (50:3) for 60s. Then, HfN_x gate stacks (90x90 μm^2) were patterned by DHF (1%) for 90s. Some samples were annealed in $N_2/4.9\%H_2$ ambient after gate stacks patterning called PMA2 process. Then, the backside Al contact was

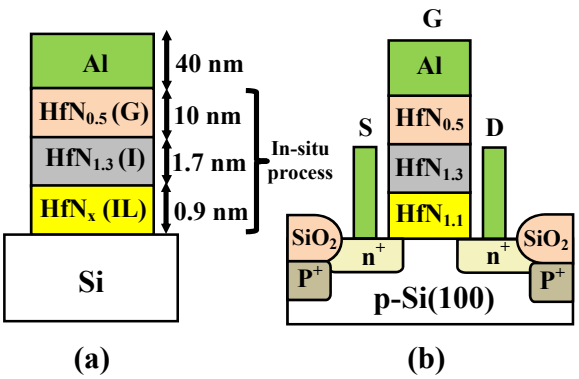

Fig. 1 Schematic cross-sectional structures of in-situ formed of HfN_x gate stacks with bilayer HfN_x gate insulator. (a) MIS-diode and (b) n-MISFET.

deposited by evaporation. Direct contact of 2.5 nm-thick $HfN_{1.3}$ (I) layer on p-Si(100) was fabricated for comparison by using ECR plasma sputtering (Ar/N_2: 8/20 sccm, N_2: 71%, 0.20 Pa). The μ-wave/RF power was 500/500W.

The n-MISFET was fabricated using gate-last process as the structure shown in Fig. 1. After local oxidation of Si (LOCOS) isolation and channel stop formation, source/drain (S/D) was formed by ion implantation of PH_3 at 20 keV with a dose of $5x10^{15}$ cm^{-2}. The activation annealing was carried out in N_2 ambient at 1000°C/2 min. The HfN_x gate stacks with $HfN_{1.1}$ IL was deposited by using the same process condition as MIS-diode. After contact holes formation, Al pads were patterned for source, drain and gate electrodes. The gate width (W) was 90 μm and gate length (L) was varied from 2 to 10 μm.

In case of 3-D structure on Si(100), sub-100 nm line-and-space (L/S) Si-etched patterns was fabricated by photoresist (PR) trimming and Si etching by CF_4/O_2 plasma utilizing an inductively coupled plasma reactive ion etching (ICP-RIE). Then the 3-D MIS diodes were fabricated with bilayer HfN_x gate insulator. The Si flattening process in $Ar/4.9\%H_2$ ambient at 925°C/10 min was also investigated on 3-D structure.

Due to the limited of the pages number in this abstract, the characterization methods were not explained. More details are precisely explained in the thesis.

Chapter 3 Effects of nitrogen concentration on the electrical properties of HfN_x gate insulator with ex-situ Al gate electrode

First, the deposition condition of HfN_x gate stacks was investigated. Utilizing the chamber cleaning process including plasma cleaning (Ar: 20 sccm, 0.16 Pa, μ-wave/RF power: 600/0W) and pre-sputtering (Ar: 20 sccm, 0.16 Pa, μ-wave/RF power: 500/500W) prior to the HfN_x films deposition can suppress the carbon contamination and oxidation in HfN_x gate stacks.

Then, the dependence on the N_2 gas flow ratio of the atomic composition of HfN_x films was investigated. The N concentrations were evaluated as $HfN_{0.5}$, $HfN_{1.0}$, $HfN_{1.2}$, and $HfN_{1.3}$ when the N_2 gas flow ratio were 2%, 28.8%, 57%, and 71%, respectively. The HfN_x film ($x \geq 1.0$) shows the insulating properties while the HfN_x film ($x < 1.0$) shows the metallic properties. Figure 2 shows that direct contact of amorphous HfN_x (I) with high N concentration ($x > 1.1$) on Si substrate severely degrades the electrical properties of HfN_x gate stacks. This might be attributed to high D_{it} and residual stress in HfN_x film induced by excess N concentration degraded the properties at HfN_x/Si interfaces. Bilayer $HfN_{1.3}/HfN_x$ gate insulator showed significantly improved the qualities of HfN_x gate stacks due to suppression of positive fixed charges. However, excess N concentration in $HfN_{1.2}$ IL generated high D_{it}.

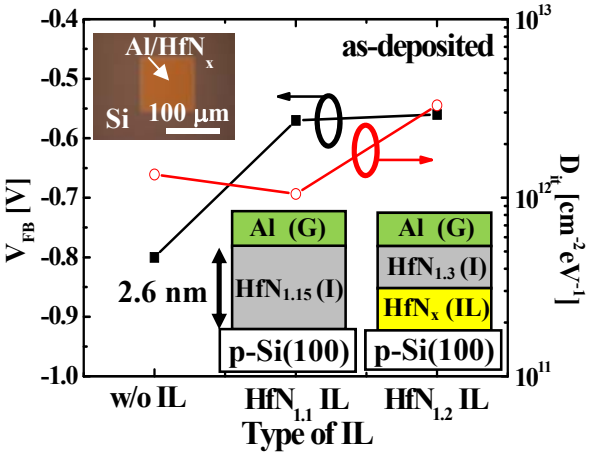

Fig. 2 Effects of N concentration in HfN_x IL on the C-V characteristics (100 kHz) of as-deposited bilayer HfN_x gate insulator MIS-diode using Al electrode.

Therefore, $HfN_{1.1}$ IL (N_2: 44%, 0.20 Pa) is suitable for bilayer HfN_x (I) to improve the interface properties of HfN_x gate stacks. However, the degradation of the electrical properties of bilayer HfN_x (I) might be due to the contamination and the oxidation during ex-situ Al (G) deposition.

Chapter 4 In-situ formation of bilayer HfN_x gate insulator with HfN_x gate electrode utilizing ECR plasma sputtering

Utilizing the in-situ deposited 10-nm thick metallic $HfN_{0.5}$ (G) (Ar/N_2: 10/0.2 sccm, 0.09 Pa, μ-wave/RF power: 500/400W) with the work function of 4.8 eV and resistivity below 0.1 mΩ·cm on bilayer HfN_x (I), the J_g was well suppressed four order-of-magnitudes compared to ex-situ Al (G). This might be due to the excellent interface properties without contamination and surface oxidation. However, the large hysteresis width (ΔV) of 184 mV and significant flatband voltage (V_{FB}) shift (V_{FB}: -1.0 V) were obtained in C-V characteristics after PMA1 in N_2/4.9%H_2 ambient at 500°C/10 min.

Chapter 5 Device characteristics of MISFETs with in-situ formed HfN_x gate stack structure with bilayer HfN_x gate insulator

Next, the electrical properties of bilayer HfN_x (I) on 3-D structure were investigated as shown in Fig. 3. The 90 nm L/S Si-etched patterns with near-vertical sidewall (θ: 80°) was fabricated by photoresist trimming process (CF_4/O_2: 15/15 sccm, RF/bias: 600/0W for 90 s) of 1.0 μm L/S pattern. The Si-etched patterns were fabricated by plasma etching (CF_4/O_2: 90/10 sccm, RF/bias: 200/20W for 10s) with the height of 20 nm. Due to the negligible substrate orientation dependence of bilayer HfN_x gate insulator, the high J_g on 3-D structure strongly depends on the surface roughness of 3-D structure, especially at the sidewall and space region of 3-D structure.

To suppress the high J_g on 3-D structure, Si surface flattening process is required. By using flattening process in Ar/4.9%H_2 ambient at 925°C/10 min, the RMS roughness of

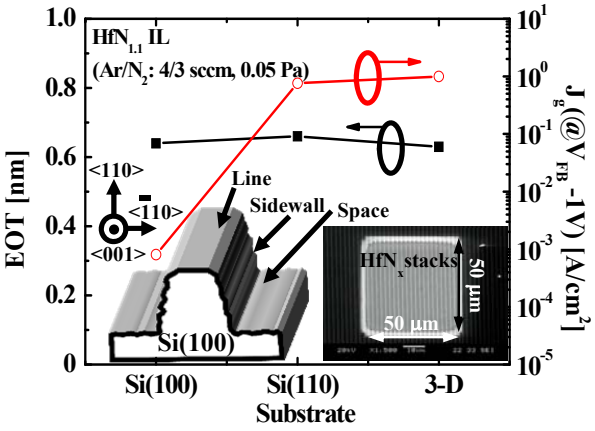

Fig. 3 Dependence of the substrate orientation and 3-D structure on the EOT and leakage current density of bilayer HfN_x gate insulator with in-situ HfN_x (G).

Si(100) decreased from 0.12 nm to 0.07 nm while the sidewall angle of Si-etched pattern decreased from 80° to 64°.

Chapter 6 Conclusions

In this dissertation, I investigated the in-situ formation of HfN_x gate stack structure with bilayer gate insulator utilizing ECR plasma sputtering. It can be concluded that bilayer HfN_x (I) with low N concentration of $HfN_{1.1}$ IL shows significantly improved the interface qualities, which leads to the superior electrical properties of in-situ formed HfN_x gate stacks with $HfN_{0.5}$ (G) on both planar and 3-D structure. Therefore, HfN_x gate stacks technology will be useful for realizing the high performance 3-D MISFETs.

Publication lists

Paper and Journal [3]

[1] **Nithi Atthi**, Dae-hee Han and Shun-ichiro Ohmi, "Si surface orientation dependence on the electrical characteristics of HfN gate insulator with sub-0.5 nm EOT formed by ECR plasma sputtering," MRS Proc., **1588**, JSAPMRS13-1588-6607 (2014).

[2] **Nithi Atthi** and Shun-ichiro Ohmi, "Investigation of bilayer HfN gate insulator utilizing ECR plasma sputtering," IEICE Electron. Exp., **13** (10), pp. 1-6 (2016).

[3] Shun-ichiro Ohmi, Sohya Kudoh and **Nithi Atthi**, "Variability improvement by Si surface flattening of electrical characteristics in MOSFETs with high-k HfON gate insulator," IEEE Trans. Semicond. Manuf., **28** (3), pp. 266-271 (2015).

International conferences and symposium [6]

[1] **Nithi Atthi**, Dae-hee Han, Huiseong Han and Shun-ichiro Ohmi, "An effect of sidewall orientation to the electrical characteristics of 3-dimensional MIS-diodes with HfN gate insulator formed by ECR plasma sputtering," IEEE EDS WIMNACT-37, P-52 (2013).

[2] **Nithi Atthi**, Dae-hee Han, Huiseong Han and Shun-ichiro Ohmi, "Si surface orientation dependence on the electrical characteristics of HfN gate insulator with sub-0.5 nm EOT formed by ECR plasma sputtering," JSAP-MRS joint symposia, 18p-PM1-32, JSAP-MRS-E-068 (2013).

[3] **Nithi Atthi** and Shun-ichiro Ohmi, "Effects of annealing process on the electrical properties of HfN_x gate stacks with bilayer gate insulator formed by ECR plasma sputtering," Asia-Pacific Workshop on Fundamentals and Applications of Advanced Semiconductor Devices (AWAD), B4-3, pp. 193-197 (2016).

[4] Sohya Kudoh, **Nithi Atthi** and Shun-ichiro Ohmi, "A study on Si(100) surface flattening process and its effect on MIS diode characteristics," Asia-Pacific Workshop on Fundamentals and Applications of Advanced Semiconductor Devices (AWAD), 1A-4, pp. 29-31 (2014).

[5] Shun-ichiro Ohmi, Sohya Kudoh and **Nithi Atthi**, "Variability improvement by Si surface flattening of electrical characteristics in MOSFETs with high-k HfON gate insulator," International Symposium on Semiconductor Manufacturing (ISSM), PO-O-36 (2014).

[6] [Invited] Shun-ichiro Ohmi, Sohya Kudoh and **Nithi Atthi**, "Influence of Si surface flatness on device characteristics of MOSFETs with high-κ gate insulator," The 5th International Symposium on Organic and Inorganic Electronic Materials and Related Nanotechnologies (EM-NANO), OB2-I-2, p. 21 (2015).

Domestic conferences [14]

[1] **Nithi Atthi**, Dae-hee Han, Huiseong Han and Shun-ichiro Ohmi, "Investigation of the substrate orientation-dependent on the electrical characteristics of HfN gate insulator formed by ECR plasma sputtering," The 74th JSAP autumn meeting, 17p-B5-9, p.13-046 (2013).

[2] **Nithi Atthi**, Dae-hee Han and Shun-ichiro Ohmi, "Electrical properties and reliability of ultrathin HfN gate insulator formed on Si(100) and Si(110)," IEICE Technical Report (SDM), vol. 113 (247), pp. 5-10 (2013).

[3] **Nithi Atthi**, Dae-hee Han and Shun-ichiro Ohmi, "Effects of annealing ambient on the electrical properties of HfN gate insulator formed by ECR plasma sputtering," The 61st JSAP spring meeting, 18a-D8-11 (2014).

[4] **Nithi Atthi** and Shun-ichiro Ohmi, "Electrical characteristics of as-deposited HfN gate insulator formed by ECR plasma sputtering," IEICE Technical Report (SDM), vol. 113 (255), pp. 19-22 (2014).

[5] **Nithi Atthi** and Shun-ichiro Ohmi, "In-situ formation of HfN_x gate stack structures utilizing ECR plasma sputtering," The 62nd JSAP spring meeting, 13a-A24-12, p. 12-325 (2015).

[6] **Nithi Atthi** and Shun-ichiro Ohmi, "Investigation of stacked HfN gate insulator formed by ECR plasma sputtering," IEICE Technical Report (SDM), vol. 115 (280), pp. 57-62 (2015).

[7] **Nithi Atthi** and Shun-ichiro Ohmi, "In-situ formation of bilayer HfN gate insulator utilizing ECR plasma sputtering," IEICE Biotechnology and Electronics Meeting, P. 11 (2015).

[8] **Nithi Atthi** and Shun-ichiro Ohmi, "Investigation of bilayer HfN gate insulator formed by ECR plasma sputtering," The 63rd JSAP spring meeting, 19a-S224-5, p. 11-019 (2016).

[9] [Invited] **Nithi Atthi** and Shun-ichiro Ohmi, "Investigation of bilayer HfN_x gate insulator formed by ECR plasma sputtering," The 77rd JSAP autumn meeting (2016).

[10] Sohya Kudoh, Dae-hee Han, **Nithi Atthi**, and Shun-ichiro Ohmi, "Effect of Si(100) surface flattening process on device characteristics," The 61st JSAP spring meeting, 19a-D9-6 (2014).

[11] Elham Heidari, Sohya Kudoh, **Nithi Atthi**, Dae-hee Han and Shun-ichiro Ohmi "Effects of nitrogen concentration on the electrical properties of HfN gate insulator formed by ECR plasma sputtering," The 61st JSAP spring meeting, 19p-D9-18 (2014).

[12] Sohya Kudoh, **Nithi Atthi** and Shun-ichiro Ohmi, "Annealing ambient dependence of Si surface flattening process," The 62nd JSAP spring meeting, 12a-A27-1, p. 12-214 (2015).

[13] Fadliondi, **Nithi Atthi** and Shun-ichiro Ohmi, "L/W ratio dependence of bottom contact pentacene OFET," The 62nd JSAP spring meeting, 14p-D3-1, p. 11-532 (2015).

[14] Mizuha Hiroki, **Nithi Atthi**, Yasutaka Maeda, and Shun-ichiro Ohmi, "Fabrication of top gate type pentacene-based OFET with α-rubrene as gate insulator," The 77rd JSAP autumn meeting, (accepted) (2016).

Awards [3]

[1] **Best presentation award**
Nithi Atthi and Shun-ichiro Ohmi, "In-situ formation of bilayer HfN gate insulator utilizing ECR plasma sputtering," IEICE Biotechnology and Electronics Meeting, P. 11 (2015).

[2] **Young scientist presentation award**
Nithi Atthi and Shun-ichiro Ohmi, "Investigation of bilayer HfN gate insulator formed by ECR plasma sputtering," The 63rd JSAP spring meeting, 19a-S224-5, p. 11-019 (2016).

[3] **Best paper award**
Shun-ichiro Ohmi, Sohya Kudoh and **Nithi Atthi**, "Variability improvement by Si surface flattening of electrical characteristics in MOSFETs with high-k HfON gate insulator," International Symposium on Semiconductor Manufacturing (ISSM), PO-O-36 (2014).

Related research

Paper and Journal [20]

[1] **N. Atthi** J. Supadech, G. Dupuy, O. Nimittrakoolchai, A. Pankiew, S. Supothina, W. Jeamsaksiri, C. Hruanun, A. Poyai and C-H. Brachais, "Increasing active surface area to fabricate ultra-hydrophobic surface by using "black silicon" with Bosch etching process," J. Nanosci. Nanotechnol, **12**, pp. 1-9 (2012).

Conferences [71]

[1] **N. Atthi**, P. Pholprasit, T. Thammabut, W. Jeamsaksiri, C. Hruanun, A. Poyai and R. Silapunt, "Adjustment of exposure kinetics simulation parameters for a 3-D microstructure fabrication using double-exposure lithography," The 26th international technical conference on circuits/systems, computers and communications (ITC-CSCC 2011), pp. 302-305 (2011).