

論文 / 著書情報
Article / Book Information

Title	Progress Toward 1000-mV Open-Circuit Voltage on Chalcopyrite Solar Cells
Author	Homare Hiroi, Yasuaki Iwata, Hiroki Sugimoto, akira yamada
Journal/Book name	IEEE Journal of Photovoltaics, Volume , ,
Issue date	2016, 8
DOI	http://dx.doi.org/10.1109/JPHOTOV.2016.2598263
URL	http://www.ieee.org/index.html
Copyright	(c)2016 IEEE. Personal use of this material is permitted. Permission from IEEE must be obtained for all other users, including reprinting/republishing this material for advertising or promotional purposes, creating new collective works for resale or redistribution to servers or lists, or reuse of any copyrighted components of this work in other works.
Note	このファイルは著者（最終）版です。 This file is author (final) version.

Progress Toward 1000mV Open-Circuit Voltage on Chalcopyrite Solar Cell

Homare Hiroi, Yasuaki Iwata, Hiroki Sugimoto and Akira Yamada

Abstract—Previously, open circuit voltage of 960mV was reported on Se-free Cu(In,Ga)S₂ solar cell with CdS buffer layer. In this paper, we report our latest progress toward 1000mV on Se-free Cu(In,Ga)S₂ solar cell with Cd-free buffer layer. Highest open circuit voltage of 973mV was demonstrated by rapid thermal annealing and Zn_{1-x}Mg_xO buffer layer application.

Index Terms—Cu(In,Ga)S₂, High open circuit voltage, Rapid thermal annealing, Zn_{1-x}Mg_xO buffer layer.

I. INTRODUCTION

Previously, we reported a new world-record efficiency (Eff) of 15.5% on Se-free Cu(In,Ga)S₂ (CIGS) solar cell via KCN-free process[1]. Regarding open circuit voltage (V_{oc}), 960mV has been achieved[2]. It was the highest V_{oc} in the field of chalcopyrite solar cells, however, it was still lower as compared with CdTe and perovskite solar cells[3,4]. Thus, we have been exploring the potential of over 1000mV on Se-free CIGS solar cells for further improvement of Eff. As a result, the highest V_{oc} of 973mV has been demonstrated by rapid thermal annealing (RTA) for sulfurization and Zn_{1-x}Mg_xO application for buffer layer, as shown in Fig. 1. In this paper, we report our latest progress toward 1000mV on Se-free CIGS solar cell.

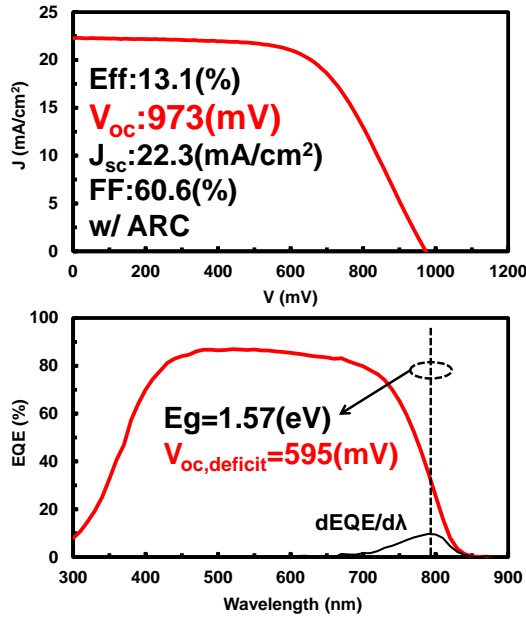


Fig. 1. J-V and EQE characteristics of 973mV Se-free CIGS solar cell fabricated by KCN-free process with Cd-free Zn_{1-x}Mg_xO buffer layer.

II. EXPERIMENTAL CONDITION

In this experiment, we prepared Se-free CIGS solar cells with an area of approximately 0.45 cm². Figure 2 shows a schematic image of our standard cell structure. First of all, Mo back-electrode layer, Cu, Ga and In metal-stack precursor layers were deposited by DC-sputtering onto glass substrate. The precursor layers were sulfurized only with H₂S gas via RTA in a furnace to form a p-type Se-free CIGS absorber layer. CdS or Zn_{1-x}Mg_xO buffer layers were deposited onto the absorber layers by chemical bath deposition (CBD) or atomic layer deposition (ALD). Then, intrinsic ZnO (i-ZnO) and In₂O₃:Sn layers were deposited by ALD and ion evaporation respectively. Finally, Ni/Al front-electrode and MgF₂ layers were deposited by electron-beam evaporation.

The current density-voltage (J-V) characteristics of our solar cells were measured at 25°C under standard air mass (AM) 1.5 spectrum condition with a constant-light solar simulator. The spectral content of the light is determined by the use of a xenon lamp (KXL-5000HFW) and five halogen lamps (JCD-100V-1000WC/Z) with an intensity of 100mW/cm² with optical lenses inside the solar simulator. The radiation power is calibrated regularly by means of a silicon reference solar cell. External quantum efficiency (EQE) characteristics of the pure-sulfide CIGS cells were investigated. The elemental composition and the depth profile of the absorber layers were measured by using inductively coupled plasma atomic emission spectroscopy (ICP-AES) and glow discharge optical emission spectrometry (GD-OES), respectively. In order to investigate the band-alignment between the buffer and the absorber layer, ultraviolet photoelectron spectroscopy (UPS) with He I light source (21.22 eV) was performed after the buffer layer deposition. For the depth-resolved UPS measurements, Ar⁺ (3kV) ion beam sputtering equipped in the UPS system was used. The reference level is the Fermi level, and the calibration was performed with Au as a standard sample.

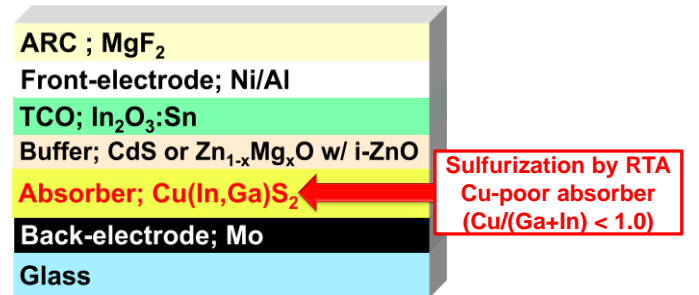


Fig. 2. Schematic image of our device structure.

III. RESULT AND DISCUSSIONS

A. Sulfurization via RTA

In this section, the benefits of sulfurization on Se-free CIGS by RTA are discussed. We used RTA for sulfurization to shorten the fabrication process. Figure 3 shows the dependence of ramp-up speed on the electrical parameters of Se-free CIGS solar cells with CdS buffer layers. It is clear that higher ramp-up speed contributed to the improvement of cell performance. It is assumed that the higher ramp-up speed has benefits of low Ga content on the surface of the absorber and superior Ga grading at the back. Figure 4 shows Ga depth profile of various ramp-up speeds (20, 40 and 140C/min) obtained from GD-OES analysis. Absorbers with various ramp-up speeds clearly show a different Ga depth profiles. The absorber fabricated with ramp-up speed of 20C/min shows a high Ga/(Ga+In) ratio of 15% at the surface compared with the others. In addition, its depth profile shows a more gradual gradient. The absorber fabricated by 40C/min shows a low Ga/(Ga+In) ratio at the surface. However, the Ga grading is less steeper than the absorber fabricated with 140C/min. In the absorber fabricated by 40C/min, both the Ga/(Ga+In) ratio at the surface and its inclination were improved. Eff of sample fabricated by 20C/min was low because of very poor electrical parameters. The poor electrical parameters are possibly caused by the high Ga/(Ga+In) ratio at the surface and the gradual Ga grading of absorber. For the sample processed with 40C/min, the cell performance improves to Eff of 14% from 7~9% due to the low Ga composition at the surface. Sample of 140C/min boosted the Eff due to the improvement of V_{oc} and J_{sc} , attributed by the increased Ga content toward the back surface (CIGS/Mo). Thus, the benefits of low Ga composition at the surface and high Ga grading at the back surface have been brought to light. Based on the depth-profile results of Ga in Se-free CIGS cells, as one of several possibilities, we believe that low Ga/(Ga+In) ratio on the surface contributes to reduced Ga_{Cu} defects and steep Ga grading can accelerate the electrons toward the space charge region. Hence, it may indicate that Ga grading can enhance J_{sc} and V_{oc} . Furthermore, the results also suggest that Ga contents on the surface and Ga grading of the absorbers are controllable by tuning the ramp-up speed. Regarding FF, it was also significantly improved by higher ramp-up speed, which suggests another benefits resulted from the ramp-up speed condition. We will try our best to find the mechanism of FF improvement in the near future.

Finally, the minority carrier lifetime was measured by time-resolved photoluminescence (PL) as a gauge to evaluate the absorber quality. The PL measurement was performed at room temperature, using a pulsed laser with a wavelength of 532nm and an excitation power of 4.67mW (excitation intensity of about 595mW/cm²). Figure 5 shows the PL lifetime of Se-free absorber fabricated by high ramp-up speed. Although with a high efficiency, its lifetime was merely 0.97ns. This short lifetime indicates that there is further room to improve the Se-free CIGS absorbers.

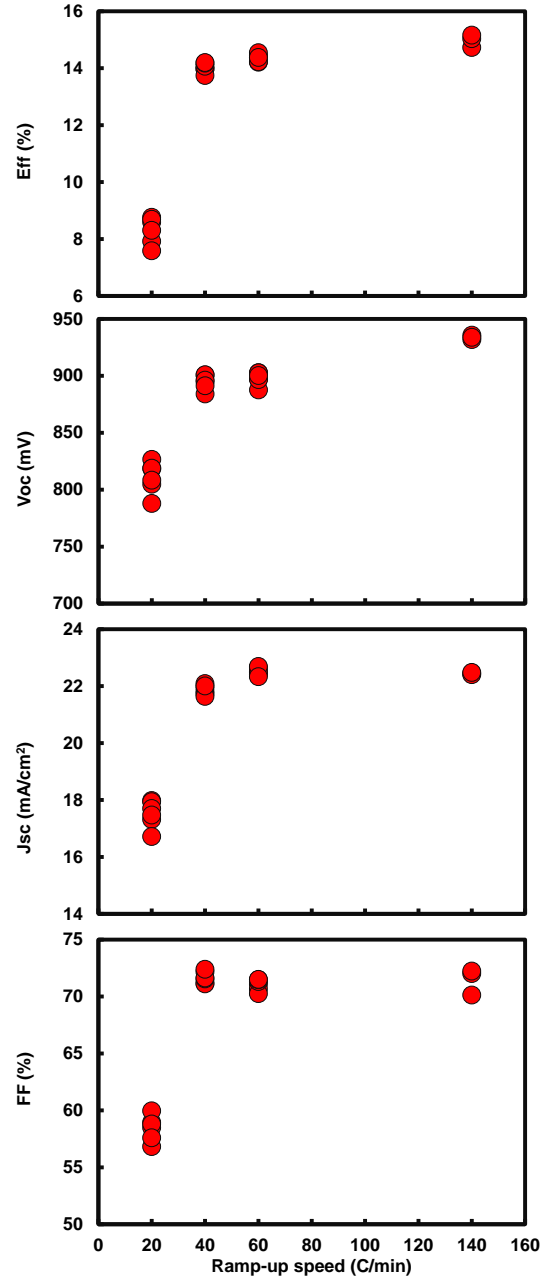


Fig. 3. Dependence of ramp-up speed on electrical parameters of Se-free CIGS solar cells with CdS buffer layers.

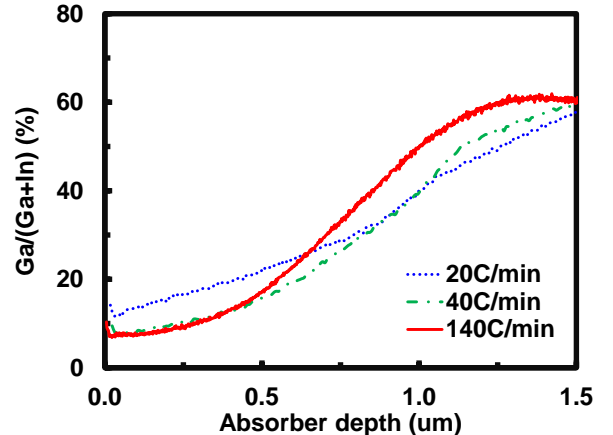


Fig. 4. GD-OES Ga/(Ga+In) ratio as a function of film depth of various ramp-up speed.

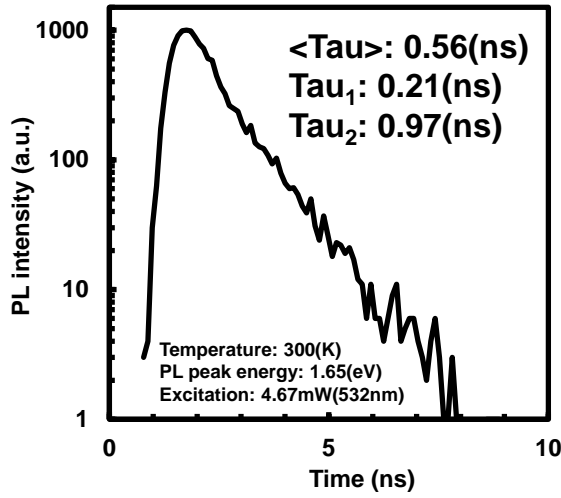


Fig. 5. PL lifetime of our Se-free CIGS absorber.

B. $\text{Zn}_{1-x}\text{Mg}_x\text{O}$ buffer layer

Figure 6 shows the dependence of Mg contents in $\text{Zn}_{1-x}\text{Mg}_x\text{O}$ buffer layer on the electrical parameters of Se-free CIGS solar cells using absorbers fabricated via the ramp-up speed of 140C/min. Higher Mg contents contribute to the improvement of cell performance. It is assumed that the conduction band-offset (CBO) between absorber and buffer layers was modulated because the E_g of $\text{Zn}_{1-x}\text{Mg}_x\text{O}$ buffer layer is known to be controllable by Zn to Mg ratio[4]. In this work, the CBO was calculated from the valence band-maximum (VBM) and the conduction band-minimum (CBM). The VBM of the $\text{Zn}_{1-x}\text{Mg}_x\text{O}$ buffer and Se-free CIGS absorber layers was measured by the UPS measurement. The CBM of the $\text{Zn}_{1-x}\text{Mg}_x\text{O}$ ($x=0.26$), $\text{Zn}_{1-x}\text{Mg}_x\text{O}$ ($x=0.15$) and Se-free CIGS was estimated by using E_g value of 3.7eV, 3.9eV and 1.55eV, respectively[5]. $\text{Zn}_{1-x}\text{Mg}_x\text{O}$ ($x=0.26$) cell shows that the CBM of buffer layer in the vicinity of the interface can be increased when compared with the $\text{Zn}_{1-x}\text{Mg}_x\text{O}$ ($x=0.15$) cell. This upward shift of CBM is potentially relevant to the V_{oc} improvement as shown in Fig. 7.

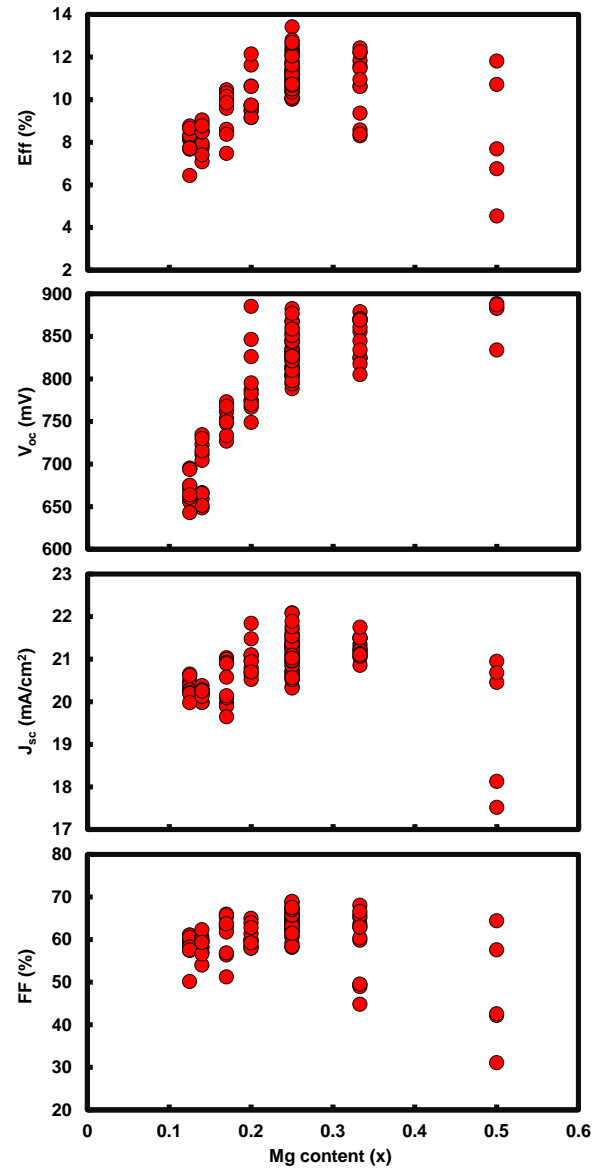


Fig. 6. Dependence of Mg contents in $\text{Zn}_{1-x}\text{Mg}_x\text{O}$ buffer layer on electrical parameters of Se-free CIGS solar cells. Higher Mg contents contributed improvement of cell performance.

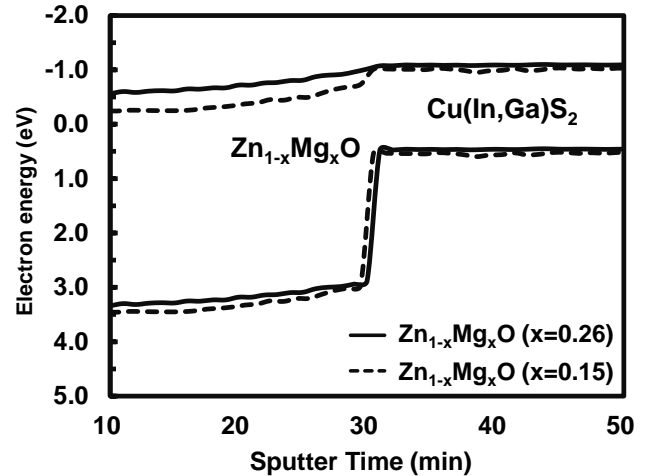


Fig. 7. Comparison of band-offset at buffer/absorber interface for Se-free CIGS cells with $\text{Zn}_{1-x}\text{Mg}_x\text{O}$ ($x=0.26$) and ($x=0.15$) buffer layers.

C. V_{oc} deficit

Figure 8 summarizes a comparison between V_{oc} and E_g of our Se-free CIGS cells fabricated via various ramp-up speed with CdS and $Zn_{1-x}Mg_xO$ buffer layers. Each triangle marker with black, blue, green, orange and red circle shows 20, 40, 60, 140C/min of ramp-up speed with CdS buffer layer and 140C/min of ramp-up speed with $Zn_{1-x}Mg_xO$ buffer layer, respectively. Higher V_{oc} was achieved by higher ramp-up speed during sulfurization, with drastically improved V_{oc} deficit ($E_g/q - V_{oc} = \Delta V$). In addition, the V_{oc} improvement was confirmed by applying the $Zn_{1-x}Mg_xO$ buffer layer. This result suggests that both the absorber quality and the interface between the buffer and the absorber layers are among the key factors to enhance V_{oc} , and it is very effective to apply $Zn_{1-x}Mg_xO$ buffer layer into the Se-free CIGS cells for V_{oc} improvement. Finally, the lowest V_{oc} deficit of 595mV was achieved with absorber's E_g of 1.57eV. It has much better V_{oc} deficit compared with the other Se-free chalcogenide solar cell such a Cu_2ZnSnS_4 cell[6].

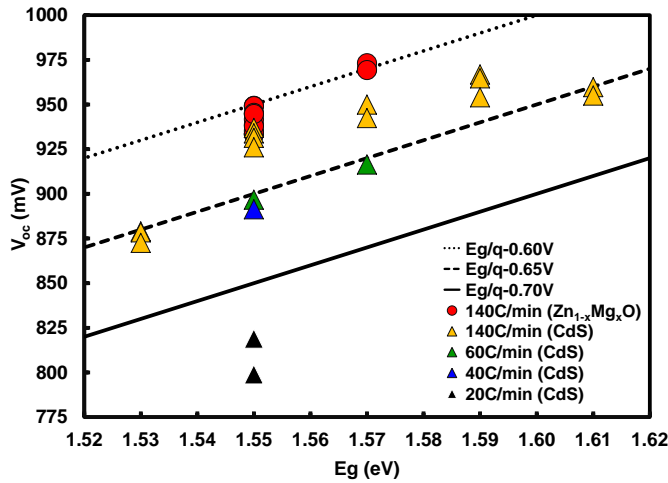


Fig. 8. Correlation between V_{oc} and E_g on our Se-free CIGS cells fabricated via four kinds of ramp-up speed (20, 40, 60, 140C/min) with CdS and $Zn_{1-x}Mg_xO$ buffer layers.

IV. CONCLUSION

The V_{oc} of 973mV was achieved on chalcopyrite solar cell thanks to the Se-free CIGS fabrication via RTA and the application of Cd-free $Zn_{1-x}Mg_xO$ buffer layer. The higher ramp-up speed was effective to reduce Ga/(Ga+In) ratio of the absorber's surface and to produce steeper Ga grading at the back. In addition, V_{oc} was boosted by optimizing Mg content of $Zn_{1-x}Mg_xO$ buffer layer. We believe that further research based on these results will boost the V_{oc} of chalcopyrite solar cells toward 1000mV, and we are now intensively developing the Se-free CIGS solar cells.

ACKNOWLEDGEMENT

The authors gratefully acknowledge discussion with Dr. KongFai Tai of Solar Frontier K.K.

REFERENCES

- [1] H. Hiroi, Y. Iwata, S. Adachi, H. Sugimoto, and A. Yamada, "New World-Record Efficiency for Pure-Sulfide $Cu(In,Ga)S_2$ Thin-Film Solar Cell With Cd-free Buffer Layer via KCN-Free Process", *IEEE J. Photovoltaics*, vol.6, no. 3, pp. 760-763, May 2016, DOI: 10.1109/JPHOTOV.2016.2537540.
- [2] H. Hiroi, Y. Iwata, K. Horiguchi, and H. Sugimoto, "960-mV Open-Circuit Voltage Chalcopyrite Solar Cell", *IEEE J. Photovoltaics*, vol.6, no. 1, pp. 309-312, Jan. 2016, DOI: 10.1109/JPHOTOV.2015.2479470.
- [3] W.K. Metzger, J.M. Burst, D.S. Albin, E. Colegrove, J. Moseley, J. Duenow, A. Kanevce, S.B. Farrell, H. Moutinho, M.O. Reese, S. Johnston, T. Barnes, C. Perkins, H. Guthrey, S.H. Wei, and M. Al-Jassim, "Resetting the Defect Chemistry in CdTe", presented at 42nd IEEE Photovoltaic Specialists Conference, New Orleans, Louisiana, USA, June 14-19, 2015.
- [4] Noh JH, Im SH, Heo JH, Mandal TH, and Seok SI. "Chemical Management for Colorful, Efficient, and Stable Inorganic–Organic Hybrid Nanostructured Solar Cells", *Nano Letters*. 2013; 13; 1764–1769.
- [5] T. Minemoto, T. Negami, S. Nishiwaki, H. Takakura, and Y. Hamakawa, "Preparation of $Zn_{1-x}Mg_xO$ Films by RF Magnetron Sputtering", *Thin Solid Films* 372 (2000) 173-176.
- [6] O. Gunawan, T. Gokmen, B. S. Shin, and S. Guha, "Device characteristics of high performance Cu_2ZnSnS_4 solar cell", presented at 38th IEEE Photovoltaic Specialists Conference, Austin, Texas, USA, June 3-8, 2012.



Homare Hiroi was born in Nagano, Japan. He received the B.S. degree in human mechanical engineering from Kanazawa University, Japan in 2008, and M.S. degree in advanced energy engineering science from Kyushu University, Japan in 2010.

From 2010 to 2014, he was a Research Scientist with Atsugi Research Center, Showa Shell Sekiyu K.K. and Solar Frontier K.K. in Japan. He was also a Visiting Researcher with

T. J. Watson Research Center, IBM, USA, focusing mainly on research of kesterite solar cells.

Since 2014, he has been a Project Leader of CIS R&D with the Technology Development Division, Solar Frontier K.K. His current research interests include high-performance (CIGSe-based) and low-cost (Se-free CIGS-based and CZTS-based) chalcogenide solar cells. In addition, he is working toward the Ph.D. degree within the Chalcopyrite Solar Cells Group, Department of Physical Electronics, Tokyo Institute of Technology, Japan.

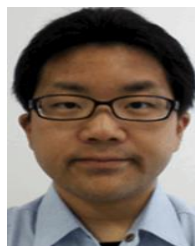
Mr. Hiroi was a recipient of the Young Scientist Presentation Award (The Japan Society of Applied Physics, 2016), the Innovative PV Incentive Award (Japan Society for the Promotion of Science, 2016), the Solar Frontier K.K. Junior Fellow Award (2016), the Solar Frontier K.K. President's Award (2014) and the PVSEC Best Paper Award (PVSEC-23, 2013).



Yasuaki Iwata was born in Yamagata, Japan. He received the B.S. degree in electronic engineering from the University of Electro-Communication, Japan in 2009, and the M.S. degree in physical electronics from Tokyo Institute of Technology, Japan in 2012. He has joined Showa Shell Sekiyu K.K. and Solar Frontier K.K. since 2012. He is now focusing on the research of chalcogenide solar cells as a research scientist of Solar Frontier

K.K.

Mr. Iwata was a recipient of the Innovative PV Incentive Award (Japan Society for the Promotion of Science, 2013).



Hiroki Sugimoto was born in Kanagawa, Japan. He received the B.S. degree in 2003, the M.S. degree in 2005, and the Ph.D. degree in electronic engineering from The University of Tokyo, Japan, in 2008. He was also a Researcher of Japan Aerospace Exploration Agency, focusing on characterization of GaAs-based triple junction and mc-Si solar cells.

From 2008 to 2010, he was a Research Scientist with Atsugi Research Center, Showa Shell Sekiyu K.K. and Solar Frontier K.K. in Japan. In addition, he became a Project Leader of CIS R&D with the Technology Development Division, Solar Frontier K.K. in 2010, and engaged in development of chalcogenide solar cells until 2014.

Since 2014, he has been a Manager of the Technology Development Division, Solar Frontier K.K.



Akira Yamada was born in Yamanashi, Japan, in 1961. He received the B.S. degree in 1984, the M.S. degree in 1986, and the Ph.D. degree in physical electronics from Tokyo Institute of Technology, Japan, in 1989. He is currently a Professor of Tokyo Institute of Technology. He is a renowned expert in thin-film solar cell device physics and technologies, and his group is now focusing on the investigation of chalcogenide

thin-film solar cells.

He is a co-author of more than 200 scientific publications and over 300 international conference presentations. He was a co-organizer of the Symposium M (Thin film chalcogenide photovoltaic materials) in E-MRS 2010 Spring Meeting and a co-organizer of the Symposium M (Thin Film Semiconductor Photovoltaics) in Spring 2009 MRS Meeting. He is a Chief Editor of the Japanese Journal of Applied Physics.

Prof. Yamada was a recipient of the PVSEC Paper Award (PVSEC-12, 2001), the WCPEC Poster Award (WCPEC-3, 2003), and the Best Paper Award of 19th Photovoltaic Science and Engineering Conference in 2013.