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Integration Techniques of Phase Locked Loops for SoCs in Fine Design-Rule Process

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Chapter 1

General Introduction

1.1 Background and Motivations

A Phase Locked Loop (PLL) is one of the most important circuit blocks in microprocessors, wireless transceivers, and signal processing integrated circuits (ICs) for various kinds of applications. Recently system-on-chip (SoC) integrates several kinds of PLL in a single chip because there are many functions which deal with real-time signal processing both in analog and digital regions [1][2]. Of course, PLL has already been used for many applications for a long time and PLL concept itself is not new. However, PLL has been taken charge of many features in ICs, for example, an on-chip high-speed clock generation, a frequency synthesizer, a clock phase synchronizer, and a modulator. Using complementary metal oxide semiconductor (CMOS) transistors in finer design rule, a PLL will operate in higher speed and more complex applications year by year. Therefore many researchers are still developing and discussing PLL techniques suitable for their applications [3]–[7].

In general it is said that PLL is one kind of control systems and is constructed by a quite simple feedback loop. Well, PLL only consists of four key functional elements, a phase comparator, a charge pump, a voltage controlled oscillator, and a divider. So far PLL operation has been

analyzed by using linear feedback theories with discrete time sampling. However, to adopt PLL into practical semiconductors, it is necessary to study PLL impairments on its performance over many non-ideal conditions, low supply voltage, large leakage current, and so on, which would be occurred in fine design rule CMOS processes. Especially to use as a synthesizer or a clock generator applications for SoCs, these PLL specifications would be very severe in jitter and frequency accuracy because they usually use PLL outputs as reference clocks. Therefore, it is becoming more and more difficult to design PLL for SoCs recently and necessary to develop new design techniques to solve the problems for large leakage current and low supply voltage and as to provide good phase noise and low jitter performance. Furthermore, new system level design should be introduced into PLL because specifications of the PLL strongly tie to system performance of the applications.

In this dissertation, firstly general PLL design and its key functional elements are described. Next new PLL techniques, especially circuits for semiconductors in fine design rule processes are proposed. Furthermore, new PLLs for signal modulation applications for wireless transceivers and storage signal processing ICs which need to integrate PLLs with much severe specifications are described and several key techniques to meet such severe specifications are proposed. And then, modulator structures using PLL and their circuit techniques in details are also discussed in this dissertation.

1.2 Organization of the Dissertation

In Chapter 2, a design procedure of PLL based on the feedback loop theory and the details of functional elements in the PLL are described. Next, PLL structures for modulation are discussed. Furthermore, several factors which impair PLL performance are explained too. Finally, some problems for practical semiconductor circuit designs for SoC and mobile terminal applications are described.

Then new PLL architecture and circuit design techniques for extremely low supply voltage is discussed in Chapter 3. In this Chapter, one solution for circuits especially suitable for such low supply voltage

and high frequency operation will be proposed.

In Chapter 4, on-chip PLL architectures for modulation and their detail circuits, especially a voltage controlled oscillator (VCO) in the PLL for SoC applications will be described. Here, two design examples will be discussed, one is the PLL with feedback loop modulation for spread-spectrum to reduce electromagnetic interference (EMI) and the other is a Gaussian frequency shift keying (GFSK) transmitter using two-point modulation.

Finally, in Chapter 5, PLL design methodologies for SoC and next trend of technical forecast for PLLs in future semiconductor process will be summarized.

Chapter 2

Conventional PLL integration techniques

2.1 Configuration of PLL

In this Chapter, a basic structure of PLL is explained. Firstly, a basic theoretical analysis of PLL based on a feedback loop theory including a stability issue is discussed. And then, details of practical PLL designs by using some examples of building blocks are introduced. Next one of the important features of the PLL, a modulator, will be discussed. Then problems and performance degradation factors are summarized in designing the practical PLL according to noise sources and other effects based on non-idealities of semiconductor circuits. Finally, requirements to PLL integration techniques are summarized by explaining some design examples of PLLs in SoCs and wireless transceivers.

2.1.1 Structure

PLL is a feedback loop to adjust both phases of an input reference clock and an output signal of a PLL. A PLL consists of a phase detector (PD), a

charge pump (CP), a loop filter (LF), a voltage controlled oscillator (VCO), and a divider (DIV). The construction of the PLL is shown in Fig. 2.1.1.

The phase detector compares phase difference between the reference signal (fr) and the feedbacked signal (fp) from the divider, and outputs control signals (UP, DN) which increase or decrease VCO oscillation frequency. Fig. 2.1.2 shows relationship between the two inputs, fr and fp, and the two outputs, UP and DN. When fr leads fp by Δ_1, the PD outputs UP, which pulse width is the same period of the phase difference between fr and fp. On the opposite condition, when fr lags fp by Δ_3, the PD outputs DN, which pulse width is also the same period of the phase difference between fp and fr. Therefore, the PD converts the phase difference of the two input signals to pulse width signals with polarity. Here the pulse width of the PD outputs is always the same period as the phase difference between the inputted two signals. Next, the charge pump converts the pulse width signals from the PD to an analog signal to control the VCO. The loop filter usually consists of a simple combination of resistors and capacitors. It is placed in front of the VCO to reduce noise from the PD and to maintain stability of the PLL.

The output of the VCO is then the output of the PLL and also feedbacks to the PD as the signal of fp. The feedback loop consists of the divider to reduce the clock rate. Here, the relationship between fp and fo is shown in

$$\mathrm{fp} = \frac{\mathrm{fo}}{N} \quad \cdots \quad (2.1.1),$$

because the divider divides phase by N, which is a divider's ratio.

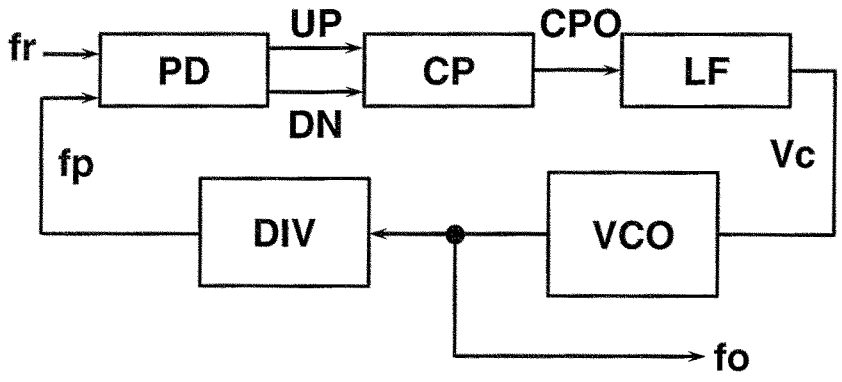


Figure 2.1.1 Construction of PLL

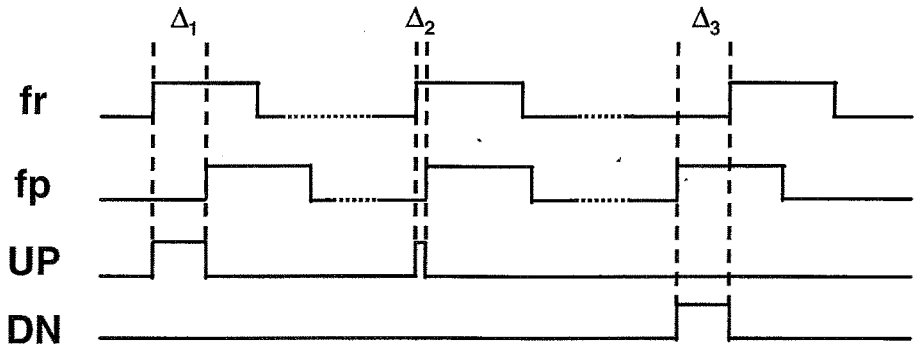


Figure 2.1.2 phase detector inputs/outputs

The feedback loop configuration shown in Fig. 2.1.1 controls Vc to become fr = fp, so fo is exactly the same value as N times of fr as shown in

$$fo = N \times fr \quad \cdots \quad (2.1.2).$$

2.1.2 Analysis for PLL performance

Fig. 2.1.3 shows an equivalent block diagram of the PLL which is shown in Fig. 2.1.1. Here, it is assumed that an equivalent gain of cascaded blocks of the phase detector and the charge pump, as Kp, and an equivalent gain of VCO's input-voltage to frequency conversion gain, as Kv. Furthermore, because the VCO has a function to convert frequency to phase, therefore, $1/s$ as an integrator of Laplace transform [8] is used as a model on the VCO. The divider model is $1/N$ because it scales relative phase difference by the factor of N.

$H(s)$ of the feedback loop which shown in Fig. 2.1.3 is

$$H(s) = \frac{\theta_{PLL}(s)}{\theta i(s)} = \frac{\dfrac{Kp\,F(s)\,Kv}{s}}{1 + \dfrac{Kp\,F(s)\,Kv}{N\,s}} \quad \cdots \quad (2.1.3).$$

$G(s)$ of the phase error transfer function using $\Delta\,\theta\,(s)$ becomes

$$G(s) = \frac{\Delta\theta(s)}{\theta i(s)} = \frac{\theta i(s) - \theta o(s)}{\theta i(s)} = \frac{1}{1 + \dfrac{Kp\,F(s)\,Kv}{N\,s}} \quad \cdots \quad (2.1.4).$$

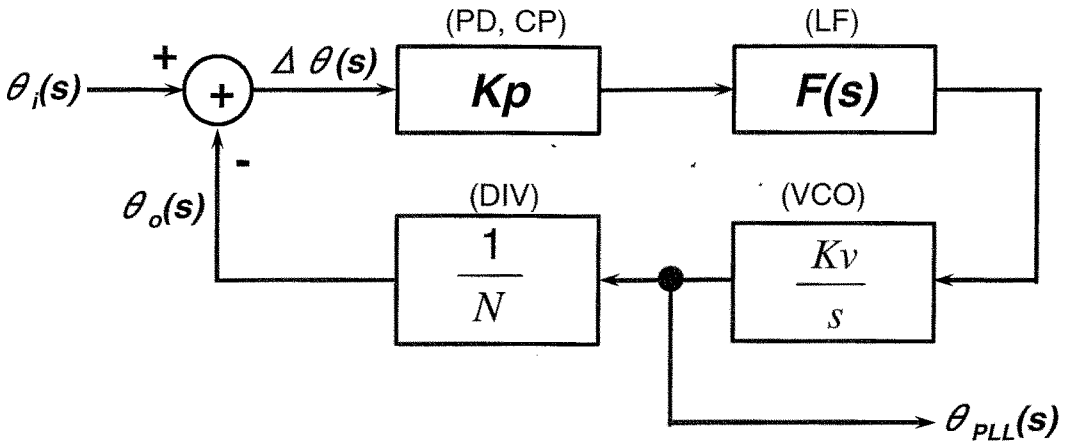


Figure 2.1.3 Equivalent block diagram of PLL

The PLL can be categorized as a number of integrators in the feedback loop, e.g. a first-order PLL, a second-order PLL, or a higher-order PLL. Especially, for the applications on clock generators in ICs, a second or a third-order PLL is usually adopted because it is easy to maintain stability in such a simple structure of the loop filter. Here, an analysis of the transfer function [9]–[13] is discussed by using a lag-lead type which has two integrators and one zero in the feedback loop.

A transfer function of a lag-lead type loop filter is shown in

$$F(s)=\frac{1+sCR_2}{1+sC(R_1+R_2)}=\frac{1+s\tau_2}{1+s(\tau_1+\tau_2)} \quad \cdots \quad (2.1.5)$$

where, we define $\tau_1=CR_1$, $\tau_2=CR_2$.

The error transfer function, *G(s)*, to an excess phase, which is derived from Eq. (2.1.4) and (2.1.5), given by

$$G(s)=\frac{1}{1+\dfrac{Kp\,F(s)\,Kv}{N\,s}}=\frac{s^2+\dfrac{s}{(\tau_1+\tau_2)}}{s^2+\dfrac{(1+\dfrac{KpKv\tau_2}{N})s}{(\tau_1+\tau_2)}+\dfrac{\dfrac{KpKv}{N}}{(\tau_1+\tau_2)}} \quad \cdots \quad (2.1.6)$$

where a lag-lead type filter is assumed to be used in a PLL.

Here, a denominator of Eq. (2.1.6) is named as a characteristic equation, which is a key design parameter to maintain stability of the PLL. Furthermore, Eq. (2.1.6) can be rewritten as

$$G(s)=\frac{s^2+\frac{\omega_n^{\,2}}{K}s}{s^2+2\zeta\omega_n s+\omega_n^{\,2}} \quad \cdots \quad (2.1.7)$$

where K, ζ, ω_n stand for a total loop gain, a dumpling factor, and a natural frequency, respectively. By comparing Eqs (2.1.6) and (2.1.7) K, ζ, and ω_n are related with Kp, Kv, N, τ_1, and τ_2 as $K=KpKv/N$, $\omega_n=\sqrt{K/(\tau_1+\tau_2)}$, $\zeta=(1+K\tau_2)/2\sqrt{(\tau_1+\tau_2)K}$. To evaluate these two parameters ζ and ω_n, stability of PLL can be analyzed easily.

2.1.3 Step response to excess phase

In this analysis, it is assumed that a step response to the excess phase, $\Delta\theta_i$, at the input of the phase detector is occurred at t=0. The step response of PLL, $\phi(t)$, is derived from an inverse Laplace transform of $\phi(s)$ which is given by

$$\phi(s)=G(s)\frac{1}{s}\Delta\theta_i \quad \cdots \quad (2.1.8).$$

There are three types of the step responses according to values of ζ. They are a) under dumping (ζ<1), b) critical dumping (ζ=1), and c) over dumping (ζ>1). Each response is expressed in Eq. (2.1.9), (2.1.10), and (2.1.11), respectively.

a) Under dumpling (ζ<1)

$$\phi(t)=\Delta\theta_i e^{-\zeta\omega_n t}\left[\cos\left(\sqrt{1-\zeta^2}\,\omega_n t\right)+\frac{\frac{\omega_n}{K}-\zeta}{\sqrt{1-\zeta^2}}\sin\left(\sqrt{1-\zeta^2}\,\omega_n t\right)\right] \quad \cdots \quad (2.1.9)$$

b) Critical dumping (ζ=1)

$$\phi(t)=\Delta\theta_i e^{-\omega_n t}\left[1+\left(\frac{\omega_n}{K}-1\right)\omega_n t\right] \quad \cdots \quad (2.1.10)$$

c) Over dumping (ζ>1)

$$\phi(t)=\Delta\theta_i e^{-\zeta\omega_n t}\left[\cosh\left(\sqrt{\zeta^2-1}\,\omega_n t\right)+\frac{\frac{\omega_n}{K}-\zeta}{\sqrt{\zeta^2-1}}\sinh\left(\sqrt{\zeta^2-1}\,\omega_n t\right)\right] \quad \cdots \quad (2.1.11)$$

These step responses, which are calculated by using various ζ, are showed in Fig. 2.1.4. The horizontal axis stands for time normalized by

ω_n, and the vertical axis does for phase error normalized by $\Delta\theta_i$. In the condition of the under dumping, the step response to the excess phase is not stable and shows ringing. On the contrary, in the case of the over dumping, the step response becomes slow but stable. In the practical PLL design, it tends to select ζ as a range of 0.5 to 0.7 to achieve good PLL performance in consideration of a trade-off between fast settling and stability maintaining.

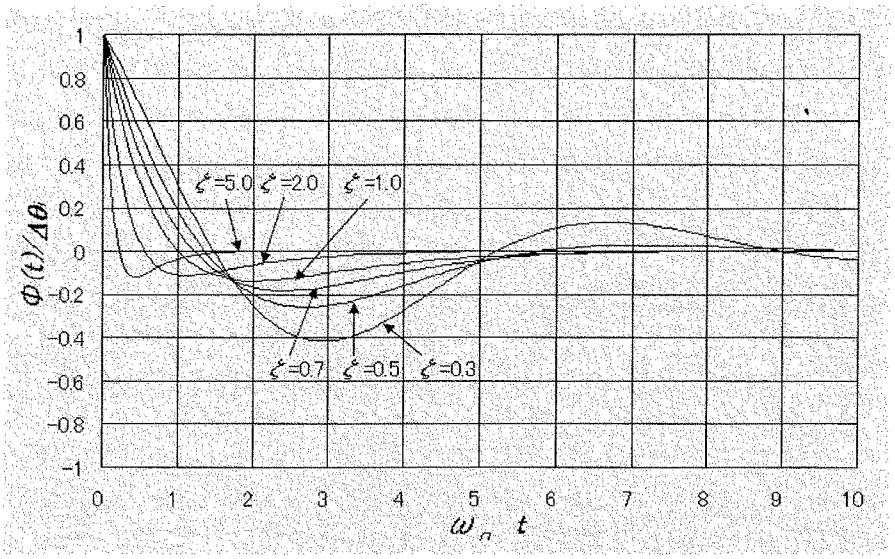


Figure 2.1.4 Step responses for various ζ

2.1.4 Functional elements in PLL

In this section, some examples of functional elements of PLL, such as the VCO, the phase detecter, the charge pump, and the loop filter are briefly explained.

a) VCO

VCO typically oscillates at a frequency when a feedback loop circuit of the VCO has a sufficient positive gain and 180° internal phase shift. Furthermore, oscillation frequency of the VCO should be controllable by at least one control signal from outside. In general, VCOs can be categorized into two types. One type is a circuit which uses a resonant circuit of inductance and capacitance, the other type is a circuit which consists of variable delays in the feedback loop. The most popular ones among VCOs

in CMOS large-scale integrations (LSI), such as a ring oscillator, a relaxation oscillator and a negative transconductance (g_m) oscillator using an LC resonator are explained hereafter.

i. Ring-oscillator type VCO

Fig. 2.1.5 shows a circuit diagram of the ring-oscillator type VCO. Here, a delay circuit (shown in dotted square) is based on an inverter circuit. To control delay time, usually current limiters of p-channel and n-channel MOS transistors (PMOS and NMOS) which are connected to a control signal Vc are inserted to both paths to VDD and ground level. The VCO is connecting odd stage delay circuits in series and is controlled its output frequency by changing bias currents of the current limiting transistors.

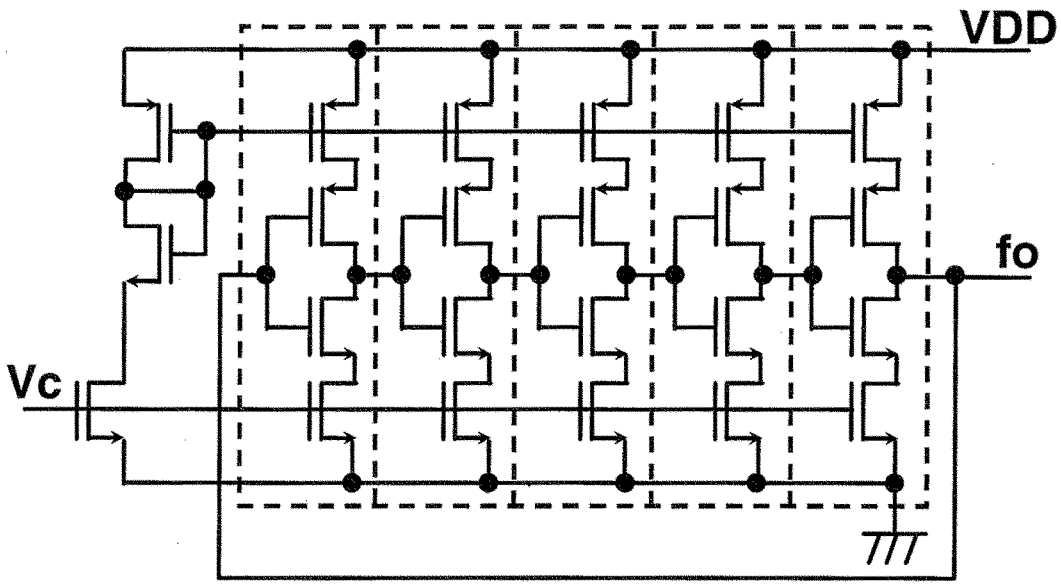


Figure 2.1.5 Example of ring-oscillator type VCO

ii. Relaxation-oscillator type VCO

A circuit diagram of the relaxation-oscillator (or it is sometimes called by a multi-vibrator) [14] is shown in Fig. 2.1.6. A control signal, Vc, is inputted to transistor M1 to be converted to Iv. Iv is transferred to a multi-vibrator block bias current via a current mirror circuit of M2 and M3.

The multi-vibrator block consists of switches of M4–M7, where

ON/OFF states are controlled by complimentary manner, capacitors of C1 and C2, two comparators to sense voltage difference between input level and reference level, and a set-reset flip-flop (SR-FF). When SR-FF outputs Q as "High", transistors of M5 and M6 are turned into ON state and charge C1 by Iv and discharge C2 simultaneously, where "High" and "Low" are assumed to be a logic level of true and false, respectively.

When a potential of Va is higher than that of *Vt*, the comparator outputs a reset signal R and then Q is transferred to "Low". At this condition, transistors of M4 and M7 are turned into ON state and charge C2 by Iv and discharge C1 simultaneously. To the contrary when potential of Vb is higher than that of *Vt*, the comparator outputs a set signal S and then Q becomes "High" again. Therefore, signals of Va and Vb are sawtooth waves whose maximum voltages are equal to *Vt*, as shown in Fig. 2.1.7. The oscillation frequency of the relaxation-oscillator type VCO is expressed by

$$\mathrm{fo}=\frac{1}{Tc}=\frac{1}{2(\frac{C\,Vt}{Iv}+Td)} \quad \cdots \quad (2.1.12),$$

where C1 and C2 are assumed to be equal to C and Td is a delay time of the SR-FF.

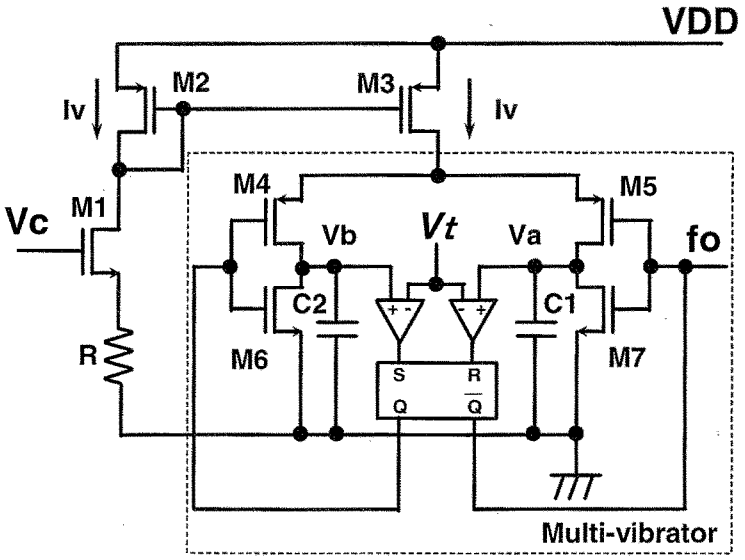


Figure 2.1.6 Example of relaxation-oscillator type VCO

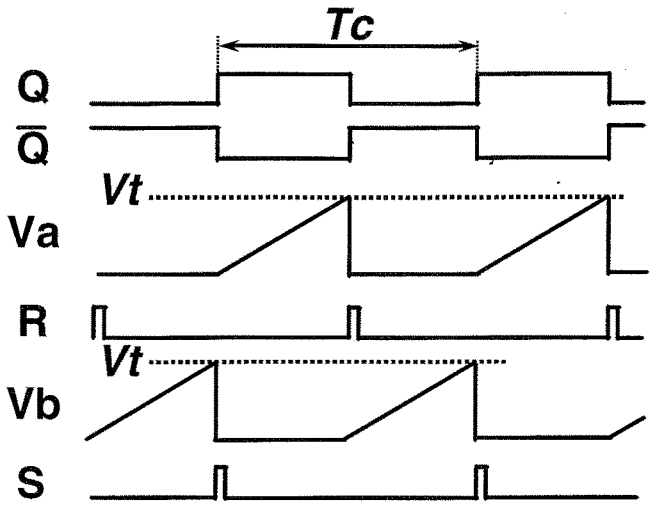


Figure 2.1.7 Time chart of relaxation-oscillator type VCO

iii. Negative-g_m LC-tank type VCO

It is well known that a tank of inductance (L) and capacitance (C) with a negative transconductance of feed-forward transistors oscillates at a quite stable frequency [15][16]. Therefore the negative-g_m LC-tank type VCO could achieve much higher quality factor (Q) and have better phase noise performance than those of other type VCOs. The negative-g_m LC-tank type VCO are adopted for various cell phones, a wireless local area network (LAN), and the other many kinds of transceivers which need to generate extremely low phase noise.

Fig. 2.1.8 shows an example of the negative-g_m LC-tank type VCO. A control voltage to vary its oscillation frequency, Vc, is connected to diodes, C1 and C2. Bias voltages of the diodes are derived from Vc and can vary p-n junction capacitance of them. An LC tank which consists of two inductors and two p-n junction capacitors oscillates at a resonance frequency of $\frac{1}{2\pi\sqrt{LC}}$, where C=C1=C2 and L=L1=L2 are assumed. The feed-forward circuit which consists of two transistors sustains oscillation of the LC tank and outputs amplified oscillation signal. Usually, the inductor is formed by a spiral pattern of aluminum layer in a silicon chip.

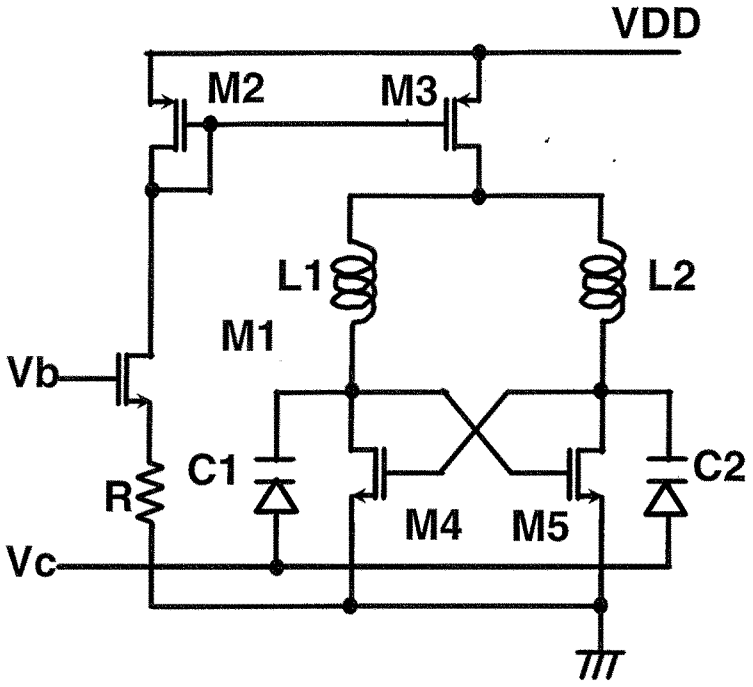


Figure 2.1.8 Example of negative-g_m LC-tank type VCO

b) Phase detector

A phase detector is a block to detect a phase difference between two inputs of the phase detector. There are two types of the phase detectors, one is a multiplier type and the other is an edge-detection type.

i. Multiplier type phase detector

The multiplier type phase detector is well known and has been adopted into many applications since the beginning of the PLL. A phase detection mechanism of the multiplier type phase detector is based on characteristics of a trigonometric function. Fig. 2.1.9 shows a relationship of inputs and an output of the multiplier type phase detector. The result of multiplication of two inputs ($\cos(\omega t+\theta)$ and $\cos(\omega t)$) is $\frac{1}{2}(\cos(\theta)+\cos(2\omega t+\theta))$, where ωt is a carrier frequency phase and θ is an phase difference between two input signals. The second term can be negligible because a loop filter at the next stage of the phase detector can eliminate it. This means that the PLL using the multiplier type phase detector settles at an input clock phase difference of 90°.

Fig. 2.1.10 shows an analog multiplier circuit diagram using bipolar transistors, which usually is called as a Gilbert cell. The multiplier type phase detector is usually adopted for applications which need to operate at extremely high frequency and are required to be low spurs level, e.g. for cell phones [17][18]. However the multiplier type phase detector needs to be adopted with a frequency adjusting method in parallel because it only generates a phase difference correctly if frequency difference between the two inputs is small.

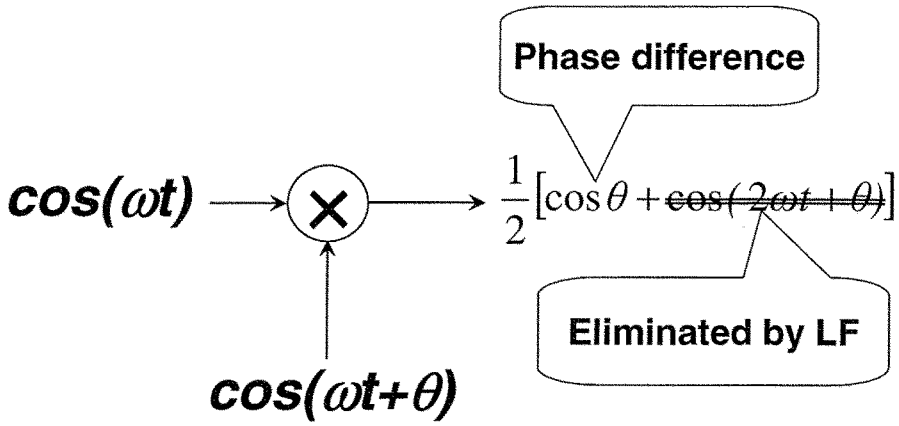


Figure 2.1.9 Input/output of multiplier type phase detector

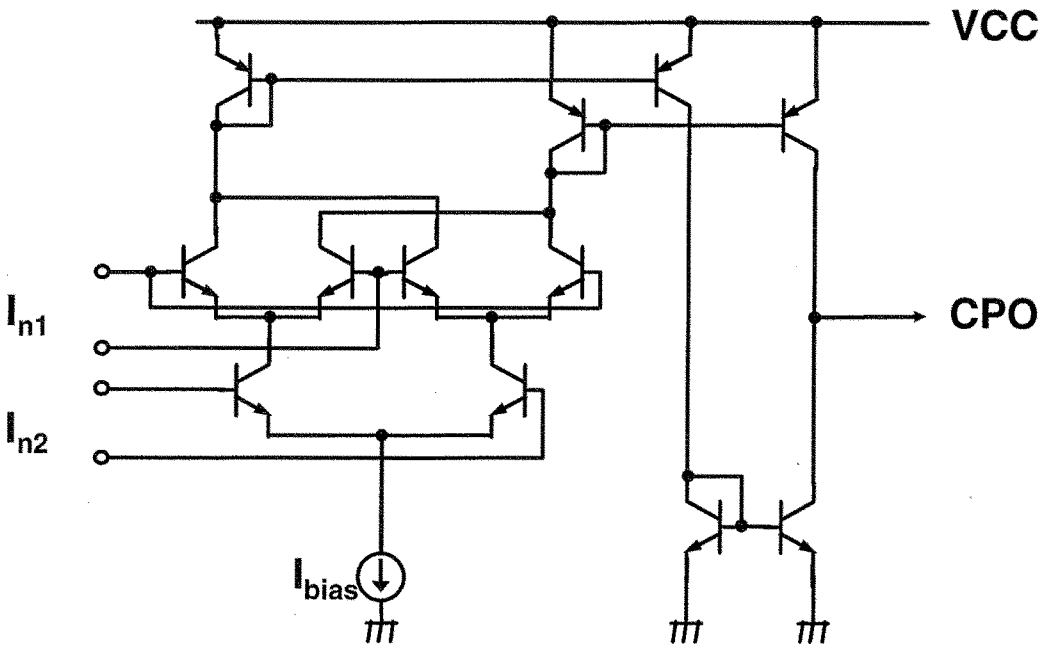


Figure 2.1.10 Example of multiplier type phase detector

ii. Edge-detection type phase detector

Fig. 2.1.11 shows a block diagram of the edge-detection type phase detector using four flip-flops. Each flip-flop consists of two NAND-gates. When a rising edge of fr is earlier than that of fp, the flip-flop which fr is inputted resets its output at a rising edge of fr and the flip-flop which fp is inputted remain "High". Then UP becomes "High" and DN is still "Low". On the other hand, when a rising edge of fp is earlier than that of fr, the flip-flop which fp is inputted resets its output at a rising edge of fp and the flip-flop which fr is inputted remain "High". Then DN becomes "High" and UP is still "Low". After rising edges of both signals of fr and fp have arrived, a 4-input-NAND-gate which is connected to flip-flops resets all flip-flops for preparation for next phase comparison. Consequently, UP and DN are shown in Fig. 2.1.2.

The phase detector shown in the Fig. 2.1.11 generates a phase difference only correctly when rising edges of fr and fp are occurred complementary. When frequency of fr is different from that of fp, rising edges are not arrived complementary. In this case, total period of UP = "High" is longer than that of DN = "High" when fr > fp, and total period of DN = "High" is longer than that of UP = "High" when fr < fp. Thus, the phase detector described above has a function to output average frequency difference between fr and fp. Consequently the phase detector also has characteristic of a frequency comparator. Therefore, this type phase detector is usually called as a phase-frequency detector (PFD) because it can detect not only phase difference but also frequency difference of the two inputs.

The important characteristic of the PFD is how narrow "dead zone" is. The PFD does not generate any output in the case of "dead zone" as shown in Fig. 2.1.12. The horizontal axis is phase difference from -2π to 2π and the vertical axis is a charge pump output current. A dotted line shows an ideal phase comparison characteristic and solid line shows practical one with "dead-zone."

If there is "dead zone" in the PFD, any phase errors do not feedback to VCO, and then VCO oscillates uncontrollably. Large frequency drift in PLL output is observed as if it is like an open loop condition. When VCO is entered into this condition, the output phase of the PLL is easily affected by noise from supply voltage or leakage current in an output of a charge pump. One of dominant factors to generate "dead zone" in the PFD is

disappearance of signals, UP or DN. When the phase difference between fp and fr is quite small, either UP or DN becomes extreme thin pulse shape and cannot drive charge pump transistors with enough margins because there are large stray capacitance of input transistors and wires to the charge pump, and then the pulse is vanished. Therefore the charge pump does not output the phase difference information according to the two inputs of the PFD.

To solve this problem, inserting a delay element at the output of the 4-input-NAND-gate (A) has already been proposed [19]. The output of this delay element which is inserted here resets timing of all flip-flops, then a pulse width of UP or DN becomes wider than that of the PFD without the delay element. Finally larger margin to prevent UP/DN pulse disappearance can be obtained.

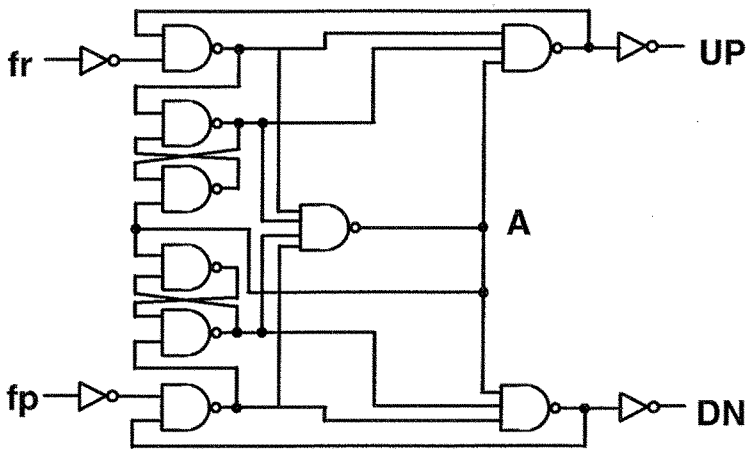


Figure 2.1.11 Example of edge-detection type phase detector

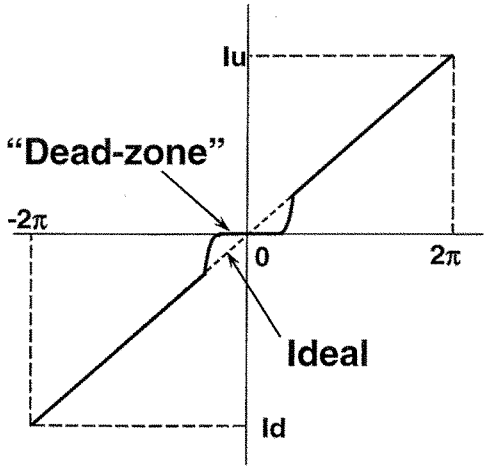


Figure 2.1.12 Dead-zone in phase detector

c) Charge pump

There are two kinds of charge pumps to be used mainly in practical PLL design. One is a voltage-output type and the other is a current-output type. The voltage-output type only consists of two switches. One switch is connected to a supply voltage and the other switch is connected to a ground. To increase a VCO frequency, the switch connected to the supply voltage is ON during the period of UP. On the contrary, to decrease it, the switch connected to the ground is ON during the period of DN. The other period when UP and DN is not "High", both switches are OFF to hold the output potential of the charge pump. Fig. 2.1.13(a) shows the circuit diagram of the voltage-output type charge pump. Here the switch to VDD is used by PMOS, so the gate signal of it is $\overline{UP}$.

The current-output type charge pump is shown in Fig. 2.1.13(b). Two current sources are inserted both paths to the supply voltage and the ground, respectively. These two current sources are controlled by a current reference of Ic. The method to control switches is the same as that of the voltage-output type charge pump. During UP="High", the current-output type charge pump sources a constant current into the loop filter. During DN="High", it sinks the same amount of the constant current from the loop filter. Here a polarity of the VCO voltage-to-frequency conversion is assumed to be positive.

Recently, to control VCO precisely, it is prefer to use the current-output type charge pump rather than the voltage-output type one for applications much severe jitter specifications.

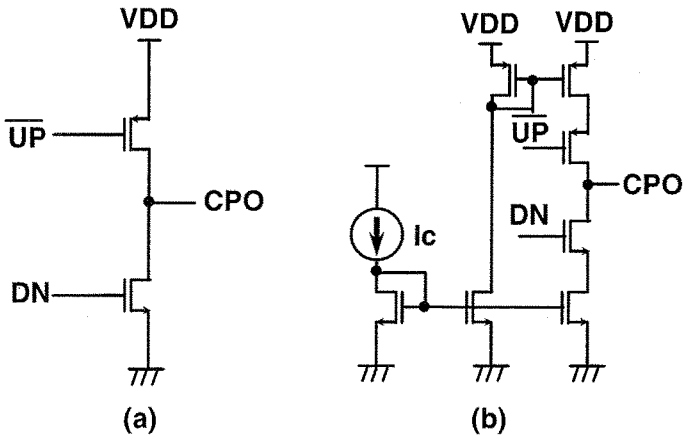


Figure 2.1.13 Examples of charge pump
(a) voltage-output type (b) current-output type

d) Loop filter

Examples of loop filters are shown in Fig. 2.1.14. Fig. 2.1.14(a) is usually called a lag-lead type loop filter and generates two poles in a PLL. Fig. 2.1.14(b) and (c) are usually connected with the current-output type charge pump [10]. The loop filter shown in Fig. 2.1.14(b) has two poles and one zero and (c) has three poles and one zero. Therefore, they generate three poles and four poles in a PLL, respectively. The higher order loop filters, which are shown in (b) and (c), can reject out-band noise sharply. From this reason they can be adopted for local signal generators in many cell phones.

Fig. 2.1.15 shows a loop filter using an auxiliary charge pump [20]. This loop filter does not need a resistors' process, therefore fabrication cost becomes lower than that of a PLL which needs resistors in CMOS process. The PD outputs of UP and DN, which are results of phase comparison between fp and fr, are inputted into both of the main and the auxiliary charge pumps. The main charge pump is connected to a capacitor C_1 and a voltage of C_1 is converted to a current signal by a voltage-to-current converter (VIC). Next, the output of the auxiliary charge pump is added to the output of the VIC. The closed loop transfer function of this feedback loop using the auxiliary charge pump is given by

$$H(s)=\frac{\omega_n^{\,2}+\dfrac{Kv\,Ig}{N}s}{s^2+2\zeta\,\omega_n^{\,2}\,s+\omega_n^{\,2}} \quad \cdots \quad (2.2.13),$$

where $\omega_n=\sqrt{\dfrac{Kv\,Ic\,g_m}{C_1\,N}}$, $\zeta=\dfrac{Ig}{2}\sqrt{\dfrac{Kv\,C_1}{N\,Ic\,g_m}}$.

The above equation has at least one zero in a closed loop transfer function. Therefore we can design PLL stable when we select appropriate parameters of *Ig*.

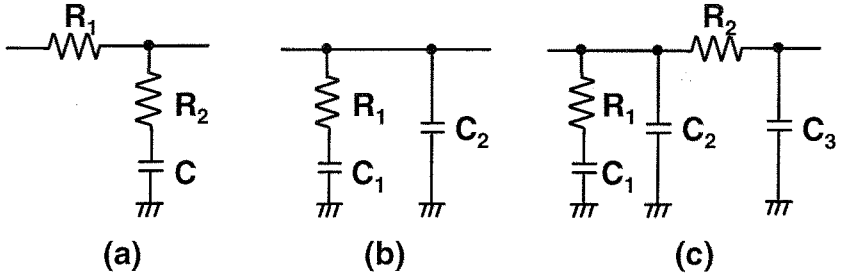


Figure 2.1.14 Examples of loop filter

(a) lag-lead type (b) 2-pole, 1-zero type (c) 3-pole, 1-zero type

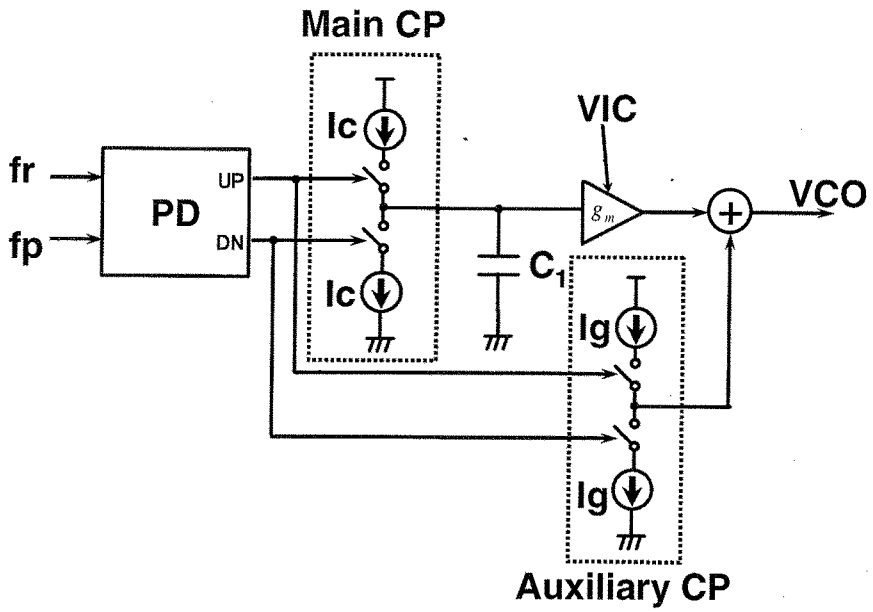


Figure 2.1.15 Examples of loop filter using auxiliary charge pump

2.2 Modulator using PLL

Many modulators using PLL have been proposed [17][21]. It is easy to turn the PLL into the modulator because the output phase of the PLL traces to a phase of an inputted modulation signal. Well, we can turn a PLL into a modulator by adding a modulation block (m) to any location within this feedback loop. Fig. 2.2.1 presents block diagrams of four modulators. In the diagrams, "m" represents the modulation signal. In general, PLLs consist of a PD, a CP, a VCO, and a DIV. The basic feedback loop of the PLL leads to the generation of a coherent frequency signal. The DIV is controlled by divisor, N. The output frequency (fo) is an accurate multiple of reference clock, fr.

The first choice for the modulator as shown in Fig. 2.2.1(a), is to insert an adder as a frequency modulator at the input of fr. This method [22] modulates the reference clock (fr) of the PLL and gives N times larger frequency shift than that of the inputted modulation signal to a VCO. Therefore, this method is usually called "input modulation."

Another possible insertion point for the adder in a PLL is shown in Fig. 2.2.1(b) [23]. Since the adder, which modulates frequency is inserted in front of the VCO, this technique is usually called "VCO modulation." It

can be used to achieve a wider modulation bandwidth compared to that of "input modulation," so it is used in many modulators, including those for Bluetooth transmitters [24][25].

Next, digital modulation in a feedback loop is shown in Fig. 2.2.1(c). The DIV is controlled by divisor, N. If N follows the inputted modulation signal, the result is a modulated signal can be obtained.

One of suitable applications for this feedback loop modulation is EMI reduction. This functional block is called a spread-spectrum clock generator (SSCG). Usually, clocks for operating logic gates inside integrated circuits are served from PLL. Of course, several kinds of PLL modulators can be utilized for generation of the spread-spectrum clock on-chip. However, the setups of the input modulation and the VCO modulation are based on analog techniques. Although both are simple, noise from digital circuits reaching the analog modulator creates jitter. Since a small amount of noise can create excessive jitter, analog modulation is not suitable for applications such as large-scale system-on-chip ICs because they generate large amounts of noise in digital signal processing.

On the other hand, the feedback loop modulation provides good linearity and is thus a strong candidate for use in the SSCG of serial advanced technology attachment (ATA) transceivers [26]. Michel et al. [27] were the first to report the use of a PLL with ΣΔ modulation in spread-spectrum generation. The EMI reduction achieved using their method is even better than using others. However, the ΣΔ modulator introduces noise components that provide an additional source of jitter. An output jitter of the spread-spectrum PLL was reported to be as large as 197 $ps_{p\text{-}p}$ [27] when the ΣΔ modulator was active. This means that it is very difficult to use this spread-spectrum PLL directly into much severer application, such as a spread-spectrum generator for a serial ATA transceiver because the jitter specification for the serial ATA should be lower than 12 ps. This jitter requirement is quite severe compared to that of an on-chip clock generator for normal logic circuits. Increased jitter is caused by a first-order ΣΔ modulator, which generates deterministic jitter, and rough frequency resolution caused by a single-bit output from the modulator to control the divider's ratio. Furthermore, these applications should be suitable for integration in many kinds of LSIs, so the clock generator must have good immunity to noise from digital circuits, be easy

to implement in CMOS process and have good portability in terms of feature size.

One alternative to the modulation using PLL is phase interpolation [28]–[30]. Here, a PLL generates a coherent frequency signal. The phase interpolation is applied to this coherent frequency signal by controlling the output phase of the phase interpolator. However, achieving a reasonable EMI reduction of around 5 dB [28] with the interpolation technique is rather difficult because the accuracy of integrated phase interpolators is not very high. Consequently, the feedback loop modulation is a good candidate for the SSCG application.

Finally, two-point modulation [31] is shown in Fig. 2.2.1(d). This modulator is a combination of the VCO modulation and the feedback loop modulation. A premise of this form of modulation is that the modulation indices on both paths, i.e. the direct VCO modulation path and the feedback loop modulation path in the PLL, are equal. The two-point modulation will not operate properly when the indices are different. Therefore the gain adjustment block, Adj.gain, is inserted in front of the VCO modulation.

The principle of modulation is now explained with the aid of Fig. 2.2.2. Fig. 2.2.2 shows Bode graphs of both of a closed-loop transfer function (lower of the figure) and an open-loop transfer function (upper of the figure) for PLL based on modulators which are shown in Fig. 2.2.1.

A transfer function of the input modulation and the feedback loop modulation are the same and is given by

$$F_A(s) = -\frac{H(s)}{1+H(s)} \quad \cdots \quad (2.2.1),$$

where we define the open-loop transfer function of the PLL as *H(s)* [32]. The frequency characteristics of *H(s)* are shown by the upper trace in Fig. 2.2.2. The cut-off frequency of the closed-loop transfer function is almost equal to the loop bandwidth, ω_c, of *H(s)*. Therefore the signal from the modulator (m) has a low-pass frequency characteristic with a cut-off frequency of ω_c (labeled A in Fig. 2.2.2). These modulators are not adequate for wide bandwidth modulation, such as Bluetooth and Digital Enhanced Cordless Telecommunications (DECT) transmitters.

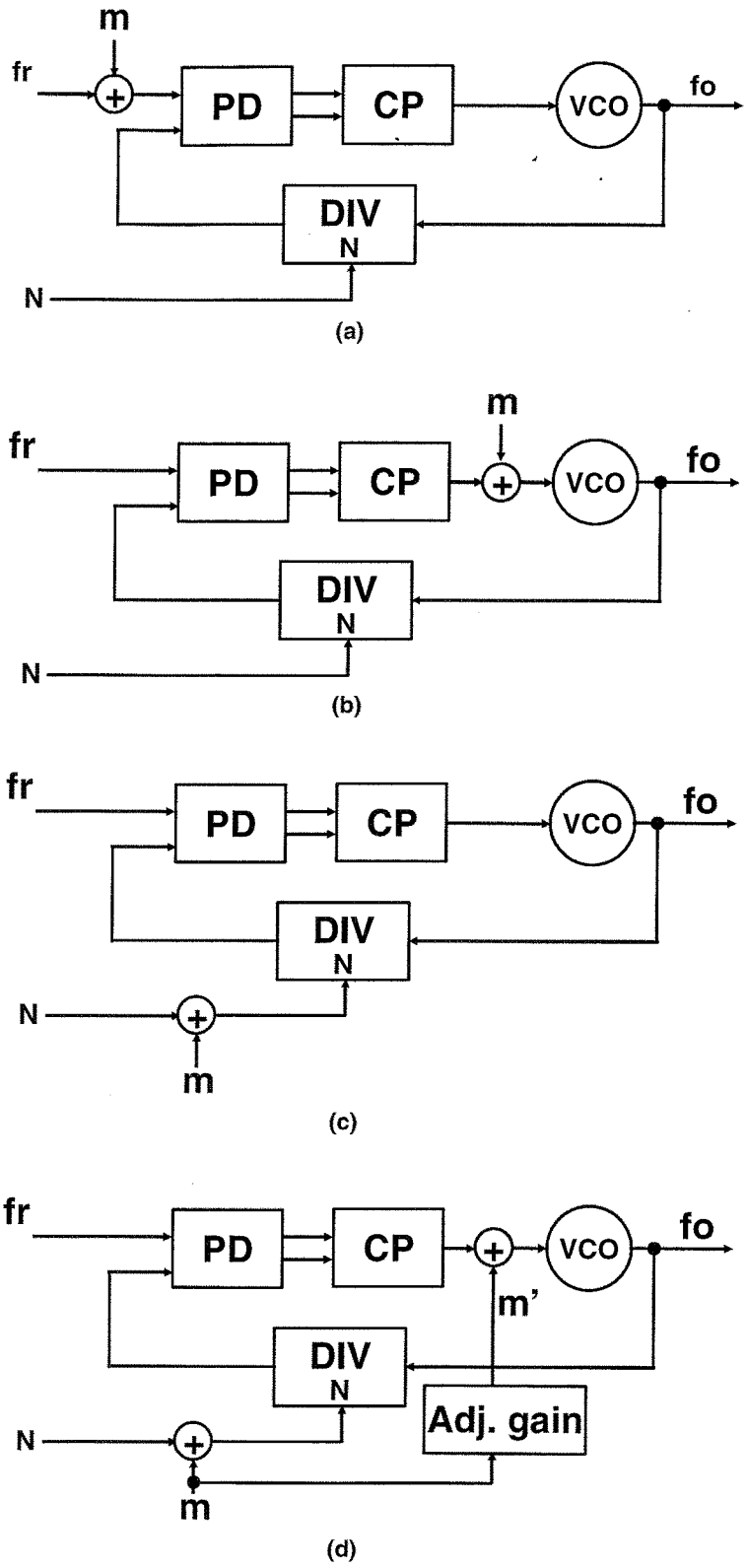


Figure 2.2.1 PLL modulation
(a) input modulation (b) VCO modulation
(c) feedback loop modulation (d) two-point modulation

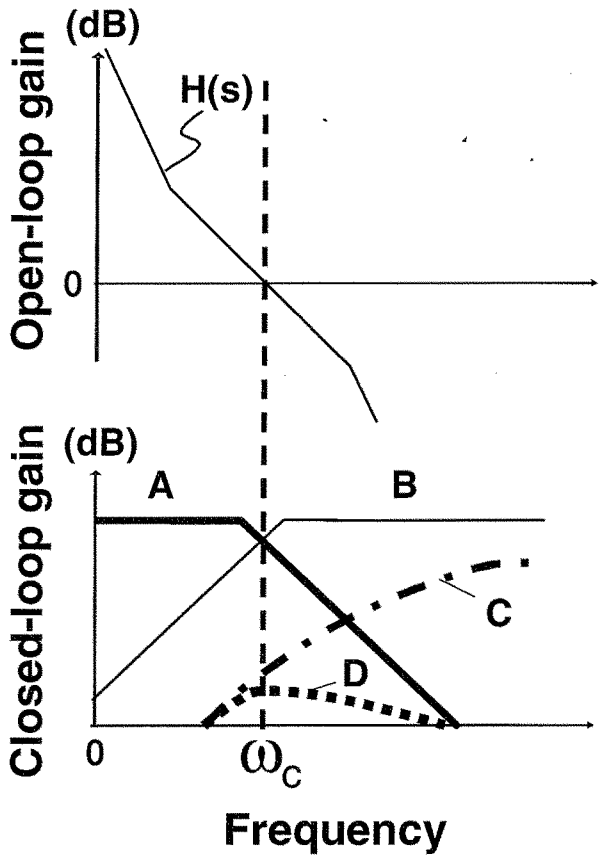


Figure 2.2.2 Frequency characteristics of two-point modulation

Next, a transfer function of the VCO modulation is given by

$$F_B(s)=\frac{1}{1+H(s)} \quad \cdots \quad (2.2.2).$$

So the signal from the modulator (m) for the VCO modulation has a high-pass characteristic labeled B in the lower trace of Fig. 2.2.2. Extremely low cut-off frequency of the PLL is necessary for this modulation.

A transfer function for the two-point modulation is almost flat when both gains of the VCO and feedback loop modulation are equal. Because the two-point modulation shown in Fig. 2.2.1(d) is a combination of both of two modulations described above, all-pass characteristics are obtained with respect to the signal input, since the transfer function is the superposition of the low-pass and high-pass characteristics for modulation on the two transmitter paths.

The other method to modulate wider frequency range signal has been

proposed as a feedback loop modulation [33] in which a frequency divider in the feedback path is controlled according to the modulation signal. However, this method needs a compensation technique to adjust the frequency characteristics of the PLL closed-loop transfer function because the PLL loop bandwidth is usually much narrower than the modulation bandwidth of the transmitter.

Compensation of frequency characteristics for the closed-loop transmission method requires a large gain in the high-frequency range, i.e. a differentiator or high-pass filter. Noise from the PLL will increase if we apply this technique to the transmitter. Moreover, determining the compensation characteristics is not easy, because the loop bandwidth of the PLL readily changes due to variation in the voltage-to-frequency conversion gain of the VCO and the charge pump current. Compensation is thus inadequate for applications that require highly precise modulation. Another example of a feedback loop modulation [34] requires two digital to analog converters (DACs) for separate correction of mismatches of the VCO gain and of the charge pump current, thus realizing precise modulation.

Therefore the two-point modulation described above is one of the practical choices for a continuous envelope modulation signal generator.

Next, a fractional counter is adopted into the feedback loop because it is a simple structure in digital circuits and the PLL with the fractional counter generates a clock with a precise frequency step. When a ΣΔ modulator is adopted into a controller of the fractional PLL, the ΣΔ modulator spreads the quantization noise $E(z)$ into the higher-frequency range. The transfer function $Y(z)$ of the noise processed by ΣΔ modulation is given by

$$Y(z) = E(z)(1-z^{-1})^N \quad \cdots \quad (2.2.3) \text{ [35]},$$

where, N and z^{-1} are assumed to be the order of the ΣΔ modulator and equivalent to the sampling period of the ΣΔ modulator, respectively. The frequency characteristic corresponding to Eq. (2.2.3) is labeled C in Fig. 2.2.2. The noise component is thus concentrated in the higher-frequency range. Although the output noise caused by this noise component is relaxed because multiplication by the PLL's low-pass frequency characteristic leads to the quantization-noise response labeled D in Fig. 2.2.2, this new noise component should be considered in designing modulators using PLLs.

2.3 Performance impairments on practical PLL

Impairments on PLL performance are (a) dead zone in a phase detector, (b) jitter from the reference clock, (c) VCO noise, (d) current or voltage unbalance in a charge pump, (e) leakage current in a loop filter, (f) flicker noise, and (g) noise from power supply. These non-idealities generate severe jitter in the PLL output clock. Here, the jitter is originally defined from uncertainty of clock phase. Fig. 2.3.1 overlays these noise sources of (a)–(g) into the PLL block diagram.

Then, factors of (a) and (b) described above can be treated as an equivalent noise component of PLL input side. Degradations from these two factors cannot be reduced by using PLL simple low-pass characteristic for excess phase variation. The factor of (c) is derived from a resonant quality factor of VCO. The factors of (d) and (e) generate phase mismatch between the VCO output and the reference clock, then consequently generate undesired spurs which are overtones of the reference clock. The factors of (f) and (g) for the phase detector and VCO mainly impair jitter performance. Especially, in the case of high sensitivity VCO, the factor of (g) causes a severe problem of the PLL output clock jitter.

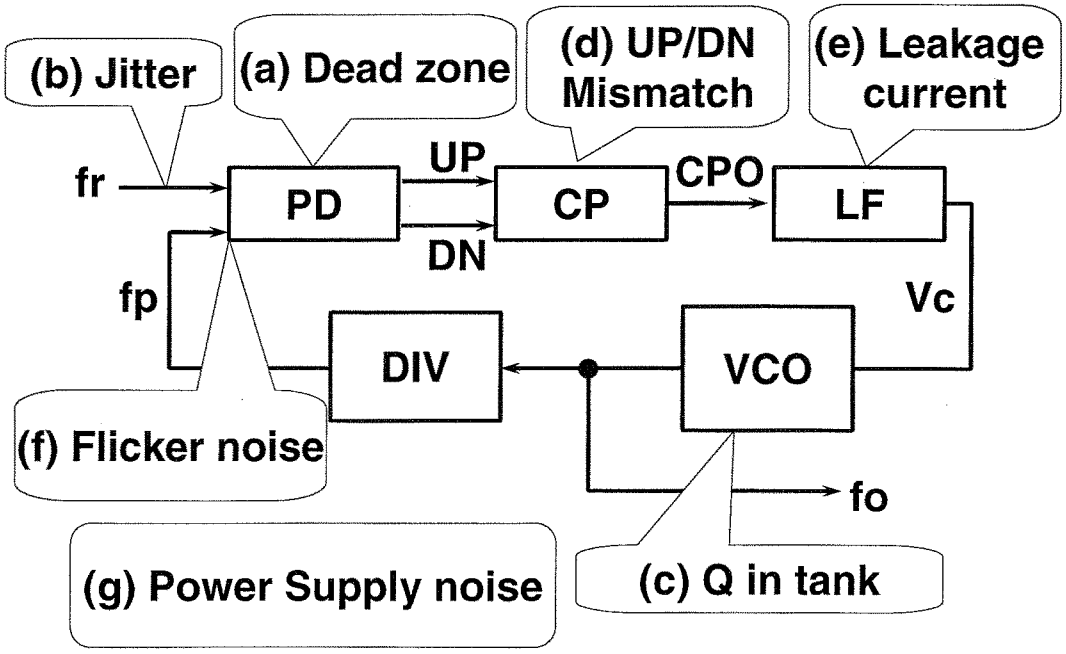


Figure 2.3.1 Noise sources in PLL

Each noise source in a PLL has different frequency characteristic depending on a node where noise sources are in a PLL. Fig. 2.3.2 roughly shows frequency characteristics for different noise sources, one is an input equivalent noise and the other is noise direct to the VCO. The noise sources of (a) and (b) can be converted to the equivalent input noise sources of the PLL, and then the frequency characteristics for them are low-pass as shown in Eq. (2.1.3). This low-pass frequency characteristic relaxes jitter in high frequency phase drift, however, a low frequency phase drift jitter is multiplied by N of the feedback divider.

On the other hand, the noise sources, (c) and (g), directly interfere into the VCO and modulate its output frequency. A frequency modulation caused by these noise sources can be suppressed by the large closed-loop gain of the PLL. However noise in high frequency may generate jitter because the open-loop gain is not sufficient.

Therefore, to improve PLL jitter performance when noise source frequency characteristics are dominant in low frequency phase drift, it is important to reduce noise level of the reference clock and non-ideality in the phase detector. Furthermore, it is more important to design the loop filter with larger suppression in high frequency. On the other hand, if dominant noise sources are located in high frequency, it is very important not only to design high Q in VCO but also to design high power supply noise rejection ratio (PSRR) in the VCO and its related circuits.

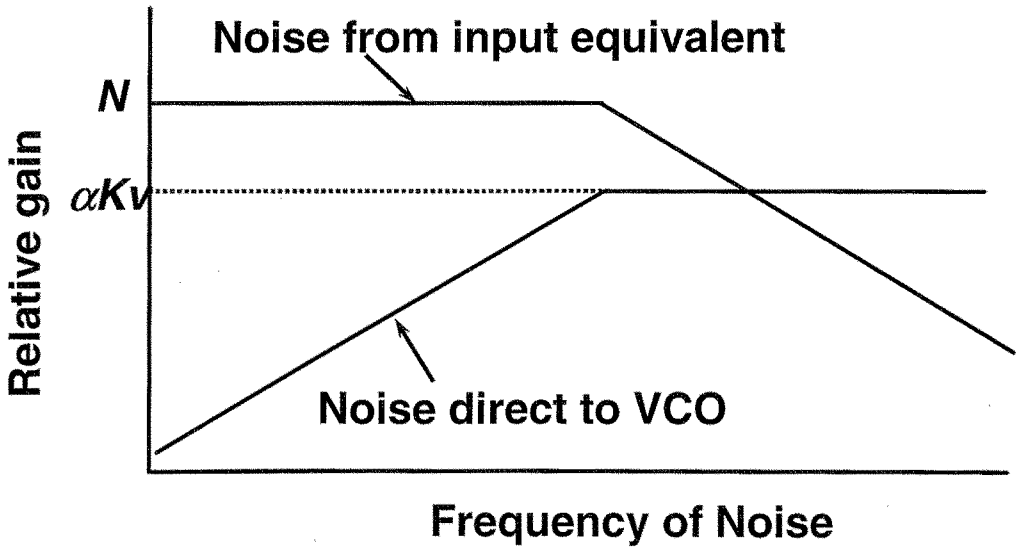


Figure 2.3.2 Frequency characteristics of noise sources in PLL

2.4 PLL requirements for system integrated circuits

It is very important for PLL designers to understand how a PLL is operating in a designed system. In this section, the examples of PLL applications in the field of SoC and wireless transceivers will be explained. Especially key techniques will be described for applications, e.g. a clock generator in microprocessors and micro wave frequency synthesizers for cell phones.

2.4.1 PLL requirements for SoC

A PLL in a microprocessor generates a high frequency internal clock signal of several hundreds mega hertz or much higher frequencies from a reference clock of a crystal oscillator which usually oscillates around several tens mega hertz. For this application, a divider ratio used in a PLL is about 20 and phase jitter required here is several hundreds of pico-seconds in peak-to-peak. To achieve lower jitter, it is important to reduce VCO jitter and design better suppression on a loop filter. For lowering jitter in a PLL, passive resistors and capacitors for the loop filter are often used. However, it is very important that the PLL for microprocessors should be integrated in a chip without any external passive components. To integrate all passive components, such as resistors and capacitors in the loop filter makes chip area larger and consequently total chip cost becomes higher. Therefore, some loop filters without necessity of a special resistor fabrication process in CMOS technology were adopted. This is a design trade-off in chip area and jitter requirements.

Another issue in PLLs for SoC is performance impaired by noise on digital circuitries. In some cases of the practical integrated circuits, noise in a PLL is due to supply voltage line layout, ground patterns, and bias node instability because of poor isolation to substrate nodes. This means that the PLL are suffered from noise, not only generated in an analog circuit itself but also in a digital circuitry. To solve these problems, many ICs are designed by using differential circuits and careful layout to reduce

unexpected noise coupling.

Furthermore, a finer design rule requires lower supply voltage because transistors designed with a finer design rule tend to have lower break down voltage. When we adopt a lower supply voltage in a semiconductor circuit, it makes head room for each transistor smaller and consequently becomes unavoidable poor dynamic range of the circuit. Then effective gain of amplifiers and their linearity are degraded. Especially, it is very difficult to maintain large positive gain in a VCO internal feedback loop at high frequency range. Then problems to halt oscillation of VCO might occur because the gain in VCO internal feedback loop is not enough to sustain oscillation.

Next, large leakage current in transistor OFF state in fine design rule processes affects an oscillation frequency range of VCO. It is very difficult to design enough frequency coverage for VCO because of this leakage problem. Techniques to stabilize VCO oscillation frequency for its leakage current variation are inevitable [36]. Furthermore, there are other issues of analog element variations which seriously affect performance of PLL.

In the near future it will be popular to use the third generation to the forth generation cell phone systems worldwide. Such cell phones include many features of multimedia signal processing, not only voice services. Therefore, these cell phones should integrate high performance processors with low power consumption. To meet this low power trend, using lower supply voltage is effective design strategy. Oscillation frequency vs. supply voltage level in International Solid State Circuits Conference (ISSCC) during recent years shows a supply voltage is gradually decline as low as 1 V or lower. For the next decade, it will be used by much finer design rule than 0.1 μm CMOS, transistors will have much lower breakdown voltage, and then lower supply voltage circuit techniques are significantly important issue for the design of the PLL.

2.4.2 PLL requirements for wireless transceivers

In general, the conventional PLL frequency synthesizers for wireless transceivers have been integrated in BiCMOS. The radio frequency circuits were implemented by bipolar transistors and base-band circuits, such as filters and variable gain amplifiers, were by CMOS transistors because bipolar transistors have good noise performance and better

current consumption for radio frequency range than those of CMOS transistors. However, to apply fine design rule into CMOS fabrication recently, there are rapid advancement in CMOS high frequency circuit designs. There are many reports of several GHz and higher frequency range transceivers with PLL synthesizers [37][38].

It is needed to use narrower channel bandwidth to achieve larger numbers of users in cell phone systems. For example, channel bandwidth for Personal Digital Cellular (PDC) in Japan and global systems for mobile communications (GSM) are 25-kHz and 200-kHz respectively. On this condition, it is necessary to set a divider number of PLL larger than 40000 to generate radio frequency (RF) signal higher than 1-GHz for cell phone applications. To realize a large divider number of PLL, synthesizers for cell phones uses a combination of a prescaler and a synchronous counter, which are named as a pulse-swallow counter. However, recently it is very popular to adopt fractional type dividers for synthesizers in up-to-date integrated transceivers [39].

When the divider's ratio is large, it is a problem that the input noise is amplified largely, and then it becomes dominant as a noise source of the synthesizer. Therefore, carefully design in PLL circuits and its layout to reduce degradations from such noise sources are needed.

Furthermore, phase noise requirement is quite severe and should be lower than 1° because the cell phone transmits digital data by using phase modulation (PM) to RF signals. To achieve lower phase noise, a Colpitts oscillator with an external inductor was employed as a conventional VCO. However, it is very difficult to reduce noise level interfered from the other circuits. The latest VCOs usually adopted a negative-g_m type on-chip LC resonant oscillator. They achieved significant low phase noise and are applicable to cell phones.

PLLs in cell phones are usually for generating pure local RF signals, however, for recent years, it is popular to minimize the number of external components in a PLL used in a transmitter. There have been reported many modulation methods using a mixer, however, the modulators using the PLL have an advantage of elimination for high-Q filters, such as surface acoustic wave (SAW) filters and a ceramic band-pass filters. For wireless transceiver standards, such as GSM, Bluetooth, and DECT, continuous envelope modulation (GFSK or Gaussian filtered minimum frequency shift keying: GMSK) are utilized because of high efficiency in an

output power amplifier. For continuous envelope modulation, changes in frequency or phase represent the transmitted data. Well-known ways of generating these continuous envelope modulation signals include heterodyne modulation [40] and direct in-phase/quadrature (IQ) modulation [41]–[45]. Both are already in common use. When these modulation techniques are adopted in a transmitter, the data for transmission is initially converted to I and Q elements, which are 90° out of phase with each other. The I and Q elements are then multiplied by local carrier waves at the several gigahertz radio frequency in two mixers, so the results also have a phase difference of 90°. After that, to avoid the generation of image-frequency components, the outputs of the mixers are added to each other by wired-OR connections. Although this method generates a modulated radio-frequency wave with small image-frequency components, it is not sufficient for the applications for cell phone transmitters, such as GSM. We need to insert a high-Q band-pass filter to eliminate spur and noise caused by the mixers.

In transceivers based on continuous envelope modulation such as those for GSM, DECT, and Bluetooth, however, these methods of modulation generate phase or frequency fluctuations according to the non-linear characteristics of the power amplifiers, i.e. amplitude modulation (AM) is converted to phase modulation. This AM–PM problem occurs with even a small mismatch in amplitudes of the I and Q elements, and is also caused by amplitude mismatches between local carrier waves. Furthermore, we must also consider a VCO frequency-pulling problem when using direct IQ modulation. Moreover, it is not easy to decrease power consumption in the transmitter because the modulation methods require mixers that operate in very high frequency bands.

On the other hand, VCO modulation is an alternative to these techniques and is used in transceivers, such as Bluetooth and DECT. This provides a very simple transmitter architecture that suits the generation of GFSK modulated signals. In this method, GFSK signals are transmitted while the PLL is cut out to open. The frequency-modulation signal or data for transmission is directly inputted to the VCO's frequency-control terminal. Of course, the PLL operates normally before transmission starts. That is, the circuit forms a closed loop and PLL frequency synthesis produces the carrier frequency for transmission.

The specified transmission bandwidth, for example, Bluetooth is about

±500 kHz, and is wider than the loop bandwidth of a typical PLL, which is several tens of kilohertz. Therefore, generating a Bluetooth GFSK modulation signal through the combination of a closed-loop PLL and VCO modulation is very difficult, because the frequency deviation is absorbed by the effect of the feedback loop of the PLL in the case of the repeated transmissions of either value, i.e. "High" or "Low".

A circuit for VCO modulation can be constructed by simply adding an analog low frequency circuit that controls the VCO control terminal to the original PLL synthesizer structure, and the circuit does not require the two radio frequency mixers of the direct IQ modulation method. A transceiver based on VCO modulation thus consumes much less power and has a smaller chip area than a transceiver based on direct IQ modulation. VCO modulation is thus adopted in many transceivers [25][46]–[49].

VCO modulation however generally suffers from a drift in the center frequency of transmission owing to supply-voltage fluctuation, noise on the VCO control terminals, and the leakage current of the charge pump and other components of the PLL's loop filter. Since the ground and power-supply lines of a small and cheap mobile transceiver are usually far from ideal, keeping the center-frequency drift within the required frequency range (less than 25 kHz) during a single-time-slot packet-transmission period in a Bluetooth transceiver is very difficult unless feedback loops are used. Since signals are transmitted to the antenna while the PLL is open loop in direct VCO modulation, a large center-frequency drift is caused by very low levels of noise or leakage at the VCO control terminal. It is not easy to avoid this center-frequency drift and to achieve good characteristics even when a circuit and a layout are carefully designed to reduce noise both inside and outside the integrated circuit.

Consequently, the two-point modulator, which was described in section 2.2, is suitable to be adopted into the transmitter with the continuous envelope modulation because of its wider modulation bandwidth. For designing the two-point modulator, we need to investigate how noise sources in the PLL affect to frequency spectrum of the transmitter in deeply consideration of its detail specifications.

Modulators using a PLL become very important technical issues currently because the transmitter using a PLL reduces number of external components and would have a good potential to achieve better

performance than that of the conventional modulator with mixers. It is well known that a PLL has frequency characteristics as a low pass filter. However, it was not popular to take advantage of this PLL's low pass frequency characteristics almost ten years ago. Recently strong requirements from users of eliminating external high-Q filters in transceivers are increasing. Then it is that such PLL's characteristic is gradually adopted in modulators and band selection filters for replacing the conventional ceramic or SAW filters. The PLLs for these applications need to generate a quite small phase noise and a wide phase modulation range, therefore it is very important to construct PLL using techniques to reduce jitter and signal processing noise.

2.5 Summarized requirements to PLL integration techniques

Based on the discussion in the section 2.4, the requirements to PLL and the problems to be solved are summarized as follows:

a) Low supply voltage for fine design rule process
   A finer design rule requires lower supply voltage because transistors designed with finer design rule tend to have lower break down voltage. We must solve the problem of poor dynamic range of the circuits when we adopt a low supply voltage.
b) Issues for applying PLL to modulators
   Number of applications of PLLs for modulators with band selection characteristics will be increasing. This technique can replace the conventional ceramic or SAW filters by an integrated PLL. Therefore, it is very important to construct a PLL with small jitter and signal processing noise.

Chapter 3

Low phase noise PLL implementation under low supply voltage

3.1 Introduction

A PLL has been widely used in microprocessor applications [50]–[52], where it plays roles of frequency synthesis [53], clock synchronization, and/or clock data recovery. Fig. 3.1.1 shows an example of a microprocessor floor plan with a PLL operating as a frequency synthesizer. All the building blocks in the PLL can be differently implemented depending on the desired system specifications like frequency synthesis resolutions, loop band width, output frequencies, etc. Nonetheless, their fundamental functions are the same and a typical PLL consists of a phase detector (PD), a charge pump (CP), a loop filter (LF), a voltage controlled oscillator (VCO), and a divider (DIV) on the feedback path as shown in Fig. 3.1.1.

As the design rule in CMOS process is becoming finer and finer every year, it is possible to integrate quite large amount of transistors in a single chip, such as a SoC, which usually consists of microprocessors,

analog functional blocks, and many kinds of peripheral interface blocks. These SoCs, especially used in applications for mobile must have low power consumption because they have to operate for a long time using only small batteries.

Furthermore, the supply voltage of SoCs has been gradually reduced by using finer CMOS design rules, because transistors in such fine CMOS does not have high break down voltage. Therefore it is very important that the key blocks, such as the PLL, the random access memory (RAM), etc., can all operate under a very low supply voltage. Of course, it is very effective to reduce the power consumption.

Next, it is also very important that SoCs operate at high speeds because small mobile terminals must deal with many complicated applications, such as video encoding and decoding, equalization, and error corrections, etc. Consequently, in the near future, SoCs in these applications will have to operate at high speeds, perhaps at 1-GHz or more frequencies using a very low supply voltage, e.g. 1.5, 1.0 V or lower. A PLL that uses such a low supply voltage is especially difficult to design because it would have to consist of so many complicate analog circuits.

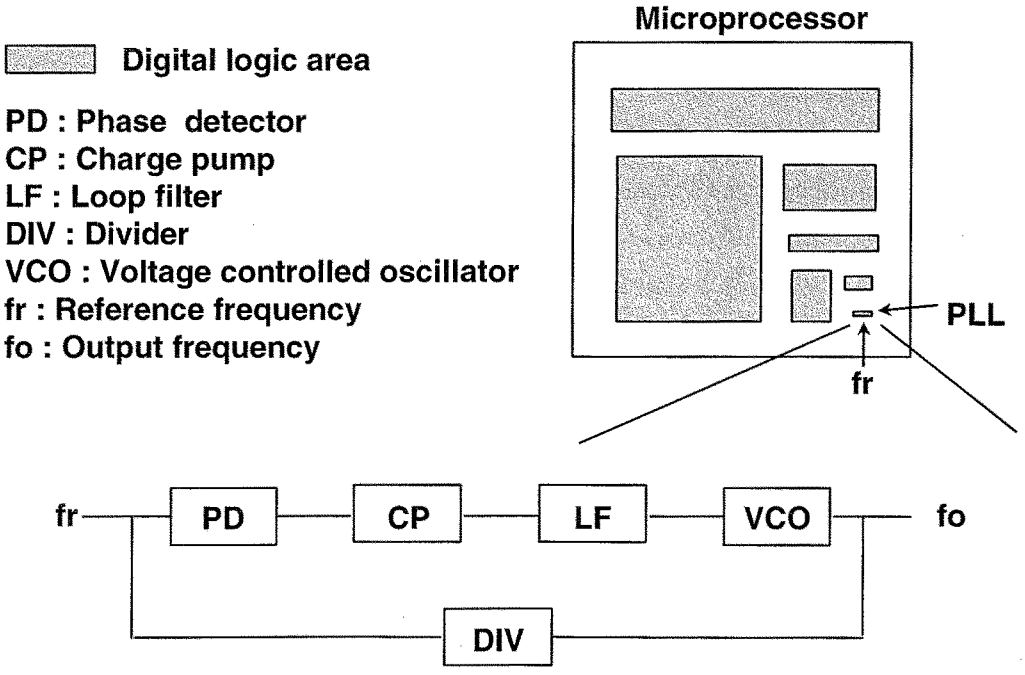


Figure 3.1.1 Example of a microprocessor floor plan with PLL operating as a frequency synthesizer

Recently, there have been several reports [54]–[57] of PLLs that can oscillate at higher frequency than 1 GHz. However, they need a supply voltage above 1.8V because it is very difficult to reduce the supply voltage level at the differential delay circuits of the VCO and the stacked current sources used in the charge pump. Based on the configuration of the PLL, the frequency capture range is limited mostly by the VCO frequency range and the charge pump output voltage swing [10][58]. Among the blocks, the VCO is a fundamental signal-generating block in the PLL. Conventionally, there are several ways to implement the VCO as an LC tuned oscillator, a relaxation oscillator and a ring oscillator. Although each method has its own pros and cons, for monolithic PLLs used in these low-voltage/low-power (LV/LP) applications, the ring oscillator has become the most popular choice due to its simplicity and compatibility with CMOS digital oriented process technology as well as small area overhead. In general, the VCO design requires careful consideration of several parameters, such as tuning range, timing jitter, and linearity of voltage-to-frequency conversion characteristic. Also, as the demand for portable and/or hand-held equipment in market has increased, LV/LP operation has become another important requirement [59].

In this Chapter, the LV/LP circuit techniques for a PLL are introduced. In section 3.2, the details circuits of building blocks such as a charge pump, a loop filter, and a ring-oscillator type VCO under low supply voltages are described. Especially because the VCO is the most critical block to design for the PLL, a design of VCO that uses new delay cells suitable for LV/LP operation will be proposed. PLL performance will be evaluated through measurements and simulation in section 3.3. Finally, in section 3.4, the important design technologies for LV/LP PLL will be summarized.

3.2 Building blocks of low supply voltage PLL

An LV/LP design for important building blocks of a PLL, a charge pump, a loop filter, and a VCO will be described in this section. They are (1) a charge pump using a switched current op-amp to reduce static-phase error and cycle-to-cycle jitter, (2) a phase margin that ensures the design method is independent of resistor variation of the semiconductor devices,

and (3) a VCO using a new delay cell which enhances the maximum oscillation frequency.

3.2.1 Charge pump feedbacked by switched current op-amp

One of the important building blocks of a PLL is a charge pump. Especially, unbalance of UP/DN step is a dominant jitter contribution in the PLL because such unbalance leads to increase in a static phase error between the input clock and the VCO output. The static phase error in the PLL outputs spurs from the VCO. However, a PLL with such the simple charge pump of switches and current sources as shown in Fig. 2.1.13 cannot avoid the static phase error because stray capacitors generate unbalance current between UP and DN signals and then it makes much worse static phase error.

A conventional method used to eliminate a static phase error caused by stray capacitors, Cs, of the charge pump was reported in Ref. [50] and its circuit diagram is shown in Fig. 3.2.1. It consists of two current sources (Ip and In), four switches (S1–S4), and an op-amp. S1 and S2 are switches for the charge pump to be connected to the loop filter, and S3 and S4 are dummy switches to operate ON and OFF complementarily to S1 and S2, respectively. The op-amp controls the node potential, V_{CPO}', between S3 and S4 so as to be as the same bias potential as the charge pump output, V_{CPO}. By keeping the bias potential at the node of S3 and S4 the same as V_{CPO}, current source output node potential, Vp and Vn, can also stayed at the same bias potential whenever S1 and S2 are ON or OFF.

However, the op-amp in this charge pump needs a phase compensation circuit because it is used as a buffer amplifier, whose gain equals to one. Usually, a phase compensation circuit limits the op-amp's bandwidth and requires the use of a large size capacitor. Therefore, the conventional method is inadequate to design a fast settling PLL frequency synthesizer of the type used in SoCs for mobile terminals. Here, we propose a new charge pump circuit using an op-amp with a switched current output stage, which does not need the phase compensation circuits.

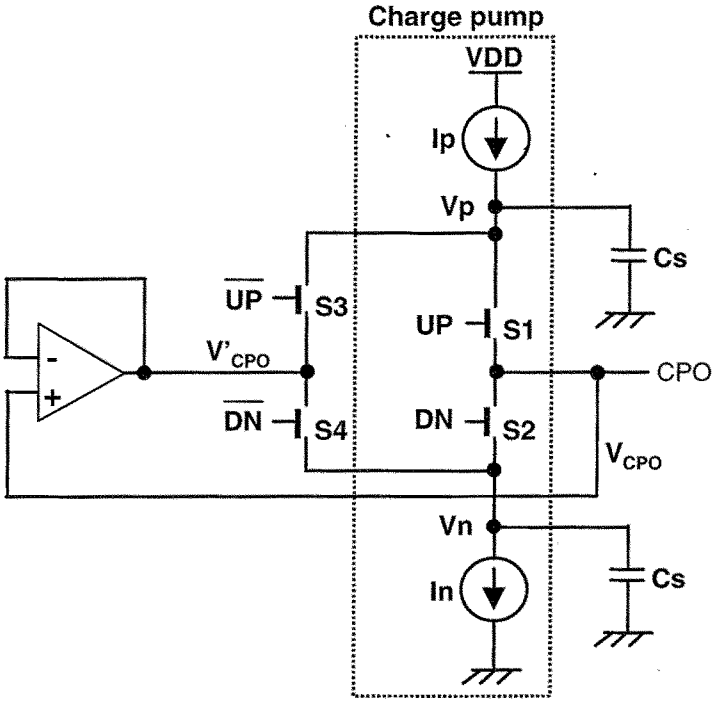


Figure 3.2.1 Conventional charge pump circuit

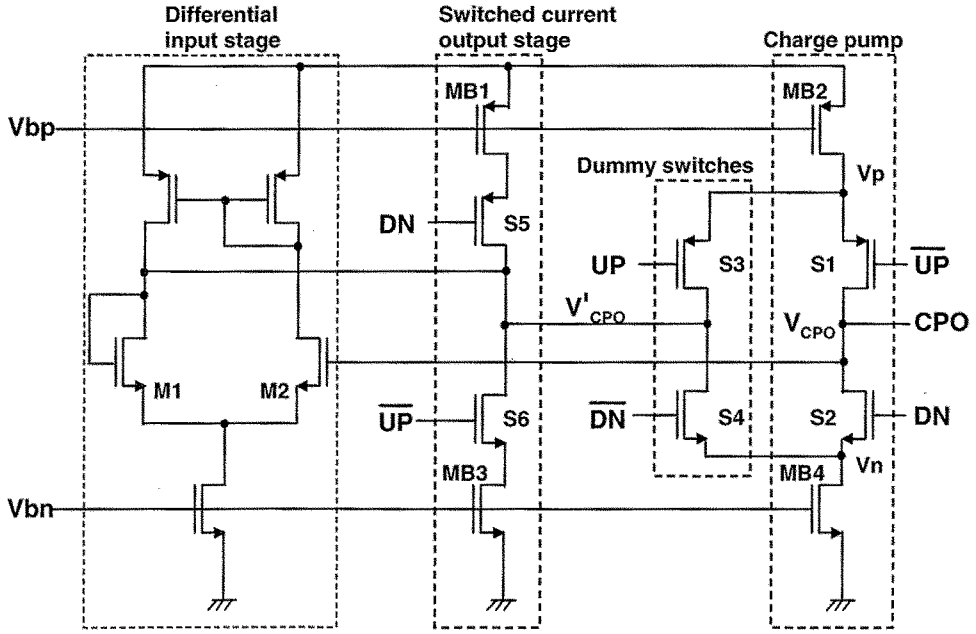


Figure 3.2.2 Charge pump with switched current op-amp

A charge pump circuit with the switched current op-amp is shown in Fig. 3.2.2. It uses the switched current output stage to the op-amp to control the bias potential, V'_{CPO}, to be the same bias potential V_{CPO}. The switched current op-amp consists of two stages, which are a differential input stage and a switched current output stage. The gain of the switched current op-amp becomes equal to one by connecting the drain and the gate of transistor M1 of the differential input stage. The output stage of the op-amp consists of two switch MOS transistors, S5 and S6, and two current source MOS transistors, MB1 and MB3, which are biased by Vbp and Vbn from a reference current source.

The charge pump charges or discharges capacitance of the loop filter according to the phase detector output signals UP and DN. There are four cases in this operation. When UP="High" and DN="Low", the current source transistor, MB2, sources the charge current into the loop filter because the switch S1 is ON. Furthermore, the current source transistor, MB1, sources a bias current into the transistor, MB4, through the switches S4 and S5. Therefore, MB4 is never cut off on this condition.

On the other hand, when UP="Low" and DN="High", the switch S2 is ON. On this condition, the current source transistor, MB4, sinks the discharge current from the loop filter, and the current source transistor, MB3 sinks a bias current from MB2 through S3 and S6. Therefore, MB2 is never cut off on this condition.

When UP="High", DN="High" or UP="Low", DN="Low", MB2 and MB4 does not cut off because the pairs of switches, S1 and S2, and S3 and S4, are ON and OFF complimentarily.

By adopting this output stage switching method, the use of phase compensation circuits for the op-amp is not necessary because the op-amp is a single-stage amplifier. Simulation results shows that DC gain of the op-amp is higher than 39 dB, and the unity gain frequency is higher than 540 MHz which is sufficiently wide for the fast settling PLL.

3.2.2 Loop filter with bias current compensation method

Usually, there is no special resistor process in a standard CMOS fabrication for a logic LSI, therefore, resistors should be composed of the same material as the gates of MOS transistors. In this case, a variation of resistor values may be very large. The resistor variation causes a phase

margin degradation of a PLL because the pole and zero locations of the feedback loop move owing to the resistor variation. Here, we propose a design methodology to relax the phase margin degradation by using a bias circuit that is inversely proportional to the square of the resistor value. In other words, a beta-multiply reference circuit is adopted to control the charge pump current in order to ensure the phase margin of the PLL.

A linear model of the general PLL is shown in Fig. 3.2.3. The PLL open-loop transfer function is

$$H(s)=\frac{I_C \cdot K_V}{2\pi N}\times\frac{1}{s^2}\times\frac{1+sC_SR_S}{sR_SC_SC_P+C_S+C_P} \quad \cdots \quad (3.2.1),$$

where Kv is the "gain" of a VCO (specified in Hz/V), Ic is the charge pump current, N is the devider ratio, and R_s, C_p, and C_s are loop filter componet values shown in Fig. 3.2.4. Two ploes are located in DC, and the dominant pole and the zero are expressed as,

$$P_3=\frac{C_P+C_S}{R_SC_SC_P}\approx\frac{1}{R_SC_P}, \quad (C_S >> C_P) \quad \cdots \quad (3.2.2),$$

$$Z_1=\frac{1}{R_SC_S} \quad \cdots \quad (3.2.3).$$

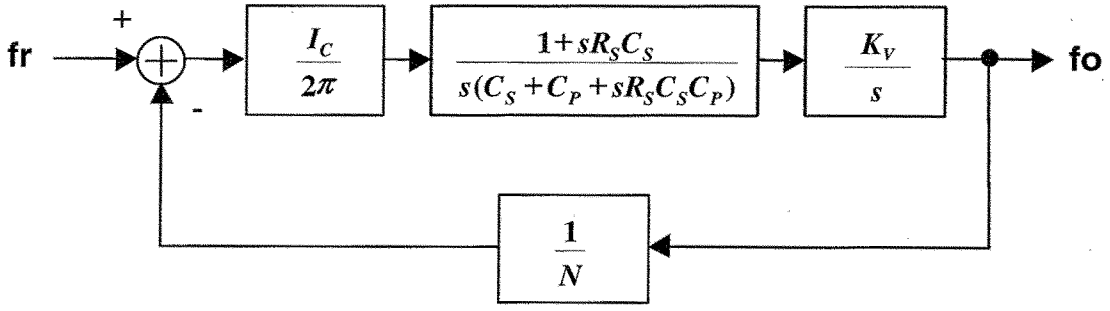


Figure 3.2.3 General PLL linear model

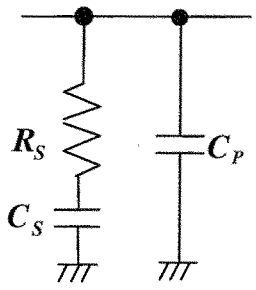


Figure 3.2.4 Loop filter (2-pole, 1-zero type)

To maximize the phase margine, we set the pole-zero ratio as

$$\frac{\omega_u}{Z_1}=\frac{P_3}{\omega_u}=A \quad \cdots \quad (3.2.4).$$

Here, ω_u is a unity gain frequency of the open-loop transfer function. Therefore, the phase margine, P_m, of the open-loop transfar function is expressed as

$$P_m=\tan^{-1}\left(\frac{A^2-1}{2A}\right) \quad \cdots \quad (3.2.5).$$

Next, we consider the phase margine degradation where the variation of resistivity of the gate material is included. From Eqs. (3.2.2) and (3.2.3), phase of open-loop transfer function is inversely proportional to R_s. Therefore, Eq. (3.2.4) holds only when

$$G_p' \times G_z' = 1 \quad \cdots \quad (3.2.6)$$

is satisfied, that is ω_u also inversely propotinal to R_s, where G'_p and G'_z are the gain at pole and zero after the resistivity varies, respectively. However, from Eqs. (3.2.1)–(3.2.3), G_p and G_z are propotional to R_S^2. Thus, Eqs. (3.2.4) and (3.2.5) are not satisfied and phase margine, P_m, degrades.

The degraded phase margine, P'_m, is shown as

$$P'_m=\tan^{-1}\left(\frac{A^2-1}{A}\times\frac{1}{\frac{(R_S+\Delta R_S)^2}{R_S^2}+\frac{R_S^2}{(R_S+\Delta R_S)^2}}\right) \quad \cdots \quad (3.2.7),$$

where R_s is the nominal value and ΔR_s is the variation from the resistor's nominal value of the loop filter. For example, when the fastest settling parameter, A=2.7, is selected for the loop filter design [60], the phase margin of the PLL degrades from 49° to 29° in case of $\Delta R_s/R_s$ = 0.5. By considering the other phase margin degradation factors such as K_V variation to the temperature and the threshold voltage of the MOS transistors, etc., the PLL might be found unstable in the worst-case scenario of the mass production.

We propose a stability technique for the PLL that can ensure that there is sufficient phase margin to counteract the resistivity variation. Fig. 3.2.5 shows the Bode graph of the open-loop transfer function. Here, we consider two kinds of resistor values: one is the nominal, Ro, and the

other is that with a resistor's variation, $Ro+\Delta R$.

We designed a current reference circuit for the charge pump, for which the current varies in inversely proportion to a square of $(R_s+\Delta R_s)^2$. As shown in Fig. 3.2.5, the zero, Z_1, the pole, P_3, and ω_u are equally shifted to Z'_1, P'_3, and ω'_u on a frequency axis, when the resistor value is changed from Ro to $Ro+\Delta R$.

Consequently, the phase margin of the PLL can be maintained whether the resistance variation is included or not. The pole zero placing method described above has ω_u dependency to a resistor value. However, its effect is not so severe to the unity gain-frequency variations of the applications in the PLL frequency synthesizers of microprocessors because the PLL settling time is much faster than that of the microprocessors. Hence, use of this method is very effective for maintaining the phase margin independent of the resistance variation.

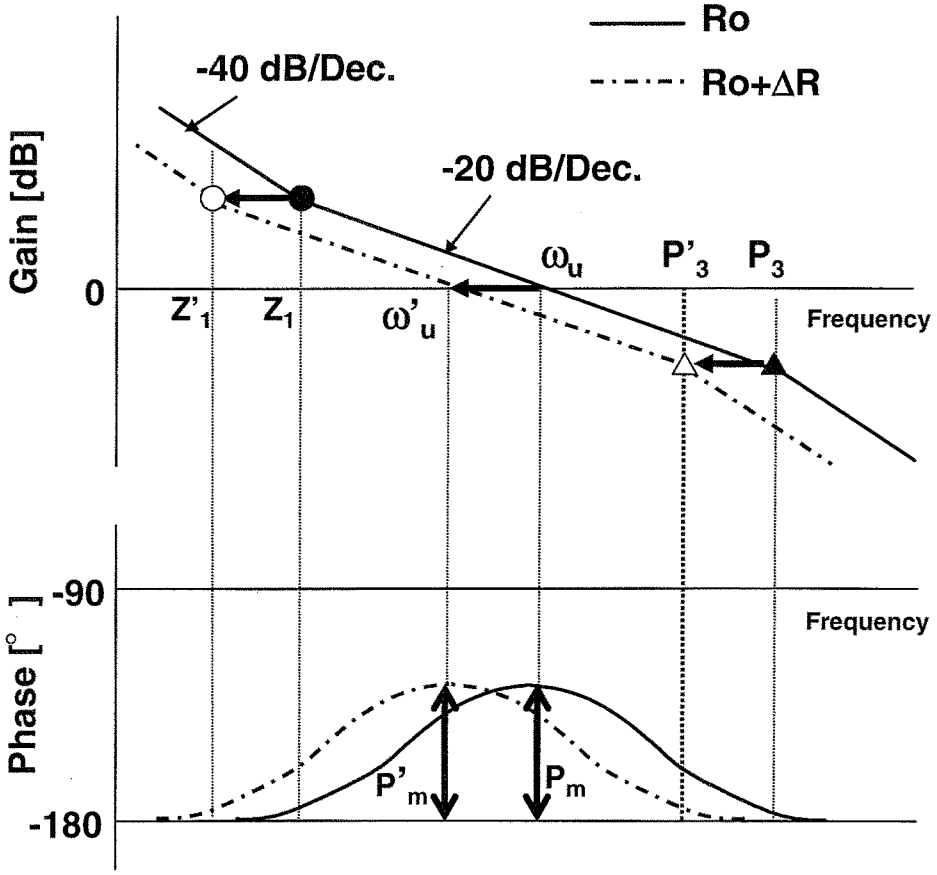


Figure 3.2.5 Bode graph of PLL open-loop transfer function

We adopt a beta-multiplier referenced self-biasing circuit [61], which is shown in Fig. 3.2.6, as the bias circuit for the charge pump. The beta multiplier referenced self-biasing circuit generates a reference current in inversely propotional to a squre of the variation of resistivity. It consists of two different size transistors, M6 and M7, two transistors for the current mirror, M4 and M5, start-up cicuits, M1–M3, and a bias resistor, R_b. When $(W_6/L_6) : (W_7/L_7)=1:K$, and K is larger than 1, the reference current I_{ref} is expressed by

$$I_{ref} = \frac{2}{\beta_{M6} R_b^2}\left(1-\sqrt{\frac{1}{K}}\right)^2 \quad \cdots \quad (3.2.8),$$

where β_{M6} is a g_m of the transistor M6. Therefore, I_{ref}, which is in inversely proportional to the square of variation resistivity, is fed to the charge pump shown in Fig. 3.2.2 by connecting Vbn and Vbp, respectivity.

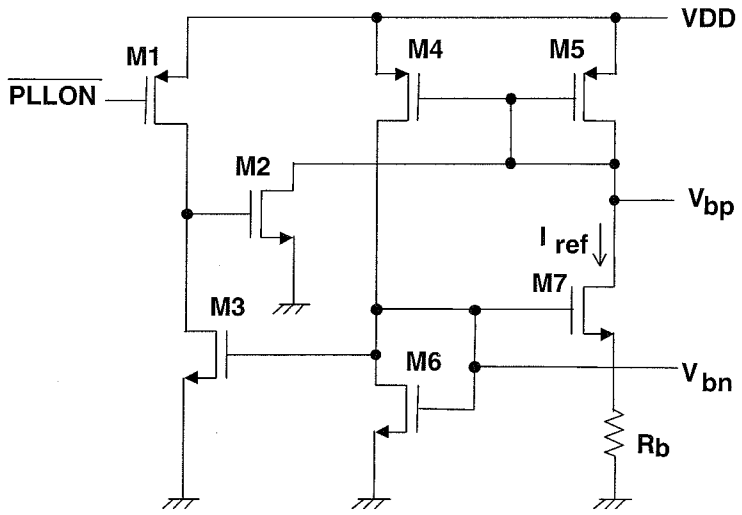


Figure 3.2.6 Bias current for charge pump

3.2.3 Current controlled feed-forward VCO

A VCO is the most important component of the PLL. However, it is very difficult to achieve both a low supply voltage operation and a high frequency oscillation because the stacked transistors of the VCO prevent high-speed turn-off and turn-on under a low supply voltage.

In this section, we will firstly explain about VCO with a feed-forward technique in a delay cell by referring to Ref. [62] and then will investigate

its operation and maximum oscillation frequency limitation. Finally an improved high frequency VCO with a new feed-forward in delay cell will be proposed.

The VCO which proposed in Ref. [62] shown in Fig. 3.2.7 consists of three delay cells and a differential converter. The VCO control signal, Vc, is inputted into the differential converter and is converted into two complementary control signals (Vcp, Vcn) for the delay cells. Here, this differential converter acts as a V-I conversion (VIC). The three delay cells are connected in a positive feedback-loop manner. The outputs of the third delay cell are inputted into a differential amplifier and are converted into a single-ended signal, fo.

The ring oscillator contains three delay cells connected in cascade with a total phase shift of 180° in a feedback loop. The delay cell can be realized in various forms [12][20][63][64], and their delay can be controlled by using different signal forms, i.e. voltage or current. Our delay cell is a differential-type, current-controlled delay amplifier, that is, the output oscillation frequency of the oscillator is linearly proportional to the input control current. This structure is usually called by a current control oscillator, CCO.

Since the available control signal in a system is voltage and the ring oscillator is current-controllable, the V-I converter with the linear voltage-to-current characteristic is required prior to the ring oscillator. Note that in some cases a delay cell does not require a V-I converter to control its frequency. For example, an LP/LV VCO with a delay cell using two consecutive differential pairs achieves good linear characteristics between input control voltage and oscillation frequency without a V-I converter [65]. In this circuit, however, the output pulses have potentially duty unbalance problem unless all cells perfectly match, that is, three consecutive output pulses (in this example) could have different pulse period and each of them with different duty cycle. Moreover, it requires complicated output circuits which cause jitter at PLL output. On the contrary, our differential delay cell adopts a simple positive feedback to increase actual gain of the cell, which makes high frequency LP/LV operation possible. Hereafter, the designs of the V-I converter and differential delay cell will be explained.

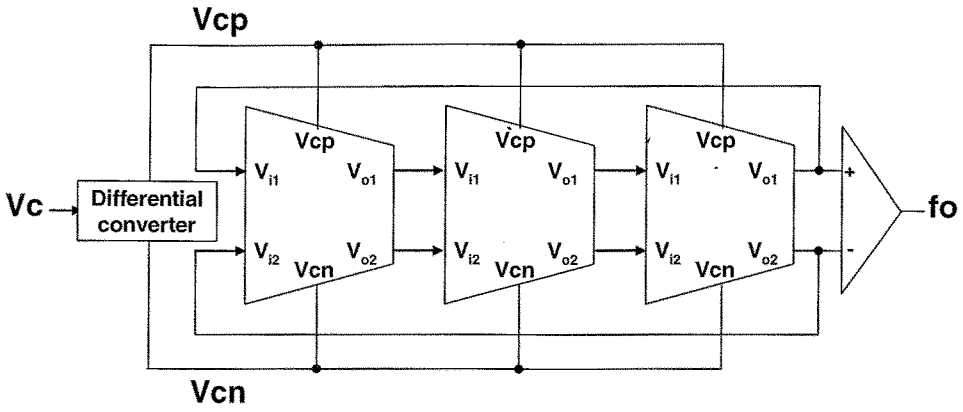


Figure 3.2.7 VCO block diagram

(a) V-I converter

Many different VICs have been developed in the literature, all of which have highly linear V-I characteristic. In the design of the VIC in PLL, however, the noise is another major concern, in addition to the linear characteristic. This is because the noise affects oscillation frequency in the form of the timing jitter, which might cause microprocessors or other digital circuit blocks to malfunction. Therefore, the intrinsic noise of MOS devices must be minimized. One effective way to reduce such noise is to keep the total number of transistors small in the VIC and its structure simple so as to achieve low noise and the good linearity simultaneously. This allows LV/LP operation as well.

Fig. 3.2.8(a) shows one of the simplest VICs implemented with bipolar transistors and a resistor, and its MOS counter part is shown in (b). Applying Kirchhoff's voltage law around M3 ($KM3$) and R in (b) gives us an equation,

$$\sqrt{\frac{I_{V-I}}{KM3}} + I_{V-I} R + V_{TH,N} = V_C \quad \cdots \quad (3.2.9),$$

where $V_{TH,N}$ is the threshold voltage of an NMOS transistor.

If we ignore $\sqrt{\frac{I_{V-I}}{KM3}}$ in Eq. (3.2.9) by making $\sqrt{\frac{I_{V-I}}{KM3}} \ll I_{V-I} R$ (it is possible with large values of $KM3$, R, and I_{V-I}), Eq. (3.2.9) can be simplified to

$$I_{V-I} = \frac{V_C}{R} - \frac{V_{TH,N}}{R} \quad \cdots \quad (3.2.10).$$

Hence, the output current I_{V-I} becomes linear to the input voltage V_C, expressed as

$$I_{V-I} \propto g_m V_C, \quad \cdots \quad (3.2.11),$$

where g_m is transconductance equal to $\frac{1}{R}$.

The upper plot in Fig. 3.2.9 depicts this result with different $KM3$ and R. As $KM3$ and R increase, the output current curve becomes more linear. The lower plot in Fig. 3.2.9 shows the slope (transconductance) of the output current curves in upper plot of Fig. 3.2.9. In the case of $KM3$=60 mA/V and R=1 kΩ, linear transconductance of the VIC is obtained over wide input control voltage range. It is worth to note that the large $KM3$ (that is, wider M3) does not cause severe silicon area penalty. In our (and also, conventional) PLL structure, the loop filter placed just prior to the VIC, composed of two CMOS capacitors (C_p and C_s) and one resistor (R_s) as shown in Fig. 3.2.10. The parasitic capacitance, C_{M3} due to the gate-source capacitance of the M3 can be lumped into C_p. Thus we can keep the total silicon area consumption, which is almost equivalent to $C_p \fallingdotseq C_{p1}+C_{M3}$, constant by reducing the size of C_{p1} when M3 (and thus C_{M3}) is large and the series resister, R, is much smaller than R_s, and vice versa.

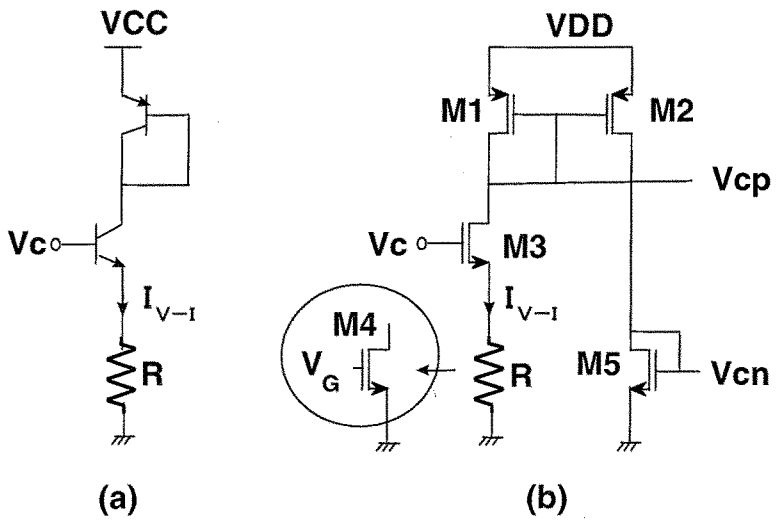


Figure 3.2.8 Examples of voltage-to-current converter
(a) simple VIC with bipolar transistor and resister
(b) bipolar and resister are replaced by MOS

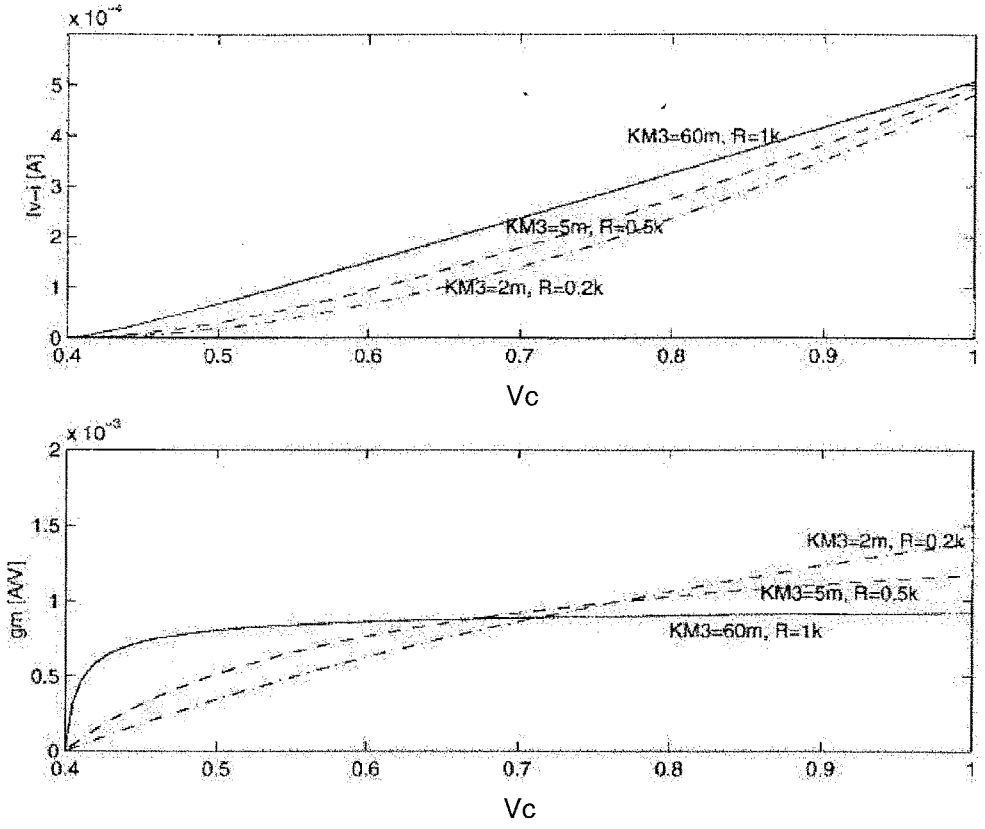


Figure 3.2.9 Mathematical simulation results of Eq. (3.2.11) (the upper plot) and the slope of the curves (the lower plot) with different *KM3* and *R*.

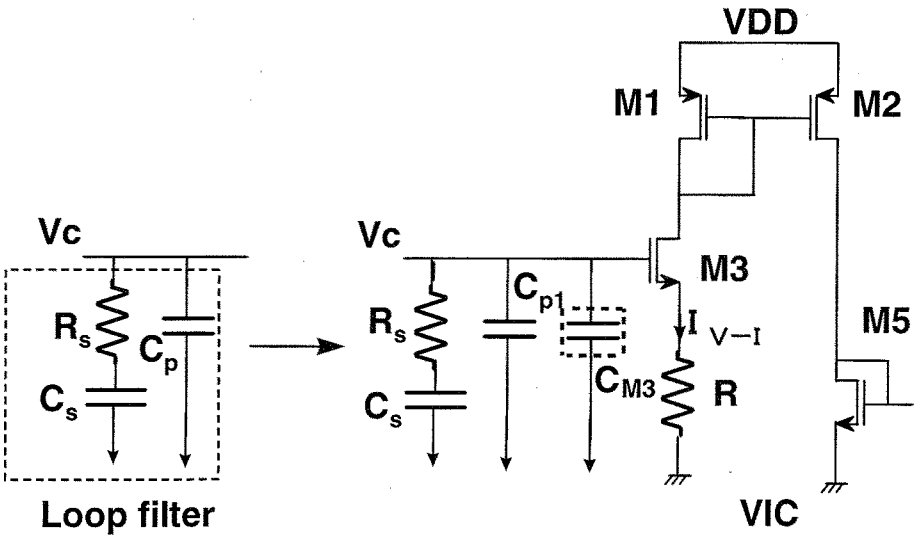


Figure 3.2.10 Lumped capacitor

It is, however, important to note that in modern CMOS-oriented process the chip-to-chip (or lot-to-lot) R variation is not negligible and causes the same variation in g_m of the above VIC. This makes the optimization of the loop filter components of the PLL extremely difficult. Hence, in many cases, it is desirable to design all-MOS VIC. All MOS VIC can be realized by replacing the resistor with M4 at the source terminal of the M3 as shown in Fig. 3.2.8(b). The gate terminal of the M4 is connected to the constant voltage. By keeping the drain voltage of the M4 within

$$V_{DS,M4} \le V_{G,M4} - V_{TH,N} \quad \cdots \quad (3.2.12),$$

the M4 can operate in the linear region and act as a resistor. Thus linear transconductance can be easily obtained using this structure and a more complicated structure is not needed. The resultant current, I_{V-I}, is used as a control signal for the ring oscillator via the current mirror (M1 and M2) and M5. In the case for applying to SoC, since high frequency (switching) noise on a power supply line is rejected through a power line decoupling capacitor and low frequency noise does not disturb oscillation frequency due to the wide bandwidth of the PLL.

(b) Differential delay cell

The new delay cell is designed as a differential type, i.e., it receives and generates differential inputs and outputs, respectively, to enable high noise immunity. The basic schematic of the cell is shown in Fig. 3.2.11, where a CMOS latch is inserted between the two outputs, V_{o1} and V_{o2}.

The delay of the cell is expressed as

$$D_{delay} = D_{charging} + D_{discharging} \quad \cdots \quad (3.2.13)$$

$$= \frac{C_{out}}{I_{charging}} + \frac{C_{out}}{I_{discharging}} \quad \cdots \quad (3.2.14)$$

$$= C_{out}\left(\frac{1}{I_{charging}} + \frac{1}{I_{discharging}}\right) \quad \cdots \quad (3.2.15),$$

where C_{out} is output node-associated capacitance (stray capacitance and the input capacitance of the next delay cell) and $I_{charging}$ ($I_{discharging}$) is charging (discharging) current.

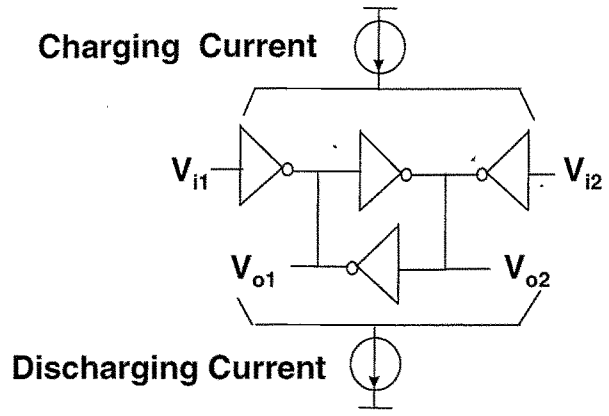


Figure 3.2.11 Schematic diagram new differential cell

From Eq. (3.2.15), the oscillation frequency ($f_{oscillation}$) of the ring oscillator based on this cell can be adjusted by controlling the current *Ic* and given by

$$f_{oscillation} = \frac{1}{2 N D_{delay}} = \frac{I_C}{2 N C_{out}} \quad \cdots \quad (3.2.16),$$

where N is the number of the cell in the ring oscillator and $I_C = I_{charging} = I_{discharging}$.

The main feature of the cell is that it employs local positive feedback [12][66][67] by using a simple latch composed of cross-coupled CMOS inverters. Having the positive feedback increases the effective gain of the cell (proportional to the square of the inverter gain in the latch by considering the two input inverter as triggering sources), which provides the following advantage.

(i) the CCO can be implemented with a small number of delay cells, which enables
- high frequency operation
- low power consumption
- low jitter [68]

(ii) Stable oscillation can be obtained under a low power supply voltage.

Fig. 3.2.12 shows the circuit implementation of the cell, where, (a) and (b) are named unbalanced and balanced cells, respectively, due to the fact

that the output voltage of the balanced cell are positioned at the center of the two power rails, i.e. balanced with respect to the center of the two power rails. On the other hand while the output voltages of the unbalanced cell are positioned slightly toward to the VDD power rails, i.e., unbalanced with respect to the center of the two power rails. In Fig. 3.2.12, Vcp and Vcn are the charging current control signal and the discharging current control signal for the CCO, respectively. They are derived from the VIC shown in the Fig. 3.2.8.

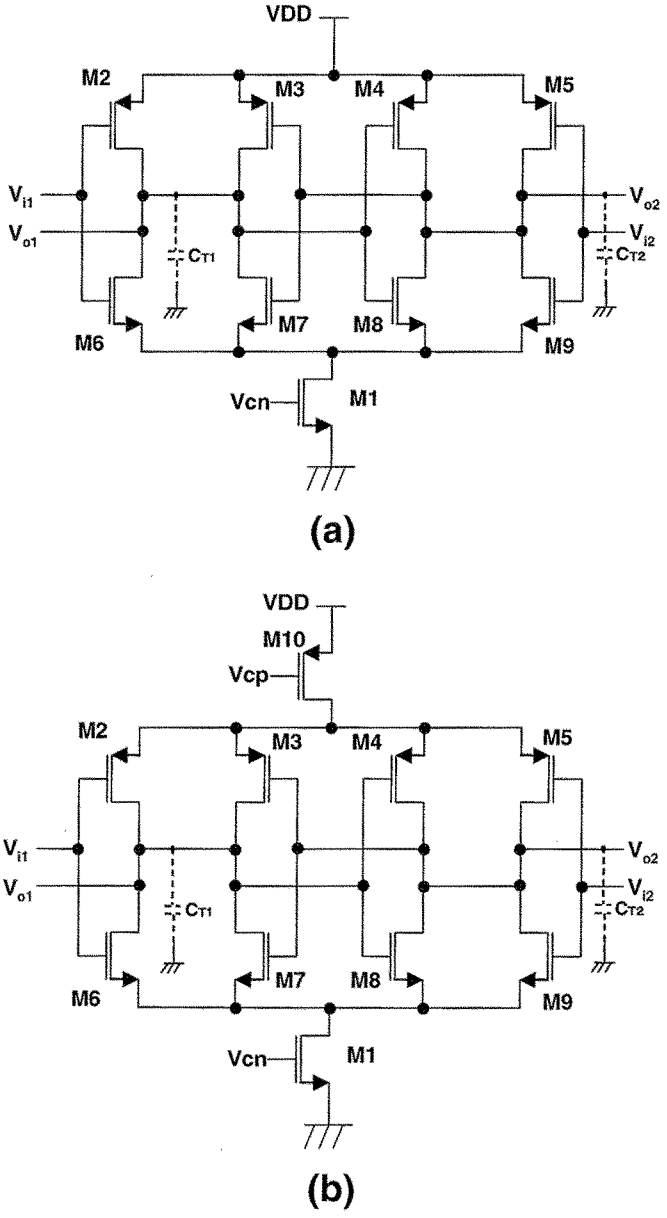


Figure 3.2.12 Circuit implementation of Fig.3.2.11
(a) unbalanced cell (b) balanced cell

Since the basic functions of the cells are the same, the unbalanced cell will be only explained. The delay of the cell is controlled through M1, whose drain current mirrors the I_{V-I} generated in the V-I converter. The cell can be functionally divided into two sub-blocks: the capacitor charge/discharge block (CB) and the CMOS latch block. The CB is composed of two CMOS inverters (M2 and M6, and M5 and M9) and parasitic capacitors (timing capacitors CT1 and CT2) at two output nodes, V_{o1} and V_{o2}. By turning the CMOS inverters ON and OFF alternately with differential inputs, the timing capacitors are charged and discharged so as to generate differential outputs. Note here that the maximum current capability of M6 and M9 must be larger than that of M1. This guarantees that the discharging current is limited by M1, not by M6 or M9, hence the cell becomes current controllable. The timing capacitors at the two output nodes are parasitic capacitors made up mainly of the gate capacitors of the CMOS inverters and partly of the node-associated interconnection capacitors. The symmetric and tight layout scheme reduces the capacitance of the timing capacitors, therefore high-frequency operation is achievable. Such a layout also helps to avoid topological mismatches between the transistors and decreases the electrical imperfection at the outputs.

To ensure differential outputs, local positive feedback loop formed by M3, M4, M7 and M8 (the CMOS latch block) is used between the two outputs. The transconductance of the transistors in the latch must be less than that of the corresponding transistors in the CB block. Otherwise, the two outputs would be latched and remain at stable voltages (no oscillation would occur). This requirement can be met by making the CMOS pairs in the CB block wider than the latch pairs with all transistors having equal lengths. The latch detects any voltage difference between the two outputs and pumps the charge at the timing capacitors up or down as needed. The positive feedback further accelerates this, causing the two outputs to be identical in magnitude and shape but opposite in phase (180°).

Here, two advantages of the proposed VCO over the conventional feed-forward type VCO shown in Ref. [12] are summarized. They are (a) lower supply voltage < 1.5 V is allowable because the proposed VCO needs only one saturation MOS transistor for the bias current control, (b) ease to avoid stacking (i.e. oscillation stop) by selecting a proper ratio between MOS transistor width of CB and that of the CMOS latch. These two new

features are very effective on designing VCOs by using a fine design rule process because they tend to have much large variation in transistor parameters and lower breakdown voltage of the transistor.

So far, the LV/LP VCO that consists of delay cells using a complementary input stage with feed-forward circuits [62] are proposed. Although the VCO described above can oscillate as high as 400 MHz under a low supply voltage of 1.2 V, we need to investigate the oscillation frequency limitation to improve its maximum oscillation frequency and propose an improved VCO that can oscillate much higher than 1 GHz. Call the delay cell described above "Type-A" and the improved VCO "Type-B" hereafter.

The Type-A delay cell of the VCO consists of a push-pull input stage, M2 and M6, and M5 and M9, a latch, M3 and M7, and M4 and M8, and the bias current control transistors, M1, M10. The latch is connected between V_{o1} and V_{o2} to speed up their slew rate. Because the latch in the delay cell has an effect to increase its actual gain of the closed loop, the VCO can oscillate relatively high frequency under a low supply voltage.

Next improvement to increase oscillation frequency and reduce current consumption in the delay cell in Fig. 3.2.12 is described. The push-pull input stage and the latch of the delay cell independently contain the load transistors, M2, M5, M3, and M4. They become not only the load capacitance for the circuits but also the main limitation factor of the maximum oscillation frequency. The reverse current flow occurs from M3 to the V_{o1} when V_{o1} is going down and the other reverse current flow occurs from M4 to V_{o2} when V_{o2} is going down in the Type-A delay cell. These reverse current flows from M3 and M4 and pulls up the outputs, V_{o1} and V_{o2} to "High", when they are going down to "Low." This delay cell circuit is symmetrical, so we focused on only the delay mechanism for V_{o1}. This reverse current that occurred in the Type-A delay cell is shown by the dotted line in Fig. 3.2.13. Here, the sink current shown in the figure means the current which sank from a load capacitance of V_{o1} to pull down its node voltage to "Low" and the reverse current of the same figure means the current supplied from VDD via the transistor M3.

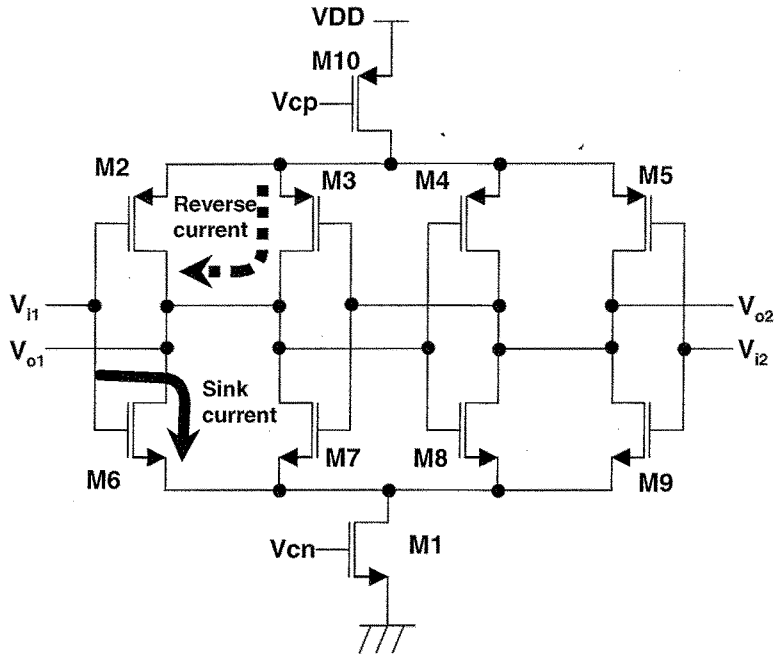


Figure 3.2.13 Reverse current in delay cell of the VCO

When V_{i1} is changed from "Low" to "High", the transistor M2 is OFF and M6 is ON, then the output V_{o1} goes down to "Low" as a result of the sinking current via M6. At this timing, however, M3 is still ON because V_{o2} stays in "Low" according to the delay of M4 and M8. As shown in the figure, M3 supplies a current to disturb the transition of V_{o1} from "High" to "Low," therefore this reverse current causes the extra delay of the delay cells. The simulation result of the Type-A delay cell is shown in Fig. 3.2.14. It shows an input signal, V_{i1}, an output signal, V_{o1}, a sink current from V_{o1}, and a reverse current from VDD. The slew rate of V_{o1} is degraded because the reverse current flows in the opposite direction to the sink current and increases the delay time.

Here, we propose a delay cell for the VCO as Type-B to reduce the extra delay caused by the mechanism mentioned above. It can oscillate at a higher frequency. The Type-B delay cell shown in Fig. 3.2.15 has two common load transistors, M2 and M5 for the push-pull input stage and the latch instead of M3 and M4 of the Type-A delay cell. Thanks to elimination of M3 and M4, there are no reverse current paths in the Type-B delay cell.

To compare the delay between the Type-A and the Type-B delay cells, we simulate the VCO oscillation frequency to the control voltage, Vc and

show the results in Fig. 3.2.16. The maximum oscillation frequencies of the Type-A VCO and the Type-B VCO are 1.4 GHz and 1.9 GHz respectively. This means that the performance of Type-B VCO is about 36% improved over that of the Type-A VCO. Fig. 3.2.17 shows the waveforms of both the Type-A and the Type-B VCOs at 1 GHz. Here, control current of the Type-A VCO and the Type-B VCO are 400-μA and 175-μA, respectively. Though the control current of the Type-B VCO is 43% of the Type-A VCO one, slew rate degradation is only 20%.

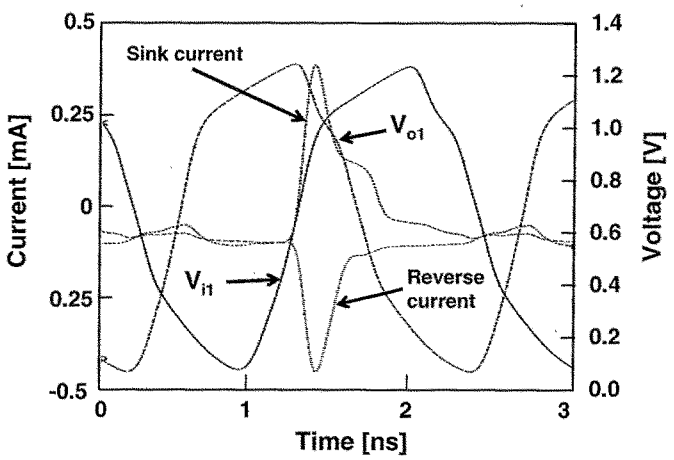


Figure 3.2.14 Simulation result of reverse current in the delay cell

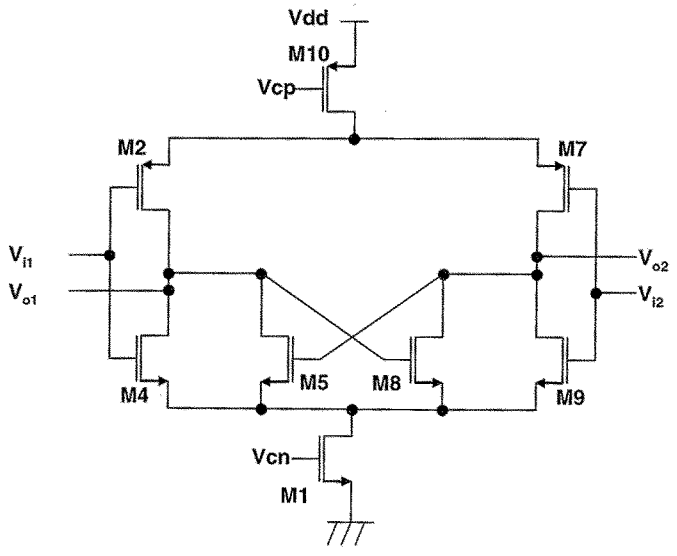


Figure 3.2.15 Improved delay cell

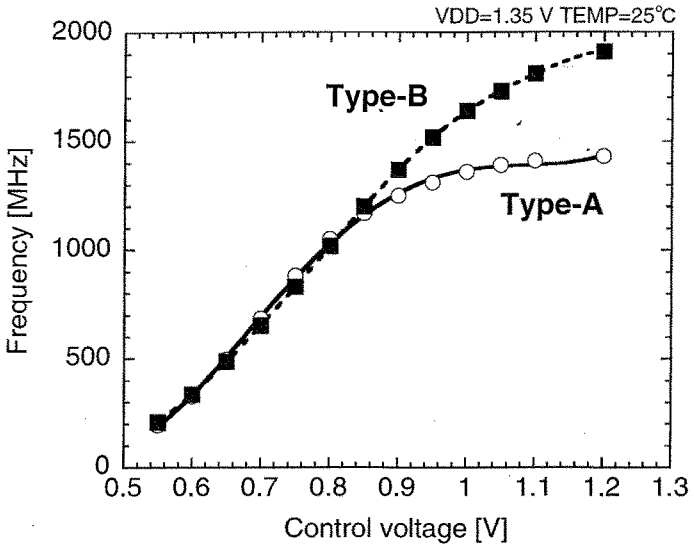


Figure 3.2.16 Control voltage to oscillation frequency simulation results

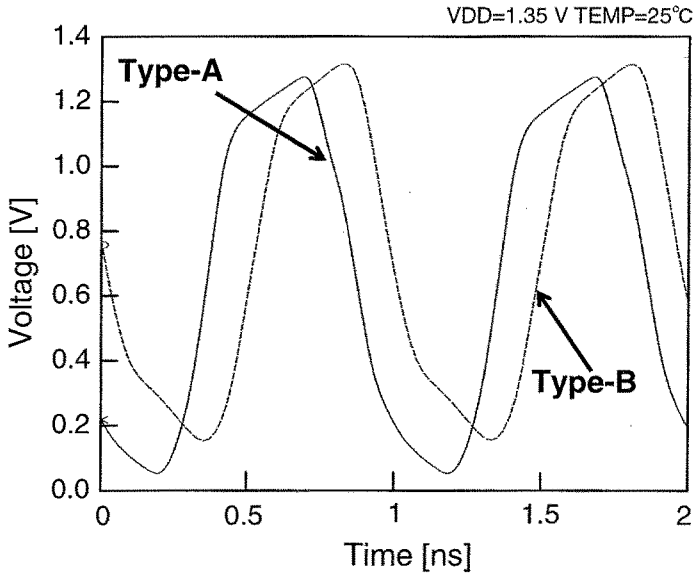


Figure 3.2.17 Waveforms of Type-A and Type-B VCOs

3.3. Experimental results

Two PLLs are fabricated by the 0.18-μm CMOS process to verify their performance. One is the PLL with the Type-A VCO and the other is one with the Type-B VCO. Fig. 3.3.1 shows the chip photograph of the PLL

with the Type-B VCO. The active area of the PLL is 0.22mm^2 (380 μm×580 μm). In all measurement results division ratio N is 12 and temperature is 25°C.

A measurement of the maximum oscillation frequency of the PLL vs. VDD is shown in Fig. 3.3.2. The PLL with the Type-B VCO oscillated at a higher frequency than 1 GHz when VDD is higher than 1.2 V and its maximum oscillation frequency is improved by about 38 % over that of the PLL with the Type-A VCO. Maximum oscillation frequency of the Type-B PLL is 1.2 GHz under a 1.2-V supply voltage and 1.4 GHz under a 1.35-V supply voltage, respectively.

The power consumption of the PLL with Type-B VCO is compared to that of the PLL with Type-A VCO in Fig. 3.3.3. The proposed technique can reduce PLL power consumption about 15% compared to that of the PLL with the Type-A VCO at an oscillation frequency of 1 GHz. This means that the elimination of the reverse current paths of the Type-A VCO is very effective not only for improving the maximum oscillation frequency but also for lowering the power consumption.

The measurement results of a cycle-to-cycle jitter test of the PLL with Type-B VCO are shown in Fig. 3.3.4. The jitter produced by the fabricated PLL is less than 100 $ps_{p\text{-}p}$ and the PLL stability is sufficient due to the new charge pump using the switched current op-amp and the new stability technique.

Measurement results are summarized in Table 3.3.1.

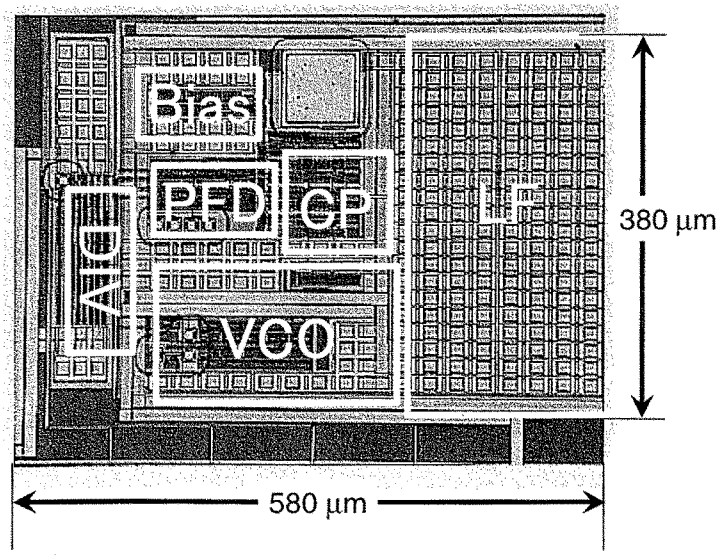


Figure 3.3.1 Chip photograph of the fabricated PLL

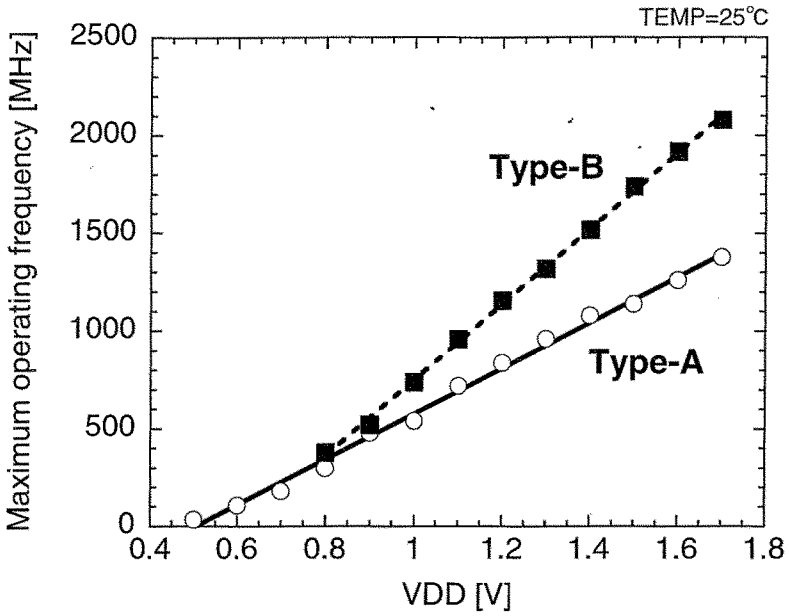


Figure 3.3.2 Maximum oscillation frequency to VDD

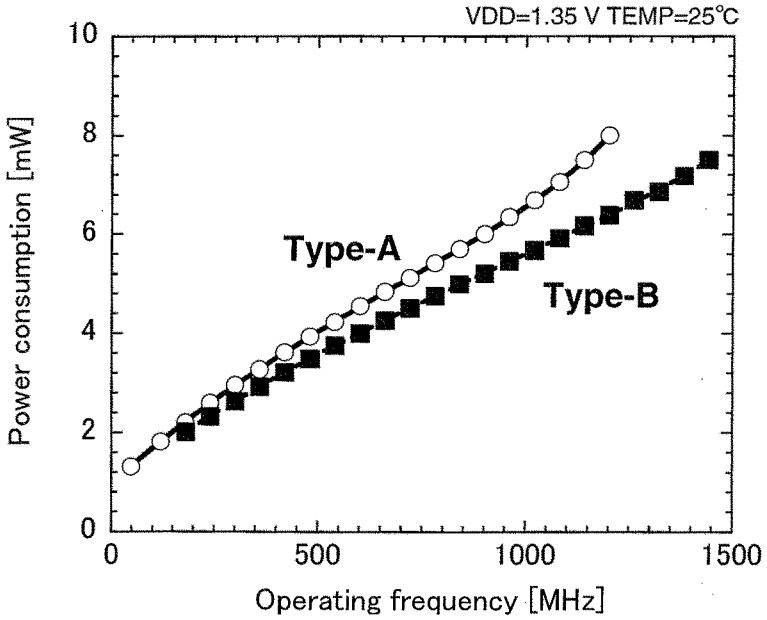


Figure 3.3.3 Power consumption of the PLL

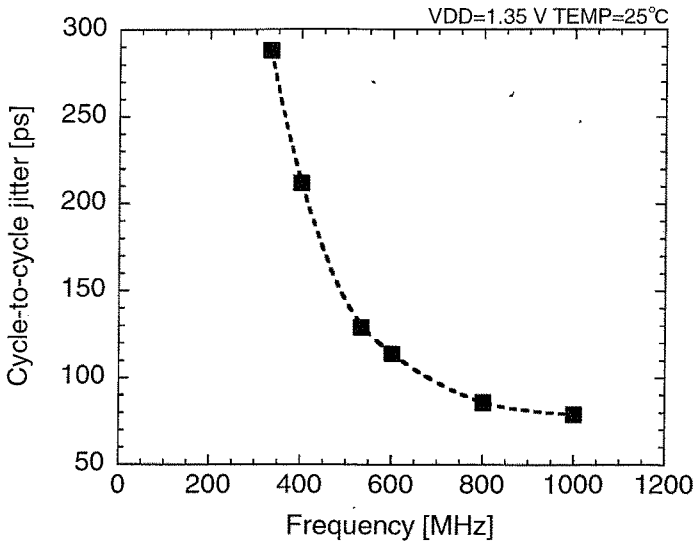


Figure 3.3.4 Cycle-to-cycle jitter of Type-B

Table 3.3.1 Summary of measurement results of Type-B

Power supply	1.35 V
Minimum PLL supply voltage for 1-GHz oscillation	1.2 V
Operating Frequency range at VDD=1.35 V	0 -1.4 GHz
Cycle-to-cycle jitter at 1 GHz	79 $ps_{p\text{-}p}$
Power dissipation at 1 GHz and VDD=1.35 V	5.6 mW
Locking time	2.5 μs

TEMP=25°C

3.4. Conclusion

We have developed a PLL for low power and low supply voltage applications, such as the system LSIs of the mobile terminals. First, we have proposed a charge pump that uses a dynamic output stage op-amp to keep the phase error small, and then a new stability technique for the process, which does not require special resistors. Finally, we have investigated a VCO under a low supply voltage.

We have already proposed a modified differential delay cell using a simple latch composed of cross-coupled CMOS inverters. This circuit technique has advantages of (a) lower supply voltage because the proposed VCO needs only one saturation MOS transistor for the bias current control, (b) avoidance of the VCO stacking problem by only selecting a proper ratio between MOS transistor width of the CB and that of the CMOS latch and insensitive to the MOS transistor parameter variation. However, we investigate the oscillation frequency limitations of the VCO with the simple CMOS latch and propose an effective modified circuit using common load transistors to improve its maximum oscillation frequency under a low supply voltage.

We have fabricated the PLL using a standard logic 0.18-μm CMOS process and have verified that the PLL operates above 1.0 GHz under a 1.2-V supply voltage. Furthermore, the PLL produces cycle-to-cycle jitter less than 79 $ps_{p\text{-}p}$ and settles shorter than 2.5 μs. These techniques described in this Chapter are very useful for the LV/LP design of PLL integrated in SoCs have been verified.

Chapter 4

Modulators using PLL for SoCs and mobile transceivers

4.1 Introduction

In this Chapter, PLL techniques for modulator applications will be described in detail. One application is using a feedback loop modulation and the other is using a two-point modulation. These modulators which are integrated into system level applications gives us advantages of elimination of a lot of expensive external components and better modulation performance.

Firstly, we will discuss a PLL for the feedback loop modulation. Noting the potential of using ΣΔ modulation to control the divider ratio of the PLL, we describe effective methods to reduce jitter caused by a ΣΔ modulator in the feedback loop. The feedback loop modulation technique is adopted into a serial ATA spread-spectrum clock generator in this Chapter because low jitter and large EMI reduction should be achieved in this application. We will propose a PLL modulator using a multi-bit third-order ΣΔ modulator to control the divider's ratio in order to achieve low jitter, which is appropriate for the serial ATA clock generator.

Next, we will discuss on a GFSK modulator using the two-point

modulation for the Bluetooth standard. As described in Chapter 2, some candidates are possible to be adopted into the GFSK modulator. Among them the two-point modulation is the best fit to the Bluetooth transmitter because it is possible for wider modulation bandwidth than loop bandwidth of a PLL without any frequency characteristic compensation blocks.

While the two-point modulation is useful as a technique for the generation of GFSK signals for Bluetooth transceivers, we must consider degradations due to the PLL loop bandwidth and drift in the center frequency of the output signal. Furthermore, while Staszewski et al. [69] have presented a method of the two-point modulation that is specifically for digital signals, the method requires a means of compensation to absorb quantization noise introduced because of the restricted clock rate and a means for adjusting a digitally controlled oscillator to maintain constant voltage-to-frequency conversion gain with varying carrier frequency.

Our proposed modulator is based on a two-point modulator with the VCO modulation and fractional frequency divider control achieved through $\Sigma\Delta$ modulation. Here, we newly develop the variable loop bandwidth control technique [70] of PLL and adopt it into the GFSK modulator for satisfying the Bluetooth specifications. The proposed new techniques reduce out-of-band frequency noise, improve an eye opening for transmitting signals, and also reduce the drift in the center frequency due to noise and leakage of circuits. We demonstrate that the new architecture is effective in reducing center-frequency drift.

In both applications using the PLL modulator, we will discuss their PLL architectures combined with their key components, especially VCO.

The remains of this Chapter are constructed as followers. In section 4.2, PLL feedback loop modulation techniques for a spread-spectrum clock generator are described. Then in section 4.3, two-point modulation PLL integration techniques for a Bluetooth transmitter will be given. In section 4.4, we will show some measurement results for these two PLL modulation techniques. Then we will conclude PLL modulation techniques in section 4.5.

4.2 PLL for feedback loop modulation

4.2.1 Serial ATA

For portable devices, reducing unnecessary radiation, for example, EMI, is very important. Dominant EMI sources in portable devices are high-speed interfaces between signal processing units and the other peripheral storage devices, e.g., hard disc drives (HDDs) and DVD/CD read-only memory (ROM) drives. A serial ATA is being used more often to cope with higher data-rate requirements because high-speed data (1.5 or 3.0 Gbps) can be transmitted through a simple serial cable when this technique is used. Ideally, EMI reduction should be done on-chip without using heavy shielding materials to produce low-cost portable equipment.

In section 4.2.2, we will describe the SSCG specifications applied to the serial ATA. After that, we will describe how to reduce jitter from the modulator.

4.2.2 Block diagram of serial ATA

Fig. 4.2.1 is a general block diagram of a serial ATA transceiver. This is our design for the first generation of ATA transceivers that meets serial ATA specifications. This specification supports a 1.5-Gbps transmission on a shielded twist pair cable. Parallel data for transmission (Din) goes to serializer (SER) and is outputted from a line driver (DRV). Input serial signal (RX) is amplified to a distinguishable signal level by an amplifier (AMP). The received signal is then retimed by a clock-data recovery circuit (CDR) and regenerated as parallel-received data (Dout) by a de-serializer (DES). Usually, SER and DES blocks are combined into a single block and are called SERDES. The SSCG produces the clock signal for it from fr; in our design, this is a crystal oscillator running at a frequency between 20 and 40 MHz. The output clock signal in our design is at a frequency (fo) of 1.5 GHz.

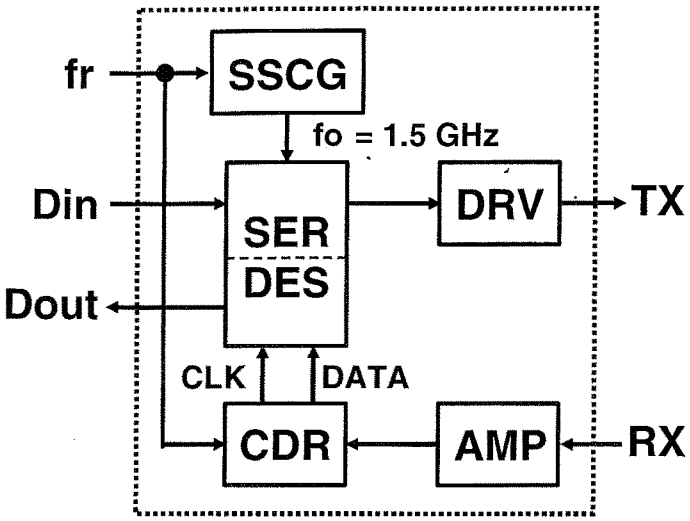


Figure 4.2.1 Serial ATA block diagram

4.2.3 Target specifications

Table 4.2.1 summarizes the requirements for SSCG in the first-generation serial ATA applications. First, the generated clock must have very low jitter. In fact, the specification states that jitter, as measured by averaging 250 consecutive samples, must be below 12 ps. Achieving this low level of jitter is the most difficult point in the design. Also, the spread-spectrum technique must reduce the EMI by at least 7 dB. While this value is the minimum requirement in serial ATA specifications, the SSCG for a portable device would ideally lower the EMI by an even greater margin, since this would relax the requirement for external shielding of ICs. The specifications also state that the spread-spectrum bandwidth must be no greater than 5350 ppm. Our target is a PLL that satisfies the specifications for the serial ATA.

Table 4.2.1 Target specifications for first-generation serial ATA

RMS jitter averaged during 250 samples	< 12 ps rms
EMI reduction	> 7 dB
Spread spectrum bandwidth	5350 ppm
Output frequency	1.5 GHz

4.2.4 Spread-spectrum clock generator architecture

Fig. 4.2.2 is a block diagram of the proposed PLL for the SSCG. We used a prescaler (PRS) in front of the DIV. In our design, the PRS division ratio (P/P+1) is set between four and five because we only need to reduce the output frequency to a range around 400 MHz where a CMOS divider for a DIV can operate. Divisor, N, which controls the DIV, is generated by a counter controller (CONT) that consists of a ΣΔ modulator (ΣΔ Mod.) and adders. The inputs of the CONT are a divider ratio, to generate fo, and a triangle wave, for spread-spectrum generation. The divider ratio can be separated into an integer part (M) and a fractional part (F). We must carefully address a re-settling problem in the ΣΔ modulator when the signals of the integer and fractional parts are processed separately because the input of the ΣΔ modulator might be discontinuous when carry-overs between M and F occur. The bit assignments to M and F is shown at the top of Fig. 4.2.3. This figure shows the bit assignments in CONT. Triangle wave, m, which is normally a decimal value shown in the second row of Fig. 4.2.3, is added to the fractional part of the divider ratio. Because down spread is required in a serial ATA transmitter, F+M+m results in a frequency lower than 1.5 GHz in a serial ATA output. The output of the adder A is inputted into the ΣΔ modulator to be converted to an integer value B because the DIV can only be controlled by integer values. In the ΣΔ modulator, the adder output A sometimes becomes larger than the one shown in Fig. 4.2.3 because A is the sum of m and F. Therefore, we design this ΣΔ modulator with multi-bit resolution. Finally, the output of the ΣΔ modulator (B) is added to M, and the output of the adder N controls the DIV in the PLL. This architecture provides a solution to the re-settling problem of the ΣΔ modulator because it prevents a carry-over between M and F with design redundancy in bit assignments in the signal processing of the CONT. With this proposed PLL, we can achieve precise control over spread-spectrum clock signals.

Next, we investigate the relation between ΣΔ modulator architecture and output jitter in the context of a serial ATA application. In this application, the major component of the output jitter is ΣΔ modulation noise. We believe the PLL eliminates higher frequency noise components from the ΣΔ modulation noise with its closed loop transfer function. This frequency response is similar to a low-pass filter for which the cut-off

frequency is almost equal to the PLL's loop bandwidth. Here, the PLL loop bandwidth is set to 300 kHz because it must be about 10 times wider than the triangle wave frequency of 30 kHz to modulate.

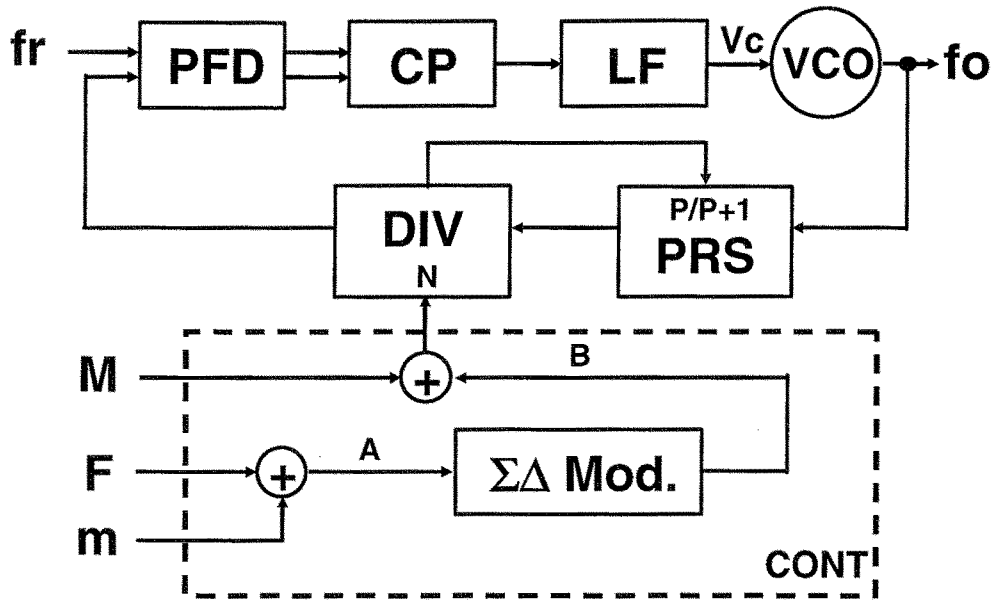


Figure 4.2.2 Diagram of proposed SSCG

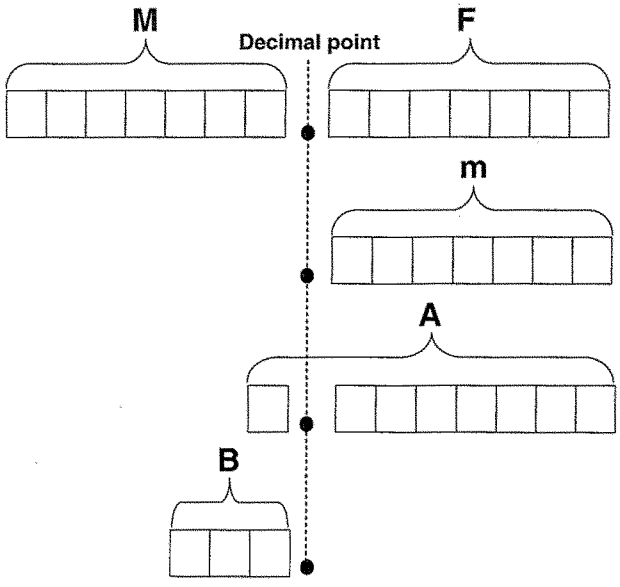


Figure 4.2.3 Bit assignments in CONT

For serial ATA applications, we average jitter measurements over 250 cycles as defined in the serial ATA specifications. The window function for averaging over n cycles is defined by

$$F_{avg}(z)=\frac{1}{n}(1+z^{-1}+z^{-2}+\cdots+z^{-n+1})=\frac{(1-z^{-n})}{n(1-z^{-1})} \quad \cdots \quad (4.2.1).$$

Here, n = 250 and z^{-1} expresses a delay by the transmission clock period equal to 1/1.5 GHz. These two frequency characteristics are multiplied by the ΣΔ modulation noise, and we obtain the average output jitter.

Then we must consider the trade-off between the PLL output jitter and the order in ΣΔ modulator in the CONT. This is because the higher jitter of lower-order ΣΔ modulators leads to larger noise components in the low-frequency range. Usually, the frequency characteristics of the ΣΔ noise, $\Sigma\Delta_{\_Noise}$ are expressed by

$$\Sigma\Delta_{\_Noise} \propto (1-z^{-1})^{N} \quad \cdots \quad (4.2.2).$$

Here, $\Sigma\Delta_{\_Noise}$ is expressed by the Nth power of a differential function; therefore, it has high-pass frequency characteristics, and the slope of the function depends on N. Using N less than two, since noise components near the frequency of the modulating triangle wave increase, leads to increased jitter at the output of the SSCG. While higher-order ΣΔ modulators improve the noise in the low-frequency range, they increase the noise components on the order of several MHz, thereby significantly increasing jitter. However, this is because the peak gain of the window function for averaging over 250 cycles, $F_{avg}(z)$ in Eq. (4.2.1), is close to the range of peak frequencies for noise from higher-order ΣΔ modulators, $\Sigma\Delta_{\_Noise}$.

The peak frequency of the Fvco/250 is around 6 MHz. Therefore, when we use ΣΔ modulators in our DIV controller, we must choose the optimal ΣΔ order for minimizing the output jitter. When we chose the optimal ΣΔ order for our SSCG, we use the PLL loop filter as a 3-pole 1-zero type (This means the total feedback loop is fourth-order.), because we wanted to reduce the peak noise component that appeared around 6-MHz as described above. In serial ATA applications, we found the optimal ΣΔ order to be three [71]–[73], based on our time region simulation using ADS: Advanced Design System [74].

4.2.5 Low phase noise VCO

The important issues around how to reduce a VCO phase noise with fine design rule CMOS transistors are described in this section. To achieve small jitter in a PLL output, we must consider how to reduce the flicker noise level because that is the main noise component in VCOs of serial ATA applications. In section 4.2.4, we discussed how the specifications place the most critical frequency noise range for jitter in the several-MHz frequency range. The corner frequency for flicker noise is not far from this. Therefore, we must design a VCO less sensitive to flicker noise.

Initially we select PMOS transistors of CMOS process for lower-jitter VCOs, since it has a smaller flicker-noise parameter. Furthermore, we lowered the sensitivity of the VCO-to-circuit noise in general by incorporating a cross-coupled load in the delay cell. This cross-coupled load acts as a feed-forward circuit. Its operation and effect have already been described in Chapter 3.

Fig. 4.2.4 is a circuit diagram of the proposed VCO, which was adapted in a previously developed technique [75] and modified for much higher oscillation frequency over 2.5 GHz. This VCO consists of differential three-stage delay cells and a voltage-to-current converter (VIC). The VIC is a simple gate-input NMOS amplifier. The delay cell consists of two push-pull input amplifiers, configured as (M1 and M3, and M2 and M4), and two cross-coupled transistors, M6 and M7, connected between the outputs of the amplifiers. The details of the VIC circuits and the delay cell are given in Figs. 4.2.4(b) and (c).

Since the cross-coupled transistors M6 and M7 are controlled by the same current source (M5), which is also used in the input amplifiers, the gain of the VCO is reduced and there is less jitter for a given amount of noise. Furthermore, this circuit increases the output signal amplitude. Fig. 4.2.5 displays a comparison of simulation results for the proposed VCO and the well-known VCO with MOS-diode delay cells [76].

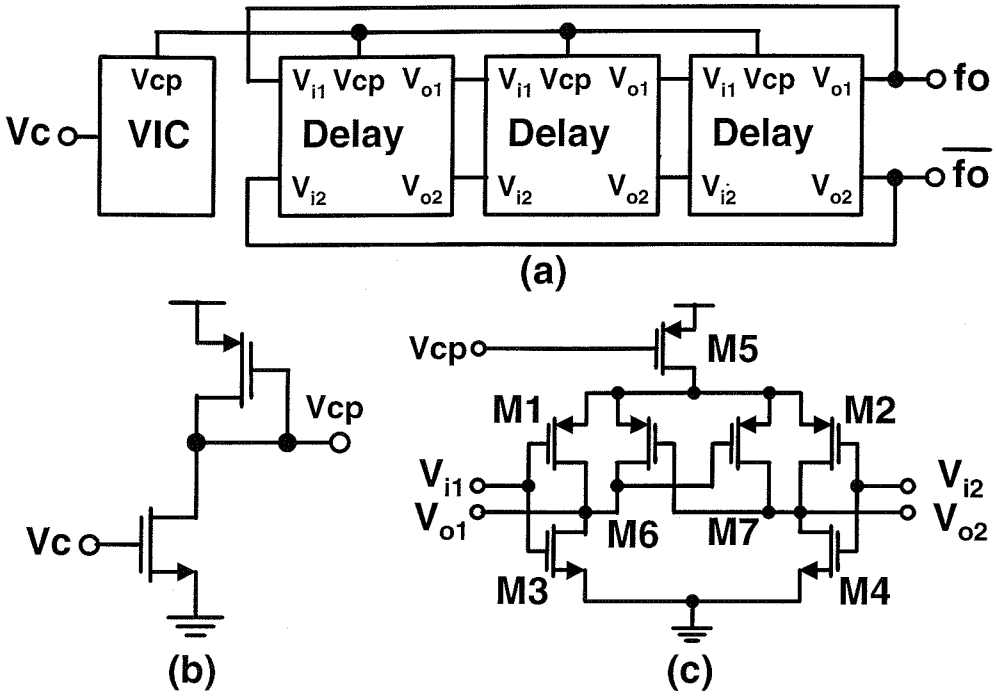


Figure 4.2.4 VCO block diagram and its detail circuits
(a) VCO (b) VIC (c) delay cell

In Fig. 4.2.5, the black triangles represent phase-noise results for the proposed VCO, and the white triangles show its output amplitude. The circles are the corresponding results for the VCO with MOS-diode cells. For a comparison of the results, we design the VCOs to have the same oscillation-frequency range and gain. The abscissa represents control voltage input to the VIC, and the left ordinate of the graph represents phase noise. The right ordinate represents output amplitude of the VCO. As the graph shows, the phase noise of the proposed VCO is improved by about 10 dB compared to that of the VCO with MOS-diode delay cells because the cross-coupled transistors with the same current source reduce the VCO gain and effectively enlarge the output amplitude.

The Figure of Merit (*FOM*) of a VCO is defined by [77]

$$FOM = L\{\Delta f\} - 20\log\left(\frac{f}{\Delta f}\right) + 10\log\left(\frac{P_{dc}}{1mW}\right) \quad \cdots \quad (4.1.3).$$

The simulation results show $L\{\Delta f\} = -90dBc/Hz @ 1MHz$ in Fig. 4.2.5, and we design both VCOs to have the same 10-mA current. Therefore, the FOM of the proposed VCO is −141 dB, which is better than that of the VCO with

MOS-diode delay cells by 10 dB under the same simulation conditions. Thus, the proposed VCO with delay cells described in Chapter 3 improves phase noise significantly.

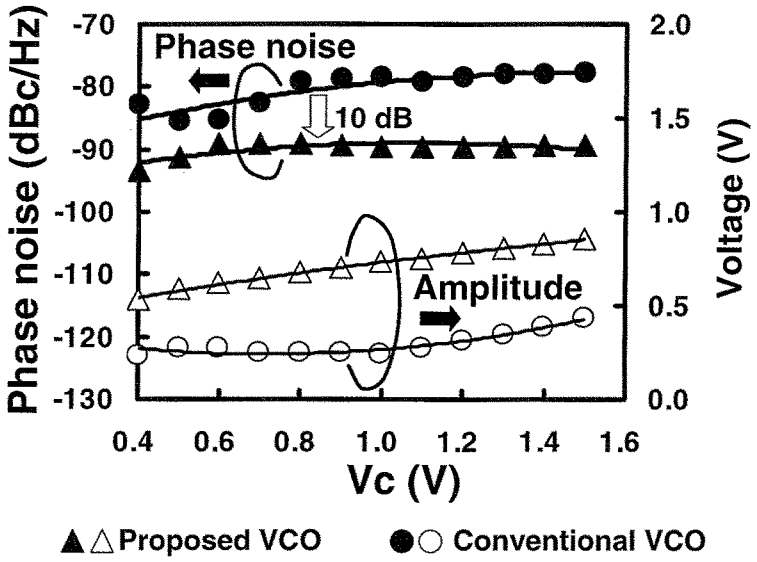


Figure 4.2.5 Simulation results for the proposed and conventional VCO

4.3 PLL for two-point modulation

4.3.1 Bluetooth transmitter

There exist various popular forms of wireless communications, such as wireless LAN, the personal handy-phone system (PHS), code division multiple access (CDMA), GSM, and other mobile-phone standards. Personal area networks (PANs), in which the network is formed through a base station or directly among individual terminals, are now being added to this list. The Bluetooth standard for wireless communications is the best-known short-range wireless access method for the realization of PANs.

The Bluetooth standard specifies a method of communication over ranges within 10 m [78]. Bluetooth terminals will popularize direct inter-device wireless data communications for multiple items of personal equipment, and will dramatically improve the versatility and interoperability of mobile devices such as cellular phones, PDAs, and

portable personal computers. A block diagram of a typical Bluetooth transceiver is shown in Fig. 4.3.1.

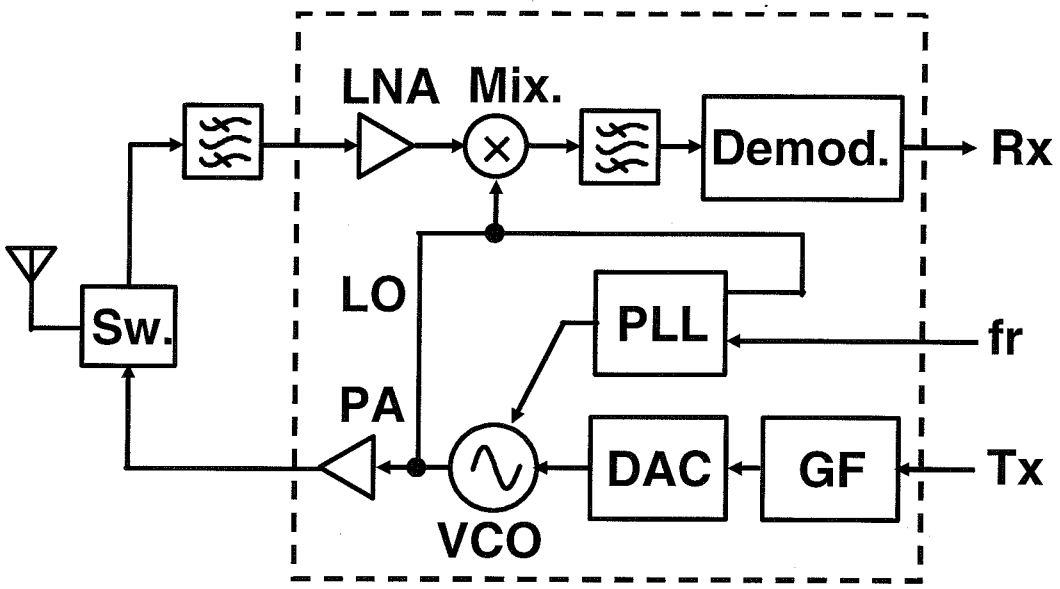


Figure 4.3.1 Block diagram of a Bluetooth transceiver

Table 4.3.1 Bluetooth transmitter specification

No.	Item		Bluetooth specification
1	Initial frequency offset		< ±25 kHz
2	Center frequency drift		< 25 kHz
3	Frequency drift rate		< 20 kHz/50 μs
4	Frequency deviation	Average	140 - 175 kHz
5		Minimum	> 115 kHz
6	Eye-opening ratio		> 0.8
7	-20-dB bandwidth		< 1 MHz
8	In-band spurious	< 2MHz	< -20 dBm
9		> 3MHz	< -40 dBm
10	Out-of-band spurious		< -30 dBm
11	PLL settling time		< 220 μs

The important requirements of the Bluetooth specification that apply to transmitters are listed in Table 4.3.1. Although a frequency offset of less than ±75 kHz is specified, the allowable frequency offset of a crystal oscillator used in the transceiver is specified as less than ±20 ppm, the initial frequency offset is ±25 kHz. Since noise from outside the IC will often have an effect, center frequency drift (item 2) arises because of power-supply noise on the board and so on. Items 4 to 7 are important in terms of the quality of the modulator. Item 8 indicates the extent to which in-band noise elements must be restrained so that they do not interfere with signal transfer on other Bluetooth channels. Item 9 indicates how much out-of-band noise elements have to be restrained so that they do not interfere with other (non-Bluetooth) signals. Non-linearities of the power amplifier (PA) and VCO are usually responsible for these disturbances. A short settling time for the PLL is also desirable, since this is part of the overall time taken to transmit a frame. The settling time listed in the table is the maximum permitted with Bluetooth.

4.3.2 Transceiver block diagram

The transmitter shown in Fig. 4.3.1 consists of the GF (Gaussian filter, i.e. a filter with a Gaussian characteristic), PLL, VCO, DAC, and PA. Tx, which indicates the data sequence to be transmitted, is inputted to the GF. We integrate the blocks inside the area marked by the dotted line. The output of the GF is converted into an analog signal by the DAC. The VCO has two control terminals, one controlled by the PLL and the other controlled by the modulating signal from the DAC so that the frequency-modulation signal for transmission is generated. The PA amplifies the output of the VCO and drives an antenna when connected through the switch (Sw.).

On the receiver side, microwave signals received from the antenna are inputted to the integrated circuit via the switch and a band-pass filter which selects the ISM (Industrial, Science, and Medical) band at 2.4 GHz. In the first stage of the integrated circuit, the input signal is amplified by the low-noise amplifier (LNA). In the next stage, the signal is converted to an intermediate frequency by the mixer (Mix.). After that, the narrow intermediate-frequency band-pass filter reduces the amplitude of disturbances potentially generated by other transceivers, selecting only

the desired frequency component. Finally, the demodulator (Demod.) regenerates Rx, the received digital data. The receiver circuits of this integrated circuit have been described in a previous report [24].

4.3.3 Transmitter using two-point modulator

Fig. 4.3.2 is a block diagram of the two-point modulator in which variable loop bandwidth is applied. The key technique is the use of a PLL synthesizer capable of fractional frequency multiplication. The two-point modulator consists of the direct VCO modulation circuit and the PLL, which includes a frequency divider (DIV). The divider is controlled by the ΣΔ modulator (Mod.), which takes the data sequence, for transmission (Tx) and transmission channel information (Tx-ch) as inputs.

As stated above, the PLL is the basis of the proposed transmitter circuit. The PLL consists of a phase-frequency detector (PFD), a charge pump (CP), and a VCO. The loop filter between CP and VCO consists of passive resistors and capacitors. Its role is to maintain stability and to suppress noise. The current from the CP is variable. Control is provided by the signal Bw-sel (select loop-bandwidth change), as is shown in the Fig. 4.3.2.

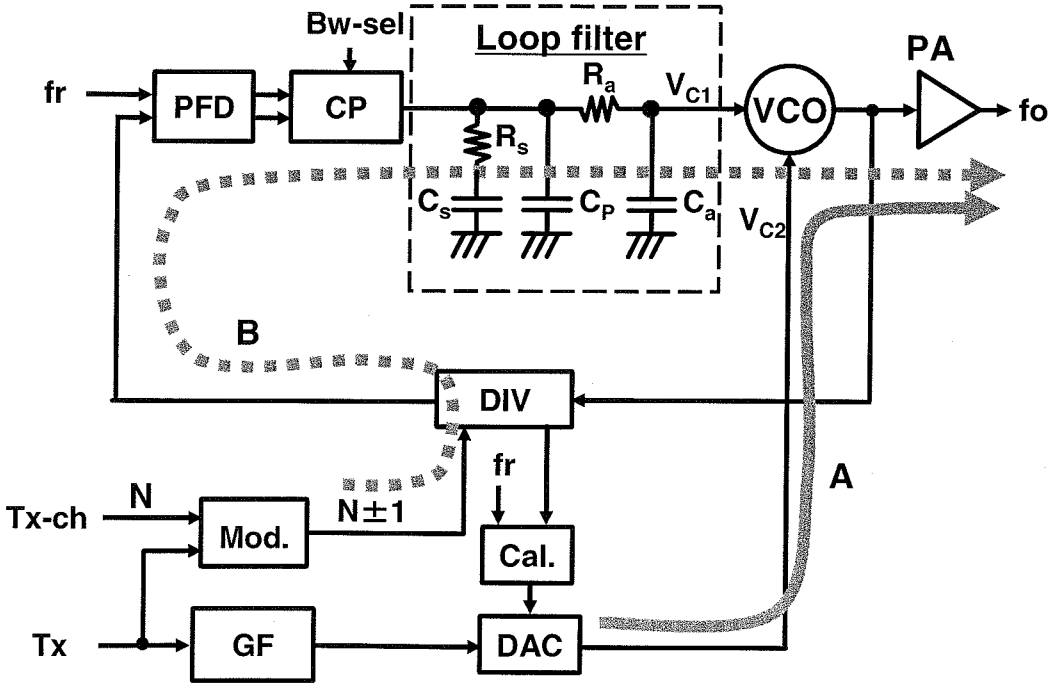


Figure 4.3.2 Block diagram of two-point modulation transmitter

The VCO is for two-point modulation and thus has two control terminals (V_{C1}, V_{C2}). V_{C1} is used as a conventional PLL control voltage and V_{C2} is used to apply the modulating signal, that is, the signal generated by passing Tx through the GF and DAC.

Next, Tx-ch and Tx are processed by the modulator to control the divider. TX-ch is an integer multiple N of the reference frequency. This selects the transmission channel of the transceiver. The modulator outputs a signal at N plus or minus one according to the current value of the data sequence for transmission. The maximum deviation of modulated signals from center frequencies in a Bluetooth transceiver is 0.16 MHz. Therefore, we use fractional frequency division to generate non-integer multiples of the 1-MHz reference frequency, for example, –0.16 MHz or +0.16 MHz. The average divisor for the divider is equal to the channel number, N.

4.3.4 Loop bandwidth requirements

The loop bandwidth, ω_c, is an important parameter which decides the noise contribution ratio of the two paths in the output signal. In other words, the noise contribution of the direct VCO modulation path increases when ω_c is lowered so that the PLL has a narrower loop bandwidth, and the noise contribution of the ΣΔ modulator path increases when ω_c is raised so that the PLL has a wider loop bandwidth. The contribution of quantization noise from the ΣΔ modulator becomes larger in the latter case, that is, we know the transmitted waveform will have a lot of noise when the loop bandwidth of the PLL is wide.

Eye patterns of the transmitted signal with three loop-bandwidth values for the PLL are shown in Figs. 4.3.3, 4.3.4, and 4.3.5. For this simulation, the order N of the ΣΔ modulator is set to two, and we set ω_c to 9 kHz in Fig. 4.3.3, 12 kHz in Fig. 4.3.4, and 17 kHz in Fig. 4.3.5. Further conditions of simulation are a large frequency drift of 600 Hz/μs for the VCO, due to noise and leakage current, and a 1-MHz sampling frequency for the ΣΔ modulator.

The figures show that a wide loop bandwidth for the PLL makes it very difficult to get an output modulated wave that contains little noise.

On the other hand, too narrow a loop bandwidth means that the PLL cannot compensate for VCO frequency drift due to noise or leakage current.

Results of simulation of the frequency drift rate vs. the loop bandwidth of the PLL are plotted in Fig. 4.3.6, along with the specified rate for Bluetooth. For the simulation shown in Fig. 4.3.6, we considered the noise sources and leakage currents occurred in PLL as the equivalent noise source at the VCO input. We measured the frequency fluctuations over the all conditions of temperature and supply voltage variations and set the VCO parameters in the simulation with the worst case drift of 600 Hz/μs. The figure clearly shows that a loop bandwidth of more than 6.5 kHz is necessary for tracking of the worst case VCO frequency drift.

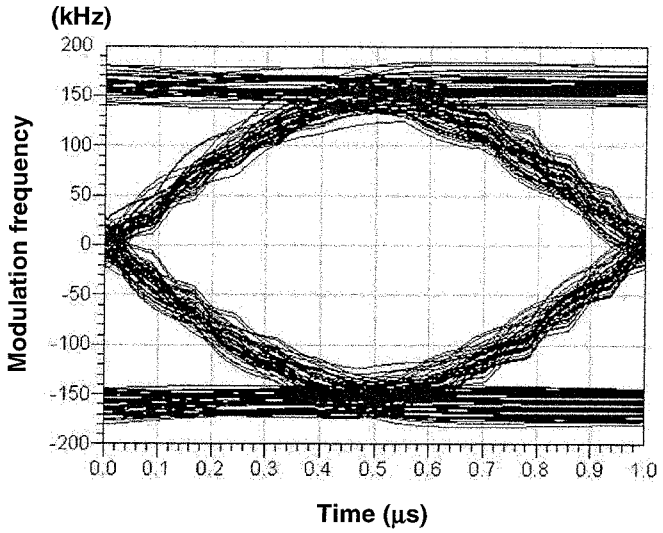


Figure 4.3.3 Eye pattern (loop bandwidth is 9 kHz)

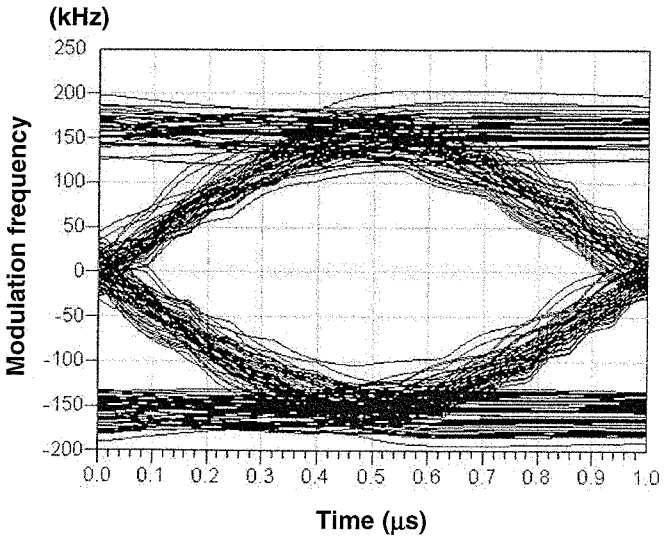


Figure 4.3.4 Eye pattern (loop bandwidth is 12 kHz)

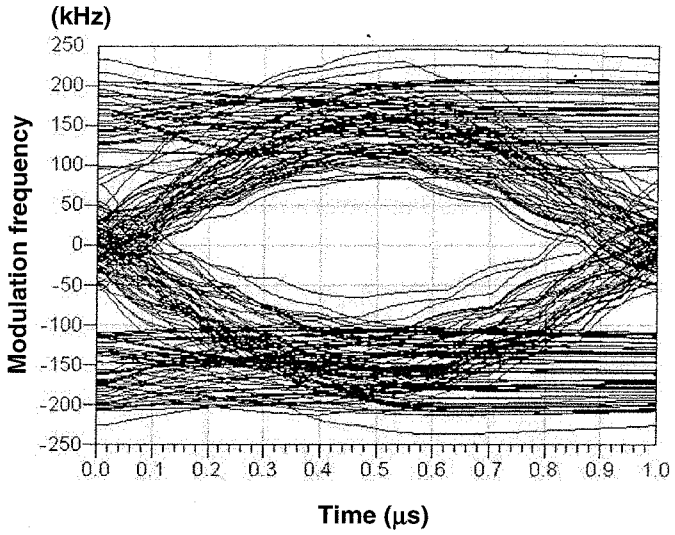


Figure 4.3.5 Eye pattern (loop bandwidth is 17 kHz)

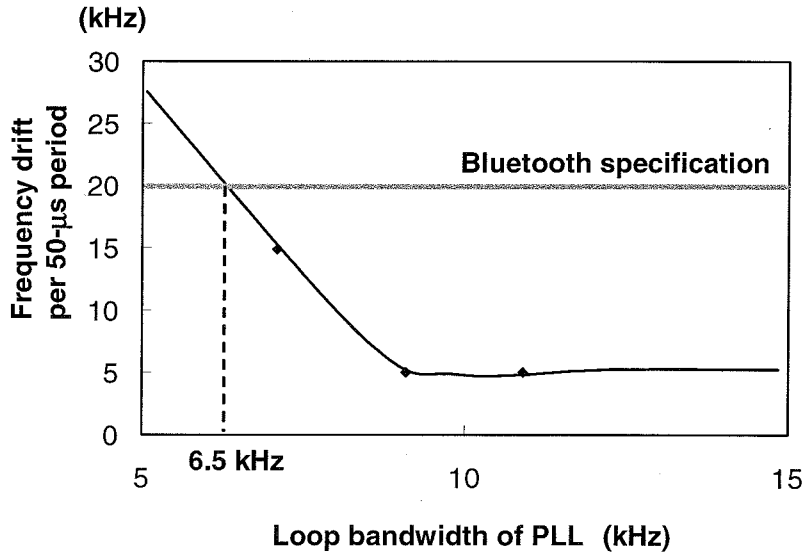


Figure 4.3.6 Frequency drift rate: result of simulation

4.3.5 Adaptive loop bandwidth control

The Bluetooth specification requires that the PLL has a convergence time less than 220 μs. Since a margin for stabilization must also be necessary, the PLL convergence must be completed somewhat before 220 μs. The settling time of a PLL is known to be a function of ω_n, where ω_n is the

free-running frequency of the PLL [79]. We selected a loop bandwidth of about 6.5 kHz for the PLL, for the reason discussed in section 4.3.4. Furthermore, we use a damping factor of $\zeta \fallingdotseq 1$. We then use Eq. (4.3.4) to get a rough estimate of settling time. The largest possible frequency hop BW in Bluetooth is 80 MHz and we assume a frequency error Δf of less than 100 Hz in the steady state. This assumption leads to

$$T = -\frac{\ln\left[\frac{\Delta f}{BW}\right]}{\zeta\omega_n} \approx -\frac{\ln\left[\frac{100}{80\times10^6}\right]}{2\pi\times6.5\times10^3} \approx 330\,\mu s \quad \cdots \quad (4.3.4).$$

The result indicates that settling within the required time period is not possible when the PLL has a narrow loop bandwidth. In this Chapter, we examine a technique where the loop bandwidth of the PLL is changed in multiple stages to achieve a shorter settling time.

A time chart from the point at which the Bluetooth transceiver activates the transmitter to just after the start of transmission is given as Fig. 4.3.7. The factors that significantly obstruct convergence by a PLL are also indicated in the figure. The top plot in Fig. 4.3.7 shows the VCO's frequency of oscillation. Successively lower plots show the PLL-start signal, PA-start signal, Bw-sel signal, and DATA (Tx data transmission).

Convergence of the PLL starts when the PLL-start signal goes high (t_0). At this time, a wide loop bandwidth is selected for the PLL, so settling is relatively fast at the beginning of convergence. In this case, we set a loop bandwidth of 40–60-kHz to obtain a settling time shorter than 100 μs for the PLL. Next, the PA is activated at point t_1. Activation of the PA changes the VCO frequency by several hundreds of kilohertz, even if the PA circuit block is mounted with an independent power supply and ground line. For this reason, PLL re-convergence is required to return the VCO to the frequency assigned for transmission.

Next, after the PLL has settled such that the VCO is within a small error frequency of the assigned frequency, the loop bandwidth of the PLL is made narrower (point t_2). However, a further very short period of re-convergence is required because of the change to the loop bandwidth, since the control signal that changes the loop bandwidth creates noise that reaches the VCO control terminals. Furthermore, the phase error of the PLL relative to the reference clock changes slightly when the loop bandwidth is changed. Therefore, if the VCO has a large frequency drift, we must include additional PLL re-convergence time for worst-case

convergence conditions. Data transmission starts at t_3, that is, after the PLL output has settled at the assigned frequency. The ΣΔ modulator also starts at this point.

To determine an adequate re-convergence time for the transmitter, we measured the frequency fluctuations induced by interference in an actual integrated circuit with open-loop modulation. We assumed that the VCO frequency drift rate was 600 Hz/μs and the frequency change on PA activation was 200 kHz based on the measurements for this study. Of course, these parameters will vary with the component tolerances, wiring layout, and so on. Therefore, our goal is to identify a margin of re-convergence time that is sufficient for use in practical design.

As a result, we selected loop-bandwidth changeover timing of t_1=80 μs and t_2=120 μs, and a final transmission start point of t_3=180 μs. We confirm that the transmitter performance in this case fulfills the Bluetooth specification, even if the loop filter time constant, charge pump current, and VCO voltage-to-frequency conversion gain are varied by changing component values in the integrated circuit through the full range of possible variation. The results of simulation, including initial frequency deviation f_0 < 10 kHz, frequency drift < 16 kHz, and eye-opening ratio > 0.95, indicate the validity of our proposed transmitter architecture. Here, we set the narrower condition of loop bandwidth for the PLL to 9 kHz, providing a margin above the 6.5-kHz minimum in consideration of manufacturing dispersal in the active and passive elements of the IC.

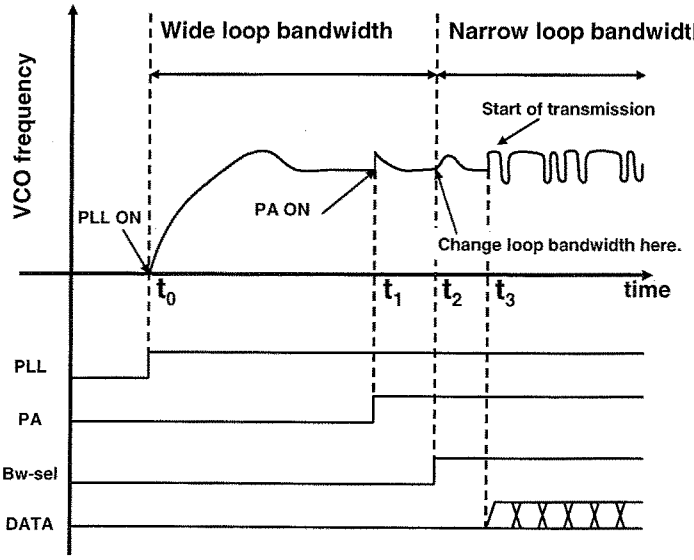


Figure 4.3.7 Start-up time chart and VCO frequency fluctuation

4.3.6 Modulator for divider control

We can adopt a ΣΔ modulator as a modulator. Firstly, a block diagram of a first-order ΣΔ modulator is given as Fig. 4.3.8.(a). The coefficient m is a modulation index, and in our case is multiplied by the data signal, Tx. Given the typical modulation index required by the Bluetooth specification of 0.16 and a setting of 2400 as the divisor for the divider in Fig. 4.3.2, the difference between the period of the divider output and the period of the reference clock is 69.2 ps. This value is almost equal to 1/6 (0.16666) of one period (416 ps) of the 2.4-GHz radio frequency signal used in Bluetooth. Therefore, we input Tx to the ΣΔ modulator after multiplication by m=0.16.

The first-order ΣΔ modulator consists of an integrator (labeled $z^{-1}/(1-z^{-1})$), a quantizer (Q), which detects the polarity of the output of the integrator and outputs plus or minus one, and a subtractor, which calculates differences between the output of Q and the input.

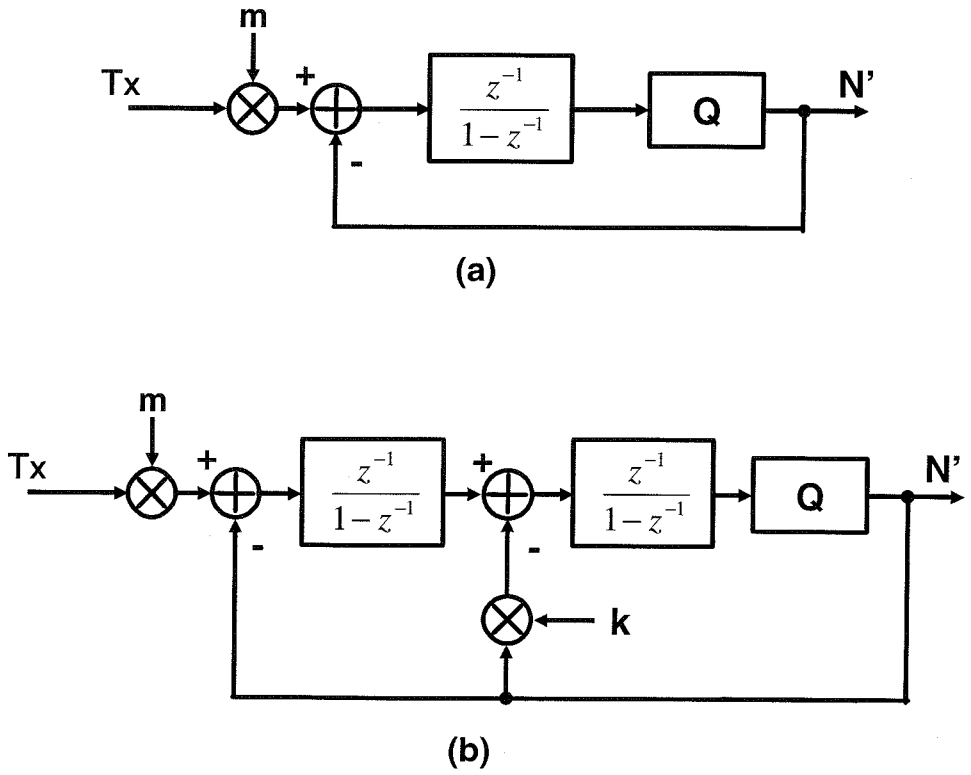


Figure 4.3.8 ΣΔ modulator
(a) first-order modulator (b) second-order modulator

After adjusting the delay of the output (N') of the ΣΔ modulator to match the fixed delay of the DAC in the path from the Tx input to the V_{C2} terminal minus the set-up period required for control of the divider, closed-loop modulation is initiated by applying N to the divider of the PLL.

Next, a block diagram of a second-order ΣΔ modulator is given as Fig. 4.3.8 (b). The structure differs from that of the first-order ΣΔ modulator in the inclusion of an additional subtractor, which subtracts the output of Q from the output of the first-stage integrator. Multiplication by the coefficient k before subtraction is adopted for stability. We use k=2 in our application.

The unique sequence "1010" is continuously transmitted for measurement of the center frequency in Bluetooth transmission. When this sequence is inputted to the first-order ΣΔ modulator, either of two output conditions is possible: continuous output of "1, 1, −1, and −1," and continuous output of "1, −1, 1, and −1." These two output patterns from the modulator are caused by differences of their initial value of the integrator of the first-order ΣΔ modulator. Of course, the average frequency is the same in both cases. However, unsatisfactory frequency drift and frequency-drift rate occur when being the former condition. The simulated response of the two-point modulator when the sequence "1, 1, −1, and −1" is continuously outputted from the first-order ΣΔ modulator is shown in Fig. 4.3.9, where the vertical axis represents modulation frequency and the horizontal axis represents time (the transmitter is activated at 180 μs). A large frequency drift of 41.5 kHz and fast frequency-drift rate of 54.2 kHz per 50-μs period are observed under the former condition, while there is no frequency drift under the latter condition. Therefore, we conclude that adopting the first-order ΣΔ modulator into the transmitter is not adequate for Bluetooth applications.

The advantage of the second-order ΣΔ modulator in this case is that it does not output a periodical fixed pattern. However, if the center-frequency-measurement pattern specified for Bluetooth, i.e. continuous repetition of "1, 0, 1, 0," is inputted to the modulator, the output of the second-order ΣΔ modulator does tend to output a fixed pattern. Frequency drift occurs just after the ΣΔ modulator is activated because of the discontinuity conveyed to the PLL, and we simulate the frequency drift in this case. Fortunately, the simulation shows that the

second-order ΣΔ modulator is effective in this application, since the results of simulation for frequency drift are lower than 8 kHz under all conditions.

Fig. 4.3.10 shows the center-frequency drift of the transmitter with the second-order ΣΔ modulator when loop-bandwidth switching is adopted. In Fig. 4.3.10, the transmitter is activated at 10 μs. This simulation is done with the maximum possible frequency drift of the VCO due to leakage current and the greatest possible level of interference due to PA activation.

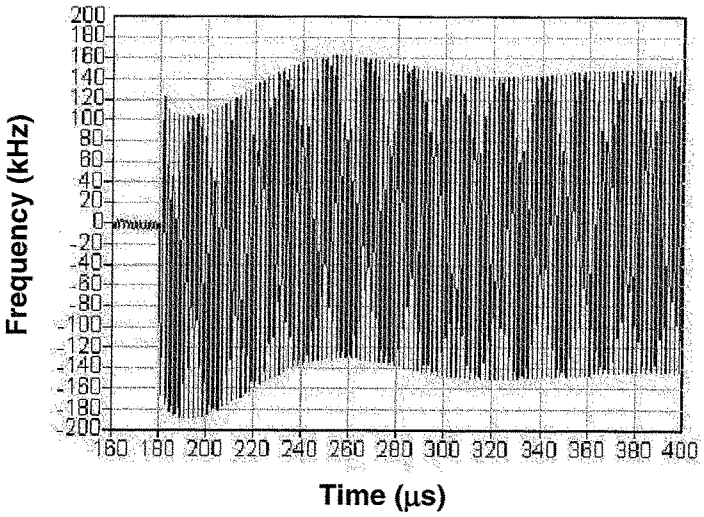


Figure 4.3.9 Result of simulation for frequency drift when using first-order ΣΔ modulation

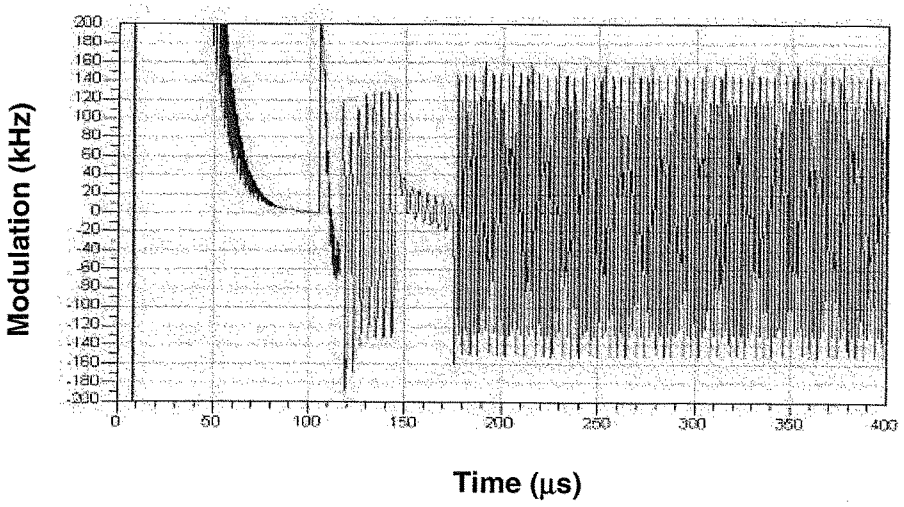


Figure 4.3.10 Result of simulation for frequency drift when using second-order ΣΔ modulation

4.3.7 Calibration for two-point modulation

For correct operation of the two-point modulator, we must design paths A and B in Fig. 4.3.2 to have equal gain. As is shown in Fig. 4.3.2, a gain-adjustment function in the form of the calibration circuit (Cal.) is included in this IC. Fixed voltages are independently supplied to each of the control terminals, V_{C1} and V_{C2}, and the counter in the divider is used to count the VCO output. We can then estimate the error frequency through comparison with the reference clock, which is generated by a crystal oscillator. We adopted the same method for this frequency comparator which has already developed [36].

Calibration can thus be completed in a short time by using a very simple and easy structure, with the only extra requirement being the calibration circuit for the DAC. Furthermore, calibration is carried out automatically when power is supplied, and the function thus always corrects any gain imbalance between the two paths to the two-point modulator.

4.3.8 PSRR improvement technique for VCO

The VCO is the most important circuit component for good transceiver performance. The VCO must have a phase-noise level below −120 dBc/Hz for Bluetooth applications and be immune to variation in the supply voltage, VCC. Fig. 4.3.11 shows the VCO circuit. It has two control terminals, V_{C1}, V_{C2} and tanks tapped by capacitors are used to provide the same ground plane for both control-terminal voltages. A single negative capacitor (C_5) ensures that the oscillation frequency of the VCO is not decreased by the parasitic capacitance of the inductor.

The transistors, Q1 and Q2, are in a cross-coupled structure, creating a negative transconductance. Fluctuation of the bias levels, V_{b1} and V_{b2}, leads to variation of the parasitic capacitances of the transistors, which in turn leads to variation of the oscillation frequency. Avoiding this by ensuring that V_{b1} and V_{b2} are fixed is not appropriate, since the voltages between the bases and collectors of Q_1 and Q_2 will still vary with VCC. This leads to fluctuations in the frequency of oscillation such that the power-supply rejection ratio (PSRR) for oscillation frequency is poor.

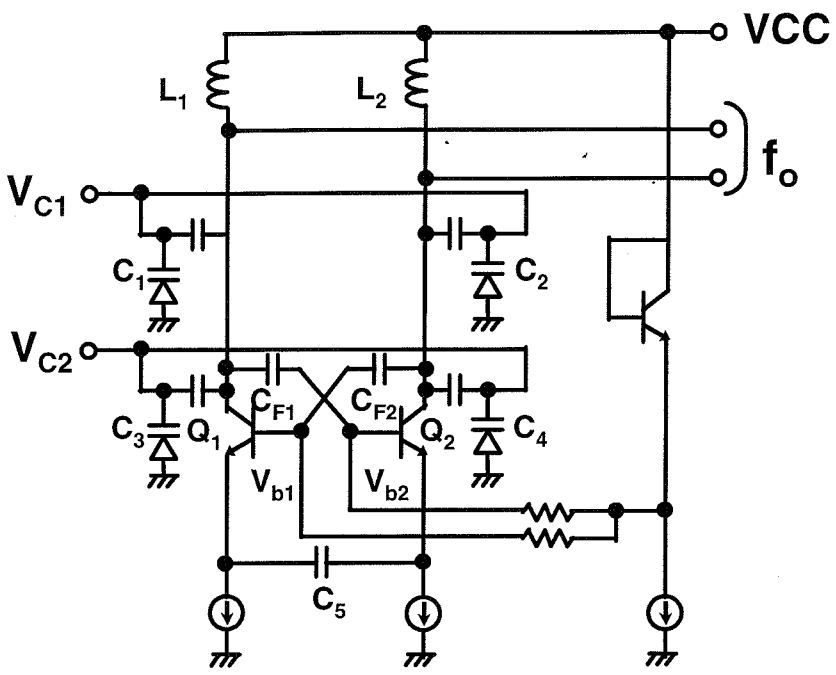


Figure 4.3.11 PSRR improved VCO

The biasing method we propose avoids both problems. As we see in Fig. 4.3.11, biasing voltages V_{b1} and V_{b2} are derived from VCC, so that the voltage between the bases and collectors of Q_1 and Q_2 are kept stable and is less dependent on variations in VCC.

4.4 Results of PLL modulator measurements

4.4.1 Measurement results of feedback loop modulator

Firstly, we fabricate an entire serial ATA transceiver with a 0.15-μm CMOS process to verify the proposed PLL with the feedback loop modulation. Fig. 4.4.1 is a chip photograph that shows only the transceiver's SSCG block. The block size is 0.88x0.48 mm^2. The counter-controller block consists of logic cells and occupies a very small area. Since the VCO is the most noise-critical element of the generator, we placed it here to keep the length of the line from the loop filter short.

Fig. 4.4.2 plots the measurements of Vc-frequency characteristics. The VCO has good linearity and its conversion gain of 3.4 GHz/V between Vc= 0.5 and 1.2 V. The VCO can oscillate up to 2.5 GHz.

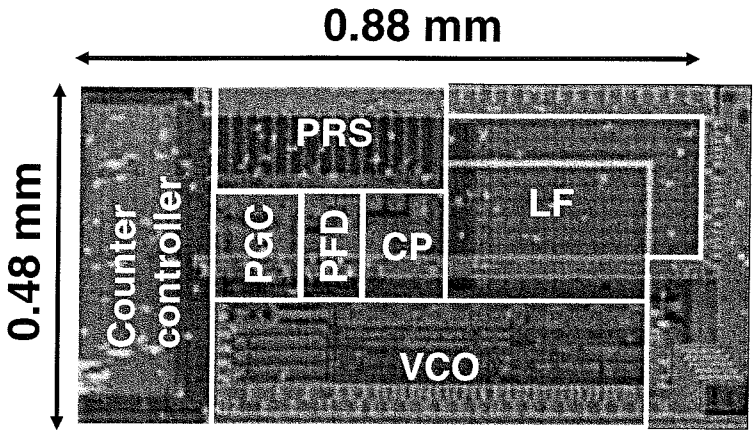


Figure 4.4.1 Chip photograph of SSCG block

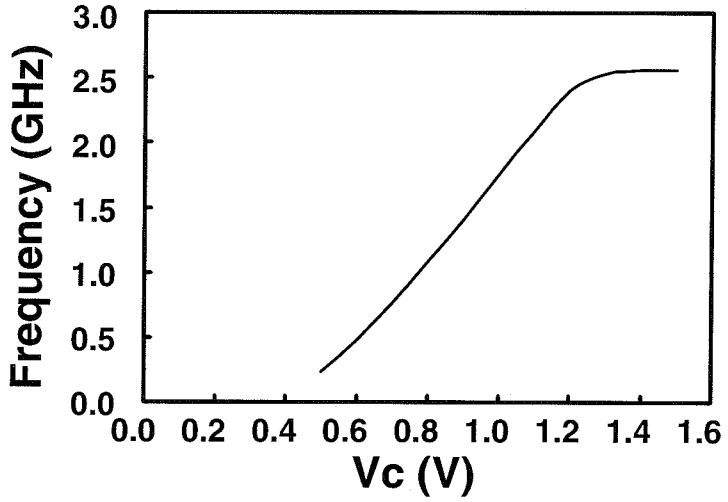


Figure 4.4.2 VCO control voltage-to-frequency conversion characteristics

Fig. 4.4.3 plots the measured results of the phase noise. For this measurement, we set the PLL's output frequency at 1.5 GHz. The x-axis represents the offset from the PLL output frequency, and the y-axis represents the phase noise at the VCO's output. At the range lower than 10 MHz, ΣΔ modulation produces very little noise. The very low levels of measured phase noise correspond to low levels of jitter and are consistent with the simulation results. The loop bandwidth of the PLL has to be wide enough to modulate a triangle wave. A loop bandwidth of 300 kHz, about 10 times wider than the frequency of the triangle wave, 31.1 kHz, is used.

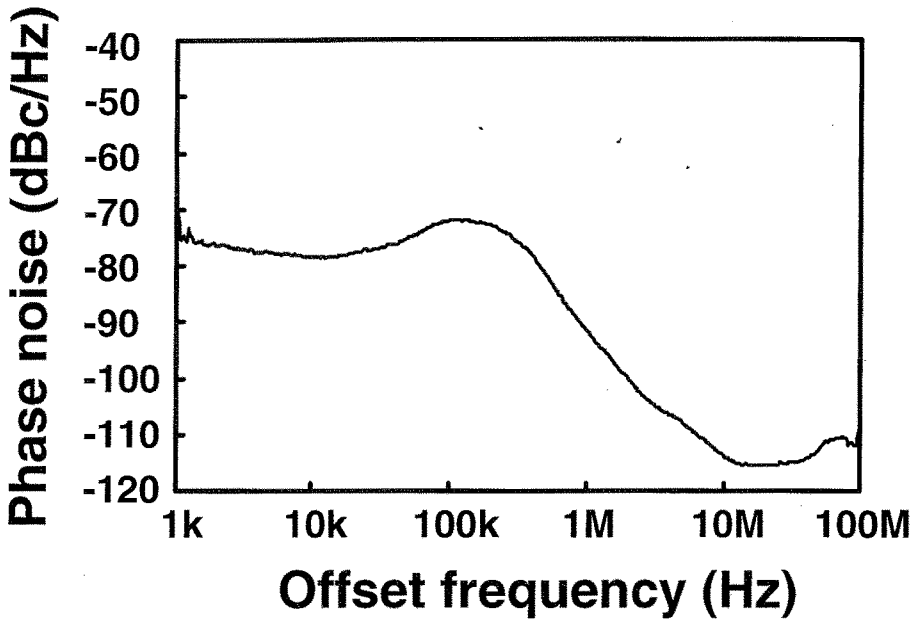
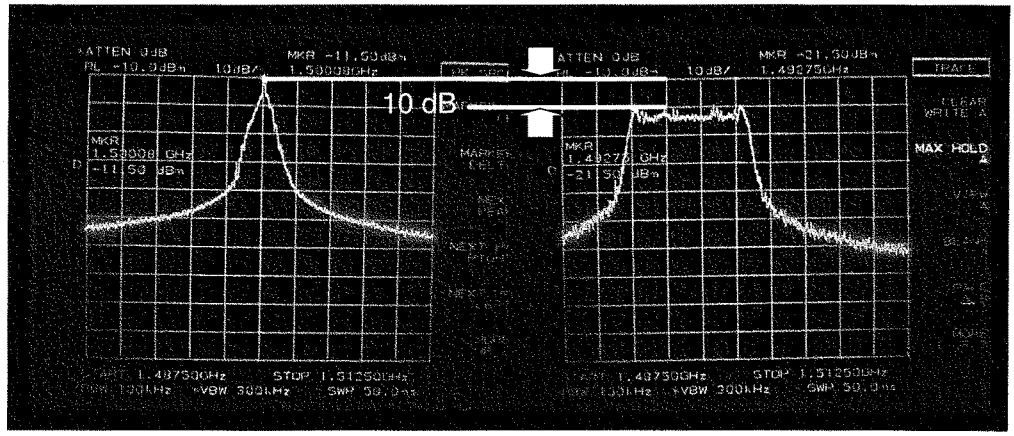


Figure 4.4.3 Measurement of PLL output phase noise



(a) Spectrum w/o spread spectrum (b) Spectrum with spread spectrum

Measurement conditions: BW=100 kHz, VBW=300 kHz,
Center frequency=1.5 GHz, Span=25 MHz
Peak Hold Mode

Figure 4.4.4 Measurement of EMI peak power reduction

Fig. 4.4.4 shows the measurement results of the SSCG output spectrum. The vertical axis is normalized by the oscillation power level of the clock generator when the spread-spectrum block is inactive. Therefore, a peak reduction level of 10 dB is achieved using SSCG when the

resolution bandwidth is 100 kHz. The techniques applied in our SSCG produced the largest reduction in EMI peak and no extra spurs caused by the ΣΔ modulation happen.

The SSCG measurement results are summarized in Table 4.4.1. Jitter of 8.1 ps with a 250-cycle averaging period, which is suitable for serial ATA, has been achieved. The SSCG consumes 36 mA from a 1.5-V supply.

Table 4.4.1 also compares our measurement results with the results of previous works. The circuits corresponding to those in [28][29], and [80] were designed as serial ATA clock generators. Our results for EMI peak-power reduction are better than those of the earlier works.

The measured jitter in [80] is very good random one, however, the PLL has a large amount of deterministic jitter caused by a unique clock control method that uses a first-order ΣΔ modulation. This is because first-order ΣΔ modulation outputs a periodic sequence that is converted to deterministic jitter from the PLL output. The proposed SSCG has lower power consumption than that in [80] because the relaxed random jitter requirement makes reducing the power consumption of the VCO easier. This comparison and our evaluation results show that the proposed PLL with a third-order ΣΔ modulation is highly suitable for a circuit with low-jitter spread-spectrum signal generation.

Table 4.4.1 Measurement results and comparison with the prior works

	This work	[28]	[29]	[80]	Spec.	Unit
Modulation method	ΣΔ	Phase Interpolation		ΣΔ	-	
EMI reduction	10.0	(5.4)	(7)	9.8	> 7	dB
Random jitter of PLL	8.1	-	9.3	3.2	< 12	ps rms
Deterministic jitter of PLL	0.3	-	-	13.6	< 133 (with driver)	ps p-p
Modulation bandwidth	+0.035/ -0.500	+0/ -0.37	+0/ -0.515	+0.0/ -0.500	+0.035/ -0.500	%
Technology	0.15	0.15	0.13	0.18	-	μm
Power	54	-	-	77	-	mW

4.4.2 Measurement results of two-point modulator

The proposed two-point modulator technique is demonstrated by fabricating a transmitter based on in a Bluetooth RF-LSI using 0.35-μm BiCMOS technology. A chip photograph of the transmitter block is shown in Fig. 4.4.5.

Fig. 4.4.6 shows the results of PSRR measurement for the proposed VCO and a fixed biasing VCO. The proposed biasing method is highly effective. Results of phase-noise are shown in Fig. 4.4.7. A good phase-noise characteristic is attained, with −128 dBc/Hz at a 3-MHz offset frequency.

The result of frequency analysis of the transmitter output is shown in Fig. 4.4.8. The vertical axis represents the frequency deviation from the center frequency of the specified channel and the horizontal axis represents the time relative to activation of the transmitter. Results under two measurement conditions are given in the figure: (a) operation with conventional direct VCO modulation and (b) operation with the proposed technique. The figures show the first two-thirds of a single transmission slot.

The transmitter with conventional direct VCO modulation has a center-frequency drift of 178 kHz in a single time slot (625 μs). The new circuit reduces the center-frequency drift to 14.9 kHz. The difference is clearly visible in Fig. 4.4.8(b), demonstrating the effectiveness of the proposed modulation technique.

The transmitter's output spectrum and eye pattern are shown in Figs. 4.4.9 and 4.4.10, respectively. The measured −20-dB bandwidth of the output spectrum is 705 kHz and the eye-opening ratio is 0.87. The transmitter thus has good performance as a GFSK modulator.

Results of evaluation for the transmitter with the proposed two-point PLL modulator are summarized in Table 4.4.2. It is confirming satisfaction of all items required by the Bluetooth specification.

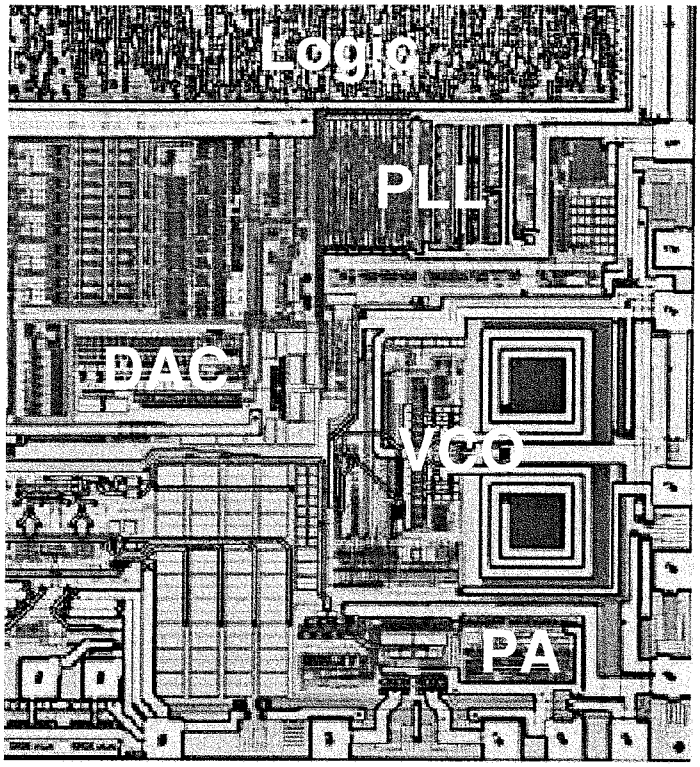


Figure 4.4.5 Chip photograph of the transmitter block

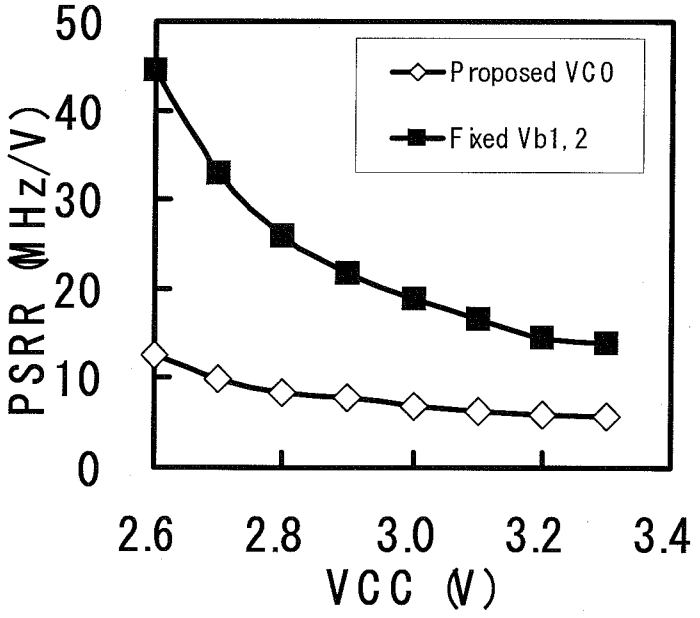


Figure 4.4.6 Results of PSRR measurements

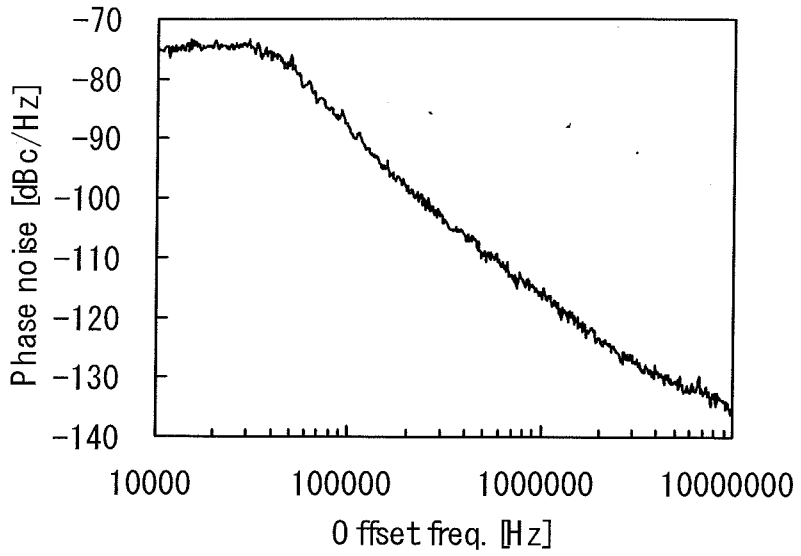


Figure 4.4.7 Results of phase-noise measurement

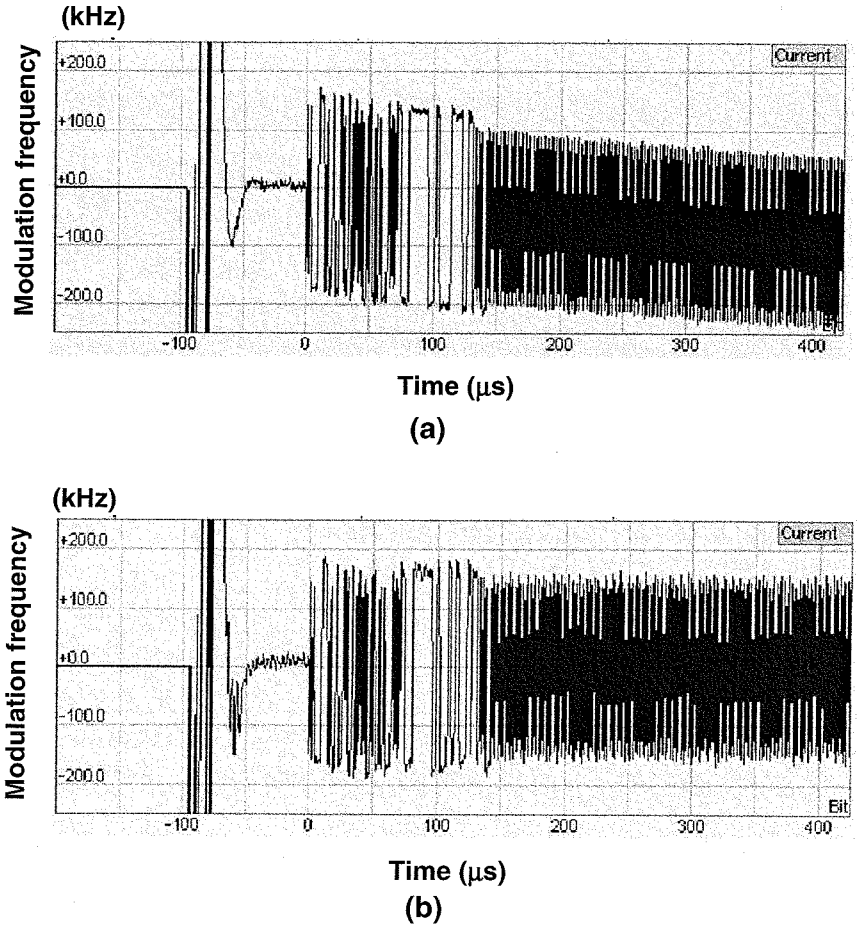


Figure 4.4.8 Transmitter center-frequency drift
(a) when the PLL is inactive (b) when the PLL is active

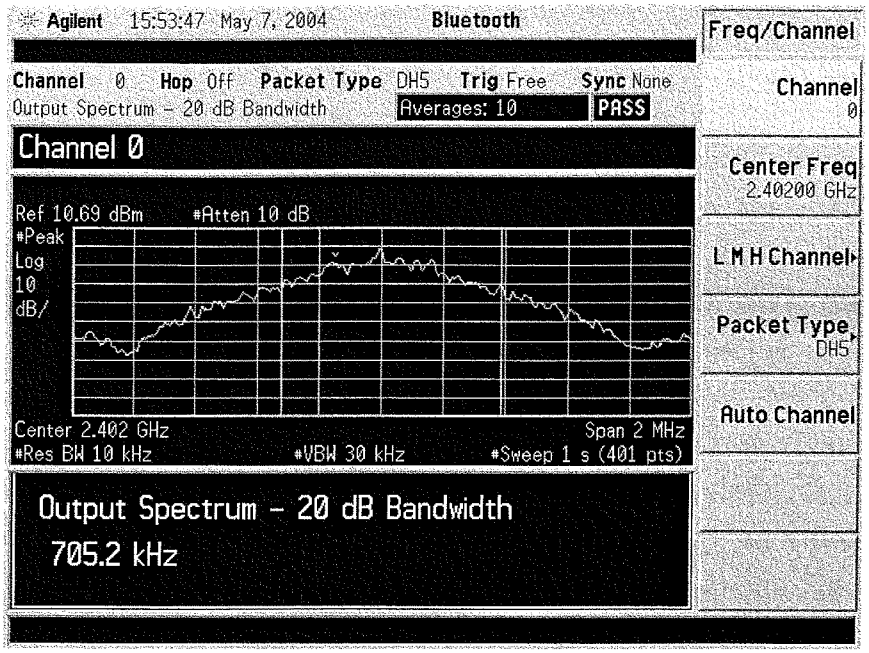


Figure 4.4.9 Output spectrum of the transmitter

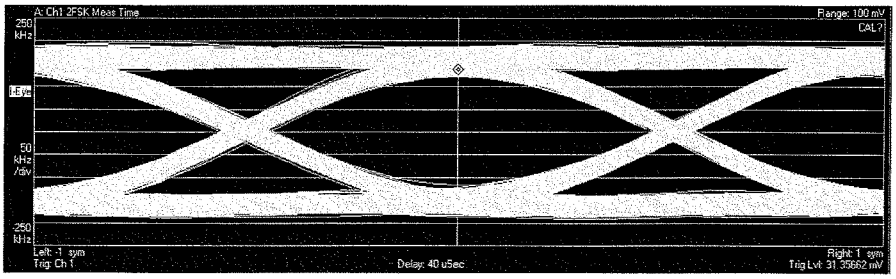


Figure 4.4.10 Transmitter eye pattern

Table 4.4.2 Evaluation results

No.	Item		Bluetooth specification	Evaluation results
1	Initial frequency offset		< ±25 kHz	-10.7 kHz
2	Center frequency drift		< 25 kHz	14.9 kHz
3	Frequency drift rate		< 20 kHz/50 μs	6.9 kHz/50 μs
4	Frequency deviation	Average	140 - 175 kHz	164.5 kHz
5		Minimum	> 115 kHz	122.9 kHz
6	Eye-opening ratio		> 0.8	0.87
7	-20-dB bandwidth		< 1 MHz	0.705 MHz
8	In-band spurious	< 2MHz	< -20 dBm	-49.5 dBm
9		> 3MHz	< -40 dBm	-53.8 dBm
10	Out-of-band spurious		< -30 dBm	-37.8 dBm
11	PLL settling time		< 220 μs	180 μs

4.5 Conclusion

Two applications concerning to modulators using PLLs and designs for the PLLs have been described in this Chapter. One is the PLL for the spread-spectrum clock generator and the other is for the Bluetooth transmitter. The techniques used in the PLLs are very effective to integrate system level functions and can eliminate a lot of expensive external components.

At the first section of this Chapter a spread-spectrum PLL for serial ATA applications have been explained. Firstly, we have investigated the relation between the output jitter of the PLL in serial ATA applications and the ΣΔ modulator's order of the PLL. On the basis of this investigation, we have achieved both of small jitter and large EMI peak power reduction through two key components, i.e., the PLL with the multi-bit ΣΔ modulator and the VCO with cross-coupled load delay cells.

Next, a two-point modulator with variable PLL loop bandwidth has been proposed for use as a GFSK signal generator of the Bluetooth transmitter. ΣΔ modulation is applied in the input of the two-point modulator. During actual transmission, the ΣΔ modulator shifts quantification noise to higher frequencies; using the PLL with a narrower loop bandwidth then prevents deterioration of the eye opening at the output. On the other hand, the loop bandwidth of the PLL is set wide for fast convergence during the earliest stage of settling. The combination of these techniques in this new two-point modulator achieves both a fast settling time and very clear and well-defined eye openings.

These two modulators using PLLs have been fabricated to verify their performance. Firstly, using a 0.15-μm CMOS process, we have fabricated a complete serial ATA transceiver featuring the SSCG. Measured results for SSCG performance have been very good, and have shown that the generator satisfies all serial ATA specifications. The results support the validity of our new techniques for PLL-based spread-spectrum clock generation.

Next, the Bluetooth RF-IC has been fabricated in 0.35-μm BiCMOS process technology. Center-frequency drift is much lower with the proposed two-point modulator than with direct VCO modulation (14.9 kHz vs. 178 kHz, both for a single time slot). This demonstrates the

effectiveness of the PLL feedback loop in reducing drift due to leakage current and noise. Furthermore, evaluation has confirmed that the transmitter satisfies all of the various conditions of the Bluetooth specifications.

Moreover, this two-point modulator is applicable to other transceivers in which frequency shift keying or phase shift keying modulation is used, that is, where transmission is at a constant signal level, and thus contributes to the simplification of a wide range of wireless transmitters.

These techniques described in this Chapter are very useful to integrate in many kinds of SoC applications and will increase numbers of applications in the near future because mobile communication will need to use multi-band and more complex coding method, and a PLL has a potential feature to deal with these requirements.

Chapter 5

General Conclusions

A PLL is one of the most important circuit blocks in many semiconductor integrated circuits, such as microprocessors, wireless transceivers, and signal processing units. Recently SoCs require various features of PLLs in a single chip, for example, the on-chip high-speed clock generation, the frequency synthesizer, and the clock phase synchronizer especially in the finer CMOS design rule processes.

In Chapter 2, a basic structure of a PLL and its applications are explained. A PLL as one kind of control systems is constructed by quite simple feedback loop. A PLL only consists of four key elements, a phase detector, a charge pump, a voltage controlled oscillator, and a divider. PLL performance degradations over many non-idealities, low supply voltage, large leakage current, and so on, which would be occurred in the fine design rule CMOS processes, has been explained. Next, PLL design in general and design of its key functional elements have been discussed. Furthermore, modulators for continuous envelope signal using PLL and their operation have been described. Finally, requirements to PLL integration are summarized by explaining on chip PLL design for an SoC and a wireless transceiver.

In Chapter3, new PLL techniques especially to be adopted into the semiconductors using fine design rule processes have been introduced and how to achieve PLL performance under low supply voltage have been

explained. A new PLL architecture has been proposed and then circuit design techniques of the charge pump, the loop filter, and the VCO, which are suitable circuits under low supply voltage and high frequency operation, have also been proposed. Especially, the effective circuit technique for the VCO with the feed-forward path and the common load transistors has been proposed. These techniques for the LV/LP PLL have been verified by the measurements of the fabricated PLL.

In Chapter 4, the modulators using the PLLs have been explained. Total system performance including PLL is discussed for this new application wireless transceivers and storage signal processing ICs. They need to integrate PLLs, which must meet with much severe specifications. Two design examples have been discussed in this dissertation. One of them is the PLL feedback loop modulation used for the spread-spectrum generator to reduce EMI and the other is the PLL with two-point modulation for applying to the GFSK transmitter of the Bluetooth transceiver. The PLL structures and main circuit techniques in details have been also discussed. For the spread-spectrum modulation, two key components: PLL with multi-bit $\Sigma\Delta$ modulator and VCO with cross-coupled load delay cells have been proposed. And then the two-point modulator with variable PLL loop bandwidth for the Bluetooth transceiver has been proposed. All features which have been described in this dissertation have been verified by the measurements for these special applications of serial ATA transceivers and Bluetooth transceivers and have also met their difficult system requirements.

For future research topics, it will be popular to use the third generation and/or the forth generation cell phone systems worldwide. Such cell phones include many features of multimedia signal processing, not only voice services. Therefore, in these cell phones, high performance processor with low power consumption should be integrated in a single-chip LSI. To meet this low power trend, it is necessary to design PLL circuits under supply voltage lower than 1 V. For the next decade, much finer design rule process than 0.1-μm CMOS process will be used. Transistors fabricated with such a fine design rule will have lower breakdown voltage, and then the lower supply voltage circuit techniques are significantly important issues for not only a PLL but also the other analog circuits.

Next, the phase noise requirement is quite severe issues because the

cell phone transmits digital data by using phase modulation to RF signal. Therefore, PLLs in cell phones are usually for generating pure local RF signals, however, for recent years, it becomes popular that phase modulation in the transmitter realized by a PLL to minimize numbers of external comportments of LSI. The modulators using a PLL became very important technical issues currently because a transmitter using PLL can reduce a number of external components and can have a good potential to achieve better performance than that of the conventional modulator with mixers. The strong requirements from users of eliminating external high-Q filters in transceivers are continuously increasing. Then it will be popular to integrate the PLL into modulators with band selection filters for replacing the conventional ceramic or SAW filters. PLLs for these applications need to generate very small phase noise and wider phase modulation range. Therefore it is very important to construct a PLL with less jitter and signal processing noise.

Conclusively the PLL techniques for good performance under low supply voltage which have been proposed in this dissertation are extremely important for the designs of analog-digital mixed signal processing ICs.

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