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Doctorial Thesis

A Study on Silicon-on-Thin-BOX (SOTB) CMOSFET for Low-Power LSIs

Takashi Ishigaki

September, 2012

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Co-supervisor: Prof. Nobuyuki Sugii

Abstract

Planar bulk CMOSFETs, which has led the device scaling trend so far, is going to end, because its large threshold voltage (V_{th}) variation significantly increases the power consumption of LSIs. Silicon-on-thin-BOX (SOTB) CMOSFET, which was fully depleted silicon on insulator (FD-SOI) with an ultrathin BOX, was proposed to realize high-performance and low-power LSIs by solving the V_{th} variation issue. The studies described in this thesis were accomplished in order to realize SOTB CMOSFET for low standby power (LSTP) in 65-nm generation and show the effectiveness of SOTB technology for reducing the power consumption quantitatively. The studies for utilizing the SOTB technology such as peripheral circuits and reliability are also described.

Firstly, the scaling of CMOSFET and the power consumption issues of recent LSIs which are caused by the variability of conventional planar CMOSFETs are introduced in chapter 1. As a solution of the problem, the concept and features of SOTB CMOSFET are described. The previous works and the purpose of this thesis are also presented in detail.

In chapter 2, the fabricating processes of SOTB CMOSFET in 65-nm generation are described. A simple fully silicided (FUSI) gate structure by using nickel silicide (NiSi) as the gate metal was combined with a raised source/drain (S/D) structure by using a selective epitaxial growth (SEG). The obtained desirable V_{th} values and low parasitic S/D resistance (R_{sd}) result in better performance than those of planar bulk CMOSFETs in the same generation. The special features of SOTB CMOSFET, that is, low V_{th} variation and wide-range back-bias control are also demonstrated.

In chapter 3, the reduction of power consumption by using SOTB technology is presented. Firstly, the off-current of SOTB CMOSFET was examined and the ultralow off-current less than 1 pA/μm was achieved by controlling the overlap length (L_{ov}) between the gate and S/D extensions. A boosted performance by using back-gate biasing was experimentally demonstrated in this ultralow off-current case. The V_{th} variation of SOTB CMOSFET was

successfully reduced to half in comparison with conventional bulk CMOSFETs even under the wide-range back-biasing. The impact of the low V_{th} variation can reduce the supply voltage of 6T-SRAM from 1.1 to 0.6 V. The reduction of standby power consumption in 6T-SRAM was also estimated to be reduced to 7%.

In chapter 4, a novel hybrid integration of SOTB and bulk CMOSFETs is introduced. By using the ultrathin SOI and BOX layers of SOTB structure, the conventional bulk CMOSFET for input/output (I/O) circuits was fabricated at the same time. There was a concern about the exposed Si substrate in this process. Hence, the quality and reliability of the gate dielectric were investigated. The comparable characteristics with conventional devices in the mobilities and time dependent dielectric breakdown (TDDB) are shown.

In order to put a new device structure in practical use, it is more important than anything to establish its reliability. Hot carrier injection (HCI) for SOTB NMOSFET and negative bias temperature instability (NBTI) for SOTB PMOSFET are investigated in chapter 5. The effects of the back-gate biasing for these phenomena were also analyzed. In this kind of device (FD-SOI with back-bias control), it is noted that these studies were the first trial. It is clarified that the intrinsic channel without halo implant of SOTB CMOSFET result in superior reliability to conventional bulk CMOSFETs. It is also presented that the back-biasing has impact on the HCI but on the NBTI with their mechanisms.

In late 2000s, trends of studies for metal gate technology were shifting toward metal-inserted polycrystalline-silicon (MIPS) gate structures. Since the FUSI gate process is hard to control its uniformity when mass production is assumed, the MIPS gate structure using TiN for SOTB CMOSFET is studied in chapter 6. The effective work function modulation was found in the case of conventional SiON gate dielectric. The way for obtaining the desirable V_{th} values considering the SOTB process is shown. The difference of the narrow channel characteristics between FUSI and TiN gates were also analyzed.

Finally, the summary and conclusions of this study are described in chapter 7.

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Symbols and Abbreviations

A_{Vt}	Pelgrom coefficient
BOX	Buried oxide
BV	Breakdown voltage
CHE	Channel hot electron
CMOSFET	Complementary metal oxide semiconductor field effect transistor
CVD	Chemical vapour deposition
CMP	Chemical mechanical polishing
C-V	Capacitance-Voltage characteristics
C_{g}	Gate capacitance
C_{load}	Load capacitance
DDD	Double diffusion drain
DIBL	Drain induced barrier lowering
D_{it}	Interface trap density
EDS	Energy dispersive X-ray spectroscopy
EOT	Equivalent oxide thickness
ESD	Electrostatic discharge
EWF	Effective work function
E_{g}	Band gap energy
E_x	Lateral electric field
E_y	Vertical electric field
FBC	Fail bit count
FD	Fully depleted
FUSI	Fully silicided
f	frequency

GIDL	Gate induced drain leakage
GL	Gate leakage
γ	Back-bias factor
HCI	Hot carrier injection
HF	Fluoric acid
HTO	High temperature oxide
IC	Integrated circuit
IEDM	International Electron Device Meeting
I/O	Input/output
IRPS	The International Reliability Physics Symposium
IT	Information technology
ITRS	International Technology Roadmap for Semiconductors
I_{cc}	Through current
I_d	Drain current
I_{dmin}	Minimum drain current
I_g	Gate current
I_{gate}	Gate current
I_{leak}	Leakage current
I_{on}	On current
I_{off}	Off current
I_s	Source current
$I_{standby}$	Standby current of 6T-SRAM
I_{sub}	Substrate current
J_g	Gate current density
k	Scaling factor
LDD	Lightly doped drain
LER	Line edge roughness
LOCOS	Local oxidation of silicon
LPCVD	Low Pressure CVD

LSI	Large scale integrated circuits
LSTP	Low standby power
L_{eff}	Effective channel length
L_g	Gate length
L_{ov}	Overlap length between gate and extensions
MIPS	Metal inserted poly-Si
MOS	Metal oxide semiconductor
MOSFET	Metal oxide semiconductor field effect transistor
NBTI	Negative bias temperature instability
n	Number of transistors
n	Power law slope
N_A	Acceptor concentration
$N_{channel}$	Channel impurity density
N_D	Donor concentration
PD	Partially depleted
PVD	Physical vapour deposition
P	Power consumption
ϕ	Electrostatic potential
RDF	Random dopant flactuation
RIE	Reactive ion etching
RTA	Rapid thermal annealing
R_c	Contact resistance
R_{sd}	Series source-drain resistance
SCE	Short channel effect
S/D	Source/drain
SEG	Selective epitaxial growth
SEM	Scanning electron microscope
SIA	Semiconductor industry association
SIMS	Secondary ion mass spectroscopy
SNM	Static noise margin

SoC	System on a chip
SOI	Silicon on insulator
SOTB	Silicon on thin BOX
SRAM	Statistic random access memory
STI	Shallow trench isolation
SS	Subthreshold slope
TDDB	Time dependent dielectric breakdown
TED	Transient enhanced diffusion
TEM	Transmission electron microscope
TEOS	Tetraethyl orthosilicate tetraethoxysilane
T_{BOX}	BOX thickness
T_{epi}	Epitaxial layer thickness
T_{OX}	Gate oxide thickness
T_{SOI}	SOI thickness
τ_{pd}	Delay time
μ_{eff}	Effective mobility
VLSI	Very large scale integration
V_{bb}	Back-gate bias
V_{bg}	Back-gate bias
V_{d}	Drain voltage
V_{dd}	Supply voltage
V_{ds}	Drain-source voltage
V_{fb}	Flat band voltage
V_{g}	Gate voltage
V_{gs}	Gate-source voltage
V_{s}	Source voltage
V_{stress}	Stress voltage
V_{th}	Threshold voltage
W_{g}	Gate width
x_{j}	Junction depth

Chapter. 1 Introduction – Background and Motive of This Study

Chapter.1 Introduction – Background and Motive of This Study

Contents

1.1 MOSFET scaling
1.2 Threshold voltage variation issues
1.3 Intrinsic-channel MOSFET
1.4 SOTB CMOSFET
1.5 Purpose of this study
1.6 References

1.1 MOSFET scaling

Since the invention of the transistor in 1947, semiconductor industry has continued growing greatly for 60 years and large-scale-integrated circuits (LSIs) have made big changes to our life. It is now possible to realize a large-scale circuit by integrating over billion transistors on one chip. Continuation of these advances, at the pace dictated by Moore's Law in which the number of transistors on a chip will double roughly every year (a decade later, revised to every 2 years) [1.1], has been towed by downsizing Complementary Metal-Oxide-Semiconductor Field-Effect Transistor (CMOSFET).

This scaling rule of MOSFET as shown in Table 1.1 was proposed by Dennard [1.2]. According to this rule, the device parameters should be shrunk by the factor *k*. As a result, the internal electric field of MOSFETs remains constant regardless of the generation. This means the downsizing of MOSFETs can be realized without changing the device structure. Therefore the ideal scaling brings easily high integration and high performance of LSIs.

Table 1.1 The scaling rule [1.2]

Device parameter	
Feature size	
channel length, L_g	**$1/k$**
channel width, W_g	**$1/k$**
junction depth, x_j	**$1/k$**
gate oxide thickness, T_{ox}	**$1/k$**
Channel dopant concentration, N_A, N_D	**k**
Supply voltage, V_{dd}	**$1/k$**

However, the actual scaling of the device parameters has diverged somewhat from the ideal one. For example, the supply voltage was not reduced in the early phase of LSI generations so as to preserve compatibility with the supply voltage of conventional systems. This increased the internal electric field of the MOSFET and caused reliability problems such as hot

carrier effect. To conquer this problem, the device structure with high breakdown voltage, such as double diffused drain (DDD) or lightly doped drain (LDD), has been developed [1.3]. As this example suggested, it could be concluded that various practical restrictions, which were not taken in consideration in the scaling rule, have caused subjects in device development.

1.2 Threshold voltage variation issues

Today's our world is greedy for power. Social system is controlled by information technology (IT). Everything is connected by network and enormous information is computed at any time. Figure 1.1 shows the power dissipation trend of IT equipment in Japan. The power consumption might reach 24 billion kWh / year by 2025. This is the five times higher than the power consumed in 2005. To overcome the power crisis, "green IT" has been proposed. The "green IT" means a energy-saving of IT itself and a energy-saving of social system by IT. LSI technology can make great contribution to the sustainable and innovative society.

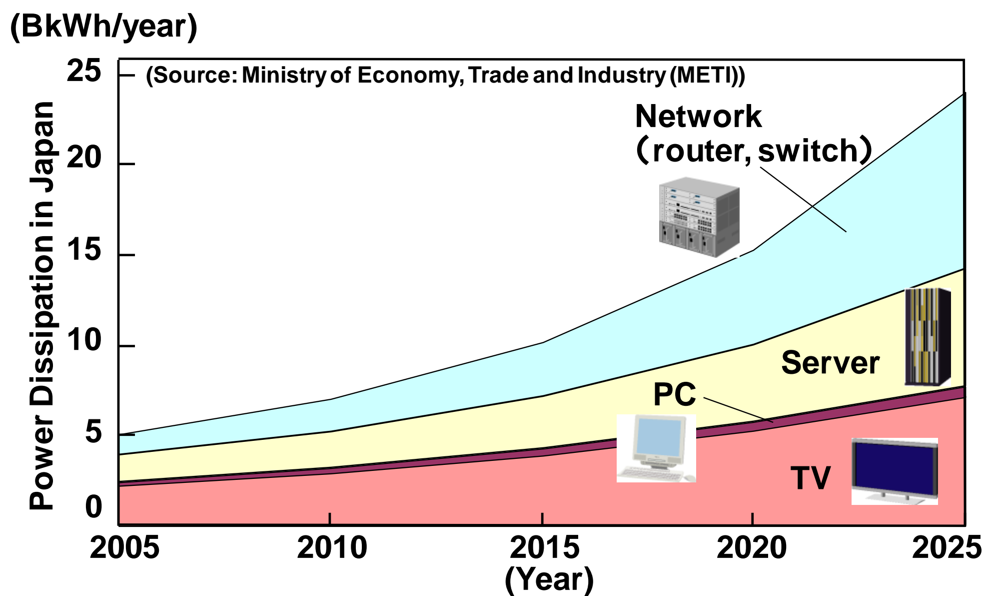


Fig. 1.1 Power dissipation trend of IT equipment in Japan

The scaling rule has been a paradigm for downsizing CMOSFETs in LSI circuits for a long period. In the ideal scaling rule, the supply voltage V_{dd} should decrease in proportion to the downsizing of the transistor. In extremely scaled transistors such as those in the 45-nm logic node and beyond, however, it is very difficult to further decrease V_{dd}. In the ITRS roadmap, the rate of V_{dd} reduction below 1 V is forecasted to be extremely small as shown in Fig. 1.2. This problem is called as "1-V brick wall". Unless V_{dd} is reduced with the scaling rule, the power consumption of the LSI will increase significantly due to an increase in both operational and standby-leakage power [1.4], [1.5].

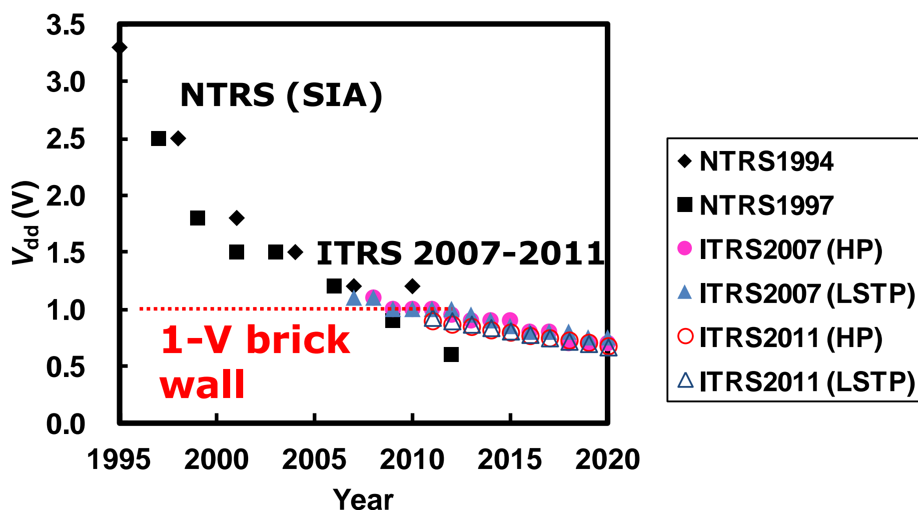


Fig. 1.2 Supply voltage V_{dd} roadmap by ITRS

The primary cause of this difficulty is widely recognized as the increase in threshold voltage (V_{th}) variation of CMOSFETs, because V_{dd} should be set higher considering the margin to the increased V_{th} variation [1.6]. Variation of transistor characteristics, primarily V_{th} variation, is increasing substantially in sub-100-nm technologies. This makes the V_{dd} reduction, required by the scaling rule, difficult, and significantly increases the power consumption of an LSI chip. Here, power consumption P of an inverter,

which is the representative unit of LSI circuit, is defined as

$$P = CV_{dd}^2 f + I_{leak} V_{dd} \quad (1.1)$$

where C, f, and I_{leak} are load capacitance, operation frequency, and leakage current, respectively. The first and second terms on the right-hand side represent operational and standby power, respectively. As the scaling proceeds, C and I_{leak} decrease due to the size reduction of transistors, and f increases for higher performance. Since the miniaturization enables the number of circuits crammed onto a single chip to increase exponentially, it is extremely important to lower V_{dd} to maintain power consumption of an LSI chip [1.7].

Figure 1.3 shows a classification of V_{th} variation. The origin of the V_{th} variation is not only due to lithographic variations and layer thicknesses, but also due to line edge roughness (LER) and random dopant fluctuation (RDF) [1.8], [1.9]. In particular, it has been pointed out that the V_{th} variation caused by the number and spacial distribution of impurities in the channel of transistors (RDF) becomes serious with the scaling as shown in Fig. 1.4 [1.10]. The magnitude of the V_{th} variation is described by standard deviation σV_{th}, since the distribution of V_{th} usually shows a normal distribution.

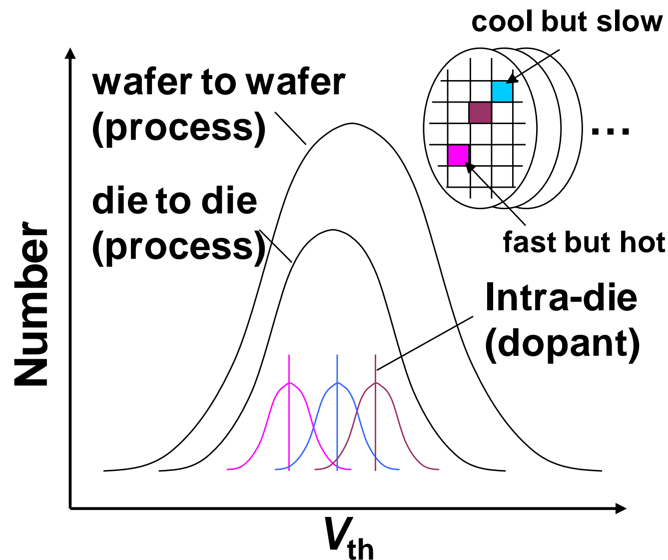


Fig. 1.3 Classification of V_{th} variation

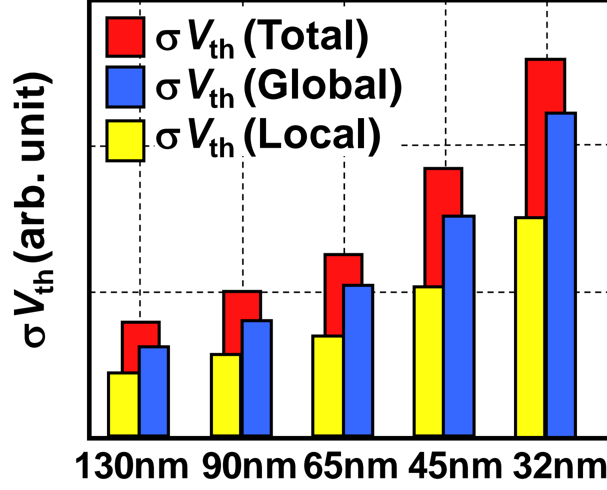


Fig. 1.4 Trend of V_{th} variation (σ V_{th}) [1.10]

The V_{th} variation becomes small with the wider area of the gate because the impurity distribution should be random. This relationship is well known [1.11] and is defined as

$$\sigma V_{th} = A_{Vt} / (L_g W_g)^{1/2} \tag{1. 2}$$

where L_g and W_g are the length and width of a gate , and the gradient A_{Vt} is called the Pelgrom coefficient. Moreover, in conventional bulk CMOSFETs, the following relationship exists

$$A_{Vt} \propto T_{ox} (N_{channel})^{1/4} \tag{1. 3}$$

where T_{ox} and $N_{channel}$ are the thickness of a gate oxide and a channel impurity density. Hence, the following relationship is drawn

$$\sigma V_{th} \propto T_{ox} (N_{channel})^{1/4} / (L_g W_g)^{1/2} \propto k^{1/4} \tag{1. 4}$$

where k is the scaling factor. Because $N_{channel}$ has increased to suppress the

short channel effect (SCE), the V_{th} variation increases with scaling inherently. Thus, it is understood that the present V_{th} variation problem is inevitably caused by the conventional bulk CMOSFETs' miniaturization.

1.3 Intrinsic-channel MOSFET

To solve these problems, it is necessary to first decrease the V_{th} variation due to size variations by suppressing SCE, and secondly to decrease RDF by lowering the impurity densities of the channel. However, intrinsic or low-dose channel devices must have some sort of countermeasure against SCE.

Fukuma proposed an intrinsic-channel MOSFET in 1988 [1.12]. The MOSFET (Fig. 1.5 left-hand side) has a thin channel and a p+ substrate under the channel through SiO_2 layer to prevent punch through. However, the device was just proposed and had no way to fabricate, for example, a very thin channel on the SiO_2 layer. A device with a 0.1-μm gate length as shown on the right-hand side in Fig. 1.5 was fabricated by using an epitaxial growth technology in 1990 [1.13]. For sub-100-nm technology node, however, a thinner epitaxial channel and dopant diffusion from the well under the channel by annealing become critical issue.

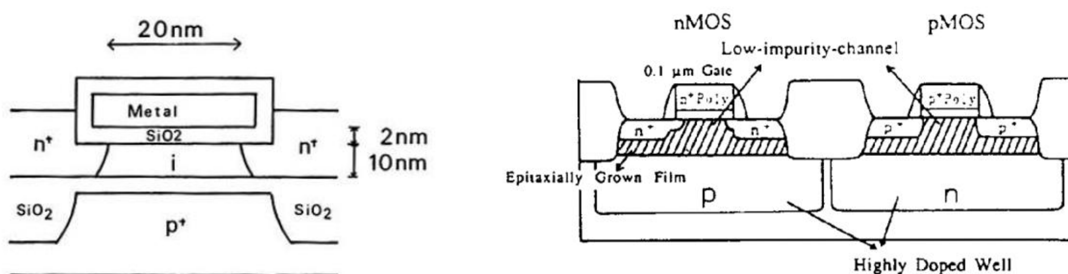


Fig. 1.5 Intrinsic-channel devices [1.12], [1.13]

Fully-depleted (FD) MOSFETs have strong immunity from SCE without increasing the impurity density of the channel because of their structures. By using commercially available silicon-on-insulator (SOI) wafers, FD-SOI

MOSFETs can be easily fabricated. Conventional SOI wafers are consisted of thick (above 100 nm) buried oxide (BOX) and SOI layers. The thickness of the SOI layer can be thinned by thermal oxidation and wet-etching. Another FD MOSFET is so called FinFET, which originally proposed as fully depleted lean-channel transistor (DELTA) by Hisamoto et al. in 1989 [1.14], as shown in Fig. 1.6. The three-dimensional gate structure is so effective against SCE. The effectiveness of these structures for V_{th} variation was reported in sub-100-nm node [1.15]. Detail comparisons with SOTB CMOSFET will be discussed in chapter 7.

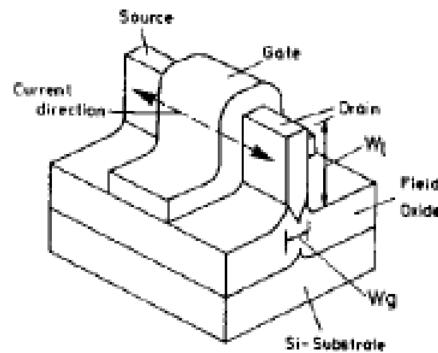


Fig. 1.6 Schematic cross section of DELTA [1.14]

On the other hand, these FD devices have some inherent issues. To continue to both improve the speed and reduce the power from the system-LSI designer's viewpoint, it is necessary to set V_{th} and V_{dd} to the best value in every circuit block or set of transistors in LSI circuits. The multiple V_{th} design, such as that with two or three kinds of V_{th} setting, is already indispensable. In conventional bulk CMOSFETs, the multiple V_{th} design can be easily obtained by adjusting the impurity density of the channel. The FD devices with intrinsic channels cannot use this way.

Additionally, a technique that controls V_{dd} adaptively according to the state of operation has also been applied [1.16]. A technique to apply substrate bias V_{bb} to control V_{th} flexibly is used in some applications, also [1.17]. This V_{bb} control technique is a strong tool that can minimize the performance deviation due to temperature fluctuation as well as the variation of each chip.

Even in present scaled bulk CMOSFETs, it is difficult to apply V_{bb} because of the increase in the junction leakage current between the source/drain (S/D) and the substrate. In FD devices, the thick BOX layer or the vertical channel structure block the V_{bb} influence.

1.4 SOTB CMOSFET

To solve the V_{th} variation problem due to RDF and satisfy the demand from circuit designers, Tsuchiya et al. proposed silicon-on-thin-BOX (SOTB) CMOSFET [1.18]. Figure 1.7 shows a schematic cross-section of the SOTB structure. Ultrathin SOI and BOX layers make the transistor highly immune from SCE, and its intrinsic channel without halo implant suppresses the V_{th} variation due to RDF. The thin BOX and impurity doping in the substrate just beneath the thin BOX enables a multiple V_{th} design. This thin BOX and the doped region also enable the wide-range back-gate controllability which realizes optimization of both performance and power after fabrication. Furthermore, conventional bulk CMOSFET can be easily co-integrated by just removing the thin SOI and BOX layers.

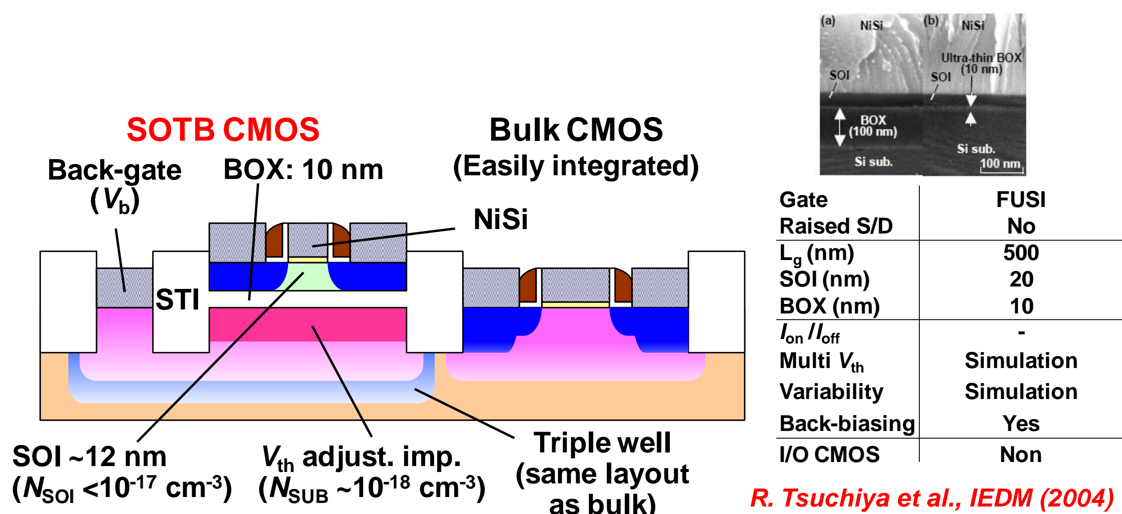
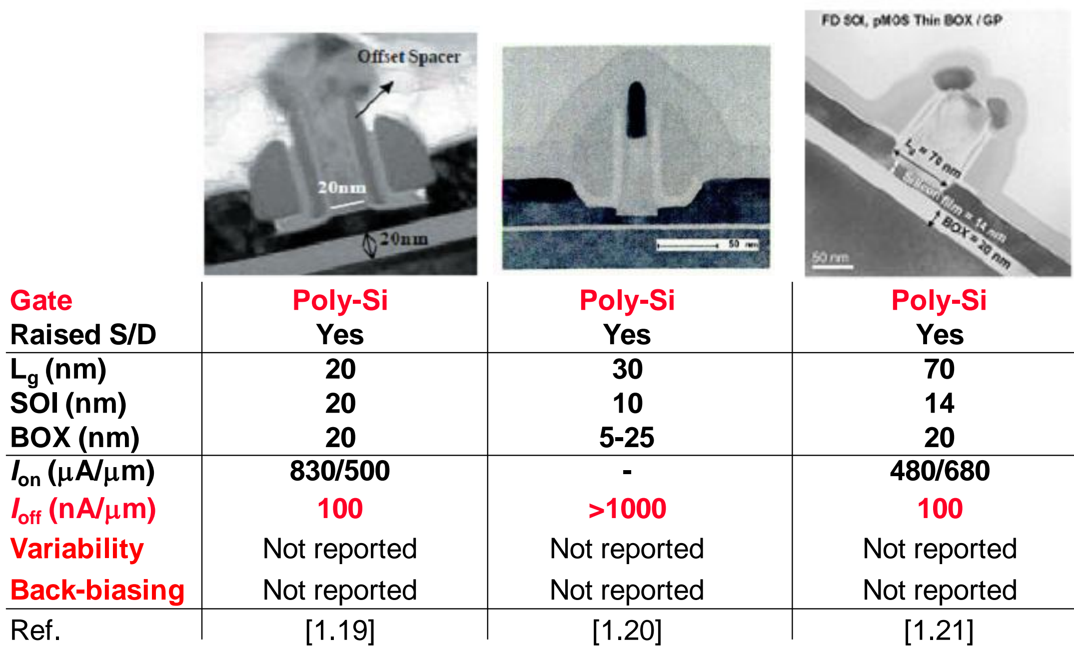


Fig. 1.7 Schematic cross-sectional view of hybrid SOTB/bulk CMOSFETs [1.18]

After Tsuchiya proposed this concept, several groups reported the results of the same structure in sub-100-nm generations [1.19]-[1.21]. Their features are summarized in Fig. 1.8. Though they all have small raised S/D structure for obtaining low external S/D resistance (R_{sd}), their off-current (I_{off}) values are too large for low-standby power (LSTP) applications due to their low V_{th} of the conventional poly-Si gates. Moreover, the special features of the SOTB structure such as low variability or back-biasing were not reported.



Gate	Poly-Si	Poly-Si	Poly-Si
Raised S/D	Yes	Yes	Yes
L_g (nm)	20	30	70
SOI (nm)	20	10	14
BOX (nm)	20	5-25	20
I_{on} (μA/μm)	830/500	-	480/680
I_{off} (nA/μm)	100	>1000	100
Variability	Not reported	Not reported	Not reported
Back-biasing	Not reported	Not reported	Not reported
Ref.	[1.19]	[1.20]	[1.21]

Fig. 1.8 Previous works as for the same structure with SOTB

1.5 Purpose of this study

Although the scaling of planar bulk MOSFET has continued so far, the end is impending. This is because the power consumption of LSIs is significantly increasing due to V_{th} variation issues as described in section 1.2. FD-SOI CMOSFETs or FinFETs are one of the most promising candidates for the issues because of their low-dose channel and high immunity from SCE.

However, they have some inherent problems, such as multi V_{th} design or back-biasing, as described in section 1.3.

The studies described in this thesis were accomplished in order to realize SOTB CMOSFET as a solution for the above stated problems, and thereby contributing to the realization of high performance and low power LSIs in the future generations. In order to sublimate SOTB from one of many candidates to the legitimate successor of the bulk planar CMOS, many problems need to be solved.

The studies of this thesis are classified roughly in two parts. Firstly, it is mentioned about the actual proof of superiority of SOTB CMOSFET to the conventional planar bulk CMOSFETs. For straight comparison with the bulk CMOSFETs, processes of SOTB CMOSFET needed to be developed in the 65-nm generation which was the latest node of those days. The characteristics of SOTB CMOSFET also needed to be examined in comparison with the ones of bulk CMOSFETs.

Another issue is solving the subjects for utilization. In order to put SOTB in practical use, it is very important that there is no inferior point to the conventional bulk CMOSFETs. However, there are following three subjects for the utilization of SOTB. The first subject is an integration of the transistor for high-voltage operation. In recent system on a chip (SoC), many functions are required to the one chip and the transistors for input/output (I/O) or analog applications are usually integrated with core transistors. The second subject is reliability issues such as hot carrier injection (HCI) and negative bias temperature instability (NBTI). The reliability of the conventional FD-SOI CMOSFETs in the advanced technology node has not been fully studied. In addition, the wide-range back-biasing of SOTB CMOSFET will be expected to influence the reliability. Lastly, the third subject is the ease of manufacturing. Though a fully-silicided (FUSI) gate process applied in SOTB fabrication for LSTP requirements is easy and simple, but the precise control of the manufacture variation is to be expected difficult especially for large scale integration. In the late 2000s, the mainstream of the gate structure to be studied had moved to the metal-inserted poly-Si (MIPS) gate structure. It is necessary to optimize the gate stack in order to applying for SOTB CMOSFET. These subjects described above are summarized in Table 1.2.

Table 1.2 Subjects studied in this thesis

Subjects	Targets	Approaches
Realizing SOTB CMOSFET in 65-nm generation	・L_g = 50 nm ・Desirable and multi V_{th} for LSTP ・Comparable I_{on}/I_{off} ・Less V_{th} variation ・Characterization of back-biasing	・Combine FUSI gate and high raised S/D ・Adjust the dopant concentration of the substrate beneath the BOX ・Suppress SCE and RDF by FD-SOI structure with low-dose channel ・Propose a way of back-biasing
Reduction of power consumption	・Ultralow off-current ・Comparable inverter delay ・Reduction of standby power ・Reduction of V_{dd} in SRAM	・GIDL reduction by controlling L_{ov} ・Boosted performance in the case of ultralow I_{off} ・Ultralow I_{off} and low variability
CMOSFETs for I/O operation	・Comparable characteristics to conventional bulk I/O CMOSFETs	・Hybrid integration ・Investigate the quality of the exposed surface
HCI and NBTI reliability	・Comparable lifetime to conventional bulk CMOSFETs ・Clarify the mechanism	・Analsis of the electric fields in SOTB by using 2D simulator ・Investigate the influence of back-biasing
MIPS gate for SOTB	・Desirable V_{th} for LSTP ・Non-degraded narrow channel characteristics	・SiON/TiN/poly-Si gate ・Less silicidation process

Figure 1.9 shows the configuration of this thesis. Chapter 2 covers the studies undertaken to develop the SOTB CMOSFET in 65-nm generation and examine the characteristics. The studies of reduction of the power consumption by using SOTB technology are covered in chapter 3. Chapter 4 covers the hybrid integration of SOTB and bulk CMOSFETs. Chapter 5 covers the analysis of HCI and NBTI of SOTB CMOSFET. Chapter 6 covers the studies of MIPS gate stacks for SOTB CMOSFET. The studies referred to in each chapter were done in order to achieve SOTB CMOSFET with high performance, low power consumption, and high reliability for future generation. Details are as follows.

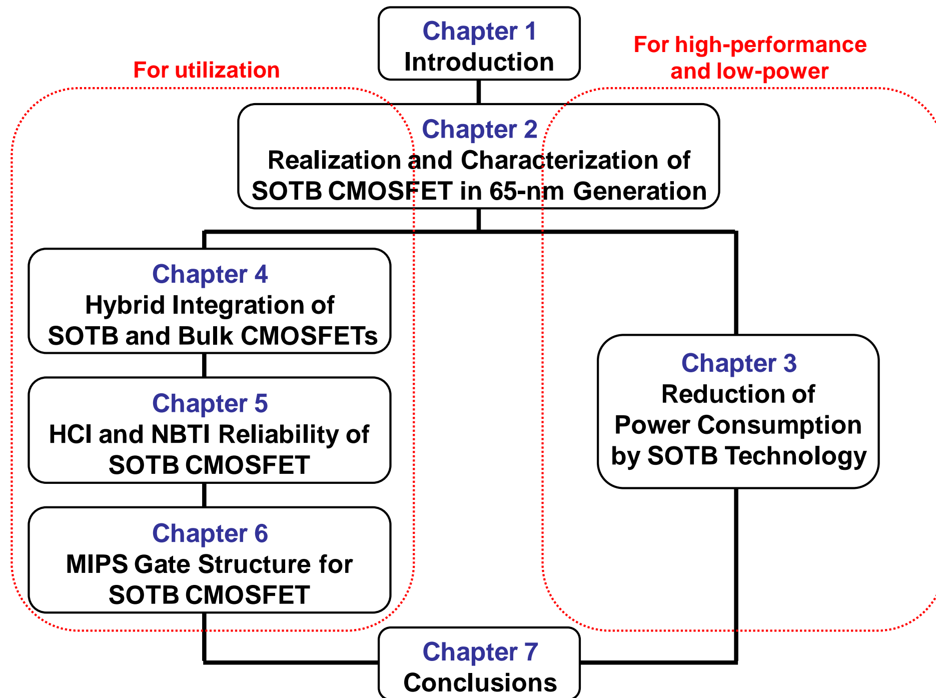


Fig. 1.9 Configuration of this thesis

a) Realization and characterization of SOTB CMOSFET in 65-nm generation (Chapter 2)

In FD-SOI devices for 65-nm generation, an ultrathin SOI layer below 15-nm is required to suppress SCE. The thin SOI layer makes increase in parasitic S/D resistance R_{sd}. A raised S/D structure by selective epitaxial growth (SEG) has been adopted for obtaining low R_{sd}. The structure needs to be optimized for SOTB CMOSFET. Another main issue for FD-SOI devices is to control the V_{th} value. The intrinsic channels of the FD-SOI devices require suitable metal gate technology. However, it usually increases process complexity.

Though some results of the SOTB structure in sub-100-nm generation had been shown from other groups, important concerns about this structure such as the V_{th} control including multi V_{th} design, variability, and back-biasing had not been reported. In chapter 2, a novel process to realize SOTB CMOSFET for LSTP specifications is presented with solving the many

trade-offs. The simple process makes a FUSI gate for desirable V_{th} and relatively thick raised S/D for low R_{sd} simultaneously. The superior characteristics of the fabricated SOTB CMOSFET to conventional bulk CMOSFETs in the same generation are shown. In addition, the special features such as low V_{th} variation and wide-range back-biasing are demonstrated for the first time.

b) Reduction of power consumption by using SOTB technology (Chapter 3)

It was very difficult to decrease V_{dd} in those days due to the increasing V_{th} variation. And it has been continuing until now. Unless V_{dd} is reduced with scaling, the power consumption of the LSI will significantly increase due to an increase in both operational and standby leakage power. Though FD-SOI devices were expected to be able to help the problem, there were few reports about the variability and power reduction at that time.

In chapter 3, studies of reduction of the power consumption by using SOTB technology are discussed. It is shown that how the low V_{th} variation of the SOTB CMOSFET impacts on the reduction of the supply voltage. An ultralow off-current (1 pA/μm) SOTB CMOSFET was developed for reducing the standby power. It is demonstrated that the wide-range back-biasing is effective for the high performance in the case of the ultralow off-current devices. It is also presented that how much the standby power of the 6T-SRAM, as a representative unit in LSI circuits, can be reduced by SOTB technology.

c) Hybrid integration of SOTB and bulk CMOSFETs (Chapter 4)

One of inherent problem of FD-SOI devices is its low breakdown voltage. In conventional SoC, however, high-voltage transistors are usually integrated for I/O operation. A simple answer to this issue in FD-SOI devices is to integrate bulk transistors with the FD-SOI platform. A previous approach was such that the thick BOX layer was removed by dry-etching and a Si layer by SEG was used to compensate the height difference [1.22].

In chapter 4, novel hybrid integration is presented. The height difference between the core and I/O regions is kept small due to the ultrathin SOI and

BOX layers of SOTB CMOSFET. Therefore, the devices for core and I/O operations can be fabricated simultaneously. The characteristics of the I/O devices are shown to be comparable to conventional I/O devices. In addition, the reliability of the exposed surface of the Si substrate is thoroughly investigated.

d) HCI and NBTI reliability of SOTB CMOSFET (Chapter 5)

The reliability of FD-SOI CMOSFETs in sub-100-nm generations has not been fully investigated. For SOTB CMOSFET, moreover, its wide-range back-biasing is expected to have much influence the reliability because the back-biasing modulates the electric fields and carriers in the device.

In chapter 5, the HCI and NBTI reliability of SOTB CMOSFET is examined for the first time. The characteristics are analyzed in comparison with conventional bulk CMOSFETs. The difference of electric fields between SOTB and conventional bulk CMOSFETs are also analyzed by using 2D device simulator. In addition, the mechanisms including the effects of back-biasing are discussed in detail.

e) MIPS gate structure for SOTB CMOSFET (Chapter 6)

There is a concern regarding the mass production of SOTB with FUSI gate because the phase and the thickness of NiSi are hard to be controlled precisely. On the other hand, MIPS gate structures were widely studied in combination with high-κ gate dielectrics in the late 2000s. For LSTP applications of 65-nm generation, however, the high-κ gate dielectric is not required intensely because the EOT is around 2 nm.

In chapter 6, a reliable MIPS gate structure using conventional SiON gate dielectric for SOTB CMOSFET is presented. It was found that the characteristics of the FUSI gate SOTB CMOSFET degraded in the narrow channel due to the excess silicidation. The configuration of the MIPS gate stack is studied to obtain the desirable V_{th} with considering the processes of SOTB CMOSFET. It is also shown that the superior narrow channel characteristics of the MIPS gate SOTB CMOSFET.

Finally, the results obtained in these studies are summarized and conclusions are presented in chapter 7. In addition, the importance of SOTB CMOSFET for future LSIs is discussed with comparing the other technology such as FinFETs.

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Chapter. 2 Realization and Characterization of SOTB CMOSFET in 65-nm generation

Abstract

SOTB CMOSFET for the target specification of 65-nm LSTP was firstly realized. A simple simultaneous silicide process for FUSI gate with relatively thick raised S/D was developed. This makes the gate fully silicided and prevents the excess silicidation in the S/D region at the same time. The characteristics such as the desirable multi V_{th}, SCE, and I_{on}/I_{off} were studied. And they are shown to be superior in comparison with conventional bulk CMOSFETs. It was also demonstrated for the first time that the wide-range back-biasing of SOTB CMOSFET could optimize device performance and reduce in V_{th} variation after device fabrication.

Chapter.2 Realization and Characterization of SOTB CMOSFET in 65-nm generation

Contents

2.1 Introduction
2.2 Fabrication of SOTB CMOSFET
2.3 DC characteristics of SOTB CMOSFET for 1.2-V operation
2.4 Wide-range back-biasing of SOTB CMOSFET
2.5 Conclusion
2.6 References

2.1 Introduction

FD-SOI devices have excellent characteristics, such as high SCE immunity, low subthreshold swing (SS), small junction capacitance and small floating body effect compared to bulk or partially-depleted (PD) SOI devices [2.1]. On the other hand, the threshold voltage needs to be controlled by the work function of the gate material. In addition, for sub-100-nm generations, parasitic source/drain (S/D) resistances (R_{sd}) become a serious problem because of the ultrathin SOI layer, which is usually less than 25 nm.

After Tsuchiya proposed the concept of SOTB structure [2.2], several groups reported the results of the same structure in sub-100-nm generations [2.3]-[2.5]. They adopted thin SOI layer for SCE and raised S/D structure for low R_{sd}. However, their V_{th} values are too low for LSTP applications in their conventional poly-Si gates because there are few depletion layer charges in FD-SOI devices with low-dose channels. Metal gates with work function close to midgap, such as nickel silicide (NiSi), are suitable for the desirable V_{th} values in FD-SOI devices [2.6]. However, a previous approach, in which the S/D and the gate are silicided separately by using a chemical mechanical polishing (CMP) technology, increases process complexity significantly [2.7].

In this chapter, a simple FUSI gate process without CMP for fabricating SOTB CMOSFET in 65-nm generation is presented. In this process, the gate and the raised S/D are silicided simultaneously by adjusting the heights of the gate and the raised S/D. The characteristics (SCE, V_{th}, I_{on}/I_{off}, and variability) of the fabricated SOTB CMOSFET are thoroughly investigated for the target specification. Moreover, the special feature of SOTB technology, that is, wide-range back-biasing, is demonstrated for the first time.

2.2 Fabrication of SOTB CMOSFET

There are three key processes of fabricating SOTB devices. Firstly, one drawback of FD-SOI structure is the high parasitic series resistance of thin SOI layer. Elevated source/drain structure by using selective epitaxial growth (SEG) was adopted to reduce the parasitic resistance. Secondly, conventional poly- Si gate devices with lightly doped channel cannot be used

for LSTP applications, since their standby current is too large due to their low V_{th}. In FD-SOI devices, one can obtain the desirable V_{th} value for LSTP by using a single midgap metal both for NMOS and PMOS. In this chapter, NiSi was adopted as a gate metal. A metal-inserted poly-Si (MIPS) gate structure can also be adopted, which described in chapter 6. Moreover, a hybrid process in which bulk I/O devices are integrated with SOTB devices is indispensable for SoC architecture. It is described in chapter 4.

Figure 2.1 shows the process steps of a SOTB CMOSFET in 65-nm generation. Firstly, commercially available SOI wafers with ultrathin BOX (T_{BOX} = 10 nm) [2.8] were thinned by sacrificial oxidation so that the thickness of the SOI layer reduced to 13 nm. By using the similar process steps as the conventional bulk CMOSFETs, shallow trench isolation (STI) formation and well implantation were done. For multi V_{th} design, the substrate beneath the BOX layer was implanted while keeping the dopant of the channel low. A halo implantation is not necessary to prevent SCE in FD-SOI devices. In the gate oxidation process, SiON gate dielectrics were formed at an equivalent oxide thickness (EOT) of 1.9 nm for SOTB core CMOSFETs.

The gate stack was constituted with a thin poly-Si layer (40 nm) and a cap SiO_2 layer (consisted by tetraethyl orthosilicate tetraethoxysilane (TEOS)). After etching the gate stack, a thin high temperature oxide (HTO) and a SiN layers were deposited. When the SiN layer was etch-backed, the HTO layer was used as a stopper to protect the thin SOI layer from the etching damage. The formed SiN offset spacer was used to control overlap length between the gate and extensions (L_{ov}) precisely in the S/D extension implantation. After forming a sidewall, an elevated S/D structure was formed by SEG to obtain low R_{sd}. To prevent decrease in the SOI thickness in the S/D region, the conditions for etchings and pre-cleaning before the SEG were carefully optimized. It was also noted that the SiO_2 layer as a gate- capping was required to protect the poly-Si layer. Unless the poly-Si layer was exposed, an excessive Si layer over the gate was formed in the SEG. The height of the S/D was set to be higher than the gate poly-Si layer for the simultaneous FUSI. After an ion implantation for S/D region, a FUSI process was done as described below.

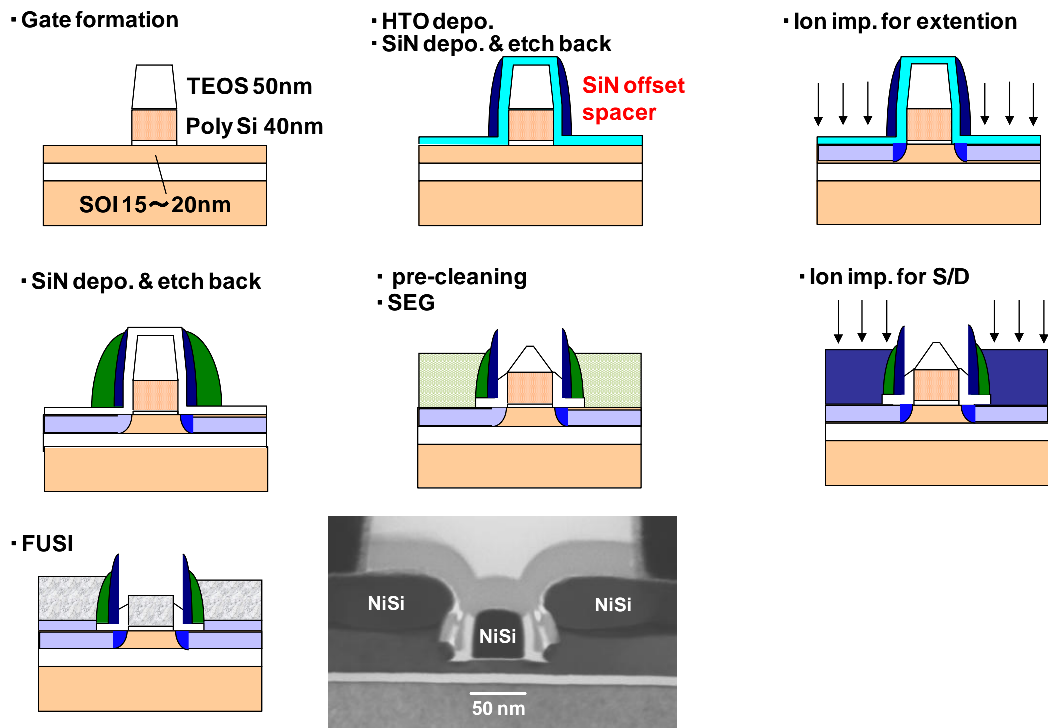

Fig. 2.1 Process steps of a FUSI-gate SOTB CMOSFET

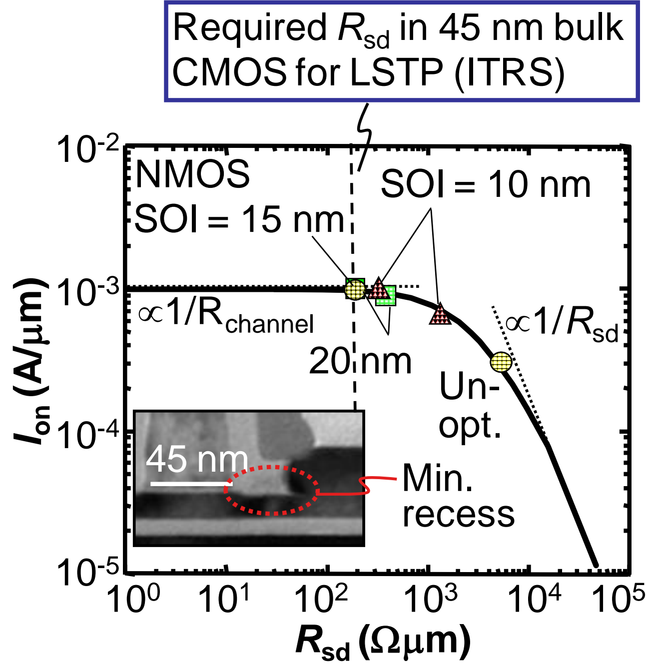

Fig. 2.2 Relationship between on-current I_{on} and external resistance R_{sd}

Figure 2.2 shows extracted R_{sd} values in several process conditions. The enough low R_{sd} below 200 Ω/μm was obtained in the optimum condition, resulting in no degradation of the I_{on} value. In the case of un-optimized condition such as excess recess in the SOI layer, the I_{on} value degraded in proportion to the high R_{sd}.

In low-power FD-SOIs with intrinsic channels, no dual metal technology between NMOS and PMOS gates, such as NiSi phase control [2.9], is required when using nickel silicide as a gate electrode material. Here, the gate needs to be fully silicided on one side. On another side, however, the S/D region must not be fully silicided. If the SOI layer under the NiSi were fully silicided, the R_{sd} increases due to the small contact area between Si and NiSi [2.10]. Therefore, the gate poly-Si and the S/D epitaxial Si were set to their optimal heights before gate-cap removal and fully silicided simultaneously in a single step without using CMP. A deposited Ni thickness was carefully designed. To precise control the thickness of the formed NiSi layer, 2-step annealing was adopted. The first annealing was to control the thickness of

the NiSi layer, and the second annealing after removing the remained Ni layer was to control the phase of the NiSi layer.

Figure 2.3 shows a cross-sectional TEM image of a fabricated 50-nm-gate-length SOTB MOSFET. Energy-dispersive X-ray spectroscopy (EDS) indicated that the NiSi atomic ratio for both the gate and the source/drain was 1:1.

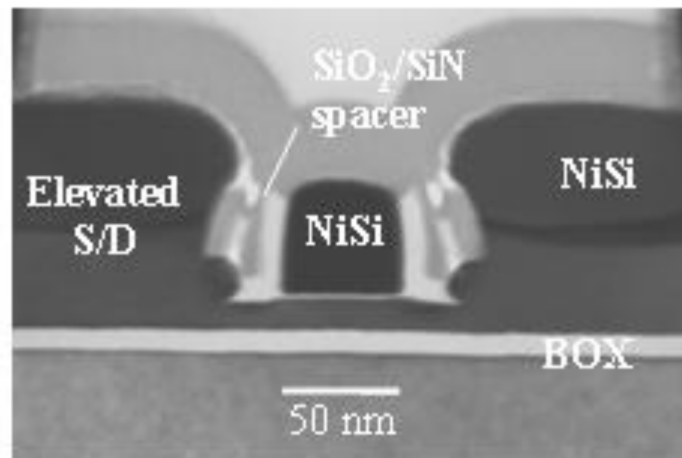

Fig. 2.3 A cross-sectional TEM image of 50-nm-gate-length SOTB MOSFET

Regarding the isolation between transistors and back-gate contacts, this SOTB technology uses a conventional STI process similar to the bulk technology. The slight change is that the trench is formed by dry etching three layers: the SOI, BOX, and substrate. Consequently, the isolation between devices on the SOI and back-gate contacts is ensured by STI. The well region, acting as a back gate and ground plane, was formed beneath the BOX layer and connected to the region of the back-gate contact through the area underneath the STI. The back-gates for NMOS and PMOS are also isolated by STI. This back-gate contact structure in SOTB technology can be fabricated with the same mask layout as the conventional bulk CMOSFET. A triple-well structure is also adopted to prevent leakage for back-gate biasing.

The typical subthreshold characteristics of the 50-nm-gate-length SOTB CMOSFETs at V_{dd} = 1.2 V are plotted in Fig. 2.4. The desired symmetrical characteristics were successfully obtained with a single Ni FUSI gate. Figures 2.5 and 2.6 show the roll-off characteristics of SOTB NMOSFET and PMOSFET, respectively. They have suppressed SCE even in low-dose channel without halo implant, resulting in *SS* less than 90 mV/decade and drain induced barrier lowering (DIBL) less than 120 mV/V. They also show that multi V_{th} values are successfully achieved for LSTP specifications by selecting the dopant of the substrates of 1x10^{18} or 1x10^{16} cm^{-3}, respectively.

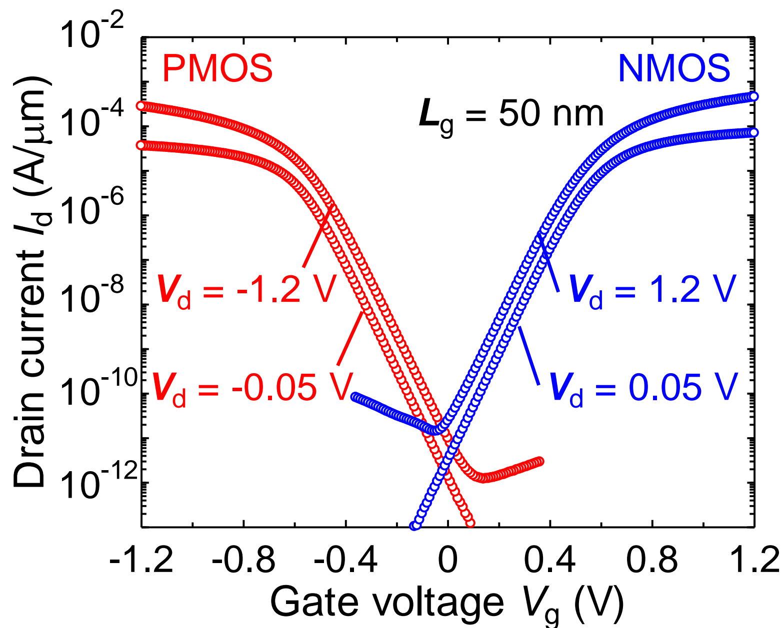

Fig. 2.4 Typical I_d- V_g characteristics of 50-nm-gate-length SOTB CMOSFET

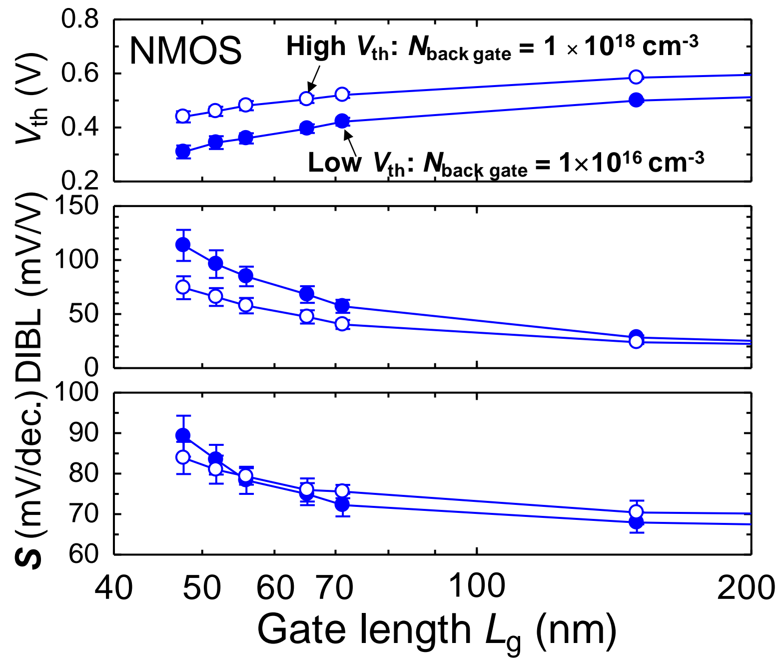

Fig. 2.5　Roll-off characteristics of SOTB NMOSFET

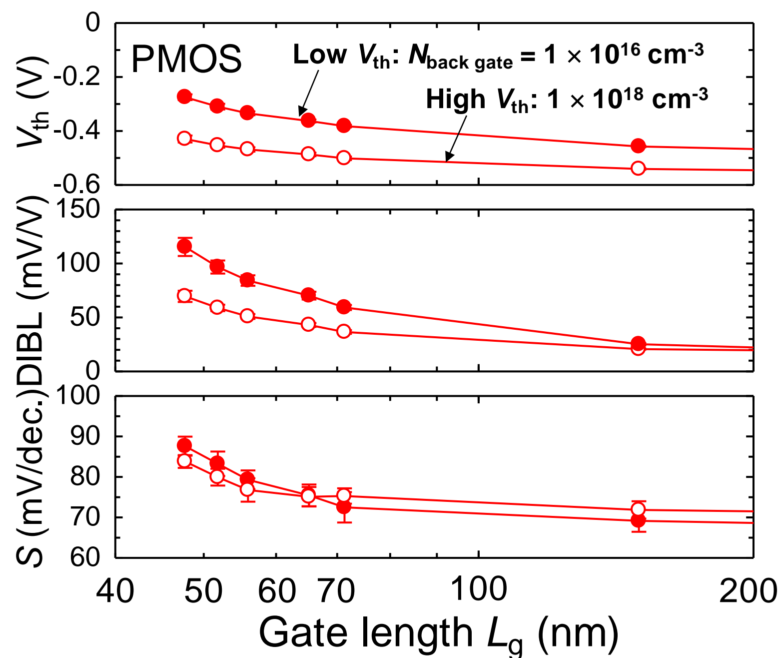

Fig. 2.6　Roll-off characteristics of SOTB PMOSFET

Figure 2.7 shows the output characteristics of SOTB CMOSFET. It is proven that the SOTB CMOSFET is free from the self-heating effect thanks to the ultrathin BOX. That is, negative drain conductance (decreasing I_d with increasing V_d) was not observed. The off-state drain currents were less than 20 pA/μm due to the reduction of gate induced drain leakage (GIDL) with properly controlled L_{ov}. At the same time, the on-currents of 550 and 320 μA/μm for NMOS and PMOS are obtained. This is because FUSI suppresses gate depletion resulting in a 0.4 nm improvement, as evaluated by C-V measurement. Additionally, it is possible that the volume expansion of FUSI gate causes compressive strain to the channel, which modulates carrier mobilities. These I_{on}/I_{off} values are in good agreement with the data based on bulk or FD-SOI technology for LSTP applications [2.11]-[2.13] as shown in Fig. 2.8. The above characteristics for the target specifications are summarized in Table 2.1.

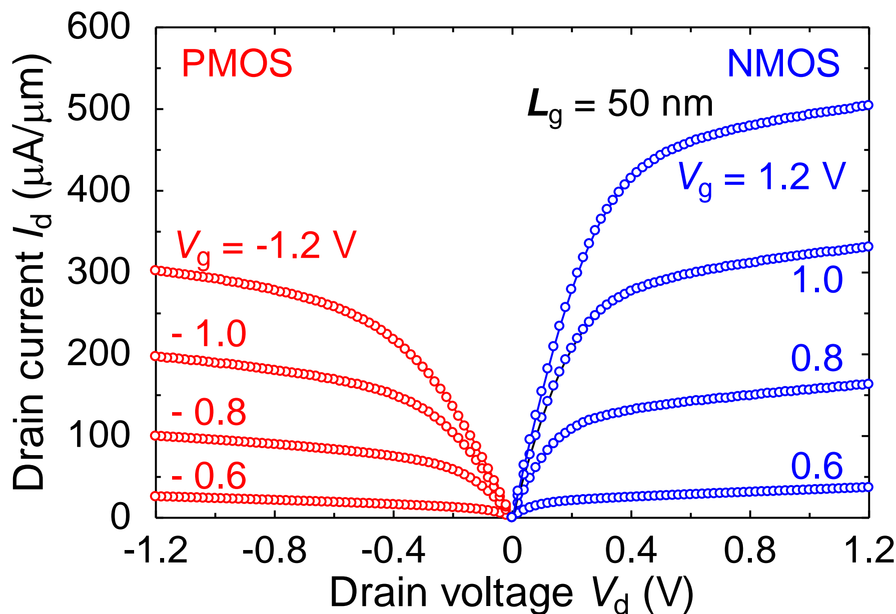

Fig. 2.7 I_d-V_d characteristics of 50-nm-gate-length SOTB CMOSFET. No self-heating is evident due to the thin BOX

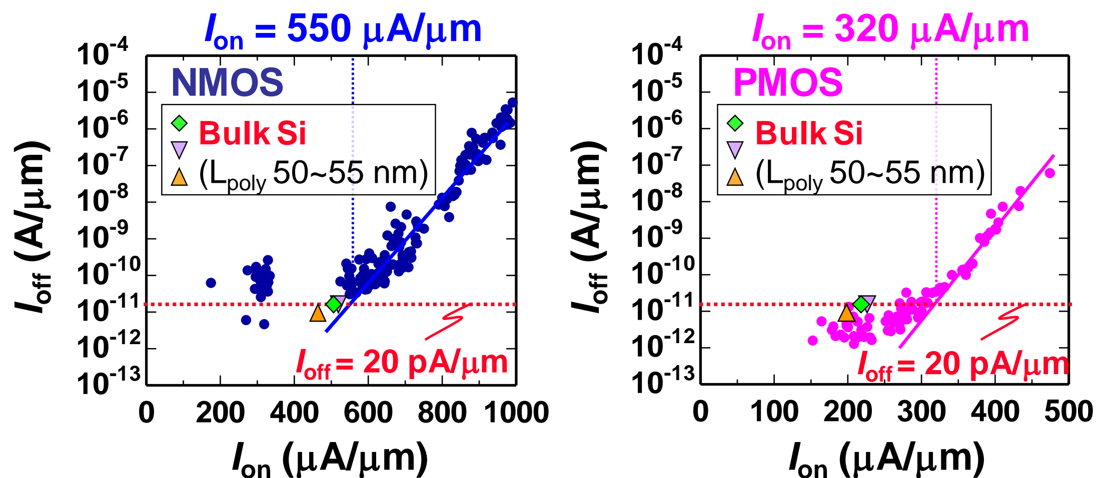

Fig. 2.8 I_{on}-I_{off} characteristics of 50-nm-gate-length SOTB CMOSFET in comparison with planar bulk CMOSFETs

Table 2.1 Comparison of the characteristics in 65-nm generation

	[2.14]	[2.15]	Target	Results
Device	bulk	bulk	-	SOTB
V_{dd} (V)	1.2	1.2	1.2	1.2
L_g (nm)	55	50	50	50
EOT (nm)	1.95	2.45 (CET)	1.9	1.9
Gate dielectric	SiON	HfSiON	SiON	SiON
V_{th} (V)	0.3	0.3-0.5	Multi V_{th}	0.35 (LVT) 0.45 (HVT)
I_{on} (NMOS) (μA/μm)	445	510	500	550
I_{on} (PMOS) (μA/μm)	190	220	300	320
I_{off} (NMOS) (pA/μm)	10	20	20	20
I_{off} (PMOS) (pA/μm)	10	20	20	20
Avt (NMOS)	3~4 (estimated as conv. bulk)		<2	1.8
Avt (PMOS)			<2	1.5

2.4 Wide-range back-biasing of SOTB CMOSFET

In the typical transistor design of SOTB, the V_{th} without applying back-biasing can be controlled by changing the dopant concentration of the substrate beneath the thin BOX. While, time-to-time or area-to-area (including die-to-die or wafer-to-wafer) device characteristics can be widely controlled using the back-gate bias V_{bb}. In particular, forward back-gate bias can be effectively used because there is no substrate leakage. Note that a forward bias higher than 0.6 V can never be applied in conventional bulk CMOSFETs owing to the significant increase in p-n junction leakage current from source to substrate. The dependences of V_{th} and the *SS* of a 50-nm-gate-length SOTB CMOSFET on V_{bb} at V_{dd} = 1.2 V are shown in Fig. 2.9. By applying a reverse V_{bb}, V_{th} increased to above 0.6 V, and the *SS* decreased to less than 80 mV/decade. In contrast, by applying a forward back-gate bias of 1.2 V, V_{th} can be lowered by more than 0.3 V while keeping the *SS* small. In such a high forward bias, there is no increase in the substrate leakage currents.

The back-gate bias dependences of the on- and off- currents of the SOTB CMOSFET are shown in Fig. 2.10. By applying a reverse back-gate bias of |1.2 V|, I_{off} can be reduced to less than 1/100 in PMOSFET. However, in NMOSFET, I_{off} cannot be decreased so much due to the large GIDL current. It will be considered extensively in chapter 3. On the other hand, the on-current of the SOTB CMOSFET can be increased by 30% for NMOS and by 44% for PMOS by applying a forward bias of |1.2 V|. This wide-range back-biasing can enable high-performance and low-power LSIs so that the forward biasing is used when faster speed is required, and the reverse biasing is used at the standby mode.

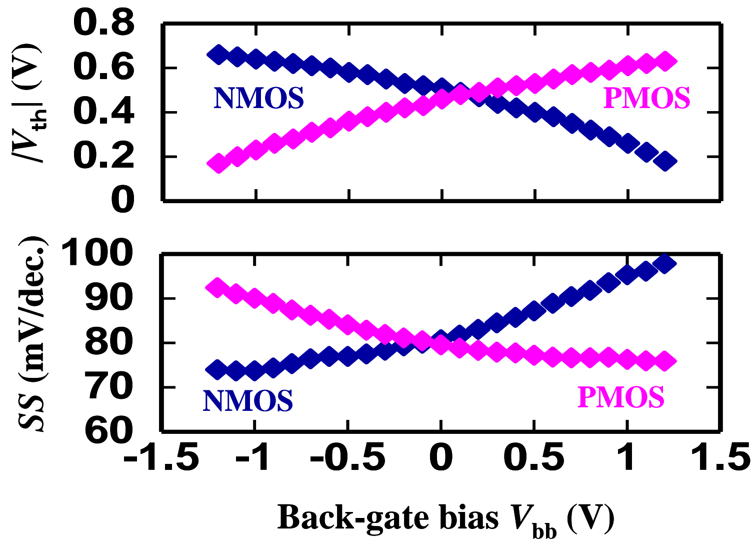

Fig. 2.9 Dependences of V_{th} and SS for a 50-nm-gate-length SOTB CMOSFET as a function of back-gate bias V_{bb} at V_{dd} = 1.2 V

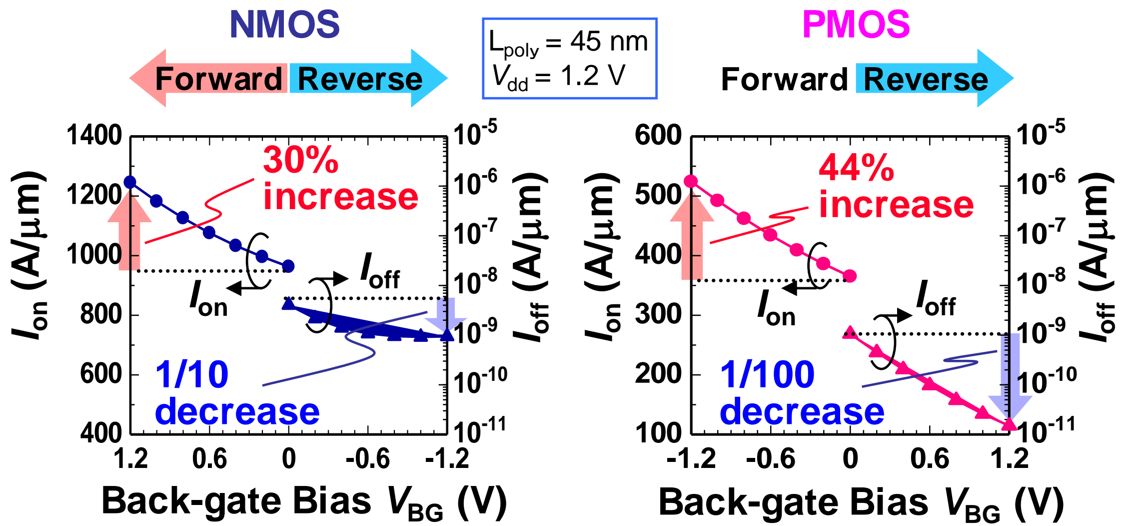

Fig. 2.10 Dependences of V_{th} and SS for a 50-nm-gate-length SOTB CMOSFET as a function of back-gate bias V_{bb} at V_{dd} = 1.2 V

As for conventional bulk structures, reverse biasing can be used to reduce the standby leakage after fabrication. However, this is less effective because both V_{th} variation and GIDL increases [2.15]. In the SOTB case, GIDL is sufficiently suppressed by the intrinsic channel and the controlled L_{ov}, and forward V_{bb} is also effective in adjusting the V_{th} variation. The die-to-die compensation for the V_{th} of each chip is demonstrated in Fig. 2.11. Each circle represents a 50-nm-gate-length NMOS of a chip. The open circles indicate the V_{th} distribution without V_{bb} control, and the closed circles indicate the distribution with V_{bb} control, that is, when the V_{bb} was adjusted for each transistor to approach the target V_{th}. The V_{bb} values range from -1.2 to 1.2 V, in 0.2-V increments. Without V_{bb} control, the range of V_{th} distributions is about 0.1 V due to size (gate length or layer thicknesses such as SOI) variations or channel dose fluctuations. The standard deviation σV_{th} with V_{bb} control was suppressed to 1/4 (case A) even with such a wide V_{bb} step. In addition, the typical V_{th} can be set arbitrarily within a range of 0.18 V (cases B and C), which is larger than the 0.1 V of the original V_{th} distribution, while keeping the variation suppressed. It is assumed, for instance, that setting the optimum V_{bb} according to the speed and the power of the chip will improve the yield.

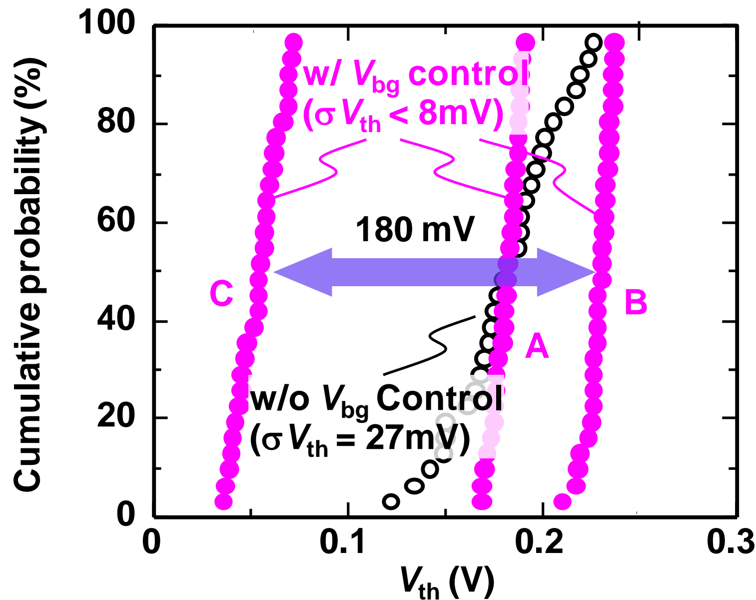

Fig. 2.11 V_{th} shift and variation reduction of poly-Si gate SOTB NMOS

using back-gate bias V_{bb} (V_{bb}: -1.2 < V_{bb} < 1.2 V, increments = 0.2 V)

2.5 Conclusion

A simple fabrication process of FUSI NiSi gate has been developed to fulfill the both requirements of full silicidation of the gate electrode and low parasitic resistance of raised S/D structure for fabricating 65-nm node SOTB CMOSFET. The optimal V_{th} for LSTP application in FUSI gate SOTB MOSFETs was obtained with a low doped channel. Multi V_{th} capability was also shown. The characteristics of SOTB CMOSFET were superior to that of the conventional bulk CMOSFETs even in 65-nm generation.

Back-gate bias control can optimize the power and performance of LSI chips after fabrication. It was shown that SOTB has a wide-range V_{th} controllability using back-gate bias, even with a gate length of around 50 nm. An effective use of the back-biasing to decrease chip-to-chip V_{th} variation was also firstly demonstrated. These results indicate that the SOTB technology can enhance the overall circuit performance and extend device scaling.

2.6 References

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Chapter. 3 Reduction of Power Consumption by Using SOTB Technology

Abstract

Ultralow off-current (I_{off} < 1 pA/μm) SOTB CMOSFET was developed in 65-nm generation. The off-current of SOTB CMOSFETs was studied and gate-induced drain leakage (GIDL) was adequately reduced by controlling the gate-overlap length. Boosted performance by using back-gate biasing in the case of the ultralow off-current SOTB was also demonstrated. And the faster inverter delay than conventional LSTP bulk CMOSFETs was shown. In addition, it was estimated how the standby leakage of a 1-M bit SRAM could be reduced by using the SOTB technology. The threshold voltage standard deviation (σV_{th}) of SOTB was shown to be half in comparison with the ones of conventional bulk devices. If the σV_{th} becomes half, the integrated standby leakage of a large number of transistors becomes half. The ultralow off-current with a small variation also further reduces the standby leakage.

Chapter.3 Reduction of Power Consumption by Using SOTB Technology

Contents

3.1 Introduction
3.2 Device design for GIDL reduction
3.3 Ultralow off-current
3.4 Boosted performance by using back-gate biasing
3.5 Variability of SOTB CMOSFET
3.6 Reduction of power consumption
3.7 Conclusion
3.8 References

3.1 Introduction

Increasing power consumption is a serious problem in the scaled CMOS technology. There are two major causes for this. One is the growing difficulty in decreasing the supply voltage as described in chapter 1. Un-scalable supply voltage increases the dynamic power. The other is increasing off-leakage current. It was shown that the leakage power has been rapidly increasing and has reached or exceeded the level comparable to the dynamic power at the sub 65-nm generations [3.1]. The major cause of the increase in both dynamic and standby power is widely recognized to be increasing V_{th} variation. Especially, because the random dopant fluctuation (RDF)-related variation has a random and local nature, it seriously degrades the stability of circuits, especially in static random access memory (SRAM).

In this chapter, it is studied what extent the small V_{th} variability of SOTB technology can reduce the power consumption. Firstly, the off-state leakage current (I_{off}) of SOTB CMOSFET is investigated. The I_{off} of the current extremely scaled CMOSFETs is mainly determined by a) the subthreshold leakage current, b) gate-induced drain leakage (GIDL) current, c) junction leakage current, and d) gate leakage current [3.2], [3.3]. As scaling continues, these leakage currents increase exponentially, and cannot be reduced without sacrificing driving performance. In SOTB CMOSFET, it was found that the GIDL current was major element of the I_{off}. By reducing the GIDL current, the ultralow I_{off} (< 1 pA/μm) in 50-nm-gate-length SOTB CMOSFETs was achieved. The suppressed I_{off} variation is also shown. It is demonstrated that the performance could be boosted and the variation could be further suppressed by using back-gate biasing. Due to the ultralow I_{off} and suppression of its variation, the impact on the reduction of the standby current of a large number of transistors was estimated. It is also shown that the low variability of SOTB technology could reduce the supply voltage in SRAM operation.

3.2 Device design for GIDL reduction

For LSTP applications, a single mid-gap metal gate with an intrinsic

channel is easily introduced in the fabrication process and is suitable for the desired V_{th}. However, unless the GIDL current is suppressed to less than the subthreshold leakage, I_{off} cannot be reduced at the desired V_{th}. GIDL increases when gate bias V_g becomes negative (for NMOS, vice versa for PMOS). This is because of band-to-band tunneling in and around the drain junction below the gate edges. This leakage current is a source-to-drain current in SOI structures because of the BOX layer, unlike the bulk transistor in which the GIDL current flows to the substrate. In the SOTB structures, the intrinsic channel is also effective to suppress GIDL because of low electric field around the drain junction below the gate edges. Note that in an SOTB device, it is unnecessary to consider either the junction depth (because it is controlled only by SOI thickness) or the channel-impurity profile (because the SOTB device has an intrinsic channel without halo implant). Therefore, the control of GIDL in an SOTB is simple. Only the gate overlap length L_{ov}, which is defined as the length of the overlapped region between gate and source/drain (S/D) extensions, needs to be controlled.

Figure 3.1 plots the calculated GIDL with various L_{ov} values by using the 2D device simulator (ATLAS) [3.4]. The parameters used in this calculation are as follows: L_g, SOI thickness, BOX thickness, gate oxide thickness, and supply voltage are 65, 15, 10, 2 nm, and 1.2 V, respectively. The inset shows the potential distribution with L_{ov} of 10 nm when V_g is -0.5 V and V_{dd} is 1.2 V. It is shown that the potential on the drain edge is steep due to the bias difference between the gate and drain. When L_{ov} is 10 nm, I_{off} (at V_g = 0 V) increases because of the subthreshold leakage and the GIDL since the large overlap enhances both the SCE and the GIDL. Figure 3.2 shows the simulated relationship between the GIDL and I_{on}. The GIDL is defined as the drain current at V_g = -0.5 V. By decreasing L_{ov} to less than a few nm, GIDL can be reduced sufficiently. At the same time, however, I_{on} also decreases. Therefore, this indicates that L_{ov} should be carefully optimized for a target specification.

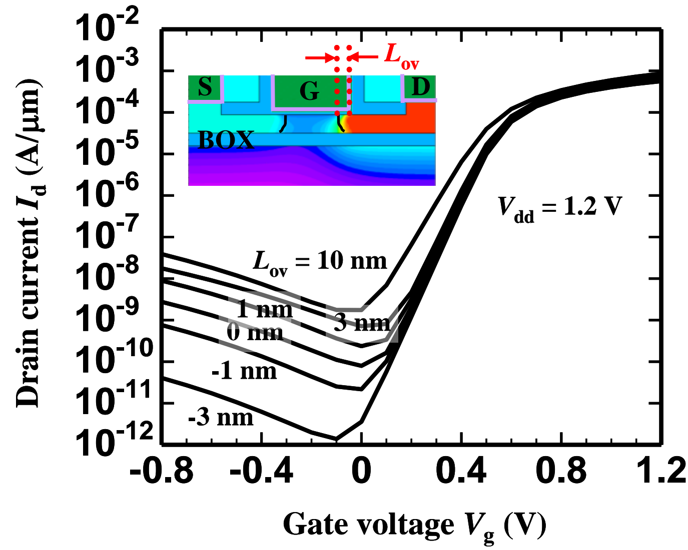


Fig. 3.1 Simulated NMOS $I_d - V_g$ characteristics as a function of gate overlap length L_{ov} at V_{dd} = 1.2 V. The inset shows the potential distribution in SOTB structure at V_g = -0.5 V.

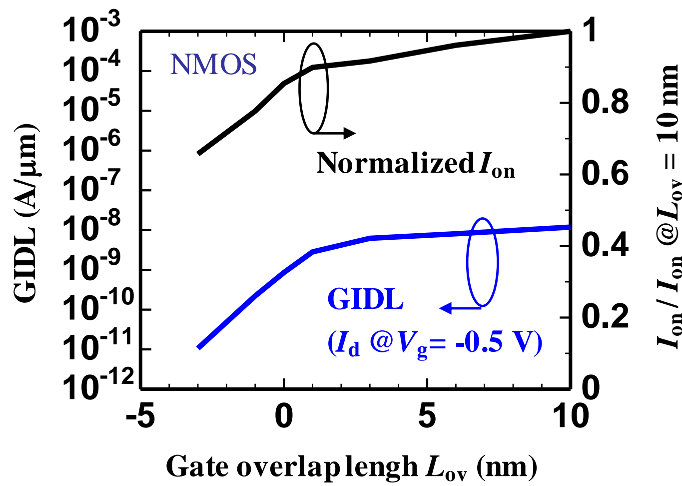


Fig. 3.2 Simulated NMOS $I_d - V_g$ characteristics as a function of gate overlap length L_{ov} at V_{dd} = 1.2 V. The inset shows the potential distribution in SOTB structure at V_g = -0.5 V.

3.3 Ultralow off-current

The subthreshold characteristics of 50-nm-gate-length SOTB MOSFETs at $|V_{ds}|$ = 1.2 V with controlled L_{ov} for small I_{off} are shown in Fig. 3.3. The off-state drain currents were less than 1 pA/μm owing to the reduction of GIDL. The desired symmetrical V_{th} were successfully obtained with a single Ni FUSI gate, and I_{on} = 313 μA/μm for NMOS and 232 μA/μm for PMOS at I_{off} = 1 pA/μm were obtained. These SOTB MOSFETs have also suppressed the short channel effect even with the intrinsic channel because of the thin SOI and BOX layers. As shown in the simulation, both I_{on} and I_{off} decreased with L_{ov} reduction. These I_{on}/I_{off} values are in good agreement with the data based on bulk or FD-SOI technology for LSTP applications [3.5].

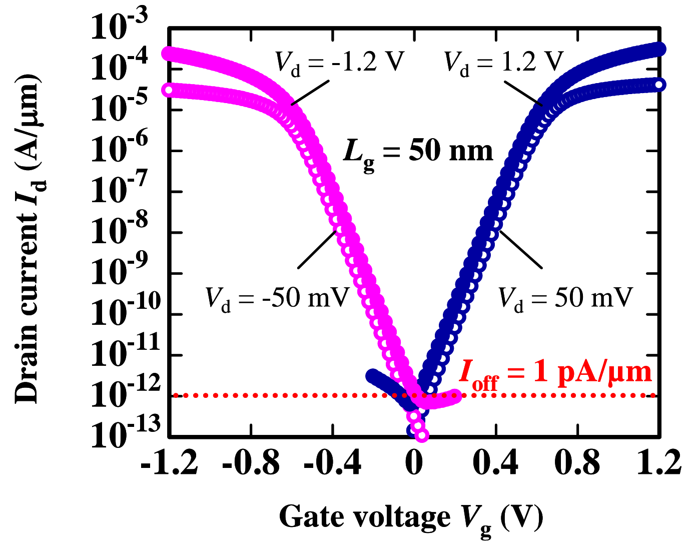


Fig. 3.3 I_d- V_g characteristics of 50-nm-gate-length SOTB CMOS with controlled L_{ov}. The subthreshold slopes are 79 mV/decade for NMOS and 79 mV/decade for PMOS respectively.

Figure 3.4 plots minimum drain current (I_{dmin}) and I_{on} versus L_{ov}. The I_{dmin} value is determined from the GIDL and subthreshold leakage, and is in a tradeoff relationship with I_{on}. Its typical value can be reduced to (or less

than) 1 pA/μm when L_{ov} is less than 4 nm. To adjust I_{dmin} to the desired I_{off} value, the control of impurity density in the substrate beneath the BOX layer and back-gate biasing are useful. The optimum L_{ov} condition should be determined by taking the inverter delay (τ_{pd}) into account, which will be discussed later.

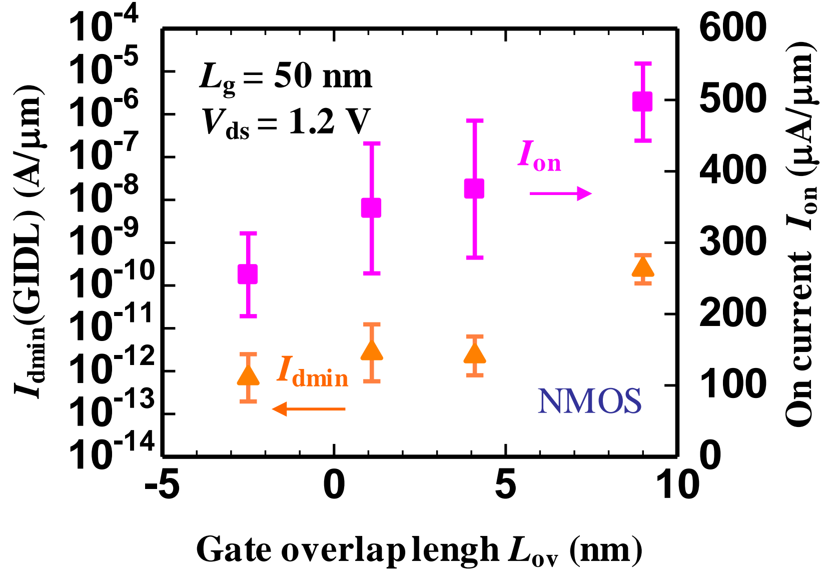


Fig. 3.4 Measured dependency of NMOS device performance on L_{ov} at L_g = 50 nm, and V_{ds} = 1.2 V. GIDL current is expressed as minimum drain current I_{dmin} within the applied gate bias V_g.

3.4 Boosted performance by using back-gate biasing

In this SOTB device, driving performance can be drastically boosted as occasion demands. Figure 3.5 shows variable transistor performance of a 50-nm-gate-length SOTB CMOSFET by changing V_{bg} from reverse 1.2 V to forward 1.2 V in 0.1-V increments. In this device, I_{off} can be reduced a little in the standby-mode by applying reverse V_{bg}. It should be noted that at high reverse V_{bg}, I_{off} slightly increases due to GIDL. On the other hand, as forward

V_{bg} increases, I_{on} can be drastically increased to more than the typical I_{on} values of conventional LSTP bulk CMOS (500 and 250 μA/μm for NMOS and PMOS). Figure 3.6 shows a comparison of the 61-stage inverter delay τ_{pd} between SOTB CMOSFETs with various L_{ov} and conventional LSTP bulk CMOSFETs at V_{dd} = 1.2 V. These τ_{pd} values are proportional to the reciprocal of the through current I_{cc}. The τ_{pd} values of the SOTB CMOSFETs with L_{ov} of 9 nm is the same as those of the conventional LSTP bulk CMOSFETs because of high overlap capacitance. By reducing L_{ov} to less than 4 nm, I_{on} decreases, but faster τ_{pd} values are obtained at the same I_{cc}. Additionally, the τ_{pd} values can be further reduced by the boost mode in calculation. These results strongly suggest that proper control of L_{ov} reduces standby current and improves speed performance, and that boosting the forward-bias is effective for further improving circuit performance.

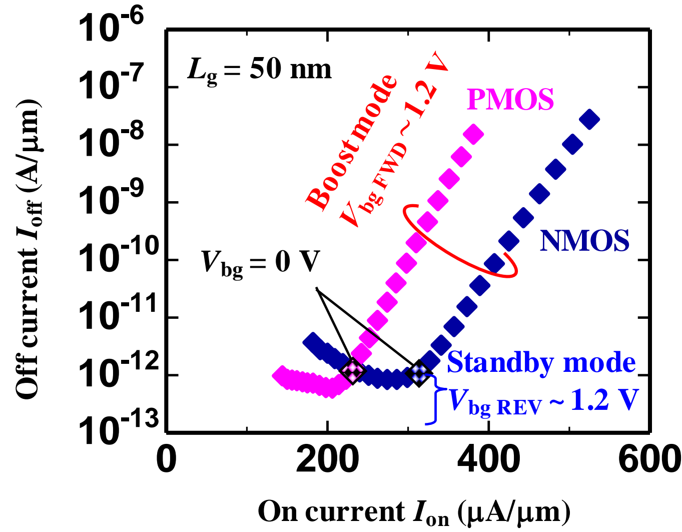


Fig. 3.5 Variable transistor performance of 50-nm-gate-length SOTB CMOSFET using back-gate bias V_{bg}. V_{bg} applied from reverse 1.2 V to forward 1.2 V, 0.1-V increments at $|V_{ds}|$ = 1.2 V.

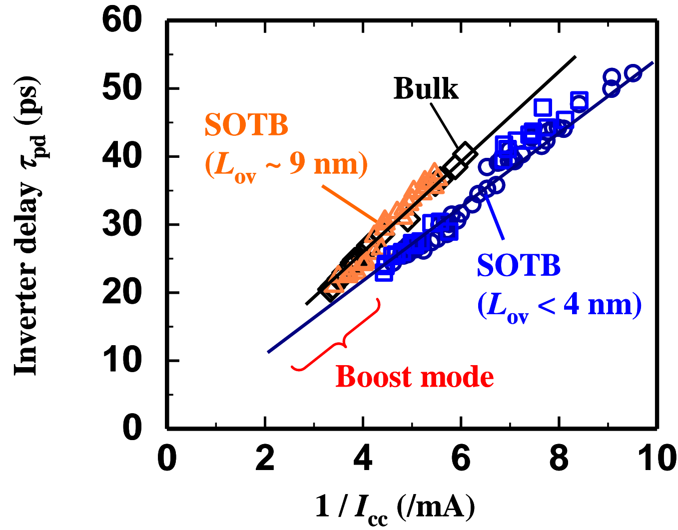


Fig. 3.6 Comparison of 61-stages-inverter delay τ_{pd} between conventional bulk CMOSFETs and SOTB CMOSFETs with various L_{ov} at V_{dd} = 1.2 V. The τ_{pd} value of an SOTB CMOSFET with L_{ov} of 9 nm was slower than the ones of SOTB CMOSFET with L_{ov} < 4 nm, and the same as the bulk values despite the increase of on current because of high overlap capacitance

3.5 Variability of SOTB CMOSFET

As for conventional bulk structures, reverse biasing can be used to reduce the standby leakage after fabrication. However, it is less effective because both V_{th} variation and GIDL increases [3.6]. In the SOTB case, GIDL is suppressed enough by controlling L_{ov}, and forward V_{bg} is also effective in adjusting V_{th} variation. The die-to-die compensation for characteristic variation of each chip is demonstrated in Fig. 3.7. Each curve represents a 50-nm-gate length NMOS device characteristic of each chip. The black curves are those without V_{bg} control, and the red ones are those with V_{bg} control, that is, adjusting V_{bg} for each transistor to obtain the target V_{th}. The range of V_{bg} is from -1.2 to 1.2 V in 0.1-V increments. By this control, the worst I_{off} value can be decreased by nearly one order of magnitude and its

range can be reduced to less than 1 order of magnitude. At the same time, the worst I_{on} value can be improved up to 25%. This die-to-die variation is well known as "global" variation, and its main source is process variation, representing gate length and layer thicknesses. In this SOTB device, the variation of drain current is caused by not only V_{th} variation but also parasitic S/D resistance (R_{sd}) variation. This is because that the height of raised source/drain structure and the condition of ion implantation were currently not fully optimized. Thus, in this case, I_{on} variation remains quite large. It will be further improved with another back-gate control. These results indicate that the process yield can be improved by using back-gate bias trimming for below-specification chips, or the specification can be raised in prospecting the back-gate bias effects.

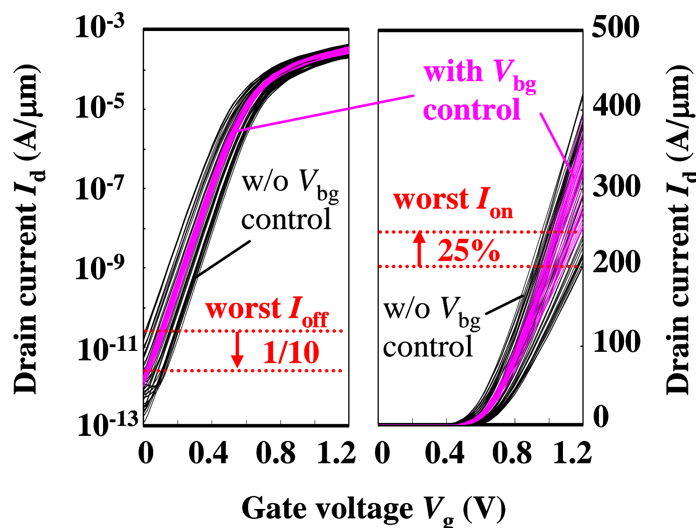


Fig. 3.7 Demonstration of die-to-die back-gate bias control to adjust I_{on}/I_{off} variation. Forward back-gate bias can be effectively used in SOTB schemes.

The nominal V_{th} cumulative probability plot of SOTB CMOSFETs indicates that the distribution is random and SCE is suppressed even down to 50 nm. The Pelgrom plot is shown in Fig. 3.8. The slope of the plot, the Pelgrom coefficient A_{vt}, is 1.8 and 1.5 mVμm for NMOS and PMOS, respectively. These values are about half those of conventional bulk CMOSFETs of the

same technology generation due to the intrinsic channel without halo implant. Impurities below the BOX layer have a small impact on the variability. The local component of variation is also plotted. To extract the local variation of V_{th}, the difference between the forward and the reverse measurement by exchanging the source and drain was used [3.7]. It has already been confirmed that this method simply represents the local variation of adjacent pair transistors [3.8]. These results suggest the SOTB CMOSFET is robust in terms of variability.

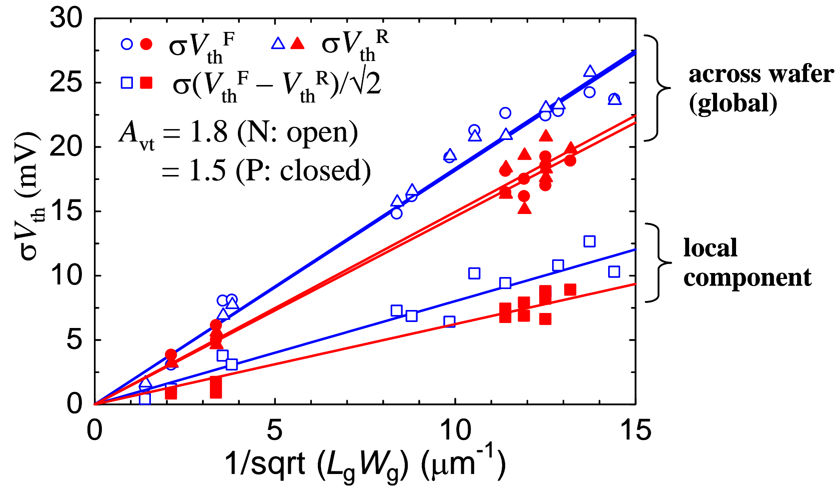


Fig. 3.8 Pelgrom plot of SOTB CMOSFETs for both global and local components.

Figure 3.9 shows σV_{th} as a function of V_{bg} at V_{ds} = 1.2 V. The device sizes are the same as L / W = 50 / 98 nm. A simulation curve is also shown. In the simulation, it is considered at possible variations, such as gate length, thicknesses of SOI, BOX, and gate-oxide layers, as well as impurity concentrations in both the SOI layer and the substrate below the BOX layer [3.9]. The assumed variations simply are ± 10 % for the process-induced variations as a result of 3σ deviation. For the RDF, the dopant concentrations of SOI and substrate are calculated by peforming Monte Carlo simulations. In this method, not only the number of dopants but also

the positions of dopants in both the channel and substrate are taken into account. The increase in σV_{th} under forward bias is due to enhanced short channel effect which mainly caused by gate-length variation. On the other hand, the increase under reverse bias is mainly due to a back-gate bias factor γ, described as ΔV_{th} / ΔV_{bg}. This factor γ depends on the thicknesses of gate-oxide, SOI and BOX layers, and σV_{th} increases with V_{bg} by the γ variation. Under the SOTB device structure, regardless of possible causes such as thicknesses of the SOI and BOX layers and the impurities below the BOX layer, σV_{th} under a wide range of V_{bg} is still smaller than that of conventional bulk devices. When considering the variability in the future generation, other causes such as line edge roughness (LER) or metal gate granularity should be taken into account [3.10].

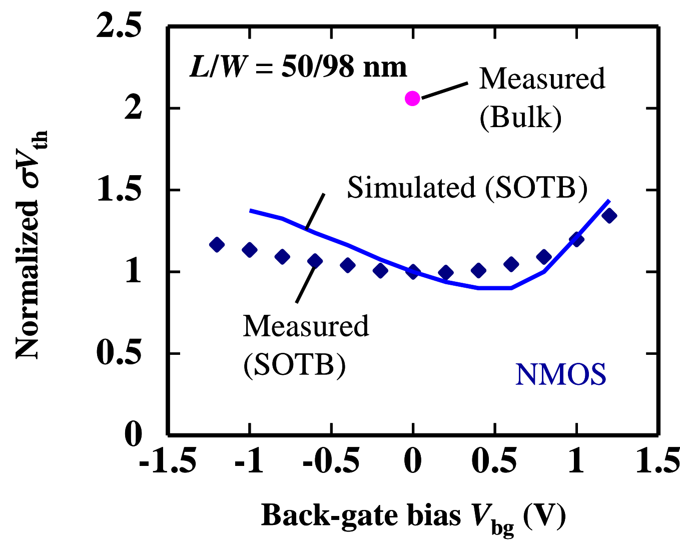


Fig. 3.9 V_{th} variation (σV_{th}) as function of back-gate bias V_{bg} at V_{ds} = 1.2 V. The solid lines are simulated σV_{th} using device simulator.

3.6 Reduction of power consumption

The variability of SOTB CMOSFETs has a significant impact on power consumption of LSIs. Because SRAM has been integrated in recent VLSI

circuits with large capacities occupying large areas, reducing the power consumption of the SRAM is becoming increasingly important. Moreover, since the SRAM circuit is most sensitive to the local V_{th} variation, it is assumed that achieving low V_{dd} is most difficult with SRAM. Figure 3.10 plots the characteristics of 6T-SOTB SRAM cells 0.99 μm^2 in area. The static noise margins (SNM) of 0.357 V at V_{dd} = 1.2 V and 0.142 V at V_{dd} = 0.6 V indicate a much more stable operation in comparison with conventional bulk ones. The fail bit count (FBC) analysis indicated that the SOTB-SRAM can operate as low as 0.6 V, whereas the bulk SRAM with the same cell size operates at 1.1 V [3.11].

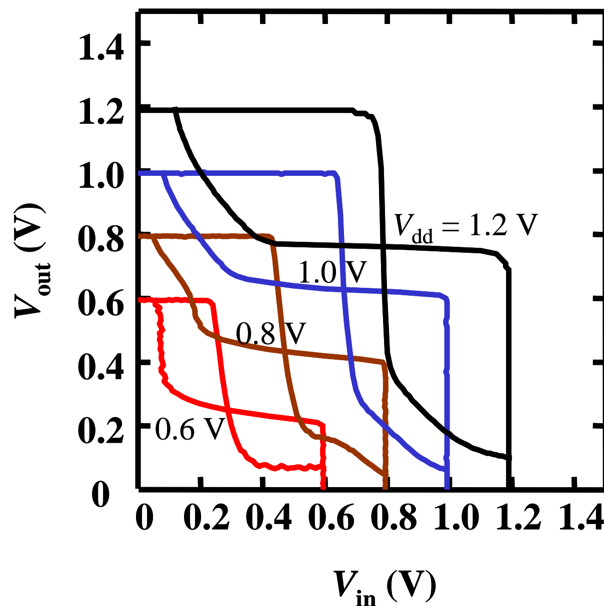


Fig. 3.10 Measured butterfly curves of 50-nm-gate-length SOTB SRAM cell.

The variability and ultra-low off current of SOTB CMOSFETs have also a significant impact on standby power consumption of LSIs. The total standby leakage of a conventional 6T-SRAM cell is roughly expressed as

$$I_{standby} = 3I_{off} + 2I_{gate} \tag{3.1}$$

where I_{gate} is the gate leakage when the gate node of a transistor is high. The standby leakage of an SRAM between SOTB and bulk devices was calculated with taking variability into account. When V_{th} decreases from a typical value (ideally at the minimum I_d point determined both by subthreshold and GIDL currents), I_{off} increases on the subthreshold slope of 80 mV/decade. On the other hand, I_{off} also increases with larger V_{th} because of the GIDL with a slope of 400 mV/decade. The summation of off-currents taking V_{th} distribution into account is expressed as

$$\Sigma I_{off} = \int P(\Delta V_{th}) \times I_{off}(\Delta V_{th}) \quad (3.2)$$

where P is a probability of V_{th} in the distribution, and ΔV_{th} is the deviation from the typical V_{th}. Figure 3.11 shows a comparison of the V_{th} probability distributions as a function of the deviation from the typical V_{th} (σV_{th}). The σV_{th} of SOTB and bulk devices is 27 and 54 mV, respectively. I_{gate} is calculated as a constant without taking variability into account because its value is much smaller for LSTP applications, where J_g is 2 x 10^{-3} A/cm^2. The integrated standby leakage of 1-Mbit SRAM is shown in Fig. 3.12. One typical I_{off} of SOTB devices is calculated as 10 pA/μm compared with bulk devices. The other typical I_{off} value of SOTB devices is 1 pA/μm. When the typical I_{off} = 10 pA/μm, the standby leakage of the SOTB device is 44% that of the bulk ones. This result indicates that reducing σV_{th} by half also reduces the standby leakage by half. Moreover, when the typical I_{off} of an SOTB device = 1 pA/μm, the standby leakage can be further reduced to 6%. In the case of I_{off} = 1 pA/μm, which indicates a lower on-state current, the driving performance can be boosted by using back-gate biasing in the SOTB technology.

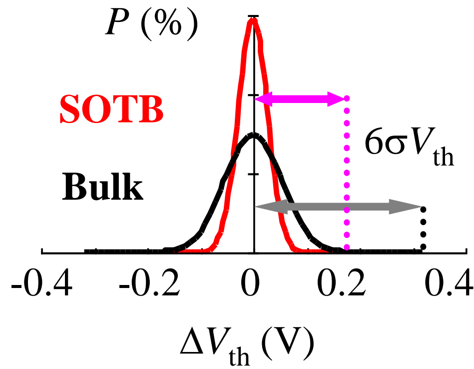
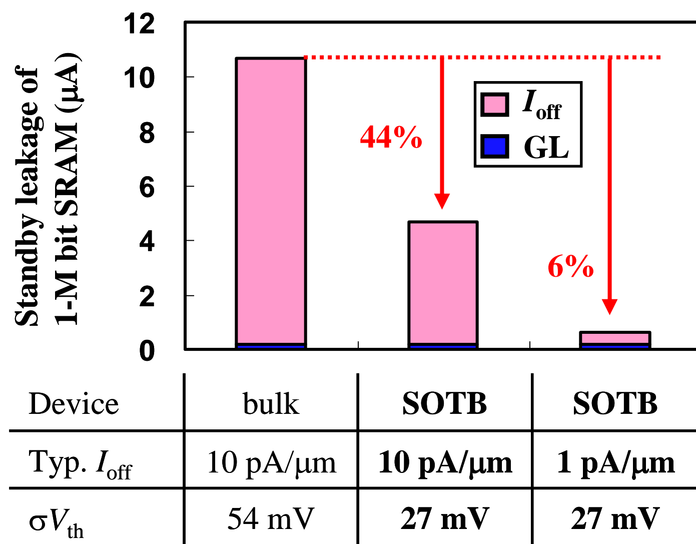


Fig. 3.11 Comparison of V_{th} distribution between conventional bulk CMOSFETs and SOTB CMOSFETs. The standard deviation (σV_{th}) of SOTB devices is half of bulk devices. The range up to 6 σV_{th} was calculated.



Device	bulk	**SOTB**	**SOTB**
Typ. I_{off}	10 pA/μm	**10 pA/μm**	**1 pA/μm**
σV_{th}	54 mV	**27 mV**	**27 mV**

Fig. 3.12 Estimated standby leakage of 1-M bit SRAM taking V_{th} variation into account. Gate leakage (GL) was calculated as constant and gate width was 90 nm.

3.7 Conclusion

The off-current of SOTB CMOSFET was investigated and successfully reduced to 1 pA/μm. It was found that the major element of the off-current in the deep subthreshold regime was GIDL. And the GIDL was adequately reduced by precisely controlling L_{ov}. The optimization of L_{ov} also reduces the overlap capacitance and produces a faster inverter delay than conventional LSTP bulk CMOSFETs. In addition, it was clarified what extent the low variability of SOTB CMOSFET impacted on the reduction of the power consumption. Both ultralow off-current and small variation in SOTB CMOSFETs drastically reduce the standby leakage of SRAMs. These SOTB schemes described here will guarantee the successful reduction of standby power consumption with superior performance in VLSI circuits.

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Chapter. 4 Hybrid Integration of SOTB and Bulk CMOSFETs

Abstract

Hybrid integration of bulk CMOSFET into SOTB technology is presented in this chapter. The novel process of the hybrid integration was developed. And the characteristics of the integrated bulk CMOSFET on the Si substrate were investigated. It is shown that there is no damage of the process for the Si substrate. It is also shown that the characteristics of the integrated bulk CMOSFET are comparable to those of conventional bulk CMOSFETs. As in the integrated bulk CMOSFET with FUSI gates, the desirable V_{th} and the uniformity of the values in a wafer are confirmed.

Chapter.4 Hybrid Integration of SOTB and Bulk CMOSFETs

Contents

4.1 Introduction
4.2 Hybrid integration of SOTB and bulk CMOSFETs
4.3 Characteristics of hybrid bulk CMOSFET for I/O operation
4.4 Conclusion
4.5 References

4.1 Introduction

Some intrinsic problems with FD-SOI technology such as poor electrostatic discharge (ESD) susceptibility and low breakdown voltage are well known [4.1]. In SoCs or microcomputer chips, however, the supply voltages of 3.3 V or 5 V are used generally. The devices for analog applications are also used in higher voltages than those of logic devices. Therefore, transistors for high-voltage operation are usually integrated in a conventional chip.

The adverse effects such as low breakdown voltage of FD-SOI CMOSFETs can be easily avoided by combining bulk technology on the same wafer. The previous approach to integrating SOI and bulk technologies required the use of selective epitaxial growth to compensate for the height difference [4.2]. However, this approach requires over 100-nm Si-epitaxial layer with high quality, which significantly increases process complexity.

In this SOTB structure, bulk CMOSFETs for high-voltage I/O operation, ESD protection, and analog circuits can be easily integrated by removing the ultrathin SOI/BOX layers. This simplified SOTB/bulk hybrid technology is preferable because no design change for the conventional peripheral circuits is required. In this chapter, the novel hybrid integration is presented for the first time. The quality of the exposed surface of the Si substrate was examined. And hybrid bulk CMOSFETs with both poly-Si and FUSI gates were fabricated. The characteristics and reliabilities were investigated as a reference of those of conventional bulk CMOSFETs.

4.2 Hybrid integration of SOTB and bulk CMOSFETs

Figure 4.1 shows a process flow and a cross-sectional TEM image of a SOI/bulk hybrid structure. After the STI formation, the SOI layers (T_{SOI} ~ 12 nm) on both the well contact and bulk active regions were removed by dry etching using a BOX layer (T_{BOX} ~ 10 nm) as a stopper. In this step, isotropic and anisotropic etchings were combined to remove the SOI layer at the STI edge especially. After removing patterned photo resists, the SiO_2 layers on the both SOI and substrate were removed by 10% fluoric acid (HF) wet-etching. In some samples, a sacrificial oxidation before the gate

oxidation was done to remove the surface of the Si substrate in order to investigate the damage of the dry-etching.

Due to the small step height of 22 nm (T_{SOI} + T_{BOX}), gate patterning can easily be performed on both the SOI and bulk regions simultaneously. This process enables the SOTB/bulk hybrid structure to be fabricated without requiring epitaxial growth to compensate for the height difference. The SOI region is on the left side of the TEM image, and the integrated bulk region is on the right. Smooth gate patterning without voids on both the SOI and bulk regions was confirmed. These integrated hybrid bulk CMOSFETs with a 7.5-nm-thick gate dielectric were fabricated on the exposed surface of the silicon support wafer by removing SOI/BOX layers.

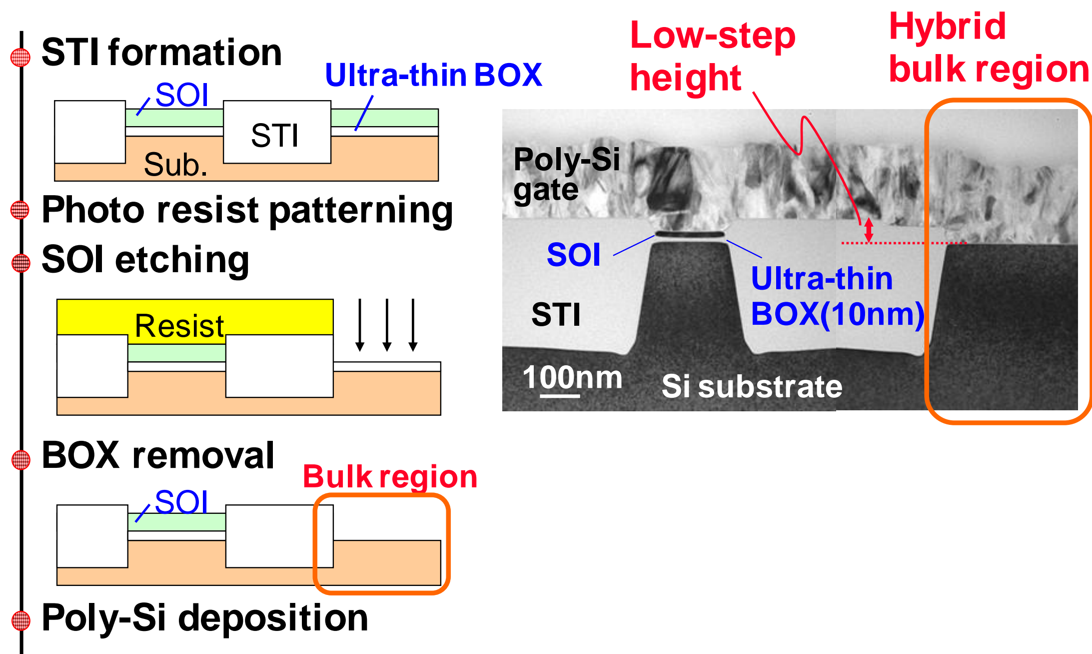

Fig. 4.1 Process flow of hybrid SOI/bulk fabrication and a cross-sectional TEM image of poly-Si gate on hybrid SOI/bulk regions

The TEM images of the cross sections of the fabricated hybrid bulk transistors were shown in Fig. 4.2 (with poly-Si gate) and Fig. 4.3 (with FUSI gate). The thicknesses of the gate dielectrics and the gate lengths were both about 7.5 nm and 370 nm, respectively. In the FUSI gate device, it was

confirmed that the gate was fully silicided even in this long gate length.

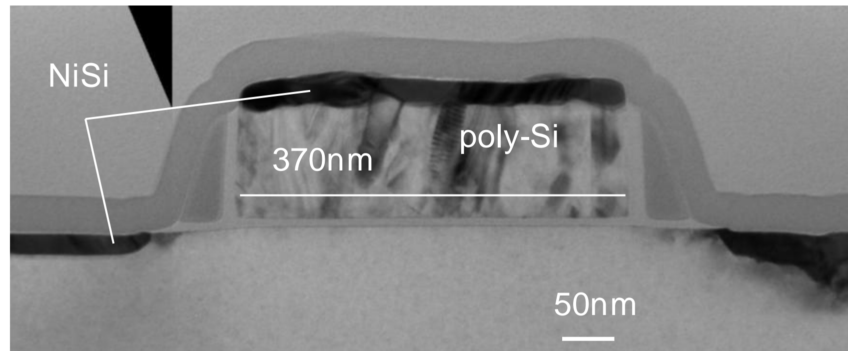

Fig. 4.2 A TEM image of a fabricated hybrid bulk MOSFET with a poly-Si gate

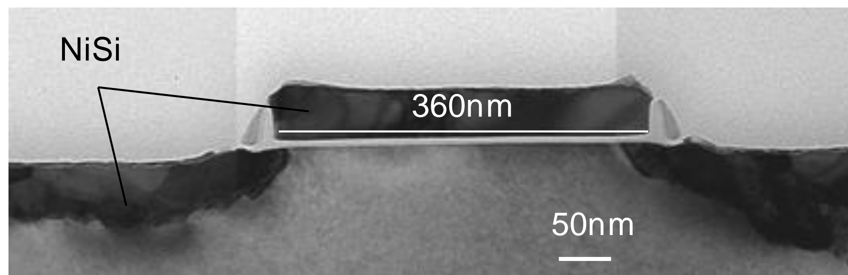

Fig. 4.3 A TEM image of a fabricated hybrid bulk MOSFET with a FUSI gate

4.3 Characteristics of hybrid bulk CMOSFET for I/O operation

The fabricated hybrid CMOSFETs for 3.3-V operation were on the exposed surface of the silicon support wafer, by removing SOI/BOX layers. The quality of the surface after BOX removal is a concern in this process. Thus, the mobility and gate oxide interface trap density (D_{it}) of the hybrid bulk CMOSFETs were evaluated by using charge pumping method [4.3]. Carrier mobilities as high as a universal curve were achieved as shown in Fig. 4.4.

D_{it} as low as 10^{11} $eV^{-1}cm^{-2}$ was achieved for both FUSI and poly-Si devices with no sacrificial oxidation of the surface as shown in Fig. 4.5. These results indicate that little damage is caused by dry etching during the SOI-layer removal. This is considered to be because the BOX layer is used as a stopper.

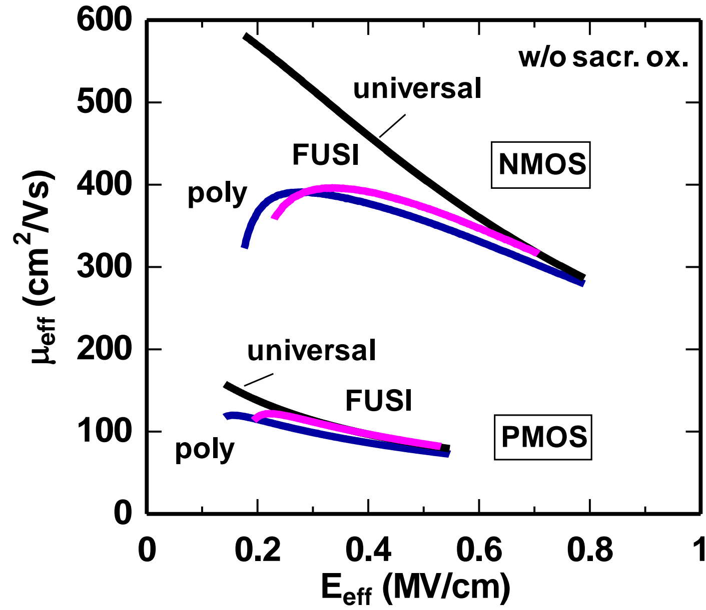

Fig. 4.4 Mobilities of hybrid bulk CMOSFETs for I/O operation

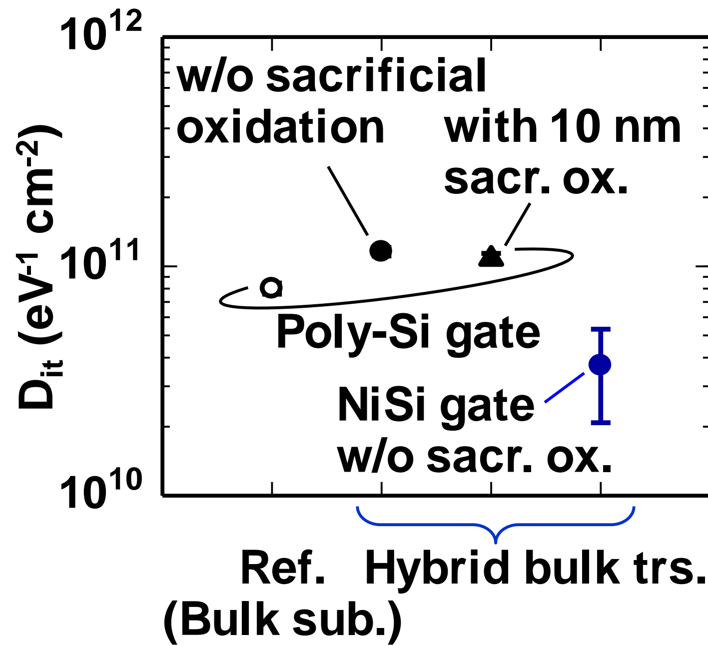

Fig. 4.5 D_{it} values of hybrid bulk MOSFETs

The FUSI gate process of SOTB CMOSFET is naturally applied also to hybrid bulk CMOSFET. In order to adjust the V_{th} of the hybrid bulk CMOSFET, an ion implantation for the channel of the hybrid bulk CMOSFET was controlled. The subthreshold characteristics of the 0.4-μm FUSI gate devices at $|V_{dd}|$ = 3.3 V are plotted in Fig. 4.6. The characteristics are also summarized in Table 4.1. The optimum values of V_{th} for the I/O transistor were obtained even in the NiSi FUSI gate. This indicated the proper control of the phase of NiSi was achieved [4.4]. The characteristics of the hybrid bulk transistor were almost comparable to those of a conventional bulk transistor. The large off-currents were due to the p-n junction leakage caused of the excess silicidation in the S/D regions. This would be solved in applying a raised S/D structure.

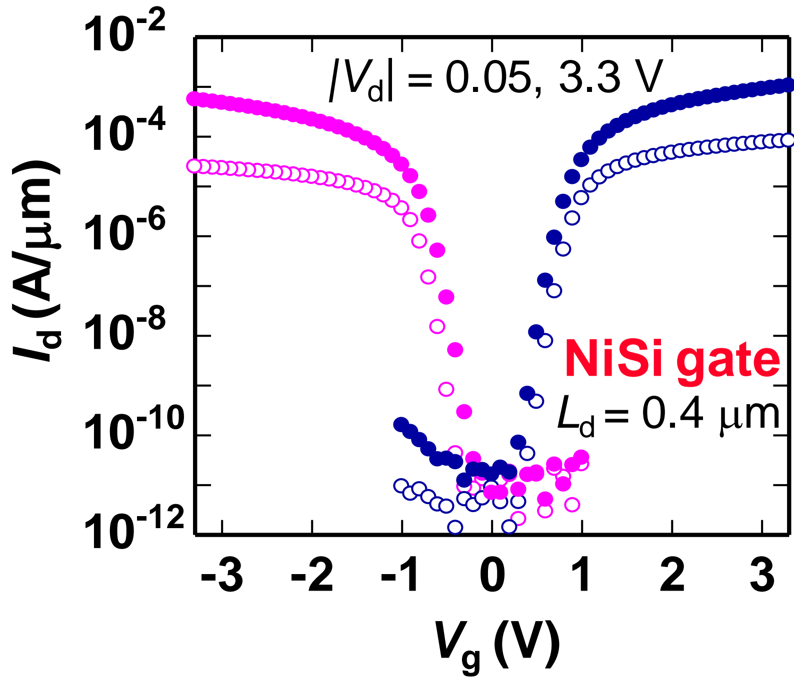

Fig. 4.6 I_d- V_g characteristics of FUSI-gate hybrid bulk CMOSFET

Table 4.1 Characteristics of fabricated hybrid CMOSFETs

	Target	Results
V_{dd} (V)	3.3	3.3
L_g (nm)	390	360
T_{ox} (nm)	7.5	7.5
I_{on} (NMOS) (μA/μm)	530	513
I_{on} (PMOS) (μA/μm)	275	272
I_{off} (NMOS) (pA/μm)	0.1	8.9
I_{off} (PMOS) (pA/μm)	0.5	4

Finally, the reliability of the hybrid bulk transistor was investigated. Figure 4.7 shows a hot carrier injection (HCI) characteristics of the hybrid bulk NMOS. The stress conditions at 25°C are as follows. The V_{gs} and V_{ds} are 1.65

V and 3.3 V, respectively. This condition corresponds to the maximum substrate current which caused by impact ionization. The estimated lifetime by this test is 0.14 year at 3.63-V operation, which is a standard value for these devices. Time-dependent dielectric breakdown (TDDB) test was also evaluated. The V_{gs} values were from 9 to 10 V at 125°C. The mean times of the breakdown were plotted in Fig. 4.8. A sufficiently long lifetime over 10 years is ensured at 3.3-V operation.

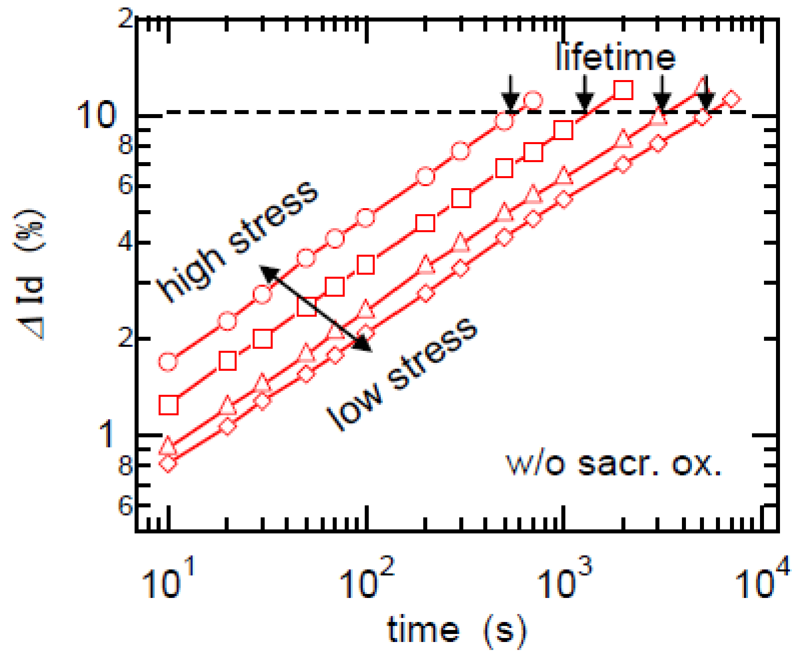

Fig. 4.7 HCI characteristics of hybrid bulk NMOS

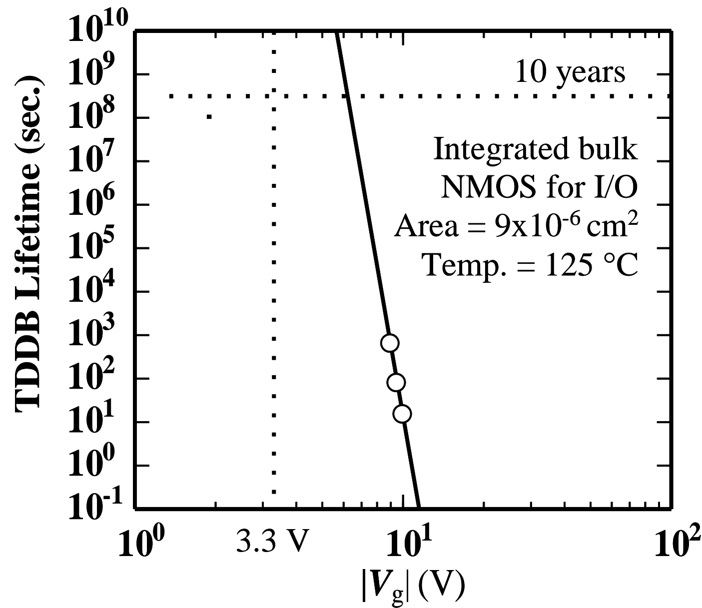

Fig. 4.8 TDDB lifetime of hybrid bulk NMOS for I/O operation

4.4 Conclusion

A hybrid integration, in which SOTB and bulk CMOSFETs are fabricated at the same time, has been developed. It was shown that the process caused no damage to the exposed substrate. The quality of the gate dielectric of the hybrid bulk device was confirmed by evaluating the mobility, D_{it} and TDDB of the device. It was also shown that the characteristics of the integrated hybrid bulk CMOSFETs were comparable to those of conventional bulk CMOSFETs. This SOTB/bulk hybrid technology can make it possible to integrate peripheral circuits into FD-SOI platform, which has been a weak point until now. Hence, this hybrid technology can bring the same usability as conventional platform.

4.5 References

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Chapter. 5 HCI and NBTI Reliability of SOTB CMOSFET

Abstract

The SOTB CMOSFET is one of the strong candidates for further scaling because of its smallest V_{th} variation and back-bias controllability. This study focuses on its reliability, that is, hot-carrier-injection (HCI) degradation for NMOSFET and negative-bias temperature instability (NBTI) for PMOSFET. A comparison of the SOTB CMOSFET with a conventional bulk CMOSFET shows that the SOTB structure, which has a low-dose channel without halo implant, exhibits higher reliability. The impact of wide-range back-biasing in SOTB devices on reliability is determined; that is, back-biasing changes the mechanism of HCI degradation but does not affect NBTI degradation.

Chapter.5 HCI and NBTI Reliability of SOTB CMOSFET

Contents

5.1 Introduction
5.2 Electrical characterization
5.3 Hot carrier injection in SOTB NMOSFET
5.4 Effect of back-biasing in the case of hot carrier injection
5.5 Negative bias temperature instability in SOTB PMOSFET
5.6 Effect of back-biasing in the case of negative bias temperature instability
5.7 Conclusion
5.8 References

5.1 Introduction

Reliability of FD-SOI structure (including SOTB) has not been fully understood. Especially, in the SOTB structure, electric-field strength in the device is different from that in conventional thick-BOX SOI devices because of the thin BOX and the efficacy of back-biasing. In order to put SOTB into practical use, it is very important to guarantee the reliability and understand the mechanism.

In this chapter, hot-carrier injection (HCI) is investigated as representative reliability issues for NMOSFET and negative-bias temperature instability (NBTI) for PMOSFET, respectively. Their characteristics are compared with ones of conventional bulk CMOSFETs. The electric field in the CMOS devices is simulated by using a 2D device simulator. Moreover, wide-range back-biasing through the thin BOX is one special feature of the SOTB device. The influences on both the HCI and NBTI degradation on device performance are examined for the first time.

5.2 Electrical characterization

The SOTB CMOSFETs described in chapter 2 are used for the examination. The channel impurities are implanted into a substrate beneath the BOX with deeper projection range, not into the SOI channel layer. Hence, the SOI layer is very lightly doped (i.e., density lower than 10^{17} cm^{-3}) without using a halo implant. In contrast, the substrate just beneath the BOX layer is doped to about 10^{18} cm^{-3} to adjust V_{th} (in case of V_{th} is about 0.4 V). Conventional bulk CMOSFETs, which have a poly-Si gate and a doped channel with a halo implant, were also fabricated for comparison. The gate dielectrics in all devices are SiON with 1.9-nm EOT. Since universal mobility is obtained [5.1], the Si/SiON interface is considered to be the same quality.

As for the stress-effect measurements, HCI was evaluated at room temperature, and NBTI was evaluated at 125°C. The drain current-gate voltage (I_d - V_g) characteristics were measured at intervals of a certain stress time without recovery operation. V_{th} values were determined by saturation extrapolation. Drain voltage (V_d) for the saturation condition was 1.2 V. The

criteria for the lifetime of the SOTB CMOSFETs was set to 10% degradation from the initial states of the on-current I_{on} or V_{th} at V_d = 1.2 V.

Firstly, the current-voltage characteristic of the SOTB NMOSFET was compared with that of a conventional bulk NMOSFET, as shown in Fig. 5.1. L_g and W_g used in this study were 55 nm and 8 μm, respectively. The device characteristics such as V_{th}, I_{on}, and I_{off} at V_{dd} = 1.2 V of the NMOSFETs were nearly identical. The SOTB NMOSFET achieved comparable driving performance to the bulk NMOSFET because the raised source/drain (S/D) structure sufficiently lowered the S/D resistance, namely, to low less than 200 Ω·μm. No kink effect was observed. This indicates fully-depleted operation without the floating-body effect. The drain breakdown voltage of the SOTB NMOSFET is about 1 V lower than that of the bulk NMOSFET. In FD-SOI devices, holes, which are generated by impact ionization at the drain edge, flow to the source. This hole current biases the source-body junction forward and amplifies drain current due to a parasitic bipolar effect [5.2]. When V_d is over 2 V, I_d of the SOTB NMOSFET starts to increase rapidly, independently of V_g. It is thought that the impact ionization occurred because of the potential difference between the source and drain in short-channel devices, unlike longer channel devices, in which breakdown voltage depends on gate voltage. Note that the drop of drain-source voltage V_{ds} due to the large current (e.g., I_d = 1000 μA/μm) through R_{sd} (200 Ω·μm) is small enough (0.2 V) to be ignored.

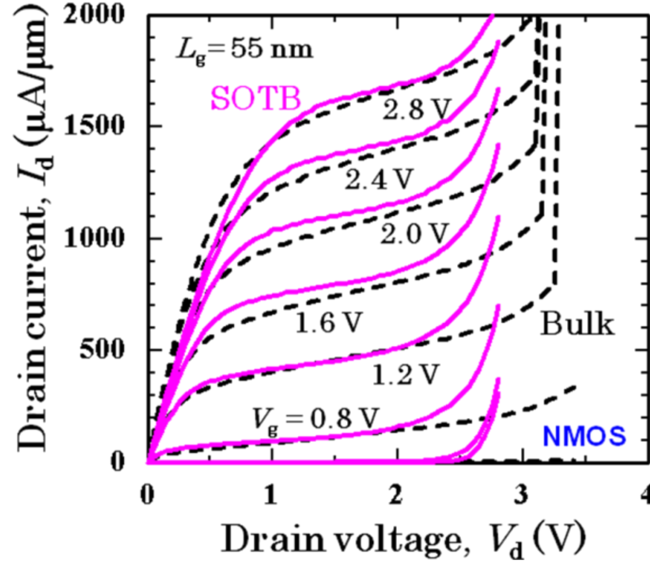


Fig. 5.1 Comparison of I_d- V_d characteristics between SOTB and bulk NMOSFETs

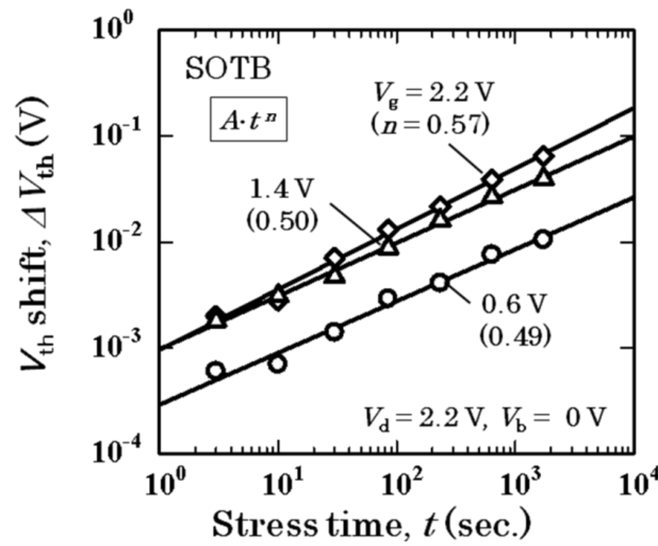
5.3 Hot carrier injection in SOTB NMOSFET

In conventional bulk MOSFETs, the largest degradation due to HCI used to occur at $V_g = V_d / 2$, which corresponds to maximum substrate current (I_{sub}). For recent short-channel devices, however, the worst case of HCI has been reported to change to the channel-hot-electron (CHE) condition at $V_g = V_d$. On the other hand, since the hole-current due to impact ionization flows to the source in SOI MOSFETs, it cannot be evaluated by monitoring I_{sub}. It is confirmed that the worst case degradation of HCI is at $V_g = V_d$ in both SOTB and bulk NMOSFETs as shown in Fig. 5.2. The time dependence of threshold voltage shift (ΔV_{th}) is represented by power-law as

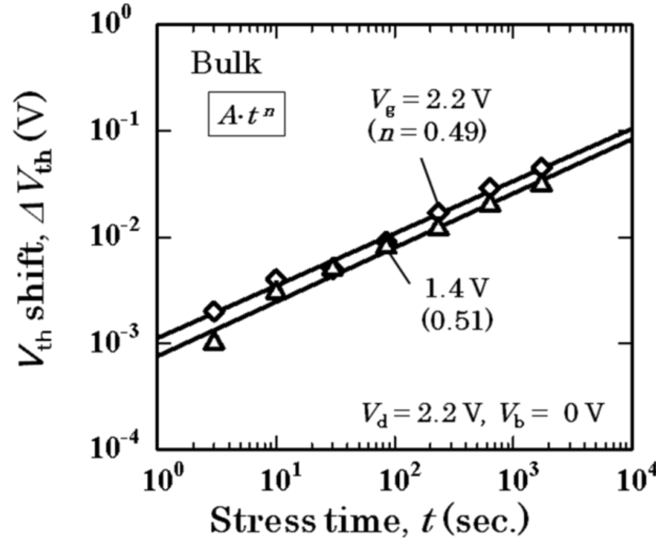
$$\Delta V_{th} = A\, t^{n} \tag{5.1}$$

Here, n is the gradient of the straight line in the Fig. 5.2. The value of around 0.5 at the CHE condition ($V_g = V_d$) indicates that the degradation is

caused by the interface trap generation [5.3]. It was reported that hot-electron injection by CHE generates interface trap and causes less electron trapping in the case of a thin gate oxide [5.4]. As for the results plotted in Fig. 5.2, the power-law slopes are all around 0.5 and independent of V_g. Hence, the mechanism of interface trap generation is the same within the V_g range in the figure, and the dominant factor is presumed to be the potential gradient between the drain and source in both SOTB and bulk devices. The amount of the degradation depends on the total drain current modulated by V_g.



(a) SOTB NMOSFET



(b) Conv. bulk NMOSFET

Fig. 5.2 Threshold-voltage shift (ΔV_{th}) with dependency on gate bias (V_g) under HCI stress in (a) SOTB and (b) bulk NMOSFETs

Figure 5.3 shows the dependency of stress bias (V_{stress}) of HCI degradation at $V_g = V_d$. The power-law slopes are also around 0.5 and independent of V_{stress}. Hence, the interface-trap-generation mechanism is thought to be the same even in the case of V_{stress} over 2 V, in which the parasitic bipolar effect occurs. The HCI lifetimes, defined as 10% degradation of I_{on}, under the CHE condition are shown in Fig. 5.4. The SOTB lifetime dependence on V_{stress} produces a longer lifetime at the operating voltage of 1.2 V than that of bulk device. To clarify the reason for this longer lifetime, the electric-field strengths in the devices with and without halo implant were simulated by using a 2D device simulator. The lateral electric-field strength, E_x, of the silicon surface along the channel (x direction) at V_{stress} = 1.2 and 2.4 V are shown in Fig. 5.5 (a). The profiles of net doping in the SOTB structure with and without halo implant are also shown in Fig. 5.5 (b). E_x at the drain edge of the devices with and without halo implant are almost the same at V_{stress} = 2.4 V due to the high drain voltage. Meanwhile, that of the device without halo implant becomes about 10% lower than that of the devices with halo

implant at 1.2 V, which is due to the abrupt p-n junction between the channel and drain. This is supposed to be the reason why the dependency on V_{stress} is different between SOTB and bulk devices. The advantage of no halo implant was also experimentally-confirmed in SOTB device [5.5].

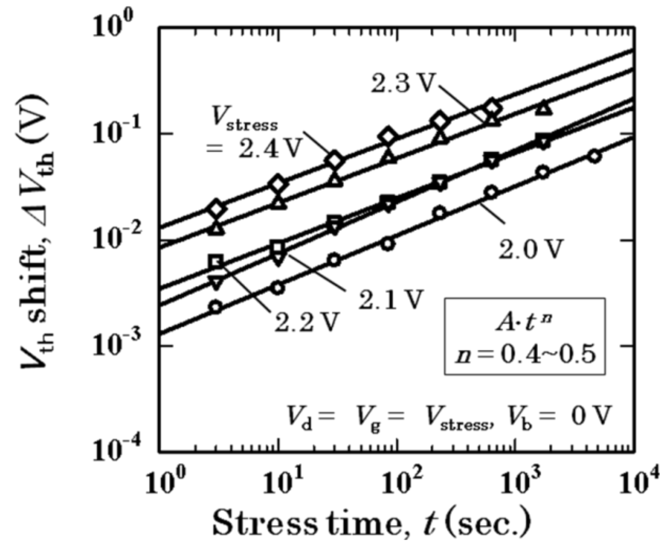


Fig. 5.3 Stress bias (V_{stress}) dependence of HCI degradation in SOTB device

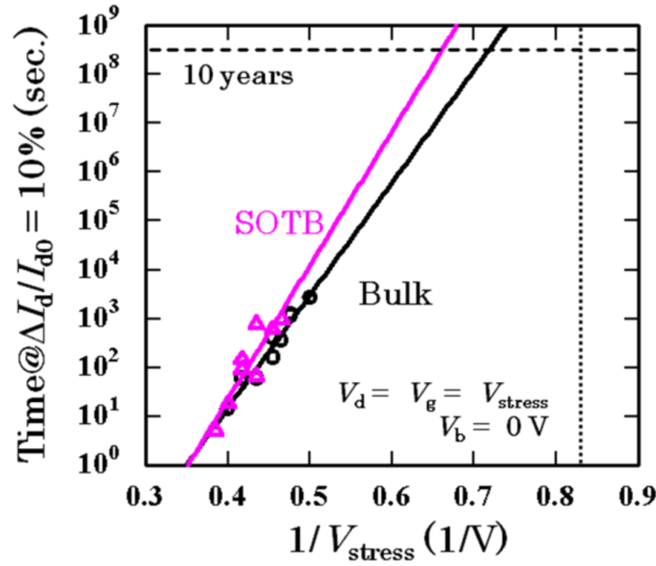
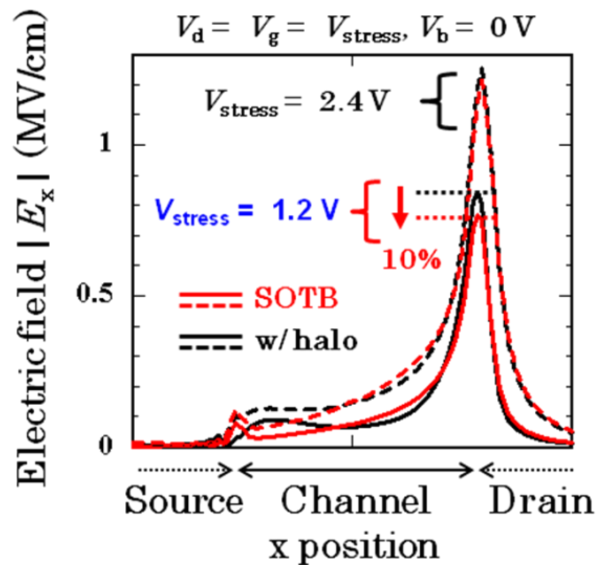
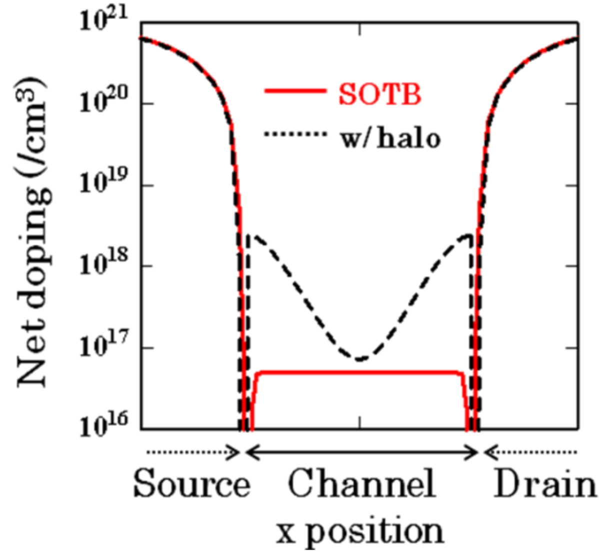


Fig. 5.4 Comparison of HCI lifetime between SOTB and bulk NMOSFETs for $V_d = V_g$



(a)



(b)

Fig. 5.5 (a) Simulated lateral electric-field strengths (E_x) along the channel surface in SOTB structures with or without halo implant at V_{stress} = 2.4 V (dashed) and 1.2 V (solid). (b) Net doping profiles along the channel surface in the SOTB structures with and without halo implant

5.4 Effect of back-biasing in the case of hot-carrier injection

In SOTB devices, wide-range back-biasing including a forward bias higher than 0.6 V is possible without any leakage due to the BOX layer. It significantly changes not only the drive current but also the strength of the vertical electric field strength (E_y). Figure 5.6 shows the dependencies of the HCI characteristics on V_b at V_{stress} = 2.4 V. The slope of the power-law changes from 0.4 at forward V_b to over 1.0 at reverse V_b. A slope of 1.0 at V_g = V_d was reported [5.4]. In that study, electron trapping sites were produced by highly energetic hot-electron injection into the oxide. This phenomenon is different from the electron trapping before stressing (where a power-law slope of 0.2 is typical). When reverse back-biasing is applied in an SOTB

device, the highly energetic hot electrons due to high drain bias would be injected into the gate oxide by enhanced E_y and generate trapping sites, especially at the drain edge. As a result, the electron trapping is thought to be the dominant mechanism in reverse back-biasing. The simulated E_y at the silicon surface along the channel is shown in Fig. 5.7. Though electrostatic potential (ϕ) of silicon surface becomes higher toward drain, drain-side of channel (beyond pinch off point) is depleted due to high drain bias. In the depleted region, the ϕ rapidly changes into the vertical y-direction depending on ϕ of the substrate beneath the BOX layer. Hence, E_y (= -dϕ/dy) increases only at the drain edge in reverse back-biasing. It is noted that the lateral electric field (E_x) does not depend on V_b (not shown). On the other hand, the worst condition is forward back-biasing because a large number of hot electrons was generated by the large drain current (37% larger than that at V_b = 0 V), though the E_y decreases under forward back-biasing. In the case of Fig. 5.6, the large drain current is a main factor for the amount of HCI degradation. Meanwhile, the E_y is considered to change the mechanism of the degradation. To evaluate the lifetime of this forward-bias state, the condition V_b = V_{stress} was used. Even under this forward back-biasing condition, the lifetime is sufficiently longer than 10 years, as shown in Fig. 5.8.

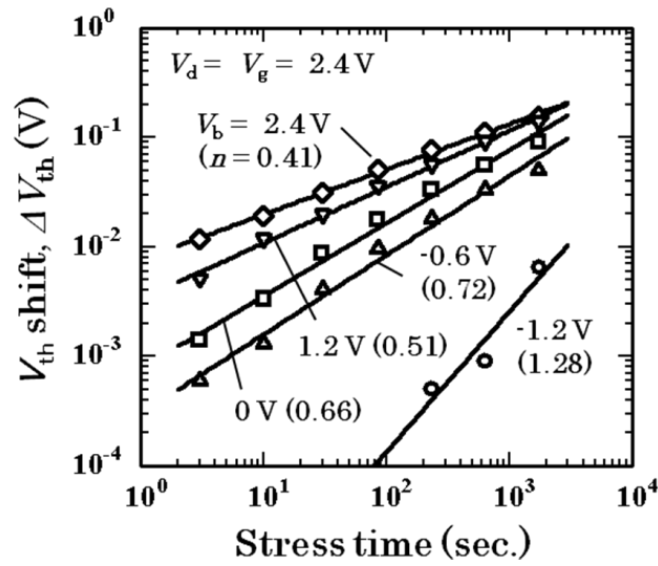


Fig. 5.6 Dependency of HCI characteristics on back-bias (V_b) at V_{stress} = 2.4 V

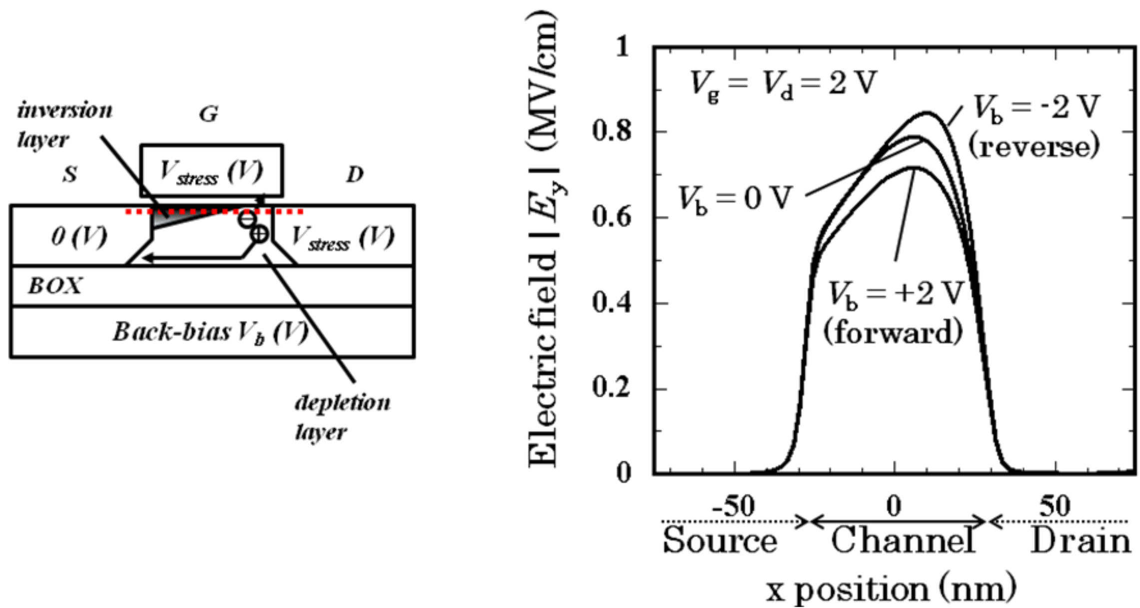


Fig. 5.7 Simulated vertical electric-field strength (E_y) along the channel surface at forward, reverse, and no back-biasing under HCI stress

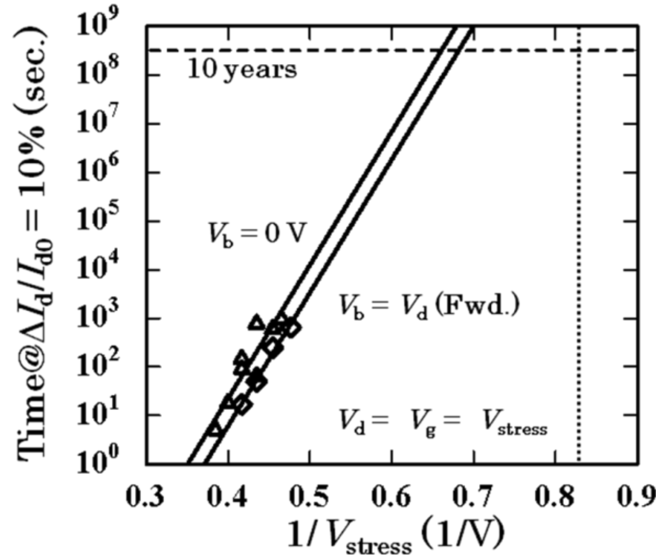


Fig. 5.8 HCI lifetime of SOTB NMOSFET under forward back-biasing (i.e., worst-case degradation)

5.5 Negative bias temperature instability in SOTB PMOSFET

NBTI has not been investigated extensively in FD-SOI devices, although it is recognized as a major reliability issue in recent bulk PMOSFETs. Firstly, the gate leakage currents of SOTB PMOSFET were compared with that of bulk PMOSFET, as shown in Fig. 5.9. In the FUSI-gate SOTB PMOSFET (low-dose channel without halo implant) and the poly-Si-gate bulk PMOSFET (high-dose channel with halo implant), the I_g–V_g characteristics are almost the same. The I_g–V_g characteristic of the poly-Si-gate SOTB PMOSFET (low-dose channel with halo implant) is also the same, though the V_{th} is different. Hence, the gate dielectrics of all devices are considered to be like-quality. Then, the NBTI characteristics of poly-Si-gate SOTB PMOSFET with that of bulk PMOSFET were compared, as shown in Fig. 5.10. The characteristic of SOTB PMOSFET with halo implant was also plotted. The gate bias V_g is set to be the same stress for each device as $V_g - V_{th}$ = -2.0 V at

125°C. The same power-law slopes suggest the same degradation mechanism in the SOTB device as in the bulk device. The *n* value of around 0.3 presumably indicates the well-known reaction/diffusion model, which is the interaction of holes with hydrogen breaks Si-H bonds at the Si/oxide interface and hydrogen diffusion away from the interface into the gate oxide, generating interface traps [5.7]. Although the typical *n* value was 0.25 in this theory, a value over 0.3 was reported in the case of nitrided gate oxide, in which the introduction of nitrogen creates a number of oxide traps [5.8], [5.9]. The NBTI degradation of the SOTB device with halo implant (at 15 keV) is severer than that without halo implant. The degradation in the bulk device with halo implant at 30 keV is further enhanced. These results indicate that the NBTI degradation is enhanced due to additional exposed Si-H bonds caused by the halo and/or a high energy implant [5.10]. The NBTI lifetime for SOTB PMOSFET is estimated to exceed greatly the 10-year specification, as shown in Fig. 5.11.

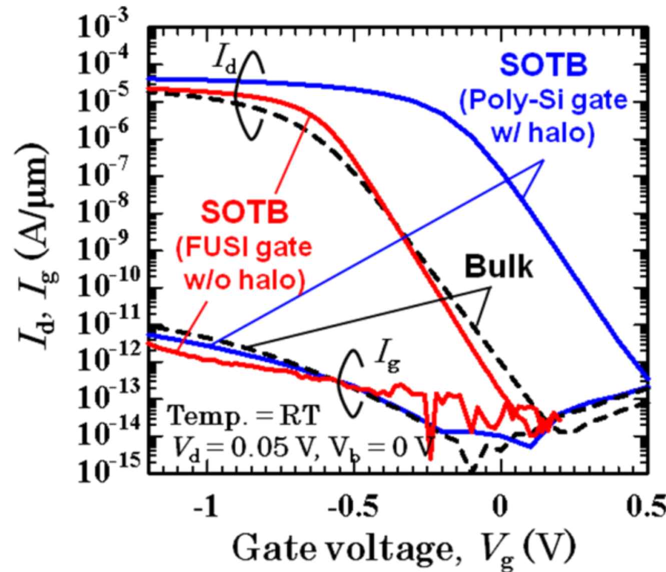


Fig. 5.9 I_d, I_g- V_g characteristics of poly-Si-gate bulk (high-dose channel with halo), poly-Si-gate SOTB (low-dose channel with halo), and FUSI-gate SOTB (low-dose channel without halo) PMOSFETs

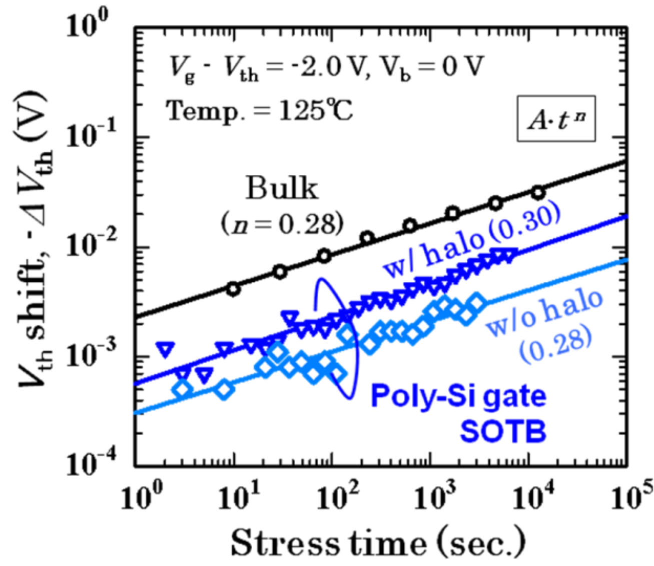


Fig. 5.10 Comparison between NBTI characteristics of SOTB and bulk PMOSFETs

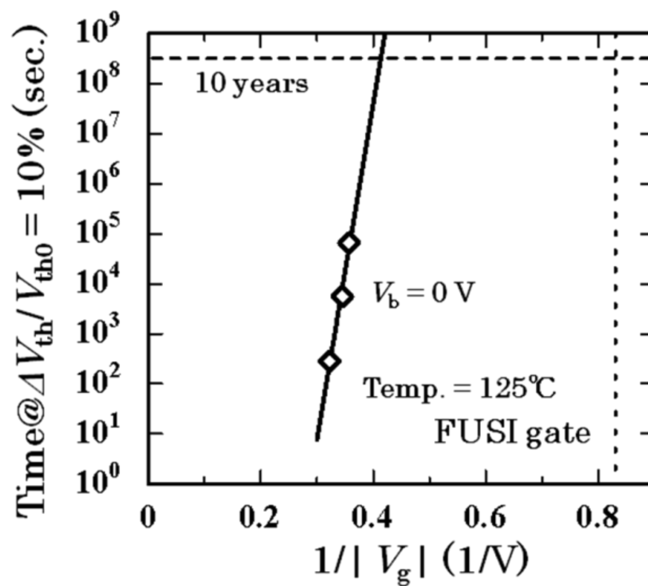


Fig. 5.11 NBTI lifetime of SOTB PMOSFET

5.6 Effect of back-biasing in the case of negative-bias temperature instability

The effect of back-biasing (V_b) on NBTI degradation in FUSI-gate SOTB PMOSFET, as shown in Fig. 5.12, was also investigated. In all three cases, there is little influence of V_b on NBTI degradation in both forward and reverse back-biasing. This result is presumably due to the fact that the influence of back-biasing on the electric fields at the channel surface and/or in the gate oxide is mostly screened by an inversion layer. Simulated vertical electric field (E_y) and hole concentration under the gate electrode as a function of back-bias voltage (V_b) are shown in Fig. 5.13. E_y in the gate oxide is determined by the gate bias (not by back-biasing). It is clear that hole concentration at the silicon surface is slightly influenced by the back-biasing. In addition, substrate hot-hole injection under reverse back-biasing, which enhances NBTI degradation in conventional bulk PMOS [5.11], does not occur in the SOTB structure because of the BOX layer. It is also noted that vertical electric field E_y at the Si surface must be lower in SOTB devices with mid-gap gate metal and low-dose channel than in bulk devices with poly-Si gate and high-dose channel.

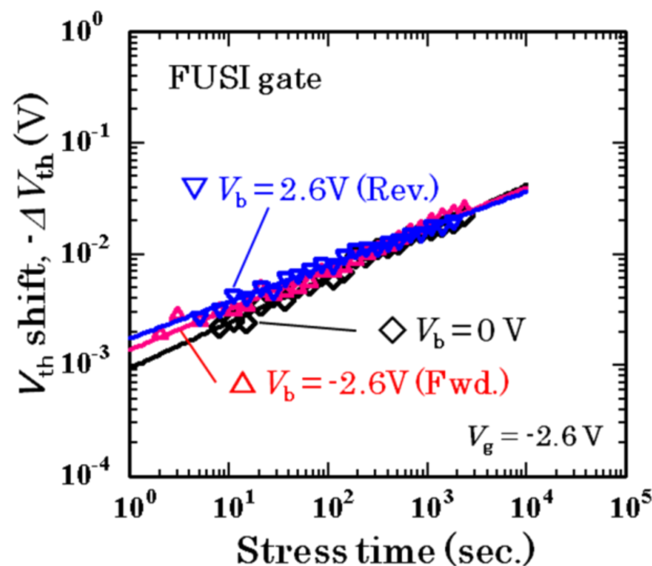


Fig. 5.12 Dependency of NBTI characteristics on back-bias (V_b)

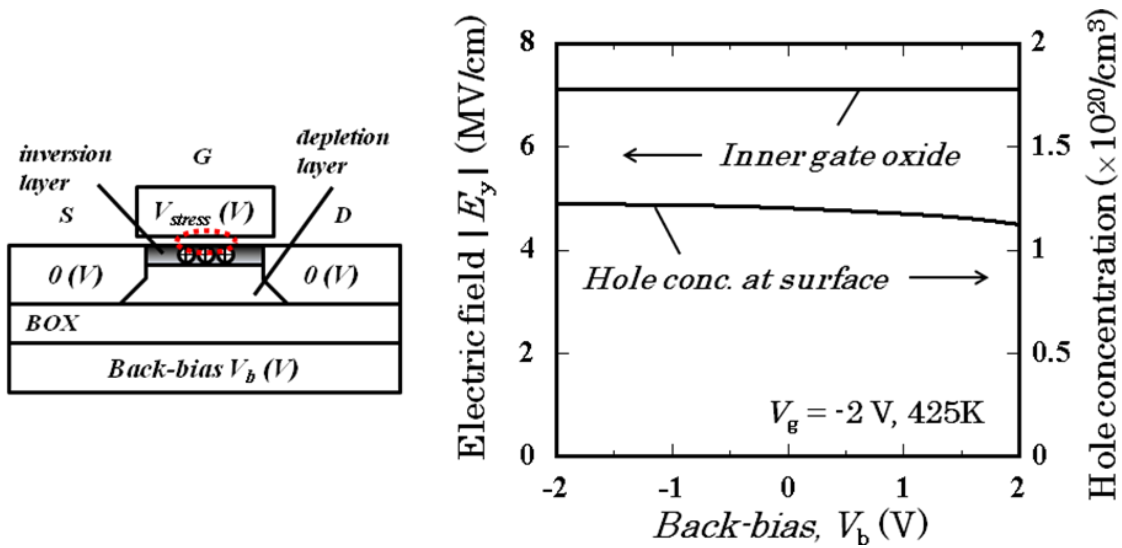


Fig. 5.13 Simulated vertical electric-field strength (E_y) and hole concentration under the gate as a function of back-bias (V_b) under NBTI stress

5.7 Conclusion

Effects of device structure and wide-range back-biasing on HCI and NBTI in SOTB CMOSFETs were studied. It is shown that HCI degradation in a NMOSFET is mainly caused by channel hot electron (CHE) injection generating interface traps, which is the same mechanism as that in a conventional bulk device. However, the lifetime of a SOTB device is longer than that of a bulk one because of a suppressed lateral electric field at the drain edge (due to no halo implant). It was found that the mechanism of interface trap generation changes to electron trapping under reverse back-biasing because of enhanced vertical electric field at drain edge, but the worst-case HCI degradation occurs in forward back-biasing because of increased drive current. The NBTI degradation in the SOTB PMOSFET can be explained by the conventional reaction-diffusion model. The long NBTI lifetime was confirmed because of low surface E_y and no halo implant. In

addition, it was demonstrated that the back-biasing has a small impact on the NBTI degradation because of the screening effect of the inversion layer. These results indicate the superior features of SOTB technology in terms of reliability, even under a high level of performance boosting (i.e., back-biasing).

5.8 References

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Chapter. 6 MIPS Gate Structure for SOTB CMOSFET

Abstract

A poly-Si/TiN/SiON gate stack for SOTB CMOSFET is studied. The flat-band voltage (V_{fb}) shift of the gate stack for the threshold voltage (V_{th}) symmetry of SOTB CMOSFETs is investigated. It was found that the V_{fb} shift depended on both TiN thickness and thermal load. Thicker TiN above 15 nm is preferable for obtaining the midgap value of V_{fb} with considering the thermal budget of the SOTB process. The gate stack was integrated into SOTB CMOSFETs, which showed that the V_{th} roll-off characteristics corresponded to the proper control of the effective work function by considering how the impurity-related work function modulation affects. Narrow channel characteristics of the TiN-gate SOTB CMOSFETs are also shown to be superior to fully silicided gate SOTB devices due to less silicidation.

Chapter.6 MIPS Gate Structure for SOTB CMOSFET

Contents

6.1 Introduction
6.2 Investigation of flat-band voltages in poly-Si/TiN/SiON gate stacks
6.3 Integration of poly-Si/TiN/SiON gate stack into SOTB CMOSFETs
6.4 Conclusion
6.5 References

6.1 Introduction

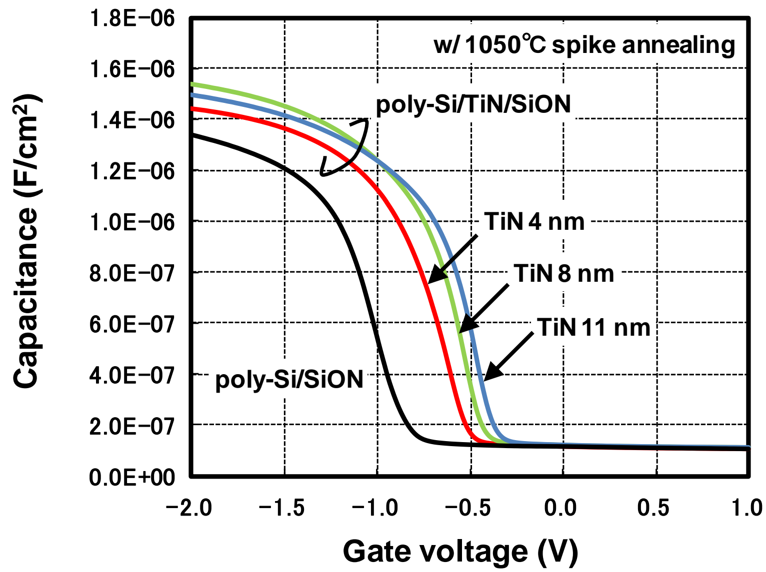
In FDSOI CMOSFETs with an undoped channel, a single midgap metal gate electrode is preferable for easily obtaining symmetrical V_{th} values between NMOS and PMOS. A metal gate also solves problems such as gate depletion and boron penetration in conventional poly-Si gates [6.1]. Nickel silicide (NiSi) is one such metal gate candidate. It is widely used to decrease the source/drain resistance (R_{sd}) at the contact region in the conventional bulk process. A fully silicided (FUSI) gate process for SOTB CMOSFETs was already described, in which the gate poly-Si and source/drain epitaxial Si were silicided simultaneously. However, this FUSI process was found to have a narrow process window. On the one hand the gate electrode should be completely silicided to control the work function, and on the other hand the silicon layer in the source-drain region should not be completely silicided to reduce access resistance [6.2]. In the narrow channels, especially, on-current (I_{on}) degradation due to excess silicidation in the source/drain region was observed.

An alternative candidate of the midgap metal gate electrode to FUSI is titanium nitride (TiN). A metal-inserted poly-Si stack (MIPS) using TiN, such as poly-Si/TiN/HfO_2 gate, with FDSOI CMOSFETs obtained symmetrical V_{th} [6.3]. However, the high-κ dielectrics are well known to cause some problems such as Fermi level pinning or degradation in mobility [6.4]. In this chapter, a reliable poly-Si/TiN/SiON gate stack for SOTB CMOSFETs was studied. The conventional SiON gate dielectric was used because high-κ technology is not necessary for the target applications; low-standby-power applications with equivalent oxide thickness (EOT) around 2 nm. The flat-band-voltage- (V_{fb}-) shift behavior of the gate stack was thoroughly investigated to adjust V_{th}, considering the thermal budget of the SOTB process. The SOTB CMOSFETs with the TiN gate stack was also fabricated and compared the characteristics between the TiN, FUSI, and poly-Si gate stacks.

6.2 Investigation of flat-band voltages in poly-Si/TiN/SiON gate stacks

The poly-Si/TiN/SiON gate stacks were investigated using NMOS capacitors fabricated on p-type bulk Si substrates. The processes of the samples were as follows. Local oxidation of silicon (LOCOS) was formed to define the active region. The SiON gate dielectric was thermally grown and the CVD-TiN film was deposited at 600°C followed by deposition of phosphorous (P)-doped n+ poly-Si. Subsequently, the gate stacks were patterned by dry-etching. Finally, spike annealing at 1050°C and additional annealing (in some samples) were carried out. Capacitance-voltage (*C-V*) characteristics were measured at 1 MHz and V_{fb} and EOT were extracted [6.5].

The dependencies of the *C-V* characteristics on the TiN thicknesses and thermal load are shown in Figs. 6.1 (a) and (b), respectively. The V_{fb} and EOT extracted from the *C-V* data are shown in Fig. 6.2. The n+ poly-Si/SiON gate stack with spike annealing at 1050°C as a control had a V_{fb} of -0.84 V and EOT of 1.98 nm. It was found that the V_{fb} value shifted toward the midgap (around -0.3 V) along with increasing TiN thickness and reached -0.4 V at a TiN thickness of 11 nm (Fig. 6.2 (a)) and the EOT values remained constant around 2 nm. Furthermore, the poly-Si/TiN (8 nm)/SiON gate stack without annealing showed a V_{fb} of -0.22 V and EOT of 1.95 nm (Fig. 6.2 (b)). The V_{fb} value of the gate stack was thus found to decrease as thermal load increased.



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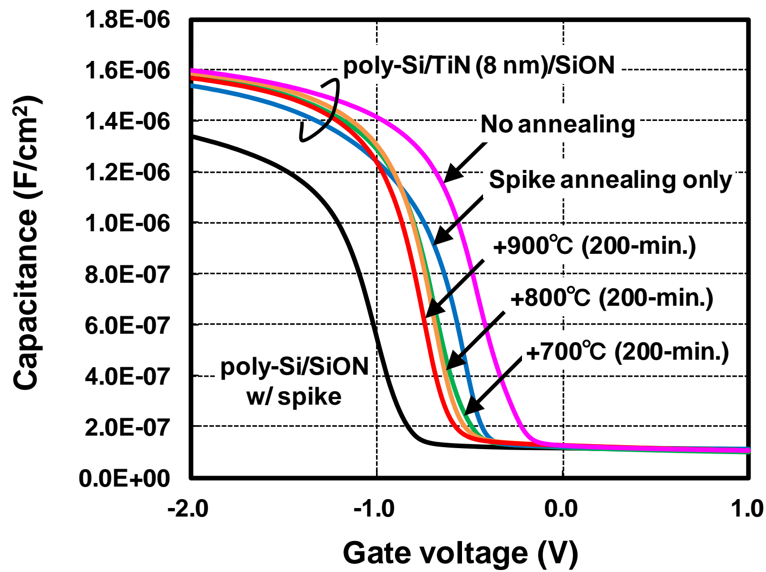
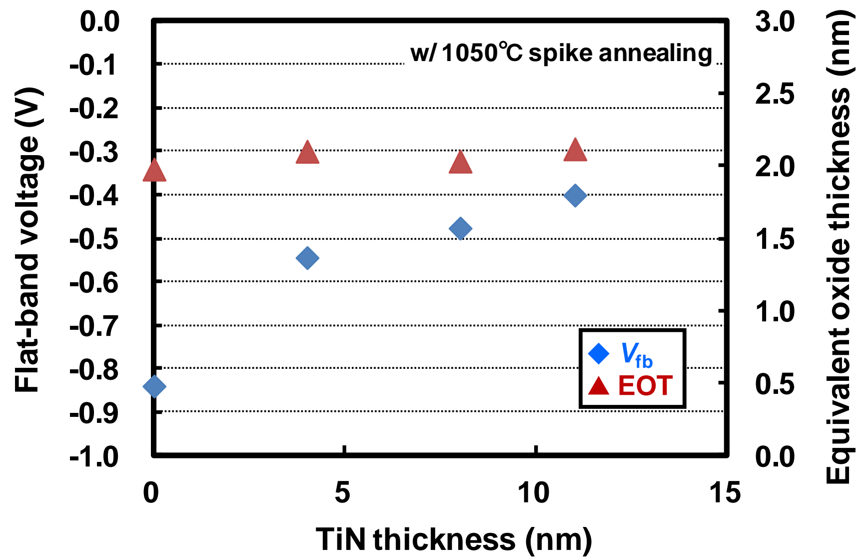


(b)

Fig. 6.1 *C-V* characteristics of NMOS capacitors with poly-Si/TiN/SiON gate stacks. (a) Dependencies on TiN thicknesses and (b) on thermal loads



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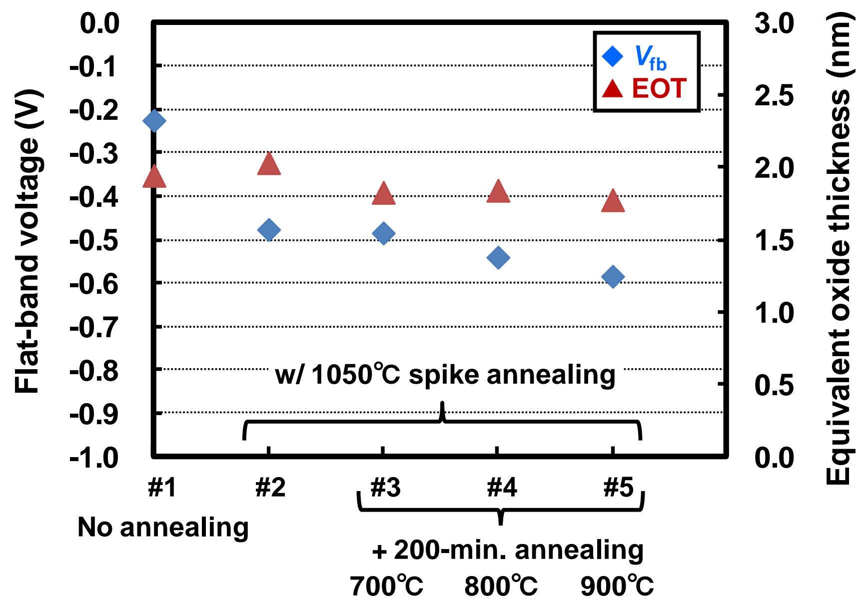
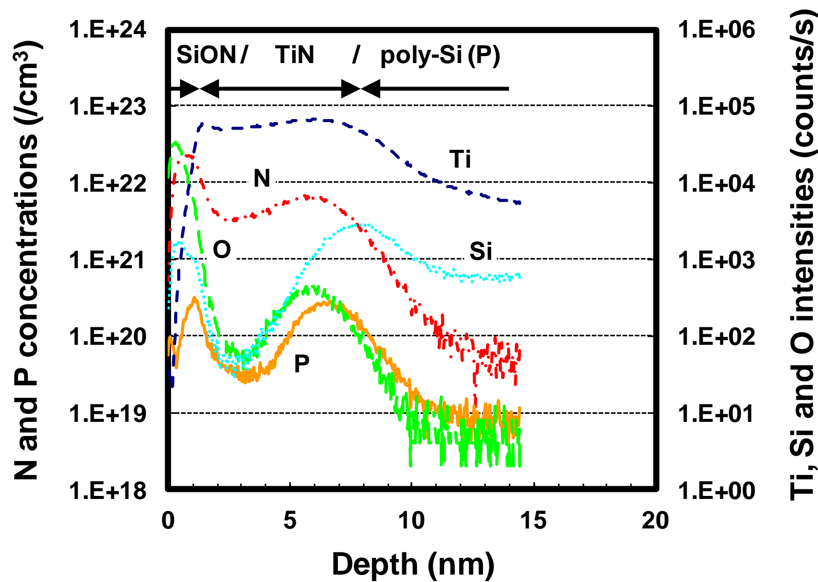


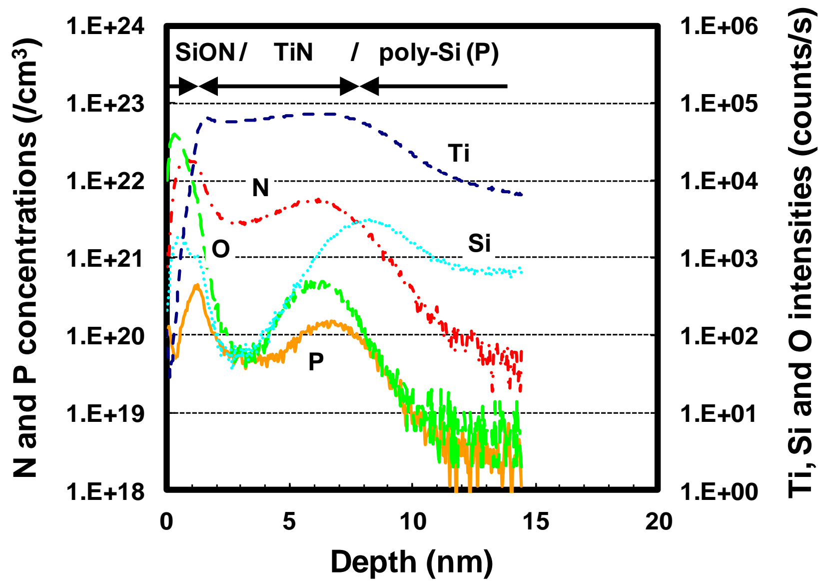
(b)

Fig. 6.2 Extracted V_{fb} and EOT of Fig. 2. (a) Dependencies on TiN thicknesses and (b) on thermal loads

Secondary ion mass spectrometry (SIMS) was conducted for investigating the V_{fb} shift. Figures 6.3 (a), (b), and (c) show SIMS profiles of the (a) poly-Si/TiN (8 nm)/SiON stack with 1050°C spike annealing, (b) the poly-Si/TiN (8 nm)/SiON stack with 1050°C spike annealing and 900°C 200-min. annealing, and (c) the poly-Si/TiN (11 nm)/SiON stack with 1050°C spike annealing. SIMS was conducted from the backside of the substrate to obtain an accurate profile of the sample surface. The tail of the Ti profile in the poly-Si was inaccurate for this measurement technique because of the knock-on effect. The peaks of Si, O, and N at the poly-Si/TiN interface were also inaccurate quantitative values due to the matrix effect. Careful comparison of Figs. 6.3 (a) and (b) shows almost the same profiles of Ti, N, Si and O, except P. The P concentration of the gate stack with additional 900°C 200-min. annealing (Fig. 6.3 (b)) was found to increase at the TiN/SiON interface. It was presumed that the P of the doped poly-Si diffused into TiN and piled up at the TiN/SiON interface during annealing. Comparison of Figs. 6.3 (a) and (c) also shows the same profiles of Ti, N. Si, and O at the SiON/TiN interface. The P concentration of the gate stack with TiN (11 nm) (Fig. 6.3 (c)) at the TiN/SiON interface drastically reduced. The diffusion of P into TiN from the poly-Si was assumed to be suppressed by increasing the TiN film thickness.



(a)



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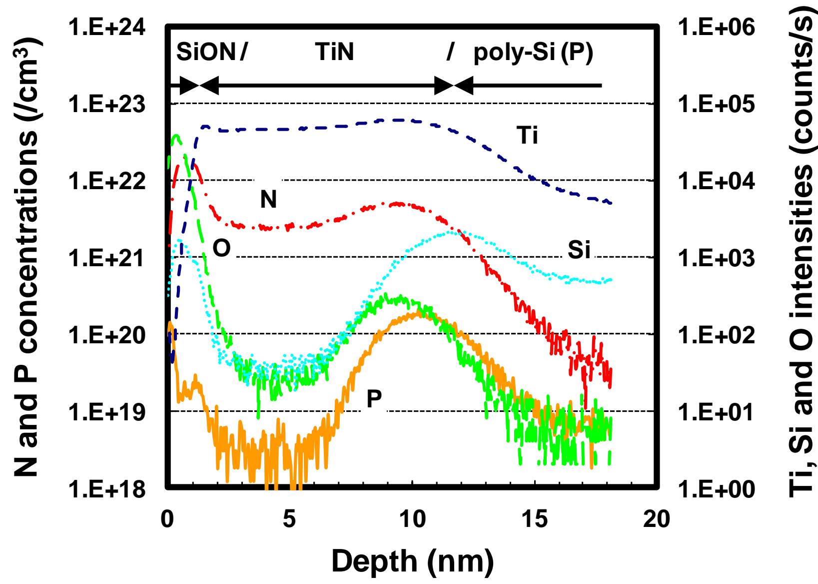

(c)

Fig. 6.3 Backside secondary ion mass spectrometry (SIMS) profiles. (a) Poly-Si/TiN (8 nm)/SiON stack with 1050°C spike annealing, (b) poly-Si/TiN (8 nm)/SiON stack with 1050°C spike annealing and 900°C 200-min.

annealing, and (c) poly-Si/TiN (11 nm)/SiON stack with 1050°C spike annealing. Note that profiles are drawn from bottom of gate dielectric film into gate electrode

The mechanisms of the V_{fb} shift in the TiN gate stacks have been extensively reported [6.6]-[6.10]. Sakashita et al. reported that Si diffused into the CVD-TiN/high-κ interface and the Fermi level might be pinned at the midgap of Si [6.6]. However, in the present experiments, Si diffusion was not observed and high-κ dielectric was not used. Kadoshima et al. reported that very thin TiO_x at the TiN/SiO_2 interface was likely formed and modulated the work function [6.7]. In the present experiments, the increase in O at the TiN/SiO_2 interface was not observed and the EOT did not increase with an increase in the thermal load. Singanamalla et al. reported that aluminum (Al) implantation into TiN/SiO_2 modulated the effective work function (EWF) [6.8]. The presence of Al at the interface could result in additional dipole formation (Al-O-Si), resulting in electron transfer from Al due to the lower electronegativity with respect to Si and O. This could lead to a barrier-height increase resulting in an increase in the EWF. In the present experiments, the presence of P at the interface corresponded with the V_{fb} shifts. The Pauling electronegativity values for P, Al, O, and Si are around 2.1, 1.6, 3.4, and 1.9, respectively. Hence, the same mechanism as a case of Al at the interface is inferable in the present case. Other causes for the V_{fb} shifts could be TiN film stress or dielectric charge. Vitale et al. reported that the increase in positive charge along with increase in TiN thickness could be due to additional gate dielectric damage during longer sputtering time in PVD-TiN films [6.11]. For integrating the gate stack into SOTB CMOSFETs to adjust V_{th}, the present results indicate that thicker TiN film and lower thermal load are preferable.

6.3 Integration of poly-Si/TiN/SiON gate stack into SOTB CMOSFETs

The poly-Si/TiN/SiON gate stack mentioned above was integrated into SOTB CMOSFETs. The process flow of SOTB CMOSFETs with FUSI gates

is described in chapter 2. The device structure is as follows. The thicknesses of the SOI and BOX layers are 13 and 10 nm, respectively. The impurity concentration of the channel is less than 1x10^{17} /cm^3 without halo implantation. The differences between the FUSI-gate and TiN-gate SOTB CMOSFETs are summarized in Table 6.1. The thicknesses of source/drain epitaxial Si and Ni silicide in the TiN-gate devices decreased to 30 and 20 nm (from 60 and 50 nm), respectively. The process temperatures decreased below 600°C, except for the 800°C epitaxial silicon process and activation annealing. Figure 6.4 shows a cross-sectional transmission electron microscope (TEM) image of the TiN-gate SOTB transistor.

Table 6.1 Process conditions for each device

	Process			
Device	SOTB			Conv. bulk
Gate	FUSI	TiN	Poly-Si	Poly-Si
Gate dielectric	SiON			
Gate poly-Si	P doped (before silicidation)	P doped	P imp. for NMOS B imp. for PMOS	P imp. for NMOS B imp. for PMOS
Si epi (S/D)	60 nm	30 nm (above TiN)	30 nm	-
NiSi	50 nm	20 nm	20 nm	20 nm
Channel immpurity	$< 1x10^{17}$ /cm^3	$< 1x10^{17}$ /cm^3	$< 1x10^{17}$ /cm^3	$> 1x10^{18}$ /cm^3 with halo

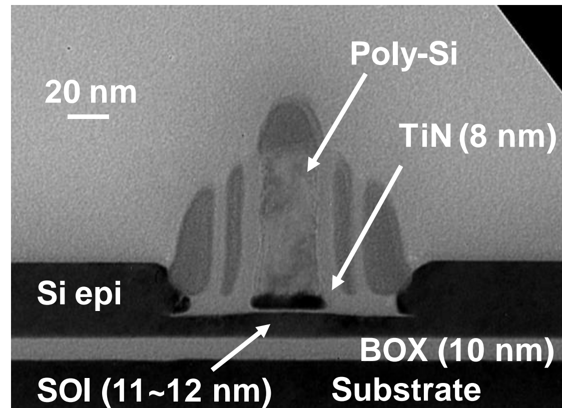

Fig. 6.4 Cross-sectional transmission-electron-microscope (TEM) image of TiN-gate SOTB transistor before silicidation. TiN thickness was 8 nm and gate dielectric was SiON

The dependency of the V_{th} roll-off characteristics on TiN thickness is shown in Fig. 6.5. The V_{th} roll-off of the poly-Si gate SOTB CMOSFETs is also plotted. The worse V_{th} roll-off of PMOS compared with that of NMOS was due to larger gate overlap length because boron (B) in the extension region of PMOS had a larger diffusion coefficient than arsenic (As) in NMOS and diffused into the channel during annealing. The V_{th} symmetry between NMOS and PMOS improves with increase in TiN thickness, which is in accordance with the EWF results of gate stacks. This linear relationship between the V_{th} symmetry and TiN thickness indicates that a TiN thickness around 15 nm or thicker is required for this symmetry.

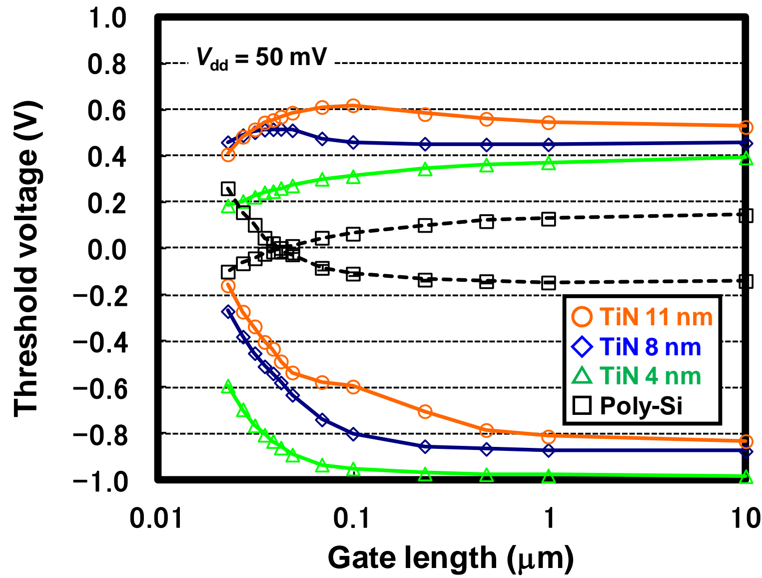

Fig. 6.5 Dependency of V_{th} roll-off characteristics on TiN thickness in TiN-gate SOTB CMOSFETs. V_{th} values were extracted by extrapolating I_d - V_g curve at V_{ds} = 50 mV. Characteristics of poly-Si-gate SOTB devices are also plotted.

Figure 6.6 compares narrow-channel characteristics between TiN-gate and FUSI-gate PMOSFETs. It is found that the on-current decreases in the FUSI-gate PMOS at the narrow-channel region, though the V_{th} characteristics are constant. The origins of the narrow-channel effects were reported as the transient enhanced diffusion (TED) of channel impurity [6.10] or the fringing of the electric field at the STI edge [6.11]. SOTB devices do not have these origins because of the undoped channel and the small bird's beak at the STI edge, resulting in no degradation of V_{th} characteristics (not shown). Figure 6.7 shows a TEM image of the source/drain region (parallel to the gate electrode) in the FUSI-gate SOTB PMOS. It was found that the NiSi encroached from the side of the raised source/drain into the SOI layer. This is because the epitaxial raised source/drain has a faceting structure and Ni-Si reaction also occurs on the side slope of the silicon epitaxial layer. Hence, the high raised source/drain could not solve the

problem in which the NiSi touches the BOX layer. If the silicide fully consumes the SOI layer, the parasitic series resistance increases significantly because the horizontal portion directly underneath the NiSi is no longer available for contact [6.2]. Figure 6.8 shows schematic cross-sectional views of source/drain structure with excess silicidation. In the case of wide channel (Fig. 6.8 (a)), the contact resistance with SOI and NiSi, R_c is not dominant in the parasitic series resistance due to the large contact area. In the case of narrow channel with excess silicidation (Fig. 6.8 (b)), the contact area reduces significantly and the parasitic series resistance increases drastically. Therefore, the on-current of the FUSI-gate SOTB device decreases in narrow channel. On the other hand, there was no degradation in the drain current for narrow channel in the TiN-gate SOTB PMOS due to the reduced NiSi thickness (20 nm). Note that the difference in the absolute value of the on-current between the FUSI-gate and TiN-gate devices was due to the higher V_{th} of the TiN-gate SOTB PMOS (Fig. 6.5) and not related to the intrinsic device structure.

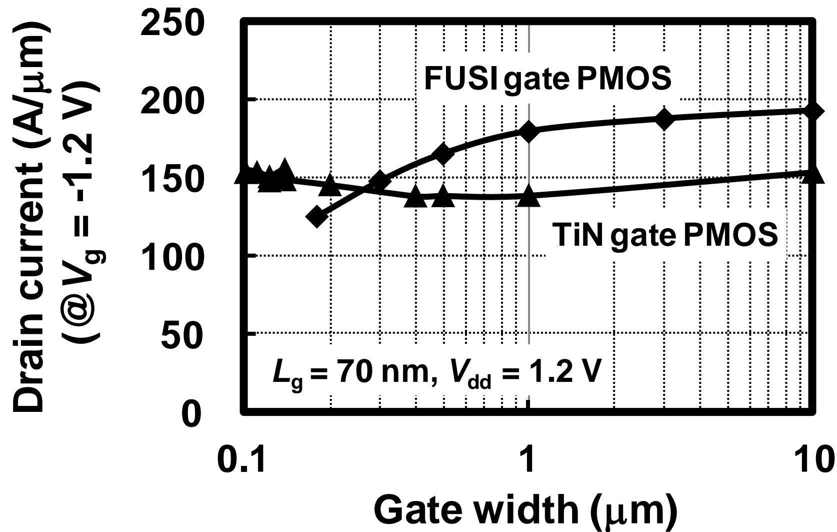

Fig. 6.6 Comparison of narrow-channel characteristics between TiN-gate and FUSI-gate SOTB PMOSFETs. Gate lengths (L_g) were around 70 nm and on-currents (I_{on}) were at V_{dd} = 1.2 V.

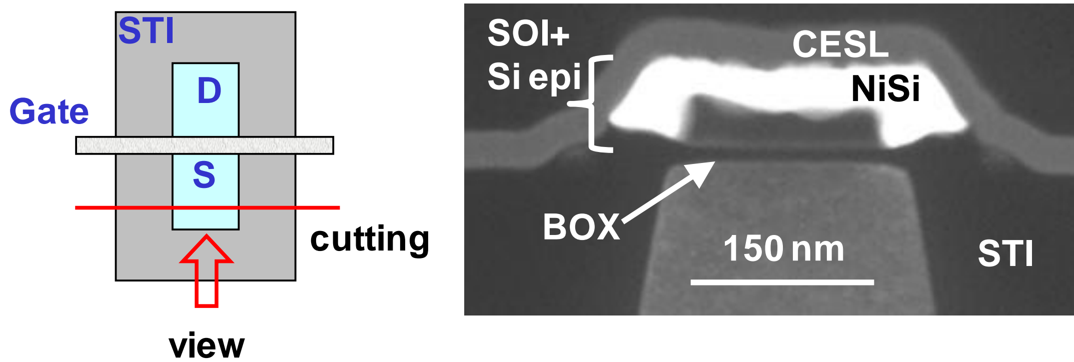

Fig. 6.7 TEM image of source/drain region (parallel to gate electrode) in FUSI-gate SOTB PMOS.

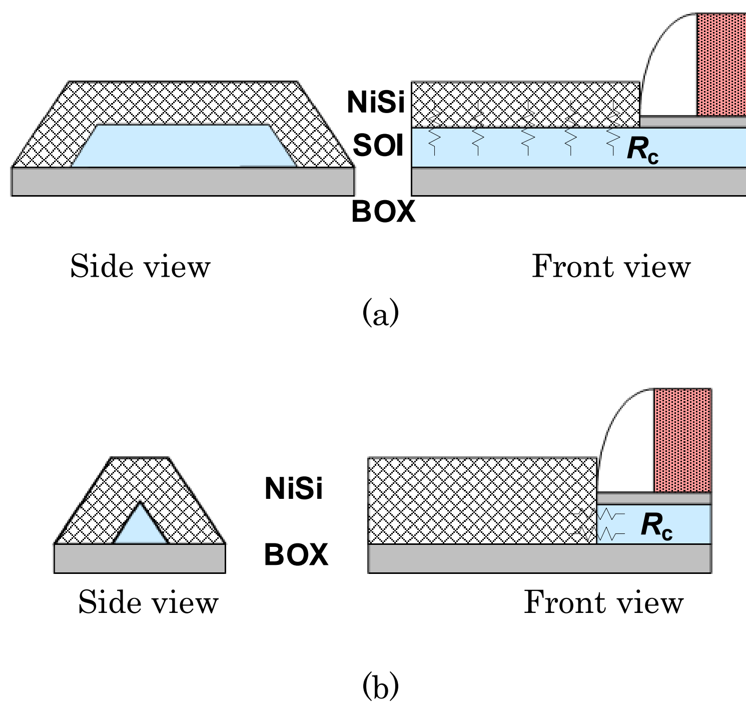

Fig. 6.8 Schematic cross-sectional view of SOTB structure with silicided source/drains. (a) wide channel (b) narrow channel

6.4 Conclusion

A poly-Si/TiN/SiON gate stack was investigated and integrated it into SOTB CMOSFETs. The V_{fb} shift was studied to obtain the desired V_{th} of the SOTB CMOSFETs. It was found that V_{fb} shifted toward the midgap direction along with the increase in the TiN thickness and decrease in the thermal load. Diffusion of P from poly-Si into the TiN/SiON interface was confirmed using backside SIMS analysis. Over 15 nm of TiN thickness, considering the thermal budget of the SOTB process, is preferable for achieving V_{th} symmetry between the SOTB NMOS and PMOS. Furthermore, the serious problem of I_{on} degradation of FUSI-gate SOTB devices in the narrow channels was observed. This is because the increased parasitic series resistance due to excess silicidation in the source/drain region. The high raised source/drain structure could not solve the problem because of the faceting structure of the epitaxial Si. The TiN-gate SOTB CMOSFETs have no degradation of on-current in narrow channel due to less silicidation. This improvement can enhance the applicability of SOTB technology for the integration of scaled device generation.

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Chapter. 7 Summary and Conclusions

Chapter.7 Summary and Conclusions

Contents

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7.1 Summary

In this thesis, various problems related to SOTB CMOSFET described in chapter 1 are investigated and solutions to those problems are proposed in order to achieve high performance, low power, and highly reliable LSIs. In chapter 7, the studies referred to in this thesis are summarized and their importance is described.

In chapter 2, realization and characterization of SOTB CMOSFET in 65-nm generation was described. The device fabrication process, that is, a simple FUSI gate and high raised S/D for the desirable V_{th} and low R_{sd}, was developed. The superior I_{on}/I_{off} and suppressed SCE to those of conventional planar bulk CMOSFET for LSTP were successfully obtained. In addition, the low V_{th} variation was also achieved and the wide-range back-biasing was presented for the first time.

In chapter 3, reduction of power consumption by using SOTB technology was described. A SOTB CMOSFET with an ultralow off-current below 1 pA/μm was developed by reducing GIDL. It was clarified what extent the low variability of SOTB CMOSFET could impact on the power consumption. In addition, it was also shown that both the ultralow off-current and its small variation drastically reduced the standby power below 10% in comparison with the one of conventional bulk CMOSFETs.

In chapter 4, novel hybrid integration of SOTB and bulk CMOSFETs was presented. The simple process flow suppressed the height difference between SOTB and bulk regions and could fabricate them at the same time. It was also shown that the process caused no damage to the exposed substrate. In addition, the quality of the gate dielectric of the hybrid bulk device was confirmed as the same with the conventional ones by evaluating the mobility, D_{it}, and TDDB. It was also shown that the characteristics of the integrated hybrid bulk CMOSFETs were comparable to those of conventional bulk CMOSFETs.

In chapter 5, HCI and NBTI reliability of SOTB CMOSFET was described.

It was shown that HCI degradation in a NMOSFET was mainly caused by channel hot electron (CHE) injection generating interface traps, which was the same mechanism as that in a conventional bulk device. However, the lifetime of a SOTB device is longer than that of a bulk one because of a suppressed lateral electric field at the drain edge (due to no halo implant). It was found that the mechanism of interface trap generation changes to electron trapping under reverse back-biasing because of enhanced vertical electric field at drain edge, but the worst-case HCI degradation occurs in forward back-biasing because of increased drive current. The NBTI degradation in the SOTB PMOSFET was found to be explained by the conventional reaction-diffusion model. The long NBTI lifetime was confirmed because of low surface E_y and no halo implant. In addition, it was demonstrated that the back-biasing had a small impact on the NBTI degradation because of the screening effect of the inversion layer.

In chapter 6, MIPS gate structure for SOTB CMOSFET was described. The poly-Si/TiN/SiON gate stack was investigated and integrated it into SOTB CMOSFETs. It was found that V_{fb} shifted toward the midgap direction along with the increase in the TiN thickness and decrease in the thermal load. Diffusion of P from poly-Si into the TiN/SiON interface was confirmed by using backside SIMS analysis. Over 15 nm of TiN thickness, considering the thermal budget of the SOTB process, is preferable for achieving V_{th} symmetry between the SOTB NMOS and PMOS. Furthermore, the serious problem of I_{on} degradation of FUSI-gate SOTB devices in the narrow channels was observed. This is because the increased parasitic series resistance due to excess silicidation in the source/drain region. The TiN-gate SOTB CMOSFETs have no degradation of on-current in narrow channel due to the less silicidation.

7.2 Conclusions

In this thesis, it have been experimentally demonstrated that SOTB CMOSFET has superior characteristics, compatible design capability, and

higher reliability in comparison with planar bulk CMOSFET in 65-nm generation. Though the advanced planar bulk CMOSFET has downsized to 28-nm generation in these days, the older generations are in mass production now. Because SOTB CMOSFET has comparable interfaces with the conventional bulk CMOSFETs, such as multi V_{th}, bulk I/O CMOSFETs, and the same layout, it could be easily represented without design changes. If would be so, both operating voltage and standby power can be substantially reduced due to the low variability of the SOTB CMOSFET as described in this thesis. Moreover, when combined with the V_{bb} control of SOTB CMOSFET, it is possible to obtain the optimum power efficiency by flexibly changing V_{dd} and V_{th} to the operation situation. It is hoped that these flexible voltage controls will be applied to VLSI circuits in the future to meet the increasingly complex application demands.

Recently, the scalability of CMOSFETs has become a topic of utmost importance. In SOTB technology, scalability can be pursued by reducing the SOI and BOX thicknesses. The minimum SOI thickness is considered to be 6 nm, after which the influence of the quantum effect or mobility degradation appears [7.1]. Given this value and considering the thickness variation, the minimum gate length of the SOTB CMOSFET is expected to be below 20 nm while maintaining a small V_{th} variation [7.2]. In addition, the applicability of back-gate biasing is important. Even if the uniformity of transistors is not maintained, the characteristic variation can be eased by correcting V_{bb} as described in this thesis. Though FinFET is starting to be adopted in 22-nm generation for high performance applications [7.3], the inherent problems such as multi V_{th} and back-biasing capabilities remain very difficult. This means that the adaptive and flexible control cannot be used and the power crisis would rise again in near future. On the other hand, some approaches for back-biasing in FinFETs have been reported [7.4], [7.5]. Although they require complex processes or SOI wafer, the effectiveness of back-biasing was confirmed. In addition, though FinFETs have superior subthreshold slope than SOTB CMOSFETs, some variation causes such as line edge roughness have larger influence in advanced technology nodes. Hence, SOTB devices have the smallest variability in comparison with conventional bulk CMOSFETs and FinFETs [7.6]. These features indicate that SOTB CMOSFETs are suitable for low power applications.

The remained subjects for utilization of SOTB CMOSFET would be large scale integration and circuit techniques to use the SOTB technology. For the early migration to new device architecture like SOTB from the conventional one, design compatibility with the existing circuit technology is very important. Moreover, circuit-device interaction in the circuit design stage is also important to fully take advantage of the features of the SOTB, for example, effective use of back-biasing. Figures 7.1 and 7.2 show a design environment and a standard cell layout of SOTB technology, respectively. The design flow for the hybrid SOTB/bulk technology is basically the same as the conventional one. The essential parts are considered to be standard-cell layout, SPICE characterization, and timing analysis. The standard-cell library of smaller area and higher back-bias-voltage stability is essential for the competitive IC design. Precise characterization of timing and power is also important. The implementation of a new SPICE model that is fully compatible with FD-SOI and the back-biasing is desired. Also, static timing analysis including the local and global variability is a core of the circuit design with maximum power efficiency.

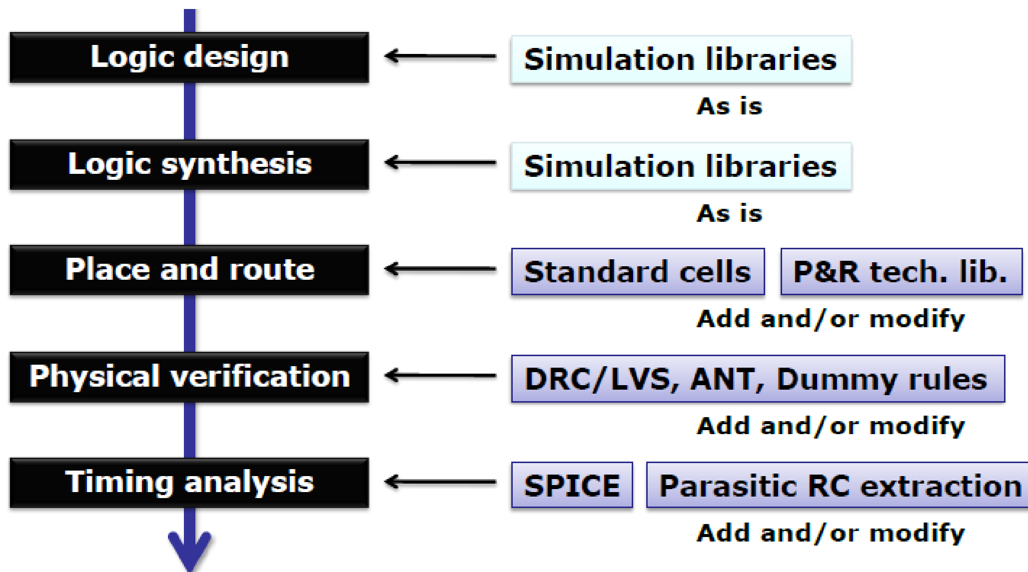

Fig. 7.1 Design environment of SOTB technology for large scale integration

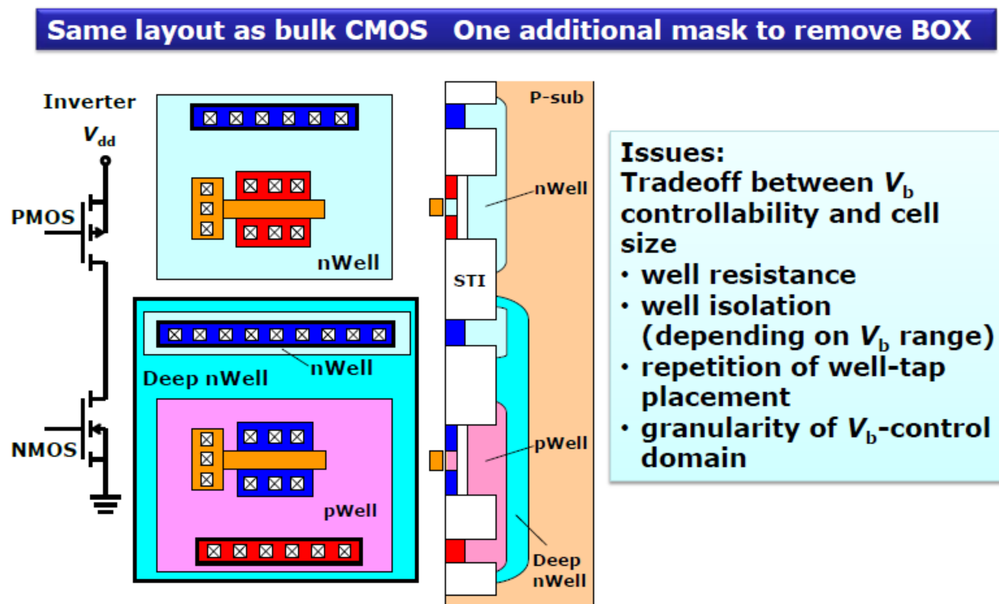

Fig. 7.2 A standard cell layout of SOTB

Studies for these subjects are now carried on into low-power electronics association & project (LEAP) [7.7]. Further V_{dd} reduction to 0.4-V (ideal minimum power per operation) is aimed in the project. With decreasing V_{dd} below 0.4 V, operation frequency f significantly decreases and the leakage power component relatively increases. In SOTB technology, the adaptive back-bias technique is useful to control the power efficiency more flexibly by changing not only V_{dd} but also V_{th}. With this technique, the power per operation can be decreased with low V_{dd} satisfying the speed requirement.

On the other hand, the SOTB technology would be starting to launch at 28-nm generation in Europe [7.8]. The author looks forward to the further progress of this FD-SOI technology and hopes this study would help it.

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