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Study on Metal/Insulator and Metal/Semiconductor Ultra-Fine Tunneling Field Effect Transistors

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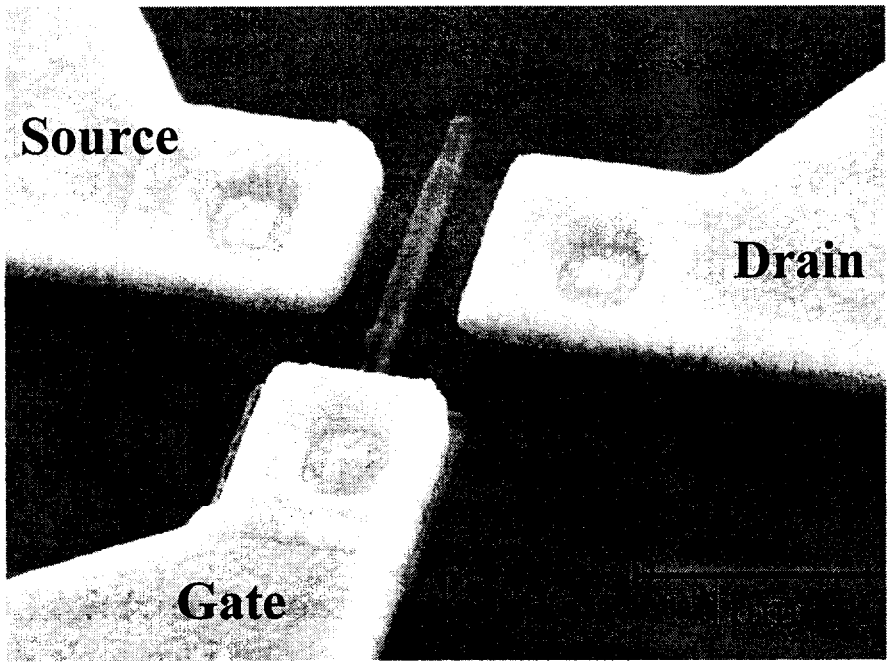
Schottky Source/Drain MOSFET



Contents

Chapter 1

Introduction

1.1 Introduction

Are you happy? If large scale integrated circuits (LSI) suddenly disappear in your life, it must be inconvenience to you, and your answer to the first question may be "No". The transistor was invented 50 years ago [1]. After this invention, electrical circuits changed from using vacuum tubes to using transistors. LSI, which are the major products of the semiconductor industry were born. Elevation of LSI capability and shrinkage of the cost have been realized by the many developments in semiconductor manufacturing technology. As a result, the market for LSI was not only in calculating computers, but also in home electrical goods, including the micro-computer.

The development of LSI has gone hand in hand with the development of the metal-oxide-semiconductor field-effect transistor (MOSFET), because LSI is principally constructed from MOSFETs.

The insulated gate field effect transistor (IG-FET), which is an antecedent of the MOSFET, was proposed in 1930 [2]. The fieldistor, in which current through a p-n junction at the surface was controlled by the gate voltage across a vacuum gate insulator was demonstrated in 1952 [3]. The interfacial traps at the insulator/semiconductor interface were problematic for the operating stability of the IG-FET, because the

device current flows at the interface. However, the IG-FET was a very attractive device for LSI due to the planar structure and the high input impedance. In the 1960s, IG-FETs with a silicon dioxide film were demonstrated [4, 5]. These reports showed that the silicon/silicon dioxide interface was very stable. Since then, a great deal of research interest has focussed on the development of the MOSFET.

Dennard et. al have reported on the scaling-rules for MOSFETs, and have shown that the capability of MOSFETs can be increased by scaling-down the device size [6]. As MOSFETs have been scaled down by scaling-rules, the number of transistors in LSI has increased. At present, 0.25 μm-long gate MOSFETs are used in mass-produced LSIs. In the research field, 40 nm-long gate MOSFETs with doped source/drains (S/Ds) have been demonstrated [7, 8]. In addition, operation of a 14 nm-long gate MOSFET with electrically generated S/Ds has been reported [9, 10]. For high-speed operation, sub 10 ps gate delay with sub 0.1 μm-long gate complementary MOS logic has been reported [11, 12].

Many novel technologies have been developed for scaling-down the MOSFET using scaling-rules, and have broken through the limits of scaling. Figure 1. 1 shows the progress of the MOSFET gate length in the research field. If the MOSFET is scaled down at the present rate, 10 nm-long gates will be realized in 2002. However, serious limits to scaling are found. Two serious limits are as follows. At 20 nm-long gates, a limit to the fabrication process is encountered [13], and at 10 nm-long gates, there is a physical limit to device operation due to quantum effects in the devices, because the device size becomes equal to the electron wave length in Si.

This paper describes a study on metal/semiconductor and

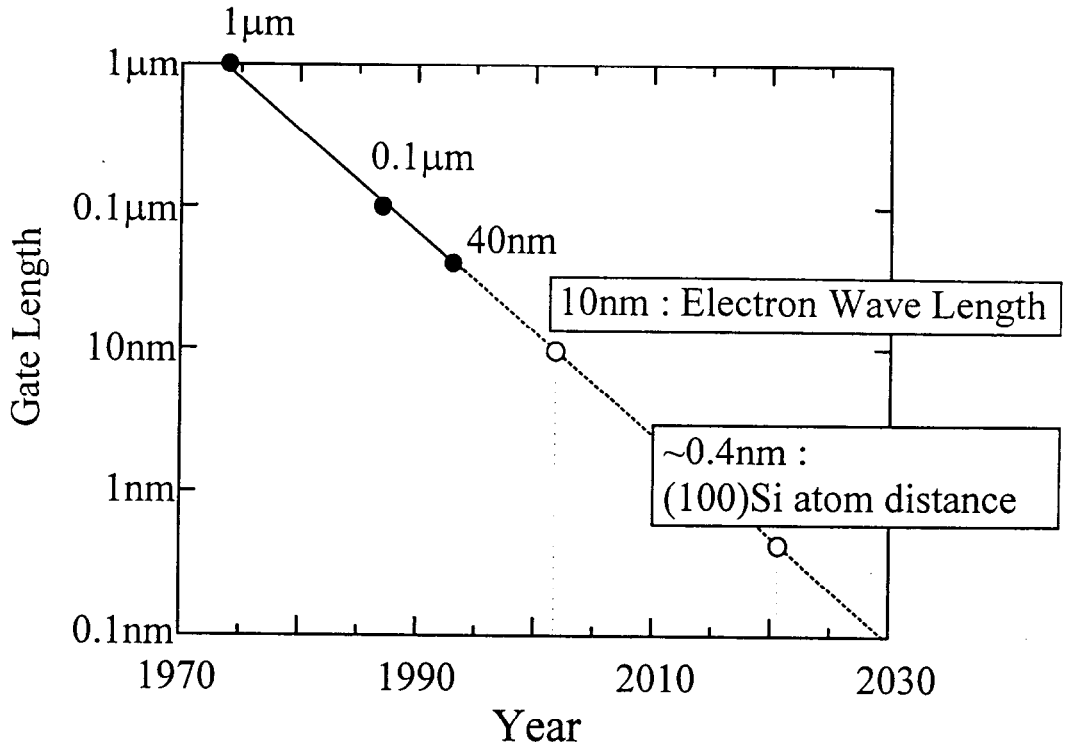


Figure 1.1: Progress of MOSFET's gate length.

metal/insulator tunneling field effect transistors to be used as ultra-fine elements in LSI in the same way as MOSFETs. These devices can break through the limits of MOSFETs.

1.2 Nanometer-size Electron Device

1.2.1 The Limits of MOSFET Scaling

In this section, the limiting size of the MOSFET and the cause of these limits are described. Short channel effects, such as threshold voltage shift and increasing subthreshold swing can be suppressed by scaling down using scaling-rules. However, the limits of the fabrication process and the physical limit of device operation appear, if the device size is scaled using scaling-rules. Figure 1. 2 shows the estimated minimum size of the MOSFET considering the limit of the fabrication process [13]. In this

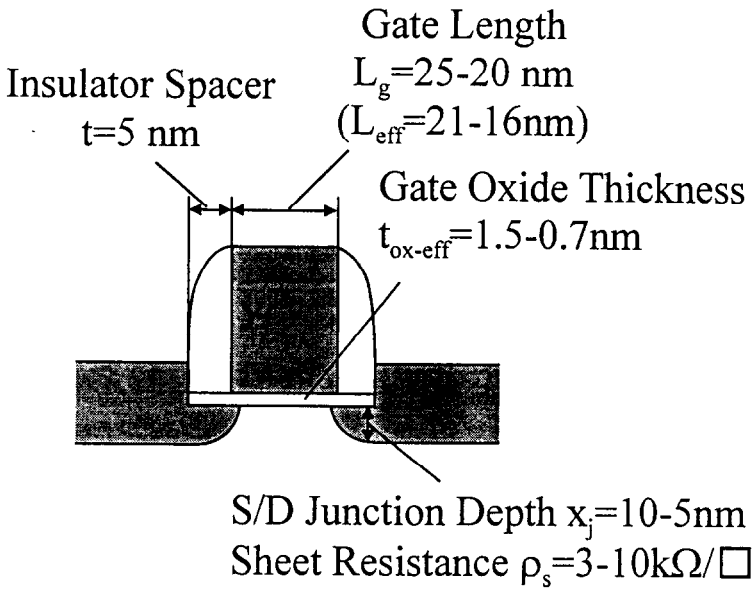


Figure 1.2: Ultimate size of the MOSFET considering the limits of the fabrication process.

estimation, the gate length is 20–25 nm and the effective channel length is 16–21 nm. These values are determined by the gate oxide thickness and the S/D junction depth. As limits, the gate oxide thickness is 0.7–1.5 nm, the S/D junction depth is 5–10 nm, and the S/D sheet resistance 3–10kΩ/□ [13].

These limiting values are determined as follows. Previously in scaling-down, the gate oxide thickness for 100 nm-long gate MOSFETs was 3–4 nm. Continuation of this scaling gives a gate oxide thickness of 1–2 nm for 40 nm-long gate devices. At 1–2 nm-thick oxides, the gate leakage current increases due to tunneling from the channel to the gate. Therefore the dynamic power dissipation increases, although the device can still be operated. Device operation of the MOSFET with a 1.5 nm-thick gate oxide has been reported [14]. Recently reliability of 1.5–2 nm-thick gate oxides has been discussed [15]–[17]. As a result, the increasing dynamic power dissipation can not be suppressed, even though the transconduc-

tance increases. To reduce dynamic power dissipation, the supply voltage must be low, because the gate leakage depends upon the electric field in the device. The limit of the gate oxide thickness depends on the tunneling leakage, although ultra-thin oxides can be grown using conventional processes, such as thermal oxidation of the substrate.

For doping S/Ds, shallow junctions have been realized using developed novel processes, such as ion-implantation. For example, 40 nm-long gate n-MOSFET with 10 nm-deep junctions were formed by solid-phase diffusion of phosphorous [7]. The sheet resistances was 6.2k$\Omega/\square$ and the dopant concentration, 1×10^{21}cm^{-3}. For p-MOSFETs, 7 nm-deep junctions were formed by ion-implantation of decaborane [8]. The sheet resistance was 25k$\Omega/\square$ and the dopant concentration was $\sim10^{20}$cm^{-3}. These values are almost the same as those in Fig. 1. 2. However, to break through the process limit, the junction depth must be a few nm and the dopant concentration must be more than 1×10^{21}cm^{-3}, which is the solid solubility limit of the dopant. The limits to S/D formation are determined by control of the dopant concentration and the solid solubility limit [18].

From this discussion, it is clear that the process limits, which depend on the gate oxide thickness and the S/D junction depth are determined by the materials from which the device is fabricated.

The physical device operation limit is as follows. 14 nm-long gate MOSFETs have been demonstrated using ultra-shallow junctions, formed by an electric field [10]. This shows that 14 nm-long gate MOSFETs can be operated using scaling-rules. However, after breaking through the process limit to fabricate 10 nm-long channels, the channel length is equal to the electron wave length in Si. Then, the device operates quantum mechani-

cally. For example, tunneling current flows directly from source to drain. Moreover, interband tunneling at the source/channel and drain/channel junctions occurs due to the increased dopant concentration required by the scaling-rules. Therefore the device operation is discussed using quantum mechanics, and scaling-rules can not be used in the nm-size region.

Therefore, to realize nm-size devices, new device materials for the process limit and a new operating principle for the physical limit are necessary.

1.2.2 Realization of nm-size Device

In this section, a method of realizing nm-size devices is described. Firstly, the gate insulator material is discussed. A high permittivity gate insulator is necessary for keeping gate control and insulation. The efficiency of the gate control is determined by the permittivity ratio between the gate insulator and the channel (Si). Thus, if an insulator, which has a higher permittivity than SiO_2 is used, the insulator thickness can be thicker giving better insulation properties. At present, silicon nitride and oxynitride are being studied [19]. Silicon nitride and oxynitride are well known insulators, due to the fact that nitride and oxynitride films are used for tunneling barriers in Flash memory devices and boron stoppers through gate oxides. In addition, MOSFETs with Ta_2O_5 (ε_r=25) gate insulators have been reported [20, 21], and thin Ta_2O_5 films, equivalent to 1.8 nm-thick SiO_2 show gate leakage reduction, when compared to SiO_2 films. Moreover, epitaxially grown nm-thick gate insulators on Si are attracting attention [22]–[24]. Using epitaxial growth, uniform and controllable nm-thick films can be realized. To break through the gate oxide thickness limit, a high permittivity insulator is necessary.

For the formation of S/D junctions, low resistance layers such as el-

evated S/Ds or self aligned silicides [25]–[28] and short insulator spacers as shown in Fig. 1. 2 are needed to reduce series resistance, while ultra-shallow junctions can be realized by developing the doping process. Therefore, metal S/Ds are very attractive prospect for nm-size devices. The metal has a high carrier concentration, of about $10^{22}cm^{-3}$, and the fabrication process is simpler. The sheet resistance of nm-thick metal is about $100\Omega/\square$, because the resistivity of metals is about $10\mu\Omega cm$. Therefore, low resistance and ultra-shallow S/Ds can be realized by using a metal without the need for a low resistance layer on S/D, and with the benefit of a low contact resistance between the S/D and the external electrode. In addition, the source/channel and drain/channel interface can be controlled precisely by the metal/semiconductor hetero-interface. Silicide technology has been developed particularly for low contact and sheet resistance [27]–[31]. Thus silicides are part of conventional Si devices and can be easily realized.

For devices with ultra-thin gate oxides, the depletion layer at the gate/gate oxide interface can not be neglected, because the gate electrode in conventional MOSFETs is formed with highly doped poly-Si. Therefore, to prevent this, the gate electrode should be formed with a metal [32, 33].

For short channel devices, statistical fluctuation of the channel dopant is problematic [34, 35]. The channel should use an un-doped layer, although the channel doping concentration must be increased to suppress the short channel effect. Therefore, a fully depleted silicon on insulator (SOI) structure is an attractive choice.

Now, a solution to the physical limit is proposed. In the nm-size region, devices operate quantum mechanically. As a result, nm-size devices be-

come quantum effect devices. Tunneling devices are one of the attractive choices for nm-size devices.

So, from these discussions, it has become apparent that a tunneling field effect device with a high permittivity gate insulator, a metal S/D and gate and un-doped channel is an attractive choice for nm-size device.

1.2.3 Utilization of Quantum Effect Devices

The appearance of quantum effects in the nm-size region have been described. In this section, the advantages of quantum effect devices will be explained. Quantum effect devices can be fabricated not only with a high level of integration, but also with a simplified circuit construction because of the different current-voltage characteristics from conventional devices [36].

Figure 1. 3 shows a flip-flop circuit using resonant tunneling diodes (RTDs). The current-voltage characteristic of a RTD has negative differential resistance (NDR), as shown in Fig. 1. 3 (b). The voltage at the midpoint of two RTDs V_{out} is either at point S_1 or S_2, which is determined by the load line (dashed line). When RTD1 is the load and RTD2 is the transistor with NDR characteristics, V_{out} is changed from S_1 to S_2 or from S_2 to S_1 by the input signal "0" or "1". The timing diagram is shown in Fig. 1. 3 (c). This R-S flip-flop circuit can be constructed using two RTDs. Using conventional MOSFETs, the R-S flip-flop circuit is constructed using two NAND gates and each NAND gate is constructed using two transistors. Therefore, four MOSFETs are necessary for a R-S flip-flop. Using quantum effect devices, the number of devices in the circuit can be decreased.

The first application of quantum devices to a circuit were demonstrated using resonant tunneling hot electron transistors (RHETs) [37, 38]. Fol-

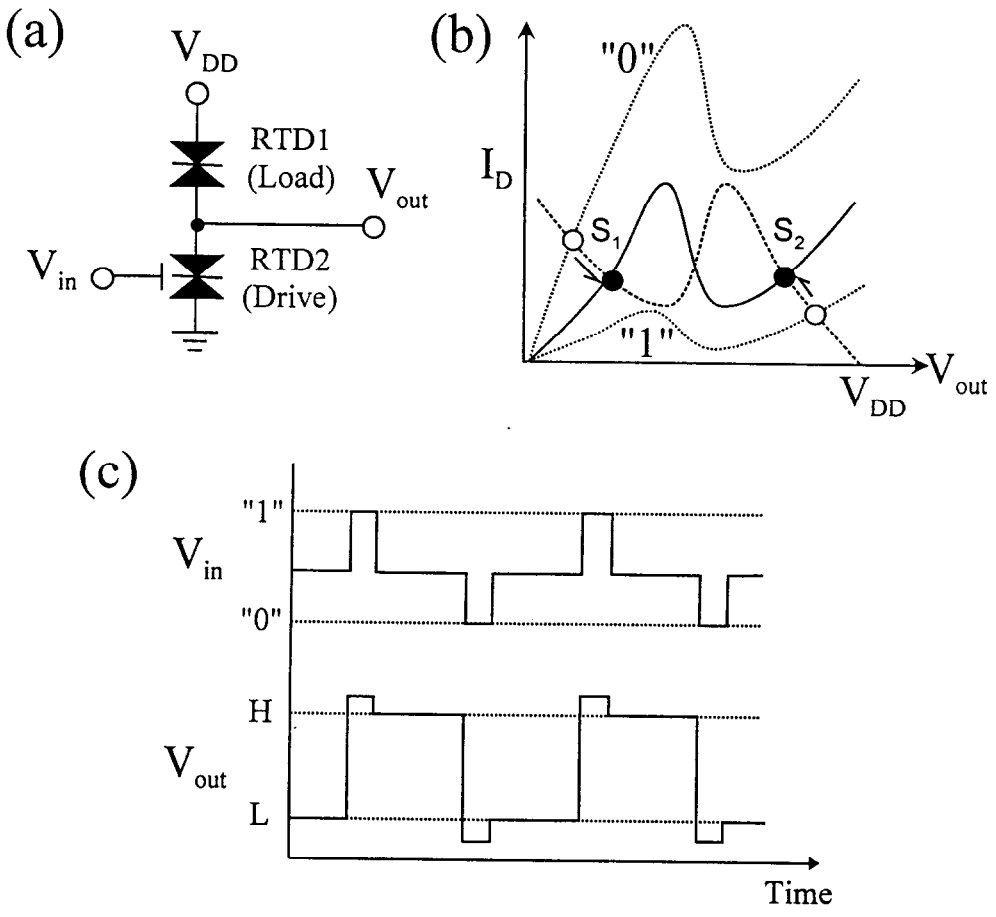


Figure 1.3: Simple flip-flop circuit using resonant tunneling devices. (a) circuit configuration, (b) current-voltage characteristics and (c) timing diagram.

lowing that, field effect type quantum effect devices, which have a high input impedance have been studied for use in LSI elements [39]–[42]. Recently, four valued analog/digital converters and 35 Gb/s D-flip-flops have been demonstrated using a NDR device, composed of a RTD and a HEMT [43, 44]. As yet there have been no reports on quantum effect device applications to circuits, although quantum effect devices on Si substrates have been reported [45]–[49]. Circuit applications with the NDR characteristics of an interband tunneling diode have been demonstrated [50]–[52].

1.3 Tunneling Field Effect Transistors

The tunneling field effect transistor with a metal S/D and gate is an attractive choice for nm-size devices and is applicable to multi functional devices, such as described above. In previous work, many kinds of tunneling field effect transistors have been proposed and demonstrated. These devices can be divided into two types of transistor. The device structures of each of these types shown in Fig. 1. 4. One of them is a Schottky S/D MOSFET, which has an ultra-shallow metal S/D junction, as shown in Fig. 1. 4 (a) [53]–[55]. The source/channel and channel/drain junctions are Schottky diode junctions. The channel region is a tunneling barrier, and carriers tunnel from the source to the channel through the Schottky barrier by application of a gate voltage. The metal/insulator tunneling transistor, which has an insulator for the channel and the same device structure as a Schottky S/D MOSFET, has been studied [56]–[59].

The other type of tunneling field effect transistor is the Vertical Tunneling Field Effect Transistor (VTFET), which consists of a metal/semiconductor/insulator heterostructure, as shown in Fig. 1. 4 (b). The gate voltage controls the electric field at the source barrier and electrons tunnel from the source to the channel through the nm-thick tunneling barrier [60]–[63]. In this work, VTFETs with a $CoSi_2/Si/CdF_2/CaF_2$ heterostructure, which can be grown on Si substrates [64]–[68] are studied. For this VTFET, the source, drain and gate is $CoSi_2$ and the gate insulator is CaF_2, which has a higher permittivity than SiO_2 and enables device operation at nm-sizes. In addition, large current drivability can be achieved, because the tunneling junction is composed of a nm-thick heterostructure.

These tunneling devices can be operated at nm-sizes and detailed char-

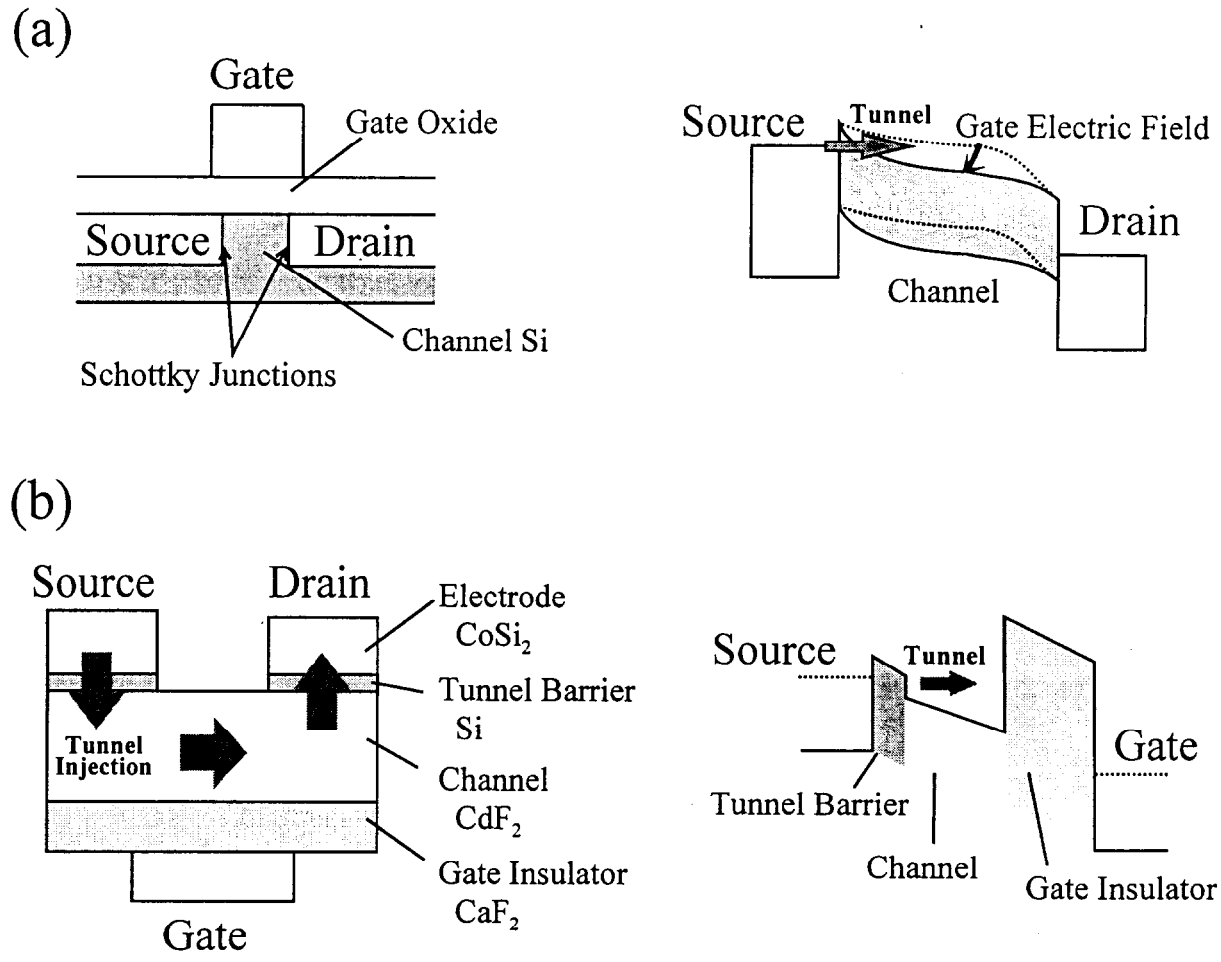


Figure 1.4: Tunneling field effect transistors. (a) Schottky S/D MOSFET and (b) vertical tunneling field effect transistor (VTFET).

acteristics at this size is described in chapters 2 and 4. The drain curves of these devices are very similar to those of conventional MOSFETs. Schottky S/D MOSFETs can easily be realized, because the fundamental device structure is the same as that of a conventional MOSFET. The VTFET can be applied as a quantum effect device, such as resonant tunneling device and quantum interference device [39, 69], because the VTFET is fabricated with multi layer heterostructures. Improvements in the circuit capability can be achieved the reducing the number of devices in the circuit using quantum effect devices [36, 43, 44].

1.4 Purpose and Outline of This Thesis

The purpose of this thesis is to realize tunneling field effect transistors with metal S/D and gate and un-doped channel as ultra-fine elements in LSI. Schottky S/D MOSFETs and vertical tunneling field effect transistors (VTFETs) with $CoSi_2/Si/CdF_2/CaF_2$ heterostructures, which can be grown on a Si substrate, were studied. For each device, degradation of the characteristics for very short channel structures was analyzed theoretically. From a comparison between conventional MOSFETs and tunneling FETs, the advantage of these tunneling devices with very short channel structures was shown theoretically. Very short metal gate Schottky S/D MOSFETs were fabricated on a SIMOX substrate, and room temperature operation of a 25 nm-long gate device was demonstrated. CdF_2/CaF_2 heterostructures, which were a fundamental structure of the proposed VTFET were grown on a Si substrate and primitive field effect transistor action with these heterostructures was demonstrated. The outline of the thesis is shown in Fig. 1. 5. In chapter 2, a theoretical analysis of the Schottky S/D MOSFET is described. The characteristics of the Schottky S/D MOSFET in the nm-size region are discussed and a comparison between the Schottky S/D MOSFET and the conventional MOSFET is shown. In chapter 3, the characteristics of the Schottky S/D MOSFET fabricated on a SIMOX substrate are described. In chapter 4, a theoretical analysis of the VTFET is done. The characteristics of the VTFET at nm-sizes are discussed and a comparison between the VTFET and the conventional MOSFET is shown. In chapter 5, fabrication of field effect transistors with CdF_2/CaF_2 heterostructures grown on a Si substrate, which is the fundamental structure of the VTFET, is described. The fabrication process and the electrical characteristics of

field effect transistors with CdF_2/CaF_2 heterostructures are discussed. In chapter 6, the conclusions of this study are described.

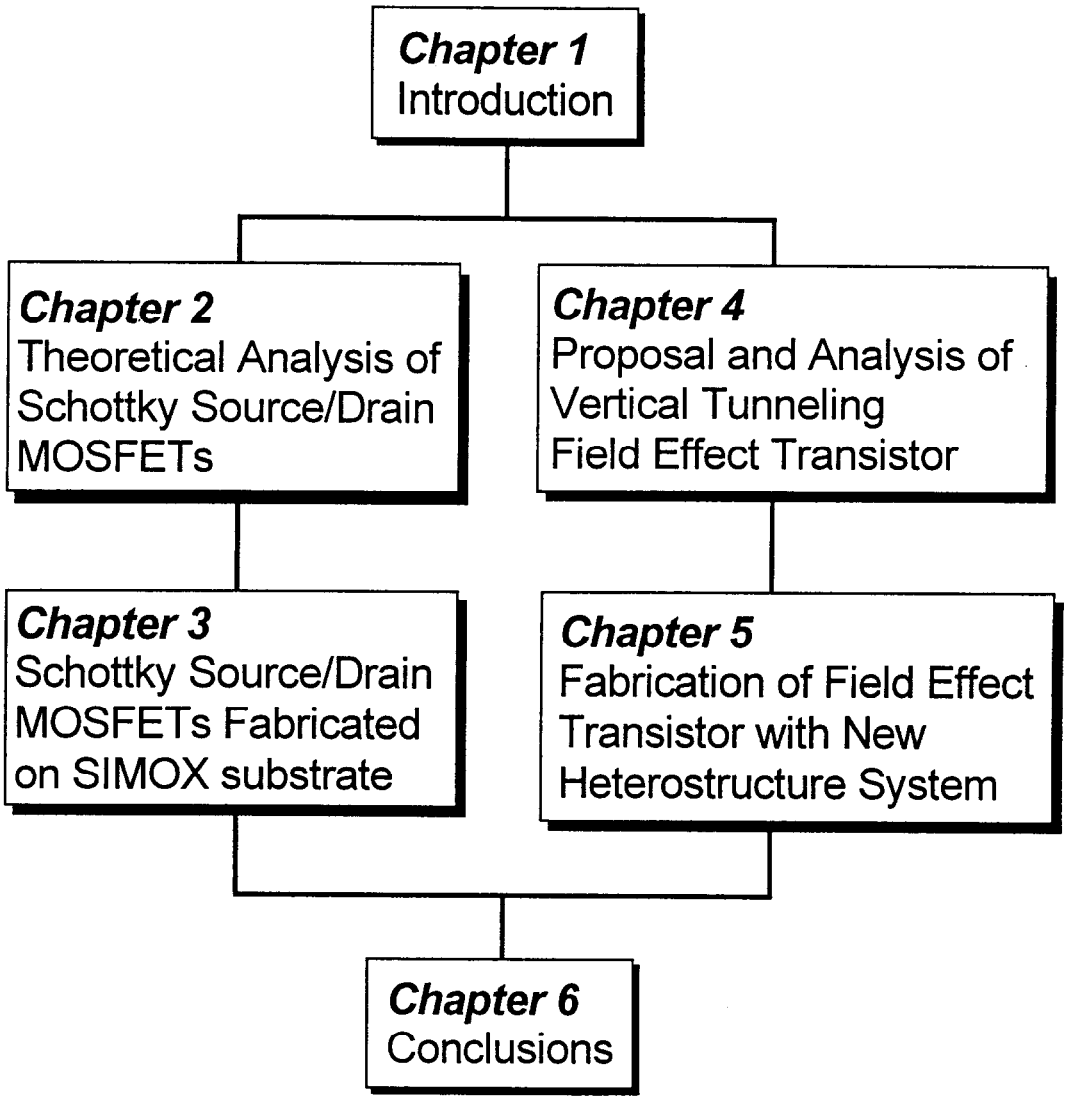


Figure 1.5: Outline of this thesis.

Chapter 2

Theoretical Analysis of Schottky Source/Drain MOSFETs

2.1 Introduction

The Schottky source/drain (S/D) MOSFET, which has ultra shallow metal S/D junctions, as described in the previous chapter, has the potential for scaling into the nanometer regime. The first demonstration of the Schottky S/D MOSFET was reported in 1968 [70]. Then several groups studied Schottky S/D MOSFETs in 1980s [71, 72, 73]. However, the current drivability of these devices was smaller than that of conventional MOSFETs, because the tunneling resistance was large due to the gap between the gate and the S/D junctions. Although the Schottky barrier thickness was thinned and drivability was increased by channel doping [74, 75], electrical circuits continued to be manufactured using conventional MOSFETs for which doping process were developed to provide low resistance and shallow S/D junctions. However, due to metal S/D and tunneling device, in 1990s, nm-sized Schottky S/D MOSFETs were analyzed theoretically [53, 54, 76, 77], and were demonstrated [55], [78]–[80]. Recently, 27 nm-long channel PtSi Schottky S/D MOSFETs have been reported [81].

Although low S/D resistances can be realized by metal S/D junctions

in the Schottky S/D MOSFET, the drain current is suppressed by the Schottky barrier. If the S/D is formed with a high Schottky barrier metal, the tunneling resistance of the Schottky barrier increases and the drain current becomes small. If this problem can be solved, the Schottky S/D MOSFET will have the same capability as a conventional MOSFET with a highly doped S/D. In addition, there are several advantages of applying Schottky S/D MOSFETs to integrated circuits. The contact resistance between the S/D and the external electrode is lower. The temperature during the fabrication process is lower, because the process requires no doping. Thus the metal gate can be easily realized [32, 33].

As mentioned in the previous chapter, the channel should be un-doped, because the statistical fluctuation of the dopant is problematic for a short channel device. However, the channel doping concentration must be increased to suppress the short channel effect. Therefore, a fully depleted SOI structure is an attractive choice. In this work, a single gate SOI structure, which is the most popular structure for suppressing the short channel effect, was chosen. Double gate, gate all around and wire channel structures have been proposed and demonstrated [82]–[90]. In these structures, suppression of the short channel effect can be realized by increasing the gate area, which has the same effect as thinning the gate oxide. Although these structures strongly suppress the short channel effect, it is difficult to apply to integrated circuits, because of the complicated structure. Although the cost of SOI wafer products is high, IBM has succeeded in reducing this and started to sell SOI chips with single gate structures. [91]. Therefore a single gate SOI structure is the pragmatic structure for suppression of the short channel effect.

In this chapter, a theoretical analysis of the Schottky S/D MOSFET is

described. The relationship between the Schottky barrier height and current drivability is discussed. The characteristics of Schottky S/D MOSFETs in the nm-size region are discussed and a comparison between the Schottky S/D MOSFET and the conventional SOI-MOSFET is drawn.

2.2 Device Structure

The device structure is shown in Fig. 2. 1. As mentioned in the previous section, the single gate SOI structure was used. The gate oxide thickness was 3 nm. The SOI layer and buried oxide layer (BOX) thicknesses were 10 and 50 nm, respectively. The S/D junction depth was the same as the SOI layer thickness. In operation, electrons or holes tunneling through the Schottky barrier from the source to the channel were controlled by the voltage applied to the gate across the gate oxide. The drain current depends on the tunneling resistance of the Schottky barrier and the channel resistance. For a high S/D Schottky barrier, the drain current depends mainly on the tunneling resistance, and for a low barrier, the characteristics become almost the same as those of a conventional MOSFET, in which the drain current is determined by the channel resistance.

2.3 Calculation Model

The device characteristics were analyzed as follows. First, the potential distribution in the device under the application of drain-source and gate-source voltages (V_{DS} and V_{GS}) was calculated by solving Poisson's equation using a finite element method. The outer material surrounding the device was assumed to be SiO_2. Then, the drain current was calculated using the potential distribution calculated above. The carrier

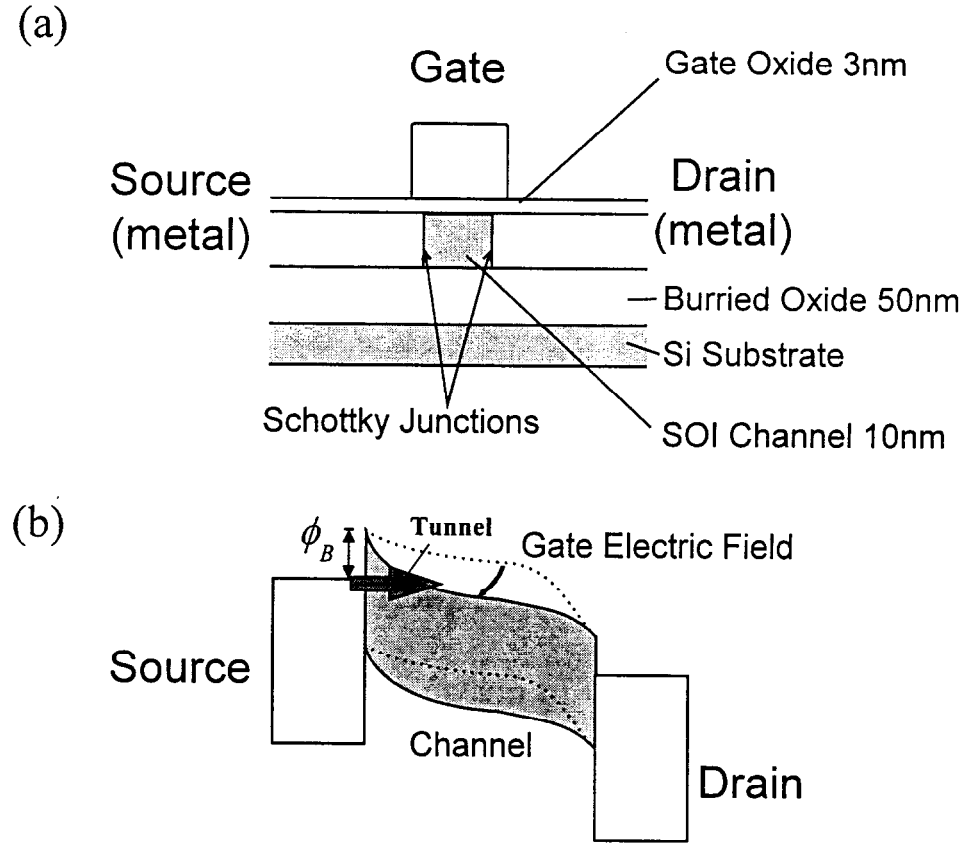


Figure 2.1: Device Structure of Schottky S/D MOSFET. (a) Cross-sectional structure and (b) band diagram.

density in the channel affects the potential distribution and the drain current. This carrier density is determined by the drain current. Therefore, the drain current was recalculated to be self-consistent with the carrier density and the potential distribution.

The potential distribution was calculated by solving the following Poisson's equation.

$$\nabla^2\phi = \frac{en_C}{\varepsilon}, \tag{2.1}$$

where e is the electron charge, ϕ is the potential, n_C is the carrier density and ε is the permittivity.

Carrier transport at the Schottky barrier was modeled by a combination of the thermal emission current J_{TH} and the tunneling current J_{TN},

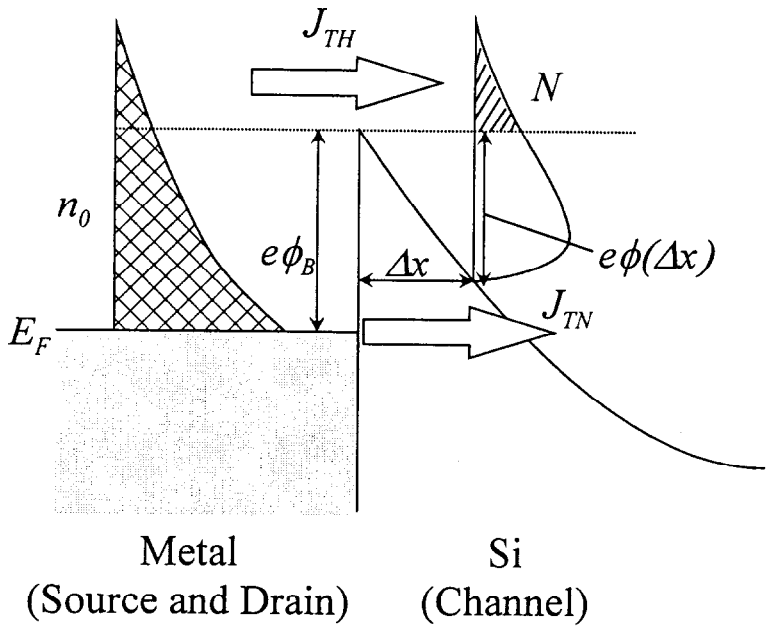


Figure 2.2: Model for calculation of the device characteristics.

as shown in Fig. 2. 2.

The thermal emission current is given by

$$J_{TH} = RT^2 \left[\frac{N}{n_0} - \exp\left(-\frac{e\phi_B}{k_B T}\right)\right], \tag{2.2}$$

where T is the absolute temperature and R is the Richardson constant, which is given by

$$R = \frac{4\pi e m^* k_B^2}{h^3}, \tag{2.3}$$

where m^* is the effective mass, k_B is Boltzmann's constant, h is Planck constant and ϕ_B is the Schottky barrier height. In eq. (2. 2) n_0 is the density of carriers having greater energy than the Fermi energy in the metal. This is shown in Fig. 2. 2 and is given by

$$n_0 = n_i \exp\left(\frac{E_g}{2k_B T}\right). \tag{2.4}$$

In eq. 2. 2, N is the density of carriers at a distance Δx from the Schottky interface, which have a greater energy than $e\phi_B$. This is shown in Fig. 2. 2

and is given by

$$N = \frac{RT^2}{eD} \exp\left(-\frac{e\phi_B}{k_B T}\right) \Delta x \exp\left(-\frac{e\phi\left(\Delta x\right)}{k_B T}\right), \tag{2.5}$$

where D is the diffusion constant.

The tunneling current through the Schottky barrier J_{TN} is given by [92]

$$J_{TN} = \frac{e^2 F^2}{8\pi h \phi_B} \exp\left[-\frac{8\pi}{3heF}\sqrt{2m^*\left(e\phi_B\right)^3}\right], \tag{2.6}$$

where F is the electric field at the Schottky barrier.

Barrier lowering due to the image force is included in the calculation using the following equation.

$$\phi_B = \phi_{B0} - \sqrt{\frac{eF}{4\pi\varepsilon}}, \tag{2.7}$$

where ϕ_{B0} is the Schottky barrier height without an applied voltage.

The drain current J_D is given by the difference between the current from the source to the drain J_{SD} and the current from the drain to the source J_{DS}.

$$J_D = J_{SD} - J_{DS} = \left(J_{THS} + J_{TNS}\right) - \left(J_{THD} + J_{TND}\right), \tag{2.8}$$

where J_{THS}, J_{TNS}, J_{THD} and J_{TND} are given by eqs. (2.2) and (2.6).

The current in the channel J_{CH} was calculated using the drift-diffusion model.

$$J_{CH} = en_{CH}\mu_{eff}\left(-\nabla\phi\right) + eD\nabla n_{CH}, \tag{2.9}$$

where μ_{eff} is the effective mobility and n_{CH} is the carrier density in the channel. For the calculation of the carrier distribution in the channel, the following equation was used as a boundary condition at each point in the channel,

$$\nabla \cdot J = 0. \tag{2.10}$$

The carrier density in the outside of the channel was assumed to be zero. The carrier density at the S/D interfaces was calculated from the drain current using eq. (2. 5). The drain current was recalculated to be self-consistent with the carrier density and the potential distribution, because the carrier density in the channel affects the potential distribution and the drain current. The process for calculating the drain current is shown in Fig. 2. 3.

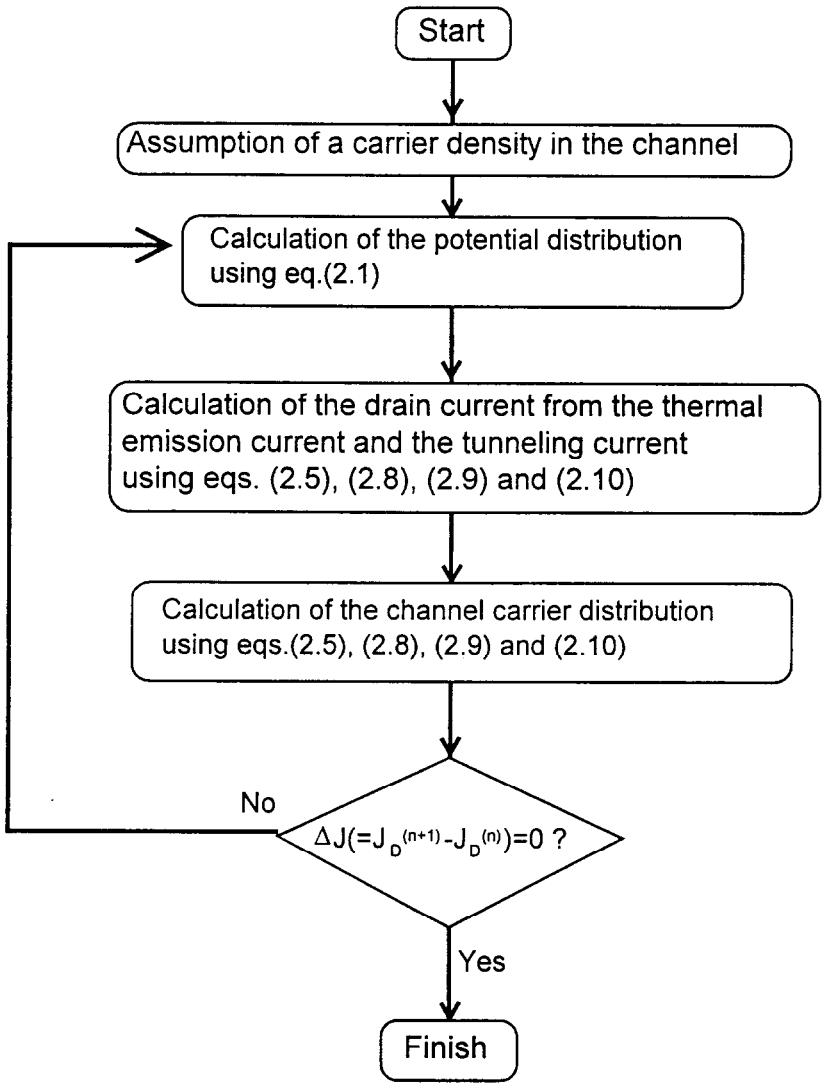


Figure 2.3: Self-consistent process for calculating the drain current.

2.4 Results of Calculation

In this calculation, the constants used for electrons and holes were as follows. For Si the effective masses were $m^*_e = 0.19m_0$ and $m^*_h = 0.15m_0$ for electrons and holes, respectively [93]. The hole effective mass used was that of a light hole. The mobilities of Si used were $\mu_e = 450$ cm^2/Vs and $\mu_h = 125$ cm^2/Vs for electrons and holes, respectively [94]–[97]. These mobilities were for an effective channel electric field of $E_{eff} = 0.4$ MV/cm [96, 97], which corresponds to the electric field in the channel at $V_{GS} =$ 1.5 V. In this calculation, velocity saturation was neglected.

2.4.1 Drain Current Curves

Figure 2. 4 shows the common-source characteristics calculated at 300K for various values of V_{GS} for a 50 nm gate length p-type Schottky S/D MOSFET. The channel length was 35 nm. The Schottky barrier height was assumed to be 0.25 eV. As with conventional MOSFETs, the drain curves for the Schottky S/D MOSFETs saturate.

2.4.2 Current Drivability

The relationship between the channel length L_C and the drain current I_D as a function of the Schottky barrier height ϕ_{B0} is shown in Fig. 2. 5. The applied voltages were $V_{DS} = V_{GS} =$ -1.2 and 1.2 V for p-type and n-type, respectively. The drain current increases with Schottky barrier lowering, due to the increased thermal emission and tunneling currents, as shown in eqs. (2. 2) and (2. 6). To compare Schottky S/D MOSFETs and conventional MOSFETs, the drain current of conventional MOSFETs [98, 99] is drawn in the same figure. These results show that for L_C<30 nm the same drivability as for conventional MOSFETs can be realized using

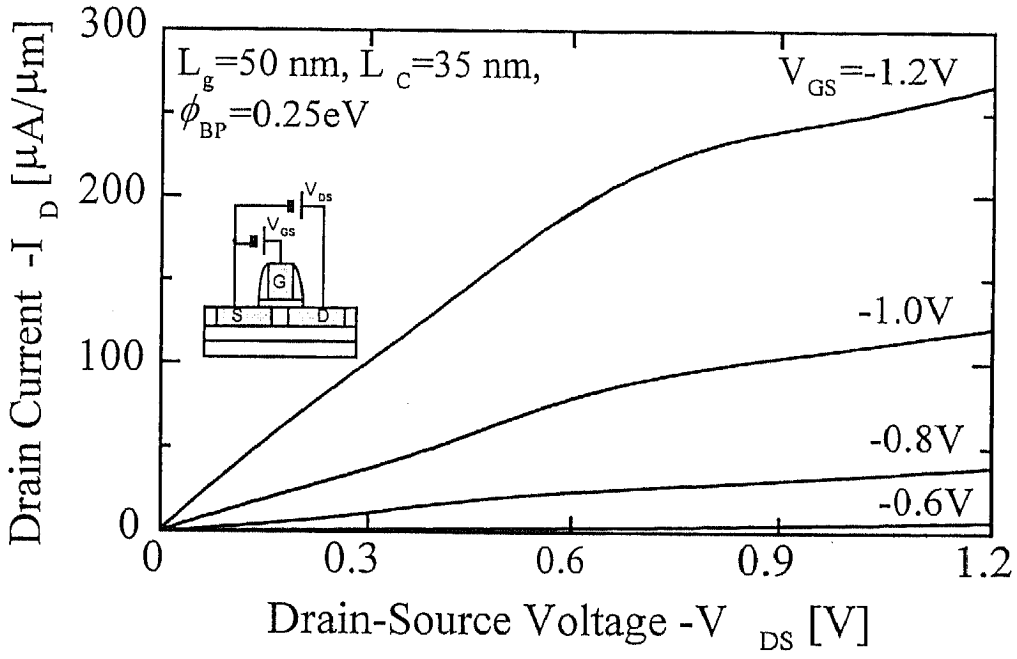


Figure 2.4: The drain current curves with common-source for a 50 nm gate length Schottky S/D MOSFET with 0.25 eV S/D Schottky barrier.

low Schottky barriers. These were estimated to be about 0.25 for p-type and 0.1–0.15 eV for n-type devices, respectively. This difference between the estimated barrier height for n-type and p-type depends on the effective mass.

Taking these barrier heights into consideration the appropriate S/D metal is discussed bellow. The Schottky barrier height depends on the material [100, 101]. Therefore both n-type and p-type devices can be realized by the choice of S/D metal. For p-type devices, appropriate S/D metals are PtSi (ϕ_{Bp}=0.24 eV) and IrSi (ϕ_{Bp}=0.18 eV) [76, 102, 103]. However, there are no silicides which meet the above requirement for n-type devices. Although the lowest Schottky barrier silicide is $ErSi_2$ (ϕ_{Bn}=0.2 eV) [79, 104, 105, 106], the drivability of $ErSi_2$ Schottky S/D MOSFETs is ten times smaller than that of conventional MOSFETs.

In previous reports, the Schottky barrier height of germanosilicide was reported to be lower than that of silicide [78, 107, 108]. Therefore good drivability can be realized using germanosilicide S/Ds.

2.4.3 Subthreshold Characteristics

The subthreshold characteristics of p-type Schottky S/D MOSFETs as a function of channel length are shown in Fig. 2. 6. The Schottky barrier height is 0.3 eV. The subthreshold characteristics degraded with decreasing channel length. In addition, a current plateau appears in the subthreshold characteristics [55]. This is because the tunneling current becomes larger than the thermal emission current in the high negative gate voltage region. In addition, in the high positive gate voltage region, the drain current increases with positive gate voltage, because the channel mode changes from p-type to n-type [80].

The band diagrams of Fig. 2. 7 illustrate the operating principle of the device. With high negative gate bias, holes tunnel through the Schottky barrier and the drain current increases with gate bias, this time along field emission characteristics (Fig. 2 .7 (a)).

With decreasing negative gate bias, only the fixed Schottky part of the barrier to holes remains and the current is limited by thermal emission (Fig. 2. 7 (b)).

In Fig. 2. 7 (c), when the device is in its off state, drain leakage current enters the channel crossing a combination of the Schottky barrier and an electrostatic barrier through thermal emission. The characteristics in this region are the same as in conventional MOSFETs.

With high positive gate voltage, electrons tunnel through the drain Schottky barrier and the drain current increases with positive gate bias (Fig. 2. 7 (d)).

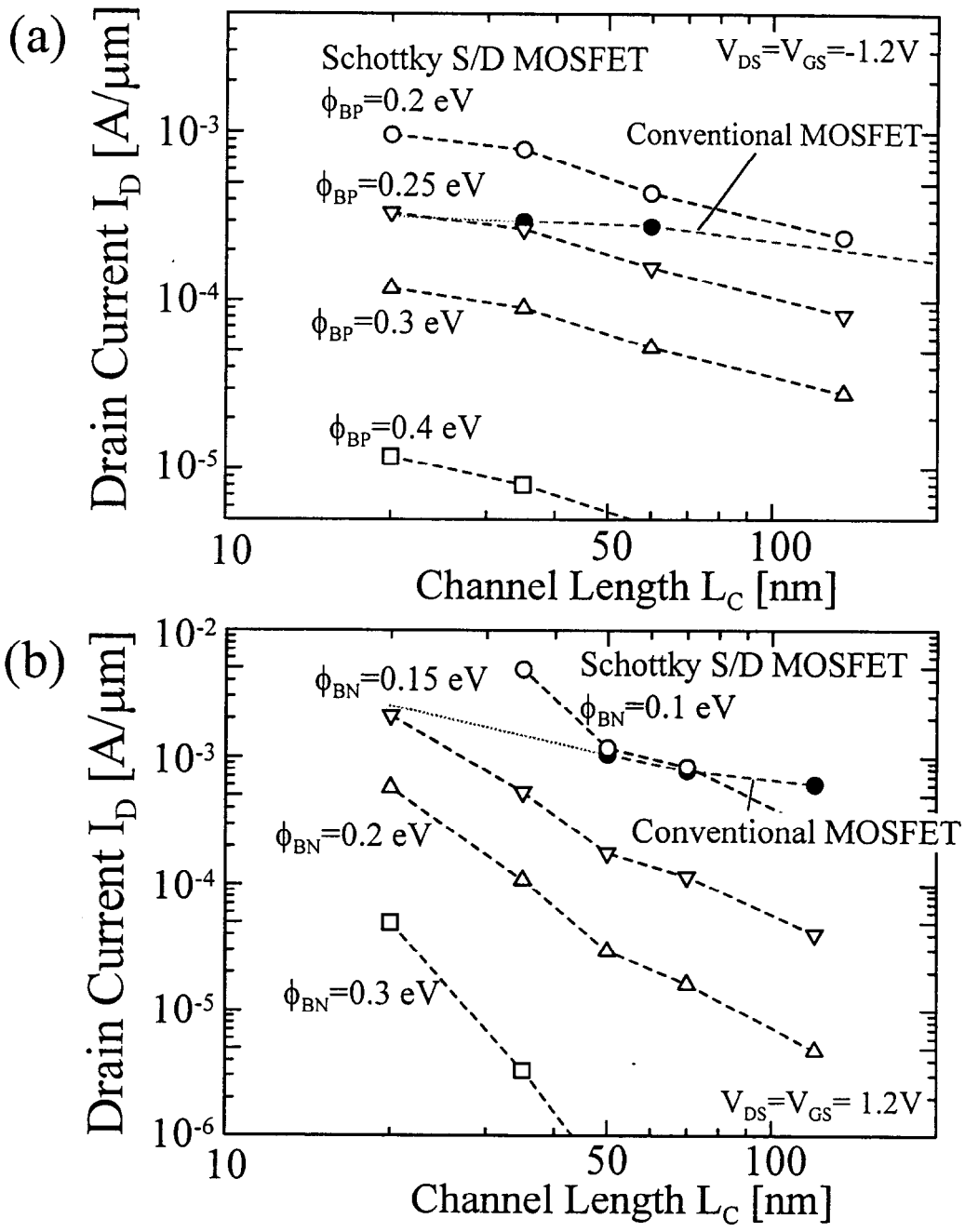


Figure 2.5: Drivability of Schottky MOSFETs as a function of Schottky barrier height for (a)p-type and (b)n-type devices.

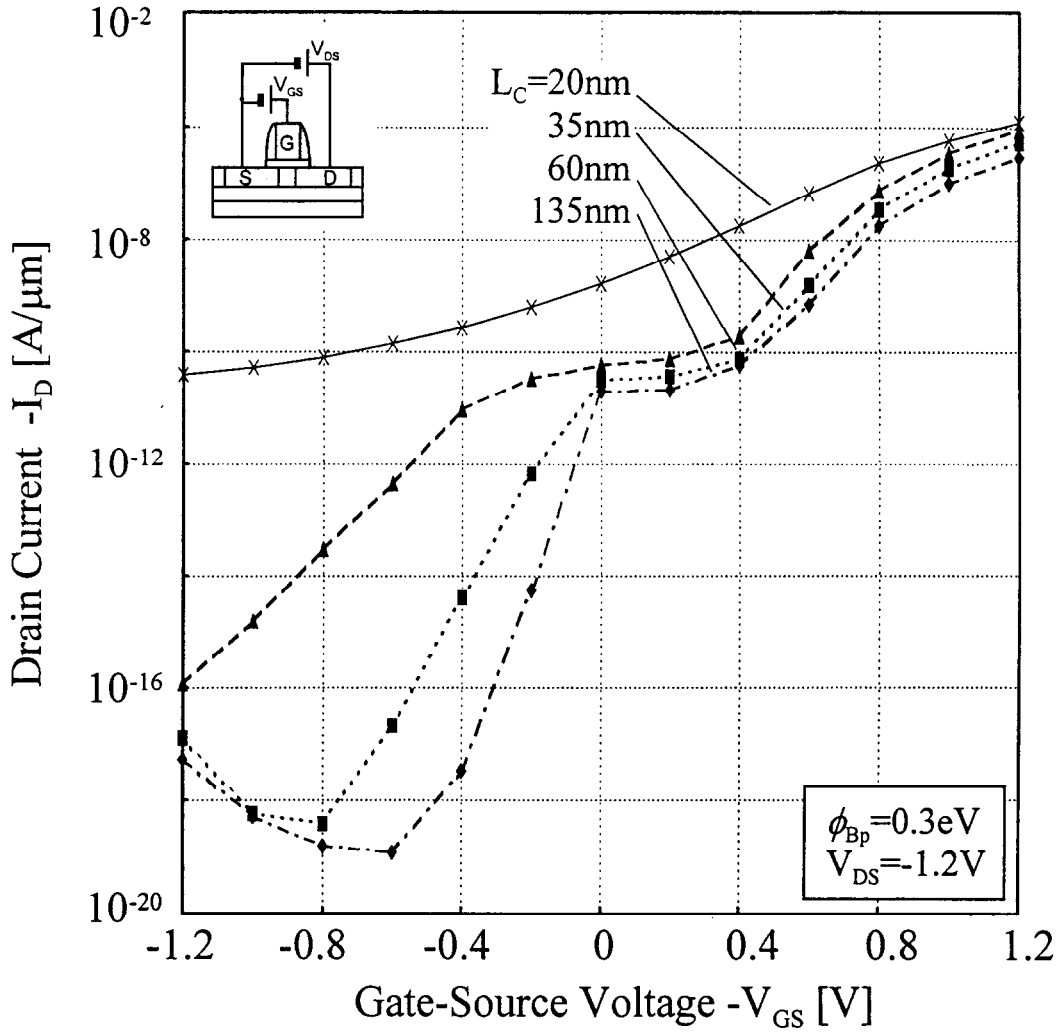


Figure 2.6: Subthreshold characteristics of Schottky S/D MOSFETs as a function of channel length.

In the subthreshold characteristics, the limit of the off current is shown. The limiting off current is determined by the change of the channel mode and depends on the drain Schottky barrier height. Therefore the off current can be small using a drain metal which has a low Schottky barrier in the on-state.

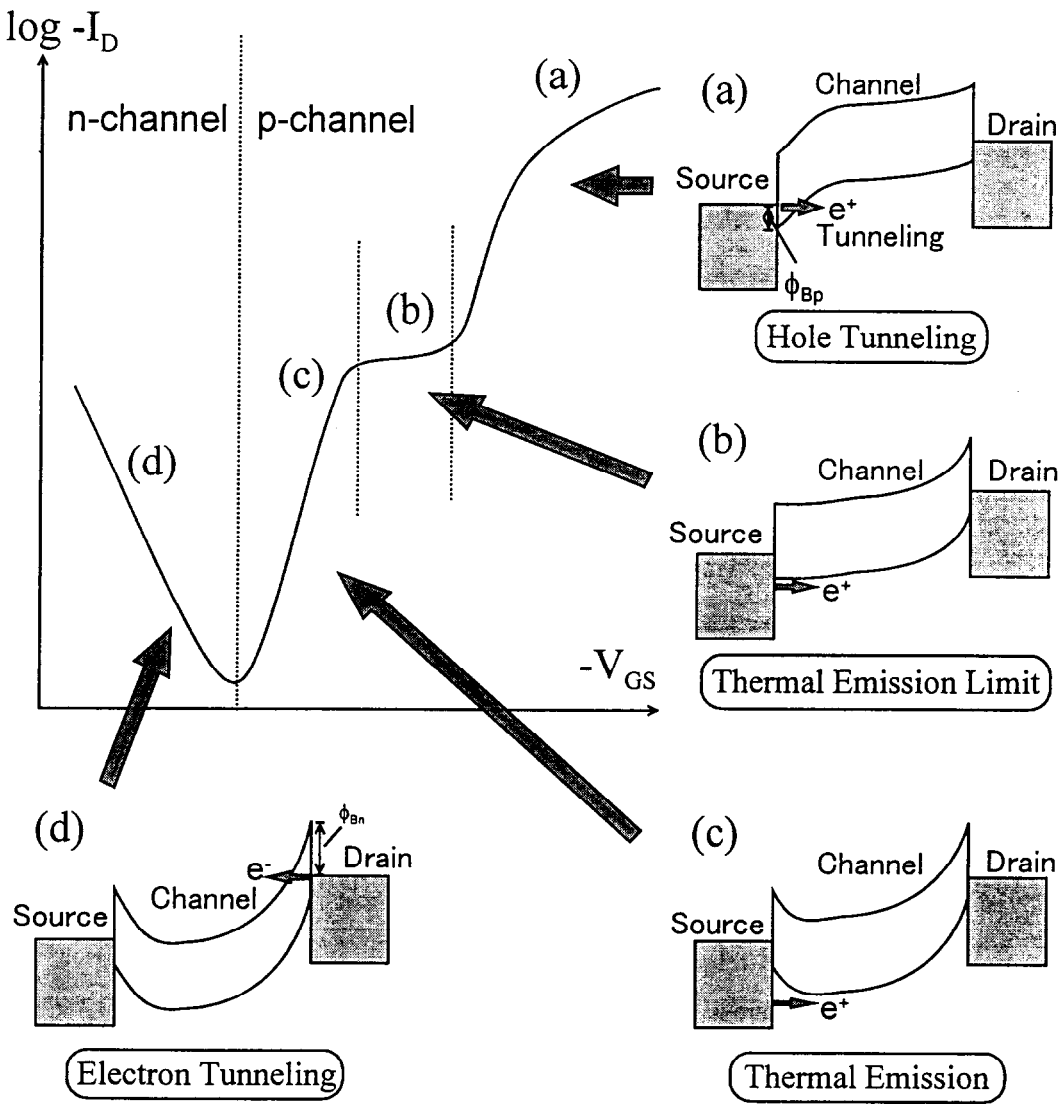


Figure 2.7: A band diagram description of the different current regimes showing typical subthreshold characteristics.

2.4.4 Short Channel Effect

The relationship between threshold voltage shift, subthreshold swing and channel length for a p-type Schottky S/D MOSFET with 0.25 eV S/D barriers is shown in Fig. 2. 8. For comparison between a Schottky S/D MOSFET and a conventional MOSFET, the results calculated by Fiegna et. al. for conventional MOSFETs with the same device structure, are drawn in the figure [99]. The threshold voltage is defined as the gate bias corresponding to $I_D L_C / W_C = 0.5\ \mu$A. The threshold voltage shift of Schottky S/D MOSFETs is smaller than that of conventional MOSFETs. However the subthreshold swing of Schottky S/D MOSFETs is larger than that of conventional MOSFETs even with a long channel. In the conventional MOSFET, the drain current is controlled by the gate bias, which modulates the channel potential under the gate electrode. In the Schottky S/D MOSFET, the drain current is modulated by the electric field at the source Schottky barrier. The drain voltage strongly affects the potential at the center of the channel. However, the potential near the source is weakly affected by the drain voltage. Therefore the threshold voltage shift of Schottky S/D MOSFETs is small. Moreover the region controlled by the gate voltage in Schottky S/D MOSFETs (source/channel interface) extends further than that for conventional MOSFETs (channel region under the gate). Therefore the subthreshold swing of Schottky S/D MOSFETs is larger than that of conventional MOSFETs. To reduce the subthreshold swing, the gate oxide must be thinned, as shown in Fig. 2. 8.

The relationship between the threshold voltage shift, subthreshold swing and the channel length as a function of SOI layer thickness is shown in Fig. 2. 9. The short channel effect can be suppressed by thin-

ning the SOI layer. The short channel effect can be suppressed even with a 15 nm-long channel with t_{OX} = 1 nm and t_{SOI} = 3 nm.

2.4.5 Influence of the gap between the gate and the S/D junctions

In previous works, the reduced drivability due to the gap between the gate and the S/D junctions has been reported [72, 76]. To realize good device characteristics, overlap of the gate and the S/D is necessary. However, the gap depends on the S/D material and the fabrication process, especially when the S/D junctions are formed by diffusion of the metal, such as silicidation. This is covered in the next chapter.

Relationships between the gap d, the drain current, the transconductance and the subthreshold swing are shown in Fig. 2. 10. The channel length is 35 nm, and the gate length is $L_g = L_C - 2d$. When the gate overlaps the S/D, the characteristics do not change. However, with increasing gap, the drain current and the transconductance decrease and the subthreshold swing increases. When the gap is 10 nm, the drain current and the transconductance are reduced by a factor of ten and the subthreshold swing becomes twice the value without a gap. To retain good characteristics, the gap must be less than 10 % of the channel length.

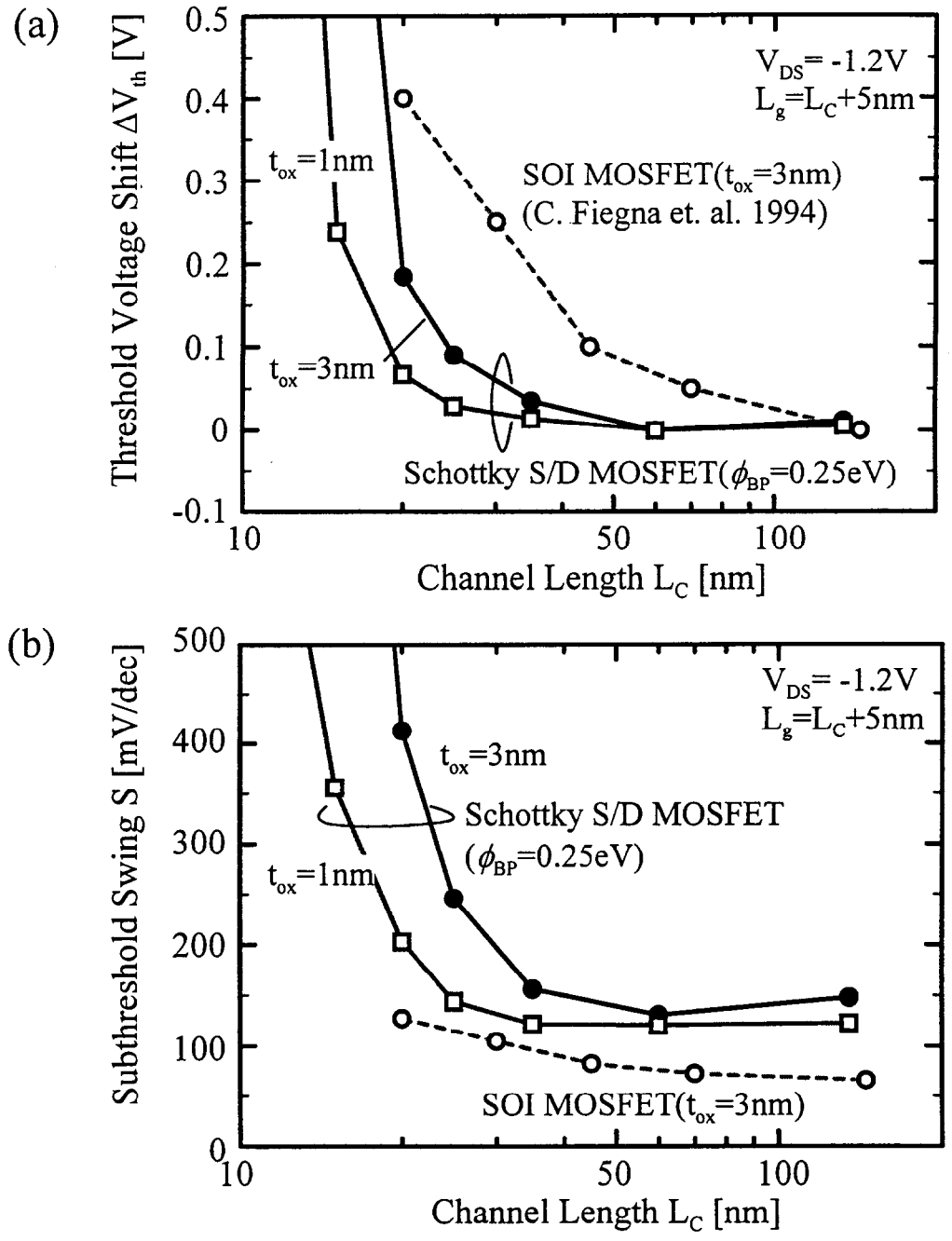


Figure 2.8: Relationship between (a) threshold voltage shift, (b) subthreshold swing and channel length of Schottky S/D MOSFETs and conventional SOI-MOSFETs.

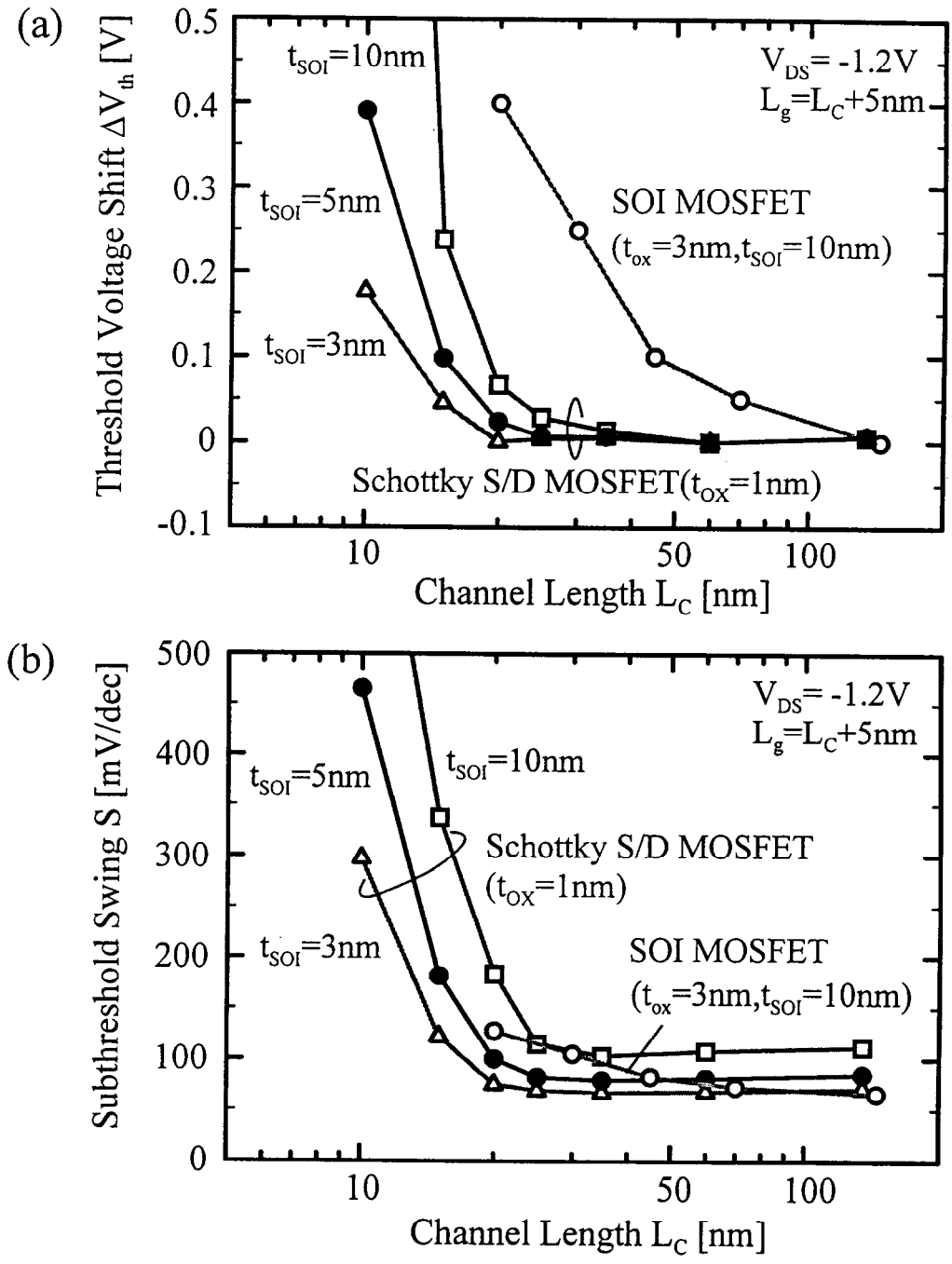


Figure 2.9: Relationship between (a) threshold voltage shift, (b) subthreshold swing and channel length of Schottky S/D MOSFETs as a function of SOI layer thickness.

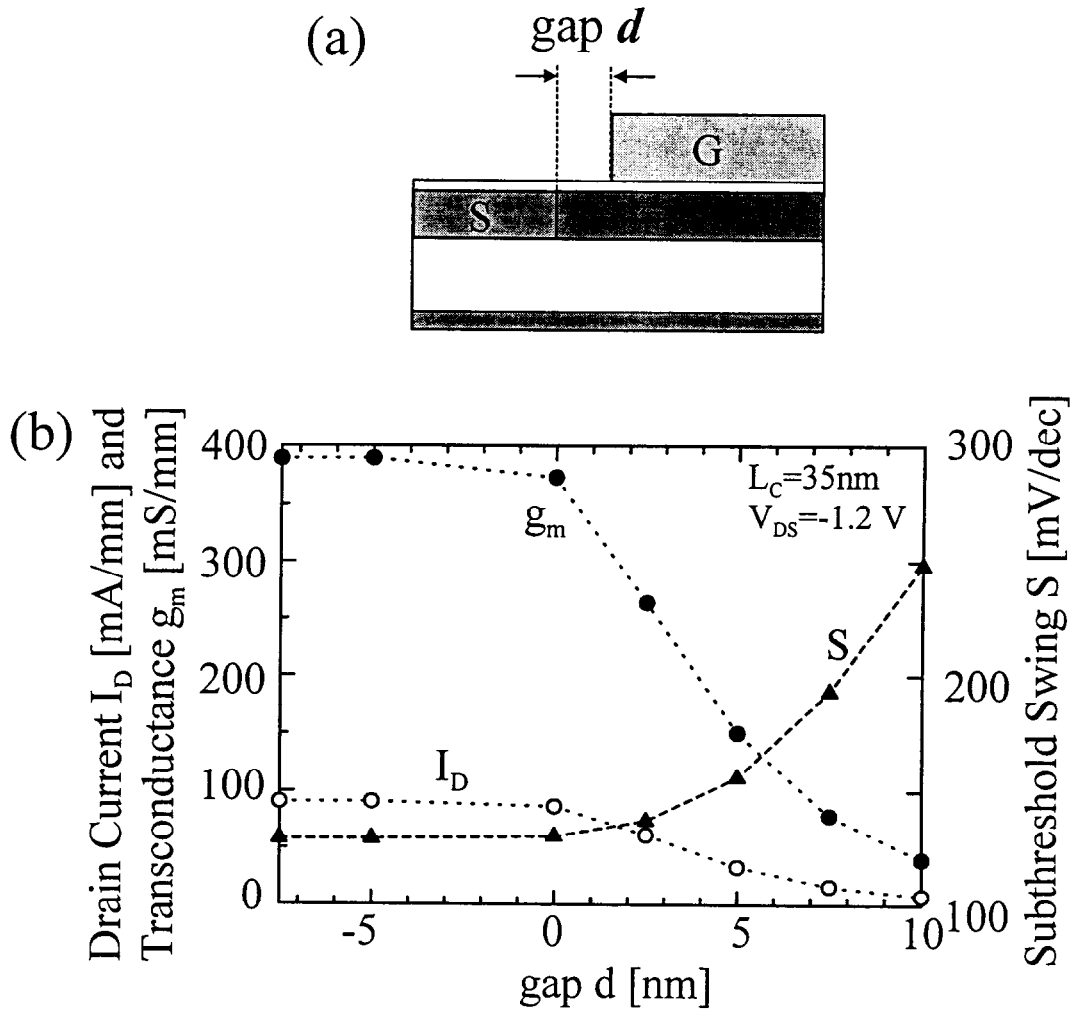


Figure 2.10: (a)Device structure with gap d between the gate and the S/D junctions. (b)Relationships between the drain current, the transconductance and the subthreshold swing and the gap.

2.5 Conclusion

Metal Schottky source/drain (S/D) MOSFETs were analyzed theoretically. The current drivability depends on the Schottky barrier height. The drivability of the Schottky S/D MOSFET, whose channel length is less than 30 nm, is the same as that of a conventional MOSFET, when the Schottky barrier height is 0.25 for p-type and 0.1–0.15 eV for n-type devices, respectively. A low drain Schottky barrier height is necessary for a large on/off ratio. Due to the short channel effect, the increasing threshold voltage shift of Schottky S/D MOSFETs is smaller than that of conventional MOSFETs. The subthreshold swing of Schottky S/D MOSFETs is larger than that of conventional MOSFETs. To reduce subthreshold swing, the gate oxide must be thinned. The short channel effect can be suppressed by thinning the gate oxide and the SOI layer. The short channel effect can be suppressed even with a 15 nm-long channel with $t_{OX} = 1$ nm and $t_{SOI} = 3$ nm. To retain good characteristics, the gap between the gate and the S/D must be less than 10 % of the channel length. Schottky S/D MOSFETs can break through the limits of conventional MOSFETs.

Chapter 3

Schottky Source/Drain MOSFETs Fabricated on SIMOX Substrate

3.1 Introduction

As mentioned in Chap. 2, the Schottky Source/Drain (S/D) MOSFET has the potential of for operating with a very short channel structure. In addition, the SOI structure is necessary for a large on/off current ratio for short channel Schottky S/D MOSFETs. In previous work on μm-long gate Schottky S/D MOSFETs, the on/off current ratio of devices fabricated on a SIMOX substrate was 10^7 [80], whereas that of the bulk devices was 10^3 [55].

In this chapter, the characteristics of short channel Schottky S/D MOSFETs with metal gates fabricated by a simple process and self aligned silicide (salicide) process on a SIMOX substrate are shown. The large on/off current ratio was achieved using the SOI structure even with very short channels at room temperature. The fabrication process for 25 nm-long metal gate devices using electron beam lithography and a salicide process is discussed. Room temperature operation of n-type ($ErSi_2$) and p-type (PtSi) Schottky S/D MOSFETs was demonstrated. For the p-type Schottky S/D MOSFETs, the drivability was comparable with that of conventional MOSFETs.

3.2 Schottky Source/Drain MOSFETs Fabricated by Simple Process

In this section, the characteristics of Schottky S/D MOSFET fabricated by simple process are discussed. The results show large on/off ratio for very short channel Schottky S/D MOSFET using SOI structure.

3.2.1 Device Structure and Fabrication Process

Figure 3. 1 shows the device structure and the band diagram of the Schottky S/D MOS-FET fabricated on a SIMOX substrate. The SOI layer of the SIMOX wafer was p-type, 25 nm-thick and 30 Ωcm. The channel width was 1μm. The source and drain were Au. The gate insulator was 5 nm-thick SiO_2. The gate was Au/Cr. Holes are injected by gate-induced tunneling from the source through a 0.38 eV Au/Si Schottky barrier in the "on" state, while carriers remain confined by the Schottky barrier in the "off" state, as shown in Fig. 3. 1(b).

The fabrication process is shown in Fig. 3. 2. The device pattern was formed by electron beam lithography using PMMA resist. In this process, S/D and gate were formed with metal by lift-off process. The gate oxide was deposited by sputter without thermal oxidation. Using deposited gate oxide film, gate oxide and isolation spacer between S/D and gate can be formed by only one step. Therefore S/D metal can be chosen easily, because reaction between metal and Si can be suppressed due to low temperature process. In this study, source and drain was gold, because gold has low Schottky barrier and ultra-fine S/D formation is easy by evaporation and lift-off process. The gate was Au/Cr. Work function of Cr is 4.5 eV. Flat-band voltage V_{FB} (= ϕ_{Cr}–ϕ_{Si}) is estimated about –0.4 V, because work function of Si ϕ_{Si} (=χ_{Si}+E_g/2e–φ_B) is estimated

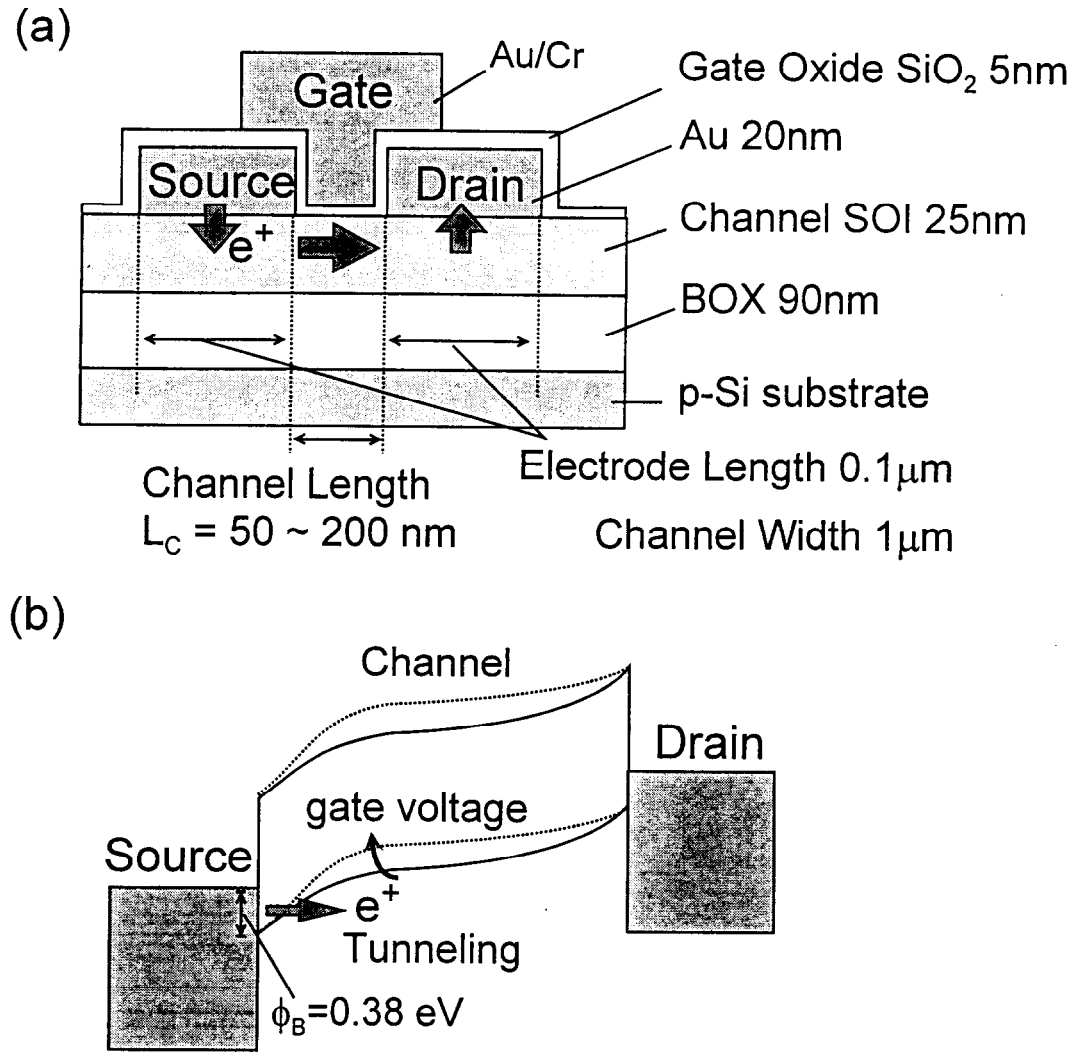


Figure 3.1: Device structure of Schottky S/D MOSFET fabricated by simple process. a) Cross-section structure and b) band diagram.

about 4.9 eV from the dopant concentration of the substrate. This value is not problematic for the operation and the flat-band voltage can be reduced to −0.1 V using an un-doped substrate. Therefore Cr is one of the ideal material for gate.

The detailed fabrication process steps are given as follows, where six steps are included. Figure 3. 3 shows a SEM view of the resulting Schottky S/D MOSFET.

- **Thinning of SOI layer**

  1. Cleaning by RCA process
  2. Oxidation of SOI layer at 1100 °C 5 hour

- **Formation of alignment marks for direct write lithography**

  1. e-beam lithography

     a. Cleaning by boiling acetone at 120 °C

     b. Baking dry at 120 °C 10 min.

     c. 100% PMMA spin coating

     1000 rpm. 1 sec. + 2000 rpm. 60 sec.

     d. Pre-baking for 60 min. at 170 °C

     e. Dose 800 $\mu C/cm^2$

     f. Development

     MIBK:IPA=1:3 45 sec., IPA 15 sec.

  2. e-beam evaporation

     100 nm-thick Au/10 nm-thick Cr evaporation

  3. Lift-off process

     Boiling acetone at 120 °C

- **Formation of source and drain**

  1. e-beam lithography

     a. Cleaning by boiling acetone at 120 °C

     b. Baking dry at 120 °C 10 min.

     c. 1:1 PMMA spin coating

     1000 rpm. 1 sec. + 2000 rpm. 60 sec.

     d. Pre-baking for 60 min. at 170 °C

     e. Dose 650 $\mu C/cm^2$

f. Development

MIBK:IPA=1:3 45 sec., IPA 15 sec.

2. e-beam evaporation

a. Removal of native oxide by 1 % BHF 15 sec.

b. 20 nm-thick Au evaporation

3. Lift-off process

Boiling acetone at 120 °C

- **Deposition of gate insulator**

1. Removal of native oxide by 1 % BHF 15 sec.
2. Baking for drying at 200 °C 10 min.
3. Deposition of 5 nm-thick SiO_2 by argon sputtering

- **Formation of gate**

1. e-beam lithography

a. Cleaning by boiling acetone at 120 °C

b. Baking dry at 120 °C 10 min.

c. 1:1 PMMA spin coating

1000 rpm. 1 sec. + 2000 rpm. 60 sec.

d. Pre-baking for 60 min. at 170 °C

e. Dose 650 $\mu C/cm^2$

f. Development

MIBK:IPA=1:3 45 sec., IPA 15 sec.

2. e-beam evaporation

30 nm-thick Au/10 nm-thick Cr evaporation

3. Lift-off process

Boiling acetone at 120 °C

- **Deposition of isolation layer and formation of contact holes**

  1. Baking dry at 200 °C 10 min.
  2. Deposition of 100 nm-thick SiO_2 by argon sputtering
  3. e-beam lithography
     - **a.** Cleaning by boiling acetone at 120 °C
     - **b.** Baking dry at 120 °C 10 min.
     - **c.** 1:1 PMMA spin coating
       1000 rpm. 1 sec. + 2000 rpm. 60 sec.
     - **d.** Pre-baking for 60 min. at 170 °C
     - **e.** Dose 650 $\mu C/cm^2$
     - **f.** Development
       MIBK:IPA=1:3 45 sec., IPA 15 sec.
     - **g.** Post-baking for 20 min. at 120 °C
  4. Formation of contact holes by wet etching using 7% BHF for 30 sec.
  5. Removal of PMMA by boiling acetone

- **Formation of external electrode pad**

  1. e-beam lithography
     - **a.** Cleaning by boiling acetone at 120 °C
     - **b.** Baking dry at 120 °C 10 min.
     - **c.** 100% PMMA spin coating
       1000 rpm. 1 sec. + 2000 rpm. 60 sec.
     - **d.** Pre-baking for 30 min. at 170 °C
     - **e.** 100% PMMA spin coating
       1000 rpm. 1 sec. + 2000 rpm. 60 sec.

f. Pre-baking for 60 min. at 170 °C

g. Dose 550 $\mu C/cm^2$

f. Development

MIBK:IPA=1:1 45 sec., IPA 15 sec.

2. e-beam evaporation

300 nm-thick Au/10 nm-thick Cr evaporation

3. Lift-off process

Boiling acetone at 120 °C

3.2.2 Measured Characteristics

The current-voltage characteristics were measured using a HP-4155 parameter analyzer. Figure 3. 4 shows the drain current curves with a common-source for 75 nm and 50 nm channel devices at room temperature. The saturation of the drain current becomes weaker with decreasing channel length because of the effect of the drain electric field on the source Schottky junction. At $V_{DS} = -1.0$ V and $V_{GS} = -2.0$ V, the drain current and the transconductance were –2.9 $\mu A/\mu m$ and 5 mS/mm for a 75 nm channel, and –7.6 $\mu A/\mu m$ and 30 mS/mm for a 50 nm channel. Although these values are smaller than those of conventional MOS-FETs, the drain current can be increased using a metal with a lower Schottky barrier, such as PtSi, [81] as mentioned in the previous chapter.

Subthreshold characteristics are shown in Fig. 3. 5. The on/off ratio decreases with decreasing channel length. The on/off ratios of 50, 75 and 200 nm channel devices at $V_{DS} = -1.0$ V were 750, 10^4 and 10^5, respectively. Relationship between subthreshold characteristics and drain voltage is shown in Fig. 3. 6. The on/off ratio becomes larger at low V_{DS}. The on/off ratio at $V_{DS} = -0.5$ V is 10 times larger than that at V_{DS}

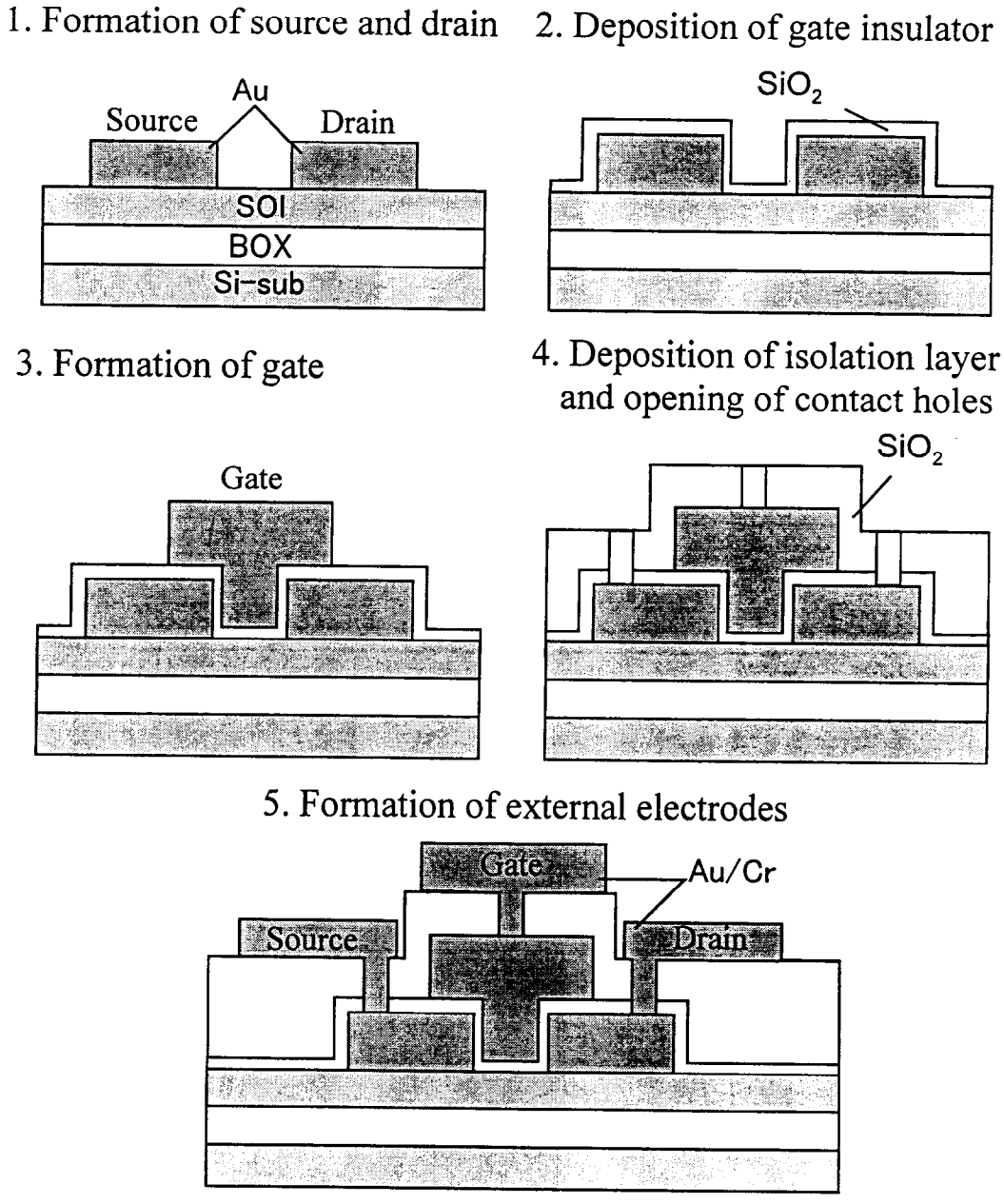


Figure 3.2: Simple fabrication process of Schottky S/D MOSFET.

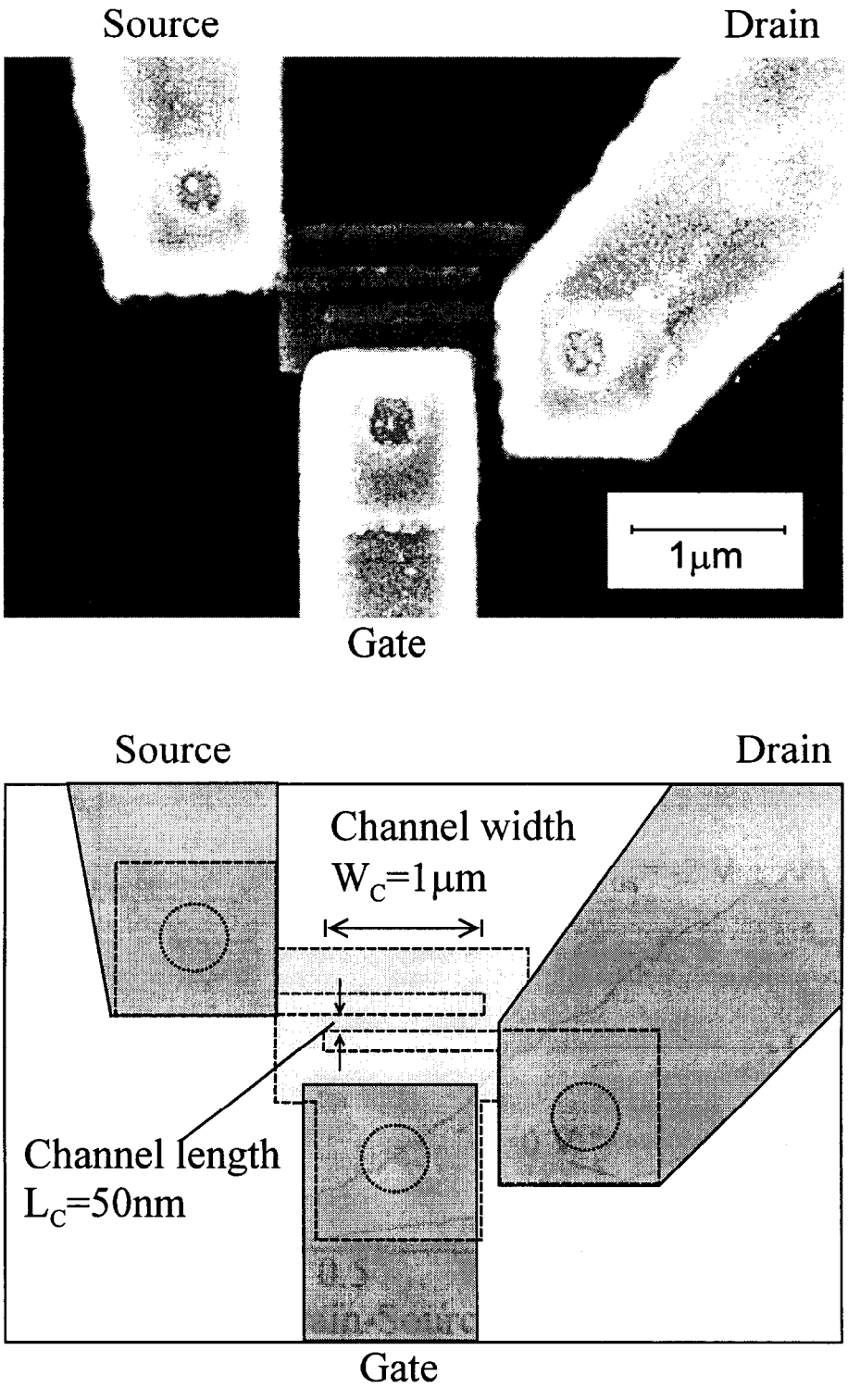


Figure 3.3: SEM plane view of Schottky S/D MOSFET fabricated by simple process.

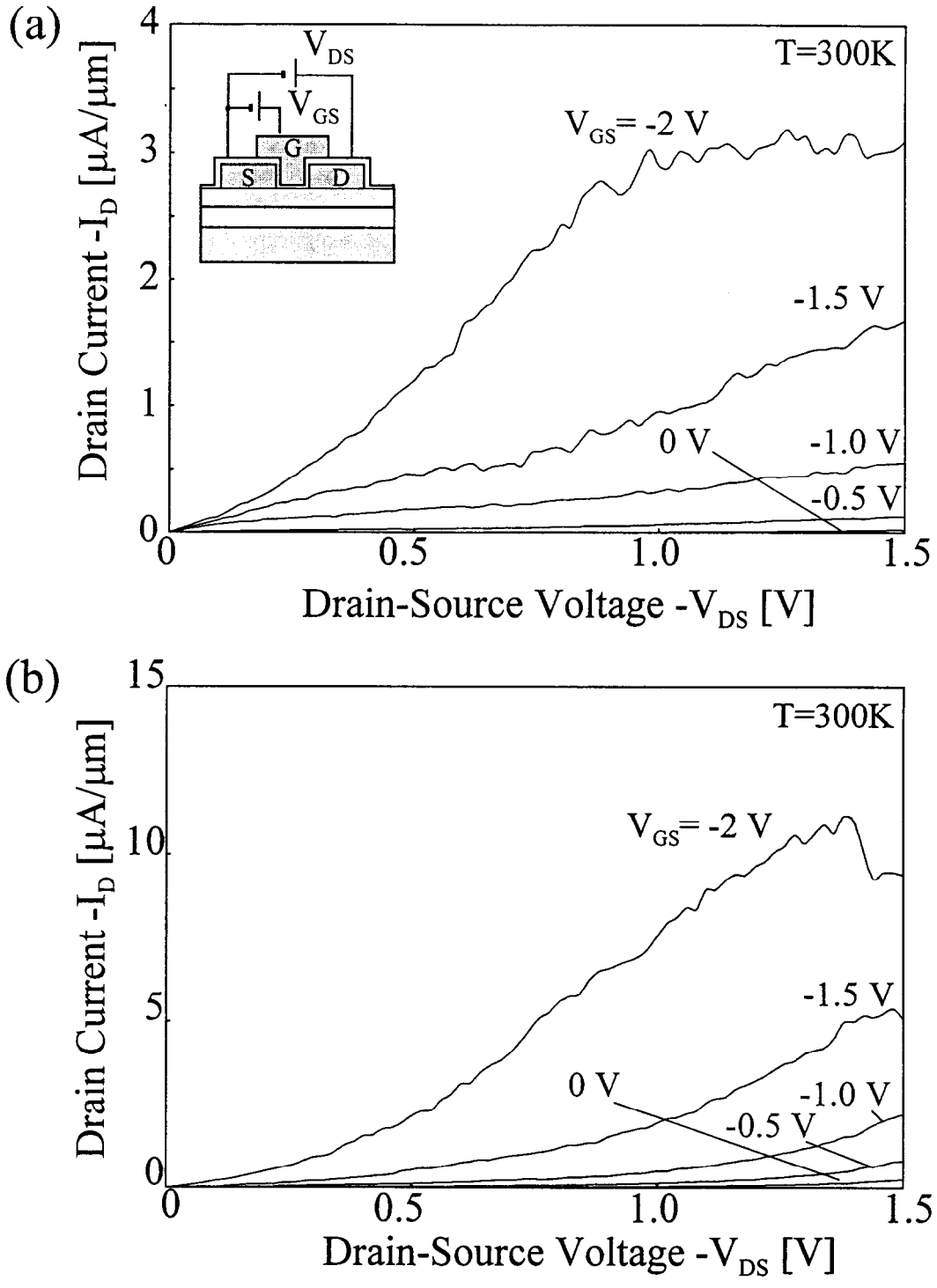


Figure 3.4: Drain current curves of the Schottky S/D MOS-FETs fabricated by simple process at room temperature. a) 75 nm channel device and b) 50 nm channel device

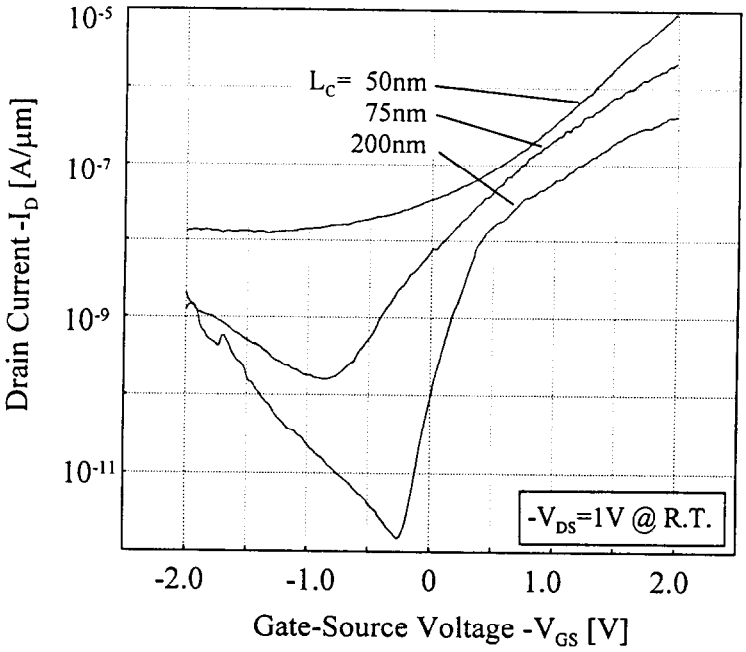


Figure 3.5: Subthreshold characteristics of the Schottky S/D MOS-FETs fabricated by simple process as a function of channel length.

= −1.0 V. The off current is determined by the drain-induced tunneling through the source Schottky junction, and can be decreased by decreasing the SOI thickness as the effect of drain voltage on the source Schottky junction becomes smaller. Dependence of subthreshold characteristics on SOI thickness is shown in Fig. 3. 7. The characteristics are for 75 nm-long channel devices. On/off ratio for 50 nm-thick SOI device was 10^3. On/off ratio becomes larger with decreasing SOI thickness. From these results, off current is suppressed using SIMOX substrate and on/off current ratio increases with decreasing of SOI thickness, because drain electric field toward the source becomes weak.

Relationship between subthreshold swing and channel length is shown in Fig. 3. 8. The subthreshold swing increases with decreasing channel length as in a conventional MOS-FET. The subthreshold swings of 50,

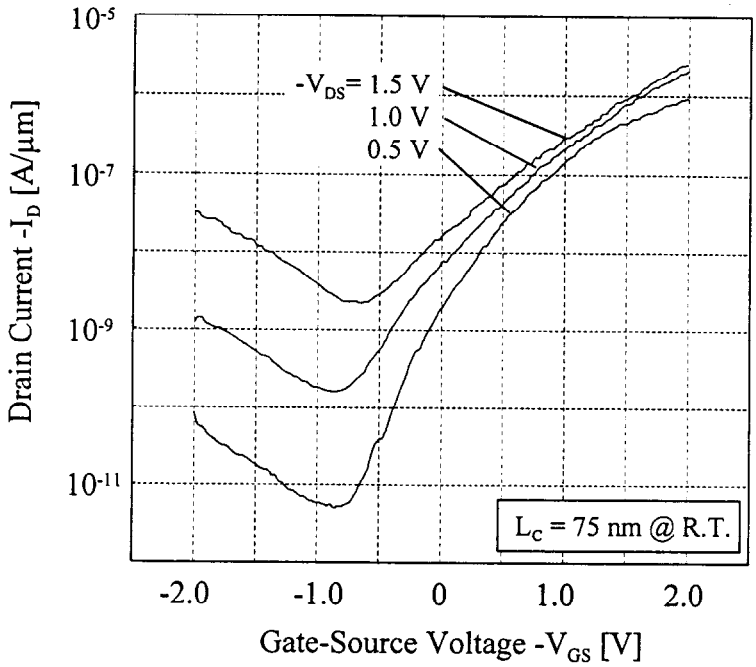


Figure 3.6: Subthreshold characteristics of the Schottky S/D MOS-FETs fabricated by simple process as a function of drain voltage V_{DS}.

75 and 200 nm channel devices at $V_{DS} = -1.0$ V were 740, 550 and 150 mV/dec, respectively. The subthreshold swing even with 200 nm-long channel was degraded. Because interfacial trapping density between gate oxide and SOI layer is large due to argon sputtering deposition. The interfacial trapping density can be reduced by argon and oxygen mixed sputtering and rapid thermal annealing [109, 110]. In addition, in this structure, the gap between the gate and source is large, as the source and drain were fabricated by evaporation only, without silicidation. Therefore subthreshold characteristics can be improved by the self-aligned silicide process of source and drain formation, as mentioned in Chap. 2, because the gap between gate and S/D junctions can be reduced using salicide process [55, 80, 81].

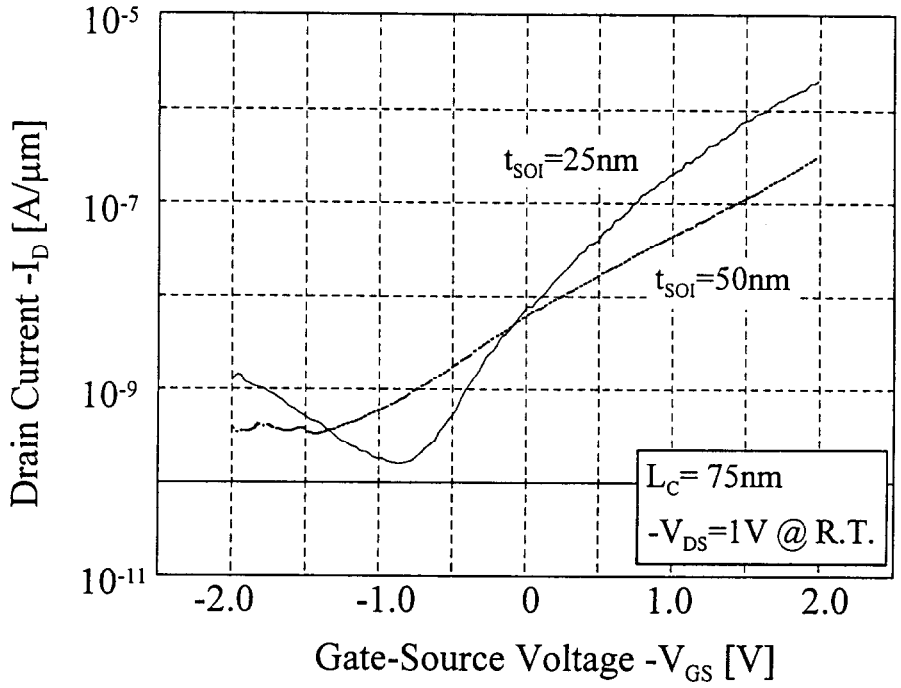


Figure 3.7: Subthreshold characteristics of the Schottky S/D MOS-FETs fabricated by simple process as a function of SOI layer thickness.

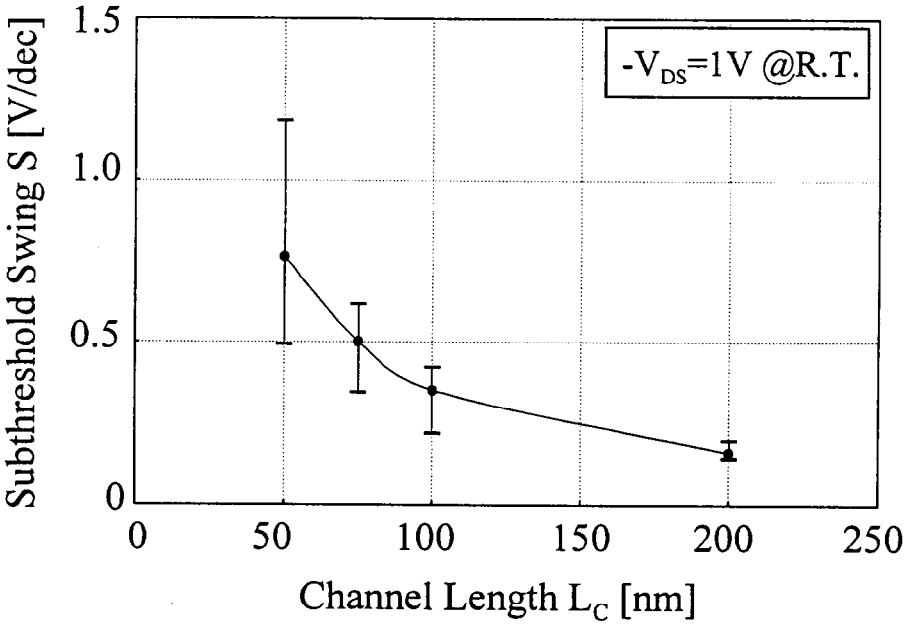


Figure 3.8: Relation between subthreshold swing and channel length of the Schottky S/D MOSFETs fabricated by simple process.

3.3 Schottky Source/Drain MOSFETs Fabricated by Salicide Process

3.3.1 Device Structure

In the previous section, the improvement of the on/off current ratio for very short channel devices on a SIMOX substrate was described. The drivability and subthreshold characteristics can be improved using salicide process, because the distance between the S/D and the gate becomes short and the Schottky barrier height of silicides is lower than pure metal [100, 101]. In this section, Schottky S/D MOSFETs fabricated by a salicide process is discussed. The device structure of n-type and p-type Schottky S/D MOSFETs is shown in Fig. 3. 9. Because they have low Schottky barrier heights, $ErSi_2$ and PtSi were chosen for the n-type and p-type S/Ds, respectively. The Schottky barrier heights of $ErSi_2$ and PtSi are ϕ_{Bn}=0.2 eV and ϕ_{Bp}=0.24 eV, respectively [102]–[106].

The gate metal used was Au/Cr, which was the same material used in the simple process. The gate oxide was 3.5 nm-thick SiO_2. The SIMOX substrates were the same as those used in the simple process. The SOI layer thickness was 25 nm. The junction depths were 10 and 25 nm for n-type and p-type devices, respectively. $ErSi_2$ MOSFETs were fabricated on a bulk Si substrate for comparison with the devices on SIMOX substrate. The dopant concentration of the bulk substrate was the same as that of the SIMOX substrate. The junction depth for the bulk device was 25 nm. The isolation layer was SiO_2 and the external electrode was Au/Cr.

3.3.2 Fabrication Process

Figure 3. 10–12 shows the salicide process used in this work. First, the gate oxide was grown by thermal oxidation. Then, the metal gate

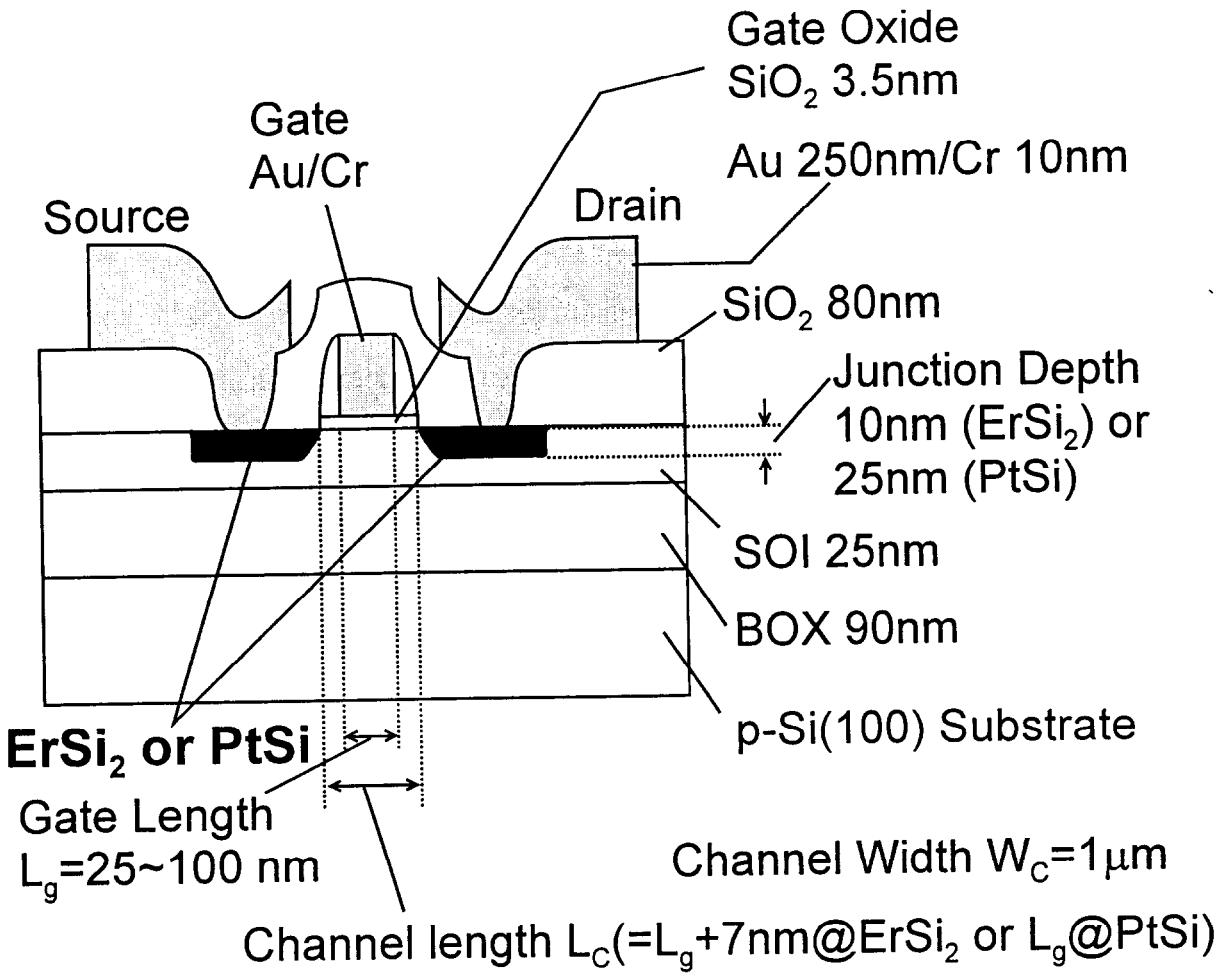


Figure 3.9: Device structure of Schottky S/D MOSFETs fabricated by a salicide process.

was formed by a lift-off process. A SiO_2 film was deposited by argon sputtering, and then the side-wall was formed by anisotropic reactive ion etching (RIE) in CF_4. Following this the S/D metal was deposited by e-beam evaporation and was then silicided at 400 °C in N_2 ambient by rapid thermal annealing. The un-reacted metals were selectively etched using nitric acid for Er and hot aquaregia for Pt [79, 111].

For fabrication of conventional MOSFETs with metal gates, melting of the gate and reaction between the gate and the gate oxide during the process can be problematic [32, 33]. Therefore metals, which have a high melting point, such as W and TiN are used for the gate material. However, the choice of gate material is easy for Schottky S/D MOSFETs, because the maximum temperature during the fabrication process is very low, due to the fact that no doping is required. The highest temperature during the process depends on the silicidation temperature, which is less than 650 °C for a conventional silicidation process. Moreover Cr is an ideal gate material, because Cr does not react with SiO_2 even at 1000 °C [112].

The accuracy of the self aligned process, which determines the distance between the S/D and the gate, depends on the cross-sectional shape of the gate. For the conventional MOSFET process, the gate is formed with poly-Si using dry etching. In this work, the gate was formed by a lift-off process. Therefore the cross-sectional shape depends on the resist shape. To suppress deformation of the resist during evaporation, the gate was formed with a Au/Cr multi-layered structure.

Silicides can be divided into two types. During silicidation, either the Si diffuses into the metal or the metal diffuses into the Si. Therefore each type of silicide has a different location of the Schottky interface [113].

The interface between the silicide and the Si remains at the interface between the evaporated metal and the Si for the Si-diffusion type silicide. For the metal-diffusion type silicide, the interface sinks into the Si layer. $ErSi_2$ is a Si-diffusion type silicide, and PtSi is a metal-diffusion type silicide. Silicidation of the total SOI layer thickness is the ideal structure for suppression of the short channel effect. However, it is difficult to form using $ErSi_2$, but is easily formed using PtSi. To sink the Schottky interface for the $ErSi_2$ MOSFETs, the SOI layer was selectively etched using tetra-methyl-ammonium-hydroxied (TMAH) [114]. Figure 3. 13 shows a cross-sectional SEM view of an $ErSi_2$ Schottky S/D MOSFET. The Schottky interface is located in the SOI layer. The (111) surface appears at the interface, because TMAH etches Si anisotropically. In addition, all of the SOI layer can not be etched to sink the interface, because Er reacts with SiO_2 [115]. Therefore the S/D junction for the $ErSi_2$ MOSFET was shallower than that for the PtSi MOSFET, because for the etching depth was equal to the junction depth of $ErSi_2$ S/D, whereas that of PtSi S/D was the SOI thickness. The gap between the gate and the S/D for the $ErSi_2$ MOSFET is controlled by the side-wall width. In this work, the gap was 3.5 nm ($L_C = L_g + 7$ nm). Figure 3. 14 shows a cross-sectional SEM view of a PtSi Schottky S/D MOSFET. The SOI layer was completely silicided. In addition, the channel was the same length as the gate.

The detailed fabrication process is given below in seven steps and is shown in Fig. 3. 10–12. Figure 3. 15 shows a SEM plan view of the resulting Schottky S/D MOSFET.

- **Oxidation of SOI layer for gate oxide**

  1. Cleaning by RCA process
  2. Oxidation of SOI layer at 1100 °C for 5 hour for thinning.
  3. Removal of oxide by 7 % BHF for 4 min.
  4. Oxidation of SOI layer at 800 °C for 10 min. to grow 3.5 nm thick oxide

- **Formation of alignment marks for direct write lithography**

  1. e-beam lithography

     a. Cleaning in boiling acetone at 120 °C

     b. Baking dry at 120 °C 10 min.

     c. 100% PMMA spin coating

     1000 rpm. 1 sec. + 2000 rpm. 60 sec.

     d. Pre-baking for 60 min. at 170 °C

     e. Dose 800 $\mu C/cm^2$

     f. Development

     MIBK:IPA=1:3 45 sec., IPA 15 sec.

  2. e-beam evaporation

     100 nm-thick Au/15 nm-thick Cr evaporation

  3. Lift-off process

     Boiling acetone at 120 °C

- **Formation of Gate**

  1. e-beam lithography

     a. Cleaning in boiling acetone at 120 °C

     b. Baking dry at 120 °C 10 min.

c. 1:1 PMMA spin coating

1000 rpm. 1 sec. + 2000 rpm. 60 sec.

d. Pre-baking for 60 min. at 170 °C

e. Dose 650 $\mu C/cm^2$

f. Development

MIBK:IPA=1:3 45 sec., IPA 15 sec.

2. e-beam evaporation

23 nm-thick Au/12 nm-thick Cr/23 nm-thick/ 12 nm-thick Cr evaporation

3. Lift-off process

Boiling acetone at 120 °C

- **Formation of side-wall**

1. Baking dry at 400 °C 10 min.
2. Deposition of 15 nm-thick SiO_2 by argon sputtering
3. Anisotropic etching using RIE

a. CF_4 1 Pa, 150 W, 35 sec.

b. O_2 10 Pa, 30 W, 60 sec.

- **Formation of source and drain**

1. e-beam lithography

a. Cleaning in boiling acetone at 120 °C

b. Baking dry at 120 °C 10 min.

c. 1:1 PMMA spin coating

1000 rpm. 1 sec. + 2000 rpm. 60 sec.

d. Pre-baking for 60 min. at 170 °C

e. Dose 650 $\mu C/cm^2$

f. Development

MIBK:IPA=1:3 45 sec., IPA 15 sec.

2. Removal of oxide by 1 % BHF for 10 sec.

3. Anisotropic etching of SOI layer for $ErSi_2$ S/D

by 2.4 % TMAH at 40 °C 20 sec.

4. e-beam evaporation

25 nm-thick Er or 15 nm-thick Pt evaporation

5. Lift-off process

Boiling acetone at 120 °C

6. Silicidation by annealing in a nitrogen ambient at 400 °C

For $ErSi_2$ 10 min. For PtSi 1 min.

7. Removal of un-reacted metal

For Er : HNO_3:H_2O = 1:5 at R.T. 15 sec.

For Pt : HCl:HNO_3:H_2O = 3:2:1 at 50 °C 20 sec.

- **Deposition of isolation layer and formation of contact windows**

1. Baking dry at 300 °C 10 min.

2. Deposition of 80 nm-thick SiO_2 by argon sputtering

3. e-beam lithography

a. Cleaning in boiling acetone at 120 °C

b. Baking dry at 120 °C 10 min.

c. 1:1 PMMA spin coating

1000 rpm. 1 sec. + 2000 rpm. 60 sec.

d. Pre-baking for 60 min. at 170 °C

e. Dose 650 $\mu C/cm^2$

f. Development

MIBK:IPA=1:3 45 sec, IPA 15 sec.

g. Post-baking for 20 min. at 120 °C

4. Formation of contact windows by wet etching using 7% BHF for 30 sec.

5. Removal of PMMA in boiling acetone

- **Formation of external electrode pads**

1. e-beam lithography

a. Cleaning in boiling acetone at 120 °C

b. Baking dry at 120 °C 10 min.

c. 100% PMMA spin coating

1000 rpm. 1 sec. + 2000 rpm. 60 sec.

d. Pre-baking for 30 min. at 170 °C

e. 100% PMMA spin coating

1000 rpm. 1 sec. + 2000 rpm. 60 sec.

f. Pre-baking for 60 min. at 170 °C

g. Dose 550 $\mu C/cm^2$

f. Development

MIBK:IPA=1:1 45 sec., IPA 15 sec.

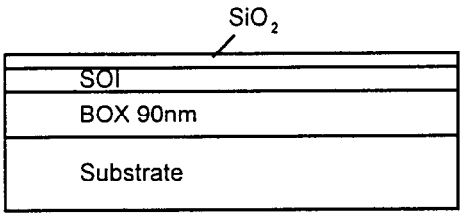
2. e-beam evaporation

300 nm-thick Au/10 nm-thick Cr evaporation

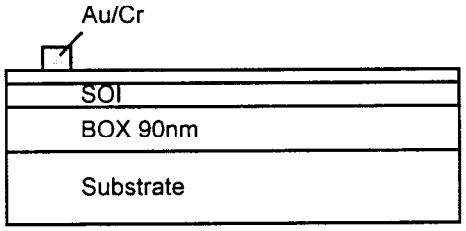
3. Lift-off process

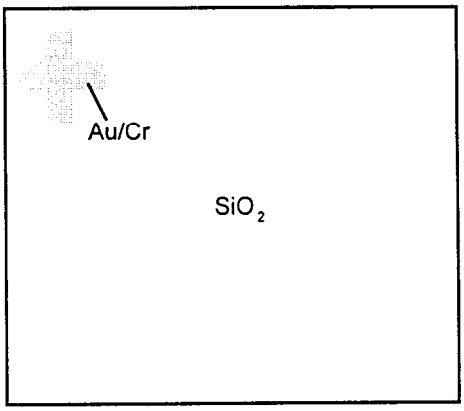
Boiling acetone at 120 °C

1. Oxidation of SOI for gate oxide

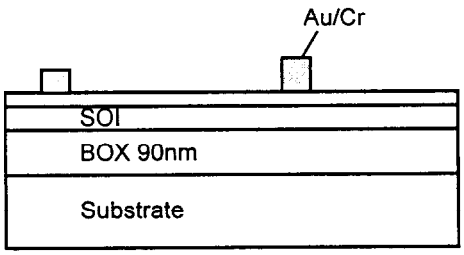


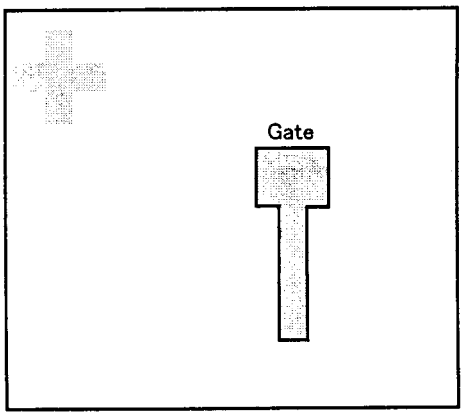
2. Formation of alignment marks for direct write lithography



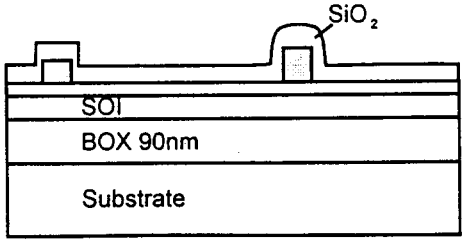


3. Formation of gate





4. Deposition of SiO_2 for sidewall



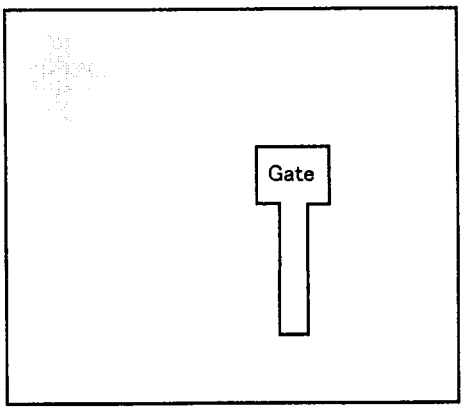
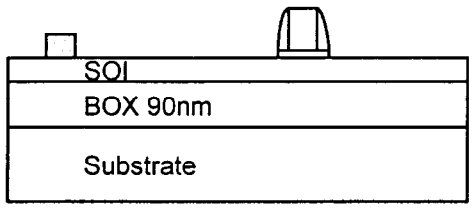
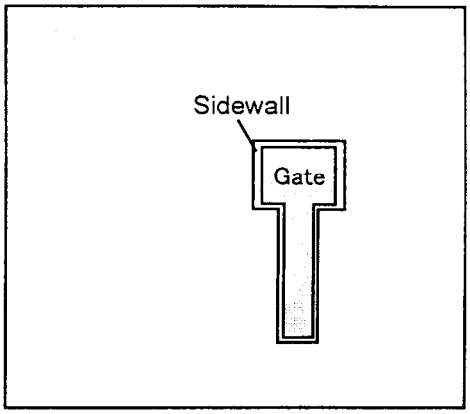


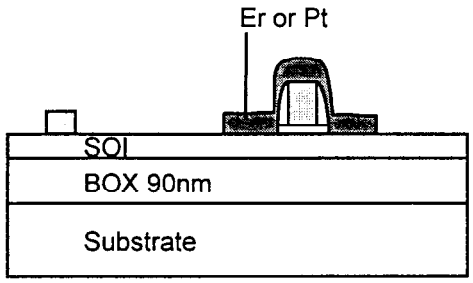
Figure 3.10: Fabrication process with self aligned silicidation of Schottky S/D MOSFET.

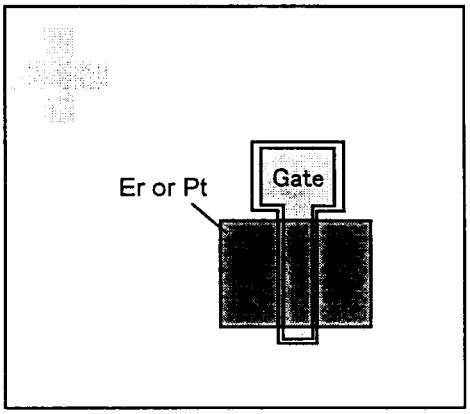
5. Formation of sidewall



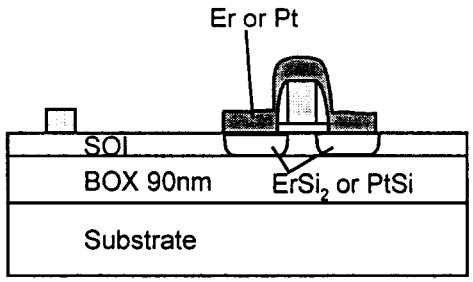


6. Evaporation of source/drain metal





7. Silicidation



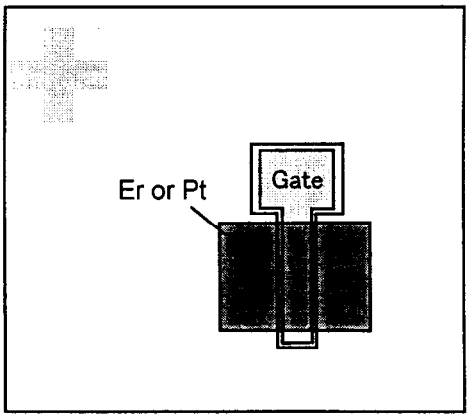
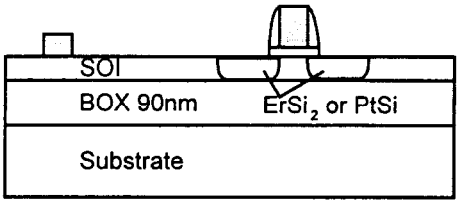
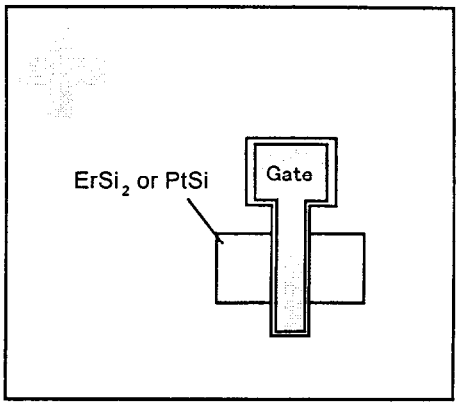


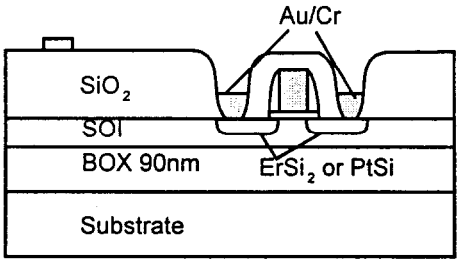
Figure 3.11: Fabrication process with self aligned silicidation of Schottky S/D MOSFET.

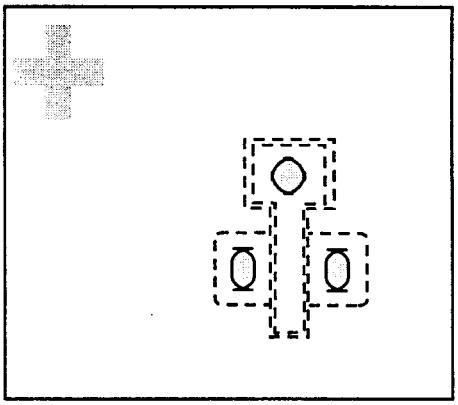
8. Removal of un-reacted metal



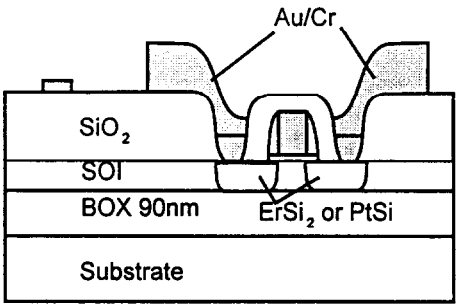


9. Deposition of isolation layer and opening of contact windows





10. Formation of external electrodes



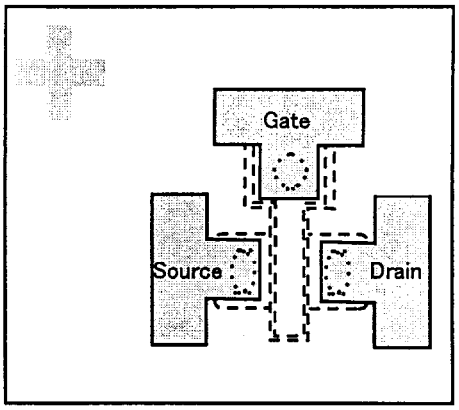


Figure 3.12: Fabrication process with self aligned silicidation of Schottky S/D MOSFET.

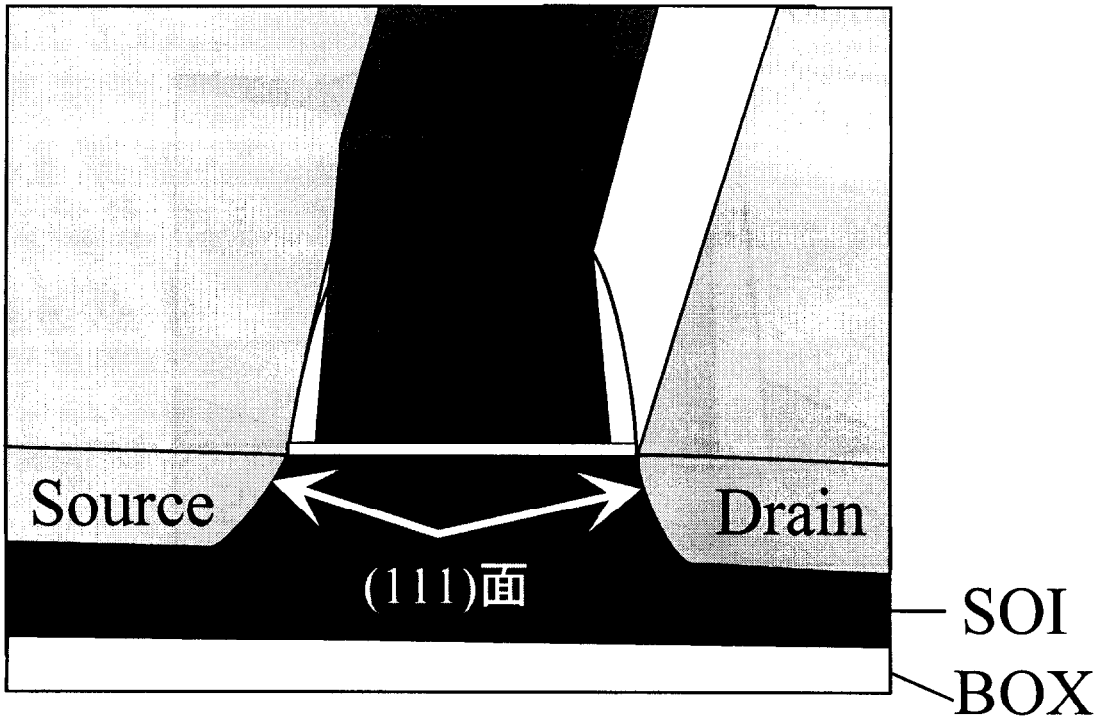


Figure 3.13: Cross-sectional SEM view of $ErSi_2$ Schottky S/D MOSFET.

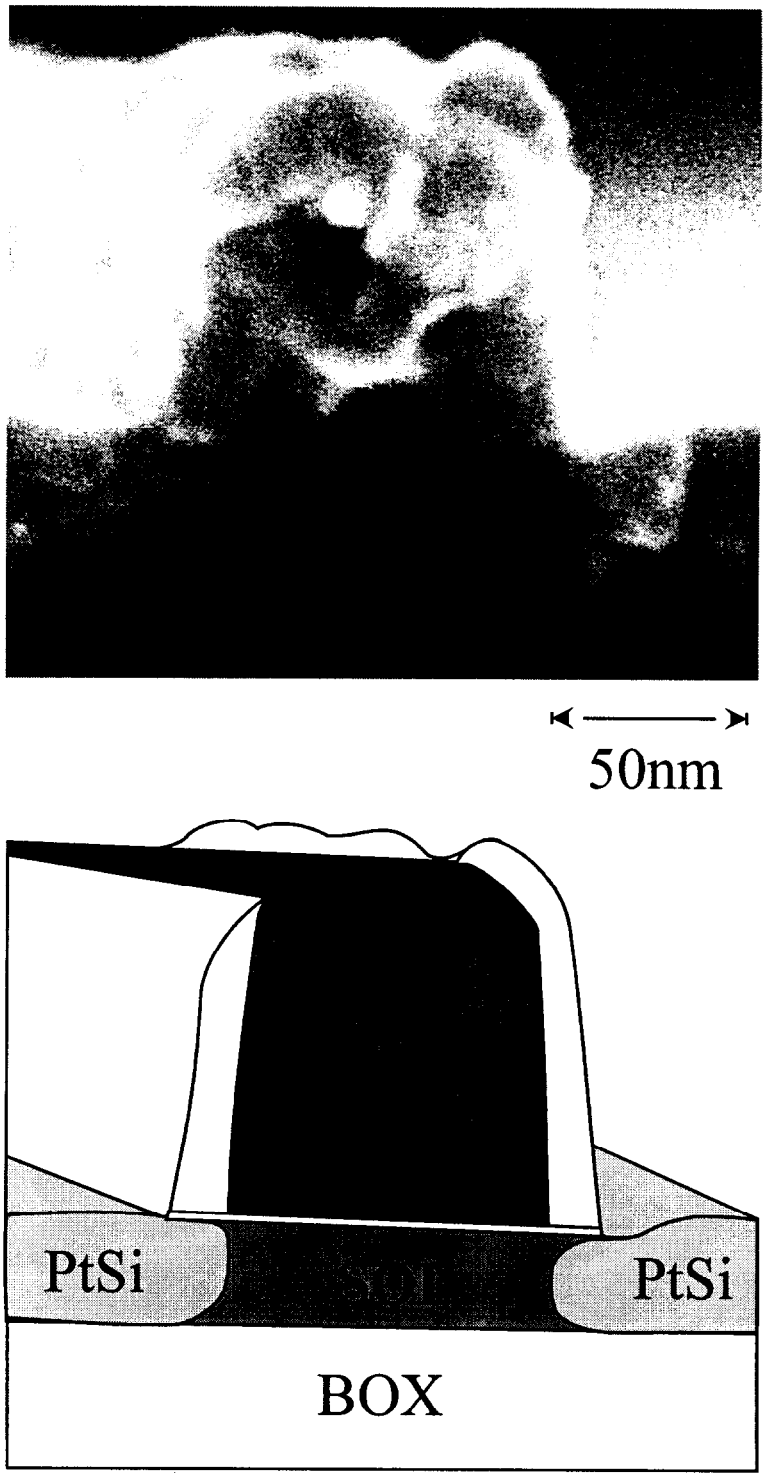


Figure 3.14: Cross-sectional SEM view of PtSi Schottky S/D MOSFET.

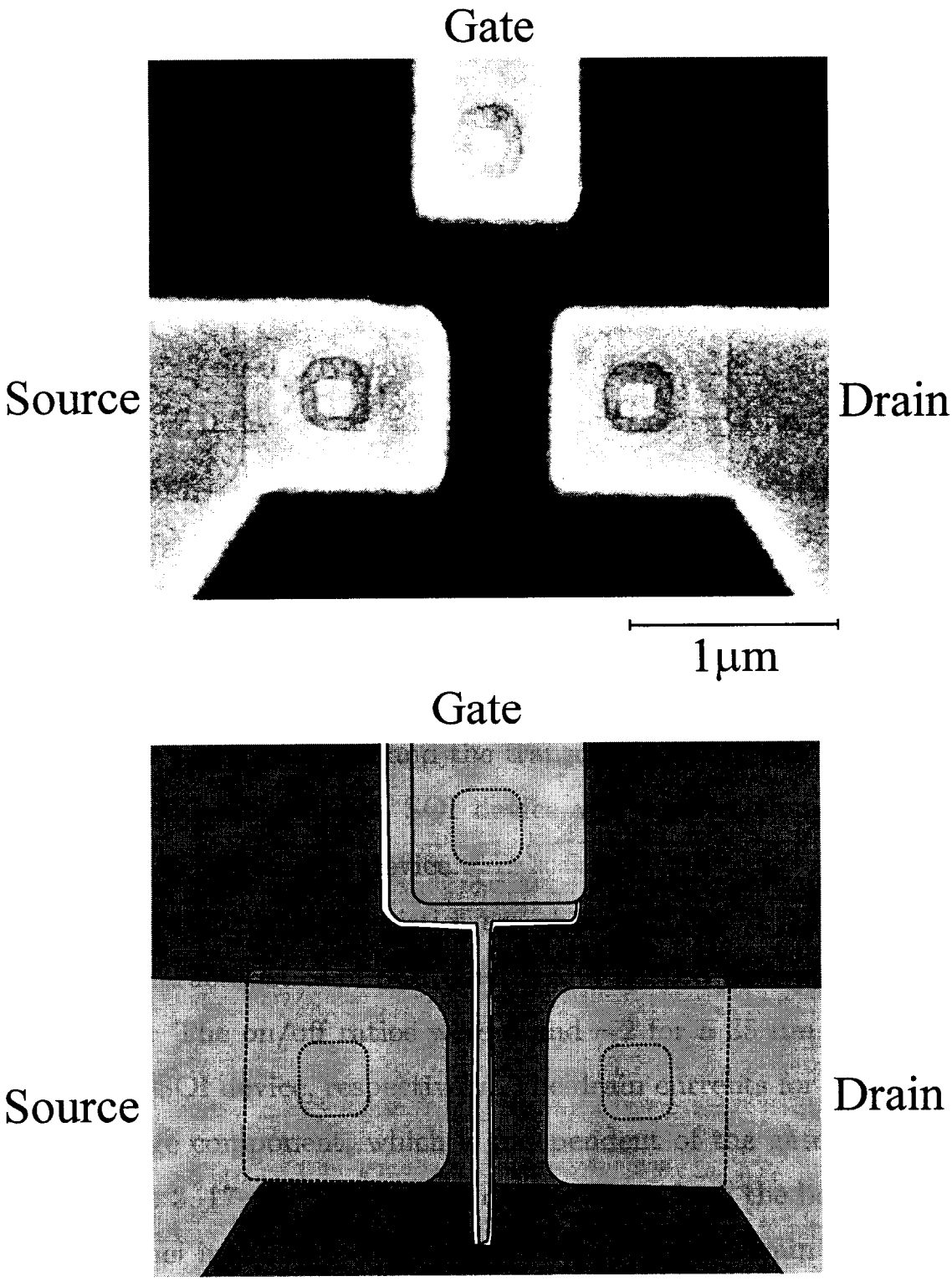


Figure 3.15: SEM plane view of Schottky S/D MOSFET fabricated by salicide process.

3.3.3 Measured Characteristics

A. n-type $ErSi_2$ Schottky Source/Drain MOSFETs

Figure 3. 16 shows common source drain curves of a n-type $ErSi_2$ Schottky S/D MOSFET on bulk Si. The measurements were made at room temperature and for various gate-source voltage V_{GS}. At $V_{DS} = V_{GS} = 2$ V, the drain current and the transconductance of the 35 nm device were 45 μA/μm and 20 mS/mm, respectively. The equivalent values for 55 nm device were 37μA/μm and 15 mS/mm.

Figures 3. 17–18 show common source drain curves of an $ErSi_2$ Schottky S/D MOSFET on a SIMOX substrate. The measurements were made at room temperature and with various gate-source voltages V_{GS}. The saturation of the drain current becomes weaker with decreasing gate length. At $V_{DS} = V_{GS} = 2$ V, the drain current was 75 μA/μm and the transconductance was 9.5 mS/mm for the 25 nm device. For the 55 nm device the drain current was 62 μA/μm and the transconductance was 11 mS/mm. The transconductance of the SOI device was smaller than that of an equivalent gate length bulk device.

The subthreshold characteristics are shown in Fig. 3. 19. The solid lines show characteristics of SOI devices and dashed lines show those of bulk devices. The on/off ratios were 6 and $\sim$2 for a 35 nm bulk device and a 25 nm SOI device, respectively. The drain currents for SOI devices have a leakage component, which is independent of the gate voltage, as shown in Fig. 3. 17–18. The leakage current flows from the bottom of the source/channel junction to the bottom of the channel/drain junction.

Figure 3. 20 shows theoretical subthreshold characteristics of $ErSi_2$ Schottky S/D MOSFETs together with the experimental results. The gate length in each case was 55 nm. Comparison between theory and ex-

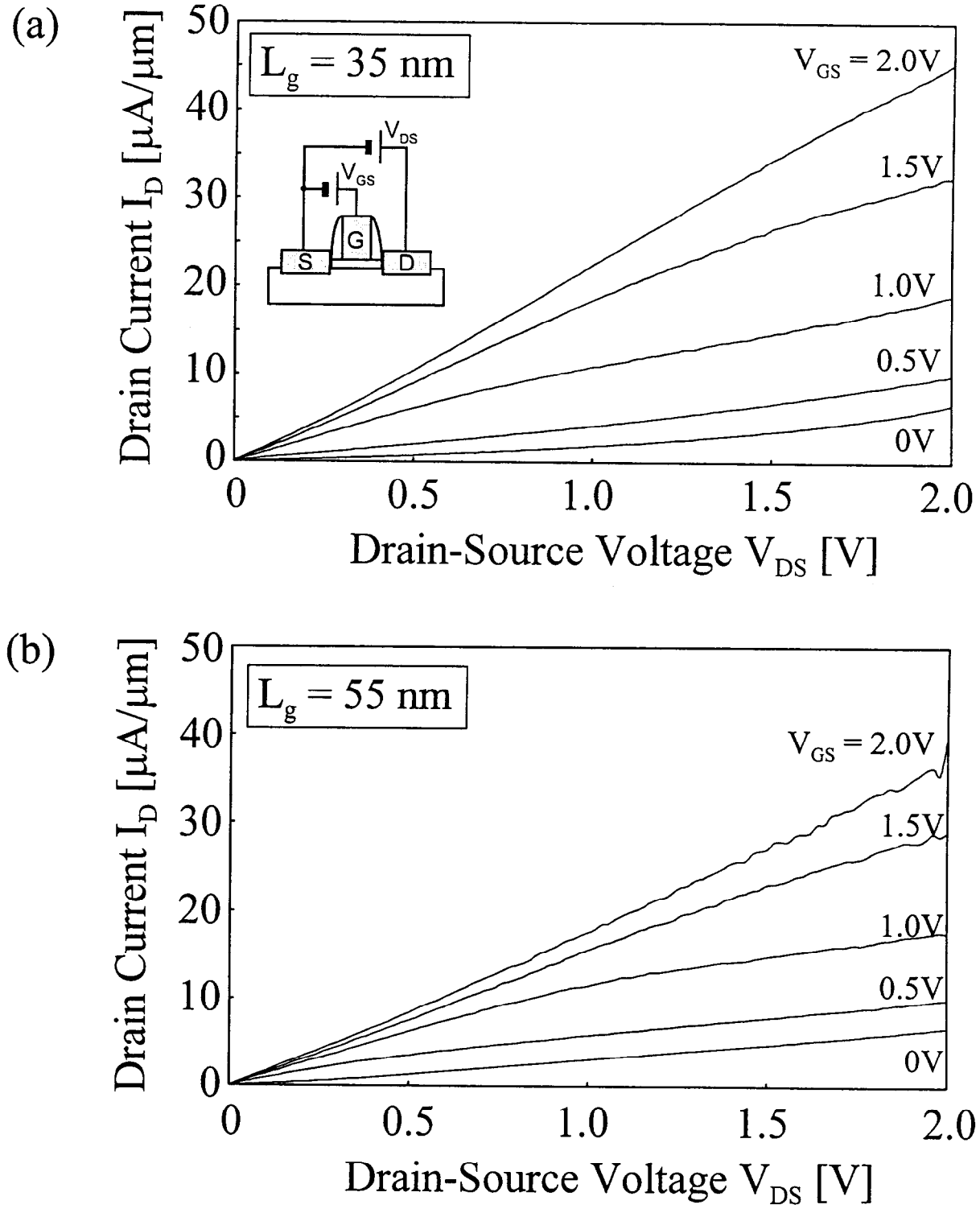


Figure 3.16: Common source drain curves for various gate-source voltages V_{GS} of an $ErSi_2$ Schottky S/D MOSFET on bulk Si. (a) 35 nm-long gate device and (b) 55 nm-long gate device

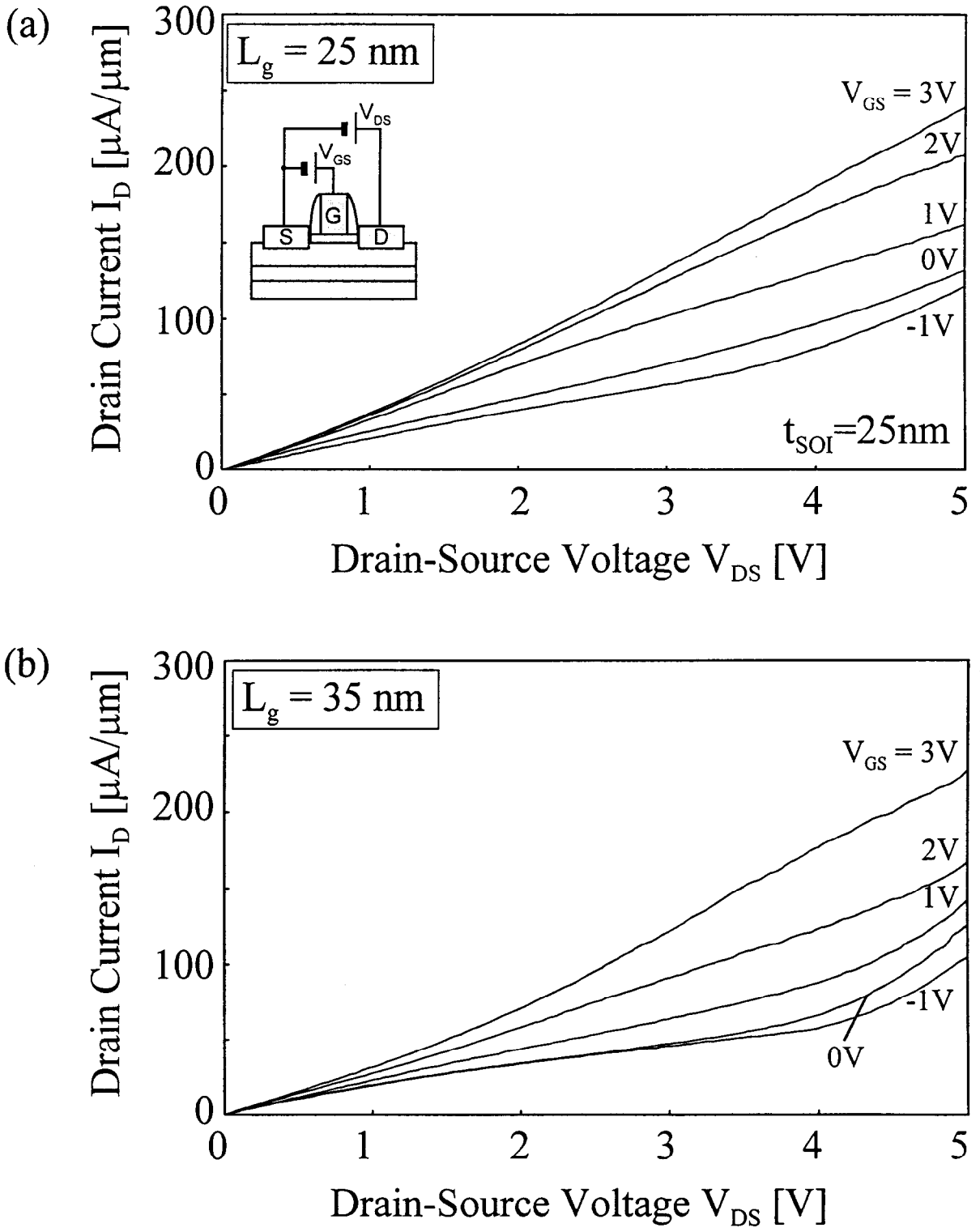


Figure 3.17: Common source drain curves for various gate-source voltages V_{GS} of an $ErSi_2$ Schottky S/D MOSFET on a SIMOX substrate. (a) 25 nm-long gate device and (b) 35 nm-long gate device

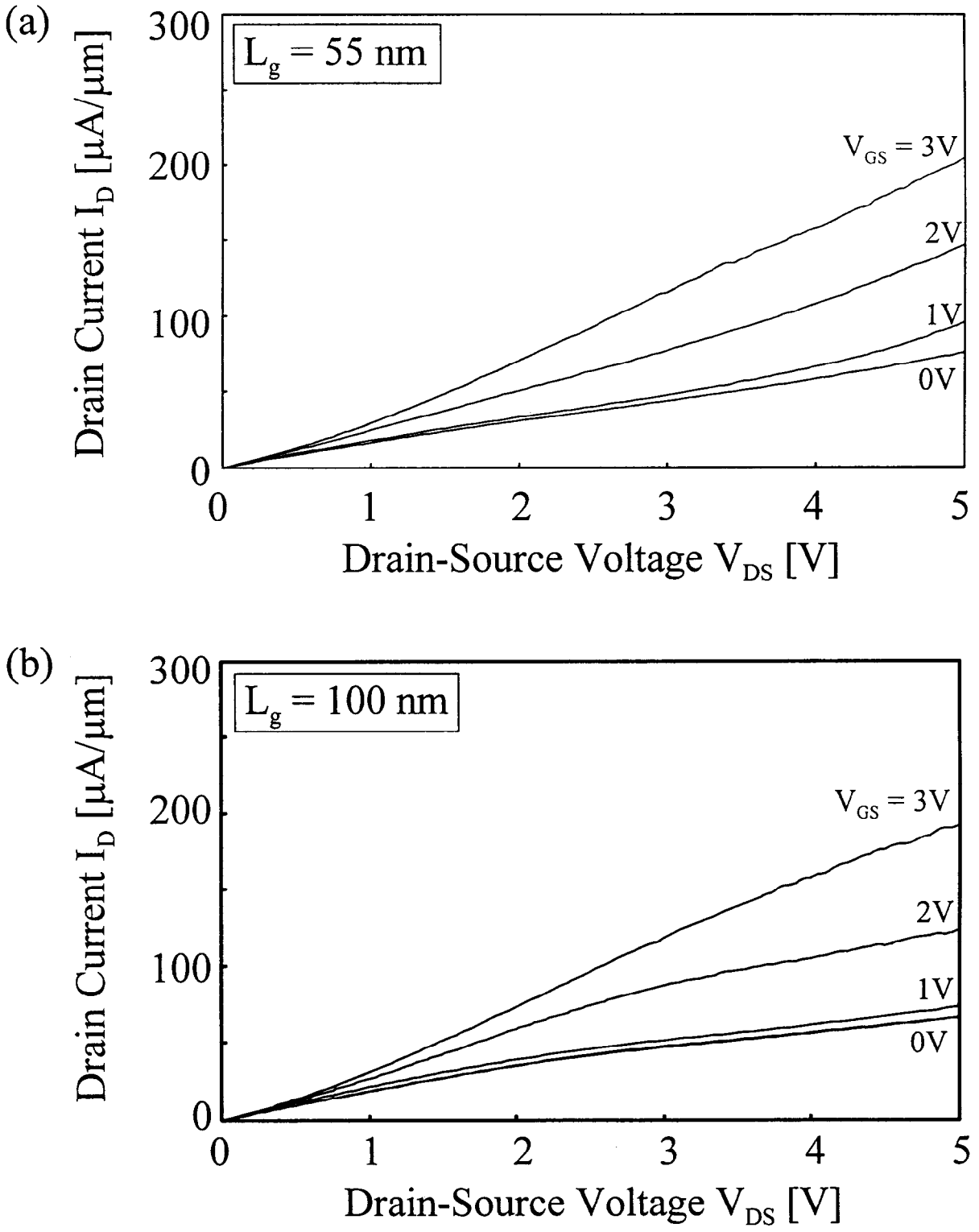


Figure 3.18: Common source drain curves for various gate-source voltages V_{GS} of an $ErSi_2$ Schottky S/D MOSFET on a SIMOX substrate. (a) 55 nm-long gate device and (b) 100 nm-long gate device

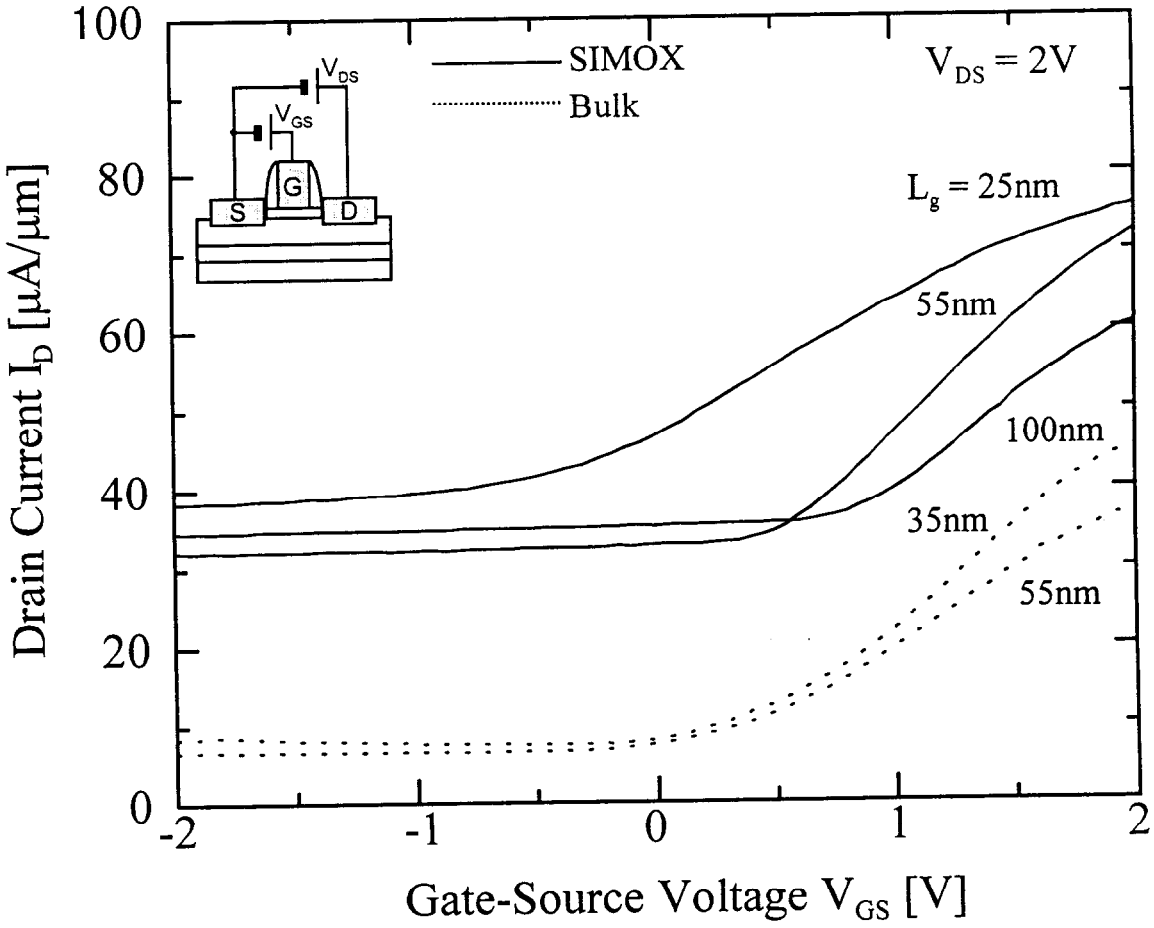


Figure 3.19: Subthreshold characteristics of Schottky S/D MOSFETs on a SIMOX substrate (solid lines) and bulk Si (dashed lines).

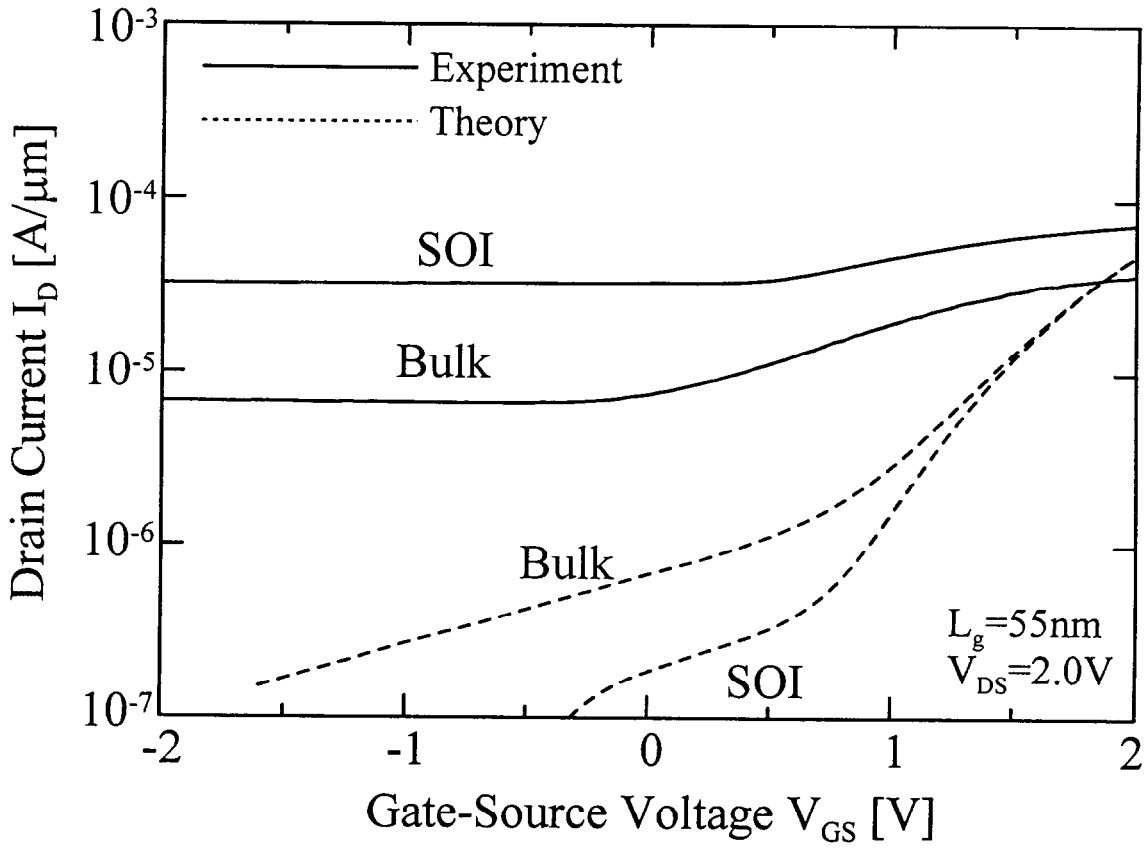


Figure 3.20: Experimental (solid lines) and theoretical (dashed lines) subthreshold characteristics of the $ErSi_2$ Schottky S/D MOSFETs.

periment shows that the transconductance and on/off ratio were degraded for fabricated devices.

The degradation of the characteristics for the fabricated devices is discussed below. The poor transistor characteristics were a results of degradation of the S/D Schottky junctions. Figure 3. 21 shows the current-voltage characteristics of the $ErSi_2$/p-Si Schottky junction in a Schottky S/D MOSFET on bulk Si. Although the characteristics show clear rectification, the n-factor and the on/off ratio were 3 and 100, respectively. The decreased transconductance and on/off ratio and increased subthreshold swing can be explained. On the basis of these values, it is hypothesized

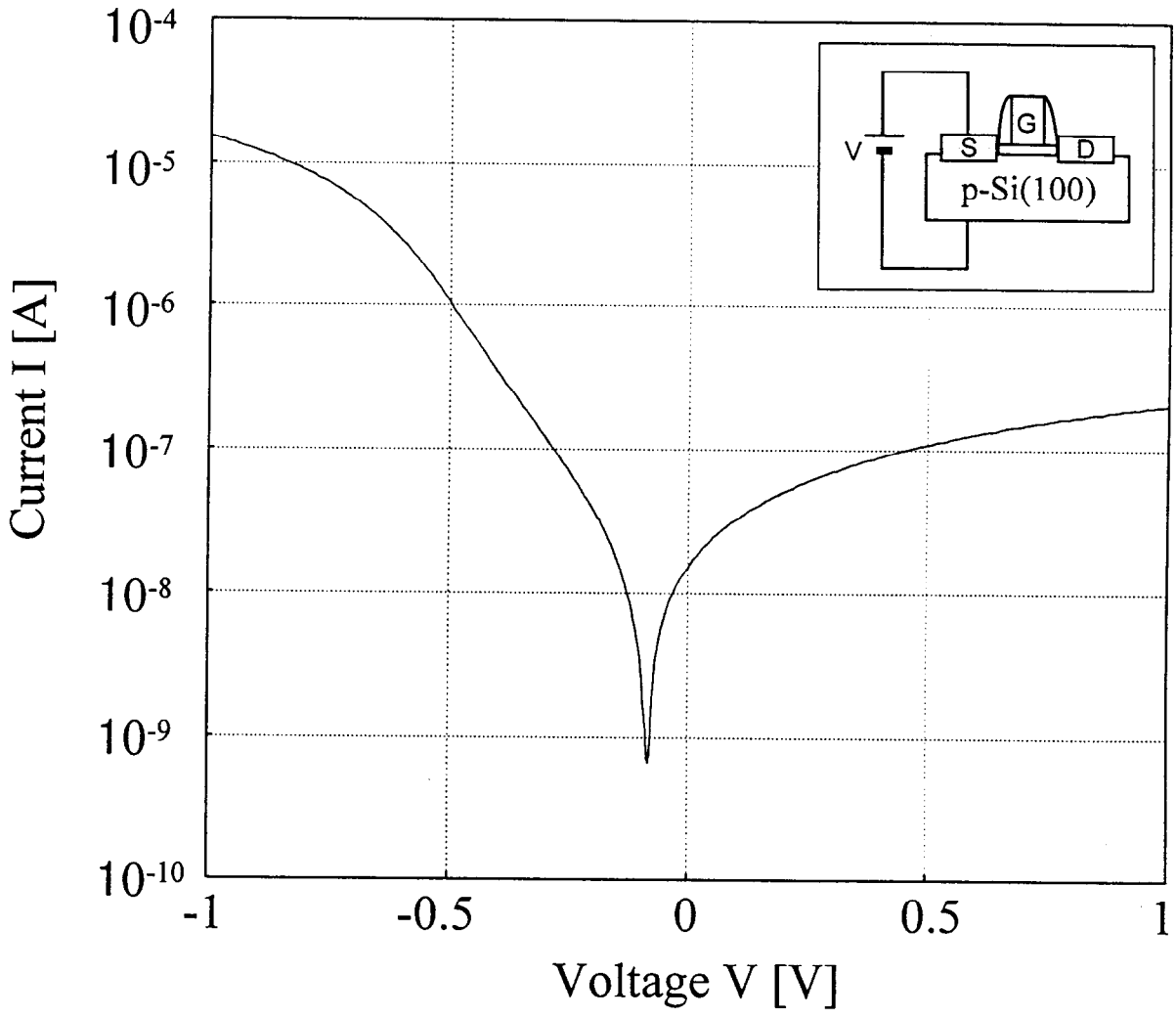


Figure 3.21: The current-voltage characteristics of an $ErSi_2$/Si Schottky junction on a bulk substrate.

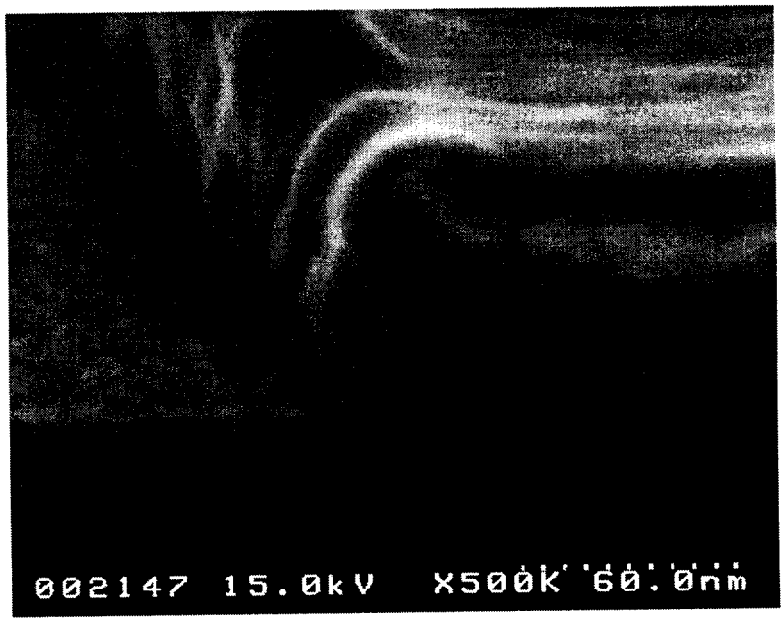
that there were many interface traps at the $ErSi_2$ Schottky junction and that the high density of these traps was due to interface roughness and metallic contamination. The roughness was a result of the etching to sink the interface and the RIE in CF_4 used to form side-walls.

Figures 3. 22 (a) and (b) show SEM images of the etched SOI surface after etching 5 nm and 30 nm, respectively. Figure 3. 22 (a) shows the condition of the Schottky interface of the SOI device and (b) is similar to that of the bulk device. The rough surface was observed in the SEM.

From these observations, the surface roughness is seen to decrease with increasing etching depth. The deep S/D junctions explain why the bulk device has better switching than the SOI device.

To suppress surface roughness and metallic contamination, an improvement in the cleaning process before evaporation of the S/D metal is necessary. CF_4 RIE generates surface damage and carbon and metallic contamination [116, 117]. The damaged layer and carbon contamination can be removed by a sacrificial oxidation [118, 119]. Moreover, the metallic contamination can be removed by a wet chemical cleaning process [120, 121]. Finally, the junction interface is formed in the SOI layer by etching using TMAH. However, it is difficult to form the nm-deep junction due to thinning of the SOI layer in the sacrificial oxidation process. The junction depth can be controlled by the process shown in Fig. 3. 23. After sacrificial oxidation and removal of metallic contamination, the SOI layer is completely etched. Then Si is evaporated. The junction depth can be controlled by the thickness of the evaporated Si, because the junction interface is at the evaporated Si surface. Thus, the characteristics of the n-type $ErSi_2$ Schottky S/D MOSFET can be improved by changing the S/D formation process.

(a)



(b)

Figure 3.22: SEM views of the SOI surface after RIE. (a) after 5 nm etching and (b) after 30 nm etching.

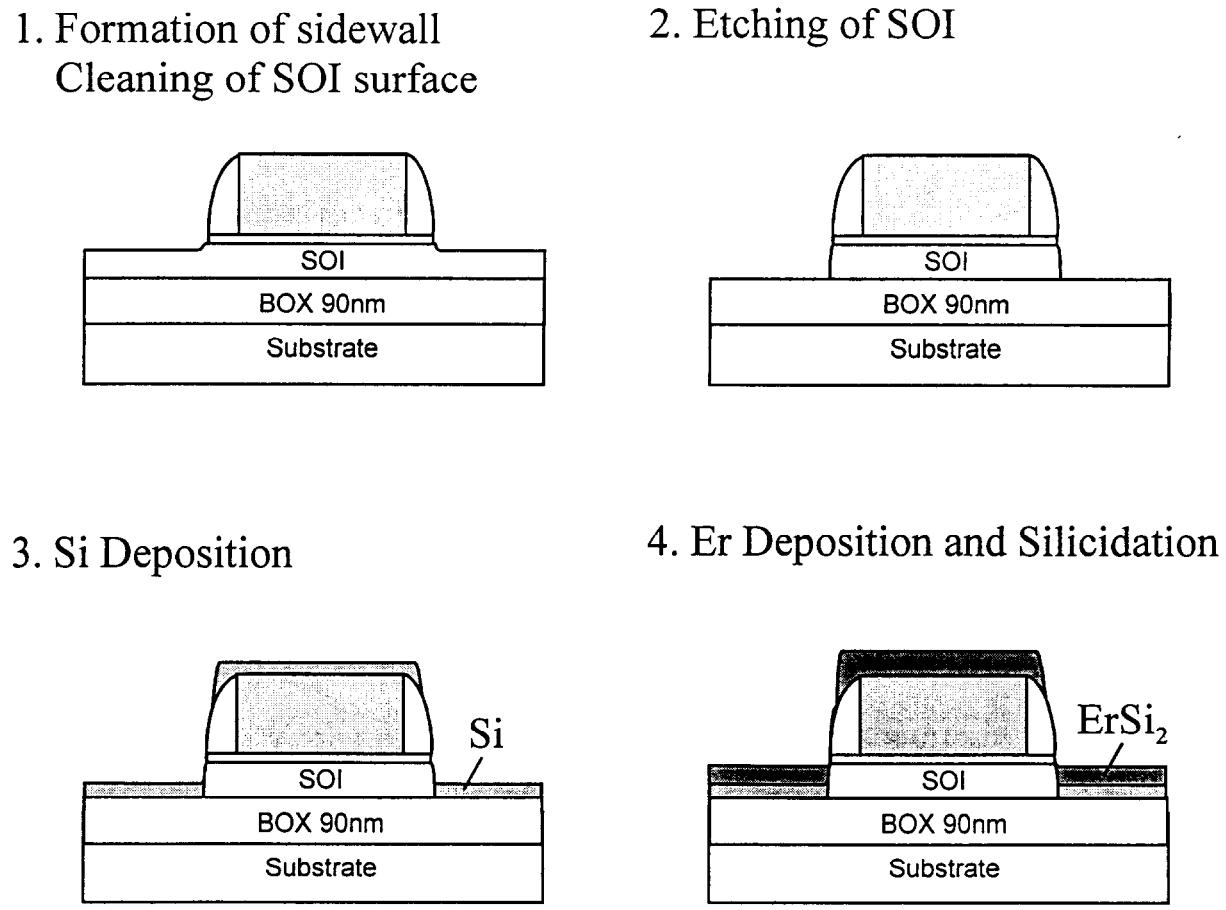


Figure 3.23: New formation process of $ErSi_2$ S/D junctions.

B. p-type PtSi Schottky Source/Drain MOSFETs

Figure 3. 24 shows the common source drain curves of p-type PtSi Schottky S/D MOSFETs for various gate-source voltages V_{GS}. The characteristics show room temperature operation even with a 35 nm-long gate. The saturation of the drain current becomes weaker with decreasing gate length. At $V_{DS} = V_{GS} = -1.5$ V, the drain current and the transconductance were -176 μA/μm and 390 mS/mm respectively for a 35 nm-long channel device.

The dependence of the characteristics on the gap between the gate and the S/D junctions for PtSi Schottky S/D MOSFETs is shown in Fig. 3. 25. The gaps were (a) 9 nm (L_C=L_g+18 nm) and (b) zero (L_C=L_g). The gate length was 100 nm. The drain current increases with decreasing gap, as mentioned in the previous chapter. In addition, the turn-on drain voltage is reduced with the gap. These experimental results show that an overlap between the gate and the S/D is necessary for good characteristics.

Subthreshold characteristics of PtSi Schottky S/D MOSFETs are shown in Fig. 3. 26. The off-current increases with decreasing gate length. At $V_{DS} = -1.5$ V, the on/off ratios of 56 and 35 nm-long gate devices were 3×10^4 and 420, respectively. The large on/off ratio was achieved by suppression of the leakage due to complete silicidation of the SOI layer.

A comparison between theoretical and experimental characteristics for 56 nm-long gate devices is shown in Fig. 3. 27. The experimental drain current was larger than the theoretical value, because the cross sectional shape of the S/D junction for the fabricated devices was different from that assumed in the calculation. For the fabricated device, the S/D junctions were round, as shown in Fig. 3. 14, whereas the junction in the calculation was assumed to be straight. At positive gate biasses,

the drain current increased with gate bias. A possible explanation is that electrons were injected from the drain through the interfacial traps. The roughness of the PtSi/Si junction may be small, because PtSi is a metal-diffusion type silicide. However, interfacial traps generate metallic contamination by RIE. Therefore the leakage current can be reduced by a cleaning process after RIE.

The relationship between the subthreshold swing and the gate length is shown in Fig. 3. 28. The subthreshold swing increases with decreasing gate length. The subthreshold swings of PtSi Schottky S/D MOSFETs were smaller than those of devices fabricated with a simple process. The subthreshold characteristics were improved by thermal oxidation to reduce interfacial trap between gate oxide and channel.

A comparison between a PtSi Schottky S/D MOSFET on a SIMOX substrate, on bulk silicon [81] and conventional p-MOSFETs on bulk [8] and SOI substrates [99] is shown in Table 3. 1. For a PtSi Schottky S/D MOSFET fabricated on a SIMOX substrate, a transconductance comparable with conventional MOSFETs was achieved, although the drain current was slightly smaller. In addition, the on/off ratio was made larger by using a very thin SOI structure. The characteristics can be further improved by thinning the SOI layer, as mentioned in Chap. 2.

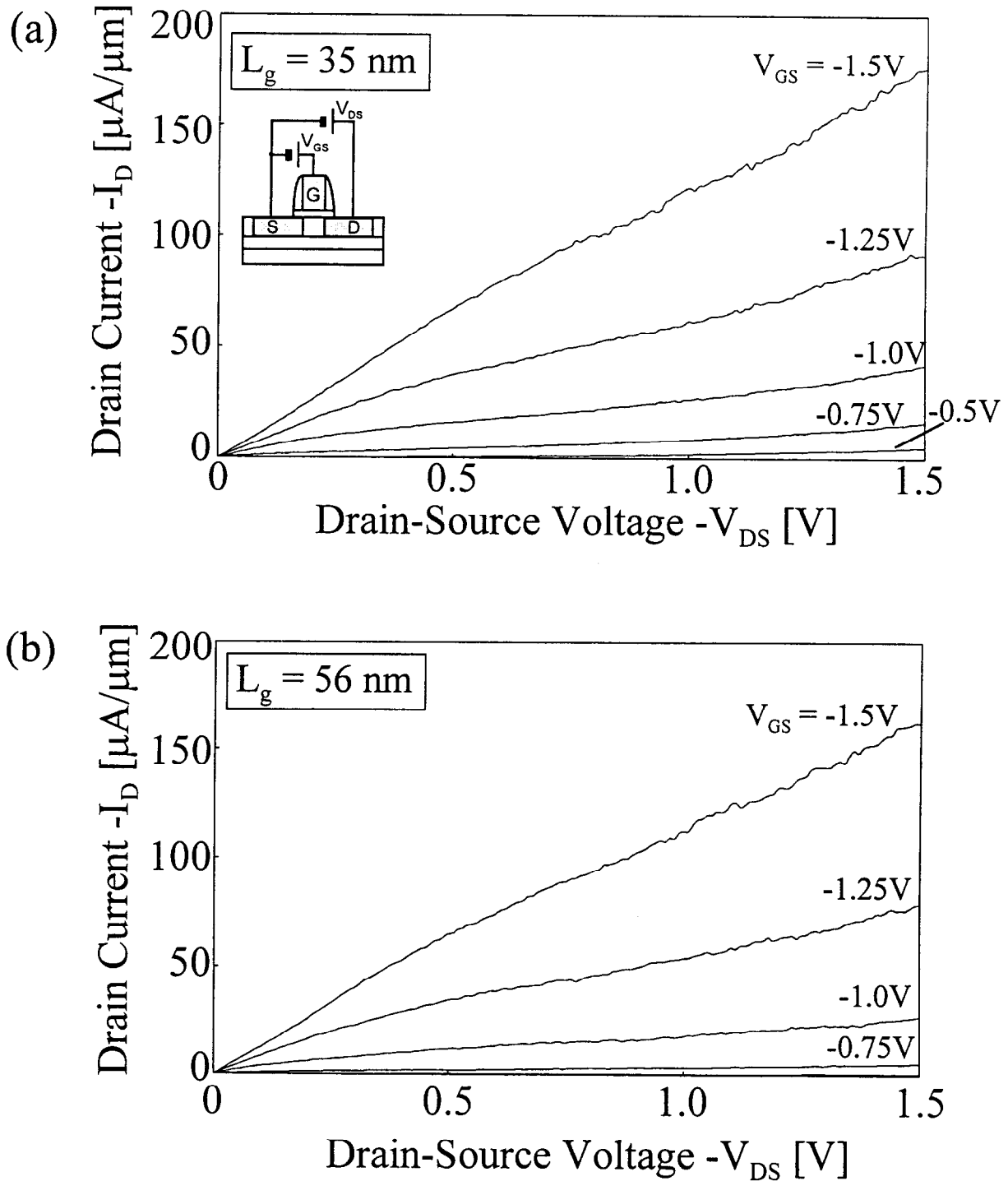


Figure 3.24: Common source drain curves of PtSi Schottky S/D MOSFETs with the gate-source voltage V_{GS} as a parameter. (a) 35 nm and (b) 56 nm-long gate device.

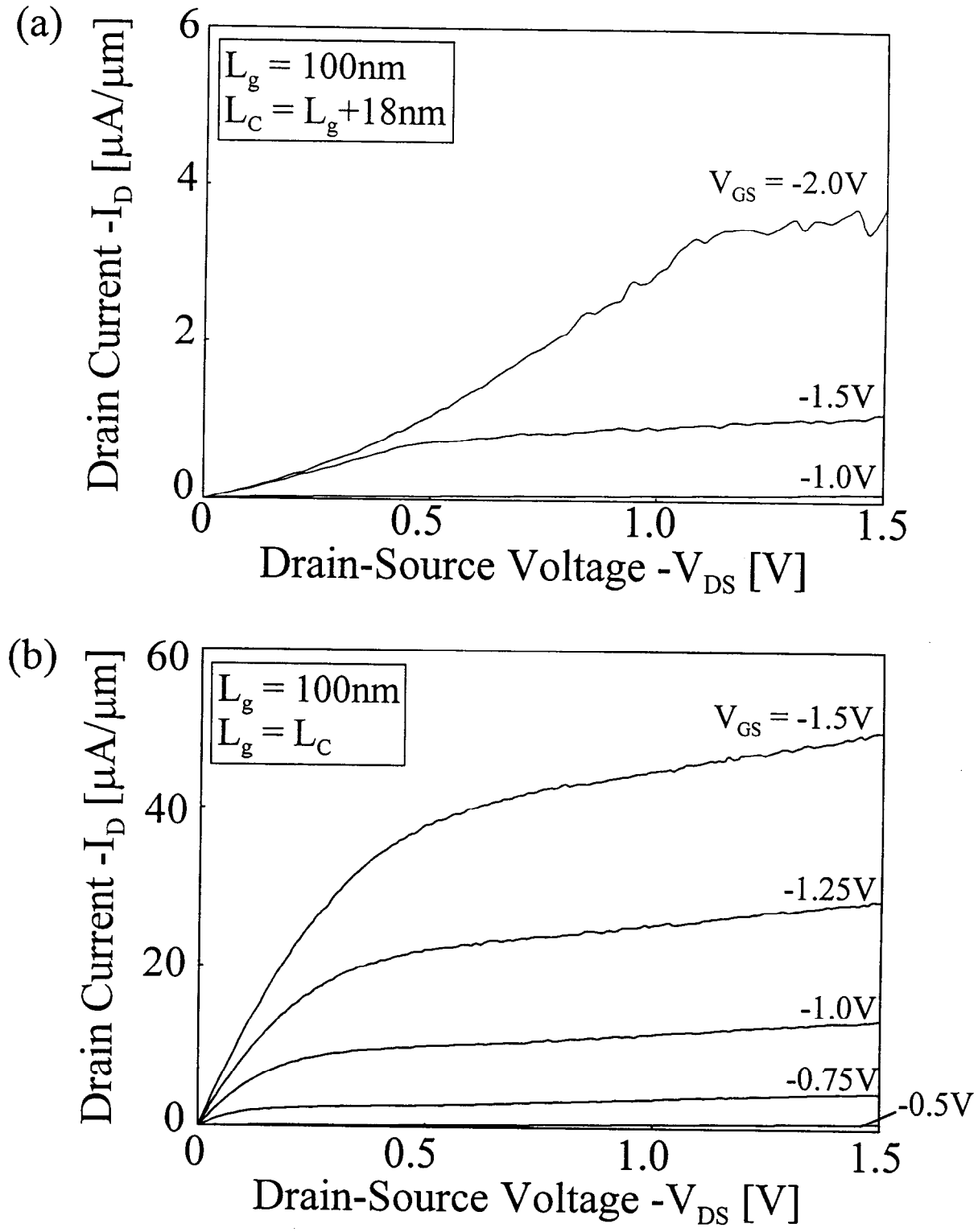


Figure 3.25: Dependence of characteristics on the gap between the gate and the S/D junctions. (a) gap d = 9nm and (b) d = 0

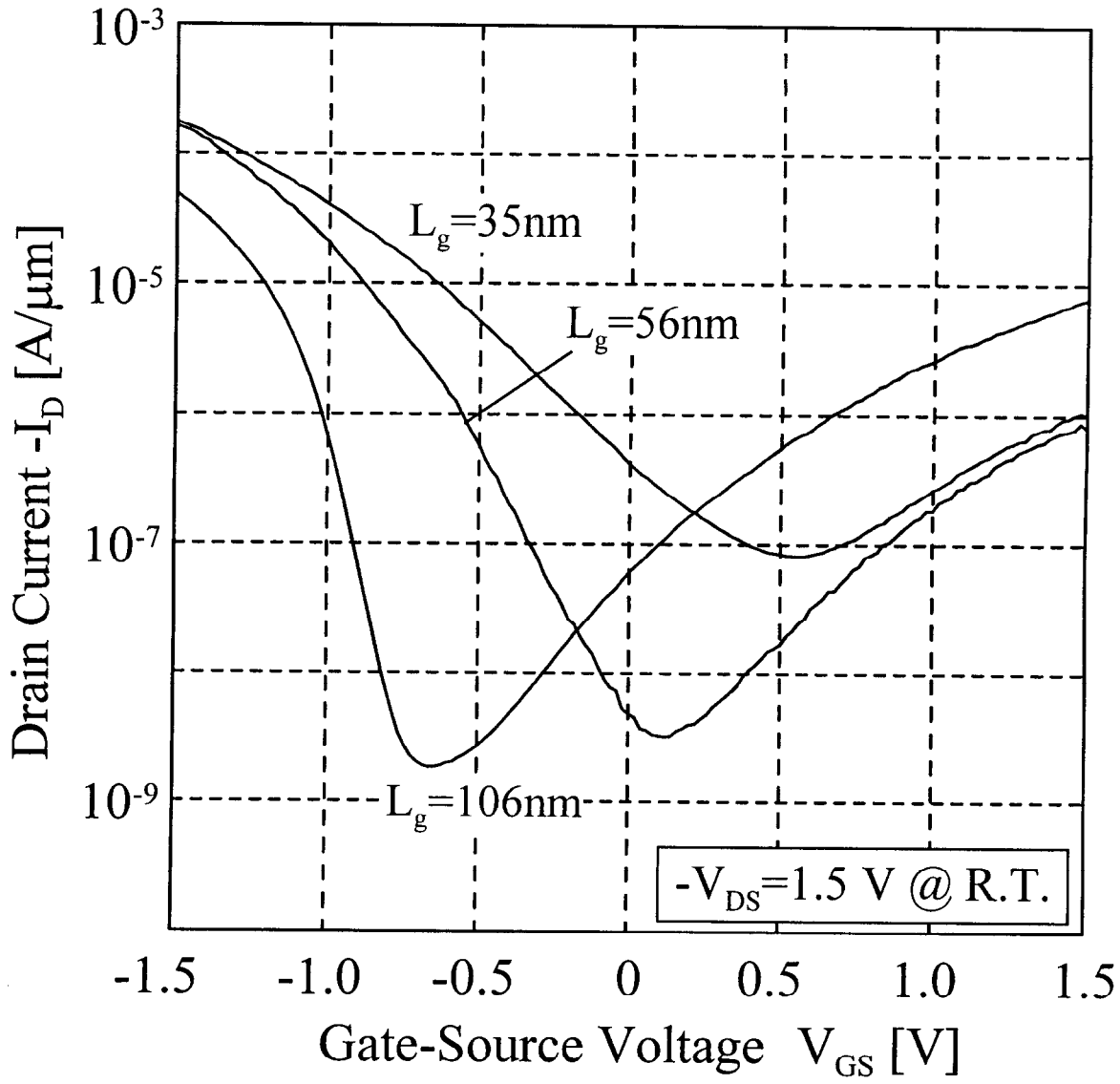


Figure 3.26: Subthreshold characteristics of PtSi Schottky S/D MOSFET as a function of gate length.

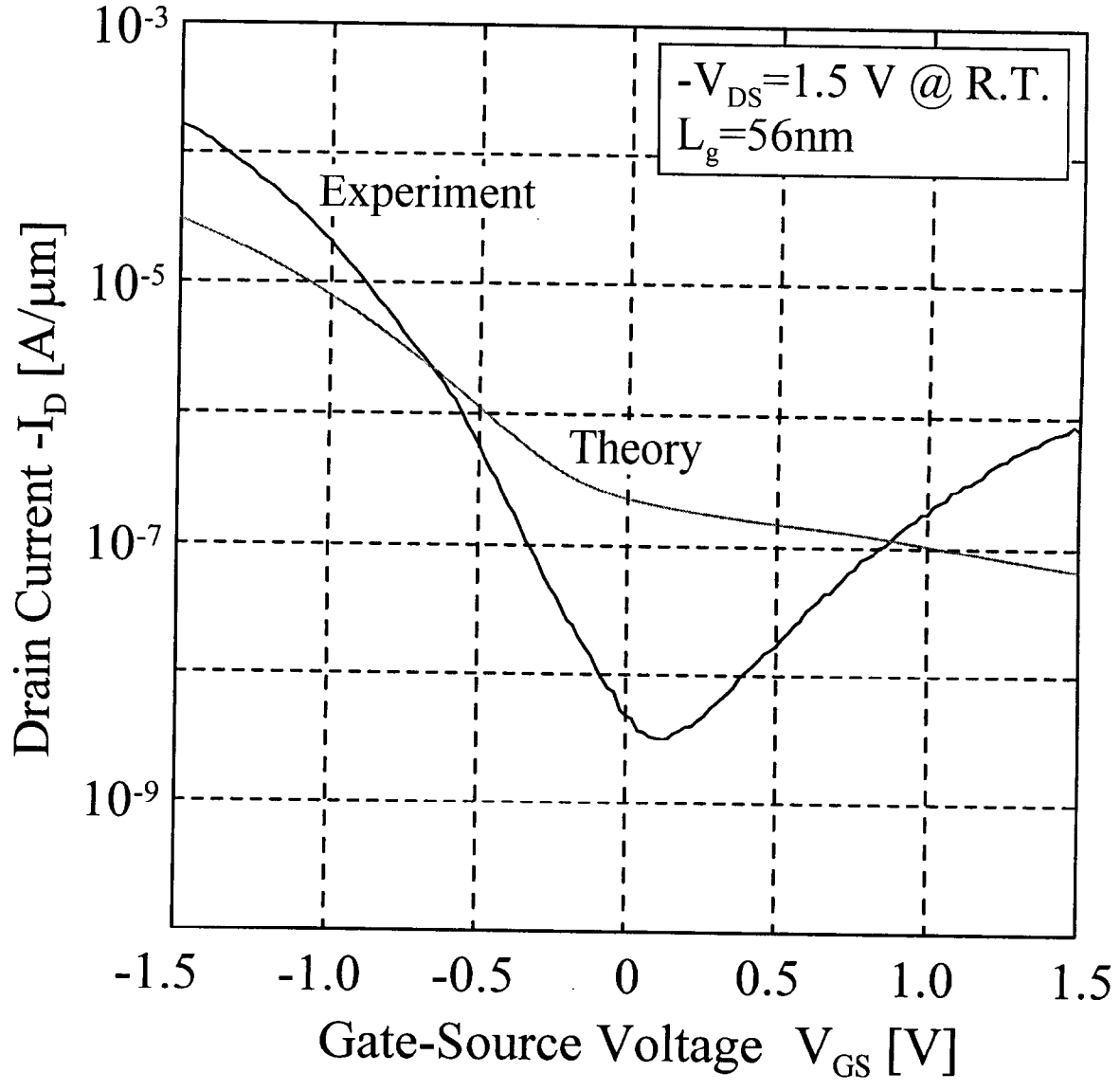


Figure 3.27: Comparison between theoretical and experimental characteristics for a 56 nm-long gate device.

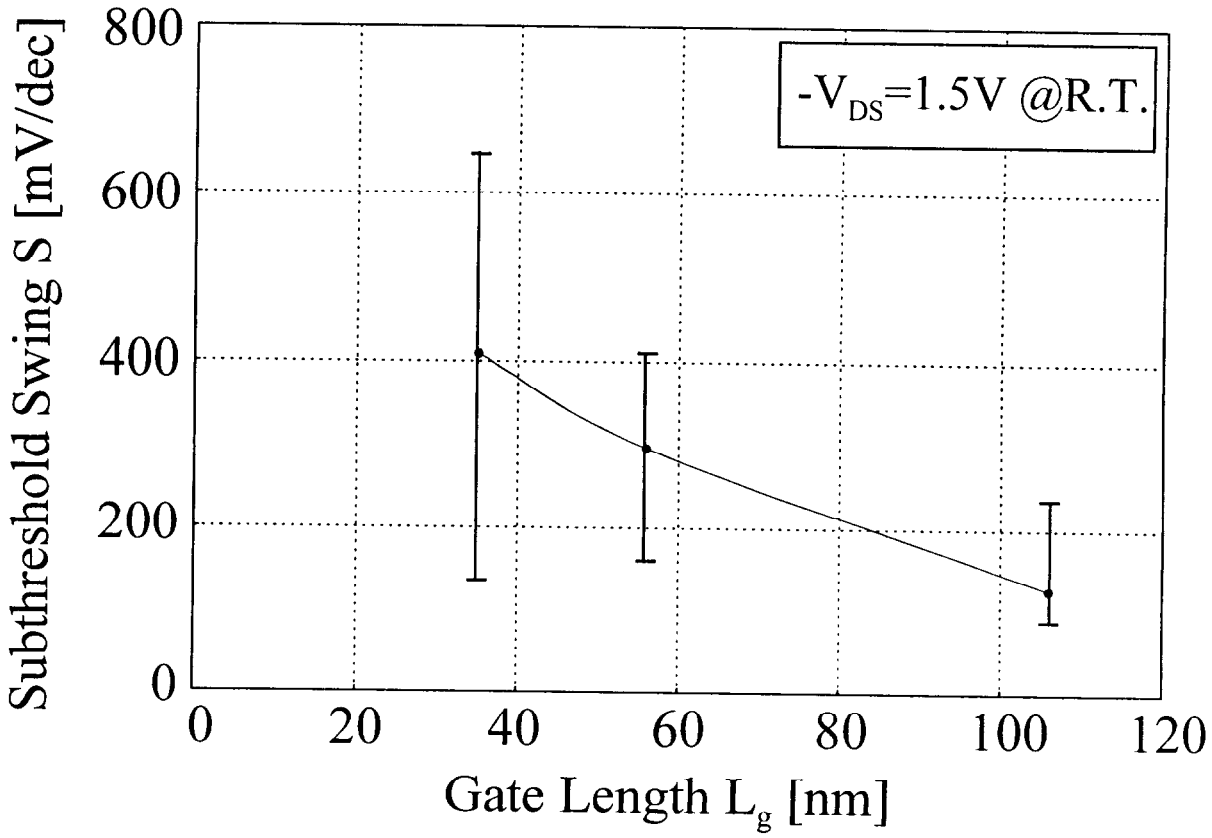


Figure 3.28: Relationship between subthreshold swing and gate length.

Table 3.1: Comparison between this work and previous work for p-type Schottky S/D MOSFETs and conventional MOSFETs

	This Work (t_{SOI}=25nm)		Bulk PtSi Schottky S/D MOSFET	p-MOSFET	
				Bulk	SOI (t_{SOI}=10nm)
Channel Length L_C [nm]	56 (t_{OX}=3.5nm)	35 (t_{OX}=3.5nm)	40 (t_{OX}=3.4nm)	38 (t_{OX}=2.8nm)	35 (t_{OX}=3.0nm)
Drain Current I_D [μA/μm]	60	70	100	260	300
Transconductance g_m [mS/mm]	220	216	240	300	
on/off ratio	3×10^4 (V_{DS}= -1.5 V)	420	31 (V_{DS}= -1.75 V)	71 (V_{DS}=-1.8V)	

3.4 Conclusion

Room temperature operation of very short channel Schottky source/drain (S/D) MOSFETs fabricated on a SIMOX substrate was demonstrated. Improvement of the on/off ratio was achieved using a very thin SOI structure. 25 nm-long metal gate devices were fabricated by electron-beam lithography with PMMA resist and a salicide process. For the S/D material, $ErSi_2$ and PtSi were used for n-type and p-type devices, respectively. For 25 nm-long gate n-type $ErSi_2$ Schottky S/D MOSFETs, the drain current was 75 μA/μm and the transconductance was 9.5 mS/mm at $V_{DS} = V_{GS} = 2$ V. For 35 nm-long gate p-type PtSi Schottky S/D MOSFETs, the drain current was -176 μA/μm and the transconductance was 390 mS/mm at $V_{DS} = V_{GS} = -1.5$ V. For the PtSi Schottky S/D MOSFET, comparable drivability to conventional MOSFETs was achieved. The on/off ratio was improved by using a very thin SOI structure. The characteristics can be further improved by a cleaning process before formation of the S/D and thinning of the SOI layer.

Chapter 4

Proposal and Analysis of Vertical Tunneling Field Effect Transistor

4.1 Introduction

Tunneling field effect transistor is very attractive device for nm-size device. Because the device is composed by metal source, drain and gate, and the device current is tunneling current, as described in Chap. 1. Vertical tunneling field effect transistor (VTFET) is composed by nm-thick multi-layered heterostructures. The drain current is determined by tunneling barrier height and thickness, because the drain current is tunneling current through the tunneling barrier. Therefore very flat nm-thick multi-layers are necessary for realization of VTFET. The crystal growth technique can be realized the required structure. However, the crystal growth has the limit of grown material, which depends on the substrate. In previous works, 25 nm-long channel VTFET with AlSb/InAs heterostructures on GaAs substrate has been demonstrated [62]. In addition, the VTFET on Si substrate was fabricated using very thin thermal oxide for tunneling barrier without crystal growth [60]. Although the tunneling barrier and gate insulator were formed with same material at these VTFET, the different materials for tunneling barrier and gate insulator are necessary for large driving current and good gate insulation.

The tunneling barrier must be low enough to allow large tunneling current densities and high transconductance, while the barrier of the gate insulator must be high enough to suppress leakage current.

In view of these requirements, i.e., appropriate barrier heights and metal-semiconductor-insulator heterostructures, we proposed a new vertical tunneling field effect transistor (VTFET) with lattice-matched $CoSi_2/Si/CdF_2/CaF_2$ heterostructures on a Si substrate with a very short channel. In this device, $CoSi_2$, Si, CdF_2 and CaF_2 are used as the electrode, tunneling barrier, channel and gate insulator, respectively, and satisfy the requirements mentioned above. $CoSi_2$, CdF_2 and CaF_2 have a fluorite lattice structure that is nearly lattice-matched to Si with mismatches at room temperature of -1.2, -0.8 and $+0.6$ %, respectively. Epitaxial growth of $CoSi_2/CaF_2$, $CoSi_2/Si$ and CdF_2/CaF_2 heterostructures on Si has been developed [64]–[68]. In addition, these heterostructures may also be used for novel field effect quantum devices on silicon [69].

In this chapter, the theoretical characteristics of VTFETs are described and are discussed the dependence of the subthreshold characteristics, transconductance and response time which depend on the structural differences of devices. From these results, potential of VTFET in nm-size region is compared with that of conventional MOSFETs. In addition, influence of carrier scattering in the channel and application to quantum device are discussed.

4.2 Device Structure and Principle of Operation

The structure of the proposed VTFET and its band diagram are shown in Fig. 4. 1. In device operation, electrons are injected from the source ($CoSi_2$) into the channel (CdF_2) through the Si tunnel barrier. The tun-

neling probability of electrons through the source barrier is controlled by the gate-source voltage which changes the voltage across the barrier. The tunneling electrons are then transported laterally along the channel toward the drain. Finally, electrons flow over the drain barrier (Si) to the drain ($CoSi_2$).

As shown in Fig. 4. 1(b), the conduction band discontinuities [122], [123] are ΔE_C=13.6 eV for $CoSi_2$/ Si, 0.6 eV for CdF_2/ Si and 2.9 eV for CdF_2/ CaF_2. The Fermi level of $CoSi_2$ is at 13.0 eV [124], [125], which is almost the same as the conduction band edge of CdF_2. Because of the low barrier, the tunneling current is large in the $CoSi_2$/Si/CdF_2 structure, resulting in a large transconductance. Moreover, good gate insulation can be achieved with the high barrier of the CdF_2/CaF_2/$CoSi_2$ structure.

The current-voltage characteristics of VTFETs are similar to those of conventional MOSFETs, in which the drain current saturates at high drain-source voltages V_{DS} region. In conventional MOSFETs, the drain current is determined by the channel resistance, while in the present VTFET, the drain current is determined mainly by the transmission probability through the source and drain barriers. This depends on the electric field at the tunnel barriers. The VTFET is insulated gate hot electron transistor [126]–[128]. The tunneling spectrum as a function of gate-source voltage is shown in Fig. 4. 2.

The device resistance is dominated by the tunneling resistance of the barriers, which is much larger than the channel resistance in very short channel structures. In this device, the drain current is almost independent of V_{DS} under appropriate bias conditions, for the following two reasons. First, the transmission coefficient of the drain barrier is nearly independent of V_{DS}, because the energy of the electrons is much higher than the

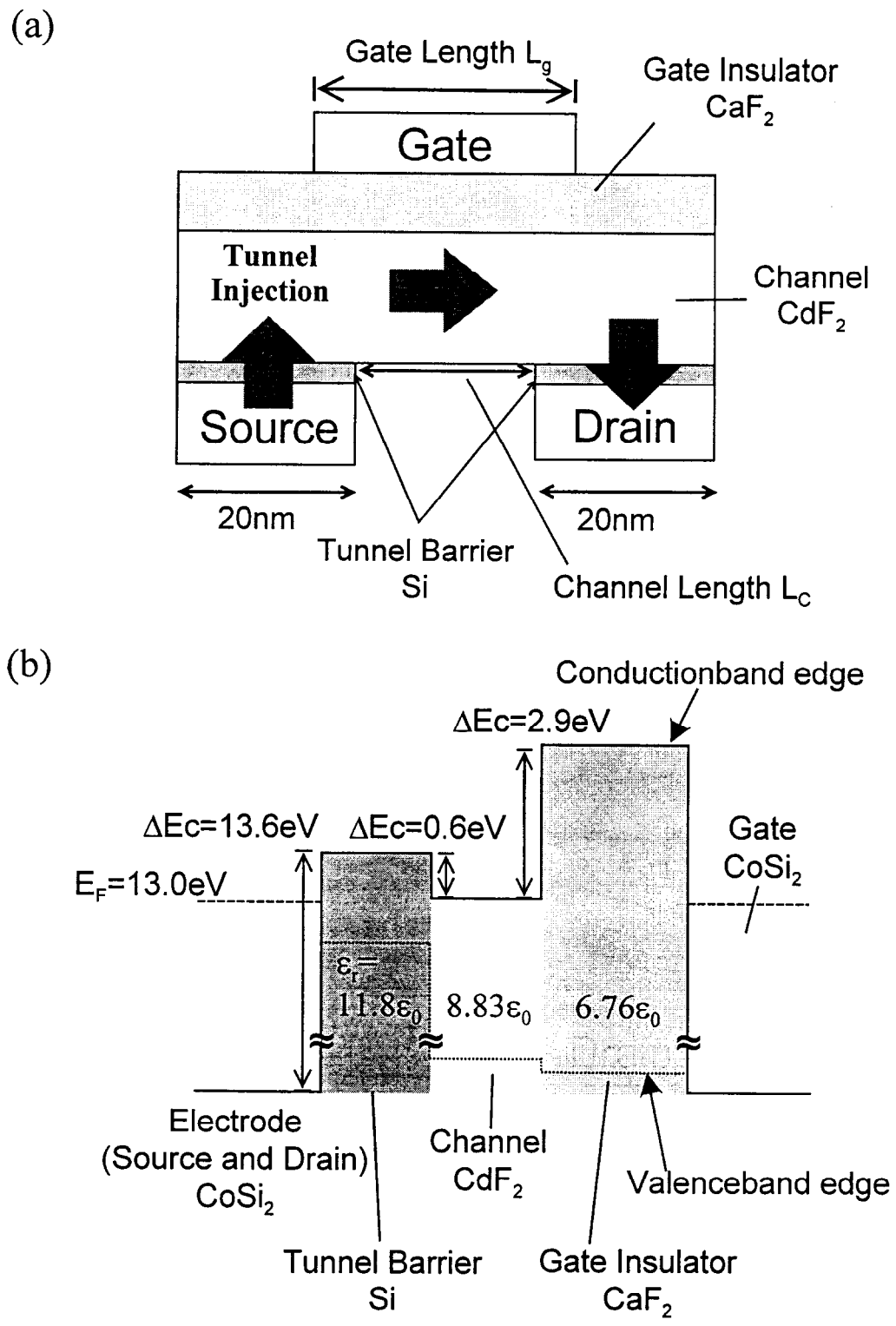


Figure 4.1: Device structure of vertical tunneling field effect transistor (VTFET). (a) Cross-sectional structure and (b) conduction band diagram in the vertical direction.

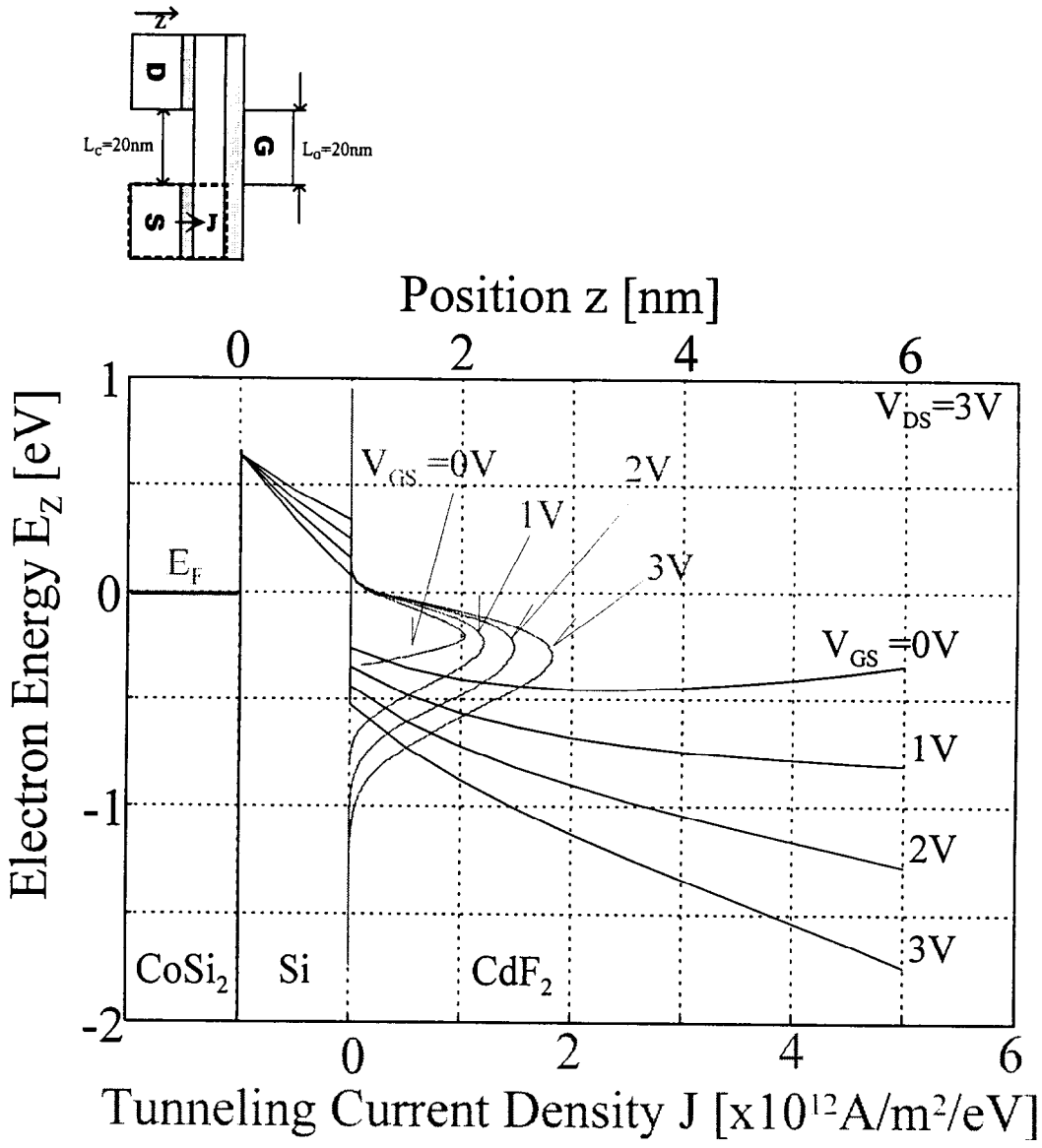


Figure 4.2: Tunneling spectrum at the source barrier as a function of gate-source voltage.

drain barrier at a high V_{DS}. Secondly, the electric field at the source barrier is almost independent of V_{DS}. Figure 4. 3 shows this situation with examples of the potential distribution, calculated using a finite element method. In the calculation, the channel length L_C defined as the distance from the right edge of the source to the left edge of the drain is 20 nm, the gate length L_g is 20 nm, the gate insulator thickness is 3 nm, the channel thickness is 5 nm, the tunnel barrier thickness is 1 nm, and the source and drain lengths are 20 nm. The gate-source voltage V_{GS} is 3.0 V and the drain-source voltage V_{DS} is 0.3 V (dotted lines) and 3.0 V (solid lines). The potential distribution in the region between the drain and the gate (channel and drain tunnel barrier) is very different for the different values of V_{DS}, while between the source and the gate the potential difference is independent of V_{DS}. As a result, the tunneling probability of electrons through the source barrier depends mainly on V_{GS}, and the characteristics, in saturation, can be expected. One advantage of the VTFET is that a very short channel is possible in principle, because the drain current depends mainly on the tunneling resistance of the barrier and is almost independent of channel resistance.

This VTFET is n-type FET due to operation by electron tunneling. A p-type (hole tunneling) device has been proposed [61]. Complementary circuit can be realized using these VTFETs.

4.3 Calculation Model without Scattering

The device characteristics were analyzed as follows. First, the potential distribution in the device under the application of drain-source and gate-source voltages (V_{DS} and V_{GS}) was calculated by a finite element method. SiO_2 is assumed for the outer material surrounding the device. Then, the

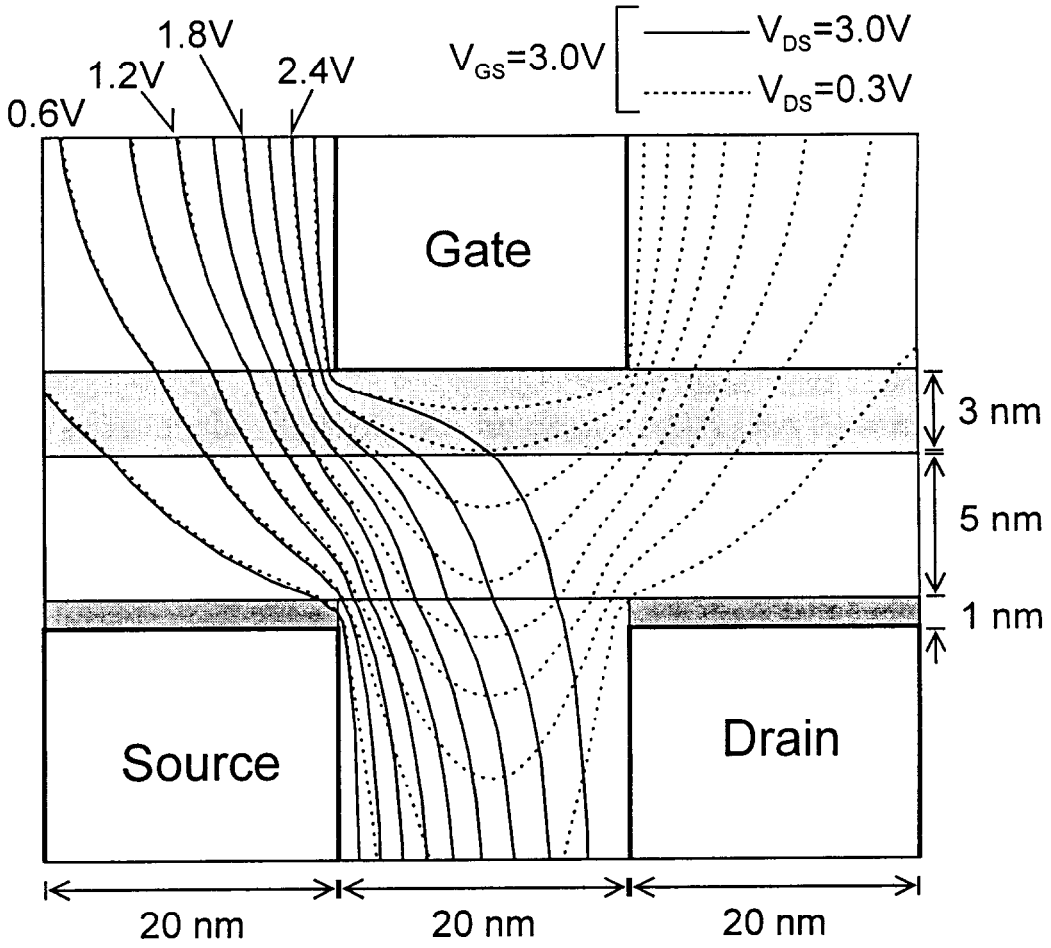


Figure 4.3: Potential distribution in the VTFET at V_{GS} = 3.0 V and V_{DS} = 0.3 V (dotted lines) and 3.0 V (solid lines) obtained by a finite element method.

transmission coefficient of an electron from source to drain at a given energy was calculated using the above potential distribution. Finally, the device current is calculated using the transmission coefficient and the electron energy distribution.

In the analysis, the following assumptions were made. Since a wide-gap material without doping is used for the channel, the carrier density in the channel without applied voltages is very small. Under an applied voltage, carriers are not generated in the channel but are injected from

the source through the barrier. The initial doping density and carrier density do not affect the analysis as long as these are much smaller than the injected carriers. Therefore, in calculating the potential distribution in the device, we have assumed that the carriers in the channel are only those injected from the source.

Since a channel length of a few tens of nanometers is discussed, carrier scattering in the channel region is neglected in this calculation. The characteristics of the VTFET can be degraded by carrier scattering. The transit velocity of electrons decreases by the scattering and the carrier density in the channel increases. Therefore the influence of the gate voltage on the electric field at the source barrier becomes weak. As a result, the transconductance decreases and the cut-off frequency of the device is degraded by the carrier scattering in the channel. The details are described later.

The transmission coefficient from the source to the drain is determined by the bent waveguide composed of source barrier, channel and drain barrier. However, electron wave resonance between the source and drain barriers, which is the same phenomenon as in the double-barrier resonant tunneling diode, is neglected in this calculation. By neglecting the resonance, the transmission coefficient from source to drain is given by the product of the transmission coefficient at the source T_1 and that at drain T_2. This is the simplest case with only one-reflection at each tunnel barrier without multi-reflections between source and drain. Neglecting the resonance is a good approximation in the present device when the drain-source voltage V_{DS} is high, so that $T_2 \simeq 1$ and the drain current is in the saturation region. If V_{DS} is low and T_2 is well below unity, the transmission coefficient is modulated by the resonance. However, this

modulation is effectively smoothed out due to the energy distribution of electrons tunneling through from the source at the room temperature. A two-dimensional analysis [129] shows that the transmission coefficient in a bent (L-shaped) waveguide without the tunneling barrier is slightly less than unity and has dips due to resonance. This effect is also smoothed out in the present device due to the electron energy distribution.

T_1 and T_2 are given by the tunneling probability at the source and drain barriers, respectively. These are determined by the electron energy along the z direction, because electrons are assumed to transport towards the drain after reflection at the channel/gate interface and the side of the device. The transmission coefficient T_1 at the source barrier was calculated using the following equation with the effective mass approximation [130]:

$$-\frac{\hbar^2}{2m^*}\cdot\frac{\partial^2\psi}{\partial z^2}+[V(z)-E_z]\psi=0, \tag{4.1}$$

where E_z is the electron energy along the z direction (Fig. 4. 4(a)) and m^* is the effective mass. The potential distribution $V(z)$ is calculated by a finite element method, taking into accounting the carrier density n_C in the channel. The value of the n_C calculated in the analysis is fed back into the finite element calculation until the solutions become self consistent. The channel is divided into piecewise-linear potentials, shown schematically in Fig. 4. 4(b). A solution of the Eq. (4. 1) in the region i ($z_{i-1}\leq z\leq z_i$), $\psi_i(z)$ is,

$$\psi_i=C_i^+\phi_i^+(z)+C_i^-\phi_i^-(z), \tag{4.2}$$

where C_i^+ and C_i^- are constants. When the potential in the region i is constant, i.e., $V_{i-1}=V_i$, ϕ_i^+ and ϕ_i^- are represented as

$$\begin{cases}\phi_i^+(z)=\exp(jk_iz)\\ \phi_i^-(z)=\exp(-jk_iz),\end{cases} \tag{4.3}$$

with

$$k_i = \frac{\sqrt{2m_i^*(E_z - V_i)}}{\hbar}, \tag{4.4}$$

where $m_i{}^*$ is the effective mass in the region. When $V_{i-1} \neq V_i$, $\phi_i{}^+$ and $\phi_i{}^-$ are described using the Airy functions A_i and B_i [131],

$$\begin{cases} \phi_i^+(z) = A_i(s) \\ \phi_i^-(z) = B_i(s), \end{cases} \tag{4.5}$$

with

$$\begin{aligned} s &= r_i\,(z + a_i)\,, \\ r_i &= \left(\frac{V_i - V_{i-1}}{z_i - z_{i-1}} \cdot \frac{2m_i^*}{\hbar^2}\right)^{1/3}, \\ a_i &= \frac{z_i - z_{i-1}}{V_i - V_{i-1}}\,(V_i - E_z)\,. \end{aligned} \tag{4.6}$$

For the boundary conditions at the interface z_i, we assume that the wave function (envelope function) and its first derivative divided by the effective mass are continuous [132], [133],

$$\begin{aligned} \psi_i\,(z_i) &= \psi_{i+1}\,(z_i)\,, \\ \psi_i'\,(z_i)\,/m_i^* &= \psi_{i+1}'\,(z_i)\,/m_{i+1}^*, \end{aligned} \tag{4.7}$$

This assumption ensures the continuity of the probability current. Using Eqs. (4. 2)-(4. 7), we have

$$\begin{aligned} M_i\,(z_i) \begin{pmatrix} C_i^+ \\ C_i^- \end{pmatrix} &= M_{i+1}\,(z_i) \begin{pmatrix} C_{i+1}^+ \\ C_{i+1}^- \end{pmatrix}, \\ i &= 1, 2, \cdots, N-1, \end{aligned} \tag{4.8}$$

where

$$M_i\,(z) = \begin{pmatrix} \phi_i^+(z) & \phi_i^-(z) \\ \phi_i^{+\prime}/m_i^* & \phi_i^{-\prime}/m_i^* \end{pmatrix}. \tag{4.9}$$

At the left and right sides of the potential ($z < z_0$ and $z > z_N$, respectively),

$$\psi_0 = \exp\,(jk_0 z) + C_{ref} \exp\,(-jk_0 z)\,, \tag{4.10}$$

$$\psi_{N+1} = C_{tans} \exp\left(jk_{N+1}z\right), \tag{4.11}$$

where C_{ref} and C_{trans} are the reflection and transmission amplitudes. ψ_{N+1} is assumed to be the wavefunction in the CdF_2 with constant potential $V(z) = V_n$. Using the boundary conditions Eq. (4. 7) at $z = z_0$ and z_N, we obtain

$$\begin{pmatrix} C_{trans} \\ 0 \end{pmatrix} = K_N K_{N-1} \cdots K_0 \begin{pmatrix} 1 \\ C_{ref} \end{pmatrix}, \tag{4.12}$$

where

$$K_i = M_{i+1}^{-1}\left(z_i\right) M_i\left(z_i\right), \tag{4.13}$$

The transmission coefficient T_1 is given by

$$T_1 = C_{trans}^{*} C_{trans} \cdot \frac{k_{N+1}}{k_0}. \tag{4.14}$$

The transmission coefficient T_2 at the drain barrier is obtained with the barrier shape approximated by a rectangular potential, as shown in Fig. 4. 4 (a), and variation of T_2 along the x direction is not taken into account. Because the potential variation along the x and z directions in the drain barrier is negligible at low V_{DS} and $T_2 \simeq 1$ at high V_{DS} as shown in Fig. 4. 3. The value at the right edge of the drain is used for T_2.

As discussed above, the transmission coefficient T from source to drain is given approximately by

$$T = T_1 T_2. \tag{4.15}$$

The tunneling current density $J_0(x)$ from the source electrode is given by [134]

$$\begin{aligned} J_0(x) &= \frac{em^{*}k_B\theta}{2\pi^2\hbar^3} \int_0^{\infty} T(x) \\ &\times \ln\left(\frac{1+\exp[(E_f - E_Z)/k_B\theta]}{1+\exp[(E_f - E_Z - eV_{DS})/k_B\theta]}\right) dE_Z, \end{aligned} \tag{4.16}$$

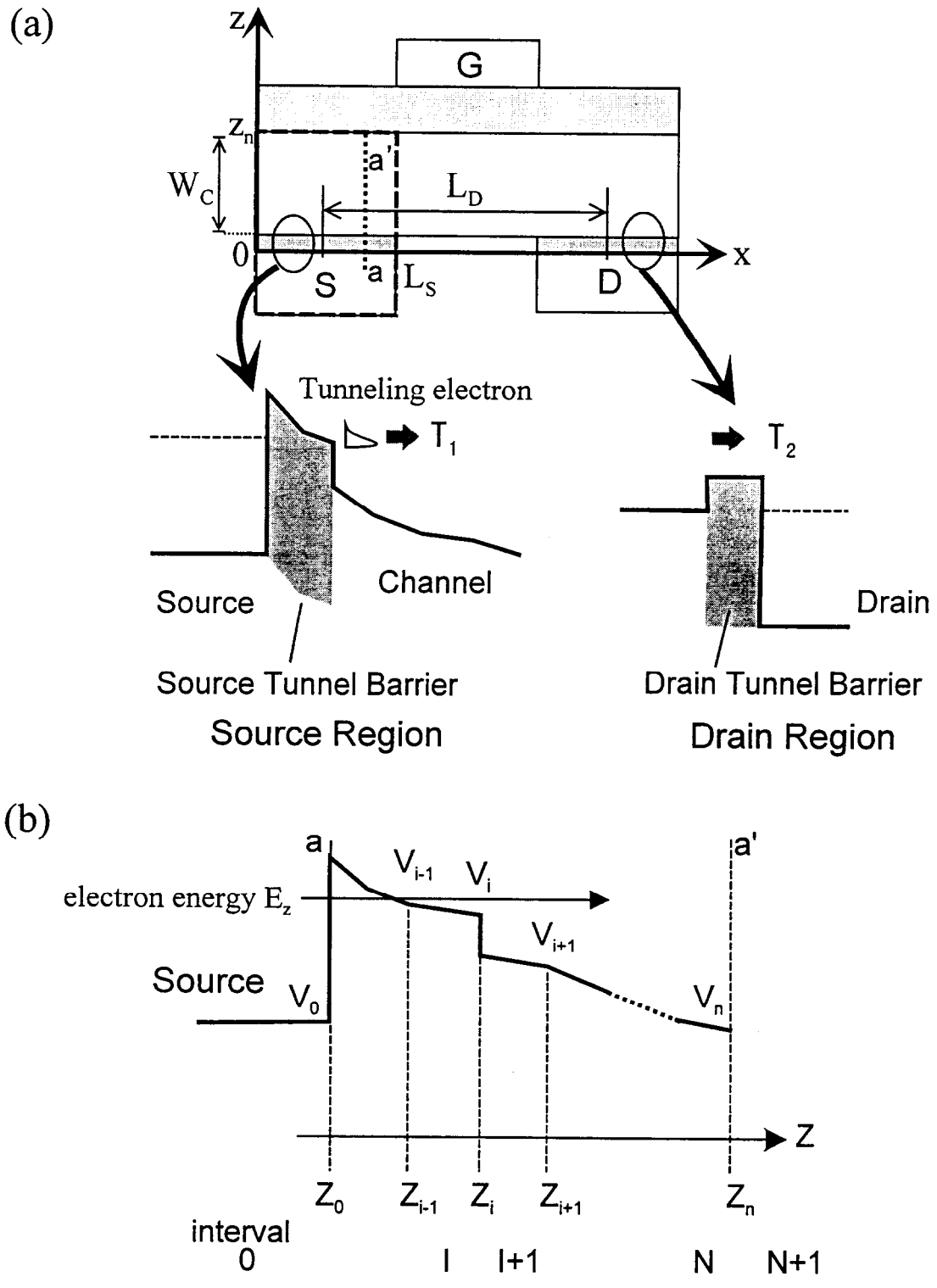


Figure 4.4: Model for calculation of the device characteristics. (a) Cross-sectional structure of VTFET and band diagrams of source region (source electrode, source barrier and channel) and drain region (drain barrier and drain electrode) and (b) one-dimensional piece-wise linear potentials in the source region.

where e is the electron charge, k_B is Bolzmann's constant, E_f is the Fermi energy of the source electrode, and θ is the absolute temperature.

Finally, the drain current I_D is obtained from the integral of the current density $J_0(x)$ over the length of the source electrode L_S, as shown in Fig. 4. 4(a).

$$I_D = \int_0^{L_S} J_0(x)dx, \tag{4.17}$$

The carrier density n_C in the channel is determined by I_D and affects the potential distribution in the device. This effect is considered by feeding-back the value of the carrier density n_C into the potential distribution calculation.

The carrier density n_C is given by

$$n_C = \frac{I_D}{eW_C\langle v_C\rangle}, \tag{4.18}$$

where W_C is the channel thickness as shown in Fig. 4. 4(a) and $\langle v_C\rangle$ is the average velocity in the channel towards the drain along the x direction. The energy of electrons in the channel along the x direction is approximately given by half of the difference between Fermi energy in the source and energy of tunneling electron along the z direction. $\langle v_C\rangle$ is given by

$$\langle v_C\rangle = \sqrt{\frac{E_f - \langle E_z\rangle}{m^*}}, \tag{4.19}$$

where $\langle E_z\rangle$ is the average energy in the z direction of tunneling electrons from the source, which corresponds to the peak energy of the transmission coefficient T. In this model, it is assumed that carriers are distributed in the channel with constant velocity and the current is carried only by carriers from the source to the drain. Although the distributions of the carrier density and velocity in the channel are modulated by the electric field, the electric field at the source barrier is almost independent of the field. Moreover, although channel carriers from the drain to the source

should also be considered in a more precise calculation, these carriers do not have a significant effect on the drain current, because they appear only at low V_{DS}, where the drain current is small and the transmission probability is low. We compared results with and without distribution of the density and velocity and with and without drain to source carriers. The difference in the drain current with and without the above points is less than 5 %. Therefore, in this calculation, it is assumed that the carrier density and velocity in the channel are uniform and are given by Eqs. (4. 18) and (4. 19).

4.4 Device Characteristics

4.4.1 Drain Current Curves

Figure 4. 5 shows common-source characteristics calculated at 300K for various values of V_{GS}. The channel length L_C defined as the distance from the right edge of the source to the left edge of the drain, is 5 nm in one case and 20 nm in another. The gate length is equal to the channel length. The gate insulator thickness is 3 nm, the channel thickness is 5 nm, and the tunnel barrier thickness is 1 nm. The gate electrode is located at the center of the device. The effective masses of the materials used are $m^*_{CoSi_2} = m_0$, $m^*_{CdF_2} = 0.16m_0$ [135] and $m^*_{Si} = 0.26m_0$. The effective mass of Si was estimated from that at the bottom of the conduction band in the (111) direction, assuming a Si(111) substrate [67], [64], [68]; i.e., $1/m^*_{Si} = (2/m_t + 1/m_l)/3$ with $m_t = 0.19m_0$ and $m_l = 0.98m_0$. In the characteristics for the 20-nm-long channel (dashed lines), the drain current clearly saturates in a way similar to conventional MOSFETs, as expected from Fig. 4. 3. Characteristics for the 5-nm-long channel (solid lines) are also similar to those of MOSFETs, although the saturation is

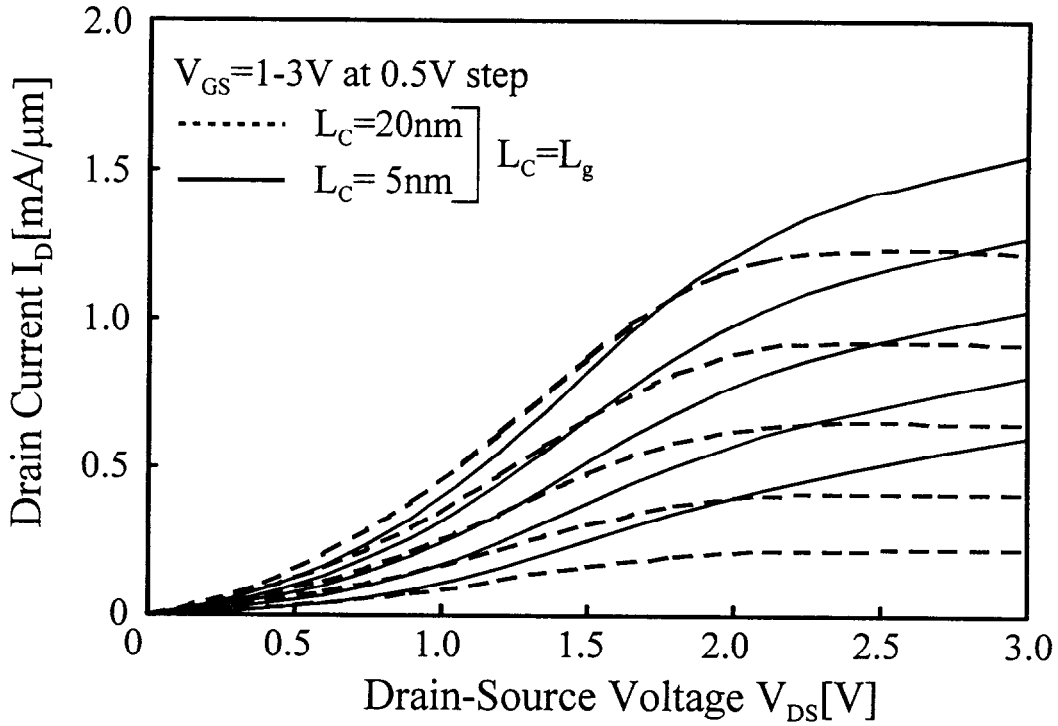


Figure 4.5: Calculated common-source characteristics as a function of gate voltage V_{GS}. Results are shown for channel lengths L_C of 20 nm (dashed lines) and 5 nm (solid lines).

weak due to the large influence of the drain electric field on tunneling at the source barrier. Figure 4. 6 shows characteristics for gate lengths L_g of 5 nm (dashed lines) and 15 nm (solid lines) with a 5-nm-long channel. The tunneling current increases with gate length, because the electric field at the source barrier becomes stronger.

Tunneling leakage current from the source to the gate is negligibly small in this structure. The direct tunneling current from the source to the gate is 1.4×10^{-9} A/μm under applied voltages of $V_{GS} = 3.0$ V and $V_{DS} = 3.0$ V in a VTFET with $L_C = 5$ nm and $L_g = 45$ nm.

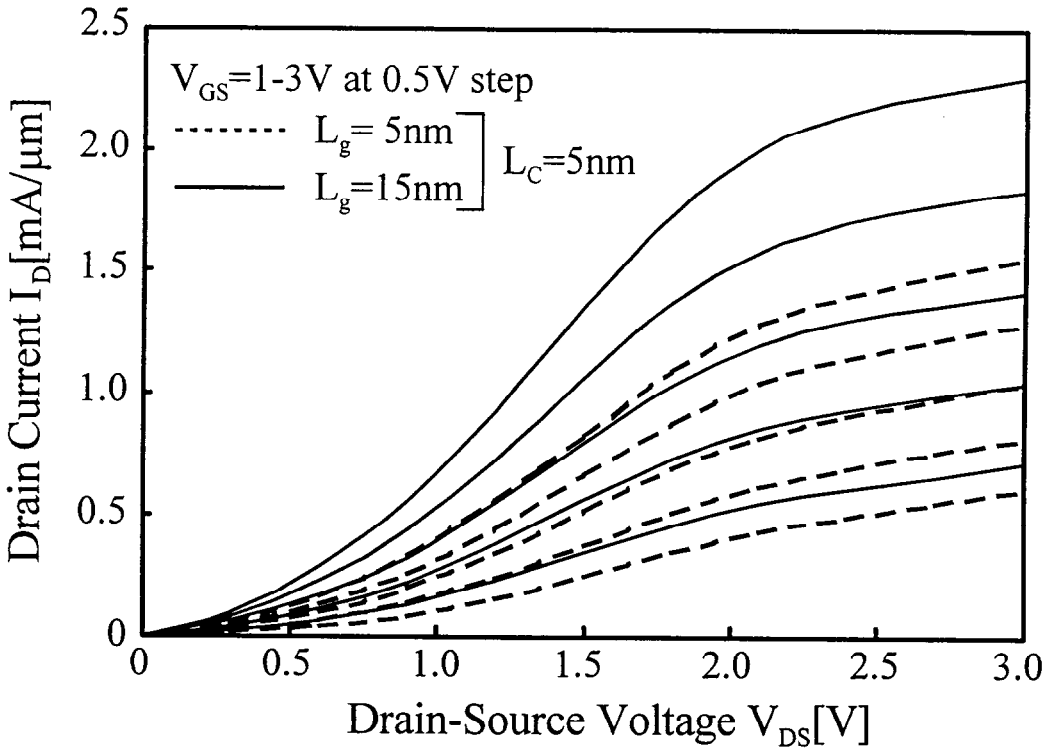


Figure 4.6: Calculated common-source characteristics as a function of gate voltage V_{GS}. Results are shown for gate length L_g of 5 nm (dashed lines) and 15 nm (solid lines).

4.4.2 Subthreshold Characteristics

The subthreshold characteristics as a function of gate length L_g are shown in Fig. 4. 7. The layer thicknesses are assumed to be same as those in Fig. 4. 5, and channel length was 5 nm. The off current decreases with increasing gate length. The subthreshold characteristics of VTFET are almost independent from the channel length and depend strongly on the gate length, because the drain current in the VTFET is determined by the electric field at the source barrier.

The relationship between threshold voltage, subthreshold swing and the gate length is shown in Fig. 4. 8. The device structure is assumed to be same as that in Fig. 4. 7. The threshold voltage is defined as the gate

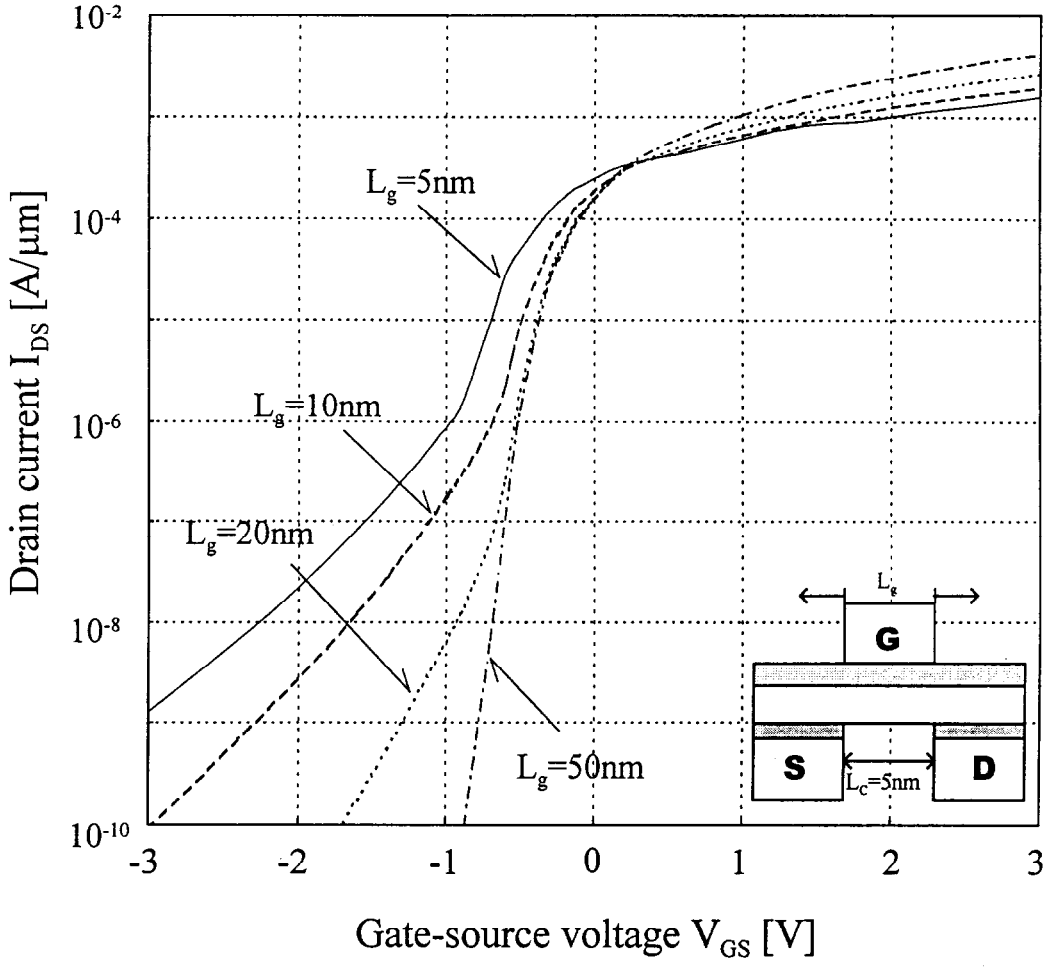


Figure 4.7: Subthreshold characteristics as a function of gate length L_g. Results are shown for channel length L_C of 5 nm.

voltage corresponding to $I_{DS}=I_{on}\times 10^{-6}$ ($I_{on}=I_{DS}$ at $V_{GS}=3$ V). With decreasing gate length, the threshold voltage decreases and subthreshold swing increases. These degradation by short channel effect is the same as conventional MOSFETs. The characteristics degrade rapidly at the gate length less than 45 nm, which corresponds to the device length from the source left edge to the drain left edge.

The subthreshold characteristics as a function of channel length are shown in Fig. 4. 9. The layer structure is assumed to be same as that in Fig. 4. 7. The gate length is assumed to be $L_g=L_C+40$ nm, which

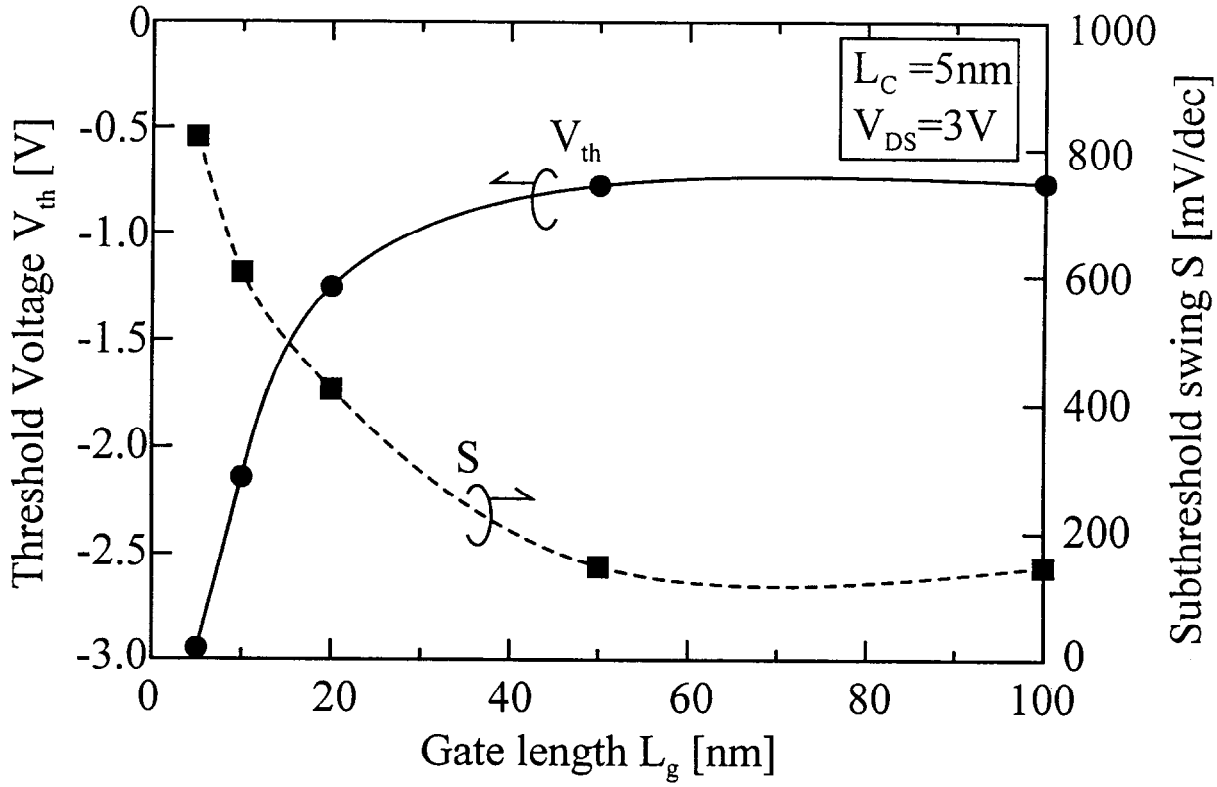


Figure 4.8: Threshold voltage $V_{\rm th}$ and subthreshold swing S as a function of gate length $L_{\rm g}$. Results are shown for channel length $L_{\rm C}$ of 5 nm.

corresponds to the device length from the source left edge to the drain left edge.

At gate length less than 10 nm, the characteristics are degraded. The relationship between threshold voltage shift, subthreshold swing and channel length is shown in Fig. 4. 10. To compare between conventional SOI-MOSFET [99], Schottky source/drain MOSFET and VTFET, the characteristics of these devices are drown in the same figure. The values for the conventional and Schottky source/drain MOSFETs are same as in Chap. 2. The characteristics of VTFET are not degraded even with 10 nm-long channel, although the SOI-MOSFET are degraded rapidly with decreasing channel length. The subthreshold swing of VTFET with

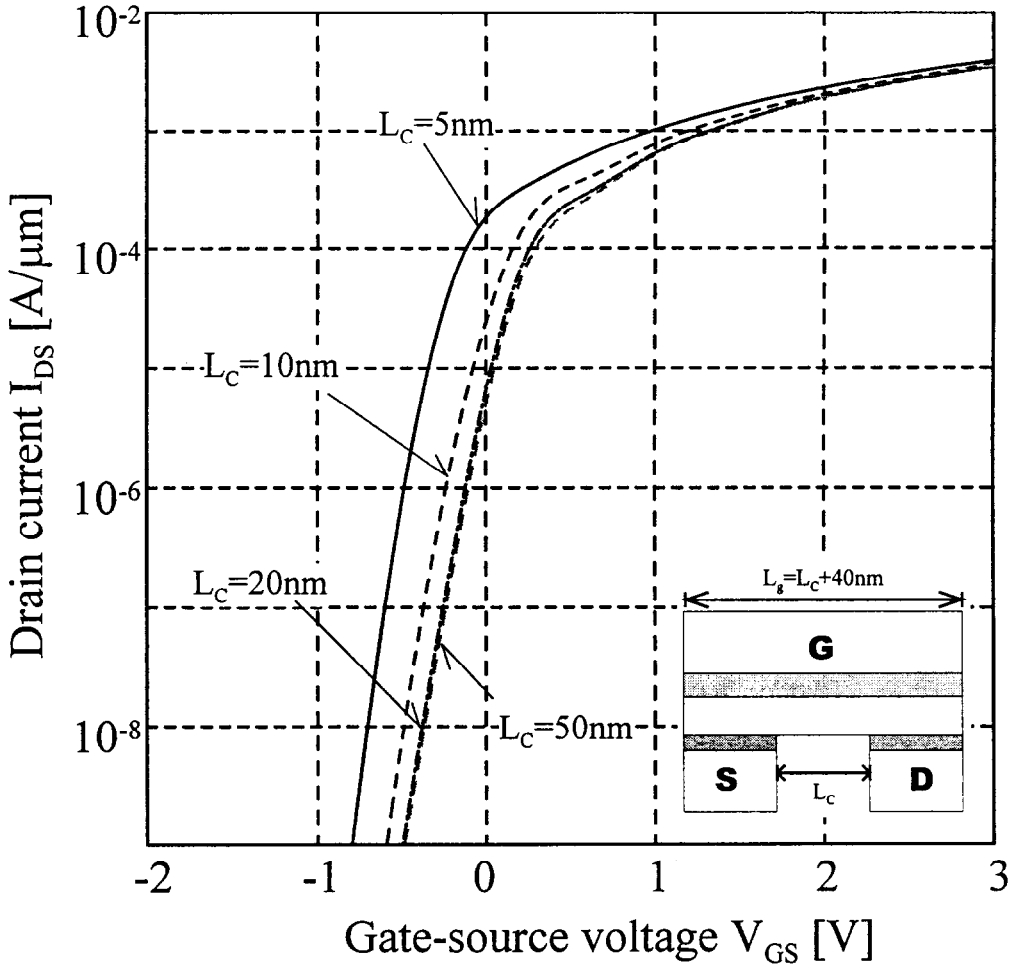


Figure 4.9: Subthreshold characteristics as a function of channel length L_C. Results are shown for gate length L_g=L_C+45 nm.

long channel is 120 mV/dec, which is larger than that of SOI-MOSFET, because the gate voltage controls tunneling barrier across the channel and gate insulator. Therefore the gate control efficiency of the VTFET is smaller than that of conventional SOI-MOSFET. However, the VTFET keeps subthreshold characteristics even with 10 nm-long channel, because the electric field at the source barrier is almost independent from the drain voltage.

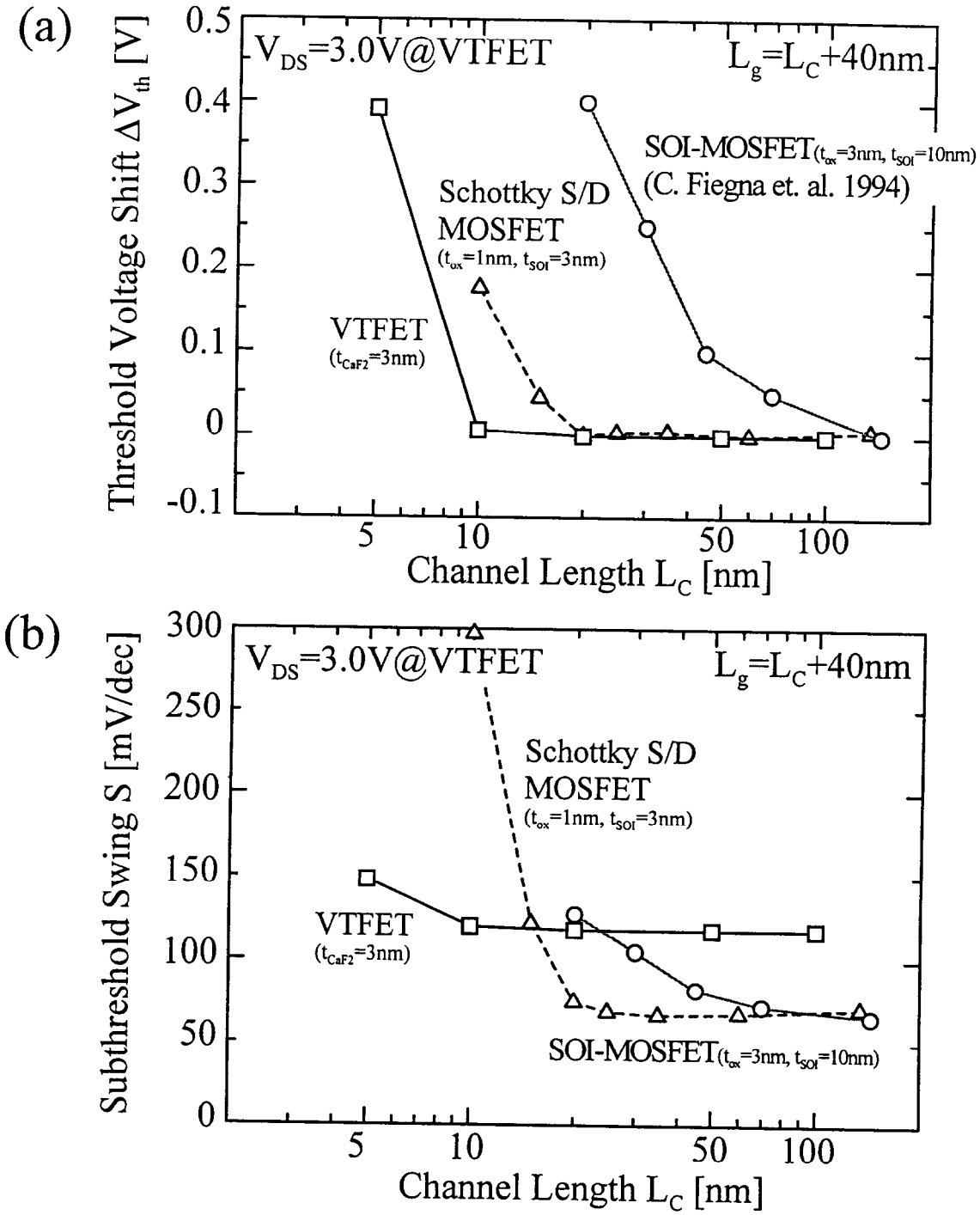


Figure 4.10: (a)Threshold voltage $V_{\rm th}$ and (b)subthreshold swing S of VTFETs, SOI-MOSFETs and Schottky MOSFETs as a function of channel length $L_{\rm C}$.

4.4.3 Response Time

The charging time τ_c is given by

$$\tau_c = \frac{C_g}{g_m} = (C_{gs} + C_{gd}) \Big/ \left(\frac{\partial I_D}{\partial V_{\rm GS}}\right), \tag{4.20}$$

where the gate capacitance C_g, which is the sum of the gate-source capacitance C_{gs} and the gate-drain capacitance C_{gd}, and g_m is the transconductance. The gate capacitance was calculated from the relationship between the charge distribution and the applied voltage using a finite element method. In this calculation, the influence of channel carriers is negligible due to low channel carrier density. The transconductance was estimated from the static characteristics discussed in the previous section. Hereafter we assume that the applied voltages for the analysis of the response time are $V_{\rm GS} = 3.0$ V and $V_{\rm DS} = 3.0$ V, located at the saturation region. These applied voltages are almost the same as the present LSI case. Reduction of applied voltage with scaling down is not discussed here.

Figure 4. 11 shows the relationship between charging time and channel length, assuming $L_{\rm C} = L_{\rm g}$. The transconductance g_m slightly decreases with the channel length, because the electric field at the tunneling barrier produced by the gate-source voltage becomes small. However, the charging time decreases with channel length, because the gate capacitance decreases more rapidly than the transconductance.

The transit time in VTFETs is comprised of the channel transit time and the tunneling times through the source and drain barriers, neglecting resonance between source and drain. In the present devices, the size is such that the tunneling times can be neglected, because these are estimated to be less than 10^{-15} sec [137] and are much shorter than the channel transit time and charging time. The transit time τ_r is approx-

imated by $\tau_r = L_D/\langle v_C \rangle$, where L_D is the distance between the center of the source and the center of the drain, as shown in Fig. 4. 4(a), and $\langle v_C \rangle$ is given by Eq. (4. 19).

The response time τ_R and the cut-off frequency f_t are related to the sum of the transit time τ_r and the charging time τ_c by

$$f_t = \frac{1}{2\pi\tau_R} = \frac{1}{2\pi\left(\tau_c + \tau_r\right)}. \tag{4.21}$$

The relation between charging time, transit time, cut-off frequency and gate length is shown in Fig. 4. 12. The transit time decreases with channel length, and for very short channels the transit time is much smaller than the charging time. The cut-off frequency increases with decreasing channel length due to the decrease in the charging time and transit time. The drain current and the transconductance increase with gate length as shown in Fig. 4. 6, because influence of gate voltage on the electric field at the source barrier increases. However, gate capacitance increases with gate length. Therefore the charging time and cut-off frequency are almost independent of gate length. The charging time τ_c and the transit time τ_r are 0.29 ps and 0.08 ps, respectively, for the 20-nm-long channel and gate. From these results, the response time without delay time from wires is 0.37 ps, and the cut-off frequency is 430 GHz.

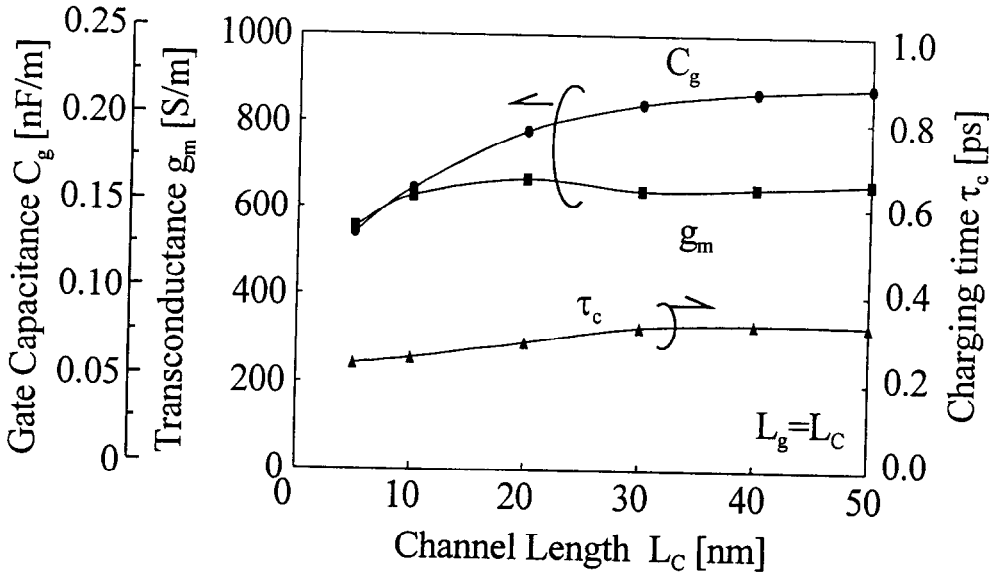


Figure 4.11: Transconductance g_m, gate capacitance C_g and charging time τ_c as a function of channel length L_C. The gate length L_g is assumed to be the same as the channel length.

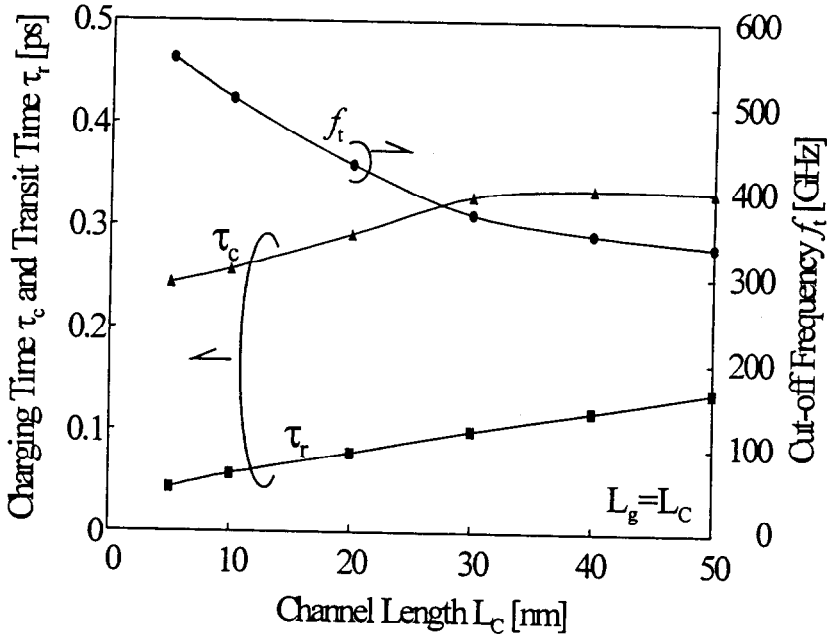


Figure 4.12: Charging time τ_c, transit time τ_r and cut-off frequency f_t as a function of channel length L_C. The gate length L_g is assumed to be the same as the channel length.

4.5 Influence of Scattering in the Channel

In the previous section, carrier scattering in the channel region was neglected. However, when carrier scattering is considered, ballistic electrons and scattered electrons are found to exist in the channel. The transit velocity of electrons decreases and the channel transit time increases, because the scattered electrons have lost their kinetic energies. Moreover, the carrier density in the channel increases due to the decrease in transit velocity. Therefore, the influence of the gate voltage on the electric field at the source barrier becomes weak. As a result, the transconductance decreases and the charging time of the device increases. The cut-off frequency of the device is degraded by carrier scattering in the channel due to the increased transit and charging times. In this section, analysis of influence of carrier scattering in the channel is discussed.

4.5.1 Calculation Model

The drain current was analyzed in the following way. First, the potential distribution in the device under the application of drain-source and gate-source voltages was calculated by a finite element method. Then, the transmission coefficient of an electron from source to drain at a given energy was calculated using the potential distribution. The drain current was calculated using the transmission coefficient by considering the electron energy distribution. The details of calculation of tunneling current are described in the previous section. The channel carrier density affects the potential distribution and the drain current. The channel carrier density is determined by the drain current. In addition, the channel carrier density increases with the scattering probability of electrons in the channel, because the velocity of the scattered electrons decreases.

Therefore, the drain current is recalculated to be self-consistent with the carrier density, the scattering probability and the potential distribution.

The calculation model is shown in Fig. 4. 13. In this model, the electrons tunneling from the source to the channel are scattered in the channel with a constant probability α and the scattered electrons are transported towards the drain to produce a drift current. In this model, we consider: a) the current from all electrons tunneling from the source to the channel I_{TD}, b) the ballistic current from the source to the drain I_{BD}, c) the current by scattered electrons I_{TS}, d) the current to the source by electrons reflected at the drain barrier without scattering I_{RB}, and e) the current by electrons reflected by scattering I_{RS}.

These currents are described using the tunneling current I_{TD} and the scattering probability α,

$$\left.\begin{aligned} I_{BD} &= (1-\alpha)T_2 I_{TD} \\ I_{TS} &= \alpha I_{TD} \\ I_{RB} &= (1-\alpha)^2(1-T_2)I_{TD} \\ I_{RS} &= \alpha(1-\alpha)(1-T_2)I_{TD}, \end{aligned}\right\} \tag{4.22}$$

where T_2 is the electron tunneling probability without scattering at the drain barrier.

In the calculation of T_2, it is assumed that the electron energy in the z-direction at the drain barrier increases by eV_{DS} due to the drain-source voltage, because channel carriers are injected toward the drain along the z-direction, as shown in Fig. 4. 13(a). This approximate electron energy is almost the same as the electron energy towards the drain from the channel after reflection at the channel/gate insulator interface and at the side of the device. Reflection of I_{RB} at the source barrier is neglected, assuming I_{RB} is small. This is a good approximation, because as we will show later $T_2 \sim 1$ in the saturation region. The drain current I_D is given by the sum of the ballistic current I_{BD} and the drift current by scattered

electrons I_{SD} ($=I_{TS}+I_{RS}$).

$$I_D = I_{BD} + I_{SD} = I_{BD} + I_{TS} + I_{RS}. \tag{4.23}$$

The calculation process of the drain current is as follows and is shown in Fig. 4. 14. First, the scattering probability α and the carrier density in the channel n_C are assumed to be constants. Then the potential distribution in the device under application of drain-source and gate-source voltages (V_{DS} and V_{GS}) is calculated. The tunneling current I_{TD} is calculated using the potential distribution, and the ballistic current I_{BD} is given by eq. (4. 22). The carrier density in the channel with ballistic motion n_B is given by

$$n_B = \frac{I_{BD}}{ev_B W_C}, \tag{4.24}$$

where W_C is the channel thickness and v_B is the average velocity of ballistic electrons in the channel towards the drain in the x-direction, as shown in Fig. 4. 13. v_B is approximately given by

$$v_B = \sqrt{\frac{E_f - \langle E_z \rangle}{m^*}}, \tag{4.25}$$

where E_f is the Fermi energy of the source electrode and $\langle E_z \rangle$ is the average energy in the z-direction of electrons tunneling from the source. This corresponds to the peak energy of the transmission coefficient.

The drift current from scattered electrons I_{SD} is described using the scattered electron density n_C-n_B, the carrier velocity in the channel v_{FC}, and the transmission probability from the channel to the drain T_{2S},

$$I_{SD} = e(n_C - n_B)W_C v_{FC} T_{2S}(f_S - f_D), \tag{4.26}$$

where it is assumed that v_{FC} is the Fermi velocity in the channel and T_{2S} is the drain barrier tunneling probability of electrons at the Fermi level in

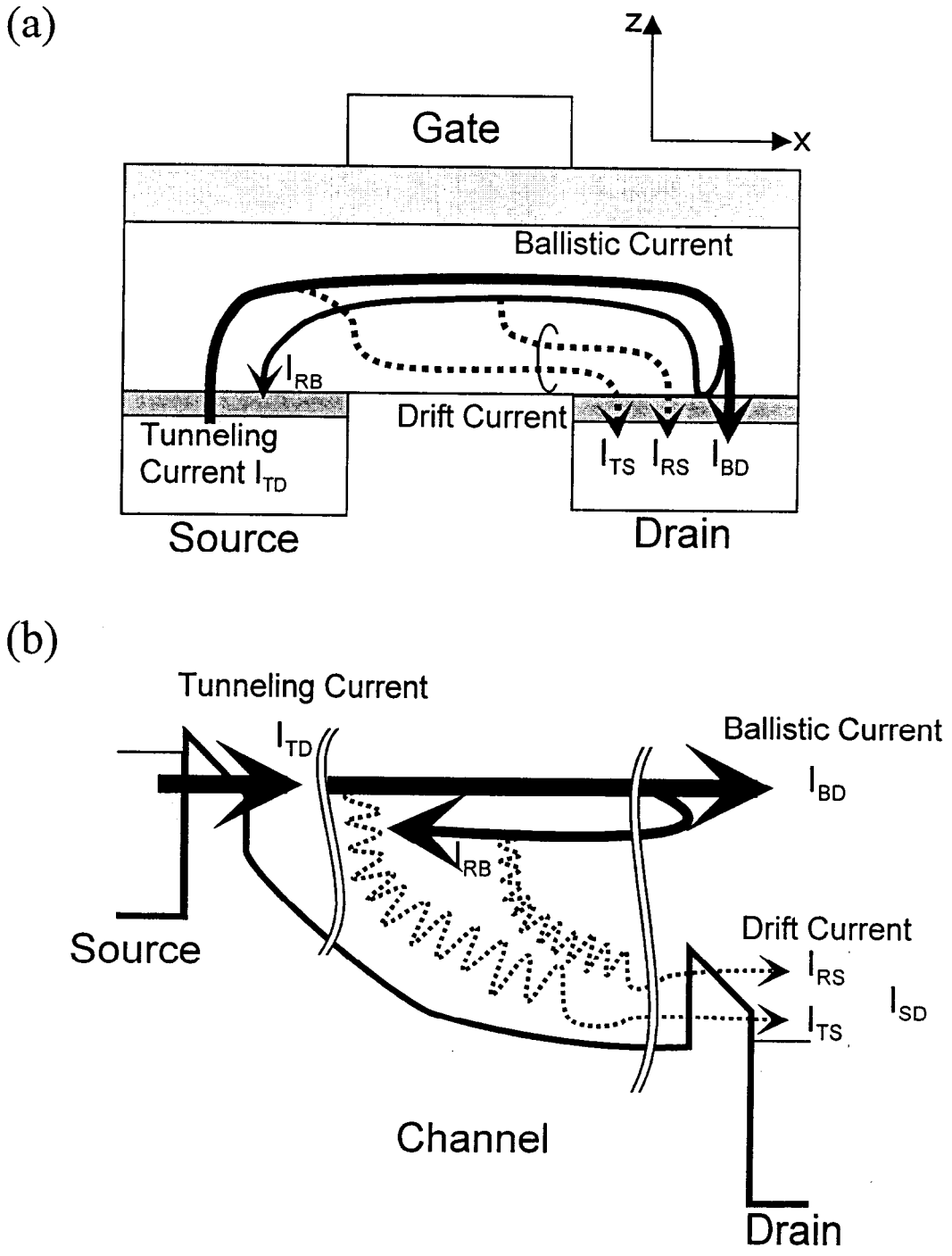


Figure 4.13: Model for calculating the relationship between the drain current and the electron scattering probability in the channel. (a) Current paths in the device. (b) Conceptual band diagram.

the channel. f_S and f_D are the Fermi distribution functions at the source and the drain, respectively. v_{FC} is given by

$$v_{FC} = \sqrt{\frac{2k_B\theta}{m^*} \ln\left(\frac{n_C - n_B}{N_C}\right)}, \tag{4.27}$$

where

$$N_C = 2\left(\frac{2\pi m^* k_B \theta}{h^2}\right)^{\frac{3}{2}}. \tag{4.28}$$

Here k_B is Boltzmann's constant and θ is the absolute temperature. Self-consistency is maintained in the calculation of the drain current by feeding back the value of the carrier density n_C into the potential calculation, in which n_C is changed according to I_{SD} in Eq. (4. 26) and the sum of I_{TS} and I_{RS} is given by Eq. (4. 22).

In this model, it is assumed that carriers are distributed uniformly in the channel with constant velocity. Although the distributions of the carrier density and the velocity in the channel are modulated by the electric field, the electric field at the source barrier is almost constant. Therefore, the influence of the electric field in the channel along the x-direction can be neglected in the calculation of the drain current. We compared the results with and without the distributions of the density and the velocity of channel carriers, which are considered with an electric field in the channel along the x-direction. As a result, the difference in the drain currents with and without these distributions taken into account is less than 3 %. Therefore, in this calculation, it is assumed that the carrier density and the velocity in the channel are uniform and are given by Eqs. (4. 24), (4. 25) and (4. 27).

4.5.2 Calculation Results

The resulting characteristics, in which scattering in the channel was considered, are shown in Fig. 4. 15. Here, the channel length is 5 nm,

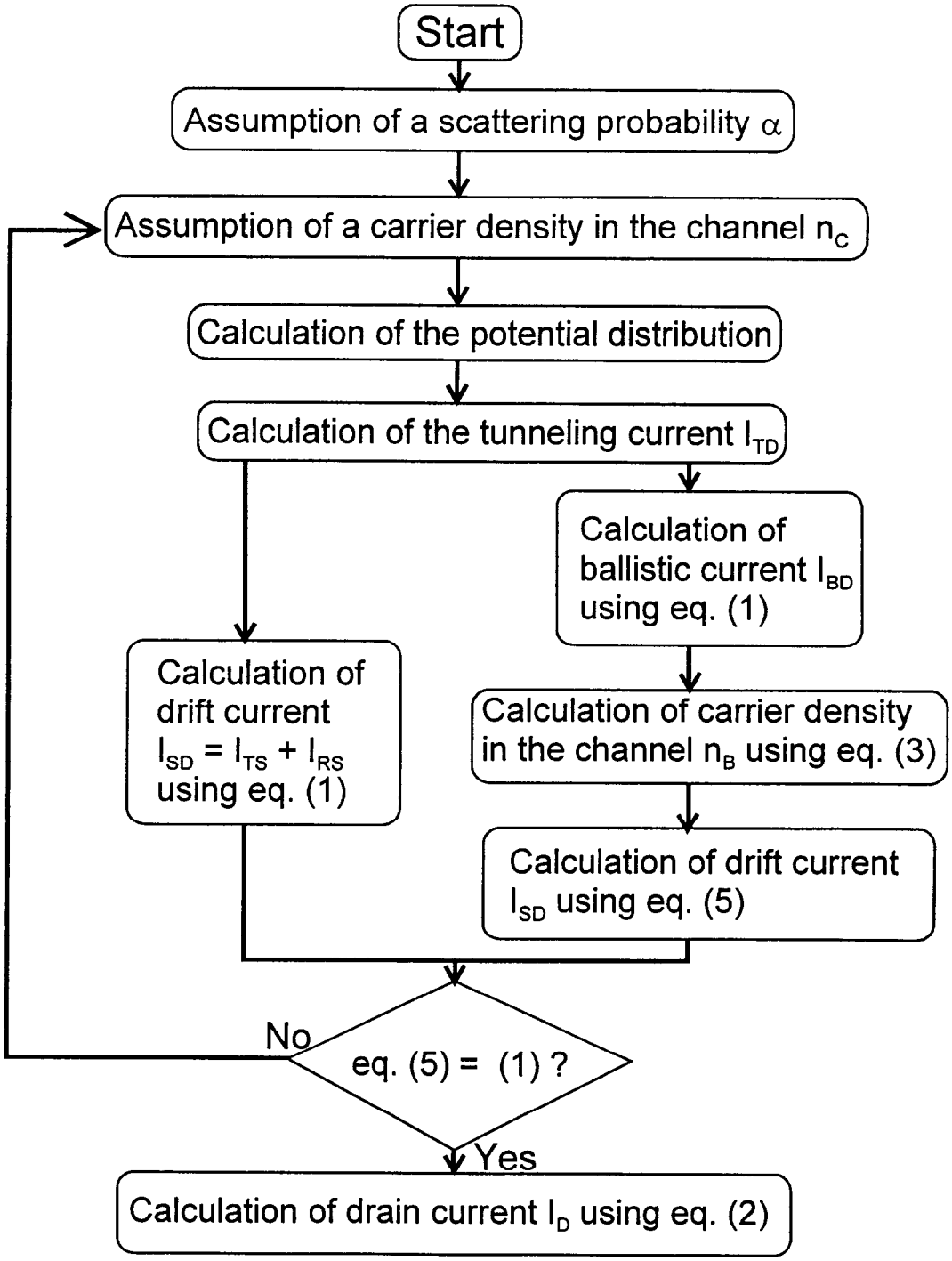


Figure 4.14: Self-consistent calculation process of the drain current.

the gate length is 5 nm, the gate insulator thickness is 3 nm, the channel thickness is 5 nm, the tunneling barrier thickness is 1 nm and the source and drain electrode lengths are each 20 nm. The effective masses of the materials are described in the previous section.

Figure 4. 15(a) shows the common-source characteristic for different values of α, the scattering probability of electrons in the channel. The gate-source voltage V_{GS} is 3.0 V. The drain current decreases with increasing scattering probability at high V_{DS}. At $\alpha = 1$, the drain current saturates at low V_{DS} compared to the characteristic at $\alpha = 0$. The ballistic current I_{BD} saturates at $V_{DS}\sim 2$ V, because T_2, the tunneling probability of ballistic electrons at the drain barrier, becomes ~ 1 due to the increased energy from V_{DS}. The drift current I_{SD} saturates at a lower V_{DS} compared to the ballistic current, because the drift current is determined by the difference in the Fermi distribution between the source and the drain as shown in Eq. (4. 26). However, T_{2S} is determined by the Fermi energy in the channel, which depends on the scattered electron density in the channel and is almost independent of V_{DS}. At high α, the drain current increases rapidly at low V_{DS} due to the increase in I_{SD}. At low V_{DS}, ballistic electrons return to the source, because the electrons are reflected at the drain barrier due to low energy. Therefore, the drain current is small at low α. However, at high α, reflected electrons at the drain barrier become the drain current due to the scattering. Although the tunneling probability of scattered electrons is lower than that of ballistic electrons, scattered electron density is much higher than ballistic electron density. Therefore, the drain current increases with α at low V_{DS}.

Figure 4. 15(b) shows the relationship between the carrier density in

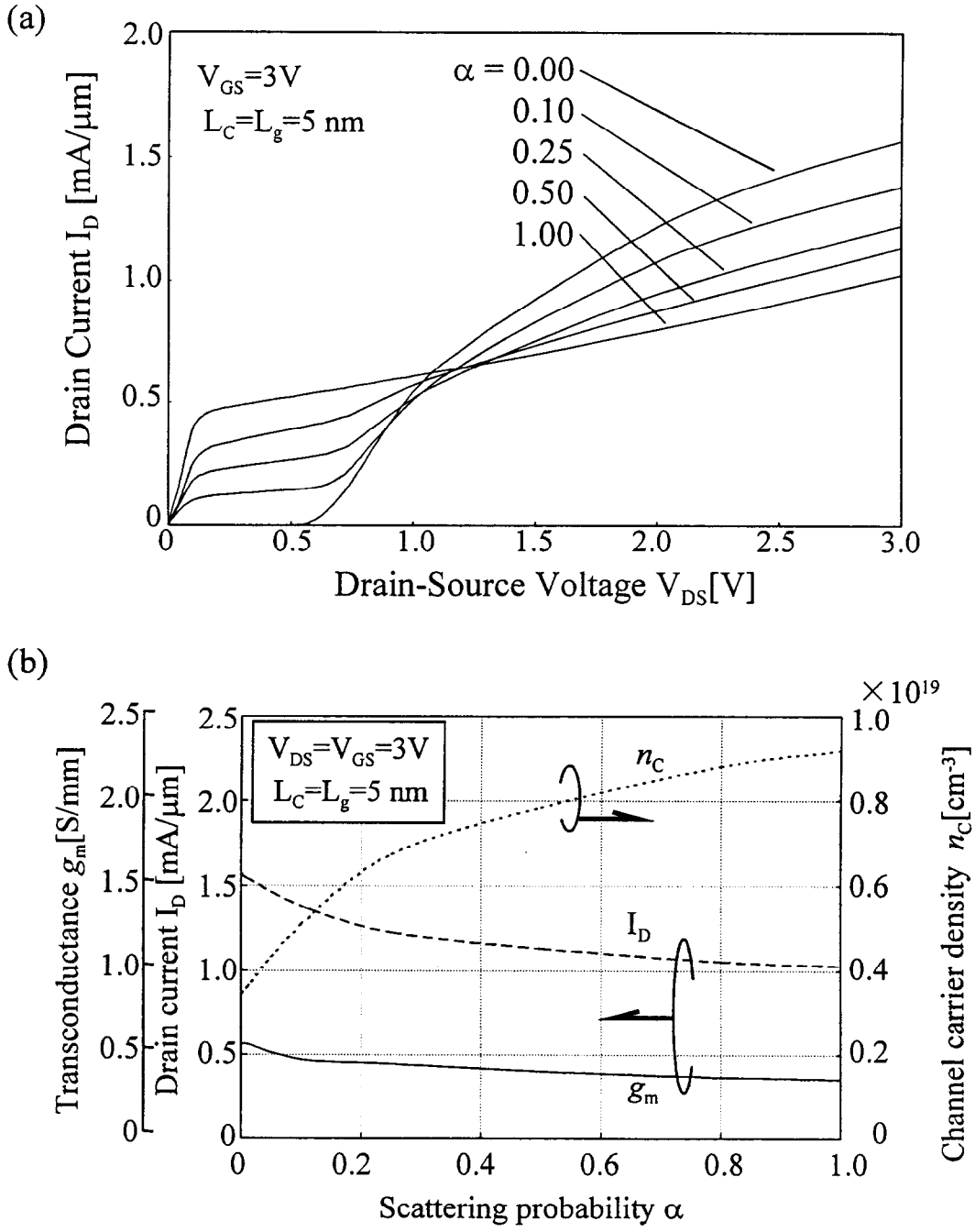


Figure 4.15: (a) Calculated common-source characteristic showing drain current I_D vs drain-source voltage V_{DS} for different electron scattering probabilities α at a gate-source voltage of 3.0 V. (b) Channel carrier density n_C, drain current I_D and transconductance g_m as functions of the electron scattering probability α at $V_{GS} = V_{DS} = 3.0$ V.

the channel n_C, the drain current I_D, the transconductance g_m and the scattering probability α at $V_{GS} = V_{DS} = 3$ V. n_C increases and I_D and g_m decrease with increasing α. At $\alpha = 1$, n_C is three times larger than and I_D and g_m are half of the values without scattering. In the VTFET, the drain current decreases with increasing carrier density in the channel, because the drain current is independent of the channel conductance.

The charging time, transit time and cut-off frequency were estimated by the method in the previous section. The relationship between charging time, transit time, cut-off frequency and scattering probability is shown in Fig. 4. 16. The device structure is assumed to be the same as that in Fig. 4. 15. The charging time increases with scattering probability due to the decrease in transconductance. The transit time likewise increases with increasing scattering probability due to the decrease in electron velocity. As a result, the cut-off frequency is reduced by a factor of two compared to the value without scattering.

Figure 4. 17 shows the relationship between response time, cut-off frequency and channel length for different scattering probabilities, assuming $L_C = L_g$. At $\alpha = 0$, the cut-off frequency is determined almost solely by the charging time. At $\alpha = 1$, the transit time becomes larger than the charging time at $L_C > 40$ nm, because the electron velocity in the channel is decreased by scattering. For long channel structures, the response characteristics are greatly influenced by scattering. For $L_C = 5$ and 100 nm, the cut-off frequency is one-half and one-third of the values without scattering, respectively.

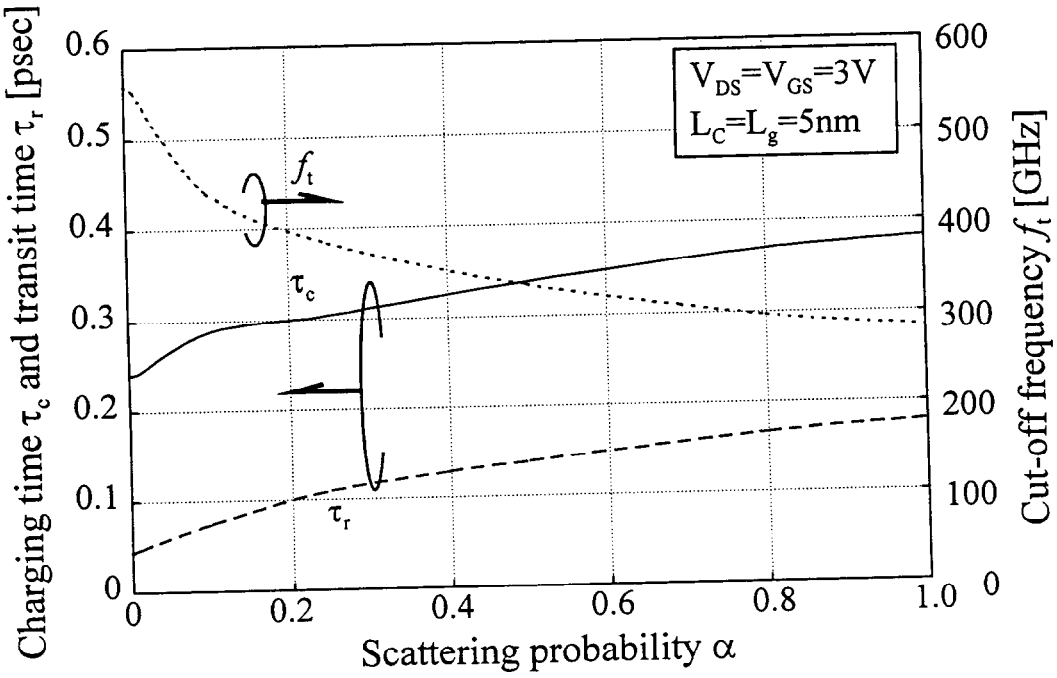


Figure 4.16: Charging time τ_c, transit time τ_r and cut-off frequency f_t as functions of the electron scattering probability α.

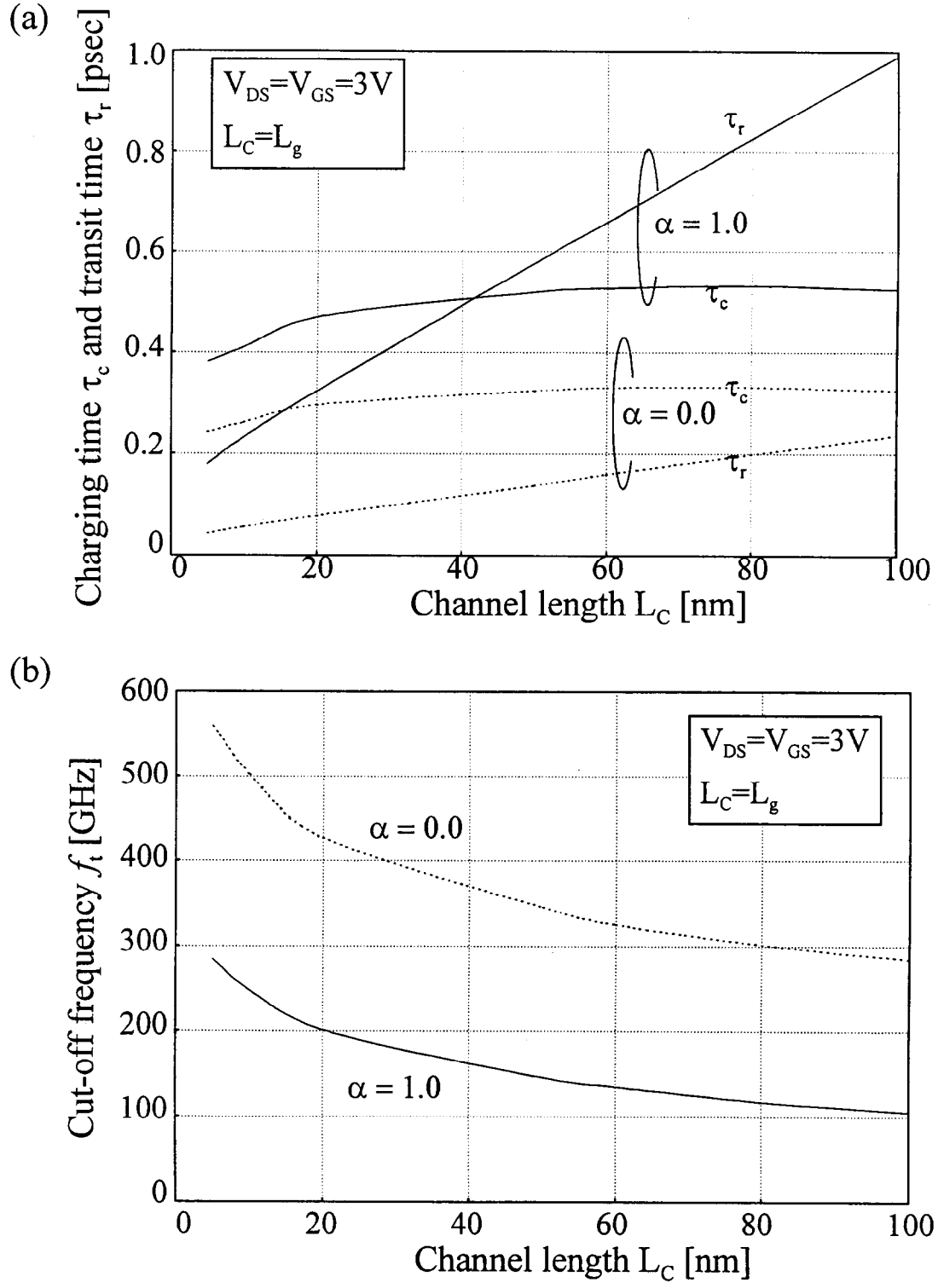


Figure 4.17: (a) Charging time τ_c, transit time τ_r and channel length L_C for different electron scattering probabilities α. (b) Cut-off frequency f_t and channel length L_C for different electron scattering probabilities α. The gate length L_g is assumed to be the same as the channel length L_C.

4.6 Application to Quantum Effect Device

VTFET is composed with nm-thick multi-layered structure. By according to multi quantum well structure, VTFET is applicable to the quantum effect device. For example, the injection of electrons from the source to the channel becomes resonant tunneling at the multi quantum well channel structure [39]. In addition, electron waveguide device can be realized at nm-long channel device, because carriers are not almost scattered in the very short channel. Several electron waveguide devices have been proposed and demonstrated [138]–[147]. VTFET can be according to the quantum interference device by attaching the other gate [69]. Figure 4. 18 shows the device structure of quantum interference device. This device is composed with VTFET and control gate region. At control gate region, the quantum interference of electrons in the double quantum well occurs [138, 139]. By this interference, the transmission probability of electrons in the channel toward the drain is modulated. The drain current is controlled by the control gate voltage, because control gate voltage modulates the interference during the double quantum well region. The calculation results of this device are shown in Fig. 4. 19. The control gate voltage is assumed to be same as drain voltage. The characteristics show transistor action with NDR. Using this device, bi-stable condition can be realized. and device number in the circuit is decreased, as described in Chap. 1 [43, 44, 36].

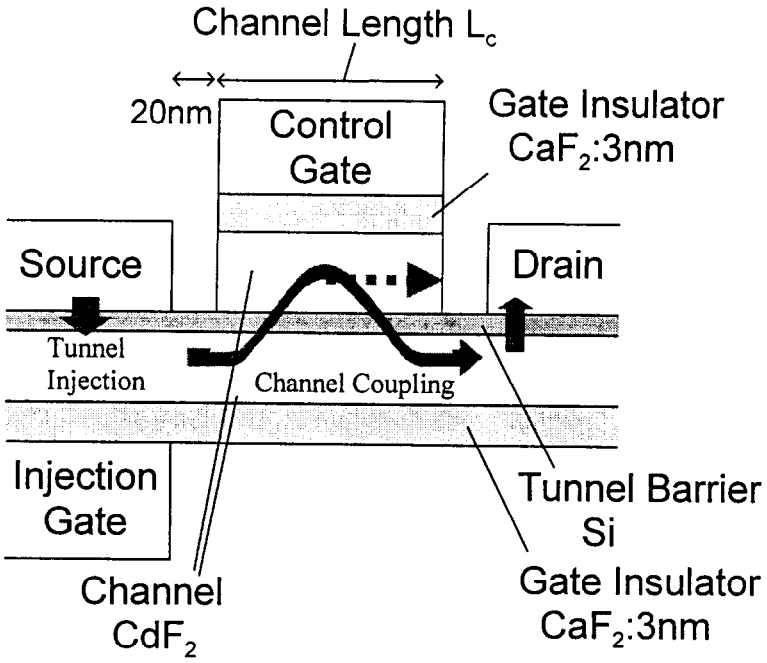


Figure 4.18: Device structure of quantum interference device.

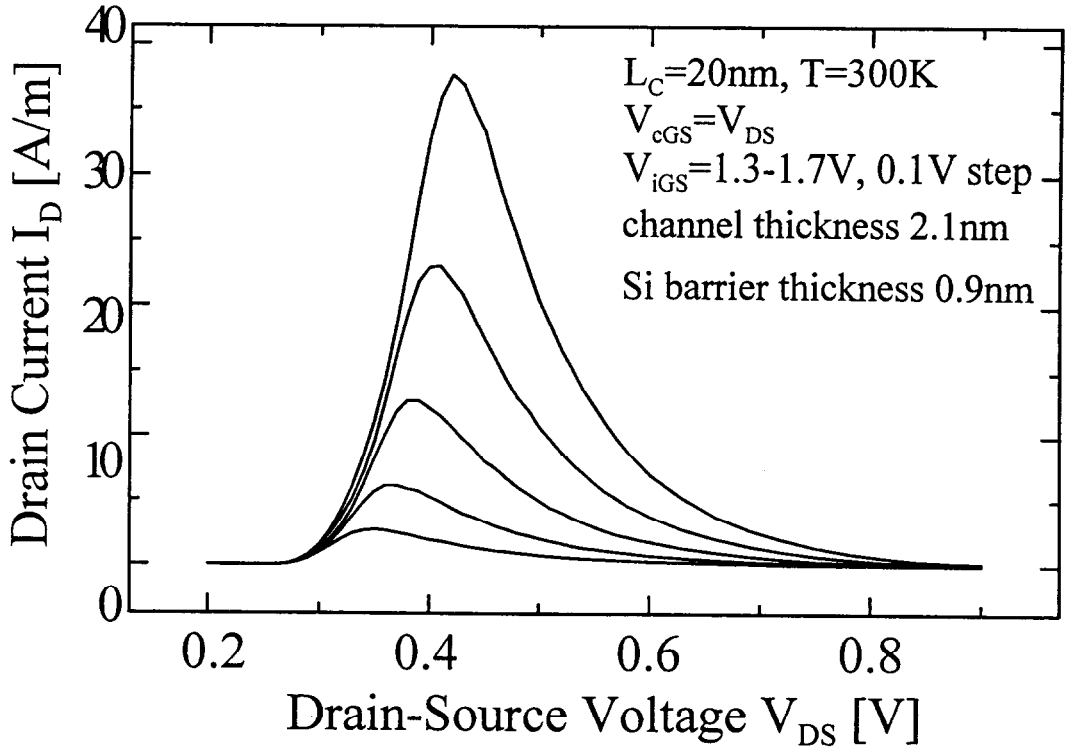


Figure 4.19: Calculated common-source characteristics as a function of injection voltage V_{iGS}.

4.7 Conclusion

Very short channel vertical tunneling field effect transistor (VTFET) using new heterostructures ($CoSi_2/Si/CdF_2/CaF_2$) on a Si substrate were proposed and analyzed. This VTFET may be very attractive for highly integrated circuits, because it has characteristics similar to those of conventional MOSFETs even with channel lengths of 5 nm. The subthreshold characteristics for VTFET with very short channel was discussed. At the VTFET, degradation by short channel effect is weaker than conventional SOI-MOSFET. The short channel effect can be suppressed even with 10 nm. We have estimated the theoretical response time and showed that this device has the possibility of subpicosecond response. The influence of carrier scattering in the channel was estimated. When all the tunneling electrons are scattered in the channel, the cut-off frequency for a 5-nm-long channel is reduced by a factor of two compared to the value without scattering. Also, this device has the potential for applications in novel field effect Si-based quantum devices, such as resonant tunneling and interference devices with CdF_2/ Si multiquantum well structures.

Chapter 5

Fabrication of Field Effect Transistor with New Heterostructure System

5.1 Introduction

Proposal and analysis of VTFET with new heterostructures on Si substrate were described in Chap. 4. Analytical results show that VTFET has potential of the operation with nm-size structure. Epitaxial growth of $CoSi_2/CaF_2$, $CoSi_2/Si$ and CdF_2/CaF_2 heterostructures on Si has been developed [64]–[68], while VTFET is composed with $CoSi_2/Si/CdF_2/CaF_2$ heterostructures. In addition, the device applications of $CoSi_2/Si$ and $CoSi_2/CaF_2$ heterostructures have been reported [48, 49, 148]. Recently, room temperature operation of resonant tunneling diodes using a CdF_2/CaF_2 superlattice grown on Si was reported [46, 149]. CdF_2 has been investigated as a new electrical and optical material, because doped CdF_2 has conductivity and visible luminescence [150]–[154]. However, there is no report on the planar device with CdF_2/CaF_2 heterostructure.

In this chapter, electrical characteristics of field effect transistors (FETs) using CdF_2/CaF_2 heterostructures on a Si fabricated using electron beam lithography and low temperature process are described. The

operation principle of this FET is that the channel carriers from the source are controlled by the gate voltage, which is similar to that of conventional MOSFETs. This FET is a fundamental structure of the proposed VTFET, and is composed of the same materials as the VTFET except for the Si tunneling barrier layer.

5.2 Device Structure

The device structure of the FET and its band diagram are shown in Fig. 5. 1 [123]. A highly doped n-type ($N_D \sim 1 \times 10^{19}$ cm^{-3}) Si substrate is used for the gate. The gate insulator is a 5 nm-thick layer of CaF_2, the channel is a 5 nm-thick layer of CdF_2 and the source and drain are Au/Cr. The channel length L_C is 100 nm, and the channel width W_C is 220 μm. In operation, electrons are injected from the source to the channel by the gate voltage, and then flow towards the drain under the influence of the drain voltage. Figure 5. 2 shows theoretical characteristics with common-source. These were calculated using a model for conventional MOSFET. In this calculation, electron mobility in CdF_2 was assumed to be 10 $cm^2V^{-1}s^{-1}$ [150] and influence of Schottky contact was neglected. The threshold voltage was assumed to be 2.1 V, which was considered with CaF_2/n-Si junction.

5.3 Fabrication Process

Firstly, the CdF_2/CaF_2 heterostructures were grown on a n-Si(111) substrate. The epitaxial growth system is illustrated in Fig. 5. 3. The system was evacuated by an ion pump to a background pressure of less than 1×10^{-9} Torr. The CaF_2 and CdF_2 layers were deposited from solid sources using graphite and CaF_2 crucibles, respectively. Before deposi-

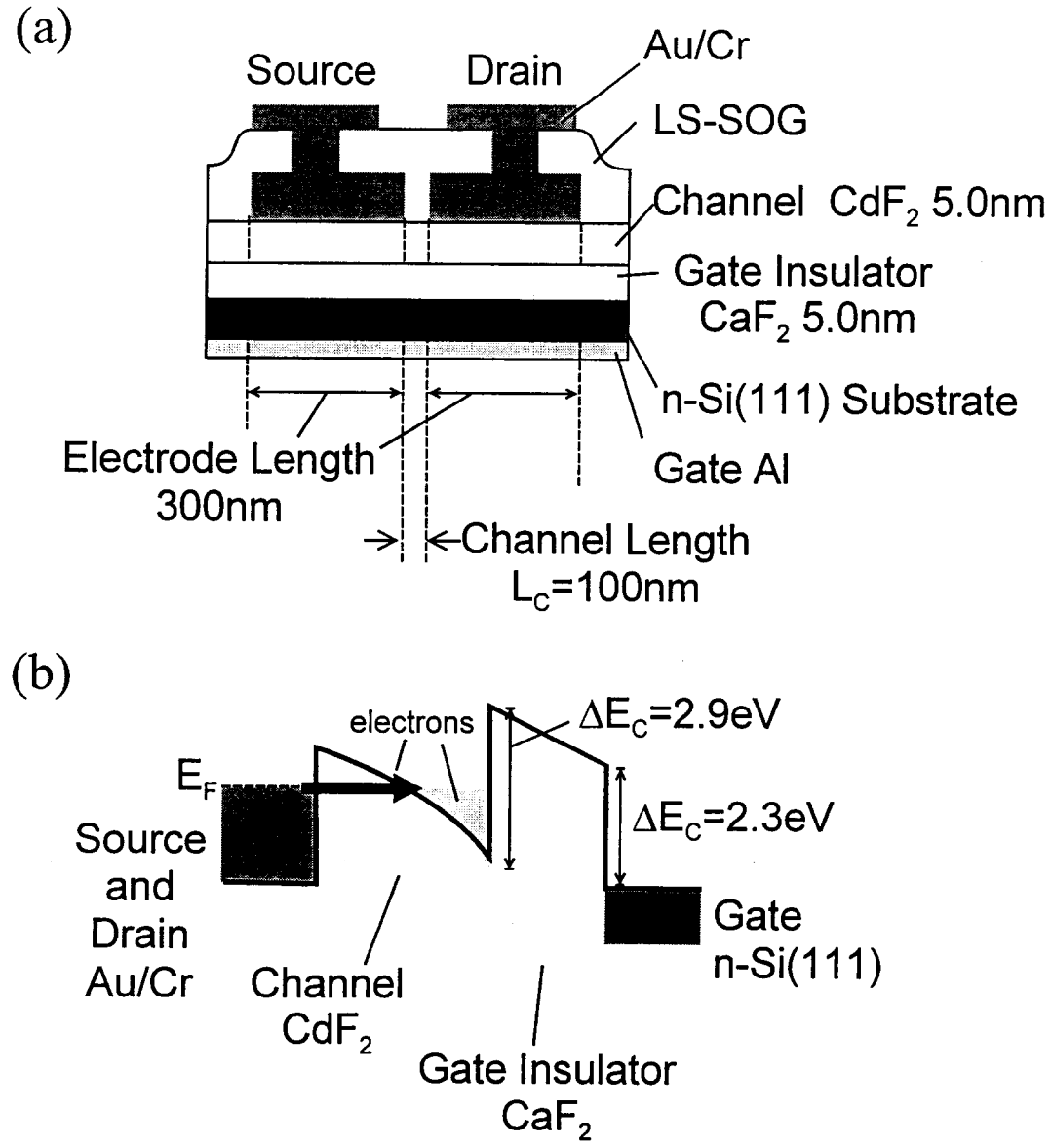


Figure 5.1: (a) Cross section of the structure of the field effect transistor. (b) Conduction band diagram in the vertical direction of (a).

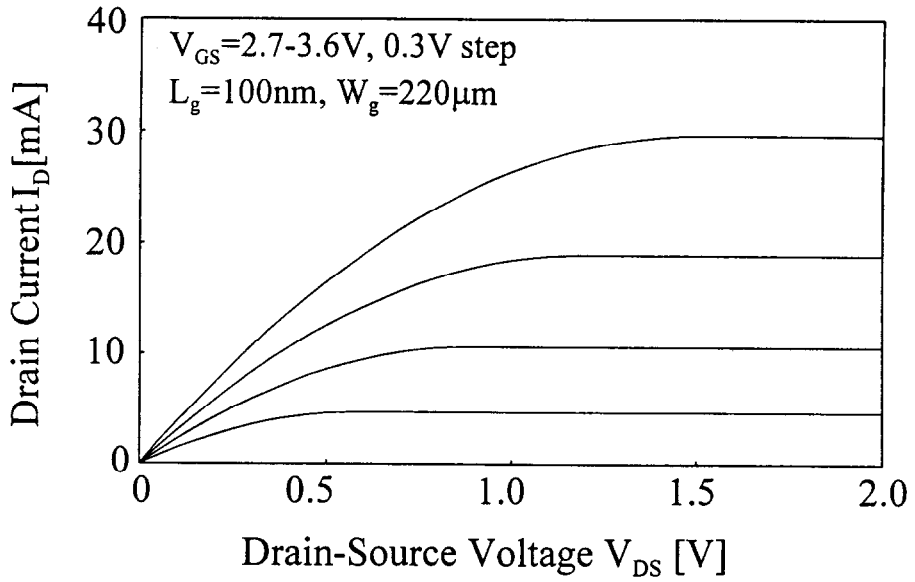


Figure 5.2: Theoretical characteristics with common-source as a function of gate-source voltage V_{GS}.

tion the substrate was chemically cleaned and a protective oxide layer was grown [120]. Then, it was loaded into the growth chamber through a load lock, heated to 750°C and exposed to a Si beam to evaporate the protective oxide layer. This process yielded a well-developed 7×7 reflection high-energy electron diffraction (RHEED) pattern. The CaF_2 layer was grown at a substrate temperature of 750°C by ionized beam epitaxy and the CdF_2 was grown on the CaF_2 at 50°C by molecular beam epitaxy [68]. Figure 5. 4 shows RHEED pattern and atomic force microscope image of grown CdF_2 layer on CaF_2/Si. A streaky RHEED pattern, which indicates single crystal and flat surface AFM image of the CdF_2 layer were observed. The surface roughness was less than 1.0 nm.

The fabrication process was shown in Fig. 5. 5. CdF_2 is dissolved by water and transforms at high temperature, more than 300 °C [155]. From these demerits, the device using CdF_2 must be fabricated by water-free and low temperature process. For the water-free process, dry etching was

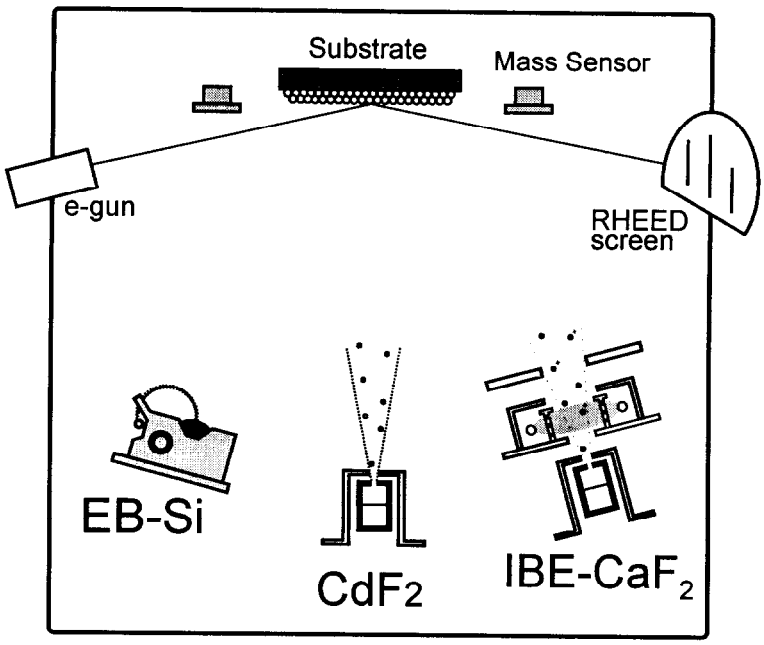


Figure 5.3: Schematic diagram of the growth chamber.

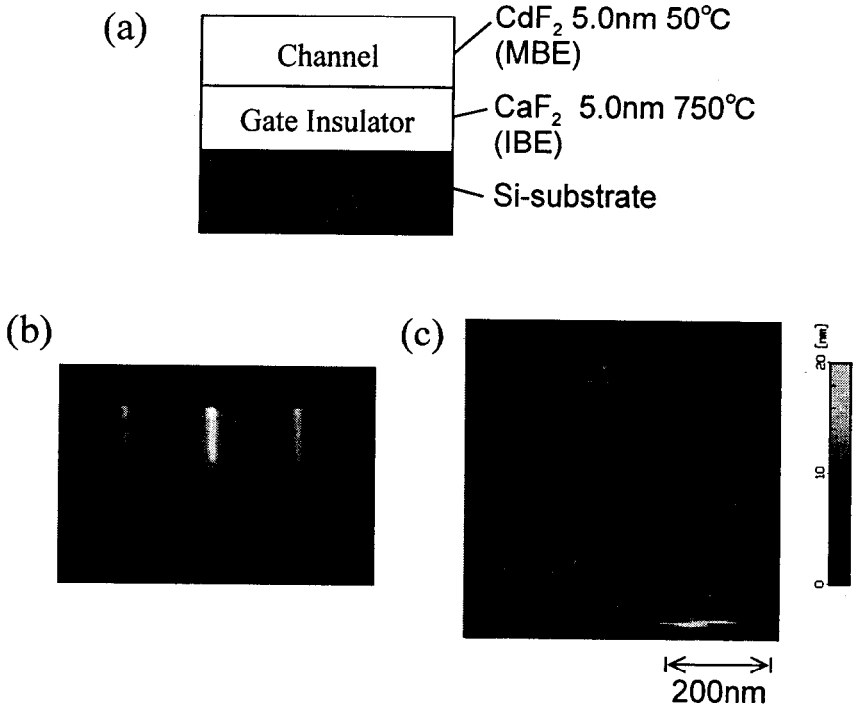


Figure 5.4: (a)Cross-section grown structure, (b)RHEED pattern and (c)AFM image of the surface of the grown CdF_2/CaF_2 heterostructures on Si(111) substrate.

used without wet etching. And electron-beam lithography with PMMA resist was used for formation of device pattern, because developer and rinse for PMMA resist are MIBK and IPA, respectively. In addition, LS-SOG was used for isolation layer material, because that can be cured at low temperature (200 °C). Source and drain were formed with Au/Cr using e-beam evaporation and lift-off process. Figure 5. 6 shows a SEM view of the resulting FET.

The detailed fabrication process steps after epitaxial growth of CdF_2/CaF_2 heterostructures on Si substrate are given as follows, where five steps are included, as shown in Fig. 5. 5.

- **Formation of alignment marks for direct write lithography and source/drain**

  1. e-beam lithography

     a. 1:1 PMMA spin coating

     1000 rpm. 1 sec. + 2000 rpm. 60 sec.

     b. Pre-baking for 60 min. at 170 °C

     c. Dose 600 $\mu C/cm^2$

     d. Development

     MIBK:IPA=1:3 45 sec., IPA 15 sec.

  2. e-beam evaporation

     60 nm-thick Au/10 nm-thick Cr evaporation

  3. Lift-off process

     Boiling acetone at 120 °C

- **Coating of isolation layer**

  1. 5% LS–SOG spin coating

     1000 rpm. 1sec. + 7000 rpm. 30 sec.

2. Baking at 200 °C 30 min.

- **Opening of contact holes**

1. e-beam lithography

   a. Cleaning by boiling acetone at 120 °C

   b. Baking for drying at 120 °C 10 min.

   c. 100% PMMA spin coating

   1000 rpm. 1 sec. + 2000 rpm. 60 sec.

   d. Pre-baking for 60 min. at 170 °C

   e. Dose 800 $\mu C/cm^2$

   f. Development

   MIBK:IPA=1:3 45 sec., IPA 15 sec.

   g. Post-baking for 20 min. at 120 °C

2. Etching of SOG by RIE

   Etching : CF_4 3 Pa, 20 W, 7 min 30 sec.

   Cleaning : O_2 3 Pa, 20 W, 3 min.

3. Removal of PMMA by boiling acetone

- **Formation of external electrode pad**

1. e-beam lithography

   a. Cleaning by boiling acetone at 120 °C

   b. Baking dry at 120 °C 10 min.

   c. 100% PMMA spin coating

   1000 rpm. 1 sec. + 2000 rpm. 60 sec.

   d. Pre-baking for 30 min. at 170 °C

   e. 100% PMMA spin coating

   1000 rpm. 1 sec. + 2000 rpm. 60 sec.

f. Pre-baking for 60 min. at 170 °C

g. Dose 550 $\mu C/cm^2$

f. Development

MIBK:IPA=1:1 45 sec., IPA 15 sec.

2. e-beam evaporation

300 nm-thick Au/10 nm-thick Cr evaporation

3. Lift-off process

Boiling acetone at 120 °C

- **Contact of gate electrode**

1. Cleaning of back of a substrate

a. Cleaning by boiling acetone at 120 °C

b. Baking dry at 120 °C 10 min.

c. 100% PMMA spin coating

1000 rpm. 1 sec. + 2000 rpm. 60 sec.

d. Pre-baking for 60 min. at 170 °C

e. Cleaning by O_2 ashing

O_2 3 Pa 20 W 6 min.

f. Etching of oxide

CF_4 3 Pa 60 W 10 min.

2. Evaporation

100 nm-thick Au/500 nm-thick Al evaporation

3. Removal of PMMA by boiling acetone

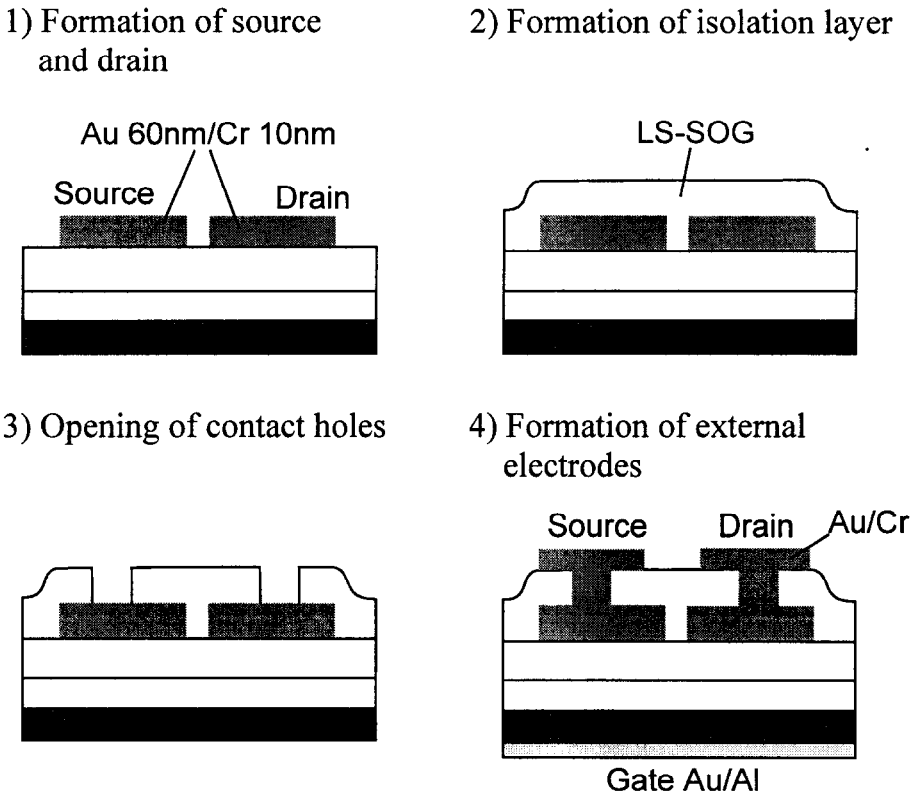


Figure 5.5: Fabrication process of the field effect transistor with CdF_2/CaF_2 heterostructures on Si(111).

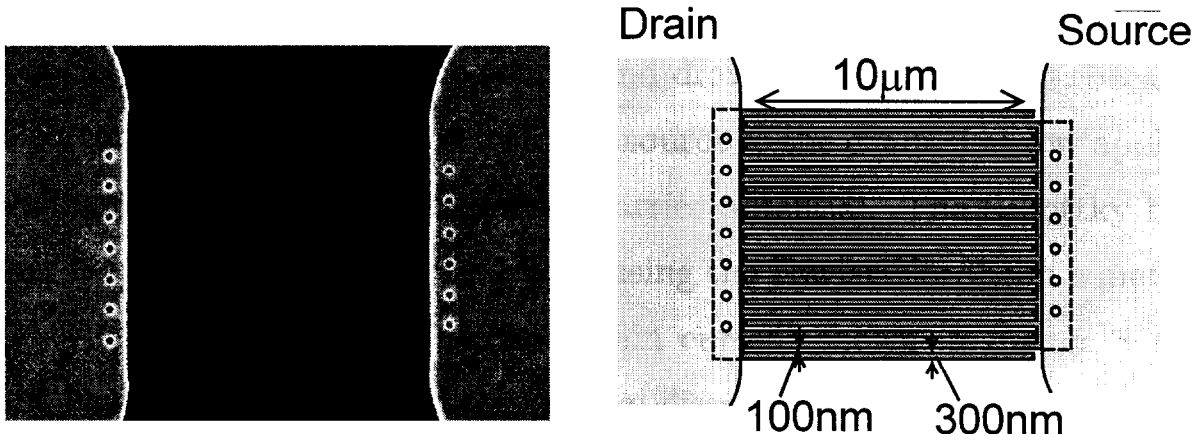


Figure 5.6: SEM planview and schematic illustration of the field effect transistor. The channel length is 100 nm and total channel width is 220 μm.

5.4 Measured Characteristics

Figure 5. 7 shows the common-source characteristics at 16 K for the drain current I_D and gate current I_G versus the drain-source voltage V_{DS} for various values of the gate-source voltage V_{GS}. These characteristics show modulation of the drain current with the gate-source voltage. At $V_{DS} = 4.5$ V and $V_{GS} = 3.9$ V, the drain current is 16 nA and the transconductance g_m is 28 nS. However, the measured drain current includes a leakage current generated by defects in the epitaxial layer, because the gate current is of the same order as the drain current. The leakage current is estimated from the modulation of the gate current by V_{DS}, because it is expected that leakage current flows between the drain and the gate through the epitaxial layer. The characteristics of the intrinsic drain current with the leakage current suppressed are shown in Fig. 5. 8. In these characteristics, modulation of the drain current by V_{GS} is also observed. The measured drain current is very small ($\sim$nA) and the operating voltage is larger than 2 V. These are very different from theoretical characteristics, as shown in Fig. 5. 2. The characteristics are degraded by the Schottky contact at the source and drain/channel interface, because electrons cannot be injected from the source to the channel at low applied voltages due to the high Schottky barrier potential. The Schottky barrier height is estimated to be 1.2 eV using the Fowler-Nordheim equation [156] obtained from the intrinsic drain current shown in Fig. 5. 8 and the channel electric field in the vertical direction, which depends on V_{GS}, where the drain current is equated with the tunneling current from the source to the channel through the Schottky barrier. In a previous paper, respective Schottky barrier heights of 0.8 and 1.4 eV for Al/CdF_2 and Au/CdF_2 were reported [157]. From these results, the Schottky barrier

heights in metal/CdF_2 junctions follow the metal work function, as shown in Fig. 5. 9. Therefore, in principle, low voltage operation and large drain current can be realized using a low work-function metal such as Er and Eu. Moreover, the interfacial trapping density at source/channel and drain/channel interface influences to the gate modulation, because potential between gate and source region can be not controlled with good efficiency by applied voltage [158]. The cleaning process before evaporation is necessary for formation of ideal metal/CdF_2 junction.

5.5 Conclusion

One-hundred-nanometre-long channel field effect transistors using CdF_2/CaF_2 heterostructures on a Si substrate were fabricated using electron beam lithography. Modulation of the drain current with the gate-source voltage was observed at 16 K. The measured drain current was very small ($\sim$nA) because of the Schottky contact at the source-to-channel and drain-to-channel interfaces.

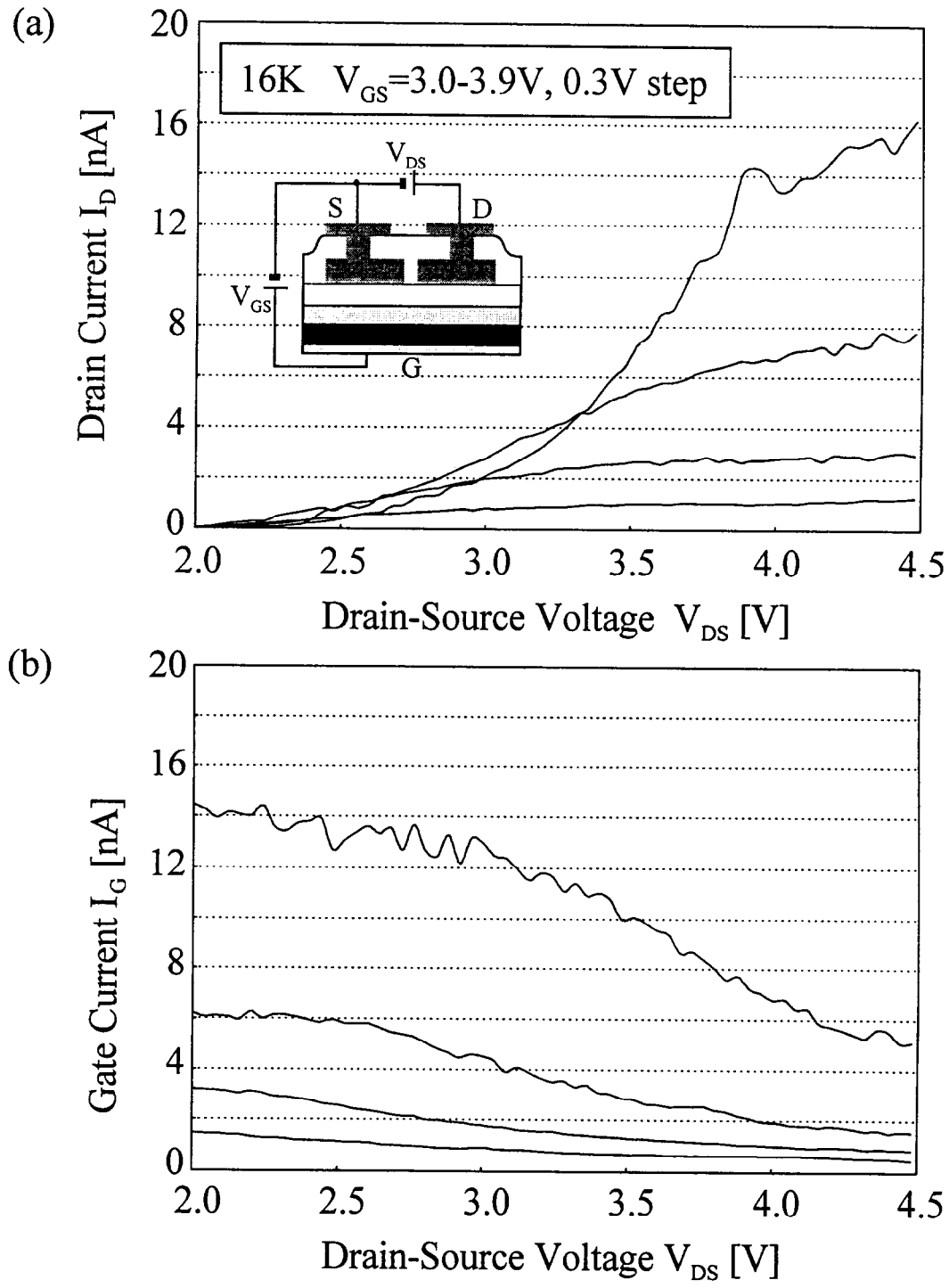


Figure 5.7: Common-source characteristics (a) $I_D - V_{DS}$ (b) $I_G - V_{DS}$ of the CdF_2/CaF_2 field effect transistor at 16 K for various values of V_{GS}.

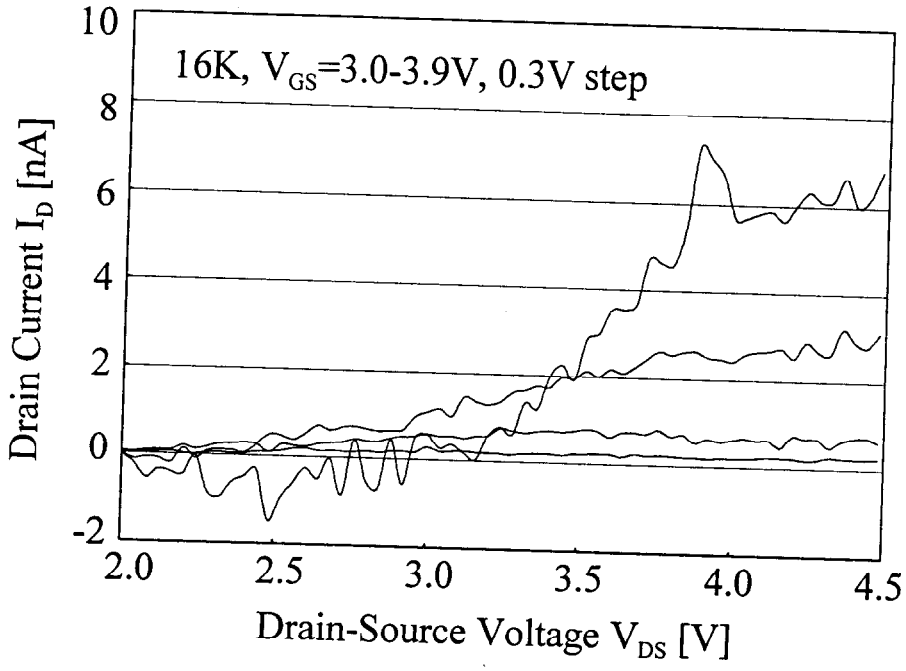


Figure 5.8: Intrinsic common-source characteristics without leakage current. It is assumed that the leakage current is the modulation of the gate current by the drain-source voltage shown in Fig. 5. 7(b).

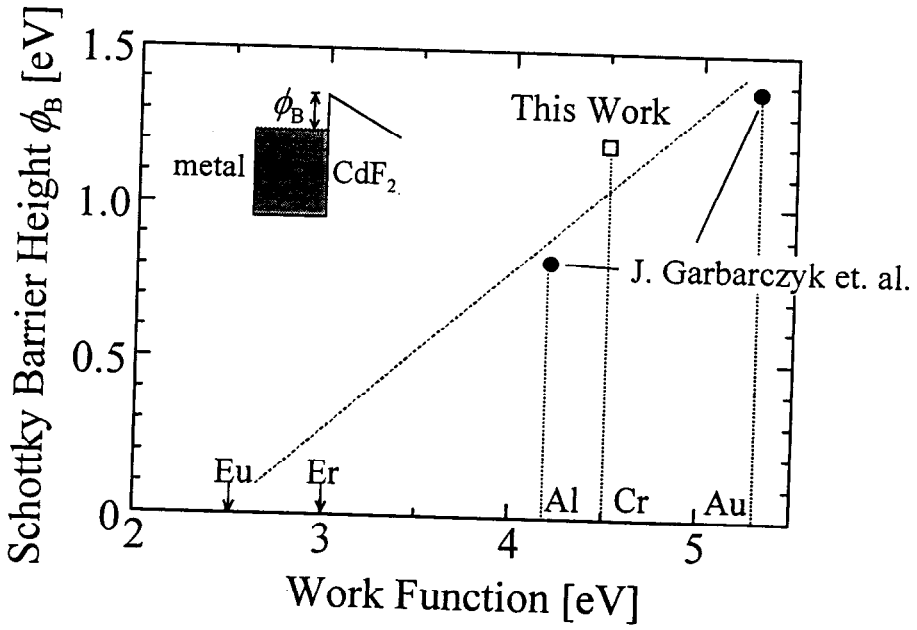


Figure 5.9: Relation between metal work function and Schottky barrier height at metal/CdF_2 junction.

Chapter 6

Conclusions

In this work, a tunneling field effect transistor with metal source/drain (S/D) and gate and an un-doped channel was studied as a nm-size device for use in high-performance and high-integrated LSI. Schottky S/D MOSFETs and vertical tunneling field effect transistors (VTFETs) with $CoSi_2/Si/CdF_2/CaF_2$ heterostructures, which can be grown on a Si substrate, were studied. For each device, degradation of the characteristics for very short channel structures was analyzed theoretically. From a comparison between conventional MOSFETs and tunneling FETs, the advantage of these tunneling devices with very short channel structures was shown theoretically. Very short metal gate Schottky S/D MOSFETs were fabricated on a SIMOX substrate, and room temperature operation of a 25 nm-long gate device was demonstrated. CdF_2/CaF_2 heterostructures, which were a fundamental structure of the proposed VTFET were grown on a Si substrate and primitive field effect transistor action with these heterostructures was demonstrated.

Detailed results are summarized as follows:

[1]The Schottky S/D MOSFET was analyzed theoretically and the characteristics of Schottky S/D MOSFETs were compared with those of conventional MOSFETs.

(1-a) The characteristics of Schottky S/D MOSFETs depend strongly on the Schottky barrier height. The current drivability and the on/off ratio increase with lower Schottky barriers. Drivability comparable to conventional MOSFETs, whose channel length is less than 30 nm, can be realized, when the Schottky barrier heights are 0.25 for p-type and 0.1–0.15 eV for n-type devices, respectively.

(1-b) The threshold voltage shift of Schottky S/D MOSFETs by the short channel effect is smaller than that of conventional MOSFETs. The subthreshold swing of the Schottky S/D MOSFET even with a long channel is larger than that of a conventional MOSFET. To reduce the subthreshold swing, the gate oxide must be thinned.

(1-c) Thinning of the gate oxide and the SOI layer is effective in suppressing the short channel effect. The short channel effect can be suppressed even with a 15 nm-long channel at t_{OX} = 1 nm and t_{SOI} = 3 nm.

[**2**]Very short metal gate Schottky S/D MOSFETs were fabricated on a SIMOX substrate, and room temperature operation of the devieces was demonstrated.

(2-a) 50 nm-long channel devices were fabricated by a simple process, which involved only SiO_2 sputtering for the gate oxide and a lift-off process for the electrodes. A large on/off ratio was achieved even with a very short channel using a thin SOI structure. At V_{DS} = –1.0 V, the on/off ratios were 750 and 10^4 for 50 and 75 nm-long channel devices, respectively.

(2-b) 25 nm-long metal gate Schottky S/D MOSFETs were fabricated by electron-beam lithography with PMMA resist and a self aligned

silicide process. $ErSi_2$ and PtSi, which have low Schottky barriers were used for n-type and p-type S/Ds, respectively.

(2-c) Room temperature operation of a 25 nm-long gate n-type $ErSi_2$ Schottky S/D MOSFET was demonstrated. At $V_{GS} = V_{DS} = 2$ V, the drain current was 75 μA/μm and the transconductance was 9.5 mS/mm.

(2-d) Room temperature operation of a 35 nm-long gate p-type PtSi Schottky S/D MOSFET was achieved. At $V_{GS} = V_{DS} = -1.5$ V, the drain current was -176 μA/μm and the transconductance was 390 mS/mm. Drivability comparable with conventional MOSFETs was achieved. The on/off ratio was improved by using a very thin SOI structure.

(2-e) Comparison between theoretical and experimental characteristics shows the measured to be greater off current than the theoretical value. A possible explanation for this is that the off current is increased through interfacial traps due to the surface roughness and metallic contamination. The characteristics can be improved by a cleaning process before S/D formation.

[3]A Vertical tunneling field effect transistor (VTFET) with a $CoSi_2/Si/CdF_2/CaF_2$ heterostructures, which can be grown on a Si substrate was proposed and analyzed. The potential of the device operation with nm-channel was shown theoretically.

(3-a) The drain curves of VTFETs are very similar to those of conventional MOSFETs even with a channel length of 5 nm.

(3-b) With increasing gate length, the drivability and subthreshold characteristics can be improved. The short channel effect can be sup-

pressed even with a channel length of 10 nm.

(3-c) The response time of VTFETs was estimated. The response time almost depends on charging time. The cut-off frequency is 550 and 430 GHz for 5 and 20 nm-long channel devices, respectively.

(3-d) The influence of carrier scattering in the channel was analyzed. The transconductance and carrier velocity are decreased with increasing channel carrier density due to carrier scattering in the channel. When all the tunneling electrons are scattered in the channel, the cut-off frequency for a 5 nm-long channel is reduced by a factor of two compared to the value without scattering.

(3-e) The application to novel field effect Si-based quantum devices with a multi quantum well channel was shown. Transistor action with a negative differential resistance can be realized by quantum interference in a double quantum well channel. The number of devices in the circuit can be reduced using this quantum device.

[4]A CdF_2/CaF_2 heterostructure, which is the fundamental structure of the proposed VTFET was grown on a Si substrate and primitive field effect transistor action with this heterostructure was demonstrated.

(4-a) CdF_2/CaF_2 heterostructures were grown on Si substrates and 100 nm-long channel field effect transistors were fabricated on these substrates using a low temperature process and electron beam lithography to suppress degradation of the grown CdF_2 film.

(4-b) Modulation of the drain current with the gate-source voltage was observed at 16 K. The measured drain current was very small ($\sim$nA) due to the Schottky contact at the source-to-channel and drain-to-channel interfaces. The Schottky barrier height was estimated to be

about 1.2 eV from the characteristics. Low voltage operation and large drain current can be realized using a low work-function metal, because the Schottky barrier heights in metal/CdF_2 junctions follow the metal work function.

From these results, the potential for scaling into the nm regime of the tunneling field effect transistor with a metal S/D and gate and an un-doped channel was shown.

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Publication List

Journal Papers

(1) W.Saitoh, T. Suemasu, Y. Kohno, M. Watanabe and M. Asada, "Fabrication and Characteristics of Metal ($CoSi_2$)/Insulator (CaF_2) Hot Electron Transistor Using Electron-Beam Lithography on Si Substrate," *Jpn. J. Appl. Phys.*, 34 (1995) pp.L1254–L1256. (Letter)

(2) W.Saitoh, K. Yamazaki, M. Asada and M. Watanabe, "Proposal and Analysis of Very Short Channel Field Effect Transistor Using Vertical Tunneling with New Heterostructures on Silicon," *Jpn. J. Appl. Phys.*, 35 (1996) pp.L1104–L1106. (Letter)

(3) W.Saitoh, K. Mori, H. Sugiura, T. Maruyama, M. Watanabe and M. Asada, "Reduction of Electrical Resistance of Nanometer-Thick $CoSi_2$ Film on CaF_2," *Jpn. J. Appl. Phys.*, 36 (1997) pp.4470–4471. (Short Note)

(4) W.Saitoh, K. Yamazaki, M. Tsutsui and M. Asada, "Analysis of Structure Dependence of Very Short Channel Field Effect Transistor Using Vertical Tunneling with Heterostructures on Silicon," *IEICE Trans. Electro. of Jpn.*, E81-C, (1998) pp.1918–1925. (Paper)

(5) W.Saitoh, K. Yamazaki, M. Tsutsui and M. Asada, "Analysis of the Influence of Carrier Scattering in the Channel of a Metal/Insulator Tunneling Field Effect Transistor," *Jpn. J. Appl. Phys.*, 37 (1998) pp.5921–5925. (Paper)

(6) W.Saitoh, K. Yamazaki, M. Tsutsui, A. Itoh and M. Asada, "Fabrication and Characteristics of a Field Effect Transistor using CdF_2/CaF_2 Heterostructures on a Si Substrate," *Jpn. J. Appl. Phys.*, 37 (1998) pp.L1138–L1140. (Letter)

(7) W.Saitoh, S. Yamagami, A. Itoh and M. Asada, "35 nm Metal Gate p-type MOSFET with PtSi Schottky Source/Drain on SIMOX substrate," submitted to *Jpn. J. Appl. Phys.* (Letter)

(8) W.Saitoh, A. Itoh, S. Yamagami and M. Asada, "Analysis of Short Channel Schottky Source/Drain MOSFET on SOI Substrate and Fabrication of sub 50 nm n-type devices with metal gate," submitted to *Jpn. J. Appl. Phys.* (Paper)

(9) K. Mori, W.Saitoh, T. Suemasu, Y. Kohno, M. Watanabe, and M. Asada, "Room-Temperature Observation of Multiple Negative Differential Resistance in a Metal($CoSi_2$)/ Insulator(CaF_2) Quantum Interference Transistor Structure," *Physica B*, 227 (1996) pp.213–215. (Paper)

(10) M. Watanabe, W.Saitoh, Y. Aoki and J. Nishiyama, "Epitaxial Growth of Nanometer-Thick CaF_2/CdF_2 Heterostructure using Partially Ionized Beam Epitaxy," *Solid State Elec.*, 42 (1998) pp.1627–1630. (Paper)

(11) M. Tsutsui, W.Saitoh, K. Yamazaki and M. Asada, "Proposal and Analysis of Coupled Channel Tunneling FET with New Heterostructures on Silicon," *Solid State Elec.*, 42 (1998) pp.1547–1551. (Paper)

(12) M. Watanabe, Y. Aoki, W.Saitoh and M. Tsuganezawa, "Negative Differential Resistance of CaF_2/CdF_2 Triple Barrier Resonant Diode on Si(111) Grown by Partially Ionized Beam Epitaxy," *Jpn. J. Appl. Phys.*, 38 (1999) (to be published). (Letter)

Related Works

(1) W.Saitoh, T. Suemasu, Y. Kohno, M. Watanabe and M. Asada, "Mulitiple Negative Differential Resistance Due to Quantum Interference of Hot Electron Waves in Metal ($CoSi_2$)/Insulator (CaF_2) Heterostructures and Influence of Parasitic Elements," *Jpn. J. Appl. Phys.*, 34 (1995) pp.4481–4482. (Paper)

(2) T. Suemasu, Y. Kohno, W.Saitoh, N. Suzuki, M. Watanabe and M. Asada, "Quantum Interference of Electron Wave in Metal ($CoSi_2$)/Insulator (CaF_2) Resonant Tunneling Hot Electron Transistor Structure," *Jpn. J. Appl. Phys.*, 33 (1994) pp.L1762–L1765. (Letter)

(3) T. Suemasu, Y. Kohno, W.Saitoh, M. Watanabe and M. Asada, "Theoretical and Measured Characteristics of Metal ($CoSi_2$)/Insulator (CaF_2) Resonant Tunneling Transistors and the Influence of Parasitic Elements," *IEEE Trans. Electron Devices*, 42 (1995) pp.2203–2210. (Paper)

(4) M. Asada, M. Watanabe, T. Suemasu, Y. Kohno and W.Saitoh, "Epitaxial Growth of a Metal ($CoSi_2$)/Insulator (CaF_2) Nanometer-Thick Heterostructure and its Application to Quantum-Effect Devices," *J. Vac. & Sci. Technol.*, A13(3), (1995) pp.623–628. (Paper)

(5) T. Suemasu, W.Saitoh, Y. Kohno, K. Mori, M. Watanabe and M. Asada, "Transfer Efficiency of Hot Electron in a Metal($CoSi_2$)/ Insulator(CaF_2) Quantum Interference Transistor," *Surf. Sci.*, 361/362 (1996) pp.209–212. (Paper)

(6) Y. Miyamoto, A. Yamaguchi, K. Ohshima, W.Saitoh and M. Asada, "Metal-Insulator-Semiconductor Emitter with an Epitaxial CaF_2 Layer as the Insulator," *J. Vac. & Sci. Technol.*, B 16(2) (1998) pp.851–854. (Paper)

(7) M. Asada, K. Osada and W.Saitoh, "Fabrication and Analysis of Small Area Metal/Insulator Resonant Tunneling Diode Integrated with Patch Antenna for Terahertz Photon Assisted Tunneling," *Solid State Elec.*, 42 (1998) pp.1543–1546. (Paper)

(8) N. Kikegawa, B. Zhang, Y. Ikeda, N. Sakai, K. Furuya, M. Asada, M. Watanabe, and W.Saitoh, "Detection Time Shorting for Observation of Hot Electron Spatial Distribution by Scanning Hot Electron Microscope," *Jpn. J. Appl. Phys.*, (1998) (to be published). (Paper)

International Conferences

(1) W.Saitoh, T. Suemasu, Y. Kohno, M. Watanabe and M. Asada, "Metal ($CoSi_2$)/Insulator (CaF_2) Hot Electron Transistor Using Electron-Beam Lithography on Si Substrate," *25th European Solid State Device Research Conference*, Netherlands, P1.7, September 1995.

(2) W.Saitoh, Y. Aoki, J. Nishiyama, M. Watanabe and M. Asada, "Epitaxial Growth of $Si/CdF_2/CaF_2$ Heterostructures on Si Substrate," *Electronic Materials Conference*, Colorado U.S.A., U9, June 1997.

(3) T. Suemasu, W.Saitoh, Y. Kohno, M. Watanabe and M. Asada, "Multiple Negative Differential Resistance due to Quantum Interference of Hot Electron Waves in Metal ($CoSi_2$)/Insulator (CaF_2) Heterostructures," *International Workshop on Mesoscopic Physics and Electronics*, Tokyo, H-2, March 1995.

(4) T. Suemasu, Y. Kohno, W.Saitoh, K. Mori, M. Watanabe and M. Asada, "Metal ($CoSi_2$)/Insulator (CaF_2) Resonant Tunneling and Quantum Interference Transistors Grown on a Si Substrate," *2nd International Workshop on Quantum Functional Devices*, Matsue, S11, May 1995.

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(9) M. Asada, M. Watanabe and W.Saitoh, "Metal/Insulator/Semiconductor Heterostructure Quantum-Effect Devices on Si Substrate," (Invited) *Nanostructures: Physics and Technology*, Russia, SBNS. 01i, June 1997.

(10) Y. Miyamoto, A. Yamaguchi, K. Ohshima, W.Saitoh and M. Asada, "MIS Emitter with Epitaxial CaF_2 layer as Insulator," *10th International Vacuum Microelectronics Conference*, Korea, August 1997.

(11) M. Asada, K. Osada and W.Saitoh, "Small Area (1μm-Diam.) Metal/Insulator Resonant Tunneling Diode Applicable to Terahertz Devices," *International Workshop on Nano-Physics and Electronics*, Tokyo, G04, September 1997.

(12) M. Tsutsui, W.Saitoh, K. Yamazaki and M. Asada, "Proposal and Analysis of Coupled Channel Tunneling FET with New Heterostructures on Silicon," *International Workshop on Nano-Physics and Electronics*, Tokyo, X20, September 1997.

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Domestic Conferences and Meeting Reports

(1) W.Saitoh, T. Suemasu, Y. Kohno, M. Watanabe and M. Asada, "Analysis of Metal ($CoSi_2$)/Insulator (CaF_2) Resonant Tunneling Hot Electron Transistor Using Equivalent Circuit," 「金属（$CoSi_2$）／絶縁体（CaF_2）共鳴トンネルホットエレクトロン

トランジスタの等価回路モデルによる特性評価」*Nat. Conv. Rec. of IEICE Japan*, C-420, Sendai, September 1994.

(2) W.Saitoh, T. Suemasu, Y. Kohno, M. Watanabe and M. Asada, "Fabrication and Room Temperature Operation of Metal($CoSi_2$)/Insulator(CaF_2) Nanometer-Thick Small-Area Hot Electron Transistor," 「金属（$CoSi_2$）／絶縁体（CaF_2）微細ホットエレクトロントランジスタの作製と室温動作」*Nat. Conv. Rec. of The Japan Soc. of Appl. Phys.*, 30p-ZK-7, Kanagawa, March 1995.

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(5) W.Saitoh, K. Yamazaki, M. Tsutsui and M. Asada, "Analysis of Static Characteristics and Response Time of Very Short Channel Tunneling FET with $CoSi_2$/Si/CdF_2/CaF_2 Heterostructures on Si Substrate," 「Si基板上$CoSi_2$/Si/CdF_2/CaF_2ヘテロ構造を用いた極短チャネルトンネルFETの静特性と動作時間解析」*Nat. Conv. Rec. of IEICE Japan*, C-10-17, Oosaka, March 1997.

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