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A Study on Accurate and Efficient Compact Models for New Components used for Integrated Circuits

HITOSHI AOKI

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Chapter 1 Introduction

In electric or electronic circuit design it is important that a circuit is smoothly working with minimum breadboard fabrications. To reduce the number of breadboard fabrications the circuit could be verified and tested before the real fabrication work. Which is obvious especially for Large Scale Integrated Circuits (LSI's) design for these days. An LSI consists of a large number of transistors and parasitics. In order to make it operate to match the specification Computer Aided Design (CAD) tools are necessary. One of the CAD tools is circuit simulators that can accurately reproduce the real circuit operations as expected. Using the circuit simulator It is possible to reduce the number of breadboard fabrications. There are several kinds of circuit simulators from fundamental ones which can only predict dc currents and voltages, to advanced and large sized software programs which this paper will focuses on to simulate static and dynamic characteristics, accurately. As the advanced circuit simulators had been used only on expensive workstations about five years ago, we can use them even on PC now.

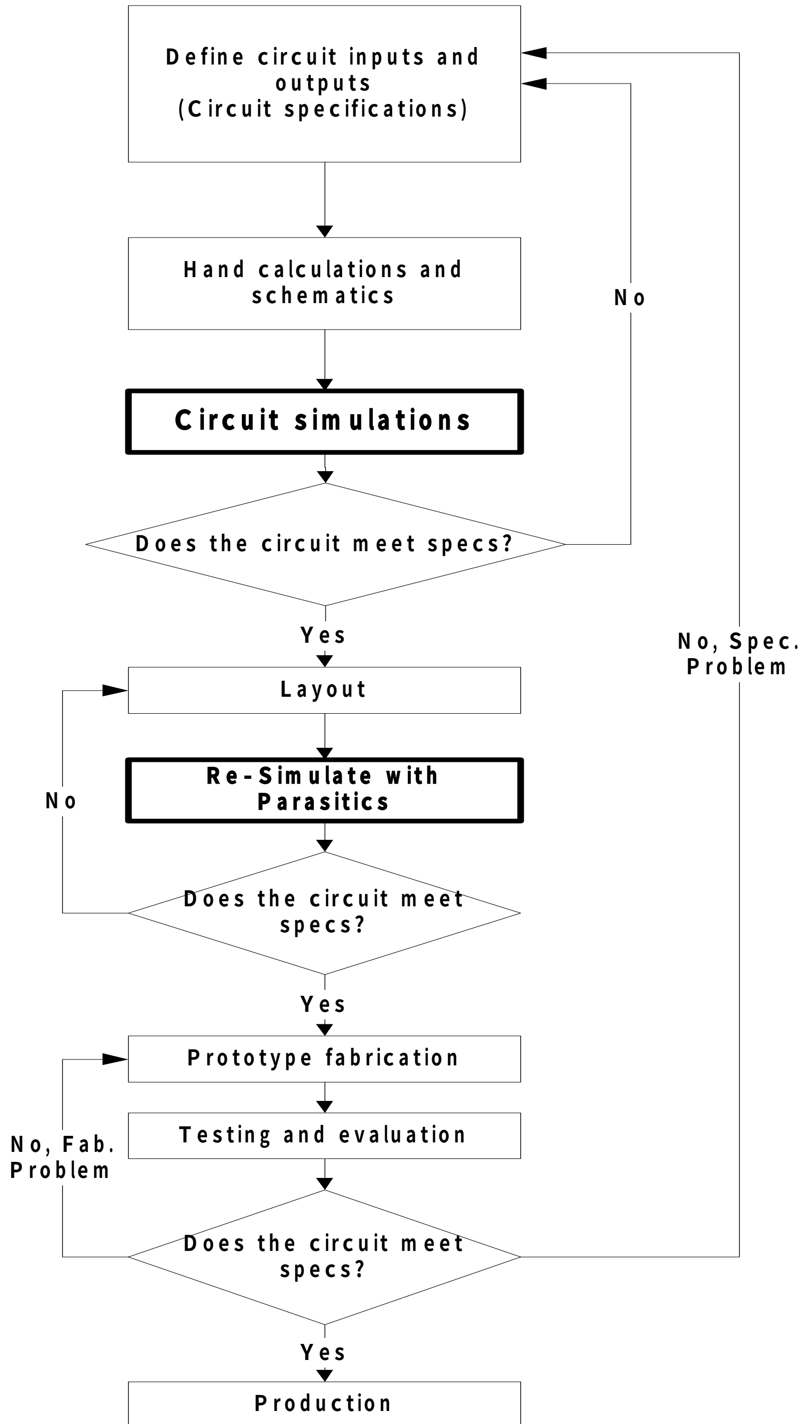


Fig. 1.1 Flowchart for the CMOS LSI design process

We mentioned the advantage of using circuit simulators for LSI design. The CMOS LSI circuit design process consists of defining circuit inputs and outputs, hand calculations, circuit simulations, layout of the circuit, simulations including parasitics, reevaluation of the circuit inputs and outputs, fabrication, and testing. A flowchart of this process is shown in Fig. 1.1. The circuit specifications are rarely set in concrete. They can change as the project matures. This can be the result of trade-offs made between cost and performance, changes in the marketability of the chip, or simply changes in the customer's needs. To design a chip of the LSI the engineer has to understand the parasitics involved in the layout. Parasitics are the stray capacitances, inductances, pn junctions, and bipolar transistors, with associated problems (breakdown, stored charge, latch-up, etc.). Such parasitics should be included in the circuit simulation topology to predict the circuit performance accurately. On the other hand for circuit simulators themselves the simulation accuracy, scattering of the process and device characteristics, and the errors of each simulator control the simulation results. Although such problems are always remaining, it is possible to improve simulation accuracy by enhancing simulation engines and algorithms. Actually in commercial circuit simulators that are mostly supplied by some CAD venders have enough simulation accuracies to be used for real LSI design work.

The accuracy of a circuit simulator is mainly determined by the accuracy of models and extracted parameters included. For silicon technologies major

physical problems were solved and these models in process and device simulators could adopt the physical equations as they are. Therefore, these simulators have enough accuracy to use them for semiconductor design works. On the other hand for circuit simulations, it is almost impossible to implement physical equations into circuit simulators without any modifications and simplifications. Since most of all circuit simulators use a combination of equivalent circuit and model equations, physical equations must be simplified by using approximation techniques. As a result, semiconductor device models for circuit simulators are not as accurate as process and device simulators'. Another issue for circuit simulations is the efficiency of circuit simulators. Convergence of the device model and the simulation engine is dominant to determine the efficiency.

SPICE (Simulation Program with Integrated Circuit Emphasis) [1] is the most popular and major circuit simulator in this field. It had been first developed by UCB (University of California, Berkeley). Later on many commercial versions were released based on UCB's source codes. As described above, the key issue to obtain an accurate circuit simulation result is how to make models of any circuit elements in SPICE close to real components in a circuit. For passive components such as resistors, inductor's, and capacitors it is relatively easy to simulate them in low frequency applications. In high frequency applications the equivalent circuits of lumped sum and electro-magnetic simulations of distributed constants have to be considered. For active compo-

nents, which are mainly semiconductor devices, such as bipolar junction transistors (BJT's), field effect transistors (FET's), and diode's the development of their models are very complicated and, therefore, difficult because they are non-linear devices.

These semiconductor device models are called as compact models since the size of the model source codes are usually smaller than process and device simulators'. Although research of the compact modeling has been active in the U.S.A. and in Europe, many problems are still remained in compact device modeling, which includes model development, model parameter extraction, and its measurement technologies.

1.1 Purpose of the Research

The research of this thesis focuses on the compact device modeling whose target devices are limited in semiconductor devices. The purpose of the research is to develop practical (accurate and efficient) models using device physics, electrical circuit analysis, and mathematical derivations and obtaining accurate and efficient (accurate and efficient) model parameters from measured data of target devices, whereas practical models of the devices have not been introduced yet in the circuit simulation community.

1.2 Research Background

Although SPICE is effectively used in some areas, there are several application areas which SPICE can exert a strong influence on. The main reason is that the device models are not developed or incomplete for the applications.

The objective of this thesis is to research models which had not been well developed in the application areas and to build and implement the new models. The modeling procedure includes to study the device physics, analyzing the electrical characteristics, formulating the model equations, designing the equivalent circuits, SPICE implement, and parameter extraction function development and executions. Also, the developed model and the parameters will be applied for real circuit design works.

The compact models in SPICE are based on either empirical models, physics oriented models, table-lookup models or macro models. Pure physical model is not existing for SPICE [2]. The physical models are based on device physics and its equations. Empirical models are based on the characteristics which are derived from experiments. physics oriented models are the combination of physical and empirical models. Table-lookup models are made from measurement database which includes dc, ac, temperature, geometry, and noise measured data and their derivatives. Lastly macro models are made of a SPICE subcircuit, which consists of any SPICE elements

[3]. In many cases the subcircuit topologies are not match with the target devices. Therefore, macro model is often called as either “Black Box Model” or “Function Model”. In this thesis physics oriented models and macro models are especially focused to develop new device and circuit models.

1.2.1 Recent Modeling Problems for Circuit Simulations

In past two decades several models and simulation algorithms have been developed and implemented into SPICE simulators. Most circuit designers use SPICE simulators in any way. However, many problems and requirements related to simulation models are still remained. Especially in this thesis the following issues are described:

1. Drain current, capacitance, and small signal low frequency noise models of amorphous silicon thin film transistors’ (a-Si TFT’s) and a liquid crystal capacitance model for dynamic characterizations

   Amorphous silicon based thin-film-transistors, which are kinds of field effect transistors, are widely used in active matrix type liquid crystal displays. The electrical characteristic is similar to large sized MOSFET’s in some conditions except an a-Si TFT does not have bulk terminal since it is made on glass material. However, some of the important characteristic are completely different from MOSFET’s.

2. A very large circuit simulation method using macro models for liquid crystal

display (LCD) panels

To simulate very large circuits such as LSI's and LCD's the simulator needs to handle extremely large number of transistors. It takes several hours or days if the circuit includes ten thousands or more of transistors. In some cases the simulation project hits the simulation limit of the simulator. For an LCD timing simulation a color XGA (1024 x 768) TFT-LCD includes at least 1024 x 768 x 3 transistors which hit the simulation limit of UCB SPICE 3. To solve the problem macro modeling technique has been adopted in order to decrease the total number of transistors to be used.

3. 1/f noise models and their measurement and extractions of metal-oxide-semiconductor field effect transistors (MOSFET's) for RF oscillator designs and a-Si TFT's for low frequency switches and sensors

   One of the most important low frequency noises existing in any FET's is the 1/f noise. Since the 1/f noise is frequency and bias dependent in the frequency range up to 10 MHz (MOSFET's), it is especially important for designing oscillators.

4. A small signal equivalent circuit model which includes parasitic and intrinsic components and direct extractions of bipolar junction transistors for radio frequencies (RF) and microwave circuit simulations

For RF and microwave circuit measurements and simulations how parasitics are handled is always the key issue. In this research a lumped sum parasitic circuit model is developed and then extracted using de-embedding and numerical techniques.

1.3 Survey of The Thesis

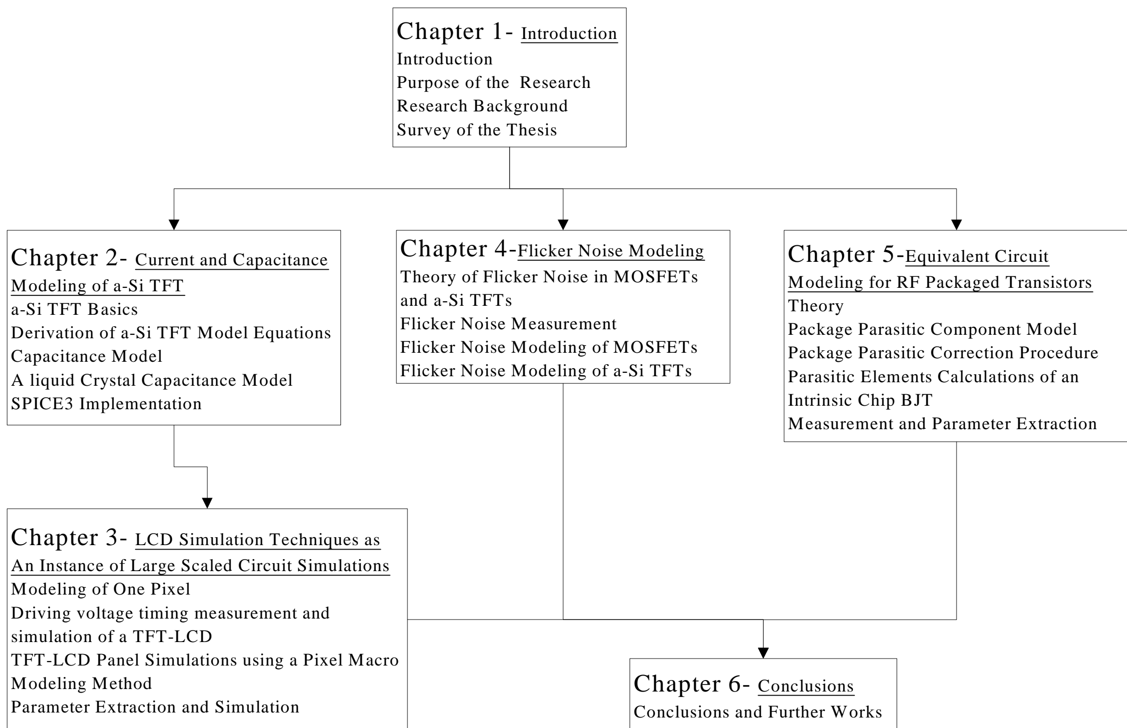


Fig. 1.2 Layout of the thesis

First of all, in chapter 2 dc current and capacitance model derivation for a-Si TFT's will be described by analyzing the device physics. To derive the model equations, the physics of an a-Si TFT will be carefully analyzed throughout the study of available papers that are related to a-Si TFT device physics and models, and comparison with MOSFET's which have similar device structures and electrical characteristics.

In the beginning electric charge calculation is started with Poisson equation. Then any terminal capacitance can be derived without any difficulty. For current equation derivation the continuous equation is used for drain current model. For developing the liquid crystal (LC) capacitance model empirical equation is directly derived by using the polynominal equation approximations. The a-Si TFT model that will be described in this thesis has been adopted by Avant!'s HSPICE as MOSFET model level 40 and Agilent Technologies' IC-CAP characterization and modeling software as HP ATFT model. Also the LC capacitance model was implemented in IC-CAP software.

In chapter 3 large scale circuit simulation methodology will be discussed by using a TFT-LCD panel as an instance. Usually for circuit simulations with SPICE the entire circuit topology was inserted. Which takes a long time to finish a very large circuit simulations such as LCD panel's since it includes large number of transistors. A new macro model has been developed based on TFT device scaling theory. The macro model makes it possible to reduce simulation speed without sacrificing the simulation accuracy.

In chapter 4 low frequency small signal noise measurement and modeling in MOSFET's and a-Si TFT's will be discussed. Especially the 1/f noise (flicker noise) modeling, which is equivalently as important as thermal noise, will be characterized. In the MOSFET's the model will be the bias, frequency, and geometry dependent which had not been published before in any other papers. On a-Si TFT's the 1/f noise characterization is not important for LCD

applications since TFT's are driven by large root mean square voltage waveform's. However on other applications such as sensors, low speed switches, and shift resistors 1/f noise characteristic is very important to simulate any pulse signals. Since none of 1/f noise modeling papers of a-Si TFT's were published so far, a new model and its characterization will be shown based on the MOSFET's.

In chapter 5 high frequency small signal modeling and de-embedding techniques of BJT's will be described. Mainly for RF and microwave (μW) circuit designers use packaged type devices, which have package and interconnect parasitic. The parasitic components should be omitted in order to characterize an intrinsic device. Another requirement is to obtain entire circuit components of the intrinsic BJT device directly from the measured data. In this thesis all parasitics and intrinsic components will be directly calculated from measured data without any optimization process.

This thesis concludes in chapter 6 where results and future research requirements will be reviewed. Throughout the entire discussion in this thesis, the most important ideas for developing compact models and parameter extractions are summarized in this chapter.

Chapter 2 Current and Capacitance Modeling of a-Si TFT

Introduction

Amorphous Silicon based Thin-Film-Transistors (a-Si TFT’s) are widely used for Active Matrix Liquid-Crystal Displays (AM-LCD’s). This has led to increasing demand for models that can predict TFT-LCD dynamic behavior with optical characteristics. Accurate a-Si TFT and Liquid Crystal Capacitance (LC cap) models are required for the characterization of TFT-LCD dynamic behavior. This paper presents the experimental results of our TFT-LCD transient analysis and the modeling method for the analysis.

Several papers have already been published regarding the physics [4] and the models [5], [6] of a-Si TFT’s. Those authors analyzed and solved the distribution of the localized states [4]-[6], which is divided into two exponential regions for the tail states and the deep states. Khakzar et al. [6] also included the temperature dependency of the current-voltage characteristics. Although those models [5], [6] are well analyzed, they are insufficient for today’s advanced LCD simulations, because they do not account for the following characteristics:

- The insulator film capacitance must be calculated from the dielectric constants of the two layer insulating film in order to keep the mobility consistent with the

process parameter [8], [9].

- Since the insulating film in some kinds of a-Si TFT's is made of two different materials, whereas MOSFETs' are one kind (S_iO_2), dielectric constant of the insulating film should be calculated independently.

- The off-leakage current, which affects the sub-threshold and off current region, must be incorporated in order to simulate the off-screen noise of LCD's.

  - Unlike MOSFET's applications, the off current is dominant for TFT-LCD simulations. Because liquid crystals are so sensitive of electron charge, even the femto-order current activate the liquid crystals.

- The threshold voltage of a-Si TFT's changes with voltage stress and device temperature [10] and must be taken into account.

  - The instability of threshold voltage is one of the major properties of a-Si TFT's. Although it is generally considered as the result of the insertion of electrons into the SiNx of gate insulated film, the physical explanation has not been presented in any conferences and papers. Therefore, the model should be empirical and flexible to represent the characteristics.

- The frequency-dependence of the gate-to-source and gate-to-drain capacitances must be taken into account in order to characterize LCD performance.

  - Because of the high resistivity material in a-Si TFT's, the intrinsic resistance of a-Si TFT to be taken account. The response time to the charge in potential is vary with the applied signals.

This paper presents an a-Si TFT model which focuses mainly on the inverted staggered type a-Si device structure. The model parameters were extracted from measured data using parameter extraction software developed with the model.

This paper also presents a liquid crystal capacitance model. The liquid crystal capacitance is critical in the simulation of LCD pixels and is voltage-dependent due to the crystal characteristic.

Sections 2.2, 2.3 and 2.4 describe the equation formulation of the a-Si TFT and Liquid Crystal Capacitance models. Especially for a-Si TFT analysis, the differences between MOSFET's and a-Si TFT's will be carefully shoveled in 2.2. Since the a-Si TFT and LC cap models are implemented into UCB SPICE 3e2 simulator, key procedures for the methodologies are introduced in section 2.5. Conclusions are summarized in Section 2.6.

2.1 a-Si TFT Basics

A key element in the current Flat Panel Display (FPD) Liquid Crystal Display (LCD) is the Thin Film Transistor (TFT) switch. A TFT can be thought of as a voltage-controlled switch that causes the crystal to block or pass the light. There are two types of TFT technologies that are pursued for LCD applications:

Amorphous silicon (a-Si) and

Polysilicon (p-Si)

Polysilicon TFT's offer performance advantages over a-Si. However p-Si TFT processing is done at higher temperatures, which necessitates use of quartz substrates. This makes p-Si TFT expensive and limits its use to high end applications at this stage. There is extensive research on p-Si silicon TFT panels with on-board peripheral circuits. a-Si TFT panels are already in production and are currently used as displays on portable PC's.

Substrate materials

The material of AM-LCD's should be transparent in order to pass through the back-light. Therefore, the substrate of a-Si TFT's must be made of quartz or glass. One exception is reflective type display whose substrate can be made of silicon because back light source is located on the surface of the display panel. Actually, MOSFET's are used for the reflection type display. a-Si

TFT technology offers better uniformity across the glass substrate and lower temperature processing, which results in reduced cost and better yield for large displays. Typical process temperature of a-Si TFT's is about 300 C because higher temperature will melt class substrate whereas p-Si TFT's is about 600 C.

a-Si TFT device structures

The array portion of an active matrix TFT LCD is similar than a DRAM array; that is, each display element is at the intersection of horizontal and vertical lines. The lines are called bus lines in the LCD terminology (similar to word and bit lines of standard memories). Most of the development effort for flat panel displays is devoted to amorphous silicon transistor switches. The technology for depositing thin film amorphous silicon with stable electrical properties has been known for some time, and is used commercially.

Two types of TFT structures are used for amorphous silicon (a-Si) devices. One is the inverted-staggered (IS) type, which can be either back channel etched (IS-BCE) or tri-layered (IS-TL). The other is called a normal-staggered (NS) device. These three transistors (IS-BCE, IS-TL, and NS) are shown in cross-section in Fig. 1.3. They are currently being used for LCD televisions.

The performance of a TFT as well as the manufacturing yield and throughput depend on the transistor's construction. The inverted staggered back

channel etched transistor, (IS-BCE), can be fabricated with the minimum number of six masks, whereas the inverted staggered tri-layered transistor, (IS-TL) requires nine. On the other hand, the IS-TL type has only a 500A° a-Si layer, minimizing the deposition time for this layer. This is important because amorphous silicon deposition is very slow, and can constitute a manufacturing bottleneck when thick layers are required.

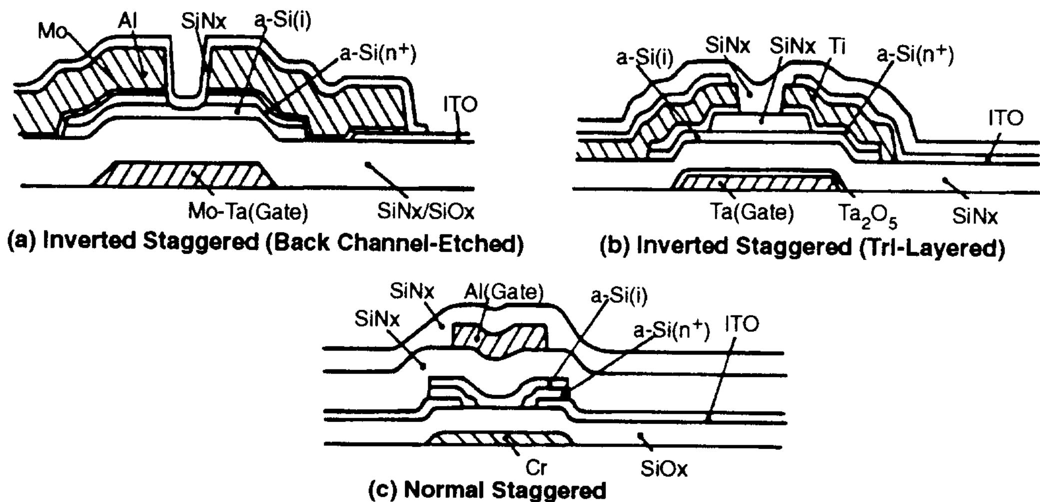


Fig. 1.3 a-Si Transistor Structures. (a) Inverted Staggered-Back Channel-Etched, (b) Inverted Staggered-Tri-Layered, (c) Normal Staggered a-Si TFT's.

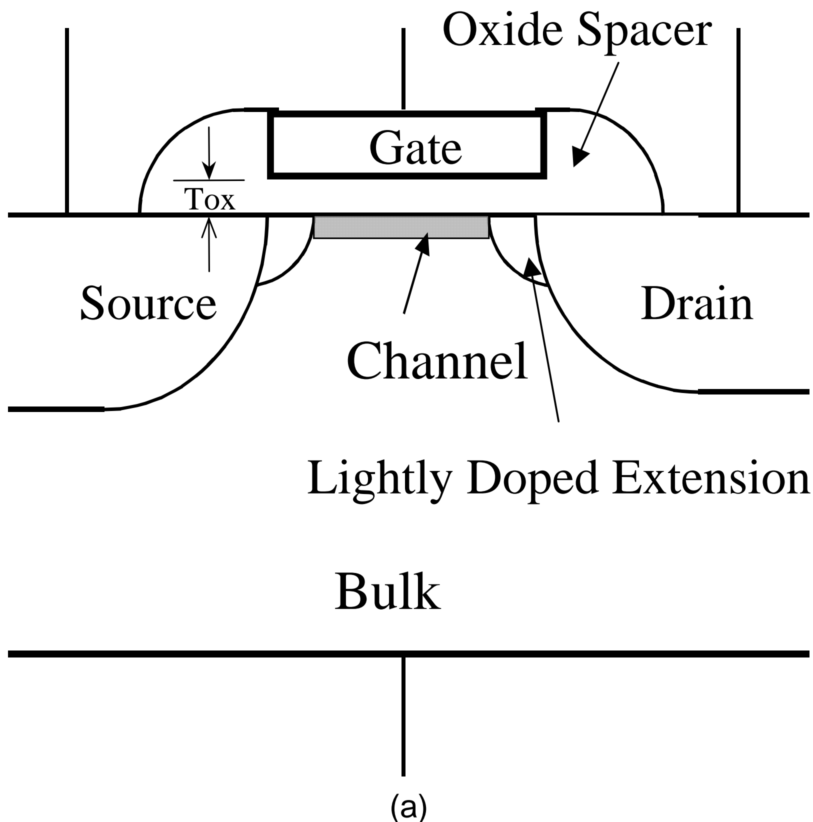
2.2 Derivation of a-Si TFT Model Equations

In order to maximize the speed and insure convergence of the large TFT-LCD pixel simulations, the some physical equations that include many exponents and gradients were modified by using mathematical transforms such as Taylor series and polynominal approximations. To make a new device model it is effective to start the development with an existing device model which has similar device structure and characteristics rather than formulating it from the scratch. We will, therefore, analyze MOSFET models since a-Si TFT's were developed based on MOSFET's device structure.

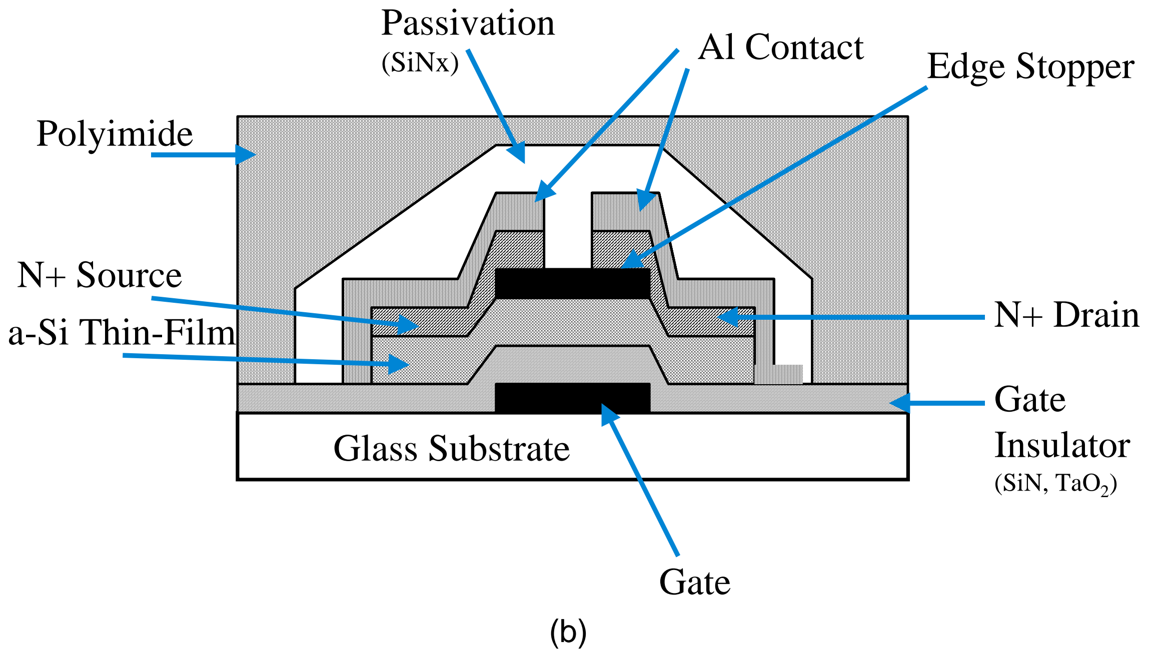
2.2.1 Analysis of a typical MOSFET model

Simplified device structures of MOSFET's and a-Si TFT's are shown in Fig. 2.1. The largest differences between them are position of the gates and the bulk materials., Since inverted stagger type a-Si TFT's are more popular than normal stagger ones as described in 2.1, the bottom gate structure has to be considered in a-Si TFT's. Since a-Si TFT's are fabricated on glasses whereas MOSFET's are fabricated on silicon, the process temperature of a-Si TFT's cannot be higher than MOSFET's. If the respective bias voltages are supplied at gate and drain terminals, majority carriers are attracted and form the channel on the surface of a MOSFET. As the result only the partial area around the source, drain, and channel will be depleted. On the other

hand for an a-Si TFT the channel is formed below the source and drain. Then entire semiconductor region of thin a-Si will be depleted. In this case the accumulation charge of a-Si TFT will be much lower than MOSFET's. Another differences between them is on the energy band diagrams. For MOSFET's most carriers are located in either conduction or valence bands. Intermediate levels are quite a little as a whole. On the contrary for a-Si TFT's the intermediate levels are a lot more than MOSFET's. They are so called localized states, that can be separated into tail and deep states. The localized charge affects a-Si TFT's electric characteristics drastically.



(a)



(b)

Fig. 2.1 Simplified device structures of (a) MOSFET and (b) a-Si TFT.

In addition to the above differences between MOSFET's and a-Si TFT's there are some other issues to be addressed. They will be discussed by inspecting a typical MOSFET model, UCB MOSFET level 3 [14]. The UCB MOSFET level 3 model has been used for modeling down to 1.2μm processed MOSFET devices for more than one decade. The model is based on a combination of physical and empirical equation formulations. It has, therefore, flexibility and good conversion performances. Since the gate channel length of a-Si TFT's is more than 1μm (Gate length, Gate width > 1.0μm), the level 3 model will be a reference for developing the a-Si TFT model. Model parameters of the level 3 model were extracted and optimized by using a

commercial characterization and modeling software, Agilent Technologies' IC-CAP [15].

In order to find the differences between MOSFET and a-Si TFT characteristic some sets of dc current versus voltage measurements of a typical a-Si TFT have been performed. Those data will be used also for evaluating the a-Si TFT model which is described later in 2.2.3. The extraction procedure for level 3 model parameters is drawn in Fig. 2.2. Also, the extracted model parameters are listed in Table 2.1.

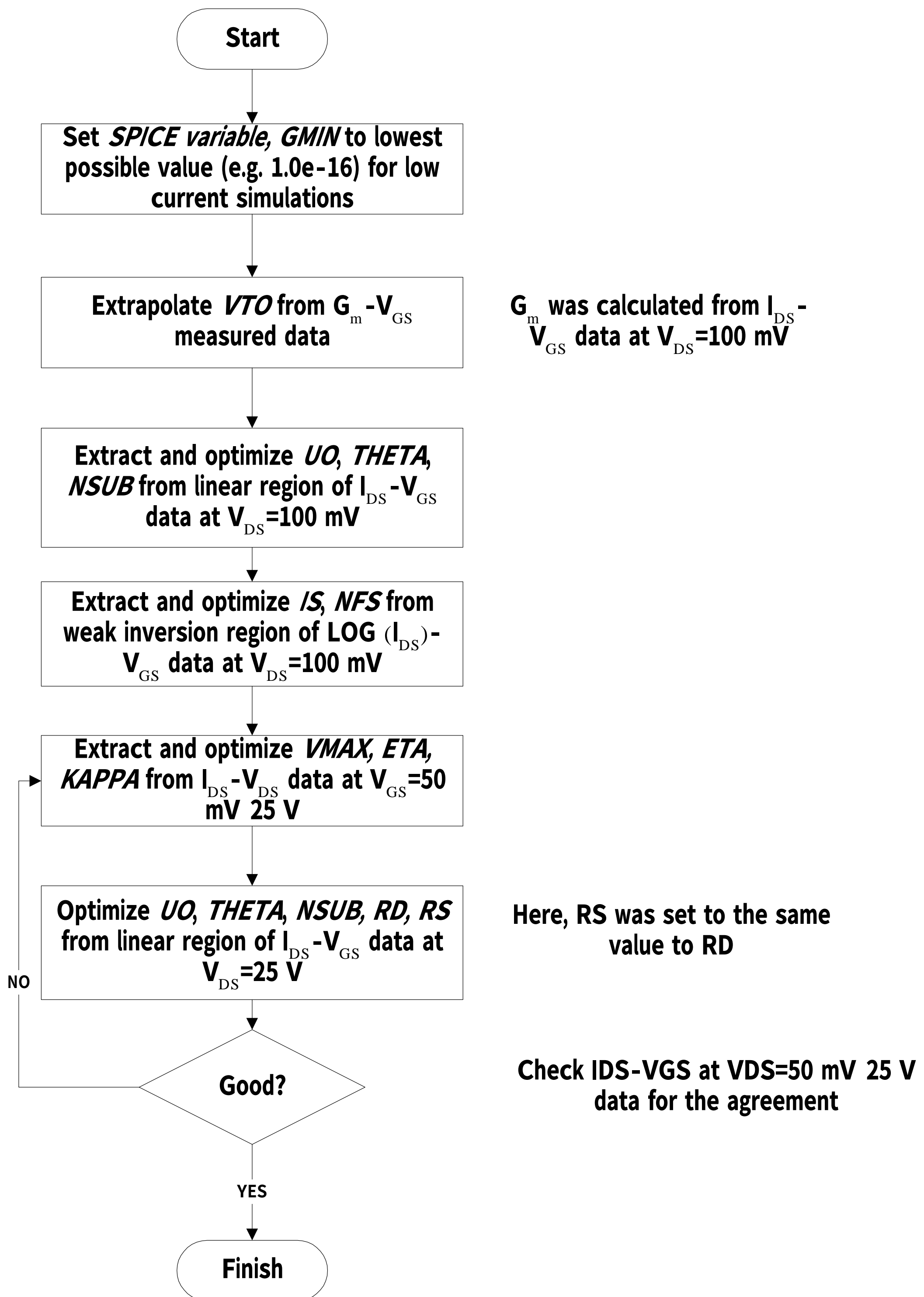


Fig. 2.2 The level 3 model parameter extraction flow using a-Si TFT.

Table 2.1 Extracted UCB MOSFET level3 parameters for an a-Si TFT.

Parameter name	Comment	Extracted value
LEVEL	UCB MOSFET model level	3
UO	Mobility	0.4598
VTO	Threshold voltage at VD=0 [V]	5.194
NFS	Surface fast state density	1.529E+12
TOX	Oxide thickness	3E-07
NSUB	Substrate doping density	1.571E+12
VMAX	Velocity saturation voltage	1E+07
RS	Source resistance	1.418E+05
RD	Drain resistance	1.418E+05
IS	Diode saturation current	1E-17
THETA	Mobility modulation	-0.01186
ETA	Static feedback on threshold voltage	2.002
KAPPA	Saturation field factor	0.001619
CGDO	Gate-drain overlap capacitance per meter	5E-06
CGSO	Gate-source overlap capacitance per meter	5E-06

In Fig. 2.3 the I_{DS} versus V_{DS} curve from strong inversion to saturation regions shows fair agreement especially at high gate voltages. However, the simulation shows clear pinch-off points whereas the measurement does not show them clearly. Saturation region drain current (measured data) of the a-Si TFT doesn't reach velocity saturation region whereas the level 3 model automatically shows. The reason is as follows:

Carriers of an n-channel MOSFET quickly reaches velocity saturation point at high electric field because most carriers are concentrated on either conduction or valence bands. On the other hand, for an a-Si TFT carriers are existing also in localized state between conduction and valence bands. Those carriers in localized state are gradually moving into the next energy level when voltages are applied. Therefore, carriers of an n-channel a-Si TFT slowly reaches velocity saturation point. The level 3 model cannot simulate this effect.

This problem can be solved without any difficulty by using P channel MOS-FET model of BSIM3 (Berkeley Short Channel I-G FET Model version 3) because the P channel model includes such parameters to change the sharpness of the pinch off point. However, the model includes huge number of model parameters that are mainly for fitting geometry dependence. a-Si TFT's are large channel and no geometry variations are needed for its applications.

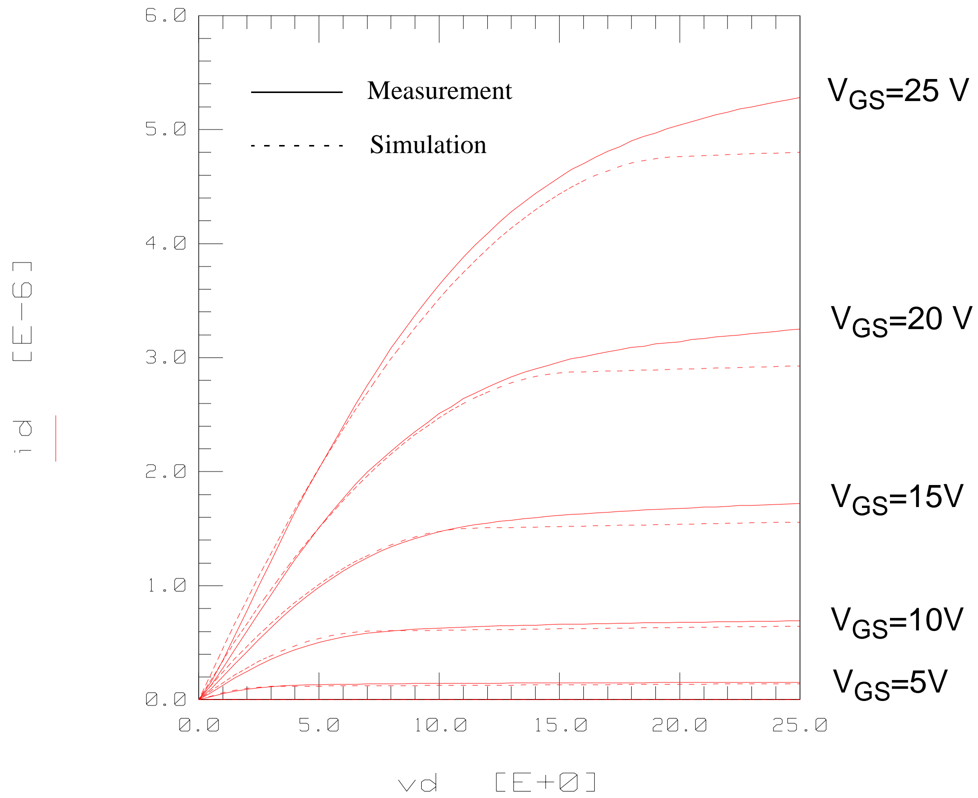


Fig. 2.3 I_D-V_{DS} measurement of an a-Si TFT and simulation of UCB MOSFET level 3 model.

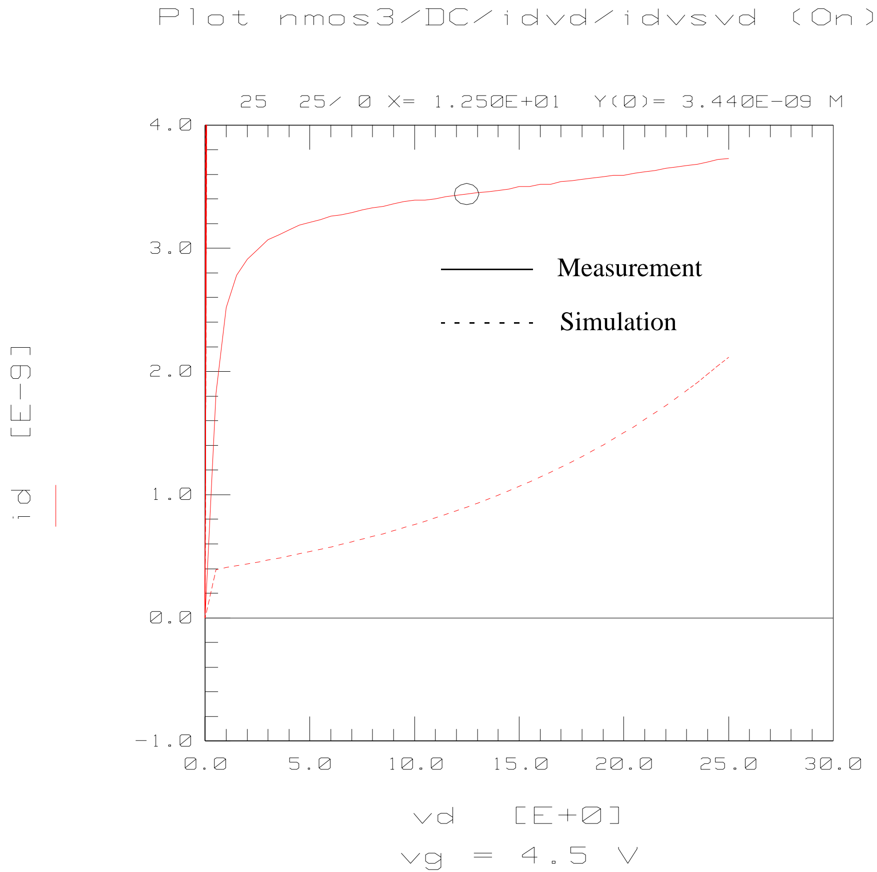


Fig. 2.4 I_D-V_{DS} measurement of an a-Si TFT and simulation of UCB MOSFET level 3 model. Here, V_{GS}=4.5 V.

Fig. 2.5 shows the good agreement between measured and simulated data since the model parameters, *UO, NSUB, THETA, and VTO* are lastly optimized with this measurement.

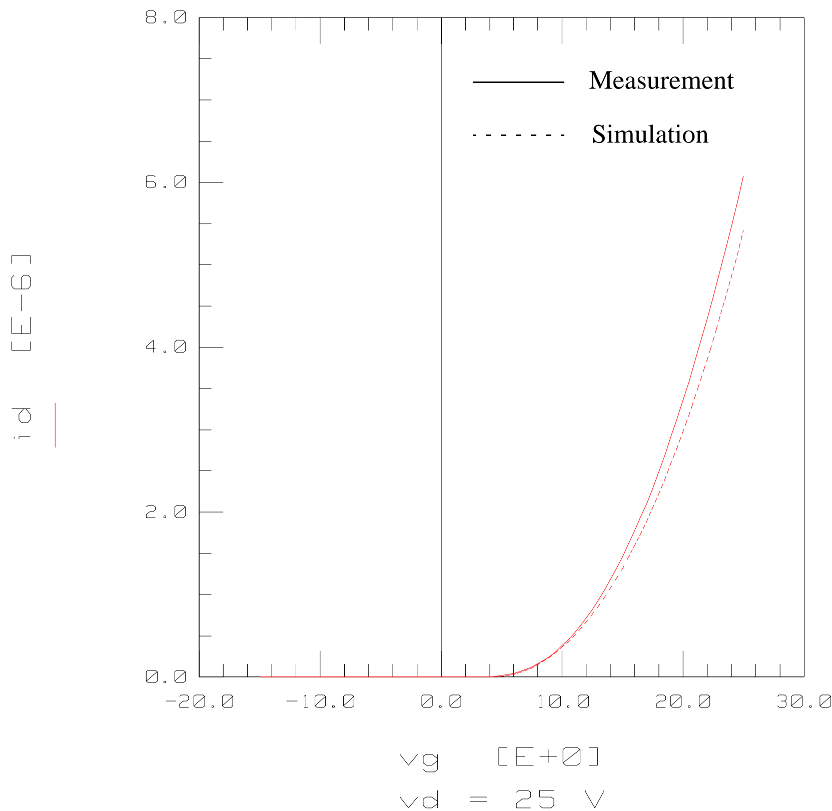


Fig. 2.5 I_D-V_{GS} measurement of an a-Si TFT and simulation of UCB MOSFET level 3 model. Here, V_{DS}=25 V.

In Fig. 2.6 the vertical scale of Fig. 2.5 was changed to logarithms. The sub-threshold to off-current region characteristic of the a-Si TFT is different from the simulated results by level 3 model. Sub-threshold behavior is comprised of a leakage current that arises from optical and channel current flowing from gate to source as well as from gate to drain.

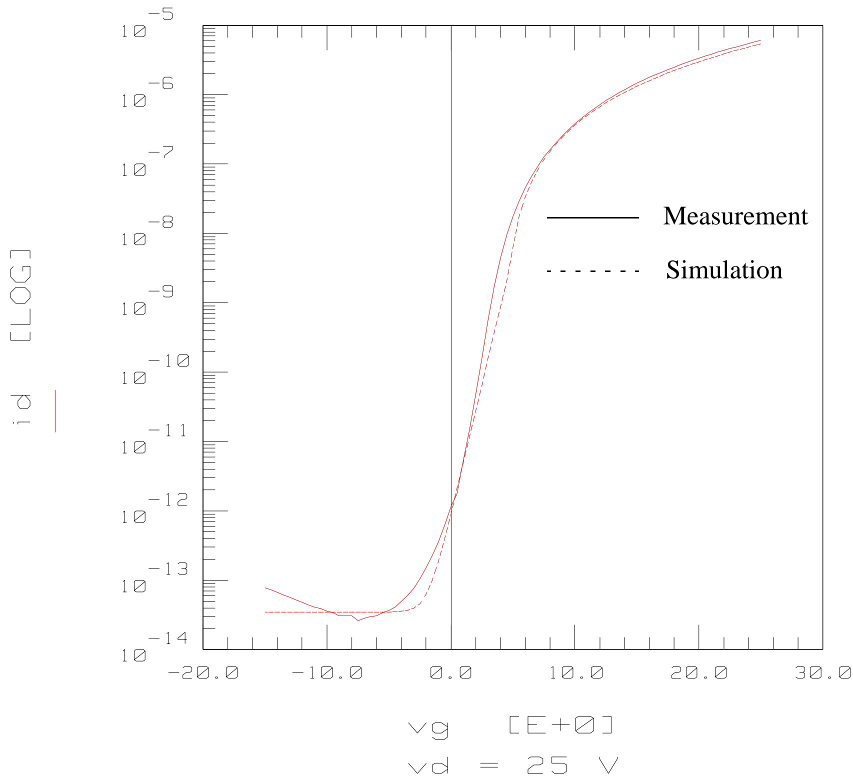


Fig. 2.6 *Log I_D-V_{GS}* measurement of an a-Si TFT and simulation of UCB MOSFET level 3 model. Here, V_{DS}=25 V.

Even though the parameter extraction of linear region was lastly tuned by using Fig. 2.5, Fig. 2.7 should show fair agreement if the model could represent the a-Si TFT characteristic. However, the result show poor agreement between measured and simulated data especially at threshold voltage.

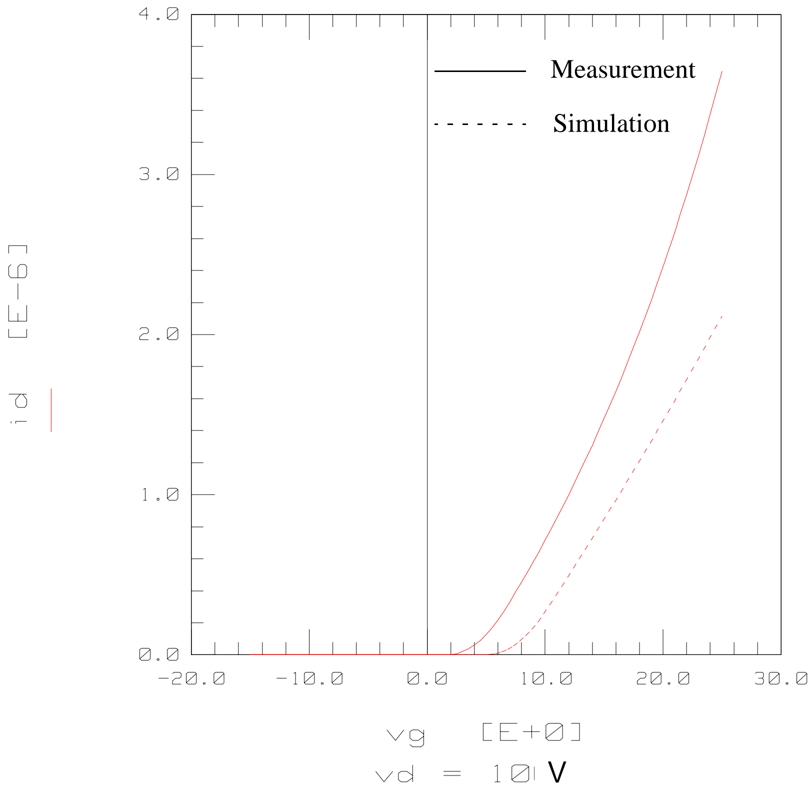


Fig. 2.7 I_D-V_{GS} measurement of an a-Si TFT and simulation of UCB MOSFET level 3 model. Here, V_{DS} = 10 V.

The logarithmic plot of Fig. 2.7 is shown in Fig. 2.8. In Fig. 2.8 the measured off-current is minus whereas the simulation could not represent.

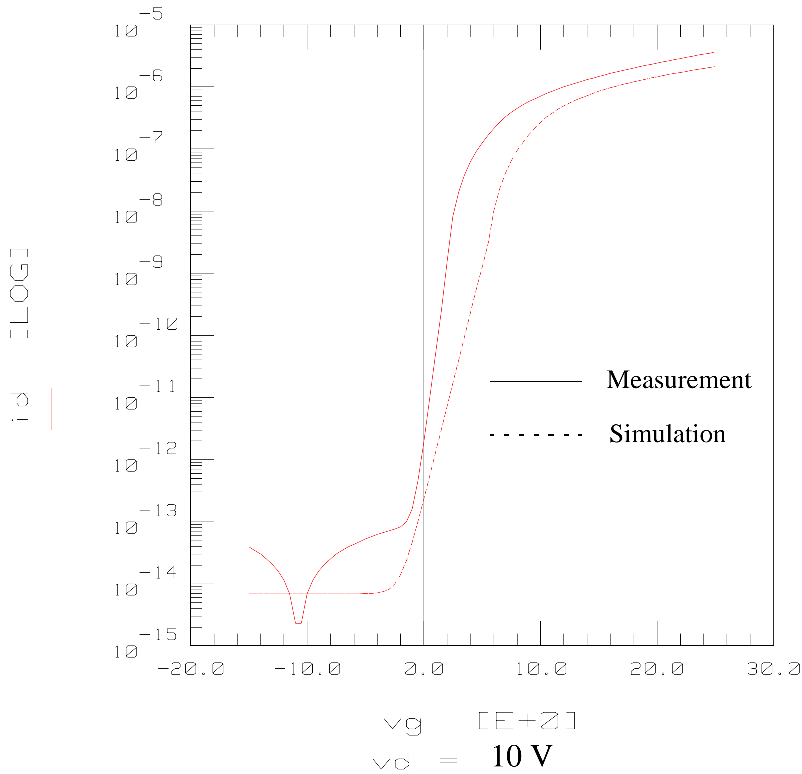


Fig. 2.8 ***Log*** $\boldsymbol{I_D}$**-**$\boldsymbol{V_{GS}}$ **measurement of an a-Si TFT and simulation of UCB MOSFET level 3 model. Here,** $\boldsymbol{V_{DS}}$ **= 10 V.**

The logarithmic I_{DS}-V_{GS} plot with multi drain biases is shown in Fig. 2.9.

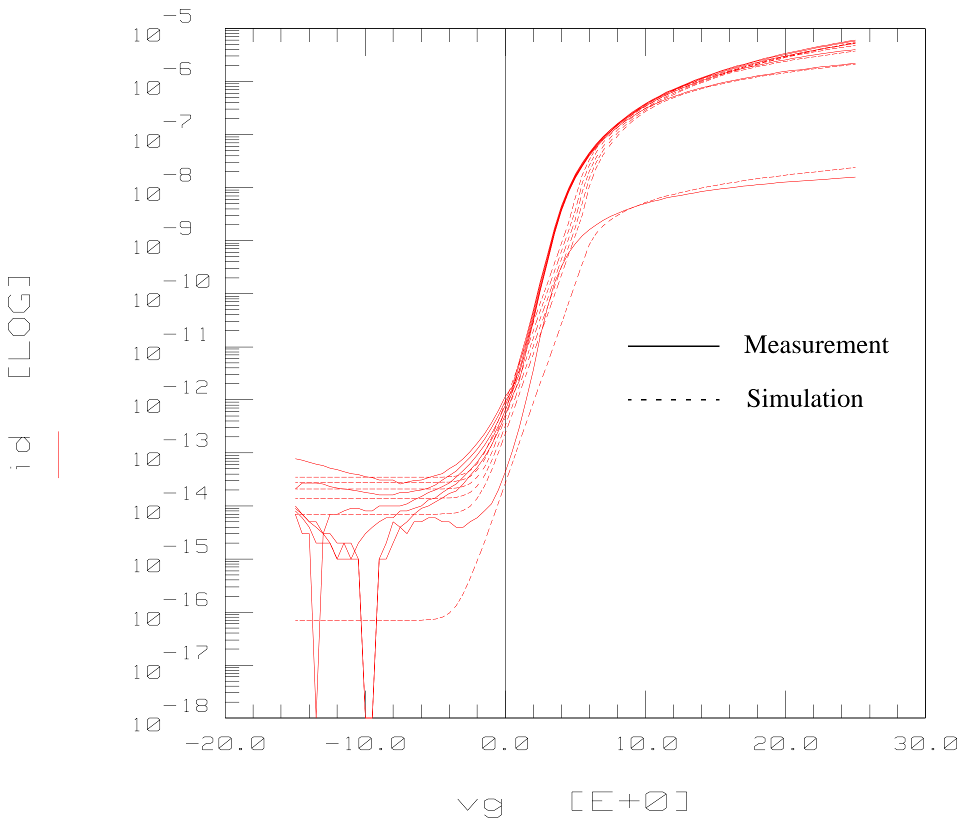


Fig. 2.9 *Log* I_D-V_{GS} measurement of an a-Si TFT and simulation of UCB MOSFET level 3 model. Here, V_{DS}=50 mV ~ 25 V.

As described above, problems for current-voltage characterization of a-Si TFT's with UCB MOSFET level 3 model were studied. On capacitance modeling it is clear that any MOSFET models cannot characterize a-Si TFT's

because the total gate charge is not comparable with MOSFET's. Those differences are mainly caused by the localized states of a-Si TFT's.

Although some a-Si TFT models were already introduced in [5], [6], and [7], they were not enough to simulate advanced a-Si TFT devices for LCD panels. In order to simulate recent a-Si TFT's accurately, the a-Si TFT model focuses primarily on the following a-Si TFT characteristics as discussed in [10]:

- Because of localized states, TFT's require a higher gate turn-on voltage than MOSFET's.

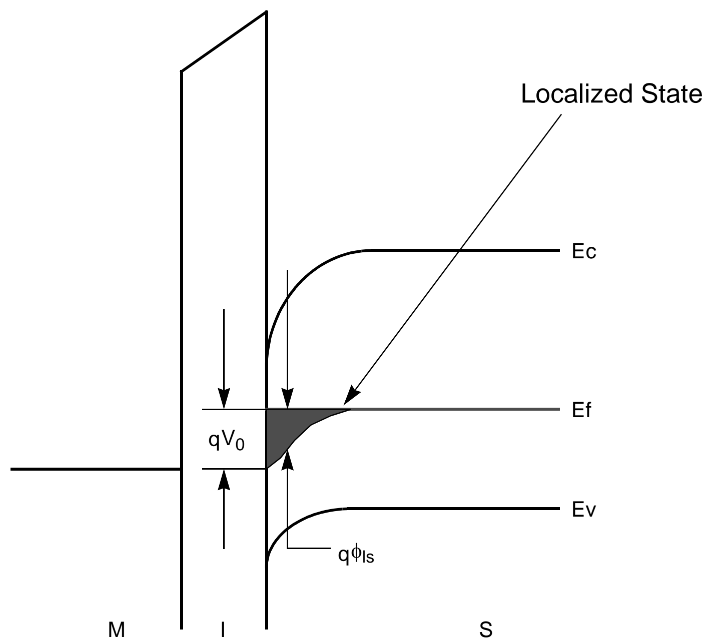


Fig. 2.10 a-Si TFT Energy Band Diagram.

- As shown in Fig. 2.10, localized state is existing below the Fermi-level. In order to turn on an a-Si TFT, energy bands should be bended by charging and discharging the localized state. The more localized states, higher gate voltage is needed to apply. Hence, the threshold voltage of an a-Si TFT is higher than MOSFET's.

- Due to photoconductivity and channel leakage current flowing from gate-to-source and drain-to-source, the sub-threshold behavior is different from MOSFET's.

  - The channel leakage current is based on Gate-Induced-Drain-Leakage (GIDL) current which will be discussed in 2.2.3. In addition optical current is generated since the substrate material is made of glass. In LCD applications back lighting increase the leakage.

- The threshold voltage varies with the temperature and duration of the voltage applied to the gate (voltage stress), which is known as threshold voltage instability.

- Some TFT's have the insulator film that consists of two layers of different materials.

- The gate-to-source and gate-to-drain capacitances are bias- and frequency-dependent.

  - The bias dependency of the capacitance can be formulated by solving charge conservation theory from the a-Si TFT's gate charge. However, the frequency dependency is not included in any MOSFET models.

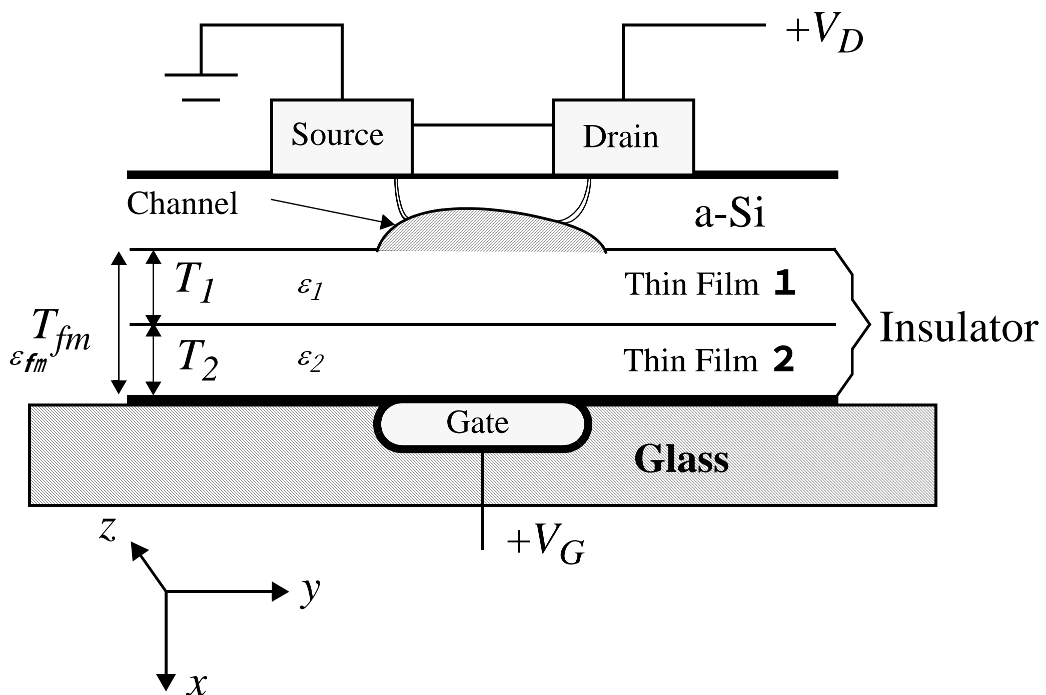


Fig. 2.11 A simplified inverted-stagger type a-Si TFT structure. Here T_{fm} is the insulator film thickness (T_1+T_2) and ε_{fm} is the dielectric constant of the insulated film. Also, T_1, T_2, ε_1, and ε_2 are the film thickness and dielectric constants of Film1 and Film2, respectively.

2.2.2 Localized Charge Distribution of an a-Si TFT

In single crystalline silicon devices such as MOSFET's all charges that are induced by the channel appear in the conduction band when the applied voltage at the gate is higher than the threshold voltage. In a-Si devices the charge mechanism is modified by the localized state charge. Because of the existing of localized state charges, higher electric field than MOSFET's in the insulated film is required to move localized state charges into the conduction band [11]. This behavior has to be analyzed in order to model an a-Si TFT.

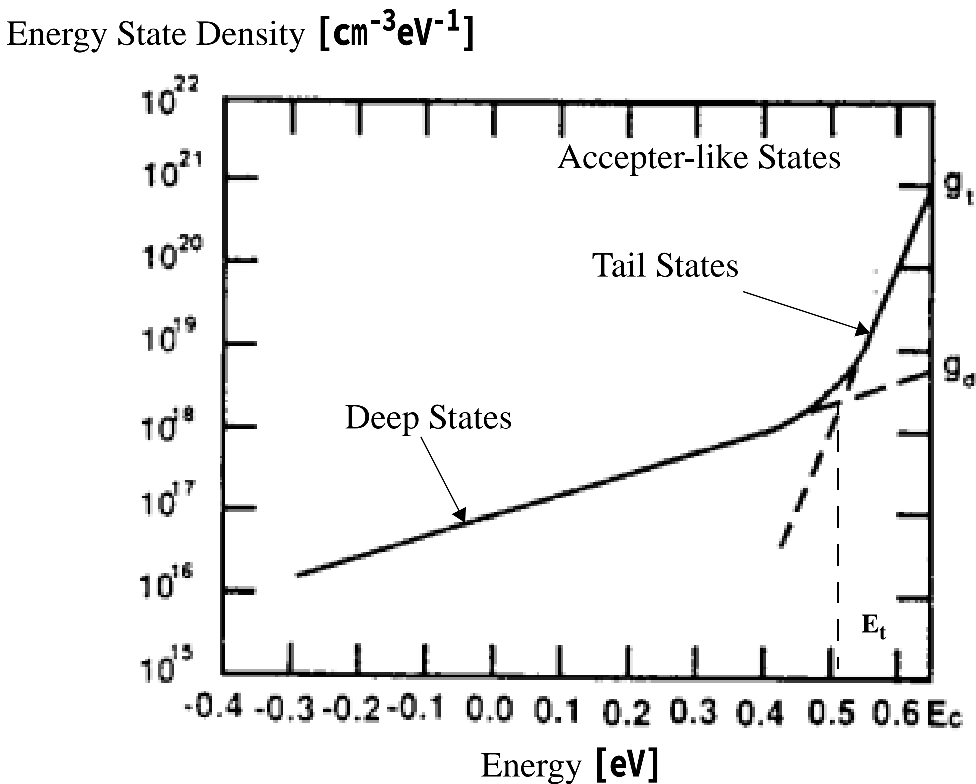


Fig. 2.12 Distribution of Acceptor-like States in the Energy Bandgap of a-Si.

The current-voltage and capacitance-voltage characteristics of a-Si TFT's strongly depend on the density and distribution of localized states in the energy gap. The position of the carrier Fermi level in an a-Si channel may vary from levels close to the bottom of the conduction band to energies near the top of the valence band depending on the sign and magnitude of the gate voltage [4]. Fig. 2.12 is the energy state density distribution diagram of a-Si. Here E_c is the bottom energy in conduction band, E_t is the bottom energy in tail states, g_d is the energy density in *deep* states, and g_t is the energy density in *tail* states. The density of this charge is determined by the density of the localized *tail* states and by the position of the carrier Fermi level. The total density N_{loc} of the localized charge [4] is approximated by

$$N_{loc} = N_{deep} + N_{tail} . \quad (2.1)$$

Here, N_{loc} is the concentration of electrons in localized states, N_{deep} is the concentration of electrons in deep states and N_{tail} is the concentration of electrons in tail states. The localized states charge per unit area, Q_{loc} [4], [5] is calculated by

$$Q_{loc} = qN_{loc} = \int_{E_{F0}}^{E_c} \frac{g_a(E)}{1 + exp\left(\frac{E - E_F}{kT}\right)} dE . \quad (2.2)$$

Here q is the electron charge, g_a is the existing acceptor states density, E is the energy, E_{F0} is the bulk Fermi level, E_F is the electron Fermi states. In

general occupancy ratio of localized states is dominated by trap Quasi-Fermi level. Also the trap Quasi-Fermi level are very close to carrier Fermi level.

$$Q_{loc} = q\int_{0}^{\infty} N_{loc}dx = \sqrt{2\varepsilon q \int_{0}^{V0} [N_{deep}(V) + N_{tail}(V)]dV} \quad (2.3)$$

where x is the vertical distance of the TFT device structure, V_0 is the surface band bending, and ε is the dielectric permittivity of amorphous silicon. A simplified structure of the inverted-stagger type a-Si TFT's is shown in Fig. 2.11. When V_G and V_D are supplied at each terminal respectively, the conducting channel is produced in the a-Si layer.

The resulting electron concentration causes an accumulation area to expand under the source and drain. The total channel charge is very small and is negligible compared to the surface states charge and localized states charge. The dominant charge in the semiconductor channel are mobile and localized charges. The drain current derivation of a-Si TFT is started with linear region.

2.2.3 Current-Voltage Characteristics

Because of the long channel device condition, dV/dx is much greater than dV/dy,

$$\frac{dV}{dx} \gg \frac{dV}{dy} \quad (2.4)$$

Here, directions of x, y, and z are illustrated in Fig. 2.11. The gate charge (Q_g) equals the negative sum of mobile charge (Q_m), surface state charge (Q_{ss}), and localized charge (Q_{loc})

$$Q_g = -Q_m - Q_{ss} - Q_{loc} = C_{fm}(V_g - V_s - \phi) \quad (2.5)$$

Here, C_{fm} is the insulated film capacitance per unit area, V_g is the gate potential, and V_s is the source potential. Current density, J_n is given by (2.6)

$$J_n = -q(\mu_n n + \mu_p p) \cdot \frac{d\phi}{dy} \quad (2.6)$$

where ϕ is the potential, n is the number of electrons, p is the number of holes, and μ_n and μ_p are the effective mobilities of the electrons and holes, respectively.

The total current of the drain-to-source is solved by

$$I_{DS} = \iint J_n \cdot dxdz = -Z \cdot \frac{d\phi}{dy} \cdot \mu_{eff} \cdot Q_m \quad (2.7)$$

$$I_{DS} \int_0^L dy = -W \int_0^{V_D} \left(\mu_{eff} \cdot Q_m\right) \, d\phi \quad (2.8)$$

Here, Z is replaced with W (channel width) in (2.7), μ_{eff} is the field effect mobility and L is the channel length. Substituting (2.5) into (2.8) and integrating with respect to V from 0 to V_D, we obtain

$$I_{DS} = \frac{W}{L} \cdot \mu_{eff} \left\{ C_{in} \left[\left(V_{GS} - V_{TO} \right) V_{DS} - \frac{V_{DS}^{2}}{2} \right] + Q_{loc} \cdot V_{DS} \right\} \tag{2.9}$$

where V_{TO} is a threshold voltage without localized states charge, which is extracted from the measured I_D versus V_G curve at low V_D (e.g. 50 mV). The field effect mobility (μ_{eff}) is a function of gate bias and is given by

$$\mu_{eff} = \frac{\mu_0}{1.0 - \theta \cdot (V_{GS} - V_{TH})} \tag{2.10}$$

where μ_o is the band mobility and θ is the mobility reduction. Because the expansion of Q_{loc} (2.3) includes a large number of logarithms and exponents, an approximation is used to decrease computation time.

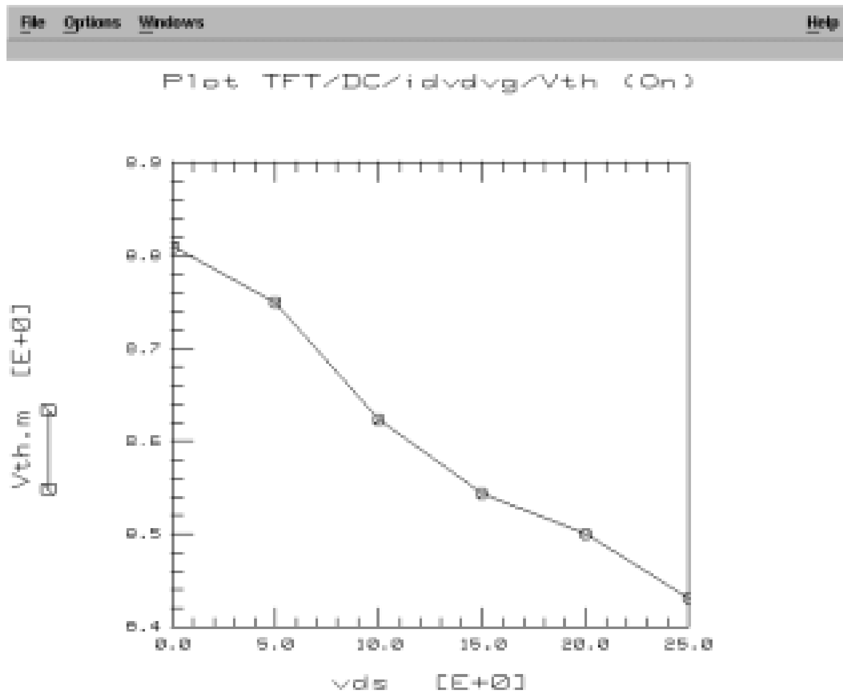


Fig. 2.13 Drain voltage dependency of threshold voltage.

For the surface band bending in Fig. 2.14, it is necessary to charge and discharge any localized states around the Fermi level. Larger numbers of localized states make it more difficult to bend the energy band and the threshold voltage increases.

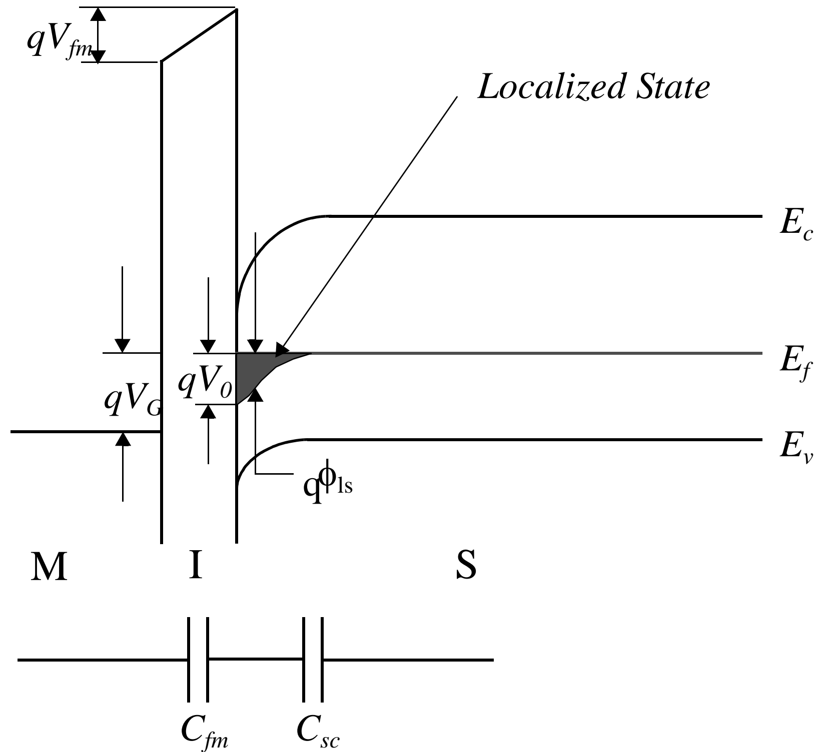


Fig. 2.14 Energy band diagram of a-Si TFT and its equivalent circuit.

Using the threshold voltage measurement as shown in Fig. 2.13, it can be shown that the threshold voltage decreases in proportion to drain voltage as

$$V_{TH} = V_{TO} - \eta \cdot V_{DS} \tag{2.11}$$

where η is a fitting parameter to express static feedback effect. In our threshold analysis, we found that the localized charge could be included in the threshold voltage as

$$Q_{loc} = C_{fm} \cdot V_{DS} \cdot \eta \ . \tag{2.12}$$

The final drain current equation for the linear region is

$$I_{DS} = \frac{W}{L} \cdot \mu_{eff} \cdot C_{fm}\left[(V_{GS} - V_{TO} + \eta \cdot V_{DS}) \cdot V_{DS} - \frac{V_{DS}^2}{2.0}\right] \quad (2.13)$$

As shown in Fig. 2.11, a typical a-Si insulated thin film consists of two layers of different types of materials [9], T_1 and T_2. The capacitance and the electrical constants are calculated in a traditional manner as shown in

$$C_{fm} = \frac{\varepsilon_0 \cdot \varepsilon_1 \cdot \varepsilon_2}{T_2 \cdot \varepsilon_1 + T_1 \cdot \varepsilon_2} \quad (2.14)$$

$$\varepsilon_{fm} = C_{fm} \cdot T_{fm} \quad (2.15)$$

where ε_o is the permittivity of a vacuum.

Due to traps, carriers reach maximum velocity slowly in the region beyond pinch off. The electrons are not traveling at a saturation velocity in an amorphous silicon TFT. The saturated velocity (v_{sat}) was defined to represent the drain saturation voltage. The derivation of the drain current equation is similar to the UCB MOS level 3 model [14]. The drain current for the saturation region becomes

$$I^{sat}{}_{DS} = I_{DS} \cdot \frac{\nu_{sat} \cdot L}{(1.0 + V_{DS}) \cdot \mu_{eff}} . \quad (2.16)$$

In the sub-threshold region, when the Fermi level at the interface exists in the energy range corresponding to the *deep* states, the drain current rises exponentially with gate voltage. Unlike MOSFET devices, the sub-threshold

current characteristic is affected by the amount of interfacial traps and the bulk states throughout the a-Si film. The more interfacial traps, the more gentle the slope of the sub-threshold current curve. This leads to discontinuity in the transition region from sub-threshold to linear. In order to avoid this phenomenon, another threshold voltage, v_{on}, is defined. The sub-threshold equation is given in (2.17).

$$I^{subth}{}_{DS} = I_{DS} \cdot \exp\left(\frac{V_{GS} - V^{eff}{}_{TH}}{xn \cdot vt} + 1.0\right), \tag{2.17}$$

$$v_{on} = V^{eff}{}_{TH} + \eta \cdot V_{DS} + \left(1.0 + \frac{q \cdot N_{FS} \cdot L \cdot W}{C_{fm}}\right) \cdot v_t, \tag{2.18}$$

where

$$v_t = \frac{k \cdot T_{nom}}{q}, \tag{2.19}$$

here, k is the Boltzmann constant, T_{nom} is the temperature, and N_{FS} is the effective fast surface state density which is affected by the bulk states and the deep states.

The leakage current in off-current region is important because it affects both of weak inversion and off current regions. Though the physical mechanism has not been solved, it is considered that the leakage current is raised by optics which are from glass substrate and GIDL (Gate Induced Leakage Current).

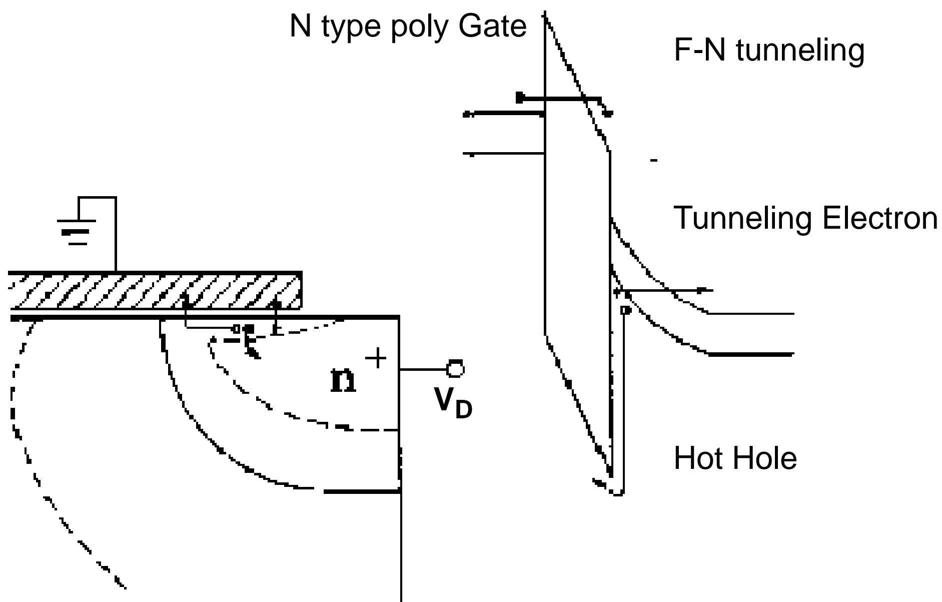


Fig. 2.15 GIDL generation mechanism.

Fig. 2.15 shows a top gate MOSFET type structure as an example to understand GIDL mechanism. A deep depletion region is formed in the gate-to-drain overlap region. The energy band diagram illustrates the band-to-band tunneling process and the flow of carriers. Valence band electrons tunnel into the conduction band and are collected at the drain. The holes created flow to the substrate.

It can be written as

$$I_{GIDL} = W \cdot A_{GIDL}(V_{DS} - V_{GS} - B_{GIDL}) \cdot e^{\frac{-C_{GIDL}}{V_{DS} - V_{GS} - B_{GIDL}}\left(1 - e^{-\frac{V_{DS}}{V_t}}\right)} . \quad (2.20)$$

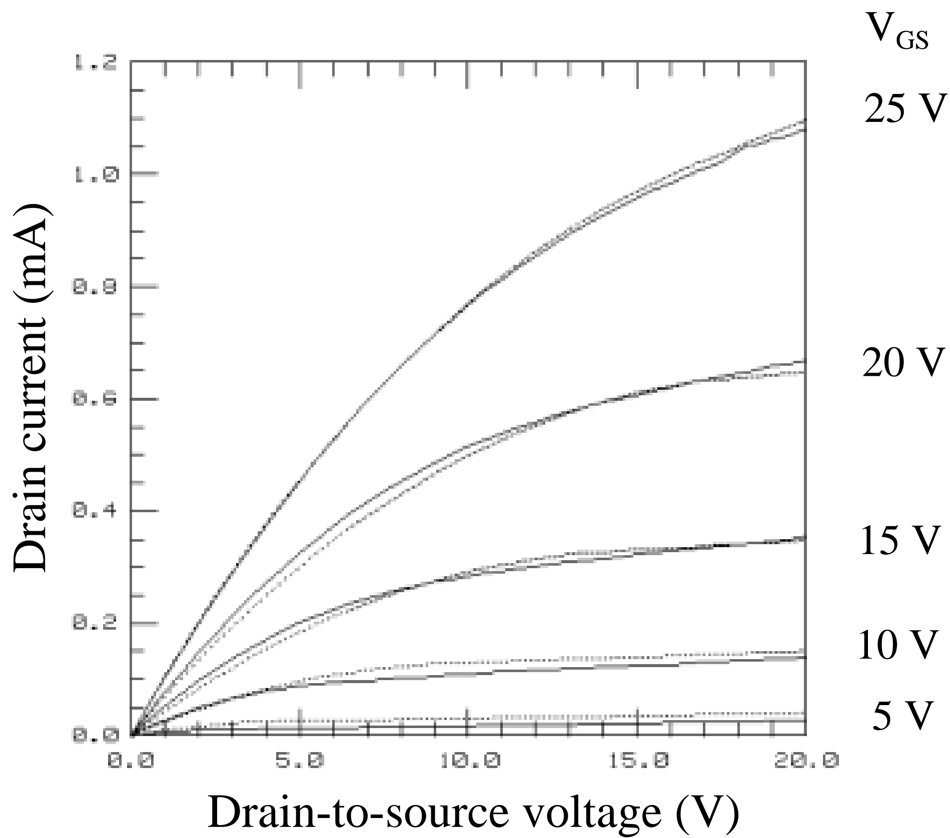
Here A_{GIDL}, B_{GIDL}, and C_{GIDL} are unknown variables and are all fitting parameters to be extracted.

In a-Si TFT's channel leakage currents are low (order of fA to pA) enough to modify the exponential component to a linear function using a conductance parameter. The drain leakage current is increased in proportional to the gate and drain voltages as

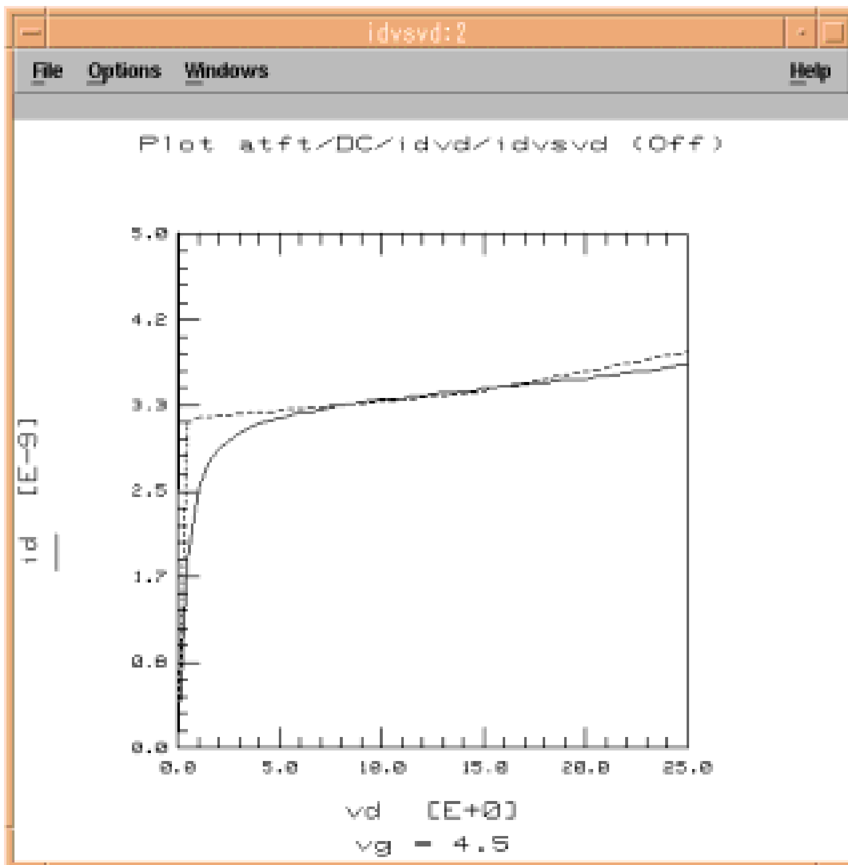
$$I_{DS}^{off} = I_{DS}^{subth} + g_o \cdot \left(V_{GS} + D_{eff} \cdot V_{DS}\right) . \quad (2.21)$$

Here g_o is the optical and GIDL conductance and D_{eff} is the coefficient of GIDL which is dependent of each TFT process.

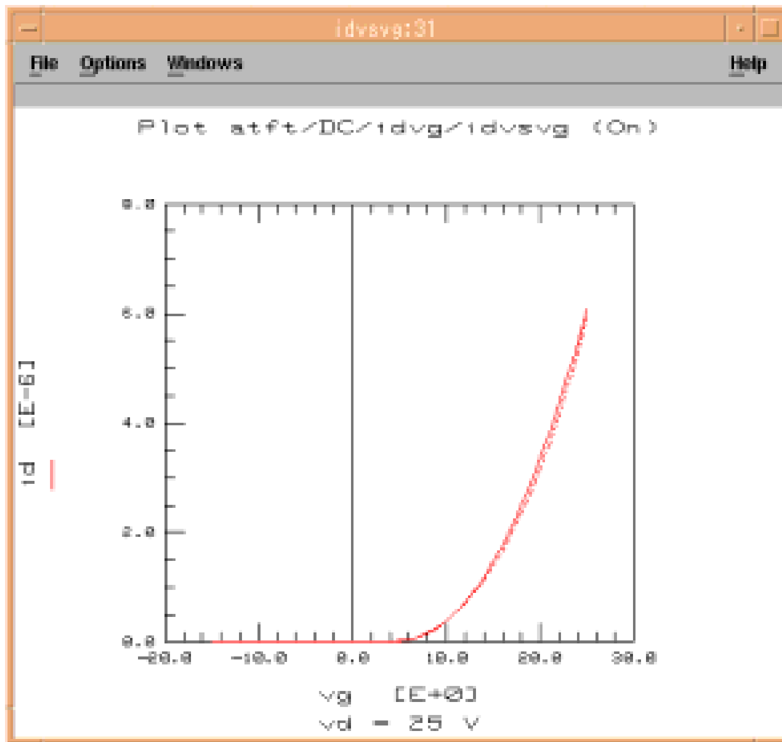
Using the drain current model and extracted its model parameters with measured data, that is used for testing UCB MOSFET level 3 model in section 2.2.1, the a-Si TFT model is verified by comparing measured and simulated data which is shown in Fig. 2.16.



(a)



(b)



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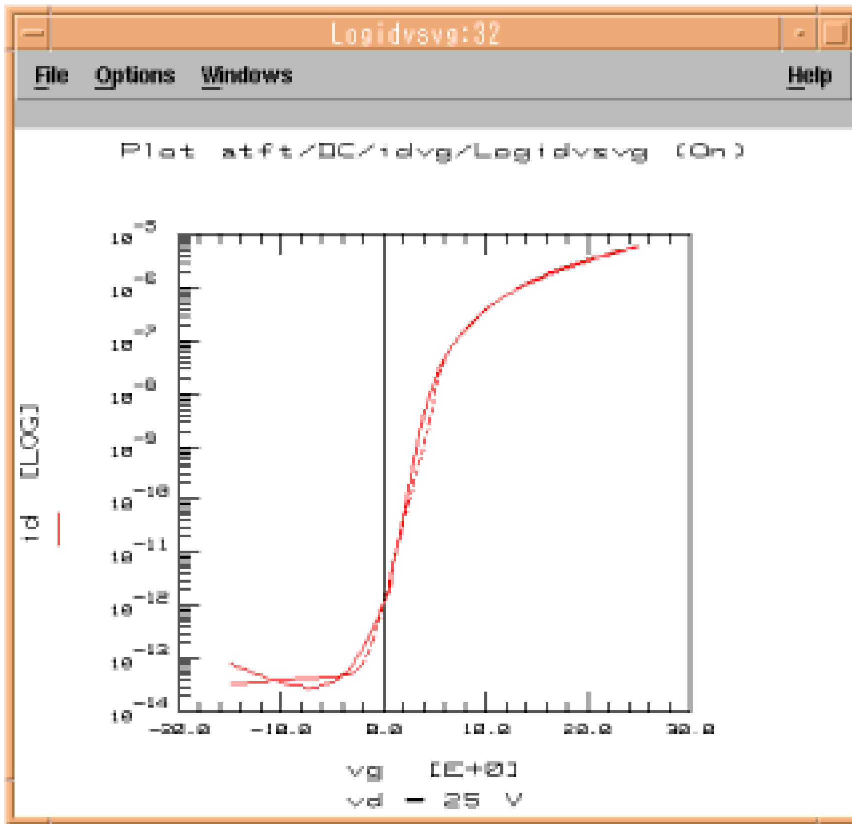
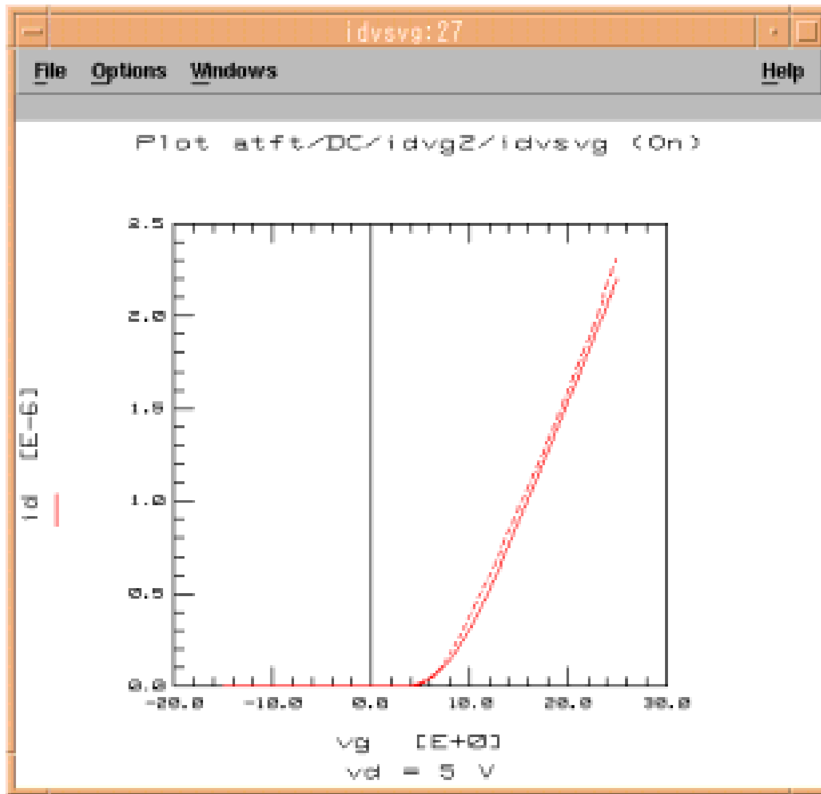
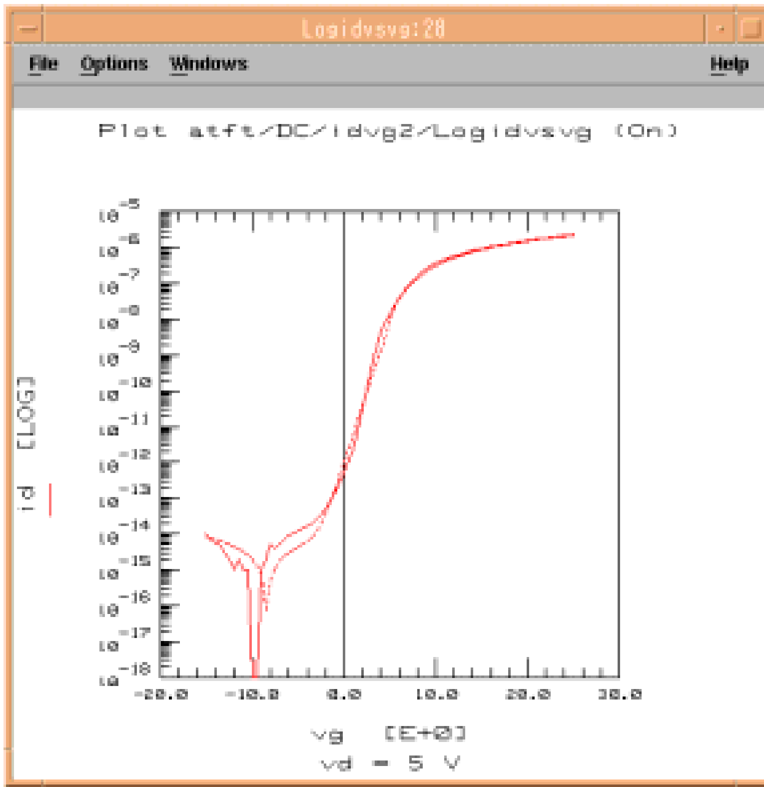


(d)



(e)



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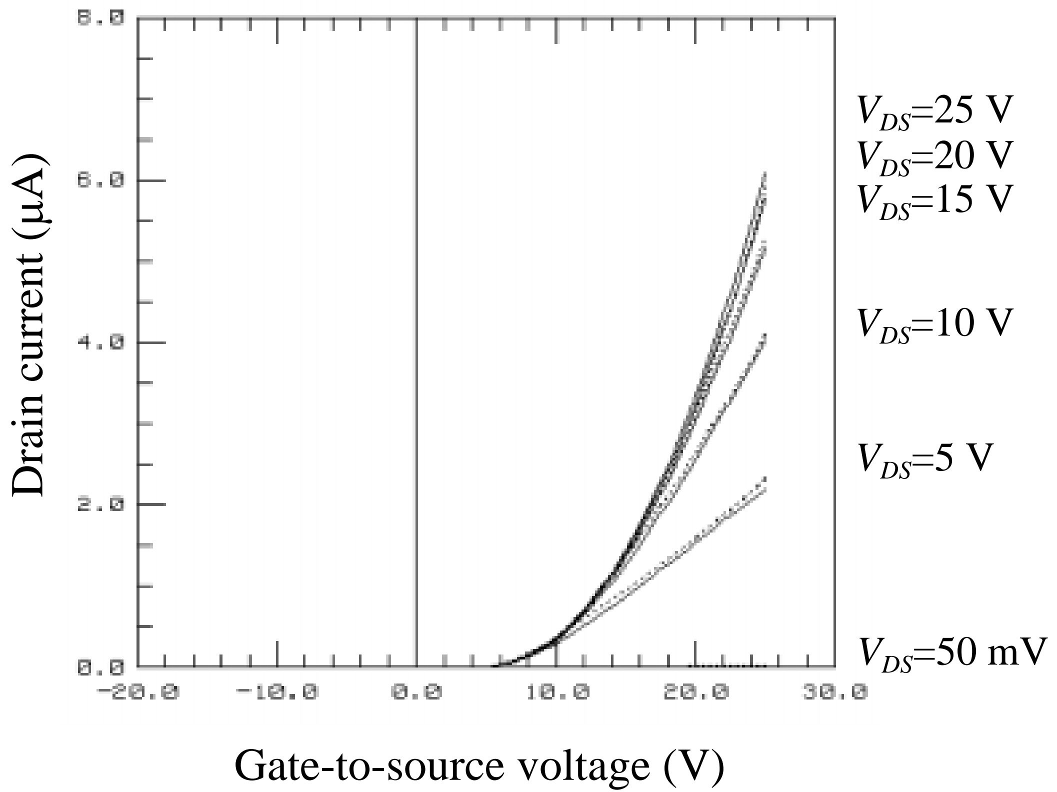
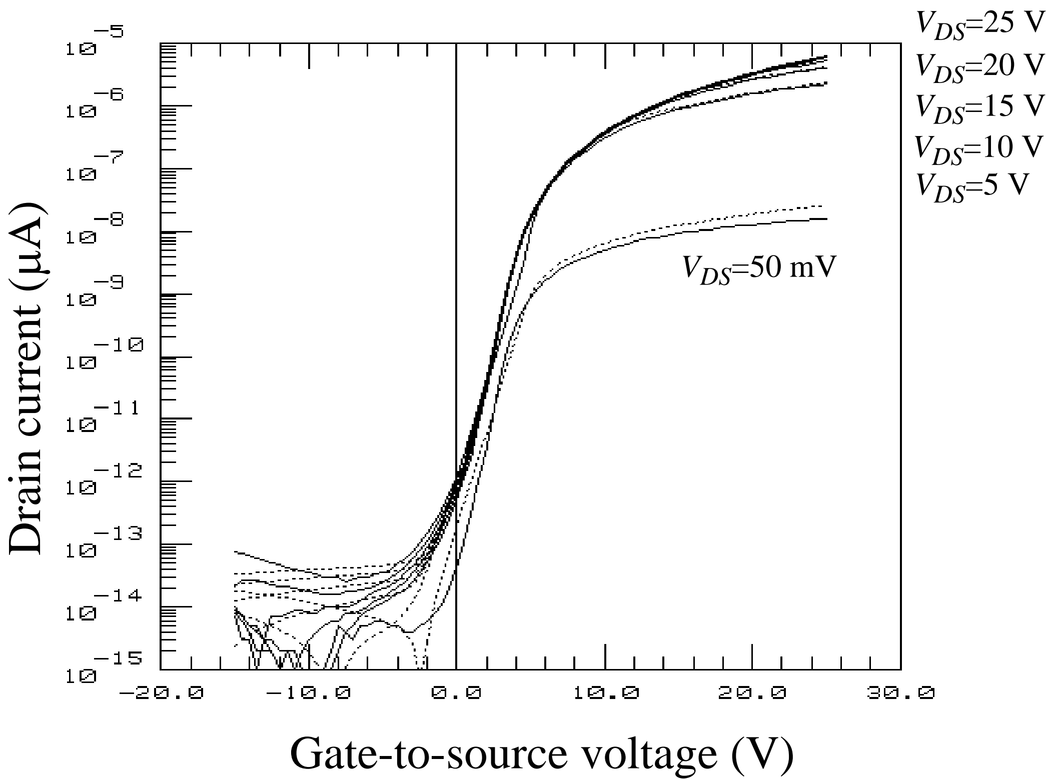


(g)



(h)

Fig. 2.16 Drain current comparison plot between measured and simulated data (a) I_{DS} - V_{DS} at V_{GS} = 5~25 V (b) I_{DS} - V_{DS} at V_{GS} = 4.5 V (c) I_{DS} - V_{GS} at V_{DS} = 25 V (d) $log_e(I_{DS})$ - V_{GS} at V_{DS} = 25 V (e) I_{DS} - V_{GS} at V_{DS} = 5 V (f) $log_e(I_{DS})$ - V_{GS} at V_{DS} = 5 V (g) I_{DS} - V_{GS} at V_{DS} = 50 mV~25 V (h) $log_e(I_{DS})$ - V_{GS} at V_{DS} = 50 mV~25 V. Solid lines are measured, break lines are simulated data.

2.2.4 Temperature effects and Stress

Temperature effects are critical for accurate a-Si TFT modeling. For example, μ_{eff} and V_{TH} are functions of temperature. Since the physical theory is not fully understood, empirical equations are used in the model to represent

those temperature effects. Field effect mobility (μ_{eff}) has a simple temperature effect.

$$\mu_{eff}^{TEMP} = \mu_{eff} \cdot \left(\frac{T_{DEV}}{T_{NOM}} \right)^{T_{REF}} \tag{2.22}$$

where T_{NOM} is the room temperature that is defined in the model, T_{DEV} is the device temperature available in SPICE simulation, and T_{REF} is a fitting parameter.

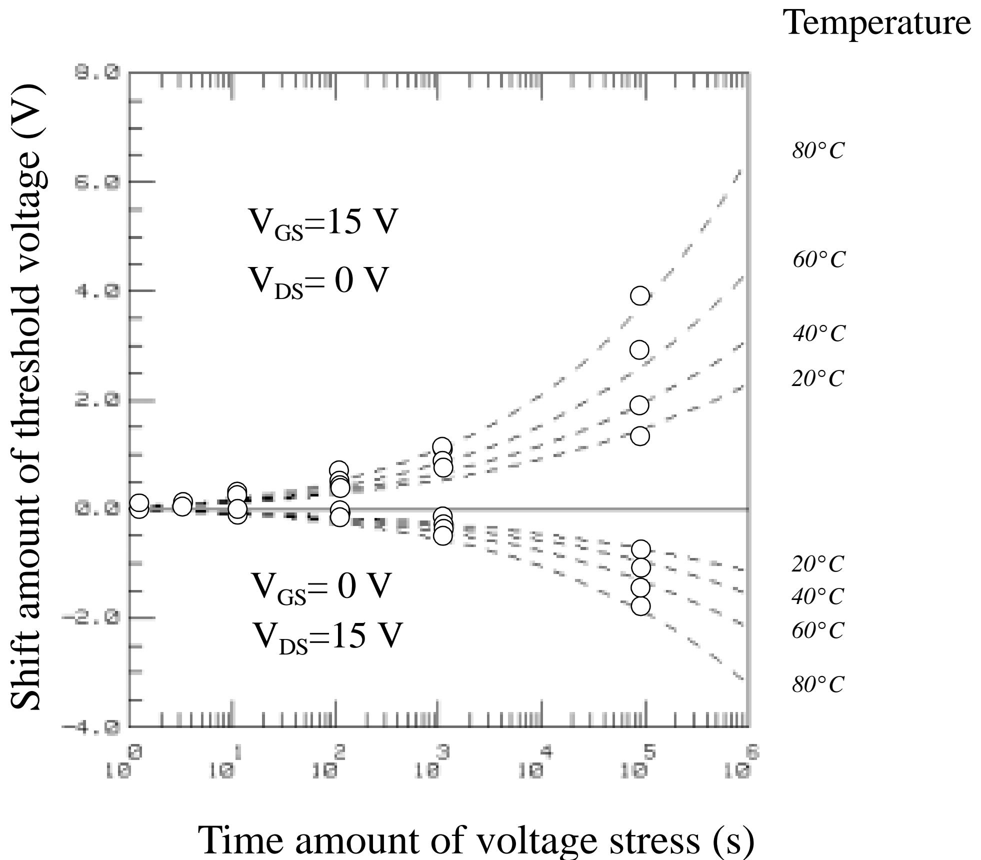


Fig. 2.17 Threshold voltage shift measurement and simulation with voltage stress and temperature. Here the step variable is temperature. The circle indicates measured data of an a-Si:H TFT device.

One of the most important properties of a-Si TFT's is the threshold instability which is generally considered the result of the insertion of electrons into the S_iN_x of gate insulated films or MOS interfaces [10], [11]. We analyzed the temperature characteristic of the threshold voltage using Ibaraki, et al. [17] and our measured data (Fig. 2.17). An inverted staggered a-Si: H-TFT with a SiNx gate insulator film was used for the measurement. The dc bias stress was supplied at TFT gate and drain terminals. Our measured data and Ibaraki, et al. [17] show that threshold voltage

(V_{TH}^{eff}) is a function of $V_{GS,}$ $V_{DS,}$ voltage supplying time (t_{vst}),

and T_{DEV}. A simple partial differential equation is obtained as

$$\frac{\partial V_{THD}}{\partial t_{lg}} = -\frac{q \cdot V_x}{k \cdot T_{DEV}} \cdot V_{THD} \tag{2.23}$$

with

$$V_{THD} = V^{eff}{}_{TH} - V_{TH} \text{ , and } t_{lg} = \log(t_{vst}) \text{ ,} \tag{2.24}$$

where k is the Boltzmann constant and V_x is a fitting parameter.

As an initial condition,

$$V_{THD} = f(V_{GS}, V_{DS}) \quad \text{for } t_{lg} = 0 \tag{2.25}$$

the $f(V_{GS}, V_{DS})$ is empirically approximated by

$$f(V_{GS}, V_{DS}) = V_{THD}\Big|_{t_{vst} = 1} = \nu \cdot \left(V_{GS}^{\psi} - \frac{V_{DS}^{\psi}}{2}\right) . \qquad (2.26)$$

After solving (2.23) with (2.24), (2.25), and (2.26), V_{TH}^{eff} is given by

$$V^{eff}{}_{TH} = V_{TH} + \nu \cdot \left(V_{GS}^{\psi} - \frac{V_{DS}^{\psi}}{2.0}\right) \cdot \exp\left[-\frac{q \cdot V_x}{k \cdot T_{DEV}} \cdot \log(t_{vst})\right] \qquad (2.27)$$

where ν is the first order temperature gradient and ψ is an empirical parameter. Every parameter used in the simulation shown in Fig. 2.17 is directly extracted from the measured data (Table 2.2). Since the measurement was performed under dc bias condition, the analysis and associated equations (2.23)-(2.27) account for steady state stressing. In a TFT-LCD the TFT gate is pulsed with very low duty cycles (0.01% ~ 1%), which will change an a-Si TFT behavior.

2.3 Capacitance Model

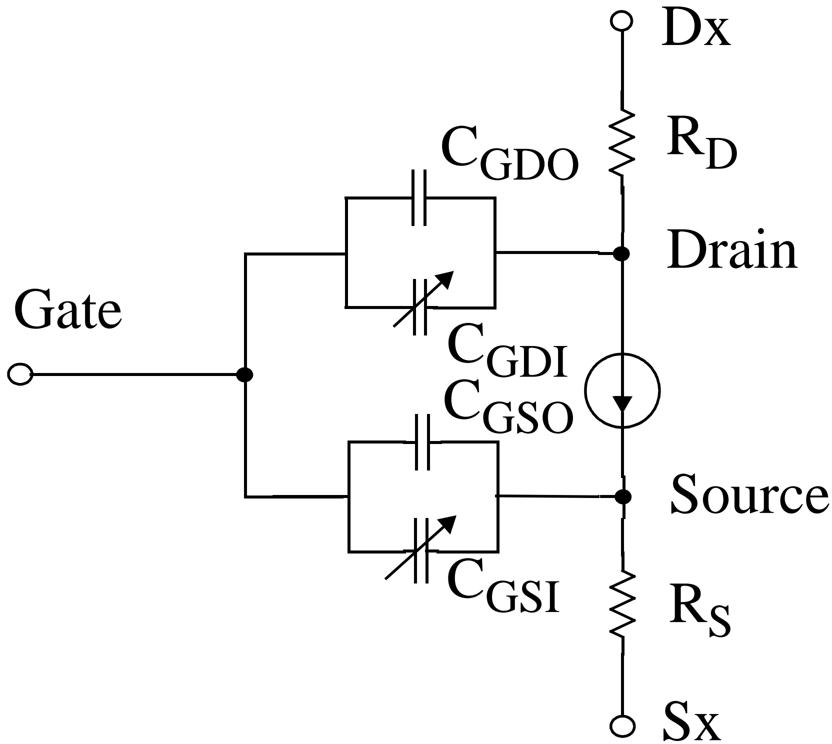


Fig. 2.18 a-Si Equivalent circuit of an a-Si TFT.

As shown in Fig. 2.18, the equivalent circuit of an a-Si TFT is very simple. C_{GS} and C_{GD} are divided into overlap capacitance (C_{GSO}, C_{GDO}) and insulated film and intrinsic a-Si capacitance (MIS capacitance). The dielectric constants of the MIS capacitance (C_{GSI}, C_{GDI}) are bias- and frequency-dependent. The MIS capacitance (C_{MIS}) is calculated as shown in (2.28) [7]

$$C_{MIS}(V) = \frac{\partial Q_{sc}}{\partial V_G} = \frac{\partial Q_{sc}}{\partial(V_{fm} + \phi_{ls})} \quad (2.28)$$

where Q_{SC} is the space charge, ϕ_{ls} is the surface potential at a certain gate voltage, and V_{fm} is the potential drop across the insulated thin film. From the equivalent circuit in Fig. 2.18, C_{MIS} in (2.28) is rewritten as shown in

$$C_{MIS}(V) = \frac{C_{fm} \cdot C_{sc}}{C_{sc} + C_{fm}} . \quad (2.29)$$

Here C_{SC} is the maximum space charge capacitance.

From Fig. 2.18, the gate-to-source and gate-to-drain capacitance are directly given by

$$C_{GS} = C_{GSO} + C_{GSI} \quad (2.30)$$

and

$$C_{GD} = C_{GDO} + C_{GDI} . \quad (2.31)$$

Using Meyer's modeling approach [18], C_{GSI} and C_{GDI} are written as

$$C_{GSI} = \left.\frac{\partial Q_G}{\partial V_S}\right|_{V_D = Const} = -\frac{\partial(Q_m + Q_{SS} + Q_{loc})}{\partial V_S} \quad (2.32)$$

and

$$C_{GSD} = \left.\frac{\partial Q_G}{\partial V_D}\right|_{V_S = Const} = -\frac{\partial(Q_m + Q_{SS} + Q_{loc})}{\partial V_D} \quad (2.33)$$

for $V_{GS} \geq V_{TH}$.

C_{GSI} and C_{GDI} in the linear region are calculated using (2.27), (2.30), and (2.31) as follows:

$$C_{GSI} = C_{MIS}\left[1.0 - \frac{V_{DS}^2}{12.0 \cdot (2.0V_{GS} - 2.0V^{eff}{}_{TH} - V_{DS})^2}\right] \quad (2.34)$$

$$C_{GSI} = C_{MIS}\left(0.5 - \frac{2.0 \cdot V_{DS}(2.0V_{GS} - 2.0V^{eff}{}_{TH} - V_{DS}) + V_{DS}^2}{6.0 \cdot (2.0V_{GS} - 2.0V^{eff}{}_{TH} - V_{DS})^2}\right). \quad (2.35)$$

Below the threshold voltage

$$C_{GSI} = C_{GDI} = 0.0\,. \quad (2.36)$$

However, the simulated result using (2.34), (2.35), and (2.36) has a discontinuity in the transition region around the threshold voltage. Also, the capacitance value in the region is dominant for TFT-LCD transient simulations. Therefore, the model equations are modified by using exponential functions, which are

$$C_{GSI} = C_{MIS} \cdot \exp-[A \cdot (V_{GS} - V^{eff}{}_{TH})]^{-1} \quad (2.37)$$

and

$$C_{GDI} = C_{MIS} \cdot \exp-[A \cdot (V_{GS} - V^{eff}{}_{TH} - V_{DS})]^{-1} \quad (2.38)$$

for $V_{DSAT} > V_{DS}$, where A is a capacitance slope in the transition region.

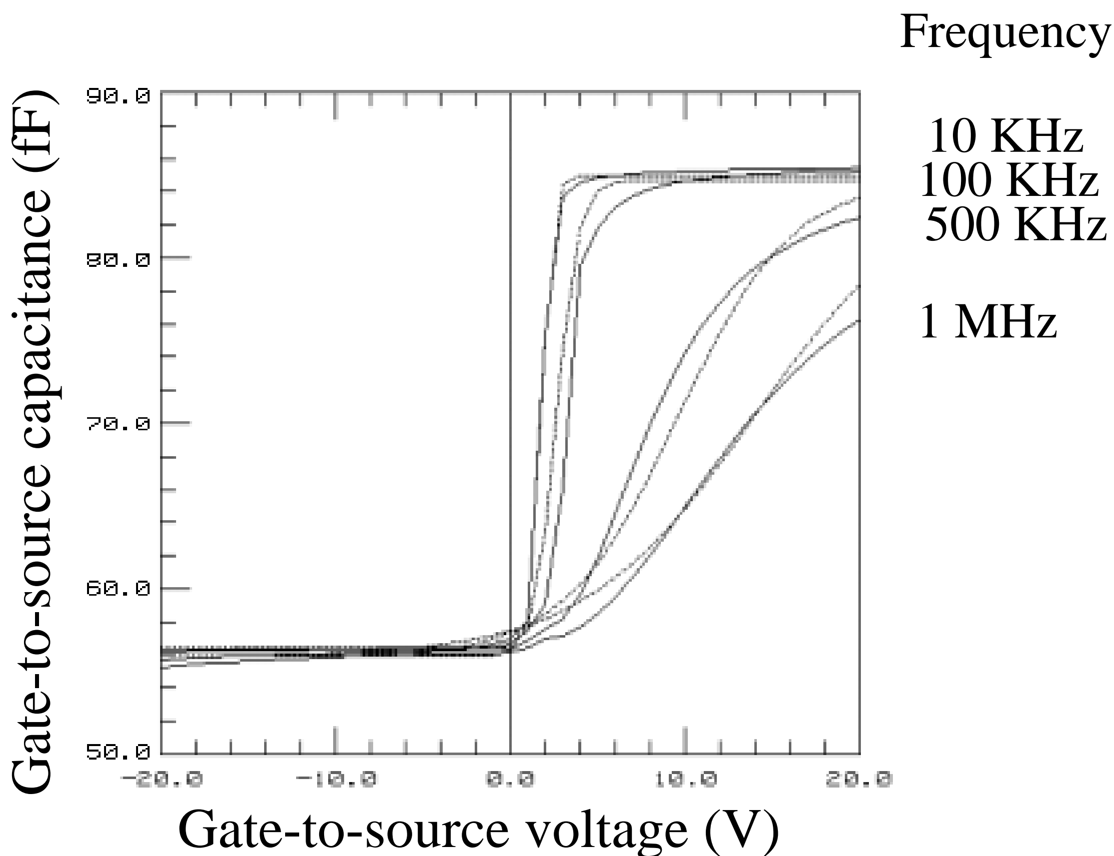


Fig. 2.19 Measured (-) and simulated (- - -) frequency variation of the VDS = 0 gate-to-source capacitance.

The measured capacitance depends also on the frequency of the supplied gate signal both because of the thermal release time of the states as shown in Fig. 2.19, which is their response time to the change in potential, and because of the high-resistivity material, which requires the intrinsic resistance of the a-Si TFT to be taken into account. However, such effects are not as critical as bias voltage effects. Because the SPICE simulator used does not support frequency-dependent capacitance, frequency is treated as a

model parameter for transient analysis. The frequency effect is implemented by using the dielectric constant of amorphous silicon as follows [19]:

$$\varepsilon_f = \varepsilon_{fmac} + \left[\frac{\varepsilon_{fm} - \varepsilon_{fmac}}{1.0 + (2.0 \cdot \pi \cdot f \cdot \tau)^2}\right] \qquad (2.39)$$

where ε_{fm} is the nominal dielectric constant of a-Si, ε_{fmac} is the dielectric constant at the highest frequency, f is the signal frequency, and τ is the relaxation time constant. (2.29) implies a pure capacitance unit.

$$C_{MISlw} = \frac{C_{fm} \cdot C_{sc}}{C_{sc} + C_{fm}} \cdot L \cdot W\,. \qquad (2.40)$$

By using (2.39), equations (2.37) and (2.38) are modified to support frequency dependencies. Now the intrinsic capacitances are derived as follows:

$$C_{GSI} = C_{MISlw} \cdot \frac{\varepsilon_{fmac}}{\varepsilon_{fm} \cdot \exp[-F_{eff} \cdot \varepsilon_f \cdot (V_{GS} - V^{eff}{}_{TH})]} \qquad (2.41)$$

$$C_{GDI} = C_{MISlw} \cdot \frac{\varepsilon_{fmac}}{\varepsilon_{fm} \cdot \exp[-F_{eff} \cdot \varepsilon_f \cdot (V_{GS} - V^{eff}{}_{TH} - V_{DS})]} \qquad (2.42)$$

where F_{eff} is the frequency effect compensation of each a-Si device.

For $V_{DS} \geq V_{DSAT},$

$$C_{GSI} = 0.5 \cdot C_{MISlw} \qquad (2.43)$$

and

$$C_{GDI} = C_{MISlw}\,. \qquad (2.44)$$

The parameter extraction of the a-Si TFT capacitance model was performed by using a set of measured data in Fig. 2.19. The extraction process is as follows:

1. Set the applied small signal ac frequency of capacitance meter to the model parameter, f
2. Read the capacitance value at the $V_{TH} < V_{GS}$ region and modify it to C_{GSO}
3. Optimize model parameters, τ, f_{eff}, C_{sc}
4. Measure C_{GD} versus V_{GS} using a capacitance meter
5. Read the capacitance value at the $V_{TH} < V_{GS}$ region and modify it to C_{GDO}

2.4 A Liquid Crystal Capacitance Model

The capacitance characteristic of liquid crystals are very important to simulate LCD panel since they are drastically modulated by the applied rms voltages. Although its details will be discussed in chapter 5, the Liquid Crystal (LC) capacitance as a bias and frequency dependent device is modeled in this section.

Liquid crystal capacitance (C_{lc}) and gate-to-source capacitance (C_{gs}) in a TFT are bias and time dependent. The dielectric constant of liquid crystal is bias dependent because of the mechanical crystal behavior. The mechanism has been thoroughly analyzed by liquid crystal makers. However, the formulation is very dependent on each liquid crystal type. An empirical approach is used to support every type of liquid crystal. A simple LC capacitance model in combination with the a-Si TFT model is used to simulate the transient response of LCD pixels.

Because of the anisotropy of LC material, the liquid crystal capacitance (C_{lc}) is not constant. It varies from a minimum capacitance when no voltage is applied across the LC cell to a maximum capacitance when the LC cell is fully turned on [20]. Thus, the liquid crystal capacitance C_{lc} is bias- and time-dependent. This mechanism has been thoroughly analyzed by liquid crystal manufacturers and some laboratories. However, the formulation is very

dependent on the specific liquid crystal type. An empirical approach is used to support various types of liquid crystal in this model.

The permittivity factor, $\varepsilon_{PS,}$ of the model is bias-dependent. The model equation is formulated based on $\varepsilon_{PL,}$ the dielectric permittivity base value. The viscosity of liquid crystals is expressed by δ. D_{TIME} is delay time at each bias step. γ is a fitting parameter used to account for the change in slope due to threshold voltage. V_C is a threshold voltage that expresses the starting value of increasing ε_{PS} as

$$\varepsilon_{ps} = \varepsilon_{pl} + \delta \cdot \gamma \cdot \exp(D_{time}) \cdot \sqrt{\frac{V}{V_C} - 1.0}\ . \qquad (2.45)$$

The total amount of LC capacitance (C_{lc}) is calculated from ε_{PS} and the geometry of the LC cell as

$$C_{lc} = \frac{\varepsilon_0 \cdot \varepsilon_{ps} \cdot A_{cell}}{D} \qquad (2.46)$$

where L and W are used to calculate the total area of the LC cell which is connected to each TFT, D is the thickness of the LC cell (cell gap), and $\varepsilon_0 = 8.854 \cdot 10^{-12}$ F/m.

Fig. 2.20 shows the measured and simulated liquid crystal capacitance using twisted nematic (TN) type liquid crystals. Model parameters of the LC cap model are optimized with the measured data. Since the model is so sim-

ple and flexible, the simulation accuracy can be high enough to use the model for LCD panel simulations.

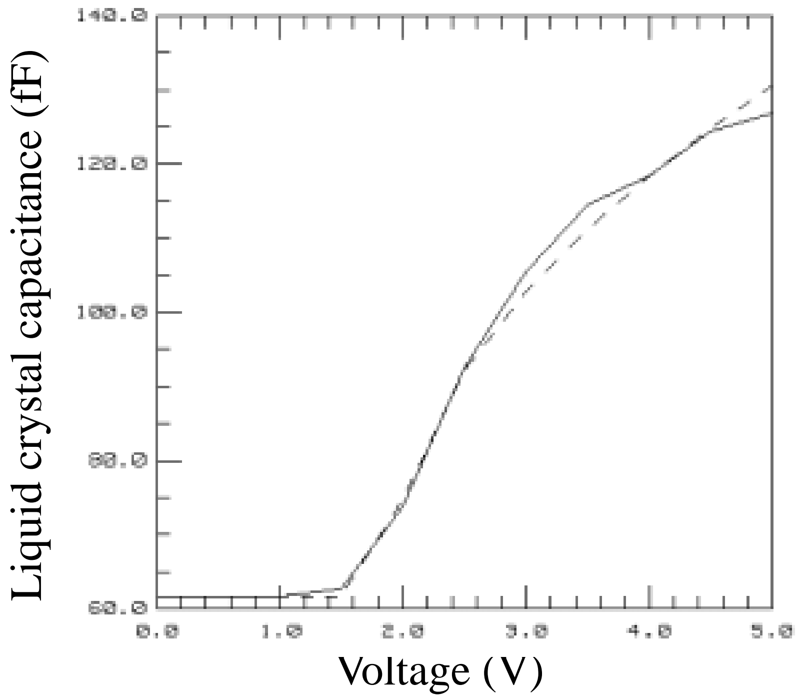


Fig. 2.20 Measured (-) and simulated (- - -) TN liquid crystal capacitance comparison of a sample device.

2.4.1 A List of the a-Si TFT and LC capacitance Model Parameters

Table 2.2 Extracted (a) a-Si TFT and (b) LC Capacitor model parameters

(a)	(b)
L = 11 μm	L = 152 μm
W = 41 μm	W = 148 μm
μ_O = 0.450 cm^2/Vs	D = 10.02 μm
V_{TO} = 1.699 V	δ = 51.0 mm^2/s
ϕ = 0.620 V	γ = 51.2 ms/mm^2
N_{FS} = 1.925x10^{21} cm^{-2}	D_{TIME} = 100 ms
V_{sat} = 2,783 m/s	V_C = 1.887 V
θ = 17.8 mV^{-1}	ε_{PL} = 3.1
η = 410.8μ	
T_1 = 300 nm	
T_2 = 0	
ε_1 = 3.9	
ε_2 = 0	
g_o = 9.728x10^{-15} Ω^{-1}	
T_{REF} = 1.5	
C_{GSO} = 52.03 fF	
C_{GDO} = 42.21 fF	
C_{SC} = 158.8 μF/m	
R_D = 8,030 Ω	
R_S = 8,030 Ω	
f = 100 KHz	
D_{EFF} = 1.968	
τ = 10.7 ns	
f_{EFF} = 0.302	
ν = 0.008	
ψ = 0.2	
V_x = 0.033 V	
t_{vst} = 100 ms	
T_{NOM} = 300.15 K	

2.5 SPICE3 Implementation

2.5.1 Non-linear Transistor Simulation with SPICE

The simplified SPICE simulation flow of an active device model is shown in Fig. 2.21. The device model consists of model equations and an admittance matrix (Y-Matrix).

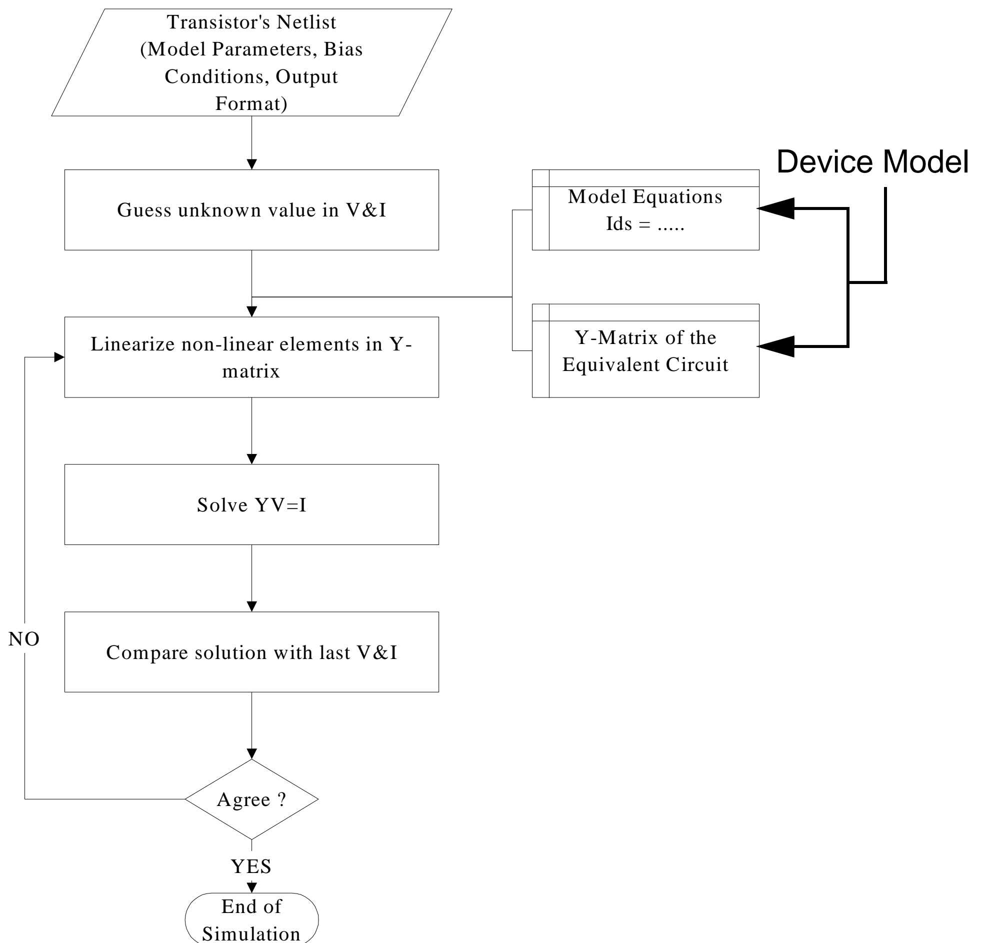


Fig. 2.21 SPICE simulation flow for non-linear device models.

However, to derive non-linear model equations linearization should be considered because SPICE can treat only linear elements in Y-matrix in addition to the model equation derivation that are described in 2.2, 2.3, and 2.4. An example of linearization is presented in Fig. 2.22

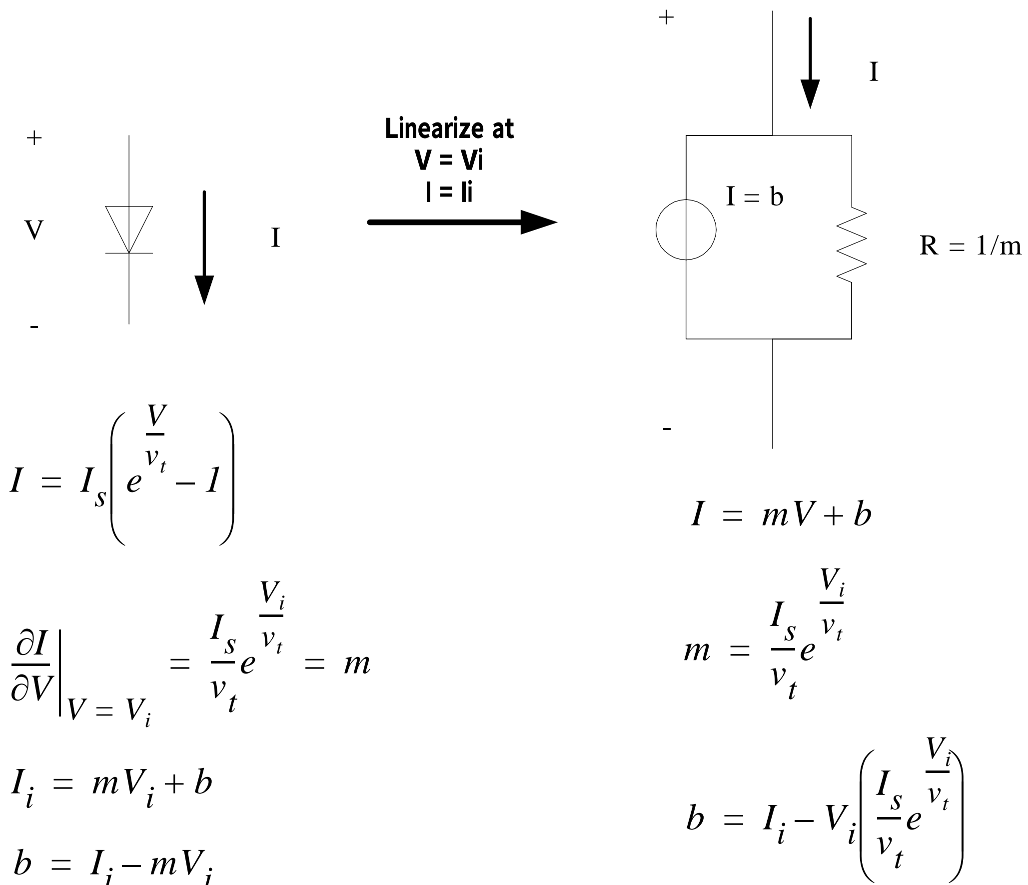


Fig. 2.22 An example of diode model linearization.

For instance a diode's characteristic is not a straight line on the *I-V* plane. By linearization the *I-V* characteristic is approximated about the bias point

with a straight line using the equation $I=mV+b$, which is much simpler to manipulate where used in a Y-matrix. Here, m and b are variable that depend on the bias point (V_i, I_i). In an iteration where the vectors V and I are being solved, V_i and I_i will change and so m and b will change correspondingly.

The Y-matrix can be loaded by using Kirchoff's voltage and current laws. Fig. 2.23 is an equivalent circuit of a three terminal FET which is used in the a-Si TFT model.

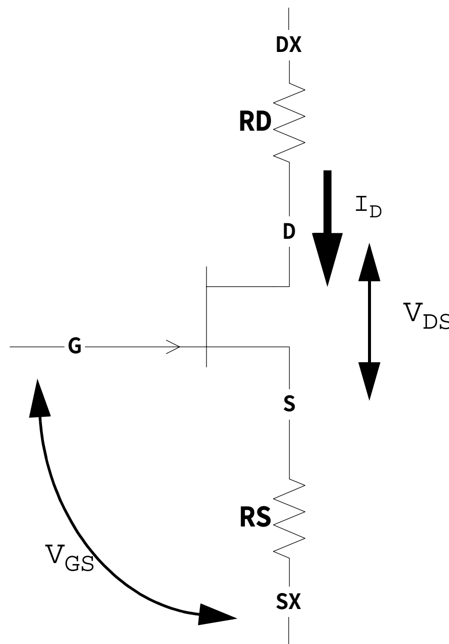


Fig. 2.23 An equivalent circuit example of a three terminal FET.

The Y-matrix for the three terminal FET is formulated as shown below:

here, reference node is assigned to the source terminal (s node in Fig. 2.23). To treat voltage controlled current sources as admittance elements the

definition of (2.48) and (2.49) are needed. (2.50) is the result Y-matrix of the FET.

$$I_D = f(V_{GS}, V_{DS}) \tag{2.47}$$

$$g_m = \frac{\partial I_D}{\partial V_{GS}} \tag{2.48}$$

$$g_{ds} = \frac{\partial I_D}{\partial V_{DS}} \tag{2.49}$$

$$\begin{array}{c} \\ \mathrm{DX} \\ \mathrm{G} \\ \mathrm{SX} \\ \mathrm{D} \\ \mathrm{S} \end{array} \begin{array}{c} \begin{array}{ccccc} \mathrm{DX} & \mathrm{G} & \mathrm{SX} & \mathrm{D} & \mathrm{S} \end{array} \\ \begin{bmatrix} g_d & & & -g_d & \\ & & & & \\ & & g_s & & -g_s \\ -g_d & g_m & & g_{ds} + g_d & -g_m - g_{ds} \\ & -g_m & -g_s & -g_{ds} & g_s + g_m + g_{ds} \end{bmatrix} \end{array} \tag{2.50}$$

2.5.2 Adding a Device to SPICE3

The basic philosophy behind the process of adding another model to the SPICE3 model library is to find an already existing model that has three terminals within the library to serve as a template for the new model. Due to the intricate structure of SPICE, many files have to be copied while other files have to be changed. Below is a listing of *all* files which need to be changed and where exactly in the files the changes need to be made.

2.5.3 Changing the Files

In the following list, the a-Si TFT model will be a new device that needs to be added from UCB junction FET model as a template:

1. In /spice3e2/src/include, copy the following files:

   from:jfetdefs.hinto:atftdefs.h
   from:jfetext.hinto:atftext.h
   from:jfetitf.hinto: atftitf.h

2. Change the file inpdefs.h to include the new device

3. In /spice3e2/src/lib/inp:

   Find the file inp2j.c (jfet file) and copy it into another file named inp2a.c ("a" for atft). Find the places where code describes how SPICE is to refer to the new device, For example (in jfet):

   mytype = INPtypelook("JFET");

   change to (for atft):

   mytype = INPtypelook ("ATFT");

   There are other places where these types of changes need to be made, as follows:

   Find inppas2.c to reference inp2a.c (look for the cases.)
   Find inpdomod.c to add new device (look in the else if statements).
   Insert inp2a.c and inp2a.o into the file makedefs for SPICE compilation.

4. In /spice3e2/src/lib/fte:

   Change the subckt.c file. Look for the case descriptions and copy the appropriate "block" of code for atft. Also towards the end of the file, make the change regarding the number of nodes the new model contains.

5. In /spice3e2/conf:

   Change the file defaults. There is a line which begins with "DEVICES" in which the "atft" name should be added to the long list of models

6. In /spice3e2/util/lib:

   Change the file make_def.bd. Change made to line which begins with "ALL_DEVICES" and add "atft" name

7. In /spice3e2/src/bin

Make changes to config.c in two places to add atft

8. In /spice3e2/src/lib/dev/jfet

   Copy over all *.c files and within those files change the JFET prefix to the ATFT prefix and the jfet prefix to the atft prefix

   Copy over makedefs and change the jfet prefix to the atft prefix.

Once all of these changes have been made, a new device will exist with the same model as JFET. Now the model equations for the ATFT model need to be added. The following paragraphs describe how to add these model equations and which of the above files need to be changed.

2.5.4 Implementation of Particular Model Characteristics

2.5.4.1 Adding "Instance" Parameters

All changes will only need to be made in two directories:

spice3e2/src/lib/dev/atft/(an assortment of *.c files)

spice3e2/src/include/(in the file atftdefs.h only)

Each model has its own set of instance parameters and model parameters. The instance parameters are the ones after each element declaration. For example:

```
A1 1 2 3 ATFTMOD L=20U W=30U TNOM=27
```

The "instance" parameters are *L, W*, and *TNOM*. To add another instance parameter we need to make changes in the following files:

- atftset.c
- atftpar.c,
- atftask.c, and
- atft.c

As an example, we will add the parameter *TNOM* (assume it has not been added). To start off, we need to tell SPICE what the default value for *TNOM* is supposed to be. Edit the file atftset.c and search for the place in the file which has: if(!here->ATFT...).

"Here" refers to SPICE referencing its instance parameters and it is in this place where we need to add:

```
if (!here->ATFTtnomGiven) {
here->ATFTtnom = 27;   /* in Celsius */
}
```

The TNOM parameter has just be set to a default of 27 (if SPICE does not find the value given by user). The next step is to tell SPICE that the instance parameter should be part of its structure. Files atftask.c and atftpar.c serve this purpose. In these files we need to add the following:

(atftask.c):

```
case ATFT_TNOM:
value->rValue = here->ATFTtnom;
return (OK);
```

(atftpar.c):

```
case ATFT_TNOM:
here->ATFTtnom = value->rValue;
here->ATFTtnomGiven = TRUE;
break;
```

Remember what you called or how you referenced “*tnom*” in atftset.c (we named it “ATFTtnom”) and duplicate its name in the appropriate places in the above files. In addition, keep track of the variable “ATFTtnomGiven” for implementation in the file atftdefs.h.

You can find the file atftdefs.h under the path /spice3e2/src/include. It was one of the files we copied from jfetdefs.h in the list at the beginning of this section. In any event, we need to declare the variables “ATFTtnom” and “ATFTtnomGiven” as instance parameters. Look for the place to do this under “typedef struct sATFTinstance {“. After doing this, search further on in the same file until you see “/* device parameters */” where there are many #defines. Recall in atftask.c and atftpar.c we had “case ATFT_TNOM”. We must now repeat that (without the word “case”) in the #defines and assign it a number. This number is the “id tag” SPICE will use to reference this parameter internally.

The final detail SPICE needs to know is how the user is going to reference this parameter from the netlist. Edit the file atft.c and look for:

```
IFparm ATFTpTable[] = { /* parameters */
```

and add the following:

```
IOP("tnom",ATFT_TNOM, IF_REAL, "Device temperature"),
```

where: IOP("tnom" is the user netlist
ATFT_TNOM is referenced by atftdefs.h
IF_REAL signifies that tnom is a real value
Device temperature is the description of the instance parameter

IOP stands for (I)nput, (O)utput, (P)arameter. The above line declares that ATFT_TNOM can be called by "tnom" by the user in the netlist. Thus "tnom" is a user inputted parameter which SPICE can now output to its simulation routines.

After all this has been done, the variable tnom can be used in atftload.c as part of model equations. But first you must "get" its value by typing "temperature = here->ATFTtnom" within atftload.c. Now the variable temperature contains whatever value as a part of its calculations.

2.5.4.2 Adding Model Parameters

Model parameters are, of course, the ones after the .MODEL statement. Their implementation in SPICE is exactly the same as that for instance parameters with some exceptions. The general rule is that we must now search for code that is named by model rather than by instance. Some examples are the following: look for "model->ATFT..." rather than "here->ATFT...". Instead of "IFparm ATFTpTable [ ] = { /* parameters */" we must look for

“IFparm ATFTmTable[] = { /* model parameters */”. There are other obvious examples.

2.5.5 DC and CV Characteristics

Adding device equations is now easy since all the variables which describe the model have been defined to SPICE. The file of interest is primarily atftload model equations is atftload.c.

The DC model equations come after the voltage initialization block of “if” statements. These “if” statements check to see which circuit mode SPICE is in order to set the correct node voltages for iteration. In atftload.c, comments explain exactly where DC calculations begin and end to facilitate future reading or debugging of the code (if the latter is necessary). The same is true for CV model equations. Comments are clearly provided to indicate the exact placement of CV code.

2.5.6 SPICE Input Deck Format of the a-Si TFT Model

2.5.6.1 General Form

AXXXX DRAIN GATE SOURCE MNAME <WIDTH> <LENGTH> <TNOM>

2.5.6.2 Example

A1 1 2 0 TFTMOD L=150U W=180U TNOM=27

Understanding this model's use is rather easy. The “A” letter tells SPICE that you want to use the ATFT. The DRAIN, GATE, and SOURCE nodes are

self-explanatory. As always, MNAME is the particular model name you assign to the declaration of the ATFT transistor in the netlist. It must of course be the same as the MNAME that appears first in the .MODEL statements. The default element (or instance as they are referred in SPICE) values are as follows:

Table 2.3 Default values for instance parameters in the a-Si TFT model

#	name	parameter	units	default	example
1	*L*	Length geometry	m	10.0u	15.0u
2	*W*	Width geometry	m	40.0u	80.0u
3	*TNOM*	Nominal device temperature	C	27	25

Besides the above “instance” parameters, the ATFT model also requires “model” parameters. These model parameters are assigned in the .MODEL card statement and the model type MUST be denoted by either “NAT” for N type Amorphous TFT or “PAT” for P type Amorphous TFT.

For example:

```
<in the netlist>
Y1 2 0 TFTMOD L=10U W=30U TNOM=30

<in .MODEL card statement>
.MODEL TFTMOD PAT
<list model parameters here as usual>
```

The various model parameters and their defaults are the following.

Table 2.4 a-Si TFT model parameters and their defaults.

#	name	parameter	units	default	example
1	*UO (U0)*	Mobility	cm^2/V*sec	1.0	4.1

#	name	parameter	units	default	example
2	*VTO (VT0)*	Zero voltage threshold voltage	V	0.0	1.1
3	*PHI*	Surface potential	V	0.0	600m
4	*NFS*	Surface fast state density	cm^2	0.0	1e18
5	*NSS*	Surface state density	cm^2	0.0	1e21
6	*T1*	1st thin film thickness	m	280n	500n
7	*T2*	2nd thin film thickness	m	0.0	400n
8	*E1*	Dielectric constant of 1st film film thickness	-	3.9	3.0
9	*E2*	Dielectric constant of 2nd film thickness	-	0.0	2.4
10	*THETA*	Mobility modulation	V^-1	0.0	-17.71m
11	*ETA*	Static feedback on threshold voltage (difficulty of band bending)	V^-1	0.0 270.3u	
12	*VMAX*	Maximum drift velocity of carriers	m/sec	1e6	1.231e3
13	*GO*	Conductance of TFT leakage current	Ohm^-1	10e-15	2.2e-15
14	*DEFF*	Drain voltage effect for TFT leakage current	-	2.0	2.15
15	*NU*	1st order temperature gradient	-	0.0	1.2
16.	*VX*	Temperature exponential part	-	0.001	0.1
17	*PSI*	Temperature exponential part	-	0.01	1.0
18	*TVST*	Voltage stress	sec	10m	100
19	*TREF*	Temperature gradient of UO	-	1.5	0.9
20	*RD*	(External) Drain resistance	Ohm	1.0K	0.0
21	*RS*	(External) Source resistance	Ohm	1.0K	1.306K
22	*CGSO*	TFT gate-to-source overlap capacitance	F	1.0p	2.1p
23	*CGDO*	TFT gate-to-drain overlap capacitance	F	1.0p	2.1p
24	*CSC*	Space charge capacitance	F/m^2	10u	500u
25	*FREQ*	Frequency of device	Hz	400	100K

#	name	parameter	units	default	example
26	*FEFF*	Frequency effect constant	-	0.5	0.3
27	*TAU*	Relaxation time constant	sec	10n	4.6n

2.5.7 SPICE Input Deck Format of the LC cap Model

2.5.7.1 General Form

YXXXX C+ C- MNAME <LENGTH> <WIDTH> <DISTANCE>

2.5.7.2 Example

Y1 2 0 CAPMOD L=150u W=180u D=500n

Understanding this model's use is rather easy. The “Y” letter tells SPICE that you want to use the LC capacitor. C+ and C- are the positive and negative polarities of the capacitor with the same usage as the standard fixed capacitor. MNAME is the model name you assign to the particular declaration of the LC capacitor in the netlist. It must of course be the same as the MNAME that appears first in the .MODEL statements. The element (known as instance) parameters such as length, width, and distance which appear after the MNAME declaration describe the geometry of the device. While “*L*” and “*W*” are self explanatory, the user might like to take note that “*D*”, which does not appear in the fixed capacitor or semiconductor capacitor model, refers to the space between the LC capacitor plates. The default values are as follows:

Table 2.5 Default values for instance parameters in the LC cap model.

#	name	parameter	units	default	example
1	*L*	Length geometry	m	2.0u	150.0u
2	*W*	Width geometry	m	3.0u	180.0u
3	*D*	Thickness of LC capacitive plates	m	500n	700n

Besides the above "instance" parameters, the LC capacitor model also requires "model" parameters. These model parameters are assigned in the .MODEL card statement and the model type MUST be denoted by "LCD."

For example:

```
<in the netlist>
Y1 2 0 CAPMOD L=150u W=180u D=500n

<in .MODEL card statement>
MODEL CAPMOD LCD
<list model parameters here as usual>
```

The various model parameters and their defaults are the following:

Table 2.6 Default values for instance parameters in the LC cap model.

#	name	parameter	units	default	example
1	*DELTA*	Viscosity constant	-	5.2	4.1
2	*GAMMA*	Bias dependent gradation constant	-	1.0	512.1m
3	*DTIME*	Bias voltage sweeping time	sec	10m	100m
4	*VC*	Threshold voltage of LC	V	1.0	1.887
5	*EPL*	Dielectric permittivity factor	-	3.1	3.1

2.6 Conclusions

A critical modeling requirement of a-Si TFT's is to simulate off-region leakage current. Also, temperature and voltage stress effects, which are caused by back lighting of the LCD and applied voltage, must be implemented in the model. The characteristics of a-Si TFT's vary according to the device processing. The model, therefore, is flexible in order to represent different types of a-Si TFT devices.

The a-Si TFT model is based on a semi-empirical approach similar to UCB's MOS Level 3 TFT model. The model focused on the inverted staggered type a-Si device structure and incorporates such unique a-Si characteristics as duo-insulating film, dependent gate capacitance, and the existence of large numbers of localized states that give rise to large threshold voltages. In addition, the model also incorporated a sub-threshold behavior that was comprised of a leakage current that arises from optical and channel current flowing from gate to source as well as from gate to drain. These and other DC behaviors were captured by 22 different model parameters. The capacitance behavior of the a-Si TFT model was derived from the simple Meyer capacitance model. Specifically, all charge storage was divided into two capacitance types: C_{GD} and C_{GS}. Each capacitance type was further

divided into two parts: overlap and intrinsic. The intrinsic capacitance is further composed of a series formulation of the insulating capacitance.

Also, the liquid crystal capacitances were dominant in simulation of LCD cells. The liquid crystal capacitance is voltage-dependent because of the crystal operation mechanism. There are several types of liquid materials and shapes. For this reason, the liquid crystal model has been developed using the algebraic method.

Those two models are accurate enough for simulating advanced a-Si TFT's used in any applications such as image sensors, low speed driver circuits, and LCD panels. The a-Si TFT model had been adopted by Avant!'s HSPICE and Agilent Technologies' IC-CAP characterization software programs.

Chapter 3 LCD Simulation Techniques as An Instance of Large Scaled Circuit Simulations

Introduction

Device models that we have mentioned so far are used with many passive components and are employed mainly for analog circuit simulations. However, it takes extremely long time to simulate a very large circuit such as an LSI and an LCD because of the limitation of the number of maximum nodes. In some cases the simulation projects cannot be completed. Recently, various kind of simulators have been developed to break into such limitation. For example, some simulators equipped function models [3] that each function block is written by mathematical equations, others adopt table-lookup models [24] that are based on electrical measurement database and normalized equations. Any simulation data points are picked up from the lookup-table. In this research macro models have been developed by using geometry scaling rules and some lumped sum elements to perform fast simulations of large LCD panels which have 800 x 600 pixels.

Transient simulations of liquid crystal displays addressed by thin film transistors (TFT-LCD's) are necessary to predict the LCD performance. To simulate an LCD panel correctly, we need to model the amorphous silicon thin film transistors (a-Si TFT's), liquid crystals (LC's), and interconnects. Since we developed a-Si TFT and LC cap models [23], the pixel level simulation can

be performed without any difficulty. Alternatively, some authors had published the a-Si TFT device physics and models [4]-[7]. However, there is no practical reports and papers for a full LCD panel dynamic simulation so far. This paper demonstrates a method to simulate an FPD for predicting the performance using macro models.

Due to the large number of pixels 640 x 480 x 3 for a standard color display monitor) a direct simulation of the whole display is not feasible. Therefore, we use dummy pixels to reduce the complexity of the simulation. We present an easy and effective simulation method using three types of dummy pixels. These pixel macro models, which include the dummy pixels and real pixels for analysis, are formed by using our a-Si TFT and LC cap models. The model parameters were extracted from measured data. We analyzed critical TFT-LCD transient effects such as the voltage drop due to gate-to-source and LC capacitance and effective drive voltage V_{rms}, which is supplied to a liquid crystal cell, by changing the number of dummy pixels.

3.1 Flat Panel Display (FPD) Basics

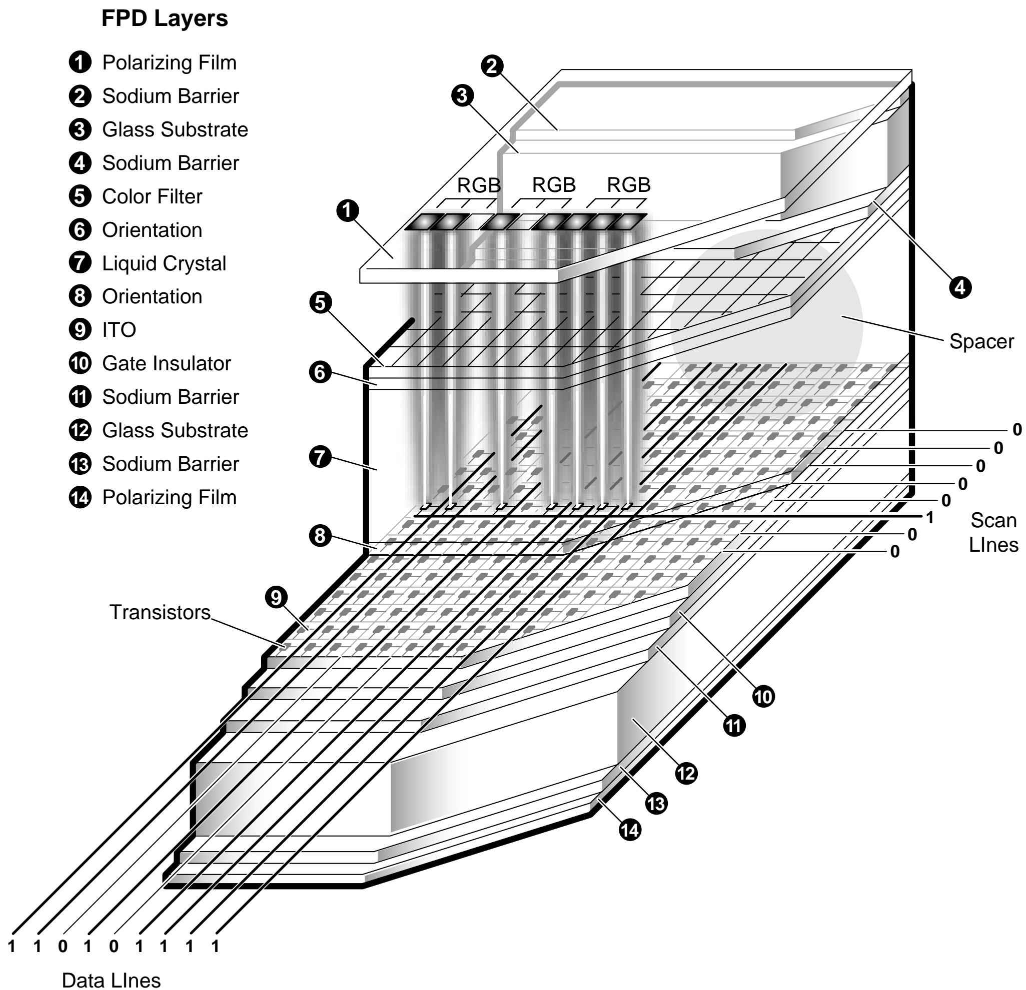


Fig. 3.1 Typical Active Matrix Flat Panel Display Construction.

A finished flat panel display consists of many layer elements. The typical layers in an active matrix FPD are illustrated in Fig. 3.1. An explanation of each layer follows.

3.1.1 Polarizing Film

Light passing through one of the layers of polarizing film, then through a pixel area of the liquid crystal layer, has its polarization direction rotated. The polarization direction follows the physical rotation of the liquid crystal molecules. The polarizing film on the exit side of the liquid crystal cell is positioned to allow the rotated light to pass through. Viewed from the exit side, the pixel is clear, or transmitting.

3.1.2 Sodium Barrier

Sodium-free glass is used for active matrix displays, because the presence of sodium is considered harmful to the reliability of displays where thin-film devices such as diodes or transistors are used. In the event sodalime glass is used, a sodium barrier is deposited that surrounds each glass substrate to prevent any possible contamination.

3.1.3 Glass Substrate

The glass substrate is an essential component of the display, and expensive compared to the rest of the FPD. Very tight control of the optical and mechanical properties of the glass are required at every stage of the process, especially when heating is involved. The glass, ordinarily 1.1 mm thick, ranges in size from 300 x 300 mm to 450 x 450 mm for the fabrication of large displays. Even larger sizes will be used in the future.

Glass substrates are trimmed to size after the fusion or float process, typically to about one meter on a side. Various mechanical operations follow the forming process, depending on the ultimate application of the material.

Since glass is brittle and easily chipped or cracked at the edges, it is typically beveled, chamfered or otherwise treated to reduce chipping during handling. Thermal stresses at edge cracks accumulate during substrate processing, and lead to breakage. Glass breakage is a major problem in flat panel production. First of all, the broken plate is itself a yield loss, but fragments of glass may remain behind in carriers or equipment to cause particulate contamination or scratching of other substrates.

3.2 Feasibility Study

Timing simulations of entire FPD are very important to predict the TFT-LCD total performance. The one pixel simulation methodology that we have discussed so far is one of the key parts for evaluating TFT-LCD's. However, for simulating entire FPD parasitics which include capacitance and resistance of busline interconnects must be modeled. Because total number of pixels in a FPD is 640 x 480 x 3 in a standard color and 800 x 600 x 3 in a high density color, it takes more than thirty minutes to simulate with a SPICE simulator on a HP 712 PA RISC workstation.

Therefore, in this research all other pixels than the pixels to be monitored, what we called as dummy pixels, are macro modeled and interconnects are modeled by using lumped sum and distributed RC components. The distributed components are used to model common busline parasitics. The accuracy and simulation speed of the fabricated macro models will be verified by comparing it with measured data and conventional simulations.

There are three types of macro models to be developed. Each of them includes a-Si TFT and Liquid crystal capacitance (LC cap) models. These macro models are based on device model parameter scaling theory. The total number of dummy pixels and monitor pixels to be used for FPD simulations are nine pixels regardless of the FPD size. To increase the number of dummy pixels the simulation accuracy will be improved. On the contrary the simula-

tion speed will be slow down drastically. Therefore, the total number of pixels are fixed to nine initially in this research. Later on, it has been further increased to 16 (4 x 4) though 36 (6 x 6) to check the relationship between the simulation speed and the accuracies.

3.2.1 TFT-LCD panel Modeling

A typical structure of a TFT-LCD is shown in Fig. 3.2. One TFT is used to turn on and off the source current which charges liquid crystals capacitance at each pixel. The small inset of Fig. 3.2 is the zoomed illustration of one pixel equivalent circuit.

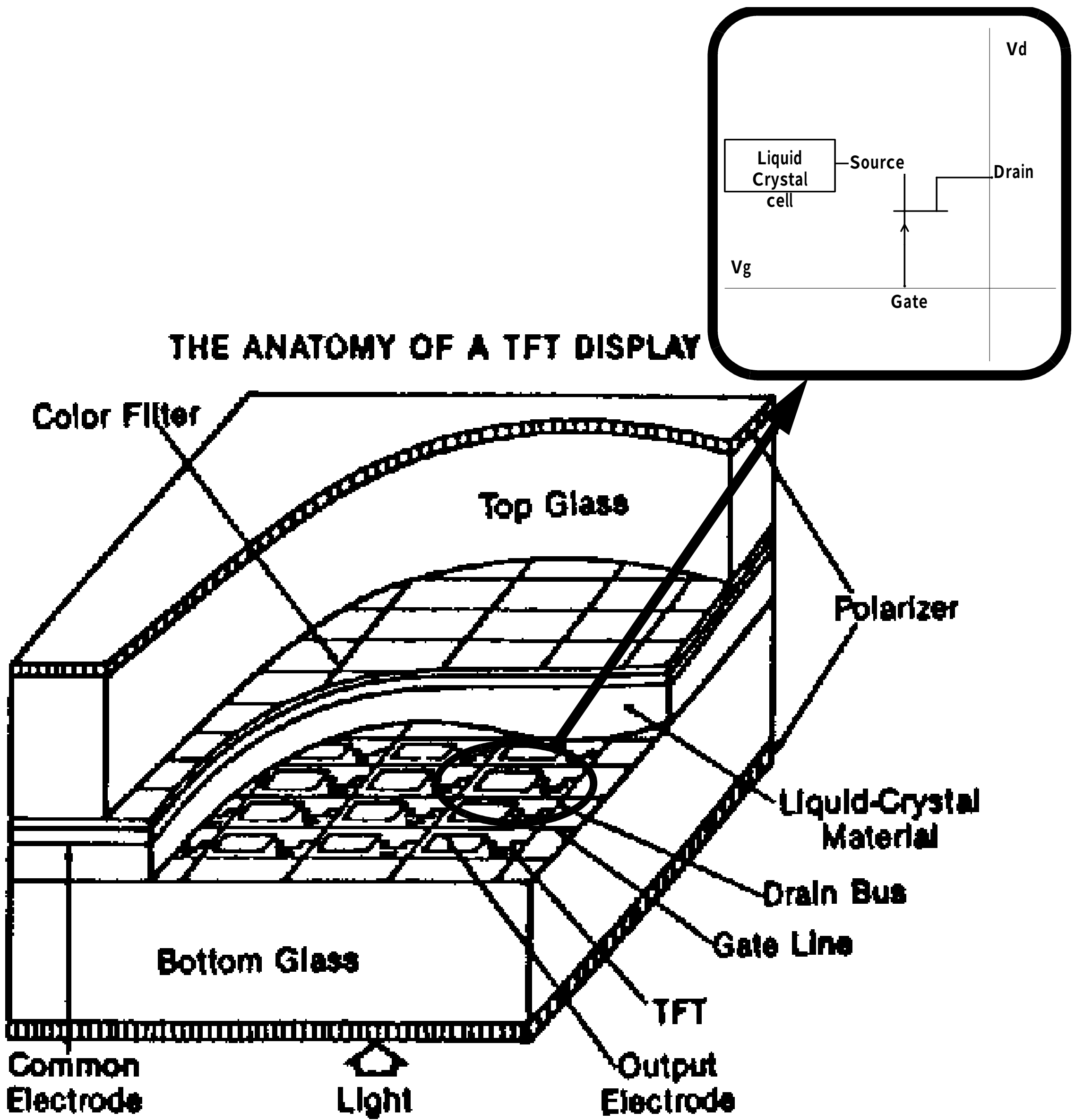


Fig. 3.2 Anatomy of a TFT-LCD.

3.3 Modeling of One Pixel

3.3.1 Accuracy verifications for each device model

In order to simulate TFT-LCD pixels accurately, the a-Si TFT model must be able to support most of the known TFT process devices. For time domain simulations, it is especially important that the model represent the following characteristics. For clear understanding the leading head alphabet of each state corresponds to the state marked in Fig. 3.3.

A. The charging state which is driven by the on-current of an a-Si: H TFT

A liquid crystal cell is charged by the source current of a TFT which is directly connected. Therefore, the source current characteristic of the TFT is dominant to analyze LC performance.

B. The holding state which is affected by the off-current of an a-Si: H TFT

The off-current is caused by optical and drain-to-gate channel leakage current. Since the gate charge is decreased by the off-current flow, the voltage level goes down.

C. The voltage drop characteristic which is controlled by the gate-to-source capacitance of an a-Si: H TFT and LC capacitance

To charge the capacitance some amount of current flows from gate to the capacitance. During the time frame pulse voltage drops because of the capacitance.

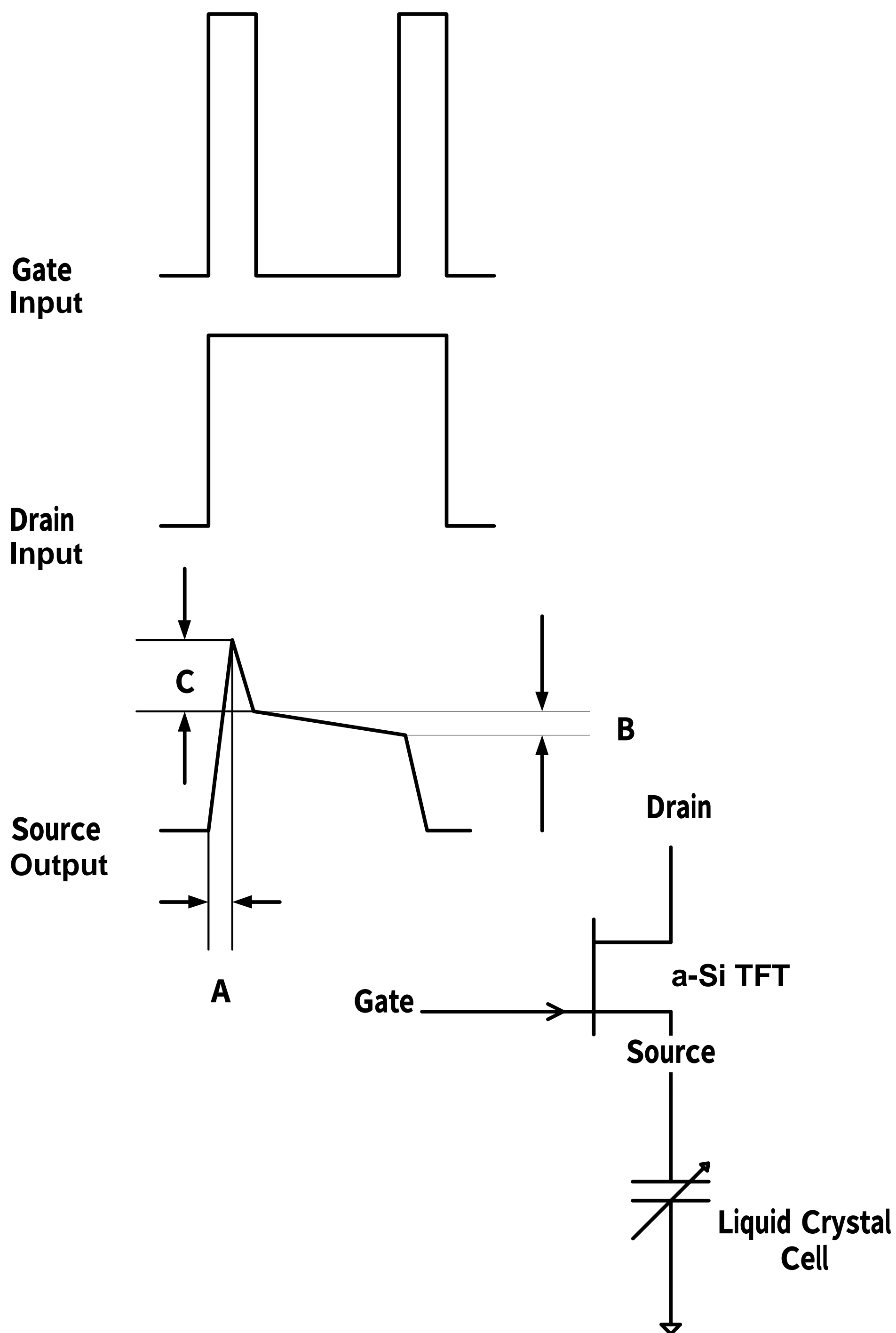


Fig. 3.3 Three states of a simplified TFT-LCD pixel which is biased by pulse signals.

A TFT-LCD pixel can be modeled by referring Fig. 3.4 which is typical one pixel structure of a TFT-LCD.

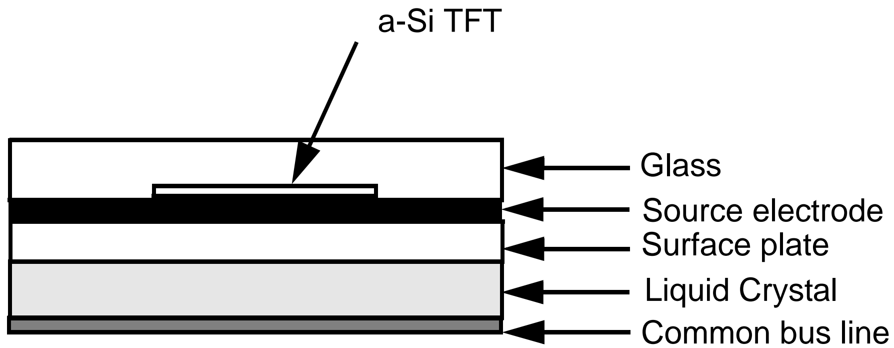


Fig. 3.4 Typical one pixel structure of a TFT-LCD.

An equivalent circuit of a typical TFT-LCD pixel is shown in Fig. 3.5.

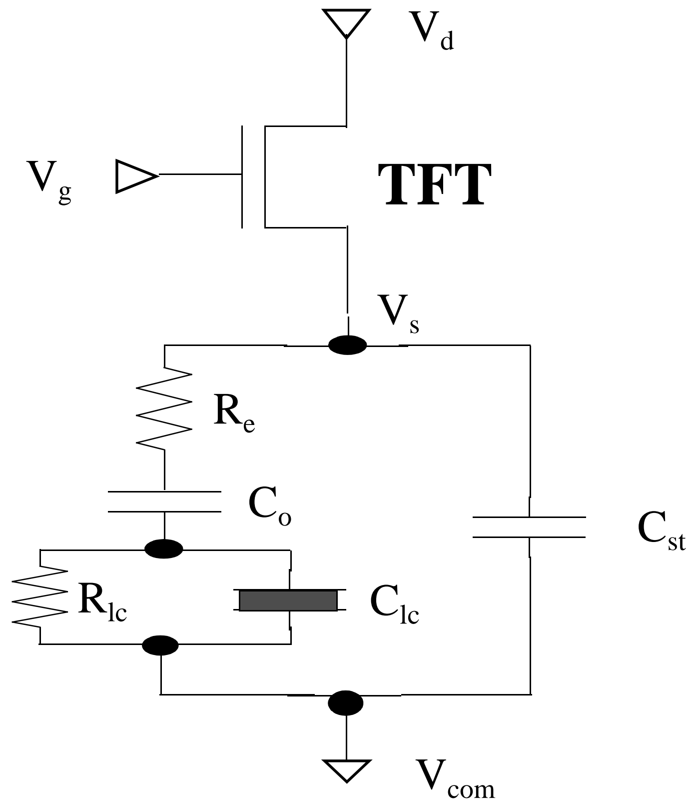


Fig. 3.5 Equivalent circuit of a TFT-LCD cell. Here R_e = 1.28 KΩ, C_o = 317 fF, R_{lc} = 10 GΩ, and C_{st} = 1.06 pF.

The Liquid Crystal Cell consists of R_e (electrode resistance), C_o (surface plate capacitance), R_{lc} (liquid crystal resistance), and C_{lc} (liquid crystal capacitance). C_{st} (storage capacitance) is formed at the source terminal of the TFT. The scanning pulse signal (V_G) is supplied at the gate terminal of the TFT device. The video voltage signal (V_D) is supplied at the drain terminal of the TFT.

Fig. 2.16 (a), (c), (e), and (g) show the model accuracy of the on-current characteristics. Fig. 2.16 (d), (f), and (h) plots I_{DS} *vs.* V_{GS} for the a-Si: H TFT on a semilogarithmic scale using the same measured and simulated data. The sub-threshold and off-region current characteristics are clearly shown in Fig. 2.16 (h). The drain bias dependency of the off-leakage current is demonstrated in this plot. The gate bias dependency of the off-leakage current is sufficient to simulate the holding state behavior.

The gate-to-source capacitance of an a-Si: H TFT was characterized as shown in Fig. 2.19. No discontinuity is observed because the capacitance model equations are continuous from below to over the threshold voltage.

Also, Fig. 2.20 is the comparison between measured and simulated data whose parameters are extracted from the measured data of a TN type liquid crystal cell discussed in chapter 2.

The result of the C_{lc} extraction is plotted in Fig. 2.20. It shows good agreement between measured and simulated data. Fig. 2.19 and Fig. 2.20 are good indicators that the model will be useful for simulating the voltage drop characteristic.

All of these model parameters used here are shown in Table 3.1 which is the same as Table 2.2 for easy understanding.

Table 3.1 Model parameter list of an a-Si:H TFT and LC cap models.

(a) **a-Si TFT model**	(b) LC cap model
L = 11 μm	L = 152 μm
W = 41 μm	W = 148 μm
μ_O = 0.450 cm^2/Vs	D = 10.02 μm
V_{TO} = 1.699 V	δ = 51.0 mm^2/s
ϕ = 0.620 V	γ = 51.2 ms/mm^2
N_{FS} = 1.925x10^{21} cm^{-2}	D_{TIME} = 100 ms
V_{sat} = 2,783 m/s	V_C = 1.887 V
θ = 17.8 mV^{-1}	ε_{PL} = 3.1
η = 410.8μ	
T_1 = 300 nm	
T_2 = 0	
ε_1 = 3.9	
ε_2 = 0	
g_o = 9.728x10^{-15} Ω^{-1}	
T_{REF} = 1.5	
C_{GSO} = 52.03 fF	
C_{GDO} = 42.21 fF	
C_{SC} = 158.8 μF/m	
R_D = 8,030 Ω	
R_S = 8,030 Ω	
f = 100 KHz	
D_{EFF} = 1.968	
τ = 10.7 ns	
f_{EFF} = 0.302	
ν = 0.008	
ψ = 0.2	
V_x = 0.033 V	
t_{vst} = 100 ms	
T_{NOM} = 300.15 K	

3.4 Driving voltage timing measurement and simulation of a TFT-LCD

Fig. 3.9 shows the supplied V_G and V_D waveforms and the simulated V_s waveform of the TFT-LCD pixel using the new TFT and LC capacitance models. The measured and simulated V_s waveforms are shown in Fig. 3.9. R_e, C_o, and C_{st} were optimized using the measured data. Geometry of the test devices and the parameters used for simulation are listed in Table 1. Theoretically, V_s must be driven by half of V_{D_HIGH} minus V_{D_LOW}. However, the Vs waveform has a voltage drop in each cycle (Fig. 3.9) because the C_{lc} charging time delay and the voltage drop caused by C_{GS}, become dominant. Here, V_{D_HIGH} and V_{D_LOW} are the maximum and minimum voltage of V_D, respectively. The voltage drop characteristic is tested using two different C_{GSO} values in Fig. 3.11.

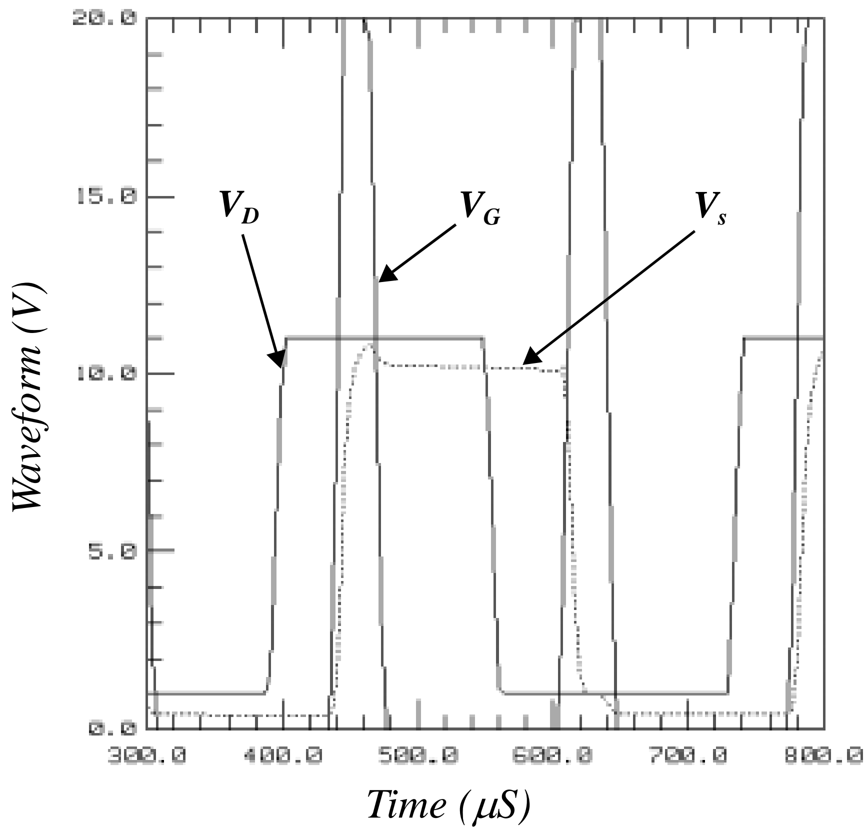


Fig. 3.9 A TFT-LCD cell transient characteristic. The input signals are drawn with solid (-) line and the output signal is drawn with dotted (- - -) line.

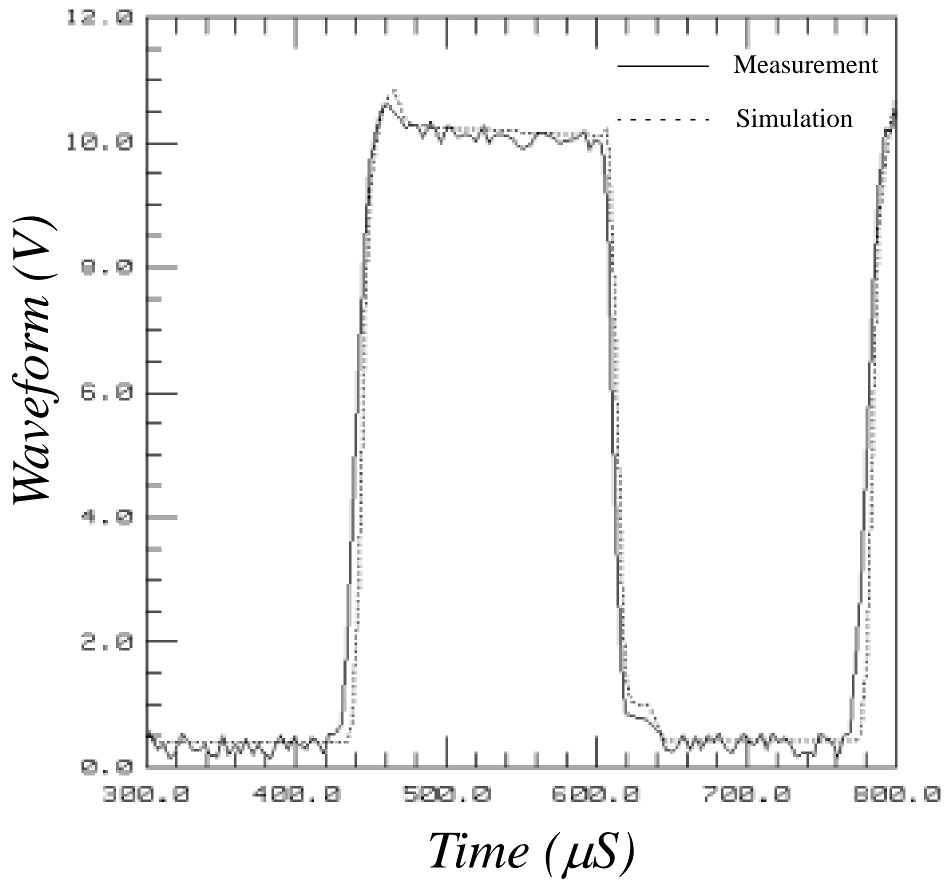


Fig. 3.10 Measured (-) and simulated (- - -) Vs waveform of a typical TFT-LCD cell which is shown in Fig. 3.5.

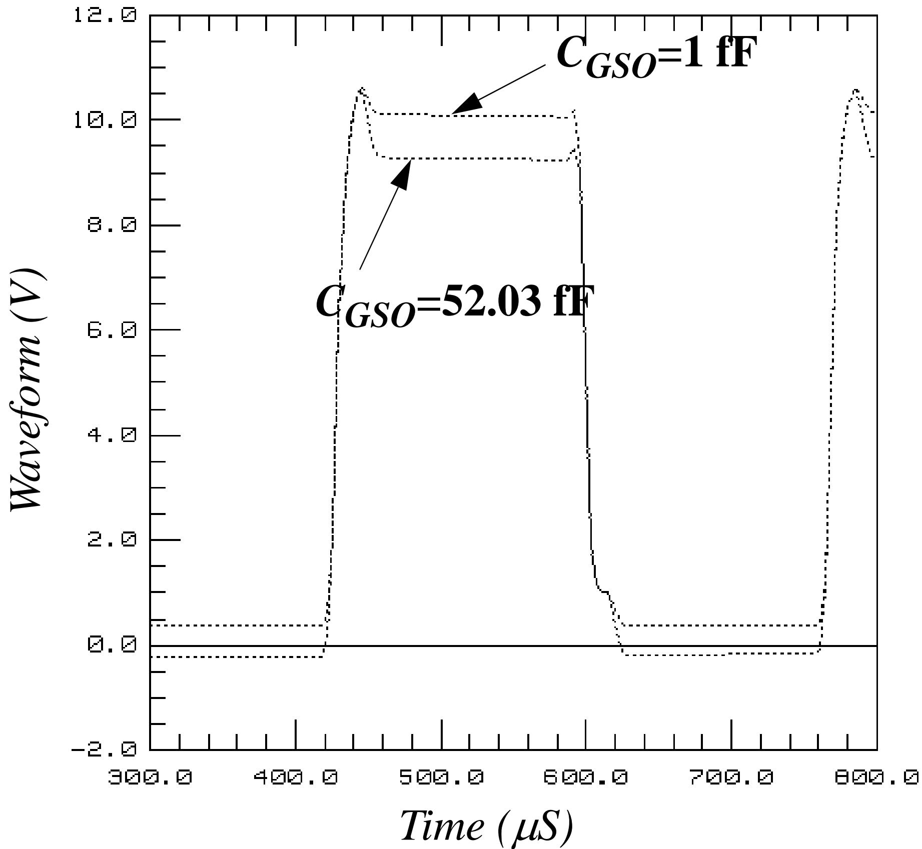


Fig. 3.11 The effect of the gate-to-source overlap capacitance on a TFT-LCD cell. The simulation is performed under the same condition as Fig. 3.10.

If the voltage is defined as ΔV, it is calculated by

$$\Delta V = C_{GS} \cdot \frac{V_{GHIGH} - V_{GLOW}}{C_{GS} + C_{total}} \tag{3.1}$$

$$C_{total} = C_{st} + \frac{C_o \cdot C_{lc}}{C_{lc} + C_o} \tag{3.2}$$

where V_{G_HIGH} and V_{G_LOW} are the maximum and minimum voltage of V_G, respectively.

The other important state of LCD dynamic behavior is the holding state which is dominated by the TFT reverse leakage current. When the a-Si: H TFT is in a holding state, the potential drop is caused by the leakage current of the TFT itself. In this case, the amount of leakage current is given by

$$I_{leak} = C_{total} \cdot \frac{dV}{dt} \tag{3.3}$$

By using (3.3) and the transient simulation result, the dynamic off-current can be calculated.

Using the TFT-LCD timing simulation results, V_{rms} (rms voltage of V_s) can also be calculated from the V_s signal, as shown in (3.4) [13].

$$V_{rms} = \sqrt{\frac{1}{t_F}\int_0^{t_F}(V_s - V_{COM})^2 dt} \tag{3.4}$$

The optical characteristics are controlled by V_{rms}, which is the voltage supplied to the liquid crystals. An accurate value of V_{rms} is necessary to analyze the optical performance of the FPD. The optical characteristics are usually defined by transmittance versus V_{rms} curves whose example is shown in Fig. 3.12. Other optical parameters such as optical threshold voltage and contrast ratio can also be calculated using V_{rms}. As described above, the simulation results are directly applicable to TFT-LCD design evaluation.

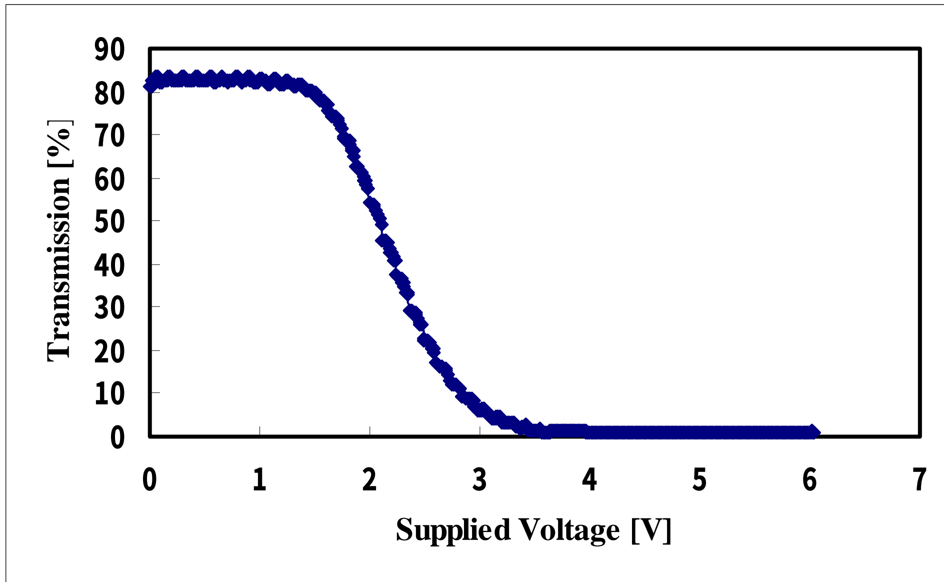


Fig. 3.12 A transmission curve of twisted nematic type liquid crystals.

3.5 TFT-LCD Panel Simulations using a Pixel Macro Modeling Method

The equivalent circuit of a TFT-LCD could be formed without any difficulty as shown in Fig. 3.5. However, the SPICE simulation of 640 x 480 pixels LCD, which is shown in Fig. 3.16, took about 40 minutes on a HP 720 workstation. What's worse, a little more pixels cause the size to reach the simulation limit. To reduce the simulation time, a macro model is discussed as follows.

3.5.1 Scaling Theory of Model Parameters

The macro model is based on the scaling theory which is used for modeling a number of large pixel modules. Therefore, TFT-LCD scaling should be discussed before implementing the LCD panel macro models. The scaling of the liquid crystal (LC) cells has to be considered in addition to the TFT device scaling in TFT-LCD. The items to be potentially scaled are the TFT's, the LC cells, and the pixel capacitance. The common assumption in dealing with these items is that the electrical field is kept constant regardless of scaling. This is the same assumption as for MOS LSI's [28].

We first discuss with the scaling of LC cells. As described in section 2.4, the LC capacitance is calculated from the permittivity ε_{ps} and the geometry of LC cells as

$$C_{lc} = \frac{\varepsilon_0 \cdot \varepsilon_{ps} \cdot L_l \cdot W_l}{D} \quad (3.5)$$

where length of a liquid crystal cell, L_l and width of a liquid crystal cell, W_l are used to calculate the total area of LC cells, D is the thickness of the LC cell (cell gap), and

$$\varepsilon_{ps} = \varepsilon_{pl} + \delta \cdot \gamma \cdot e^{D_{time}} \cdot \sqrt{\frac{V}{V_C} - 1.0} \quad (3.6)$$

Where ε_{pl} is the dielectric permittivity base value, δ is the viscosity of LC's, γ is a fitting parameter, D_{time} is the delay time of charge, and V_c is the threshold voltage. As shown in (3.5) and (3.6), the V_c is solely determined by the physical constants of the LC. Therefore, V_c cannot be controlled by changing the physical dimensions such as D. If the V_c is not scaled, then the relevant voltages are not scaled either. This makes an assumption that the TFT related voltages, which are drain voltage V_D, gate voltage V_G, TFT threshold voltage V_{TH}, and the signal voltage V_{sig}, are all independent. Also, channel length L and the film thickness T_{fm} of the TFT are not scaled because of the framework of a constant field condition. However, channel width W is scaled to the number of pixels N.

We next discuss the scaling of drain current and gate capacitance. The drain current model equation [23] is written as

$$I_{DS} = \mu_{eff} \cdot C_{fm} \cdot \frac{W}{L}\left[(V_{GS} - V_{TO} - \eta \cdot V_{DS})V_{DS} - \frac{V_{DS}^2}{2}\right] \tag{3.7}$$

where μ_{eff} is the field effect mobility, C_{fm} is the TFT insulator film capacitance, and η is a fitting parameter to express static feedback effect. Since the TFT-LCD panels operate only in the linear region, (3.7) is sufficient for analyzing FPD operation. I_{DS} is scaled to N through W.

For gate-to-source capacitance C_{GS} scaling we have to treat two separated regions which are overlap and intrinsic capacitance. As a reference, the equivalent circuit of the a-Si TFT model is shown in Fig. 2.18 of Chapter 2.

The overlap gate-to-source capacitance C_{GSO} is constant and is scaled by the area of overlap insulator film to N^2. The intrinsic gate-to-source capacitance C_{GS} is a function of V_{DS}, V_{GS}, and frequency [23], which is conceptually expressed as

$$C_{GSI} = C_{MIS} \cdot f(V_{DS}, V_{GS}, frequency) \tag{3.8}$$

$$C_{GDI} = C_{MIS} \cdot f(V_{DS}, V_{GS}, frequency) \tag{3.9}$$

where C_{MIS} is the metal-insulator-semiconductor capacitance. C_{MIS} is given by

$$C_{MIS} = \frac{C_{fm} \cdot C_{SC}}{C_{SC} + C_{fm}} \tag{3.10}$$

here C_{sc} is the space charge capacitance. By analyzing (3.8) and (3.10), it is found that C_{GSI} is scaled only by C_{MIS} to N^2. The total pixel capacitance C_{pix} is represented by

$$C_{pix} = C_{st} + \frac{C_o \cdot C_{lc}}{C_{lc} + C_o} + C_{cs} \tag{3.11}$$

where C_{st} is the storage capacitance and C_o is the surface plate capacitance. As discussed above with (3.5), ε_{ps} and D are not scaled. Only L_l and W_l are possibly scaled. However from design rule, they are not simply multiplied by the fixed constant. Therefore, C_{lc} is not scaled in this approach. According to the equivalent circuit of a TFT-LCD cell in Fig. 2.18, C_o and C_{st} are scaled to N. The final point related to the scaling parameters is resistance. R_{lc} is not scaled due to the same reason as C_{lc}. Electrode resistance R_e, drain resistance R_D, and source resistance R_s are scaled to $1/N$ because of the series connection in a FPD.

3.5.2 Implement of pixel macro models

We assumed an 640 x 480 stages LCD panel for our simulation. As shown in Fig. 2.18, the equivalent circuit of an LCD panel consists of 9 pixels. Since the macro model is used to predict output source signals at the first and the last pixels, all other pixels can be lumped to some large dummy pixels. The four pixels called Pixel1, which are located at each corner, are used to represent a cell for monitoring source signals. As shown in Fig. 3.14, the equivalent

circuit of Pixel1 is accurately modeled by a pixel model, which consists of the a-Si TFT (whose equivalent circuit is shown in Fig. 2.18) and the HP LC models. The other 5 pixels called Pixel2, Pixel3, and Pixel4 are dummy pixels, which act as 638 x 1, 1 x 478, and 38 x 478 pixels, respectively. Since these pixels operate as loads, every pixel also uses the same model, which is shown in Fig. 3.14, and the parameters that are discussed in 3.5.1 are scaled by the number of connected pixels in parallel. For each pixel module the scaling factor is listed in Table 3.2.

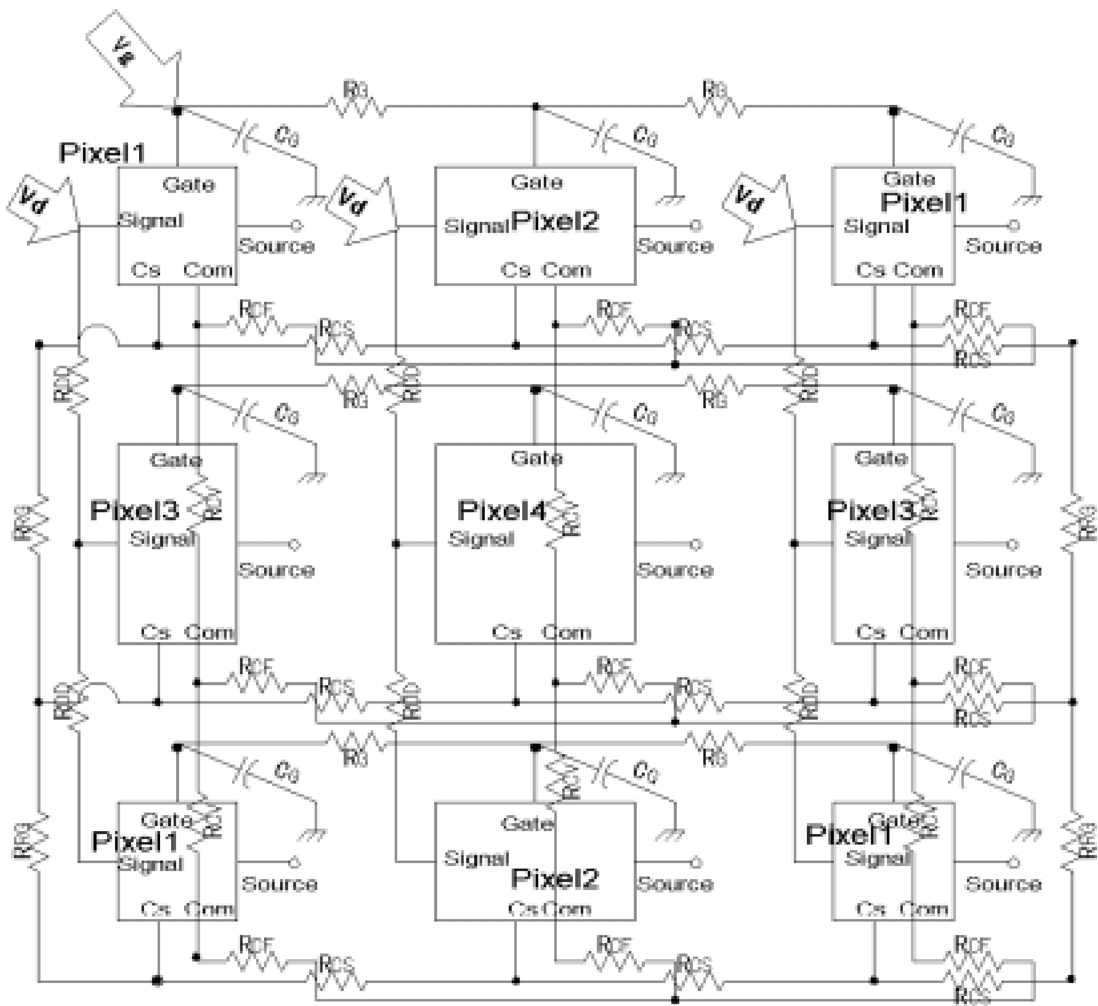


Fig. 3.13 Equivalent circuit of an LCD panel for simulation.

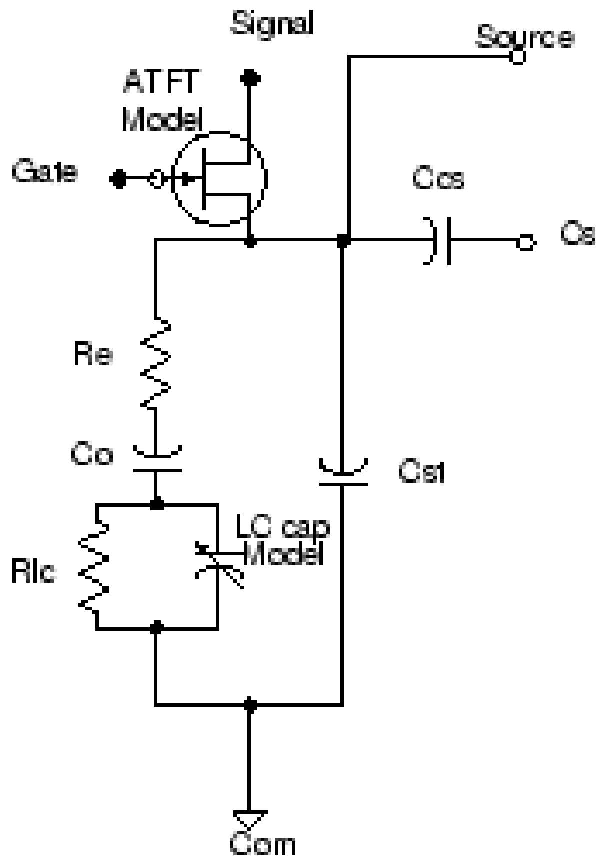


Fig. 3.14 Modified equivalent circuit of a TFT-LCD cell.

Table 3.2 LCD scaling factor. Other parameters should not be scaled. Here, m is the number of columns and n is the number of rows.

Parameter Name	Scaling Factor			
	Pixel 1	Pixel 2	Pixel 3	Pixel 4
W	1	m	1	m
C_{GSO}	1	m^2	1	m^2
C_{GDO}	1	m^2	1	m^2
C_{MIS}	1	m^2	1	m^2
C_o	1	m	n	$m \times n$
C_{st}	1	m	n	$m \times n$
C_{cs}	1	m	n	$m \times n$
R_e	1	1	$1/n$	$1/n$
R_S	1	1	$1/n$	$1/n$
R_D	1	1	$1/n$	$1/n$

All interconnects are modeled mainly with busline resistance except for gate bus lines. Because the gate signal delay becomes the dominant effect as the size of a display panel increases, gate busline can be modeled by using distributed RC [26]. Gate delay, t_d, can be estimated as [28]:

$$t_d \cong \frac{C_b \cdot R_b \cdot n_h^2}{2} \quad (3.12)$$

Where C_b is the busline capacitance per pixel, R_b is the busline resistance per pixel, and n_h is the number of pixels in the horizontal direction of the panel. C_b and R_b are:

$$C_b = 3(C_x + C_{gs} + C_{gd} + C_G) \quad (3.13)$$

$$R_b = \frac{\rho \cdot L_h}{W_b \cdot T_b} \qquad (3.14)$$

where C_x is the capacitance of the crossover between the gate busline and the data busline, ρ is the specific resistivity of the busline metallization, L_h is the horizontal length of the pixel, W_b is the width of the busline, and T_b is the film thickness of the gate metallization. R_G is included in R_b. C_{gs} and C_{gd} are gate-to-source and gate-to-drain capacitance of an a-Si TFT, respectively. Since we used a simplified lumped sum RC model to reduce the simulation time though a more accurate model can be easily incorporated in our analysis method, C_x and R_b are employed for the gate busline modeling.

3.6 Parameter Extraction and Simulation

The model parameters for the a-Si:H TFT and the LC capacitance were extracted using the extraction and optimization functions of the HP IC-CAP software. The extraction employs a twisted nematic (TN) type LCD pixel based on a typical inverted staggered a-Si:H TFT with a SiNx gate insulator film. dc voltage source/ low current meter, and capacitance meter were used to measure I_d-V_{gs}, I_d-V_{ds}, C_{gs}-V_{gs}, and C_{gd}-V_{gs} data. Fig. 3.10 shows a dynamic measurement (solid line) and simulation (dotted line) plot of a pixel which is shown in Fig. 3.5. In order to make a condition to monitor one frame signal, every terminal is biased with respective voltage sources. An input pulse voltage V_g of 14 to 11V, cycles of 48.67ms, and width of 60μs were applied to a Gate at the upper-left corner device (a blank arrow is marked in Fig. 3.13). Gate voltage of the other two left-most devices was set to -14V. An input pulse voltage V_d of -3.0 to 3.5V, cycles of 97.34ms, and width of 48.67ms (one frame signal) was applied to a Signal terminal at the top three devices in common (three blank arrows are marked in Fig. 3.13). Com terminals of four corner devices were set to -1V. V_s was monitored at Source terminal of the bottom-right corner device. V_g, V_d, and V_s waveforms are shown in Fig. 3.15 in order to understand the timing of pulse signals.

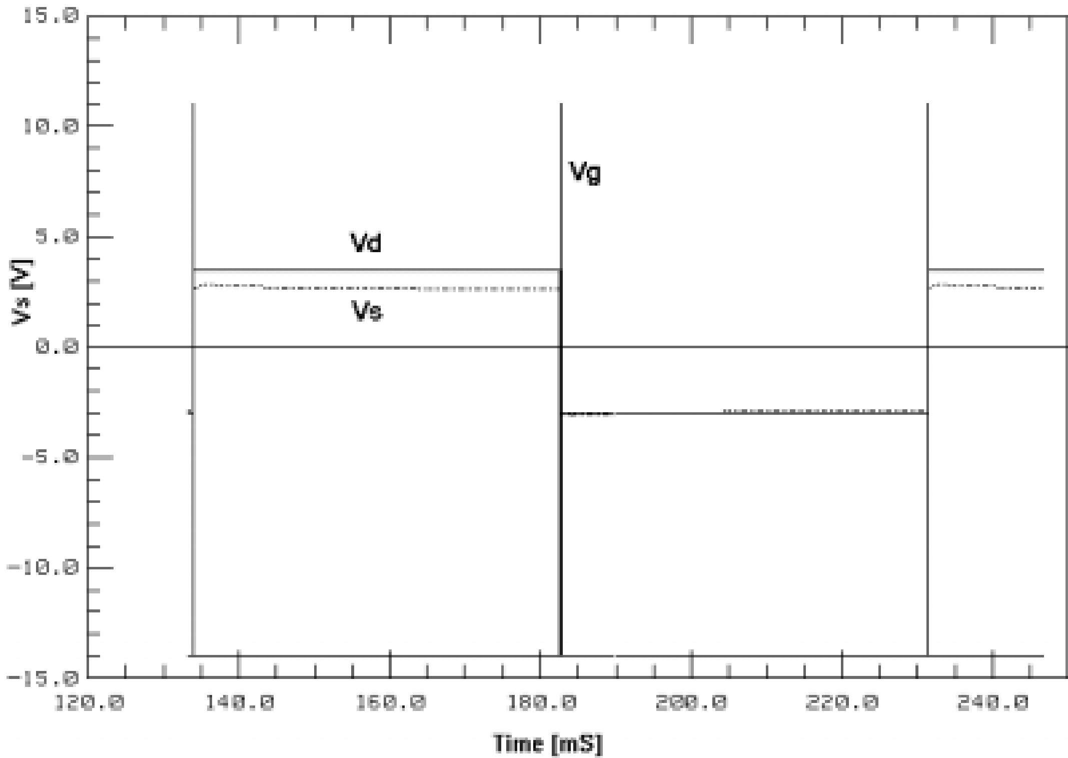


Fig. 3.15 Input and output pulse waveform of 640 x 480 TFT-LCD panel.

Using the extracted model parameters of a pixel and the macro model in Fig. 3.13, the LCD panel simulation shown in Fig. 3.16 was obtained. A small inset is a zoom graph of a circle, which shows the voltage drop (δV_H) due to gate-to-source, LC, and gate line capacitance. The δV_H is calculated by

$$\delta V_H = C_{gs} \cdot \frac{V_{gh} - V_{gl}}{C_{gs} + C_{pix}} \quad (3.15)$$

Here, V_{gh} and V_{gl} are the maximum and minimum voltage of V_g, respectively. The RMS voltage of V_s waveform (V_{rms}) should be expressed as (3.16) if charging and storage characteristics are sufficient [26].

$$V_{rms} = V_{sig} + \frac{\delta V_L - \delta V_H}{2} \quad (3.16)$$

However, the simulated V_{rms} of 2.77V was smaller than the calculated value from (3.16) of 3.10V, which mainly by load of other pixels and parasitic resistance. Since the equivalent circuit simulation, Fig. 3.16, is very close to Fig. 3.16, the macro model can be used for other size of TFT-LCD simulations.

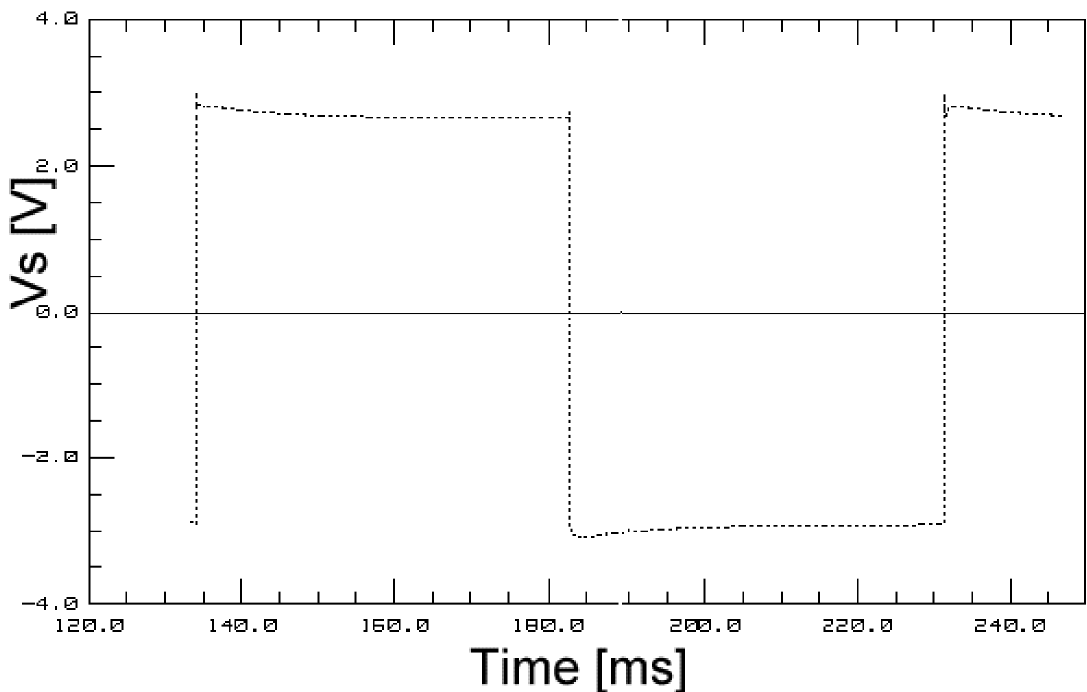


Fig. 3.16 A 640 x 480 pixels TFT-LCD panel simulation using conventional equivalent circuit, which includes all components.

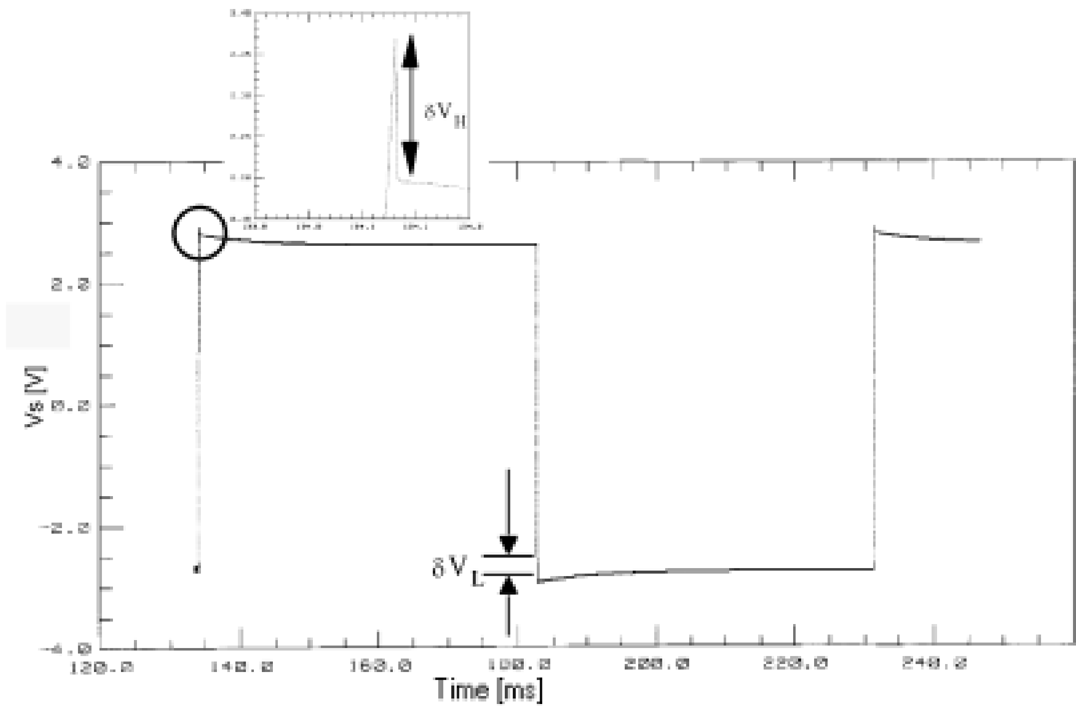


Fig. 3.17 A 640 x 480 TFT-LCD panel simulation using the 9 pixel macro models.

Fig. 3.18 shows the comparison plot between measured cell output signal and macro model based simulation.

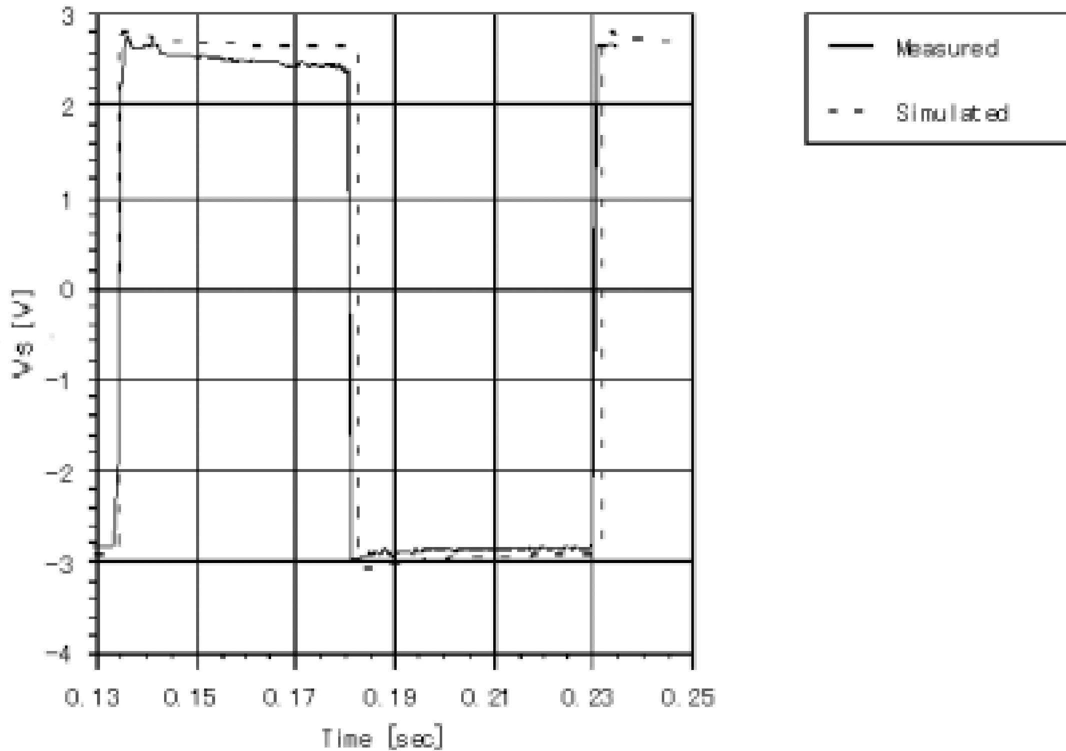


Fig. 3.18 A Measurement and simulation comparison of a 640 x 480 TFT-LCD panel. Simulation was performed by using the 9 pixel macro models.

Since the number of macro model based dummy cells were five, the voltage level of the simulated signal is slightly higher than the measured signal. As we tested to increase the number of total pixels from 9 (3 x 3) to 36 (6 x 6) by using the same method as shown above, we found that the simulation accuracies had been improved at 16 (4 x 4) and 25 (5 x 5) pixels panels. The simulation accuracy of 36 (6 x 6) pixels macro model panel was almost the same as 25 pixels' whose simulation result is shown in Fig. 3.19. The simulation error against the measured data was 1.1% r.m.s. whereas the 9 pixel

macro models' were 3.4% rms. However, the simulation speed was ten times slower than the 9 pixel macro models'.

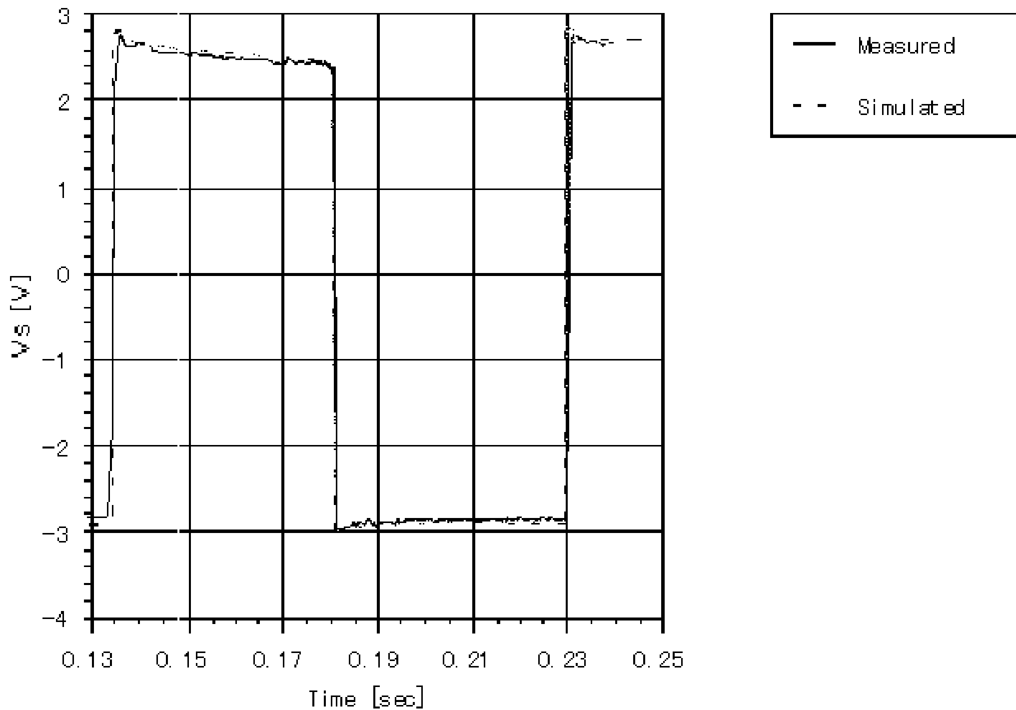


Fig. 3.19 A Measurement and simulation comparison of a 640 x 480 TFT-LCD panel. Simulation was performed by using the 25 pixel macro models.

The simulation speed and the accuracies at each pixel macro models are compared and plotted in Fig. 3.20. If the total number of pixels will be further increased in 1024 x 768 and larger display panels, the simulation will be drastically slower than the 9 pixel macro models'.

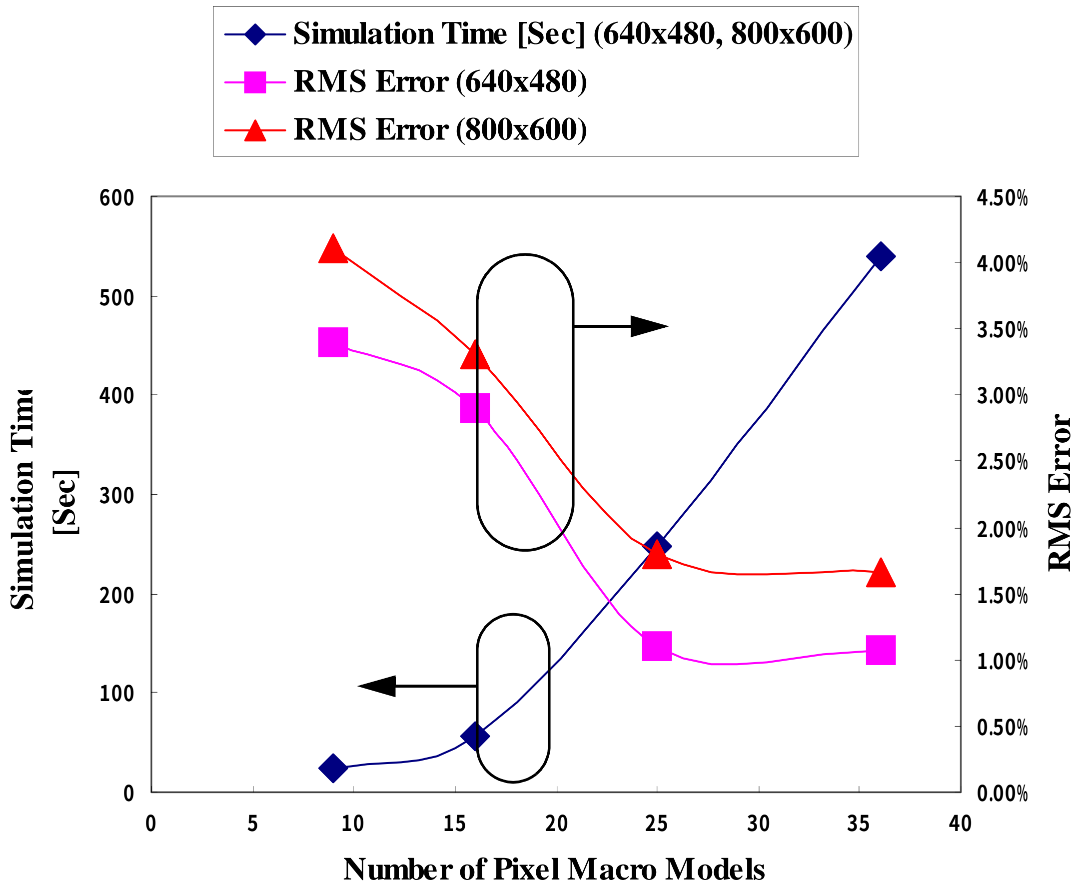


Fig. 3.20 Optimum number of pixel macro models.

In order to analyze dependencies of the number of pixels and interconnect parasitic, other sizes than 640 x 480 TFT-LCD have been simulated in the same manner. Here the 9 pixel macro models are adopted for macro model simulations in Fig. 3.21. The total simulation time of each example was completed in 30 seconds (with a HP712 workstation) regardless of the panel

sizes. Fig. 3.21 is a simulated V_{rms} plot at each number of pixels which is followed by existing display technologies.

Also, measured and simulated (conventional method) V_{rms} of 640 x 480 and 800 x 600 are plotted to check the macro model accuracy. Here, we could not obtain other size of LCD panels for the measurement. Because of the SPICE simulation limit, conventional method could not simulate 1024 x 768 and larger LCD panels. The plot shows the logarithmic dependency between V_s and the number of pixels.

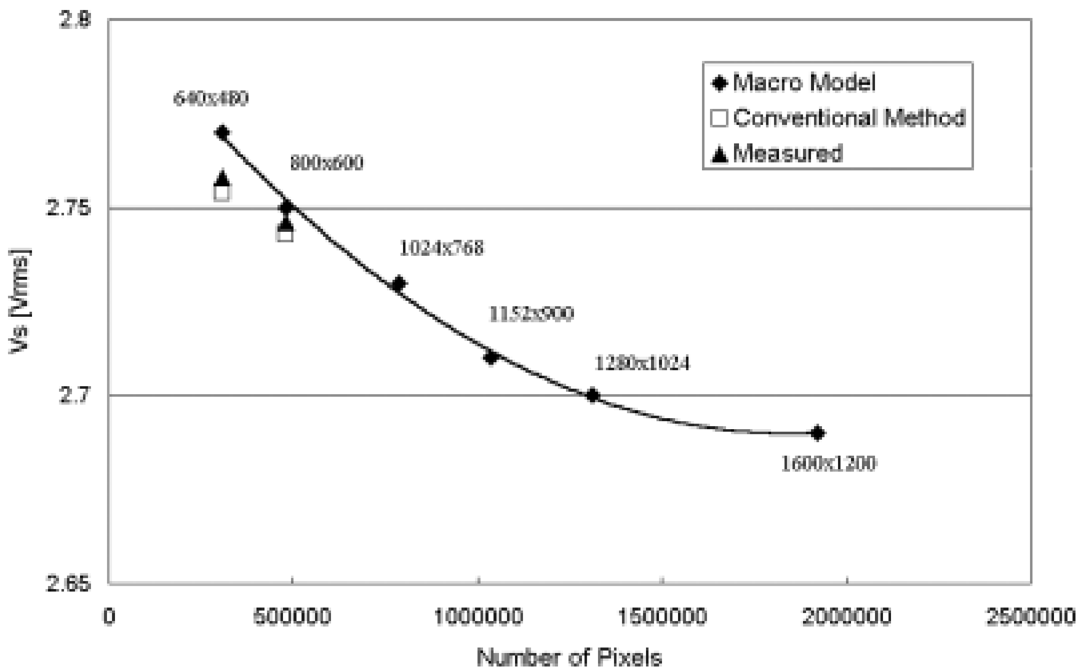


Fig. 3.21 Source effective voltages at each display size of TFT-LCD's.

As discussed above, existing large TFT-LCD panel could be simulated by using only nine pixel macro models accurately. However, in some cases more accurate simulations are needed for predicting holding voltages of LCD's. We tested to increase the total number of macro models in a 640 x 480 TFT-LCD panel. The accuracy was improved from 3.4% rms to 1.1% rms in 25 pixel macro models although the simulation time of 25 pixel macro models was ten times slower than 9 pixel macro models'. There is a trade-off between the simulation speed and accuracy.

3.7 Conclusions

As an instance of large scale circuit modeling method to reduce the simulation time, we presented an approach to implement macro models which accurately predict the circuit performance without using the real equivalent circuit topology.

The target circuit to apply this method was TFT-LCD's which were widely used on laptop computers, personal digital assistance, and so on. The circuit macro models were based on device scaling theories of TFT's and LC's, and busline interconnect parasitics. The device models to configure the circuit macro models were the a-Si TFT and the LC cap models that were discussed in chapter 2. Every model parameter of the a-Si TFT and the LC cap models was accurately extracted from measured data of an inverted stagger type a-Si:H TFT and TN type liquid crystals. The interconnect parasitics were initially calculated with design variables and then optimized using a commercial modeling software program. A 640 x 480 pixels and a 800 x 600 pixels FPD panels had been used for measuring and simulating the transient characteristic. The results showed excellent agreements between measured and simulated data especially for the 25 pixel macro models. The simulated waveform demonstrated critical characteristic of TFT-LCDs' such as voltage drop of holding states and effective voltage reduction. Simulation experiments for larger display panels had been successfully performed in order to

observe the effective driving voltages of liquid crystals. The simulation time for 9 pixel macro models was less than 30 seconds on an HP 712 workstation regardless of the display sizes.

This simulation method and the macro models can be effective tools for reducing simulation time of TFT-LCD panels with maintaining the reasonable accuracies.

Chapter 4 Flicker Noise Modeling

Introduction

In order to design oscillators and switches phase noise characteristic is the key to obtain high quality frequency spectrums. Since the phase noise is directly affected by the 1/f noise of transistors in the circuit, 1/f noise measurement and modeling are important. So far, bipolar transistors were used for designing oscillators because their flicker noise level is much lower than MOSFET's'. However, in some applications MOSFET's are actively used because of their advantages of process cost and low power consumption. One of these applications is low speed switches, whose phase noise appeared to be jitters of pulse signals. Even in the oscillator applications, MOSFET's are sometimes used in voltage-controlled oscillators of portable handy phones. Therefore, flicker noise characterization of MOSFET's and TFT's are very important to estimate and simulate phase noise of analog circuits. Moreover, 1/f noise characteristic is adopted for process monitoring and analysis since it can be measured in case of thin oxide damage whereas capacitance measurement cannot be made.

So far, some authors [30]-[32] published the 1/f noise analysis and modeling of MOSFET's. Others [35] mentioned the measurement and the extraction techniques of BJT's using 1/f noise corner frequencies. The techniques cannot be applied to MOSFET 1/f noise characterization because the noise corner frequency of sub-micron devices is usually higher than the measurement frequency range. For the bias dependencies simulation accuracy of these models is not so high enough to use it for analog circuit design. The other remained problem is that geometry dependencies of drain 1/f noise characteristic in MOSFET's had not been well discussed, yet. Especially, channel width dependency of drain 1/f current noise was poorly

described in any textbooks and papers [32], [36]-[41]. No paper was published on 1/f noise modeling with TFT's.

This thesis describes 1/f noise measurement, frequency and bias dependent flicker noise model, and noise parameter extraction method of MOSFET's and TFT's. Also, for MOSFET's geometry dependencies of drain current 1/f noise are analyzed and modeled. In this thesis we will focus only on single gate stripe MOSFET's.

In this chapter we first describe our 1/f noise measurement concept and configuration. Then, drain 1/f noise current model of a-Si TFT's are developed based on the dc and capacitance model which was mentioned in chapter 2. Next, drain 1/f noise current model of MOSFET and its parameter extraction method are described. Finally, the MOSFET model is verified by using a simple negative resistance RF oscillator as a test vehicle of circuit module.

4.1 Flicker Noise Measurement

To develop an accurate noise model for any devices measurement is the key element for verifying the model. We have designed a flicker noise measurement system whose block diagram is shown in Fig. 4.1.

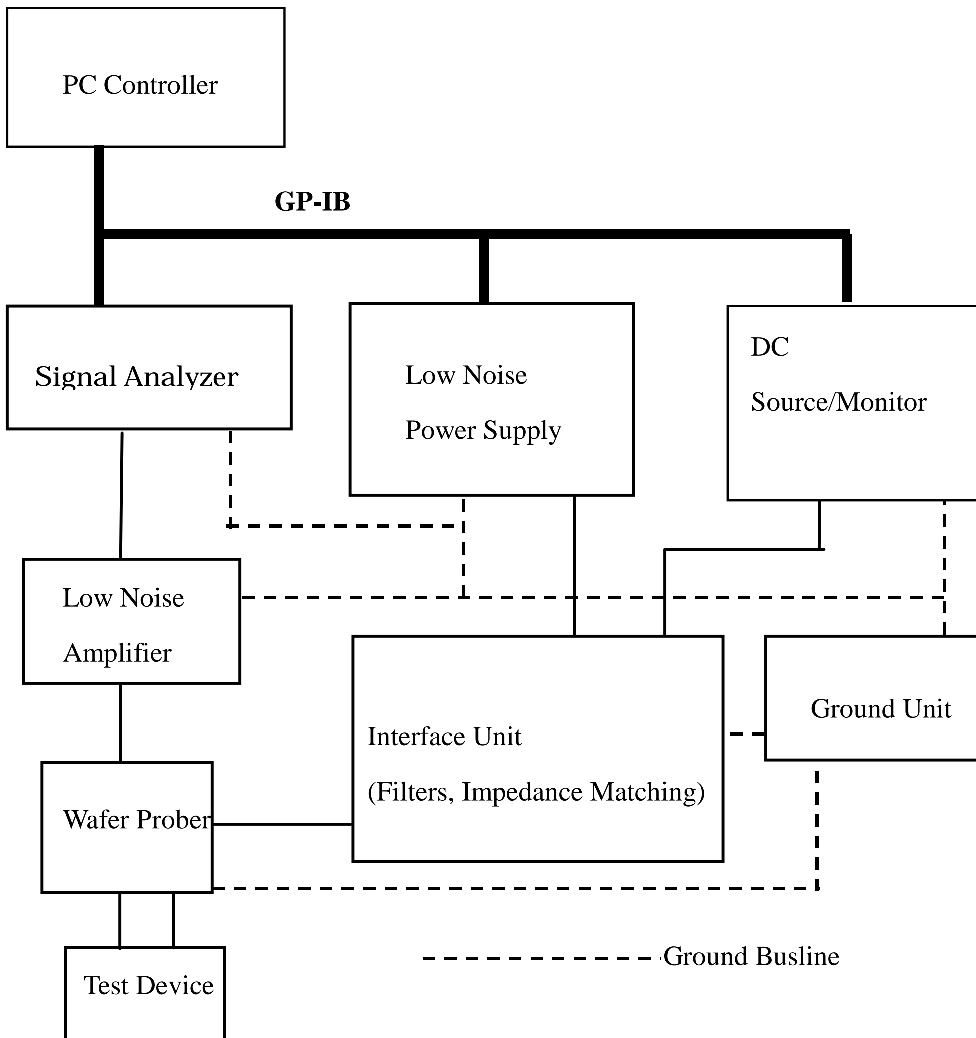


Fig. 4.1 The block diagram of the 1/f noise measurement system.

The low noise power supply in Fig. 4.1 is used to apply voltage biases through the interface unit, which will be discussed later. The signal analyzer is to measure output noise voltage spectrums with very high sensitivity and high dynamic range, therefore, ordinal FFT analyzers are not sufficient for this purpose. We use an Agilent Technologies' Vector Signal Analyzer (Agilent 89441A). Since it is normally for measuring modulated vector signals, it has more than 100 dB dynamic range and higher sensitivity (the specifications vary with the frequency ranges) than ordinal FFT analyzers'. The low noise amplifier is to amplify the measured noise voltages from a DUT. The DC source/monitor unit is used to measure current-voltage characteristic to find out the amount of input current bias to be applied since the target devices (a-Si TFT's and MOSFET's) to be measured are voltage controlled. The ground unit is designed to keep ground voltage level of every instrument in common.

The core part of this 1/f noise measurement system is interface unit, which includes impedance matching and filtering circuits. The filter circuit is developed to defuse high frequency noises. Here, we designed a low pass filter whose cut off frequency was 10 MHz. The impedance matching circuit is carefully designed as shown in Fig. 4.2.

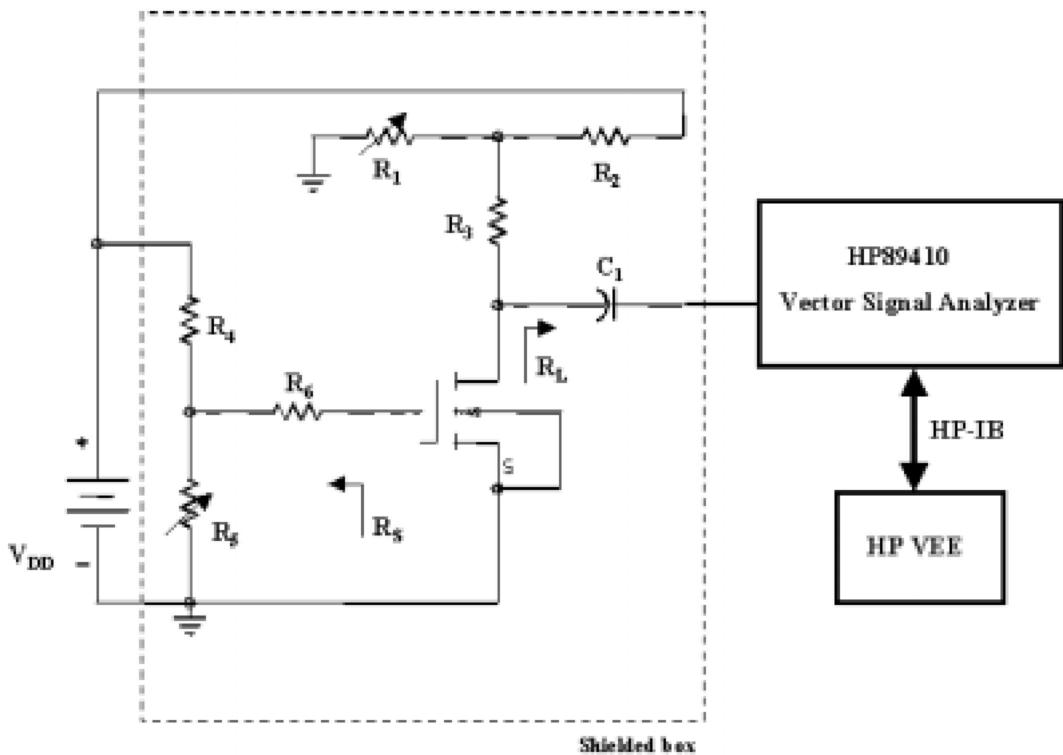


Fig. 4.2 The simplified topology of noise measurement impedance matching circuit [42].

To make our discussion clear Fig. 4.2 shows the simplified circuit topology of impedance matching in the interface unit. The interface unit is based on [35]. As the method [35] uses a large capacitor at the end of DUT in order to suppress noises from power supply and fluctuation of output load, it makes difficult the bias adjustment because of the large time constant. We designed a new interface circuit, which is configured by resistance as much as possible to overcome the problem. Only one capacitor (C_1) is used at the input of the signal analyzer. As the result, noise measurement with very low system noise level (1nV^2/Hz) can be performed. This measurement circuit is simple yet accurate comparing to another method using Lock-In-Amplifier. Also, this method has no particular limitation of driving current. To avoid the

fluctuation of output load, R_L, it is important to select appropriate circuit topology and resistance value.

In this research the input impedance of signal analyzer was set to 1 MΩ which is relatively high, R_L is simply represented as:

$$R_L = R_3 + \frac{R_1 \cdot R_2}{R_1 + R_2} \tag{4.1}$$

Where for $R_3 \gg R_2$ the fluctuation of R_L can be controlled. Foe instance, if the drain voltage is set to 5 V and then the measured drain current is from 0.5 mA to 10 mA, the fluctuation of R_L can be controlled within 5%. Usually, the fluctuation of output load of 5% is small enough to measure and model 1/f noise. However, if the fluctuation cannot be ignored, the output noise voltage density can be converted to the output noise current density by:

$$\overline{I_{nout}^2} \cong \frac{\overline{V_{nout}^2}}{R_L^2} \tag{4.2}$$

Here, V_{nout}^2 is measured output noise voltage density and I_{nrout}^2 is calculated output noise current density. Equation (4.2) can only be used if the drain-source resistance (*1 / Gds*) of DUT is much greater than R_L.

Also, for DUT input side, to reduce the fluctuation of input load resistance (R_S) has been carefully selected to satisfy $R_6 >> R_4$. If a MOSFET is selected as a DUT, the input noise current can be ignored because of the infinitesimal gate current. Because of that, R_S does not need to be set to large value. However, we used relatively large resistance (1 KΩ) of R_6 in this research to reduce the fluctuation of R_S. Also, large R_6 is convenient since the mutual inductance (G_{mgs}) of DUT in the measurement bias range is as small as 7.5 mA in maximum. Thermal noise generated by R_S and R_L is not ignored,

therefore, is included in the measured noise current density. It is represented by:

$$\overline{I_{nout}^2} \cong \overline{i_{nd}^2} + \overline{I_{nrl}^2} + \overline{V_{nrs}^2} \cdot G_{mgs}^2 \qquad \textbf{(4.3)}$$

Here, $\overline{I_{nrl}^2}$ is the thermal noise current generated by R_L, $\overline{V_{nrs}^2}$ is the thermal noise voltage generated by R_S, and $\overline{i_{nd}^2}$ is the drain noise current of DUT. After calculating $\overline{I_{nrl}^2}$, $\overline{V_{nrs}^2}$ and G_{mgs}^2, $\overline{i_{nd}^2}$ is obtained by solving (4.3).

The other important condition to determine R_S and R_L is DUT stability against the input and output load conditions [43]. In this kind of very small noise measurement if the input and output load impedance are located in the instability region, stable noise measurement cannot be made in many cases. Therefore, it is important to check if the input and output load impedance are not located in the instability region by drawing stability circles from the following equations:

$$\left| \Gamma_S - \frac{(S_{11} - S_{22}^* \cdot \Delta)^*}{|S_{11}|^2 - |\Delta|^2} \right| = \left| \frac{S_{12}S_{21}}{|S_{11}|^2 - |\Delta|^2} \right| \qquad \textbf{(4.4)}$$

$$\left| \Gamma_L - \frac{(S_{22} - S_{11}^* \cdot \Delta)^*}{|S_{22}|^2 - |\Delta|^2} \right| = \left| \frac{S_{12}S_{21}}{|S_{22}|^2 - |\Delta|^2} \right| \qquad \textbf{(4.5)}$$

$$\Delta = S_{11} \cdot S_{22} - S_{12} \cdot S_{21} \qquad \textbf{(4.6)}$$

Here, (4.4) and (4.5) represent orbit of the stability circle on Γ_S plain at the input side and on Γ_L plain at the output side, respectively. * means conjugate complex number.

Photoes of the noise measurement system that we developed and connection to a wafer prober are shown in Fig. 4.3 and Fig. 4.4.

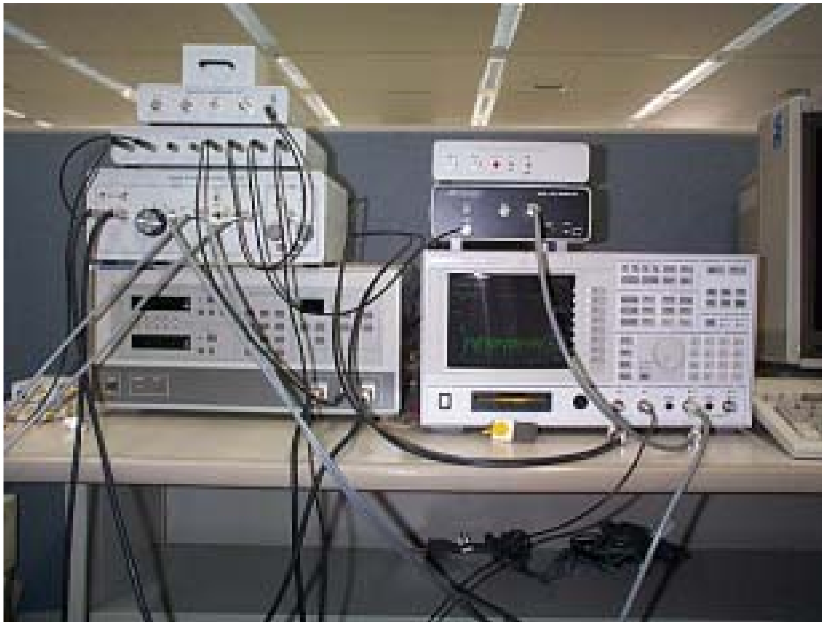


Fig. 4.3 Overview of 1/f noise measurement system.

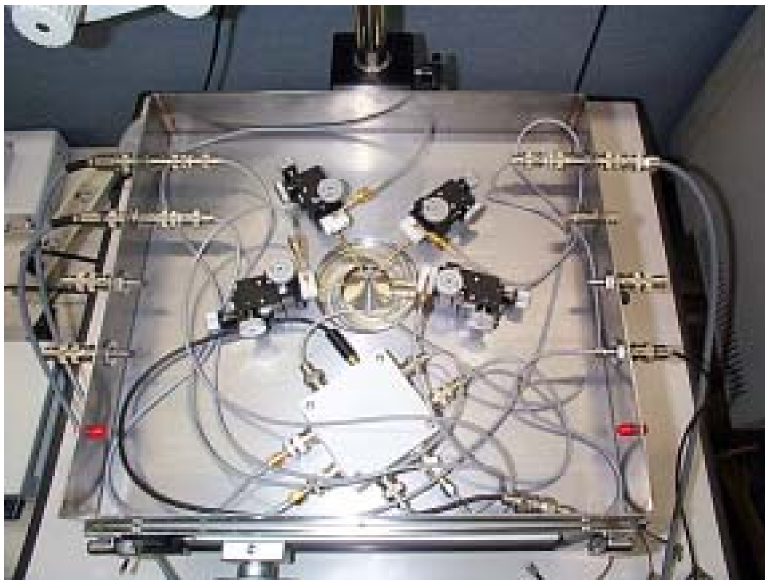


Fig. 4.4 Connection to a wafer prober for 1/f noise measurements.

4.2 Flicker Noise Modeling of a-Si Thin-Film-Transistors

There are number of noise sources existing for a-Si TFT's. They are thermal, shot, popcorn, and flicker noises. Since popcorn noises are irregularity generated and difficulty of their theoretical analysis, we do not treat them. Since shot noises are induced by gate leakage current in any silicon based field effect transistors, they are not affected in active linear and saturation regions where most analog circuits work. We, therefore, focus on thermal and flicker noises in this research. a-Si TFT model [23] that were described in Chapter 2 will be used for adding a flicker noise model to dc and capacitance models.

4.2.1 A small signal noise equivalent circuit and model equations of a-Si TFT's

Fig. 4.5 shows an equivalent circuit of an a-Si TFT. Here, C_{gs} and C_{gd} are the gate-to-drain and gate-to-source capacitance, V_{gs} is gate-to-source voltage, i_{rd}, i_{rs}, and i_d are the noise current of drain, source, and internal drain-to-source resistance, respectively.

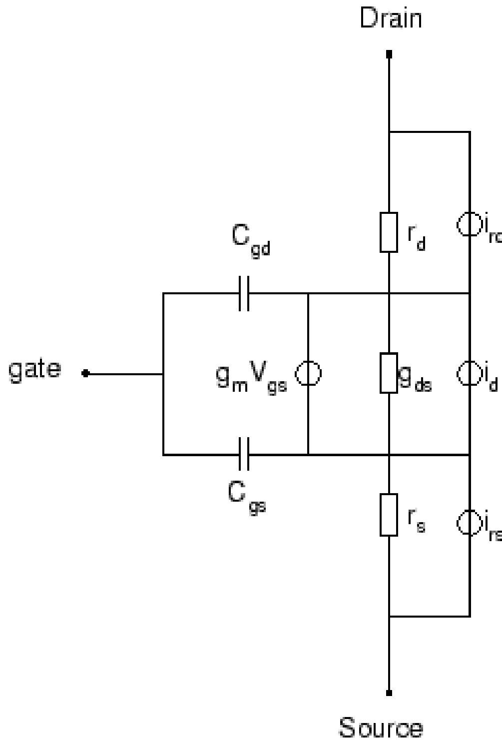


Fig. 4.5 A small signal noise equivalent circuit of a-Si TFT's.

As thermal noises are generated at any resistance elements, thermal noise sources are existing at drain and source resistance. First, we observe drain resistance, r_d. Since a noise voltage source and r_d are connected in series, the noise power is [22] written as:

$$P_{NA} = kT\Delta f = \frac{\overline{e_n^2}}{4r_d} \tag{3.7}$$

Therefore, the noise current, $\overline{i_{rd}^2}$, is re-written as:

$$\overline{i_{rd}^2} = \frac{\overline{e_n^2}}{r_d^2} = \frac{4kT}{r_d}\Delta f \tag{4.8}$$

In the same manner, source thermal noise current, $\overline{i_{rs}^2}$, is represented as:

$$\overline{i_{rs}^2} = \frac{4kT}{r_s}\Delta f \qquad (4.9)$$

Here, k is Boltzman constant, T is the device temperature, and Δ_f is the frequency band width. Though i_d can be formulated in the same manner, thermal noises generated at the element is low enough to disregard.

It is considered that flicker noise of an inverted staggered a-Si TFT is generated by trapping and de-trapping localized states. However, since conduction channel is not made at the surface, the noise level is not so high as MOSFET's but is higher than bipolar junction transistors' **[32]**. The slope of frequency characteristic of noise might be different from MOSFET's. Based on the above prerequisite, the noise current density generated from drain-to-source channel is written as:

$$\overline{i_d^2} = \frac{8kT}{3}(g_m + g_{ds})\Delta f + K_f \cdot \frac{I_d^{A_f}}{f^{E_f} \cdot C_{ox} \cdot L \cdot W} \qquad (4.10)$$

Here, K_f is a coefficient to correct noise current level and A_f and E_f are exponents to express drain bias current dependency and to express frequency dependency of current noise, respectively. These are all model parameters. The drain current equation is from **[23]** and is represented as (4.11). Where noise analysis presented in this research is performed in either linear or saturation regions.

In linear region,

$$I_{ds} = \frac{W}{L} \cdot \mu_{eff} \cdot C_{fm} \cdot \left[(V_{gs} - V_{TO} - \eta \cdot V_{ds}) \cdot V_{ds} - \frac{V_{ds}^2}{2}\right]. \qquad (4.11)$$

In saturation region,

$$I_{ds}^{sat} = I_{ds} \cdot \frac{v_{sat} \cdot L}{(1.0 + V_{ds}) \cdot \mu_{eff}} \cdot \quad (4.12)$$

Here, V_{TO} is the threshold voltage, μ_{eff} is the effective electron mobility, C_{fm} is the gate insulator film capacitance, L and W are the effective gate channel length and width, respectively, η is a fitting parameter to express static feedback caused by localized charge, and v_{sat} is the electron velocity saturation parameter.

4.2.2 Flicker noise model parameter extraction [44]

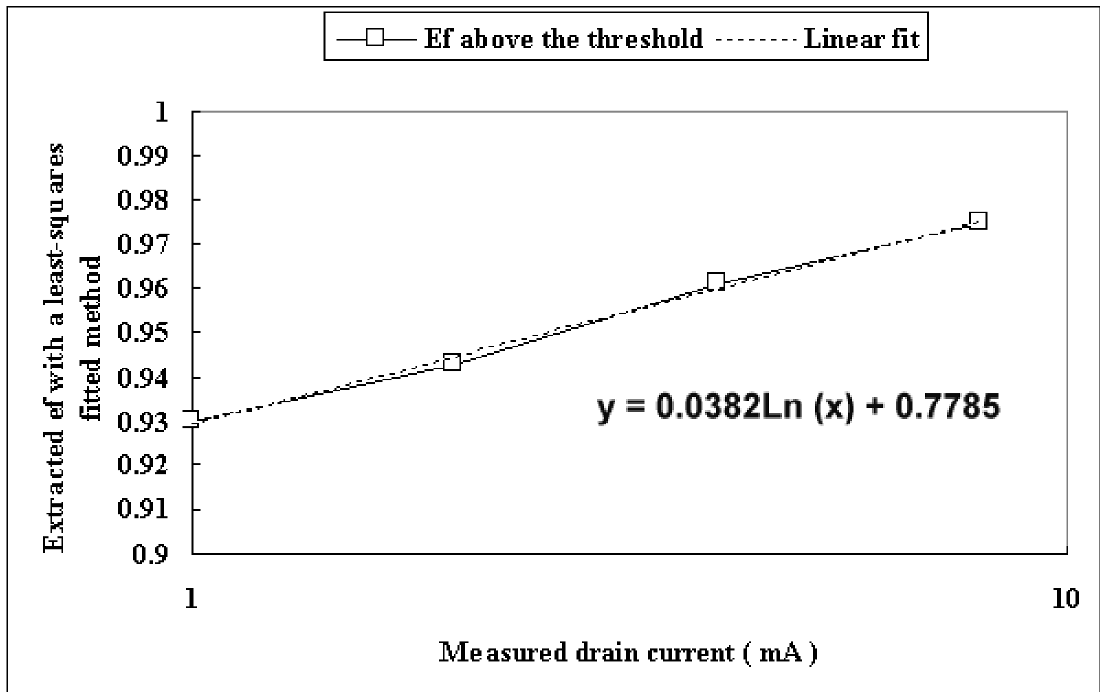


Fig. 4.6 **Drain current dependency of** E_f.

Next we discuss the extraction method of E_f.

By means of (4.10), E_f is a parameter which represents the negative slope of flicker noise characteristic against frequencies. Therefore, if E_f equals one,

the noise current densities are decreased with the inverse number of frequencies. Since the slope is not depend on bias, the average value within the application biases can be adopted. In this research we analyze the bias dependency of E_f and calculate the nominal value. Fig. 4.6 shows drain current dependency of E_f which is extracted by using least square interpolation. The drain current bias range is set from 0.4 mA to 7.6 mA. As shown in Fig. 4.6, it is clear that E_f is bias dependent and whose value is approaching to one as the current higher. The drain current dependency of E_f in Fig. 4.6 was measured after the drain voltage was set to 20 V and the gate voltage was set to the voltage greater than threshold. It is clearly shown that the plot can be approximated by linear equation against $log_e(x)$ which is shown in (4.13). This kind of characterization process is important because optimum value of E_f can be easily obtained at the drain current which is needed in the application.

$$E_f = a \cdot \log e(I_{ds}) + b \tag{4.13}$$

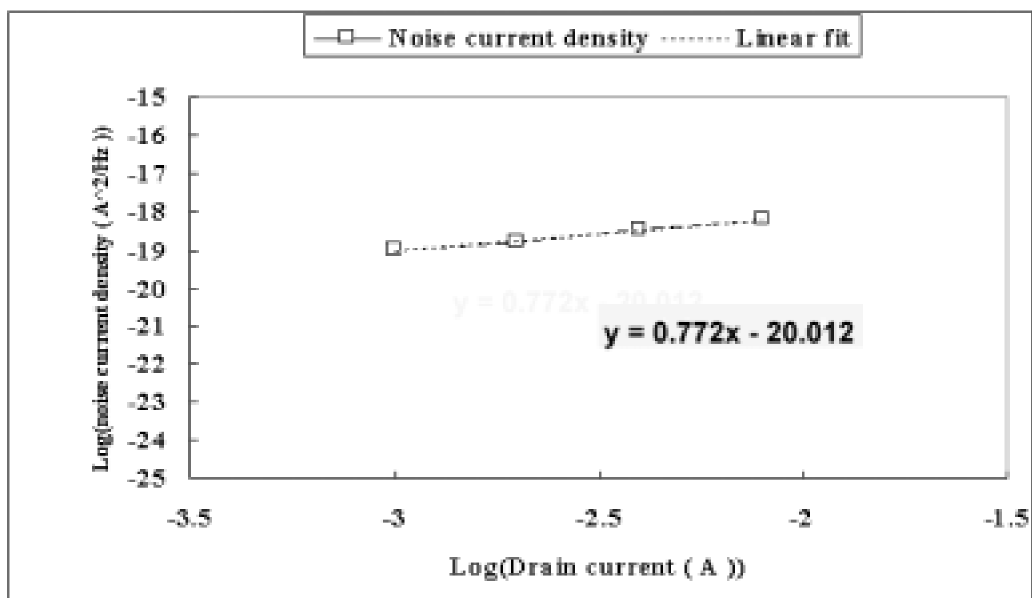


Fig. 4.7 A plot for extracting A_f and K_f, directly.

A_f and K_f is model parameters to represent bias dependencies of current noise. For MOSFET devices the typical value of A_f is close to one and K_f is in the range from 1 x 10^{-28} to 1 x 10^{-19} **[22]**. Since conduction channel of TFT's are made below to the surface, flicker noise level is much lower than MOSFET's. Therefore, K_f will be higher than MOSFET's. In order to extract two unknown variables, A_f and K_f, at least, two bias sets of noise data are required. In **[35]**, these parameters were extracted by using noise corner frequencies. However, this method cannot be used to extract flicker noise parameters for MOSFET's and TFT's since their corner frequencies are too high to measure in this measurement method. In this research A_f and K_f are extracted by using noise current density data directly. Using **Fig. 4.8**, the frequency point to be used was selected at 10 KHz since the noise characteristic is stable. **Fig. 4.7** shows logarithmic scale of drain current, Ids, versus drain noise current density, $\overline{i_d^2}$, plot. If the slope of linearly approximated by one dimensional equation assumes as *a* and the **intersection point** to *Y* axis as *b* in the graph, **(4.14)** and **(4.15)** can be derived from **(4.10)**. Here, Δf is set to one for simplify the calculation.

$$A_f = a \qquad (4.14)$$

$$K_f = 10^b \cdot C_{fm} \cdot L^2 \cdot f^{E_f} \qquad (4.15)$$

(4.14) and **(4.15)** make the direct extraction of A_f and K_f possible without optimizations. Because of this, the extracted parameters are theoretically **allegiance** and no **inconsistency**, which are very important to apply these parameters for statistical analysis or modeling **[46]**.

4.2.3 Noise Measurement and Simulation of an a-Si TFT

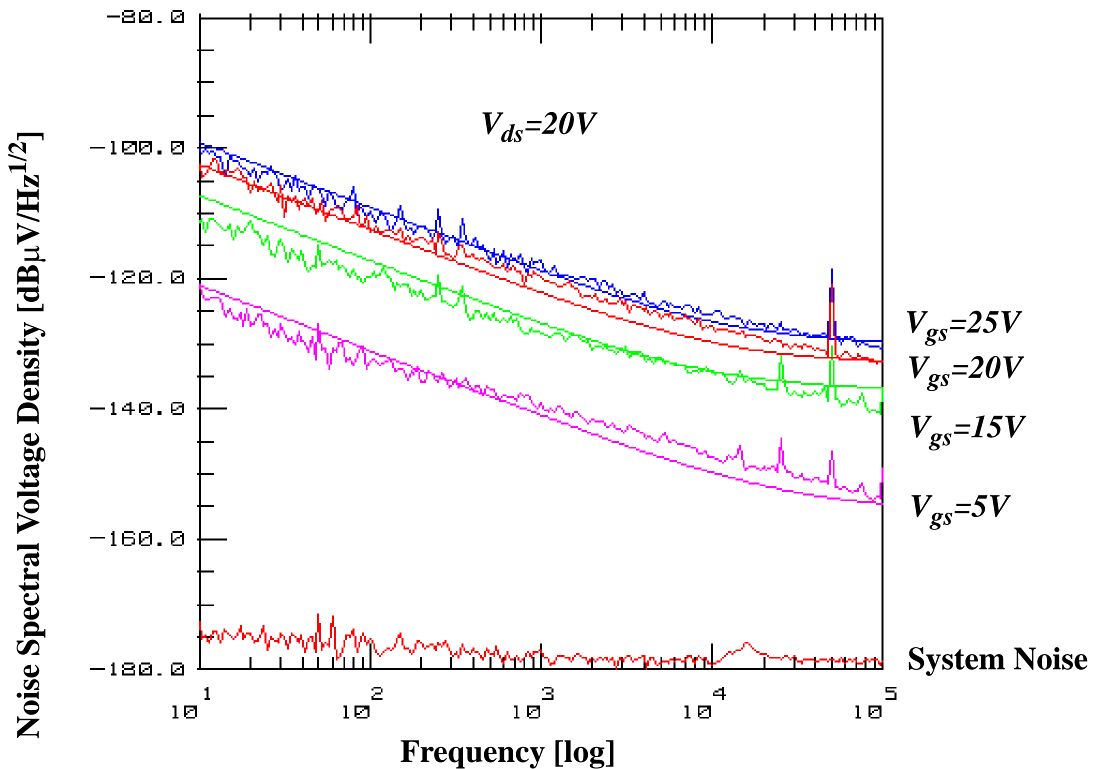


Fig. 4.8 **Flicker noise voltage density measurement (solid line) and simulation (dotted line).**

The developed model and extraction methods have been verified by comparing with measured noise voltage density of an a-Si TFT. The DUT is an a-Si:H TFT whose channel length, channel width, and the thickness of gate insulator film are **11**μm, **41**μm, and **300**nm, respectively. Also, the gate insulator film is made from SiN. Where, in **Fig. 4.8** the solid line represent the measured flicker noise voltage density and the dotted line shows the SPICE simulation of the model newly developed.

Before extracting flicker noise model parameters, A_f, K_f, and E_f, drain current model parameters **[23]** were measured and extracted. The rms error

of drain current versus drain voltages between measurement and simulation was less than 3%. Flicker noise parameters were extracted by the method described in 4.2.2. As shown in **Fig. 4.8**, the simulation shows good agreement with measurement. The result can also be applied for other simulations such as transient analysis which reverse Fourier transform function is used.

4.3 Flicker Noise Modeling of n-MOSFET's

CMOS transistors are often required as the core parts for analog circuits and applications. Those are preferred for dense, low voltage, and low power applications. While the advantages of CMOS technology are well established, there is a major drawback for analog applications. The MOSFET's are so noisy although so called "analog low noise" fabrication processes are used. The excess noise of MOSFET's is dominated by 1/f noise up to relatively high frequencies of the order of several tenth of kilohertz. The origin of 1/f noise in MOSFET's has been the subject of numerous studies. According to recent studies, the origin is carriers trapping detrapping between the transistor channel and oxide traps but the precise mechanisms involved are not fully characterized. According to other studies, mobility fluctuations, either by themselves or in addition to number fluctuations, are identified as the cause of 1/f noise in MOSFET's.

Adding a 1/f noise current source to general small signal equivalent circuit produce the model in Fig. 4.9. The extrinsic resistance exhibits thermal noise. For certain device structures, the polysilicon gate resistance and substrate resistance can be significant contributors to noise.

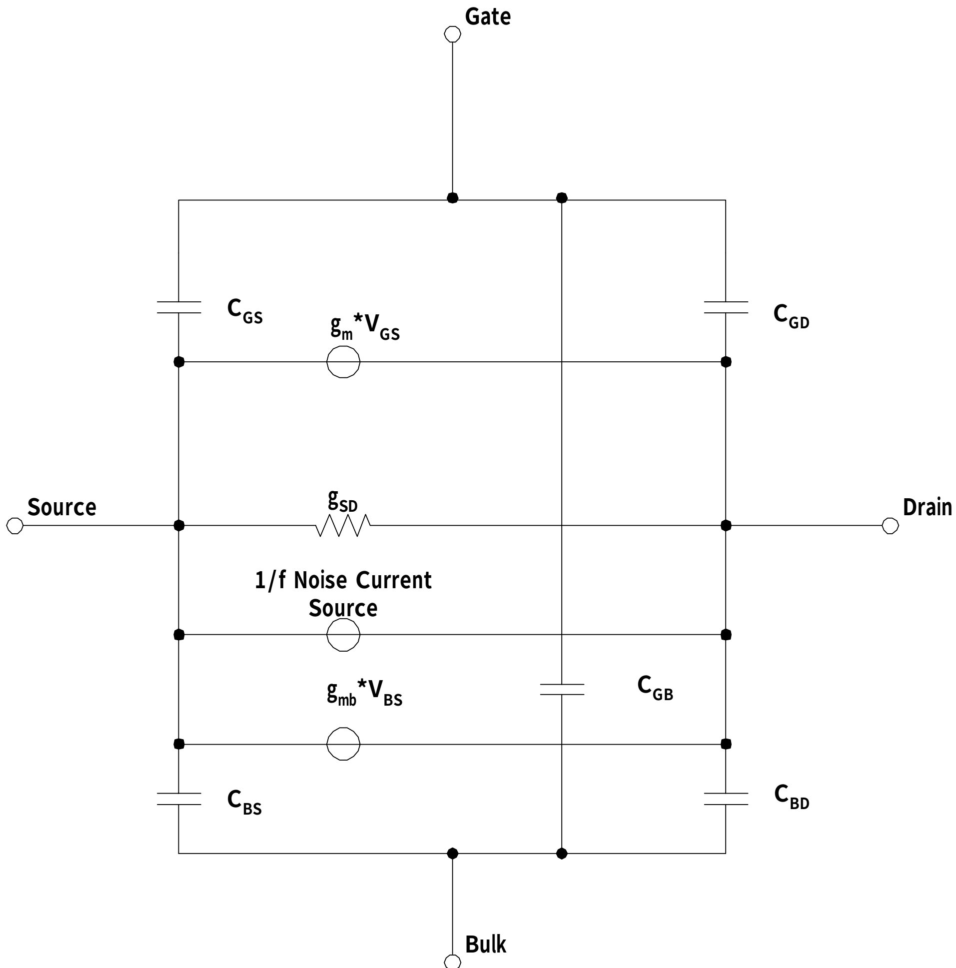


Fig. 4.9 A small signal equivalent circuit for the intrinsic part of a MOSFET with a noise current source. Here, C_{GS}, C_{GD}, C_{GB}, C_{BS}, and C_{BD} are gate-to-source, gate-to-drain, gate-to-bulk, bulk-to-source, and bulk-to-drain capacitance, respectively, g_{SD} is the source-to-drain conductance, and g_m and g_{mb} are trans conductance and substrate trans conductance, respectively.

Since a generally accepted physical model is still lacking, analog designers and users rely on empirical models, whose drain flicker noise current density, i^2_{fD}, is formed as

$$\overline{i_{fD}^2} = K_f \cdot \frac{I_D^{A_f}}{f \cdot C_{OX} \cdot L_{eff}^2} \cdot \Delta f, \quad (4.16)$$

or

$$\overline{i_{fD}^2} = K_f \cdot \frac{I_D^{A_f}}{f \cdot C_{OX} \cdot L_{eff} \cdot W_{eff}} \cdot \Delta f. \quad (4.17)$$

Here, Δf is a small band width at frequency f, I_D is the drain dc current in saturation region, C_{OX} is the oxide capacitance, L_{eff} and W_{eff} are the effective gate channel length and width, A_f and K_f are the flicker noise exponent and coefficient, respectively. For the bias dependencies simulation accuracy of these models is not so high enough to use it for analog circuit design. The model lacks bias dependencies of frequency characteristic in drain current noise density that has been observed especially in deep-submicron MOSFET's.

4.3.1 Bias dependencies of flicker noise current

We developed a new flicker noise model which is based on [30]. Existing models which include BSIM3 [16], UCB MOSFET's [14], Philips MOS Model 9 [33], and HSPICE's [34] formulate the frequency dependency as a constant exponent, E_f. This assumption can be used for long channel MOSFET devices. However, as the channel length becomes shorter in the saturation region, hot electrons will be generated because of the high electrical field at the drain channel. Such electrons may change the flicker noise frequency characteristics. We, therefore, analyzed frequency and drain current dependencies as shown in Fig. 4.10.

The measured drain current dependent function of E_f, which is represented as E_{ff} (I_{ds}), is in proportional to the drain current, which is included in our drain noise current model equation as:

$$\overline{i_{nd}^2} = \frac{8kT}{3}(G_{mgs} + G_{mbs} + G_{ds})\Delta f$$

(Thermal noise term)

$$+ \frac{K_f I_{ds}^{A_f}}{C_{ox} L_{eff} W_{eff} f^{E_{fa} \cdot \log e(I_{ds}) + E_f}} \Delta f \quad . \qquad (4.18)$$

(Flicker noise term)

Here, E_{fa}, which can be set to zero in order to maintain the compatibility of [32] and other UCB SPICE models, is a coefficient to represent drain current dependency of E_f, G_{mgs} and G_{mbs} are the trans conductance of gate-to-source and gate-to-bulk, respectively, G_{ds} is the output conductance, Δf is the frequency band width of noise, C_{ox} is the oxide film capacitance, L_{eff} and W_{eff} are the effective channel length and width, respectively, and A_f and K_f are an exponent and a coefficient of drain current dependencies, respectively.

Before extracting E_f, E_{fa}, A_f, and K_f we measured an RF MOSFET, whose gate oxide thickness, gate mask length, and gate mask width are 10nm, 0.8μm, and 200μm, respectively. The measured current noise densities are shown in Fig. 4.10. Since the thermal noise component of is much lower than measurement system noise level at the room temperature, the E_{ff} (I_{ds}) is calculated from frequency characteristic of the flicker noise current density component (4.19).

$$\overline{i_{ndf}^2} = \frac{K_f I_{ds}^{A_f}}{C_{ox} L_{eff} W_{eff}} \Delta f \cdot f^{-E_{ff}(I_{ds})} \qquad (4.19)$$

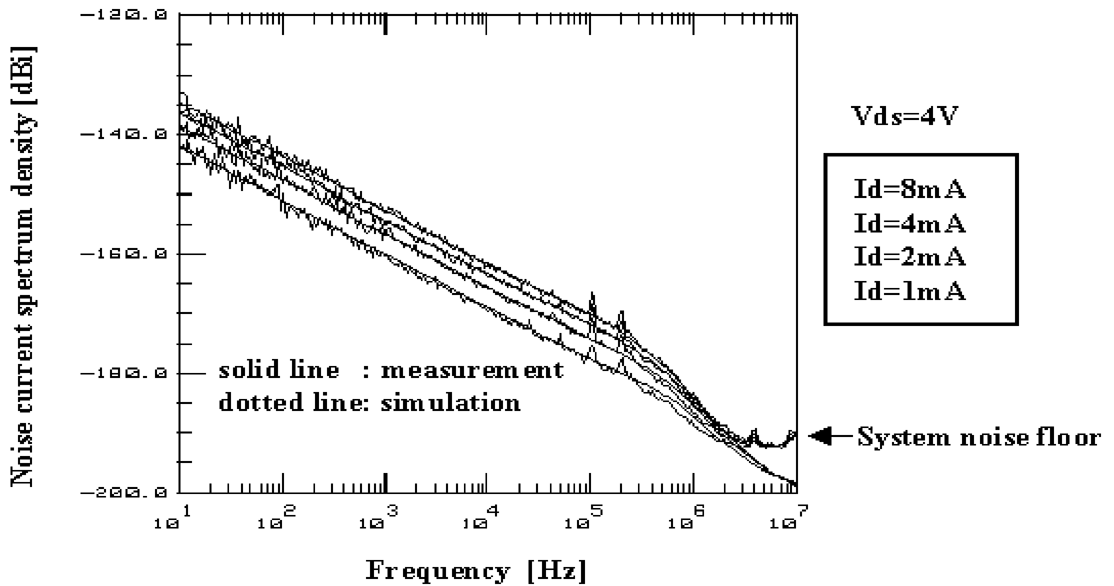


Fig. 4.10 Noise current spectrum density measurement and simulation.

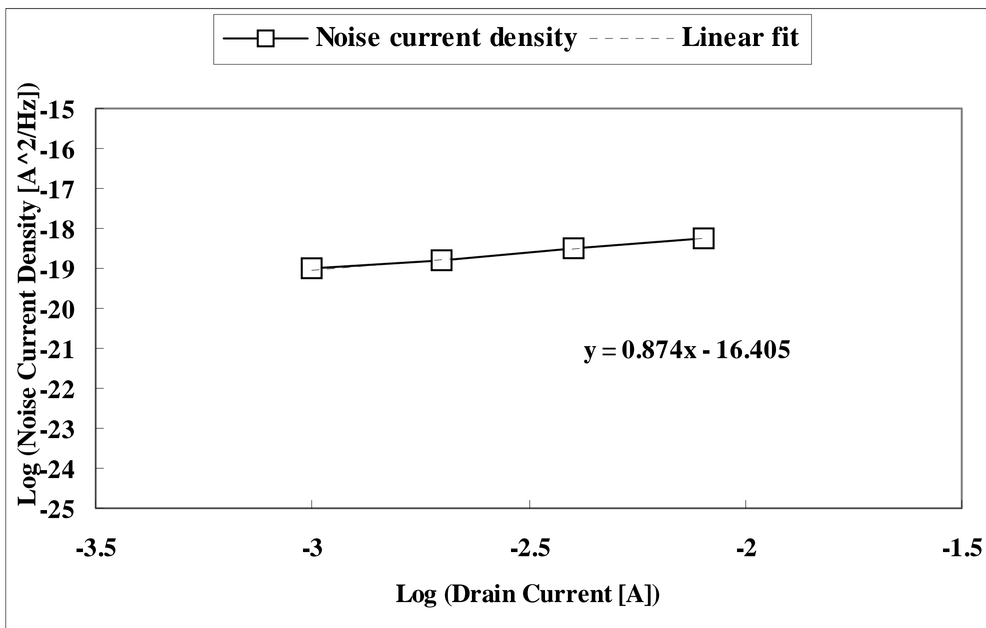


Fig. 4.11 Direct extraction of A_f and K_f.

Using the E_{ff} (I_{ds}), E_f and E_{fa} are extrapolated from Fig. 4.10.

To extract A_f and K_f, (4.19) should be transformed by logarithm function to apply linear approximation to the measured data in Fig. 4.11. The transformed logarithm scale plot is shown in Fig. 4.11. A_f and K_f are written as

$$A_f = a \,, \tag{4.20}$$

$$K_f = 10^b \cdot C_{ox} L_{eff} W_{eff} f^{E_{ff}(I_{ds})} \tag{4.21}$$

here, Δf was set to unity to follow the measurement condition, a is 0.874, and b is -16.405.

Fig. 4.10 shows roll off characteristic at high frequency region. In order to simulate the roll off the gate-to-drain parasitic capacitance (C_{gd}) should be measured accurately. The simulation in Fig. 4.10 has been obtained by extracting drain current, flicker noise, and capacitance model parameters with BSIM3 after flicker noise model modifications. These modeling process was completed by using Agilent IC-CAP modeling software [15].

4.3.2 Analysis of Geometry Dependency

Short channel MOSFET devices (L_o is shorter than 2 μm), which channel length modulation effect becomes significant, can be noisier than long channel MOSFET's. It is mainly caused by velocity saturation and hot electron effects. Both of these effects are related to the electric field at the drain channel. Hot carriers are responsible for the drain-to-substrate current, I_{BD}, which shows shot noise at low substrate current values and excess noise at high current values in this current. Since I_{BD} produces a voltage drop across the substrate resistance, its noise modulates the effective substrate potential. This means that the fluctuations in the latter are coupled to the drain current through the substrate trans conductance, g_{mb}, and can contribute to

an increase in the observed drain 1/f current noise. Existing model equations to represent channel length dependencies in saturation region are conceptually two types that are (4.16) and (4.17). In our experiments reverse square of L_{eff} dependency in (4.16) could represent device characteristic accurately, which is shown in Fig. 4.15, whereas (4.17) did not work at all. As a result, our model (4.19) should be corrected.

For channel width dependencies, so far, it had been described that flicker noise decreased with the gate area ($L_o \times W_o$) of a MOSFET. Our assumption of channel width dependencies of flicker noise is as follows: Although some percentages of noise were averaged out in wide channel devices [32], it had been further summed up as an increase in the channel width, if flicker noise was generated in the surface gate channel at any channel length per unit channel width. Even though the channel width had been further narrowed, the noise level was not so decreased with the channel width.

Using the above assumption we start with the modification of (4.19) as

$$\overline{i_{fD}^2} = K_f \cdot \frac{I_D^{A_f} \cdot f(W_{eff})}{f^{E_{fa} \cdot \log(I_D) + E_f} \cdot C_{OX} \cdot L_{eff}^2} \cdot \Delta f . \quad (4.22)$$

As we discussed above, i^2_{fD} increases with any function of W_{eff}, which is expressed by $f(W_{eff})$. Here, we focus on single gate stripe MOSFET's for analyzing channel width dependency. In order to derive the function we adopted correlation analysis between adjacent unit current noises in the channel width. As shown in Fig. 4.12, we assume each unit current noise density ($i^2_{fD}(1)...i^2_{fD}(n)$) is traveling from drain to source channel. Although one unit current noises correlate with other unit current noises than the next, the next current noise has the strongest correlation. Therefore, the total noise current density will be represented as the summation of each current noise source with correlation coefficient as shown in Fig. 4.12.

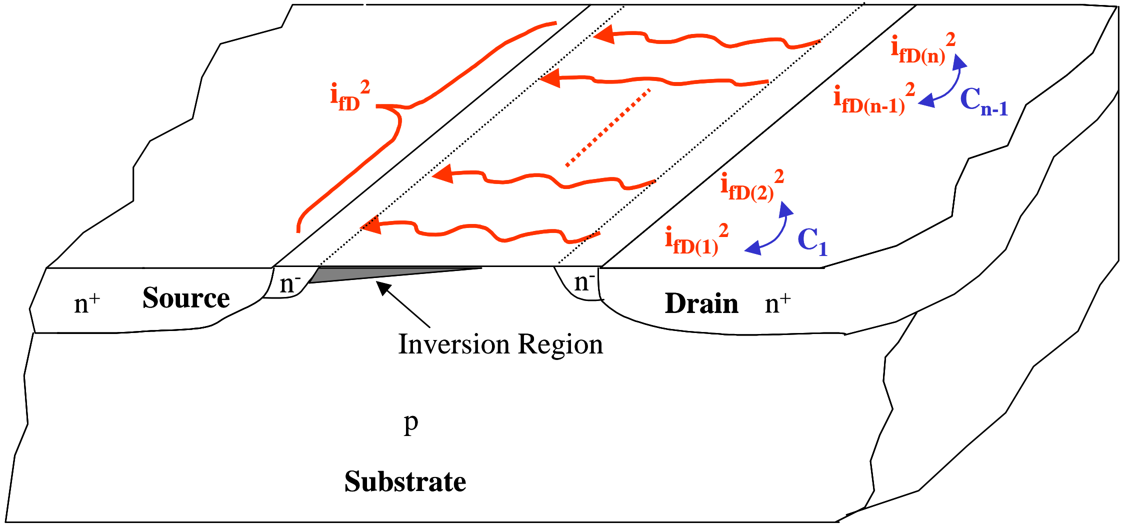


Fig. 4.12 Illustration of flicker noise behavior with correlation coefficient for the normalized current noise source per unit channel width.

Total flicker noise current i^2_{fD} in Fig. 4.12 can be represented as (4.23).

$$i_{fD}^2 = i_{fD(1)}^2 + i_{fD(2)}^2 + \dots + i_{fD(n-1)}^2 + i_{fD(n)}^2 + 2C_1 \cdot i_{fD(1)} \cdot i_{fD(2)} + \dots + 2C_{n-1} \cdot i_{fD(n-1)} \cdot i_{fD(n)} \quad (4.23)$$

Where $i_{fD(1)}$, $i_{fD(2)}$, ... ,$i_{fD(n-1)}$, and $i_{fD(n)}$ are normalized minimum current noise sources per unit channel width. C_1,..., C_{n-1} are the correlation coefficients for adjacent current noise sources and n is number of the current noise sources. When each current noise arises from a common phenomenon, the noise sources should be partially correlated and have the range of the correlation coefficient from 1 to -1. If the coefficient equals to 0, the noise sources are not correlated. When the coefficient equals to 1, the noise sources are totally correlated and *r.m.s.* values of each noise can be added linearly. A coefficient value of -1 implies subtraction of correlated noises.

Since we expect that $i_{fD(1)} = i_{fD(2)} = ... = i_{fD(n)}$ and $C_1 = C_2 = ... = C_{n-1}$, (4.23) can be simplified to (4.24).

$$i_{fD}^2 = n \cdot i_{fD(n)}^2 + 2C_{n-1} \cdot i_{fD(n)}^2 \quad (4.24)$$

Flicker noise current density (4.24) with noise correlation theory had been validated by comparing measured noise spectral current density for channel width from 10μm to 100μm as shown in Fig. 4.13.

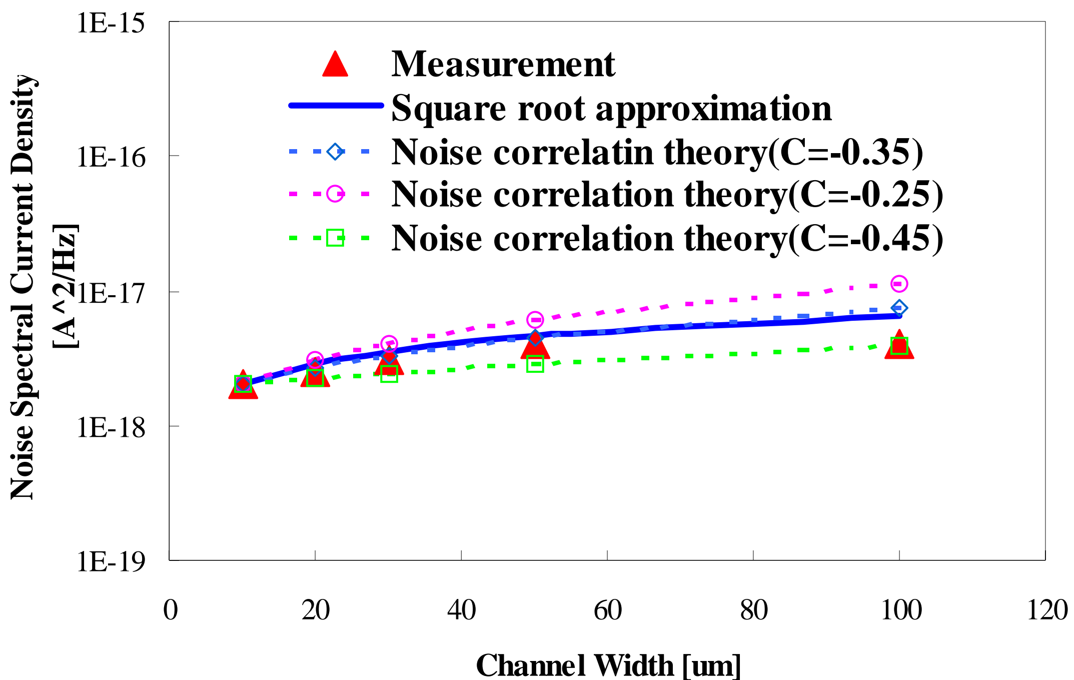


Fig. 4.13 W_{eff} dependencies of flicker noise current density. Measured noise current density is compared with the functions of the noise correlation theory and proposed square root approximation for channel width.

Excellent agreements have been obtained between measurement and the noise correlation theory with *C=-0.35* for channel width from 10μm to 50μm.

Also, we have found that the *f (Weff)* with noise correlation theory at *C=-0.35* could be approximated by square root function of W_{eff} as shown in (4.25).

$$i_{fD}^2 = K_f \cdot \frac{I_D^{A_f} \cdot \sqrt{W_{eff}}}{f^{E_{fa} \cdot \log(I_D) + E_f} \cdot C_{OX} \cdot L_{eff}^2} \cdot \Delta f . \qquad (4.25)$$

4.3.3 Noise measurement and extraction of n-MOSFET's

Since there are no geometry independent model parameters in (4.25), only a set of frequency characteristic of noise current density curves is needed in one size for parameter extractions as shown in Fig. 4.14.

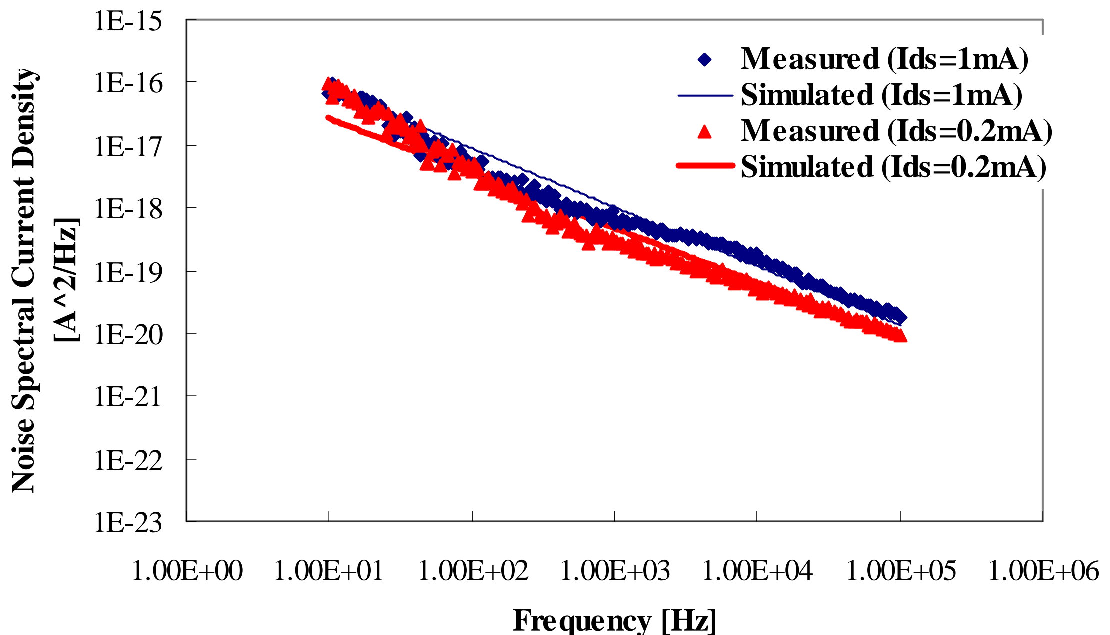


Fig. 4.14 An n-MOSFET characteristic of noise current density which was used to extract flicker noise parameters (A_f, K_f, E_{fa}, and E_f) in the strong inversion region (I_D=0.2 mA, 1 mA and V_D=3 V) using the 0.5 µm CMOS process. Here, drawn length, L_o and drawn width, W_o are 0.8 µm and 20 µm, respectively. Dc and CV parameters in BSIM3 model were extracted in advance.

Using our automated high sensitivity 1/f noise measurement system [42], whose system noise floor was $5.8x10^{-26}$ A^2/Hz, we performed extensive flicker noise measurements. In order to keep close the bias conditions for all geometry devices both of constant drain current and gate voltage measurements were made. During the measurement process dependent noise fluctuations [39] have been observed. Therefore, we selected typical devices that have less noise fluctuations. The measured data in Fig. 4.14 is the only measurement to be used for extracting the flicker noise model parameters, A_f, K_f, E_{fa}, and E_f.

Fig. 4.15 is the comparisons between measurement and simulation to analyze the channel length dependencies after extracting dc, CV, and flicker noise parameters. Here, the channel length dependencies are close to the inverse number of square function.

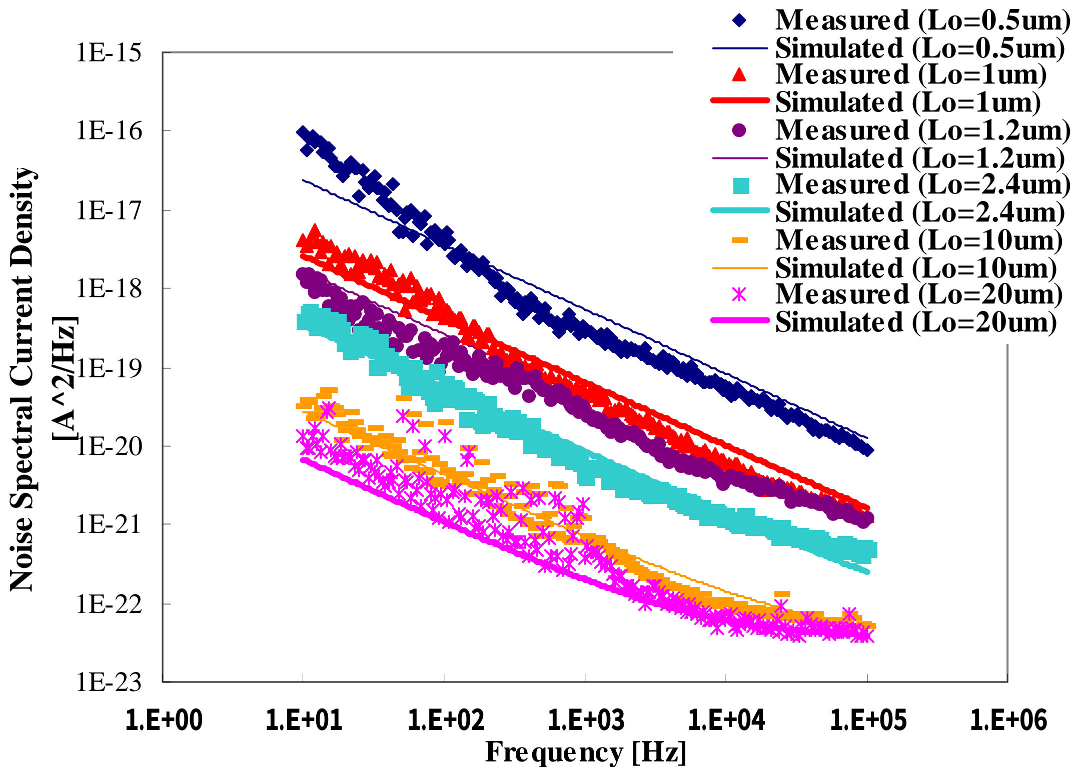


Fig. 4.15 N-MOSFETs noise current density comparisons between measured and simulated data to analyze the channel length dependencies (L_o=0.5, 1.0, 1.2, 2.4, 10, 20 μm and W_o=20 μm) for constant drain current (I_D=0.2 mA) using the 0.5 μm CMOS process. Here, the supplied drain bias voltage is 3 V.

For better understanding the noise spectral current density versus effective channel length at two frequencies was plotted from Fig. 4.15 as shown in Fig. 4.16.

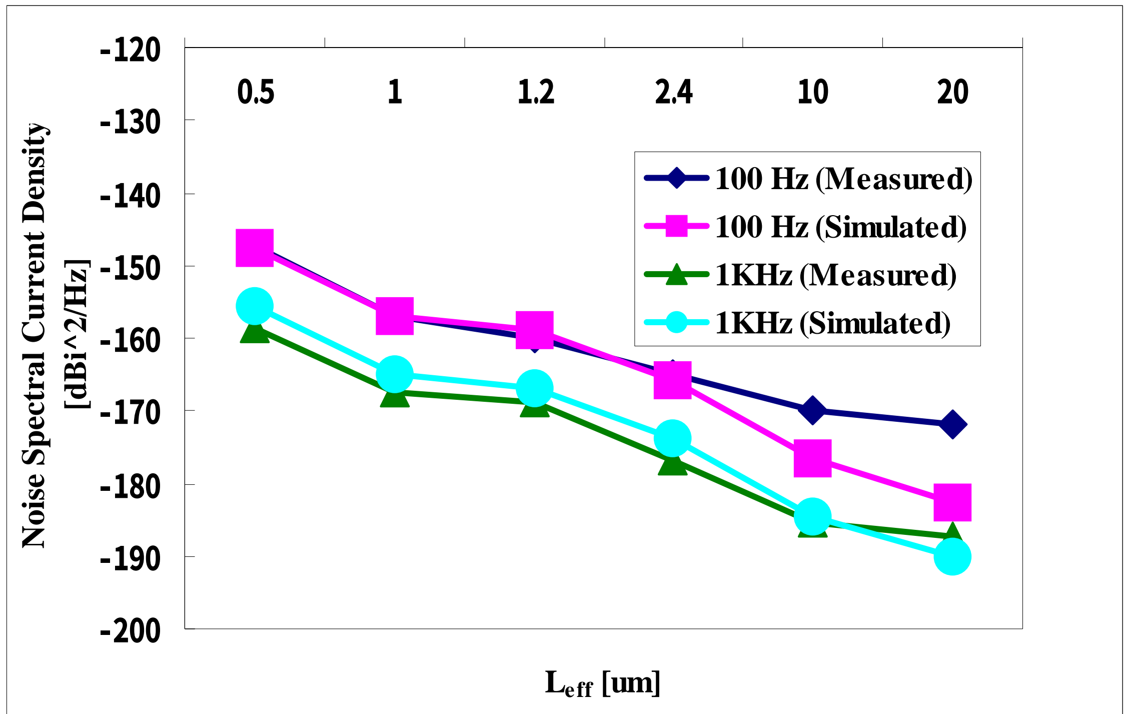


Fig. 4.16 N-MOSFETs' channel length dependencies of measured and simulated noise current density (100 Hz and 1 KHz) for constant drain current (I_D=0.2 mA) using the 0.5 μm CMOS processes. Here, the supplied drain bias is 3 V.

Fig. 4.17 and Fig. 4.18 show the channel width dependencies of measured and simulated data using the same parameters extracted in Fig. 4.14.

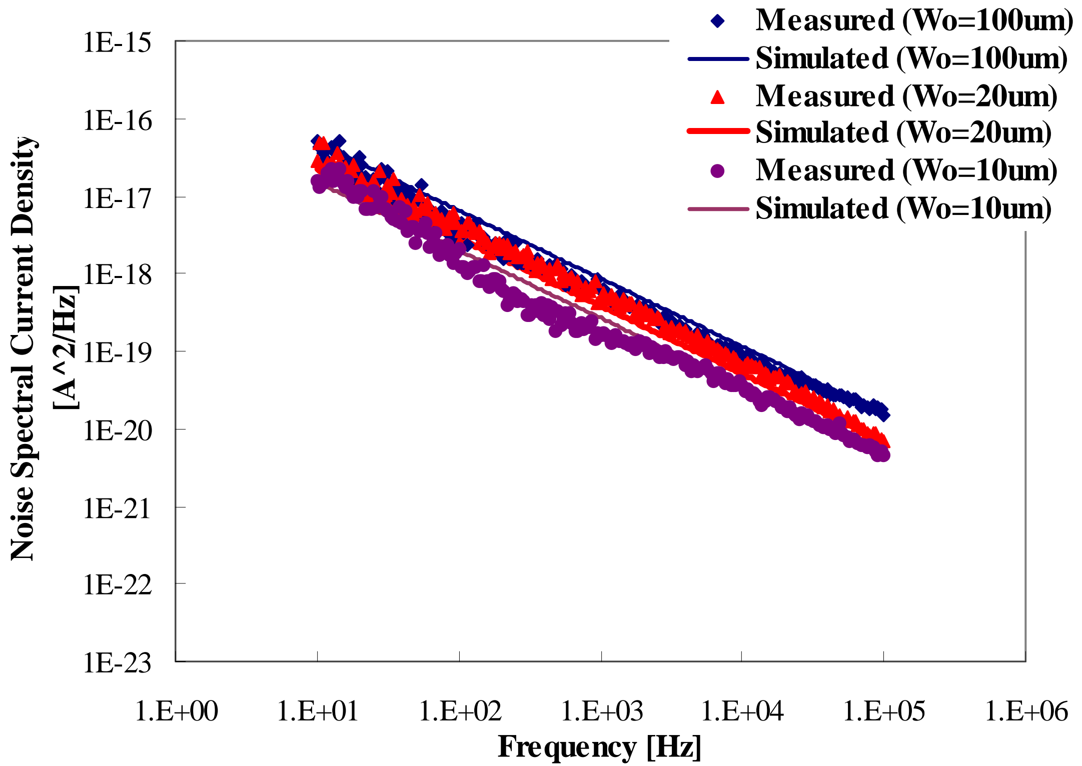


Fig. 4.17 N-MOSFETs noise current density comparisons between measured and simulated data to analyze the channel width dependencies (W_o =10, 20, 100 μm and L_o=0.5 μm) for constant drain current (I_D=0.2 mA) using the 0.5 μm CMOS process. Here, the supplied drain bias voltage is 3 V.

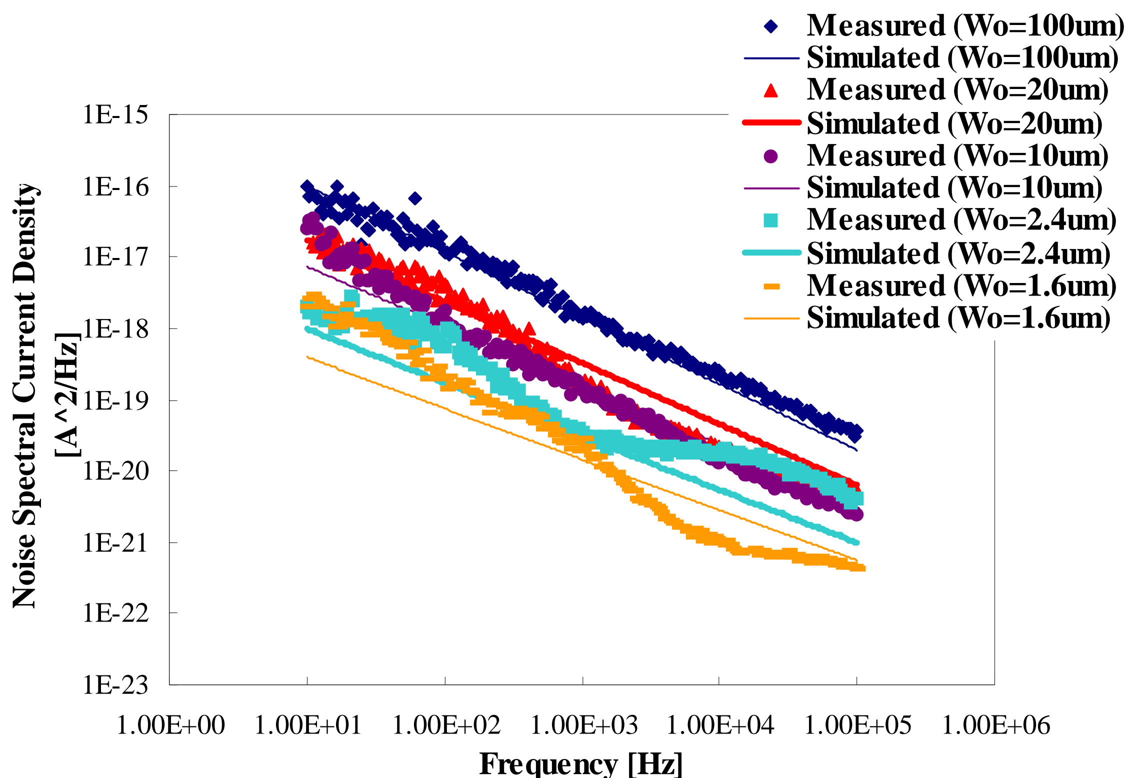


Fig. 4.18 N-MOSFETs noise current density comparisons between measured and simulated data to analyze the channel width dependencies (W_o=1.6, 2.4, 10, 20, 100 μm and L_o=0.5 μm) for constant gate voltage (V_G=1.4 V) using the 0.5 μm CMOS process. Here, the supplied drain bias is 3 V.

As we discussed in previous section, when the channel width was narrowed, the noise level was not so decreased at the width of 1.6μm in Fig. 4.18. As shown in Fig. 4.18, measured data at the width of 1.6μm and 2.4μm show noise fluctuations caused by device fabrication.

This could be approximated by square root function. The assumption was verified by calculating the noise current spectral density correlation of channel width in two different process devices as shown in Fig. 4.19 and Fig. 4.20.

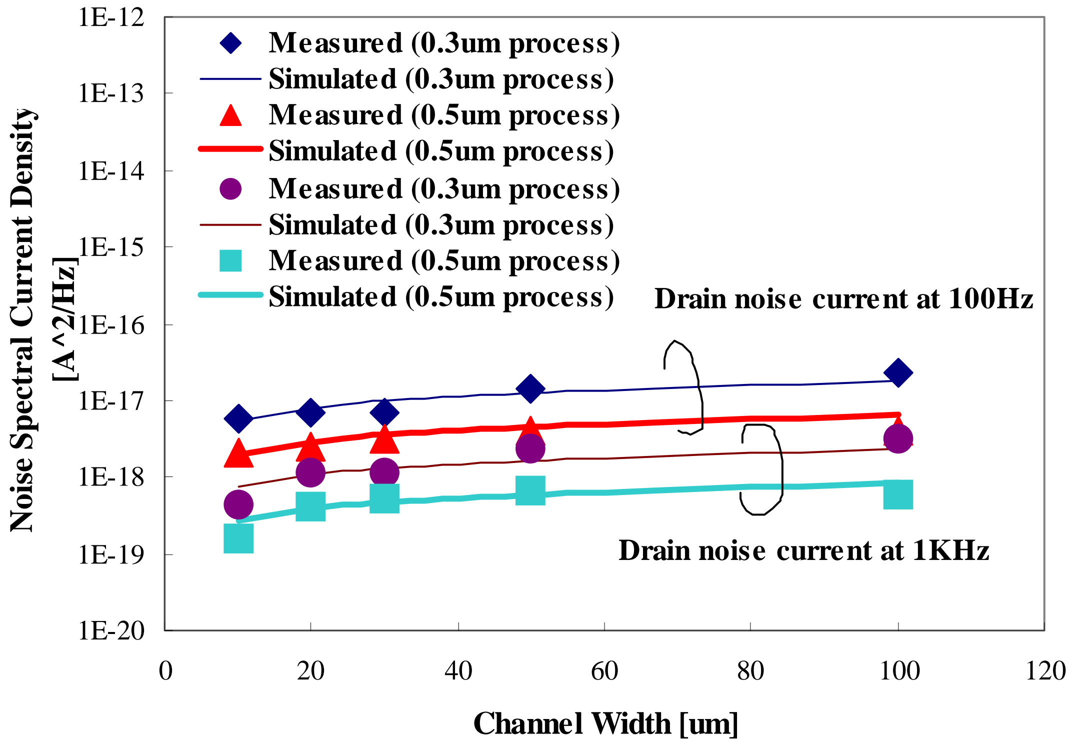


Fig. 4.19 N-MOSFETs' channel width dependencies of measured and simulated noise current density (100 Hz and 1 KHz) for constant drain current (I_D=0.2 mA) using the 0.3 μm and 0.5 μm CMOS processes. Here, the supplied drain bias is 3 V.

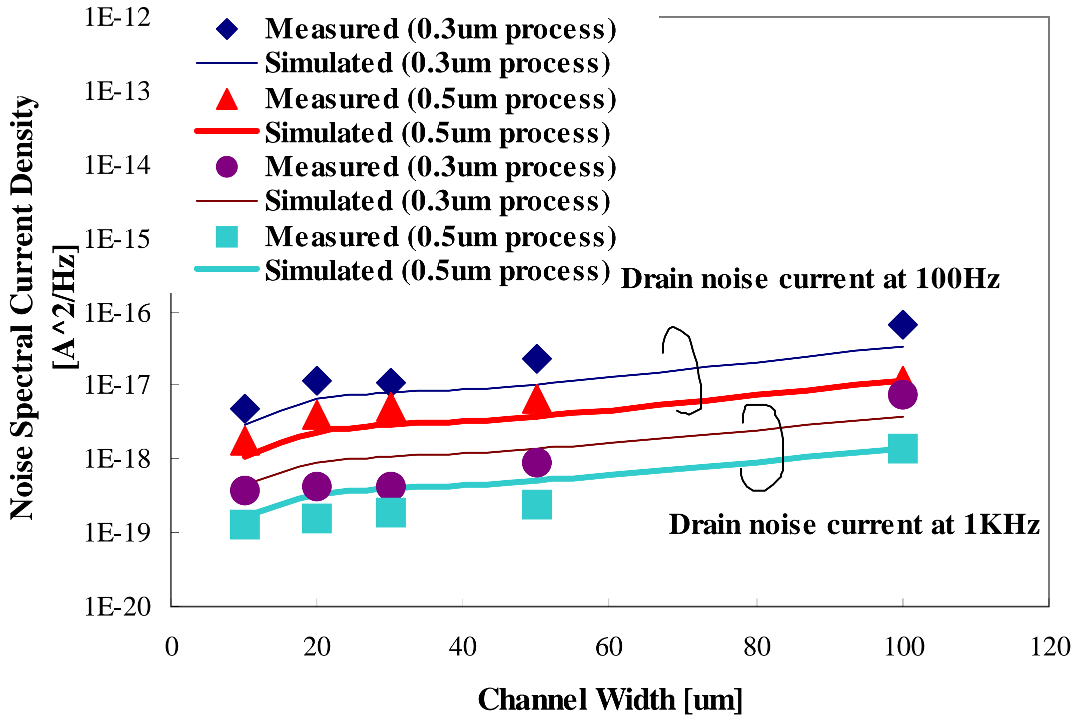


Fig. 4.20 N-MOSFETs' channel width dependencies of measured and simulated noise current density (100 Hz and 1 KHz) for constant gate voltage (V_G=1.4 V) using the 0.3 μm and 0.5μm CMOS processes. Here, the supplied drain bias is 3 V.

4.4 Conclusions

Flicker noise measurements, analysis, and modeling both for a-Si TFT's and n-channel MOSFET's were described. An automated new flicker noise measurement system has been developed using commercial measurement instruments and a specially designed interface unit. A flicker noise model and its extraction functions of a-Si TFT's were newly developed for analog switch applications. Existing bias dependent flicker noise models of n-channel MOSFET's had been modified to use it for recent deep sub-micron MOSFET's. Also, gate channel width and length dependencies of n-MOSFET's flicker noise current have been measured and analyzed using our automated 1/f noise measurement system. A new flicker noise model, which includes novel effective channel width dependency of the noise, and its extraction functions were developed. The model was verified by measuring two different process devices. These models and their analysis will be useful for today's a-Si TFT and CMOS circuit designers.

Chapter 5 Equivalent Circuit Modeling for RF Packaged Transistors

Introduction

S-parameter measurement of transistors in a high-frequency region is an effective means to evaluate their dynamic characteristics. Presently, automatic network analyzers are used widely for this purpose. Highly accurate calibrations are available even for measurement test jigs such as wafer probers and test fixtures. In reality, however, there exist parasitic elements between the test jigs and device under test. For the on-wafer measurement, bonding pad corresponds to the parasitic while the package and the lead wires are those in the packaged transistors. A calibration and compensation method in the on-wafer measurements is described by van Wijnen et al. [47]. The calibration and compensation method for packaged measurements is considered a significant problem by many engineers and no good method has been proposed in 1991. We have developed a novel model of the parasitic elements of the packaged transistor and a new de-embedding method to eliminate these parasitics. We created two dummies for de-embedding. One of them is OPEN in which the transistor is removed from the package, and another is SHORT in which all the terminals are short-circuited after the transistor is removed. S-parameters have been measured for these dummies

under the same conditions as those for the package DUT with two kinds of bipolar transistors with f_t of about 1 GHz (An Agilent 8753C network analyzer was used) and 10 GHz (An Agilent 8510 network analyzer was used). From the measured data for each case, the S-parameters of the intrinsic transistors can be obtained only by subtractions with mutual transformations of *Y* and *Z* parameters:

$$Z_t = Z(Y_{meas} - Y_{open}) - Z(Y_{short} - Y_{open}) \qquad (5.26)$$

here,

$$Y_{meas} = \begin{bmatrix} Y_{11meas} & Y_{12meas} \\ Y_{21meas} & Y_{22meas} \end{bmatrix}$$ and so on,

and

$Z(Y)$ means a transform function from Y (admittance matrix) to Z (impedance matrix). Other cases follow the same way.

where Z_t denotes the *Z* parameters for the intrinsic transistor. Also, base, collector, and emitter resistance and inductance of internal chip transistors which are located in the package have been extracted by applying the “Cold-chip Measurement method” [48] to bipolar transistors. Other non-linear model parameters could be easily extracted and optimized by using ordinal methods that are equipped in any commercial modeling software programs.

5.1 Package Parasitic Component Model

5.1.1 Calibration procedure

Especially accurate calibration is needed in the case of S-parameter measurement in RF and microwave frequency ranges. One of the methods presently used is the 12-term error-calibration method.

In this correction method, calibration models are formed for two-port and 12 terms. Twelve measurements in total are carried out in the forward and backward directions for the directivity, source match, load match, reflection frequency characteristics, transfer frequency characteristics, and isolation. These measurements must be carried out at each frequency point with short, open and through standards with known specifications. Hence, these measurements are carried out with a computer.

5.1.2 "On wafer" parasitic element model and de-embedding [47]

First of all, we will review the "On wafer" correction procedure developed by P. J. van Wijnen, et al [47].

Using the standard 12 term calibration procedure for “on wafer” S-parameter measurements all errors before bondpads can be accurately neglected. However, the bondpads capacitance and substrate resistance are still remained. The bondpads capacitance is a dominant element for S-parameter measurements. Also, substrate resistance is existing between two adjacent pondpads as shown in Fig. 5.1. In many cases all of these parasitics are in parallel with the device under test (DUT) and can be modeled with resistors and capacitances. In the frequency ranges, approximately, greater than 10 GHz, inductances and resistances on all transmission lines should be considered. However, in this paper [47] they were not mentioned because the length of transmission lines were short enough to be ignored.

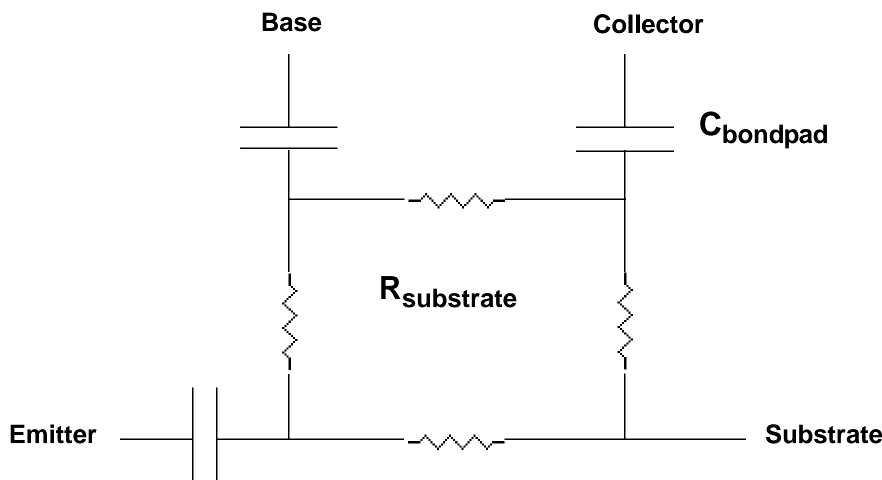


Fig. 5.1 An equivalent circuit diagram of the major parasitics on wafer.

Fig. 5.1 can be redrawn as Fig. 5.2 where substrate connected to emitter for RF applications.

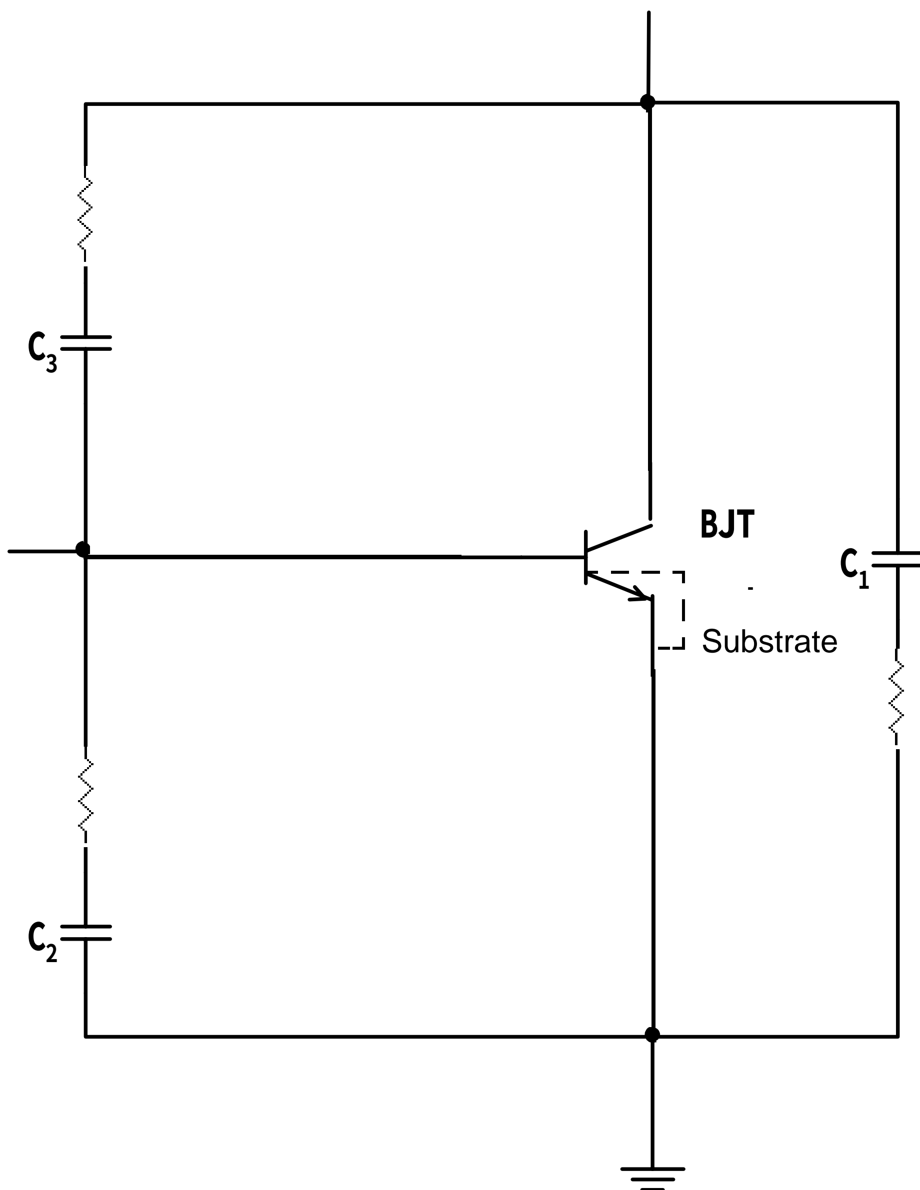


Fig. 5.2 An equivalent circuit diagram of the major parasitics for "on wafer" RF measurements.

The equivalent circuit model of is drawn as Fig. 5.3. Measured S-parameters are transformed to Y-parameters in order to subtract parasitics from measured DUT as follows:

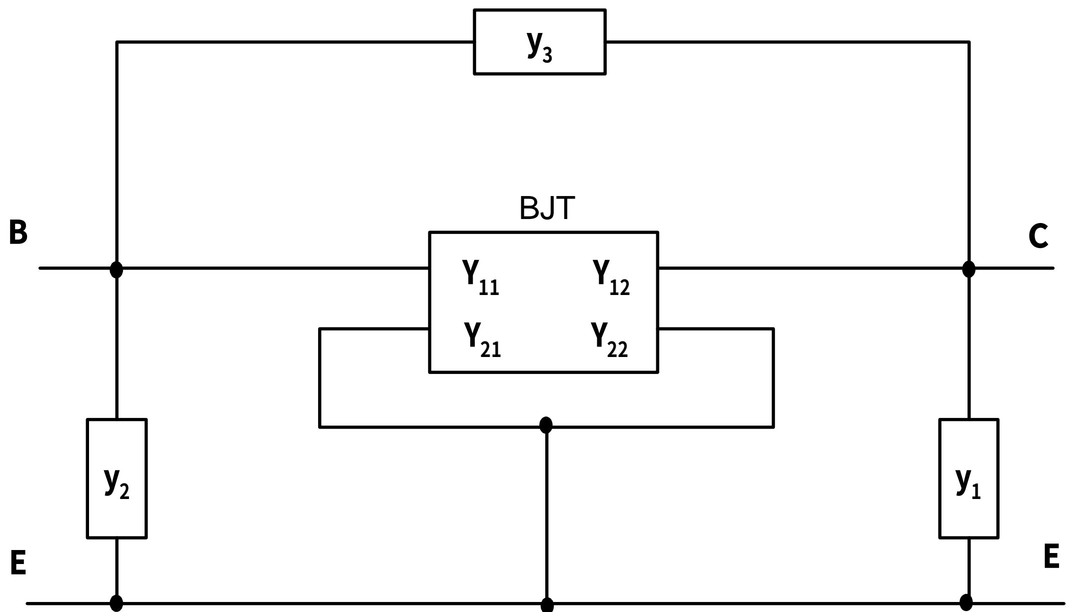


Fig. 5.3 Representation of the "On wafer" parasitic admittance branches.

Here, we fabricate a "Open pad" dummy which does not have the chip transistor. In this case only y_1, y_2, and y_3 are remained as formed of a π type circuit in Fig. 5.3. The measured Y-parameters of "Open pad" dummy are:

$$\begin{bmatrix} Y_{11d} & Y_{12d} \\ Y_{21d} & Y_{22d} \end{bmatrix} = \begin{bmatrix} y_2 + y_3 & -y_3 \\ -y_3 & y_3 + y_1 \end{bmatrix} \quad (5.27)$$

The measured Y-parameters of the DUT are:

$$\begin{bmatrix} Y_{11m} & Y_{12m} \\ Y_{21m} & Y_{22m} \end{bmatrix} = \begin{bmatrix} y_2 + y_3 + Y_{11} & -(y_3 + Y_{12}) \\ -(y_3 + Y_{21}) & y_3 + y_1 + Y_{22} \end{bmatrix} \quad (5.28)$$

The corrected Y-parameters which represent Y-parameters of the intrinsic chip transistor are:

$$\begin{bmatrix} Y_{11t} & Y_{12t} \\ Y_{21t} & Y_{22t} \end{bmatrix} = \begin{bmatrix} Y_{11m} - Y_{11d} & Y_{12m} - Y_{12d} \\ Y_{21m} - Y_{21d} & Y_{22m} - Y_{22d} \end{bmatrix} \quad (5.29)$$

The authors [47] verified the theory with some measurement at the frequency ranges from 45 MHz to 18 GHz.

5.1.3 Package parasitic element model

In order to model packaged transistors additional parasitic elements should be considered. There are many kinds of packages used for several purposes. We focus only on relatively simple packages such as TO cans, mini-mold, super-mini-mold, and co-planer types. The parasitic elements of these types consist of stray capacitance of external packages and induc-

tance and resistance of bonding wires. The equivalent circuit is shown in Fig. 5.4.

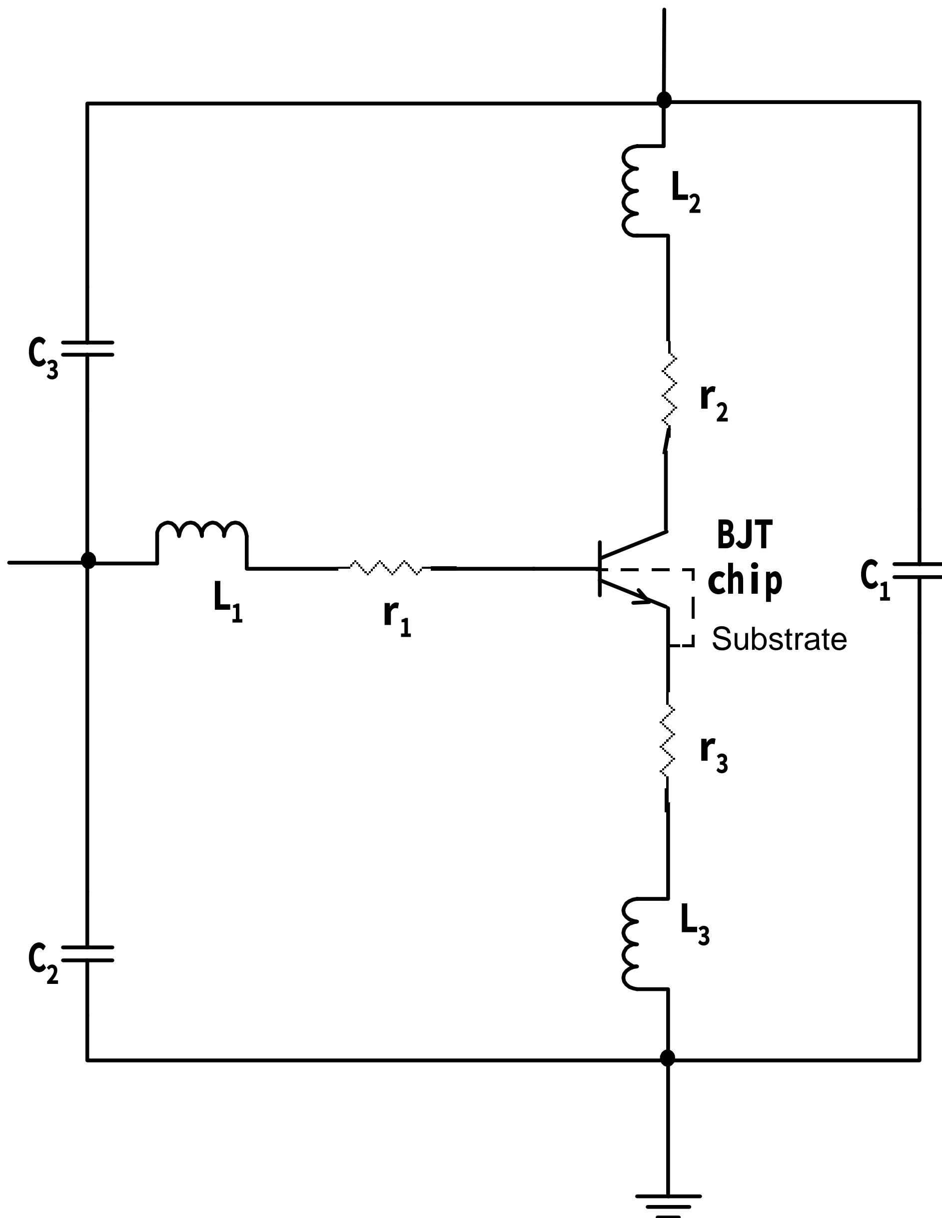


Fig. 5.4 Parasitic components model for packaged transistor.

In this model, C_1~C_3 are the capacitances between terminals due to the package while L_1~L_3 are the inductance components of the lead wires, and r_1 ~r_3 are the resistance components. Since the frequency range used for the BJT device is low (~ 1 GHz), capacitance of package parasitics is much larger than bonding pads' which are existing on the BJT chip. Therefore, bonding pads capacitance is not included in the model.

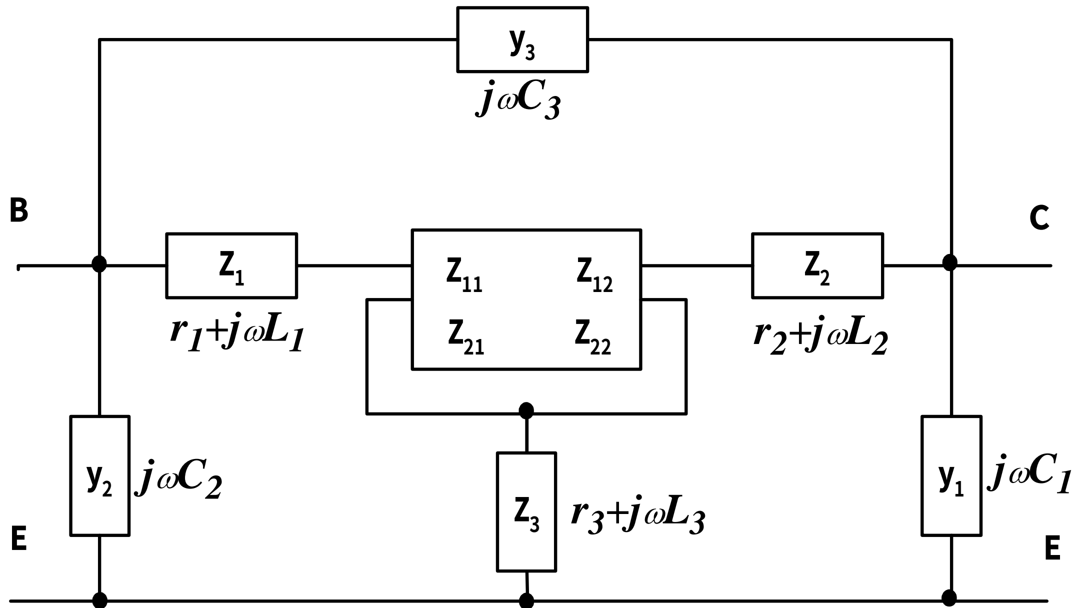


Fig. 5.5 Representation of the packaged admittance and impedance with the device.

In this case, since we need to treat not only for Y parameters but also for Z parameters to de-embed parasitics, more complicated calculation process than "on wafer" correction procedure is needed to transform Y to Z and Z to Y parameters. When the model in Fig. 5.4 is expressed in terms of *Z* and *Y* parameters, Fig. 5.5 is obtained. Next, the package less device (Open)

becomes a π network while the situation in which the interior of the package is short-circuited (Short) is expressed in terms of a composite of it and T networks. The Open package used here makes use of the one identical to that used as the transistor package. A bonding wire with an identical length attached to the bonding pad is floating. In the Short package, bonding wires are placed in a floating situation to form a short-circuit condition in the same package. S-parameters were measured for several lengths of bonding wires (in the Open package). The obtained data changed very little at this frequency range. Hence, in this paper, the parasitic capacitance components of the bonding wires (less than 3 fF) are neglected.

In the Open package, Y_{11} element is

$$y_1 + y_3 = j\omega(C_1 + C_3) \quad (5.30)$$

while Y_{11} element in the Short package is

$$y_2 + y_3 + Y_{11S} = j\omega(C_2 + C_3) + \frac{Z_2 + Z_3}{|Z|} \quad (5.31)$$

where

$$Z_2 + Z_3 = (r_2 + r_3) + j\omega(L_2 + L_3) = A + j\omega B \quad (5.32)$$

For simplicity, let the real part of $|Z|$ be C and the imaginary part be D. Then

$$\frac{Z_2 + Z_3}{|Z|} = \frac{AC + \omega^2 BD}{C^2 + \omega^2 D^2} + j\omega \frac{BC - AD}{C^2 + \omega^2 D^2}, \tag{5.33}$$

which is a positive real function. Similarly, the Y_{11} element of the transistor package is also a positive real function. From the foregoing, Y to Z and Z to Y transformation and additional subtraction between the matrices become possible. Y parameters of open and short package are calculated based on Fig. 5.6 and Fig. 5.7.

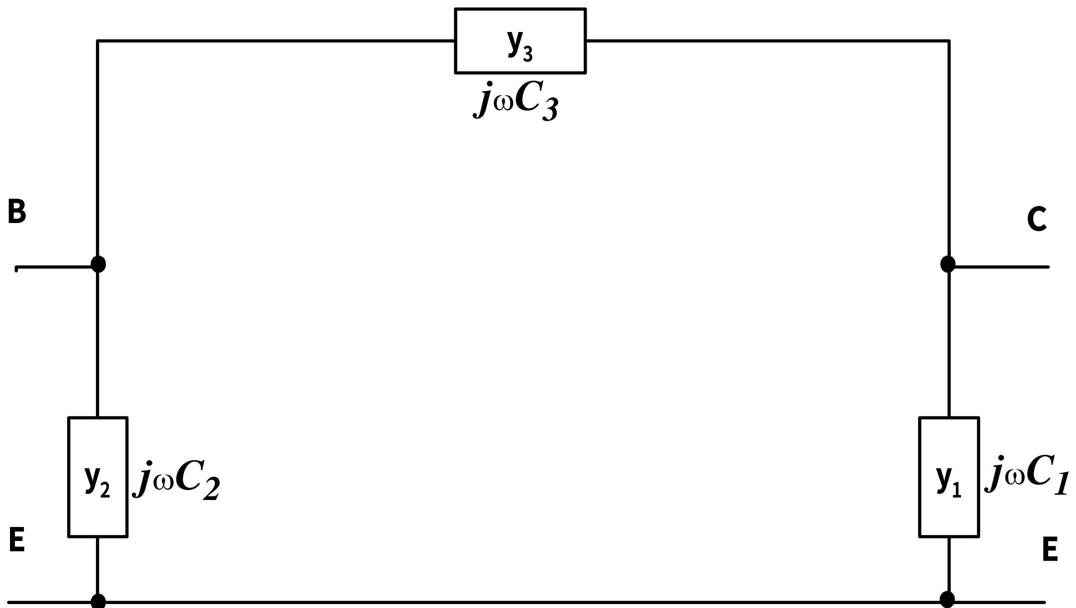


Fig. 5.6 Representation of the open package in admittance and impedance parameters.

Open package

$$Y_{open} = \begin{bmatrix} y_2 + y_3 & -y_3 \\ -y_3 & y_3 + y_1 \end{bmatrix} \tag{5.34}$$

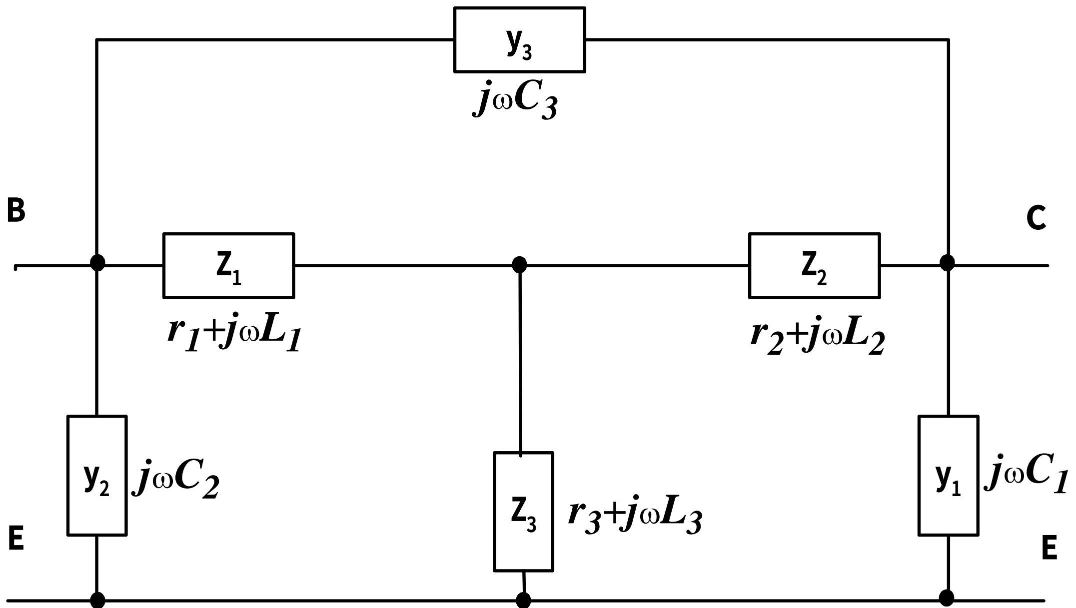


Fig. 5.7 Representation of the short package in admittance and impedance parameters.

Short package

$$Y_{short} = \begin{bmatrix} y_2 + y_3 + Y_{11S} & -y_3 - Y_{12S} \\ -y_3 - Y_{21S} & y_3 + y_1 + Y_{22S} \end{bmatrix} \tag{5.35}$$

where Y_{11s}~Y_{22s} indicate the Y parameters in the case where the T network of Z_1~Z_3 is transformed to a π network. Y_{11M}~Y_{22M} are Y parameters converted from the Z parameters of the transistor containing Z_1~Z_3.

The Y parameters needed in (5.35) are Y_{11S}, $-Y_{12S}$, $-Y_{21S}$, and Y_{22S}.They can be obtained by subtracting the Y parameters of the Open package from those of the Short package. Similarly, in (5.36), Y_{11M}, $-Y_{12M}$, $-Y_{21M}$ and Y_{22M} need to be derived. Hence, the Y parameters of the Open package are subtracted from those of the Short package:

$$Y_{ijS} = Y_{short} - Y_{open} \qquad (5.36)$$

$$Y_{ijM} = Y_{meas} - Y_{open} . \qquad (5.37)$$

$(i, j: 1,..., 2)$

Next, when Y_{ijS} and Y_{ijM} are computed by transforming them back to Z parameters,

$$Z_{ijS} = \begin{bmatrix} z_1 + z_3 & z_3 \\ z_3 & z_3 + z_2 \end{bmatrix} \qquad (5.38)$$

$$Z_{ijM} = \begin{bmatrix} z_1 + z_3 + Z_{11t} & z_3 + Z_{12t} \\ z_3 + Z_{21t} & z_3 + z_2 + Z_{22t} \end{bmatrix} \qquad (5.39)$$

Since the parameters needed in (5.39) are Z_{11t}, Z_{12t}, Z_{21t}, and Z_{22t}, they can be obtained by subtraction of (5.38) from (5.39):

$$Z_{ij} = Z_{ijM} - Z_{ijS} . \quad (5.40)$$

As a result, only the Z parameters of the transistor itself in the package remain. When the foregoing is expressed in terms of a conceptual equation, (5.26) is obtained.

5.3 Parasitic Elements Calculations of an Intrinsic Chip BJT

As described in sub-section 5.1.3, the model and its model parameters of the package parasitics could be calculated, therefore, be de-embedded. Next step is to extract parasitic resistance and inductance at base, collector, and emitter in the BJT chip device.

A small measurement technique called “Cold-chip measurement” in [48] can be applied for extracting series resistance and inductance of BJT.

Cold-chip measurement

The method uses small signal measurements, with the dc value of drain-to-source voltage set to zero and gate-to-source voltage set to a value larger than the Schottky barrier height in a GaAs MESFET. Two port measurements are then taken at increasing gate-to-source biases. The method does not require that channel resistance or diode resistance be evaluated or that excessive values of gate current be used in the measurements.

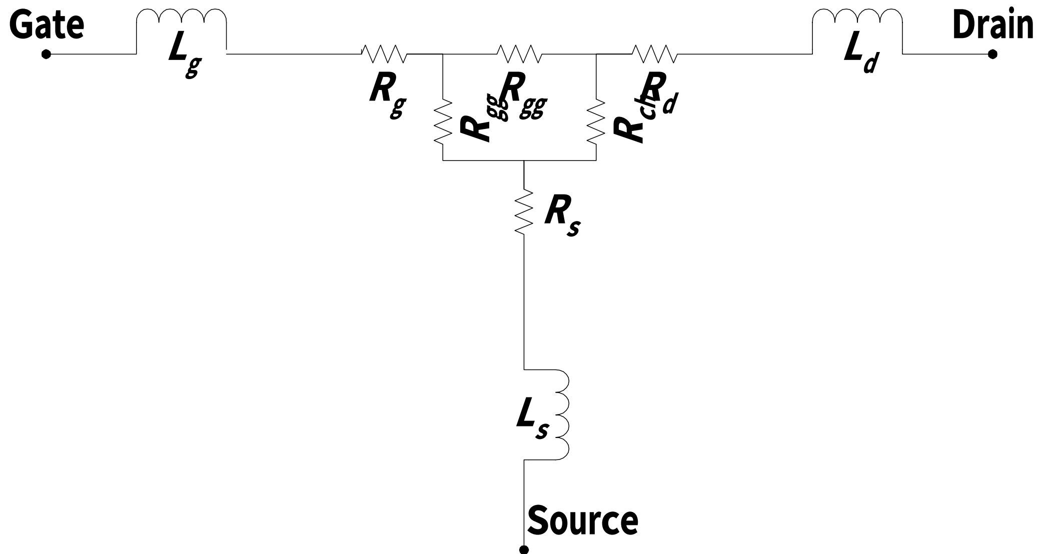


Fig. 5.8 Small signal model of a MESFET with "Cold-chip" biasing.

Fig. 5.8 shows the intrinsic distributed gate region of the forward-biased FET with only three resistors. The forward bias applied at the gate-to-source and gate-to-drain junctions eliminates the device capacitances gate-to-source capacitance, C_{gs} and gate-to-drain capacitance, C_{gd} from the measurements. Where R_{ch} is the channel resistance and R_{gg} is the diode resistance of the Schottky junction. The model can be applied to both GaAs MESFET's and HEMT's. Once the equivalent circuit is made, every components are easily calculated by using Z parameter and type T equivalent circuit formulation.

Series parasitics extraction by applying "Cold-chip measurement"

We apply large current to the base in order to expand base width to prevent base width modulation. Hence, the current will be divided into two other terminals which are collector and emitter. The equivalent circuit of this chip transistor can be represented as a type T circuit in Fig. 5.9.

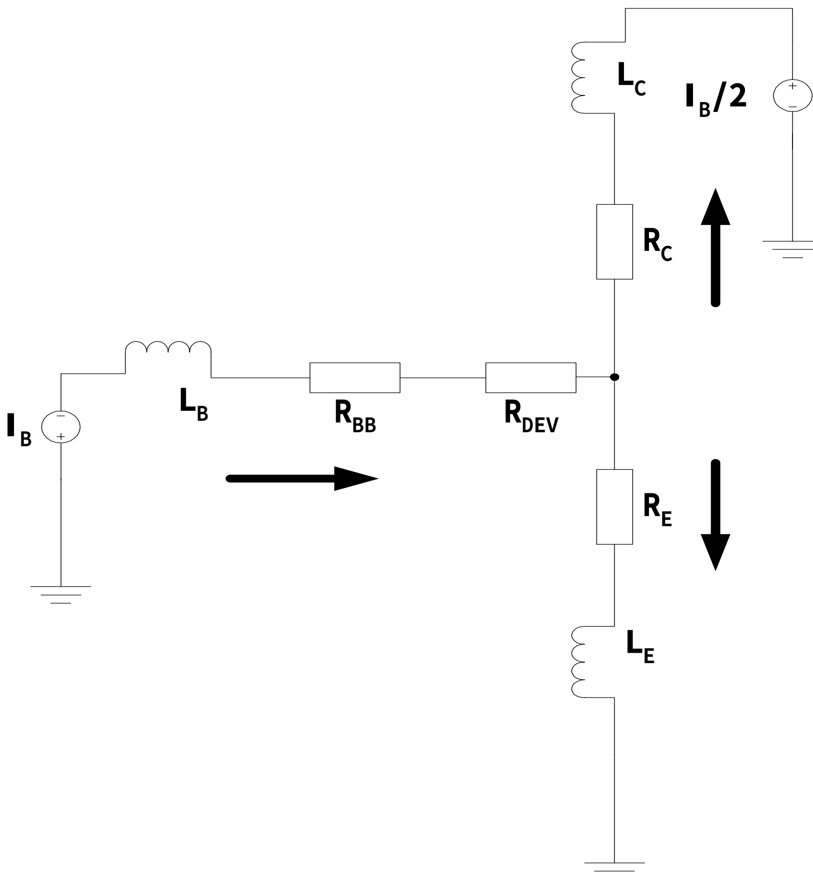


Fig. 5.9 The equivalent circuit of the chip BJT using the "Cold-chip measurement" method.

1. R_{DEV} extraction

The intrinsic part of the chip BJT can be represented as a resistance, R_{DEV}, in this bias condition as shown in Fig. 5.9. To extract R_{DEV} total base, base-collector, and base-emitter current at any constant bias voltage should be accurately calculated. The base-collector and base-emitter current are derived by using a large signal model. In this research we will use BJT Gummel-Poon model [51]. As shown in Fig. 5.10, R_{DEV} is further divided to two parallel resistance, R_{DC} and R_{DE}.

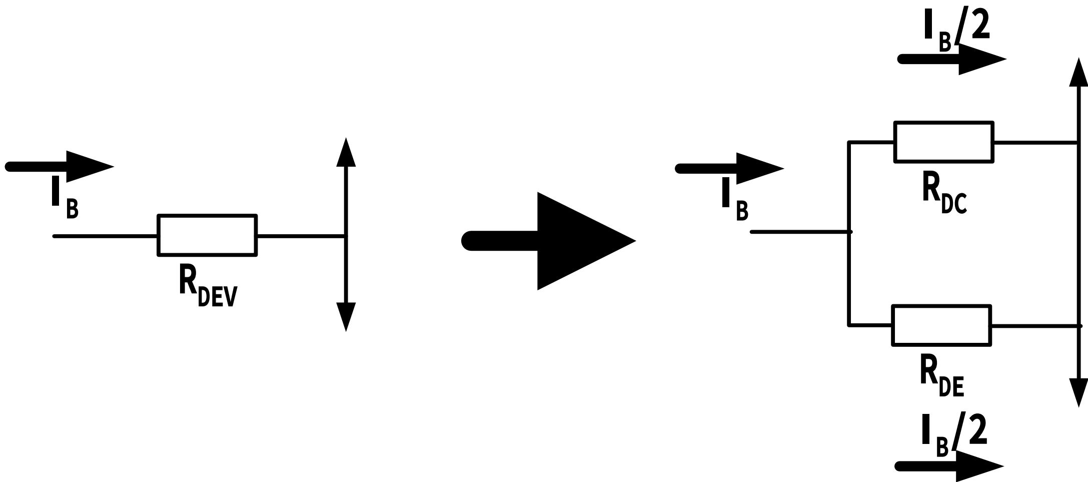


Fig. 5.10 An equivalent circuit of R_{DEV}.

R_{DE} can be calculated by

$$R_{DE} = \left(\frac{\partial I_B}{\partial(2 \cdot V_D)}\right)^{-1} \quad (5.41)$$

$$= \left(\frac{\partial((I_S/B_F) \cdot (e^{V_D/(N_F \cdot v_t)} - 1))}{\partial V_D}\right)^{-1} \quad (5.42)$$

$$= \frac{2 \cdot N_F \cdot v_t}{I_B} . \quad (5.43)$$

In the same manner R_{DC} is calculated by

$$R_{DC} = \frac{2 \cdot N_R \cdot v_t}{I_B} . \quad (5.44)$$

Therefore, R_{DEV} is finally derived by

$$R_{DEV} = \left(\frac{1}{R_{DE}} + \frac{1}{R_{DC}}\right)^{-1} \quad (5.45)$$

$$= \frac{2 \cdot v_t}{I_B} \cdot \left(\frac{1}{N_F} + \frac{1}{N_R}\right)^{-1} . \quad (5.46)$$

Here, I_S is the saturation current, B_F is the maximum forward current gain, N_F is the forward diode's ideal factor, N_R is the reverse diode's ideal factor, and v_t is the thermal threshold voltage. They are all model parameters for BJT Gummel-Poon model. The meaning and extraction method of each forward model parameter can be found in Fig. 5.11. Also, N_R can be easily extracted by using reverse Gummel-plot as described in [49].

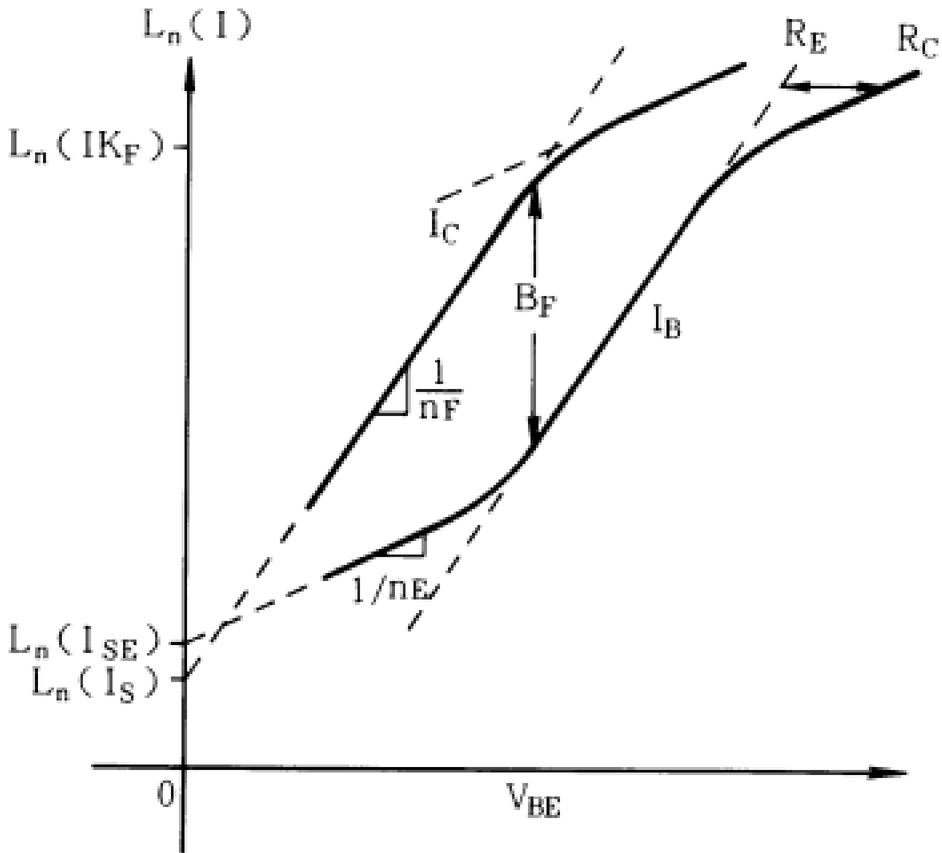


Fig. 5.11 Forward Gummel-Poon model parameters extraction by using forward Gummel-plot.

2. L_E, L_C, L_B, R_E, R_C, R_{BB} extractions

Emitter, collector, and base inductors (L_E, L_C, L_B) represent transmission line inductance. Emitter and collector resistors (R_E, R_C) are transmission line resistance. In the same manner R_{BB} represents variable resistor which is

caused by the base width modulation. However, in this small signal model R_{BB} is treated as a constant resistor.

S-parameters are measured by using the Cold-chip measurement bias condition. As the equivalent circuit of the Cold-chip measurement condition which is shown in Fig. 5.9 is drawn as type *T* circuit, each parameter can be calculated from *Z*-parameters. If we focus on packaged type BJT whose equivalent circuit shows in Fig. 5.4, all inductance and resistance (L_1, L_2, L_3, r_1, r_2, r_3) should be de-embedded from the measured *S*-parameters. The transformed *Z*-parameters are written as

$$\begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} = \begin{bmatrix} R_{BB} + R_{DEV} + R_E + j\omega(L_E + L_B) & R_E + j\omega L_E \\ R_E + j\omega L_E & R_C + R_E + j\omega(L_E + L_C) \end{bmatrix} . \tag{5.47}$$

Resistance and inductance are calculated from (5.47) as

$$L_E = Im(Z_{12})/\omega , \tag{5.48}$$

$$L_B = Im(Z_{11})/\omega - L_E , \tag{5.49}$$

$$L_C = Im(Z_{22})/\omega - L_E , \tag{5.50}$$

$$R_E = Re(Z_{12}) , \tag{5.51}$$

$$R_C = Re(Z_{22}) - R_E , \tag{5.52}$$

$$R_{BB} = Re(Z_{11}) - R_E - R_{DEV} . \tag{5.53}$$

5.4 Experiments

The theory in the previous sections was used in characterization software (Agilent TECAP, which is a Transistor Electrical Characterization and Analysis Program and Agilent IC-CAP, which is an Integrated Circuits-Characterization and Analysis Program) that were confirmed by measurement on an Agilent 8753C and an Agilent 8510C with a computer. The first experiment is to verify only the package parasitic de-embedding for TO can packaged BJT's using a low f_t (*ft*~1GHz) BJT with TECAP and 8753C. The next is to verify the package parasitic de-embedding and on-chip parasitic elements calculations using Cold-chip measurement for Super-Mini-mold type BJT's using a high f_t (*ft*~10GHz) BJT with IC-CAP and 8510C.

5.4.1 Low frequency TO-CAN package BJT modeling

The f_t of CAN packages are relatively lower (less than 2 GHz) than that of mold and strip line type fixtures. In this research we adopted a TO-12 can package BJT device to verify the Open/Short de-embedding technique described in 5.1.3.

Test fixture design for TO can package BJT's

As shown in Fig. 5.12 three types of test packages are needed for the de-embedding procedure. There are three TO can packages that have the same sizes and dimensions. The bonding wires in Short and Test device packages should have the same length at each terminal position in order to keep lead line and bonding wire parasitic condition.

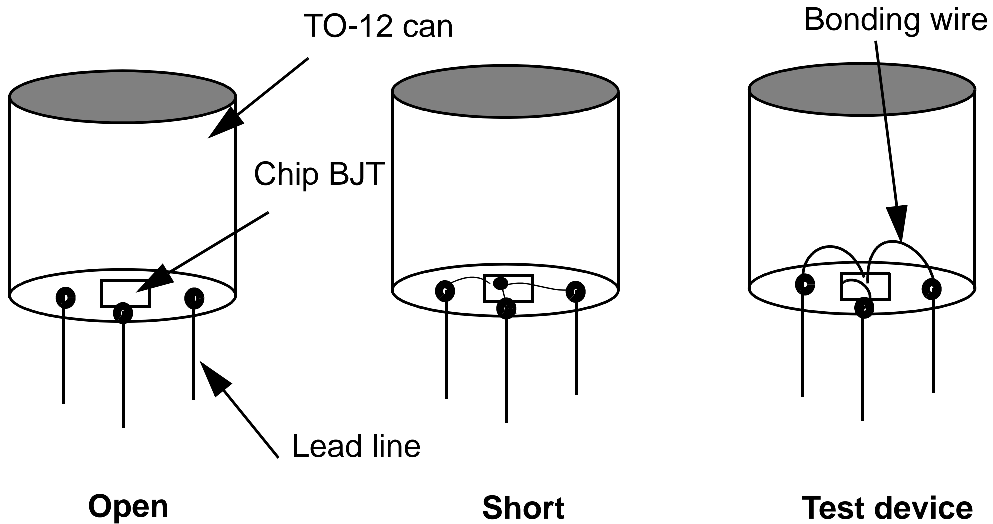


Fig. 5.12 Open/Short and test packages for de-embedding.

AC current gain measurement

The measurement conditions of the experiment are such that a bias of 750 mV is applied between the base and the emitter with an ac signal of -5 dBm applied between the base and the emitter while the output signal between the collector and the emitter is extracted via a 15 dB attenuator. All operations except bias application are carried out inside the Agilent 8753C.

From $Z\ (Y_{short} - Y_{open})$, we obtained r_1, r_2, r_3, L_1, L_2, and L_3. From the value of Y_{open}, we obtained C_1, C_2, and C_3 and the results are compared from a low frequency (f = 1 MHz) to a high frequency (f = 1 GHz). The errors were several ohms in r_1, r_2, and r_3 while they are about 200 μH in L_1, L_2, and L_3 and are about 50 fF in C_1, C_2, and C_3. Hence, the average values over the entire frequency points are used in the simulation in Fig. 5.14. Also, the model for the transistor itself in the simulation was the Gummel-Poon model in UCB SPICE2G.7. The model parameters are listed in Table. In addition to measurement of the H-parameters after compensation, DC/CV measurement was carried out so that the parameters extracted and optimized from the measured data are used and a SPICE simulation was performed.

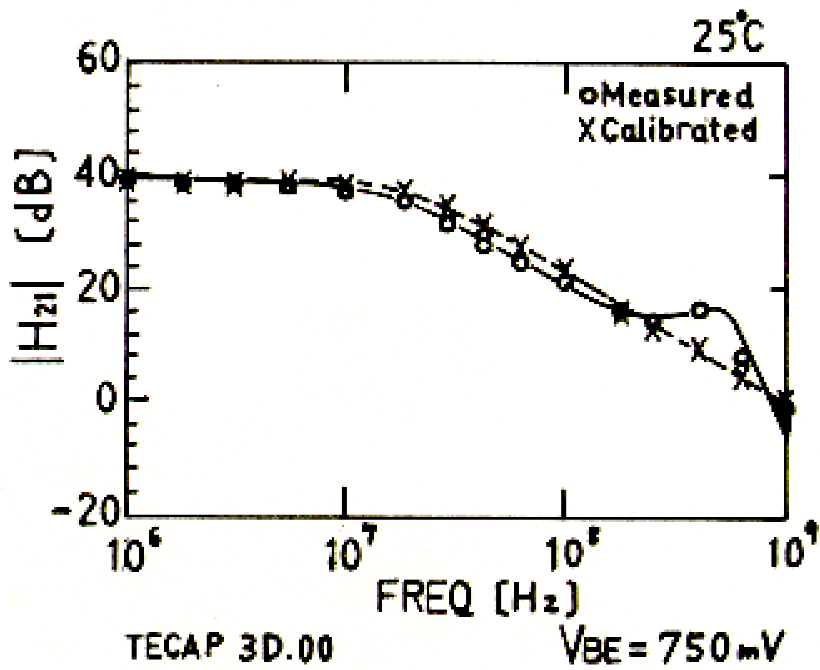


Fig. 5.13 *H21* vs. frequency measurement curve of packaged transistor and corrected curve using the method.

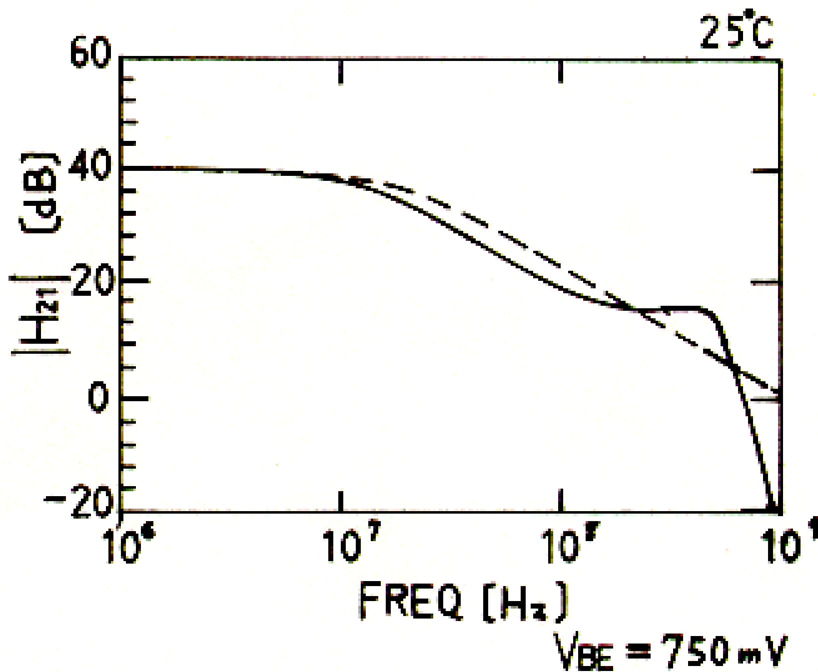


Fig. 5.14 SPICE simulation data for comparing the pure transistor result with parasitic model (Fig. 5.4) result. The transistor model parameters are extracted by TECAP. Capacitances are calculated by using Y_{open} and inductances and resistances are calculated by using $Z\,(Y_{short} - Y_{open})$.

When the measured data in Fig. 5.13 are compared with the SPICE simulation results with the model in Fig. 5.4 as shown in Fig. 5.14, it is found that there is a resonance of the *L* components of the lead wire and the bonding wire with the *C* component of the package at about 500 MHz. The values of this resonant frequency f_0 almost coincide on Fig. 5.13 and Fig. 5.14. Also, in the data in Fig. 5.13 after correction, $|H_{21}|$ decreases at a slope of 6 dB/Oct. from the -3 dB point to the point at 1 GHz so that the basic characteristics of

a bipolar transistor are revealed faithfully. From the foregoing, it is found that the model in Fig. 5.4 can be used in the frequency range from 1 MHz to 1 GHz and the calibration method in this paper is practical.

In addition to the SPICE model parameters of the transistor, transition frequency, f_t and the maximum frequency of oscillation, f_{max} are important parameters for device and circuit design. From the fact that $|H_{21}|$ decreases at 6 dB/Oct. from the -3 dB point on the $|H_{21}|$ vs. frequency characteristic, f_t can be extrapolated from the value at an arbitrary point since the slope on the logarithmic axes (in both *X* and *Y* axes) is -1. Also, f_{max} can be obtained by a method identical to the one for f_t, by computing the unilateral gain from the *S*-parameters. This implies that *S*-parameters measurement must be carried out up to only one-fifth to one-third frequency of f_t. A similar argument holds in the extraction of the SPICE model parameters. Hence, from the measurement following the present procedure, evaluation of the transistors with f_t = 3 ~ 5 GHz is considered possible. It can be estimated easily that the method is effective also for the FET's.

5.4.2 High frequency Super mini-mold package BJT modeling

In this section a higher frequency (f_t ~ 10 GHz) Super Mini-mold packaged BJT than the TO can packaged BJT is adopted to verify Cold-chip measure-

ment [48] method for extracting on-chip parasitics in addition to the Open/ Short de-embedding technique. As an advanced experiment, BJT Gummel-Poon dc model (which is a large signal model) parameters are additionally extracted and used for the final result simulations in order to observe the effectiveness of this research.

Test fixture design for Super-mini-mold type BJT's

At RF frequencies the test fixture should be designed on 50 Ω transmission lines. Also, the signal lines should be formed by any waveguide to avoid wire loss and power radiations. In this experiment we adopted coplanar waveguide which microwave wafer prober can handle it without any difficulty.

Fig. 5.15 shows the test fixture design structure for Super-mini-mold package BJT's. A transistor chip will be mounted on the center island that is drawn as a square shape. Only the collector terminal of the transistor chip is contacted on the metal signal line. The base is connected to the other side through a bonding wire. The emitter is connected to both of two ground metals that are located on upper and lower sides. Therefore, the Ground-Signal-Ground microwave prober can be contacted from both sides with this test fixture.

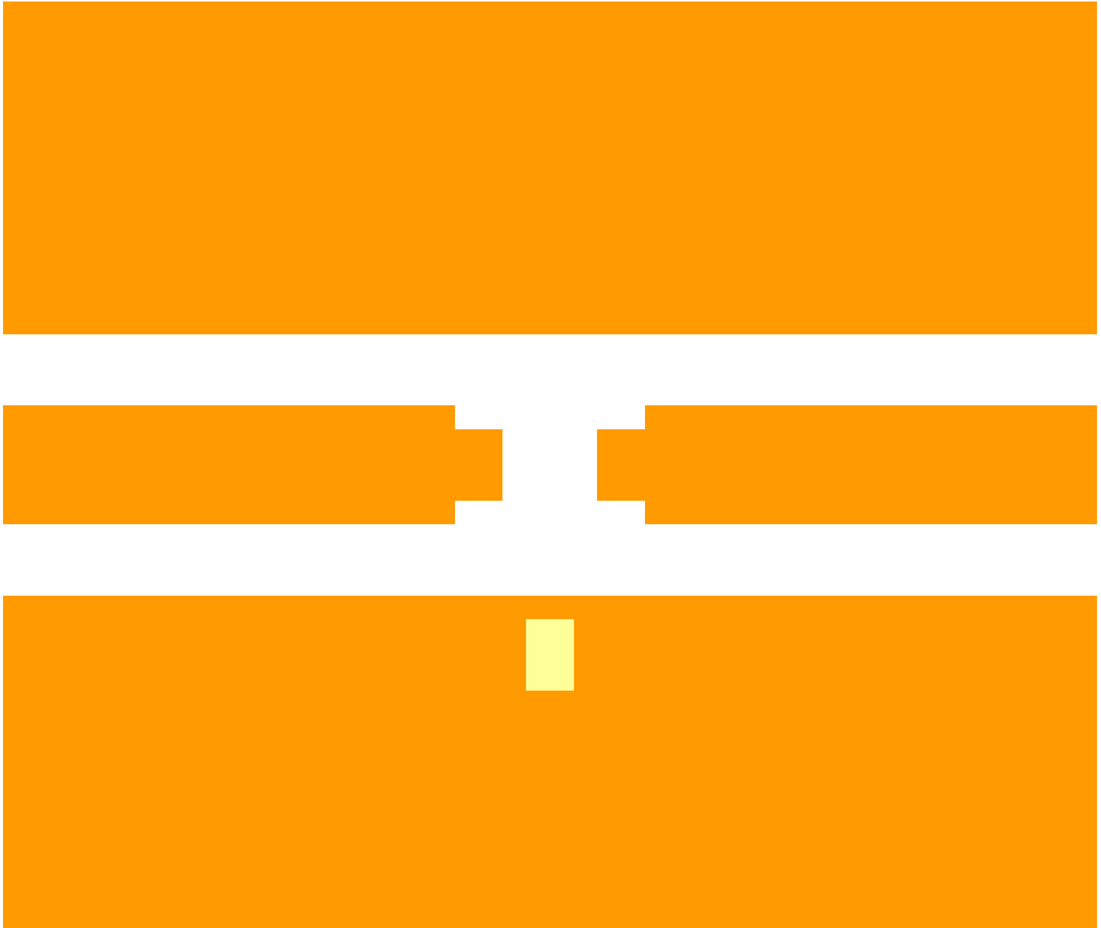


Fig. 5.15 Test fixture for Super-mini-mold packaged BJT measurement.

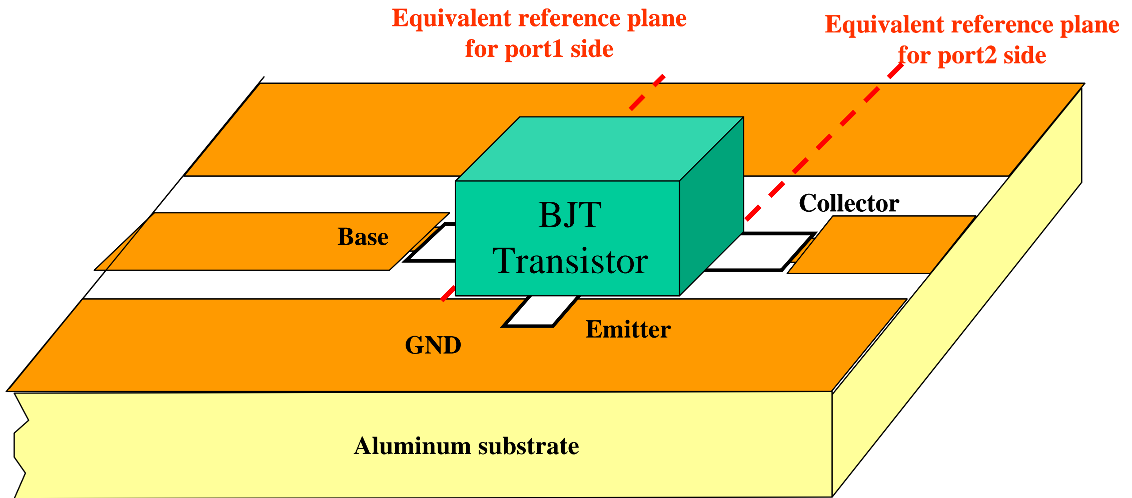
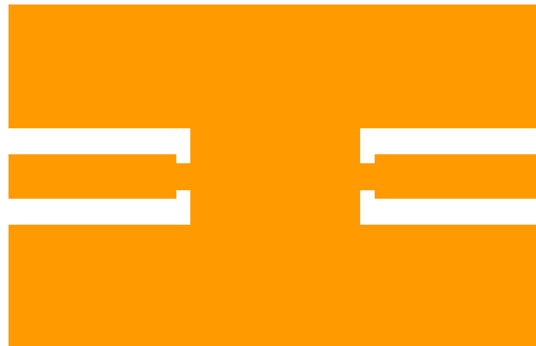


Fig. 5.16 Illustration of Super-mini-mold transistor on the test fixture.

Fig. 5.17 shows the correction standards for the test fixture in Fig. 5.15. In order to use the Open/Short de-embedding technique we have to prepare, at least, two correction standards as mentioned in 5.1.3. Open and Short correction standards are needed at ① and ② in Fig. 5.17 because the measurement reference plane should be moved from the probing point at each side to the point where the BJT chip is mounted.

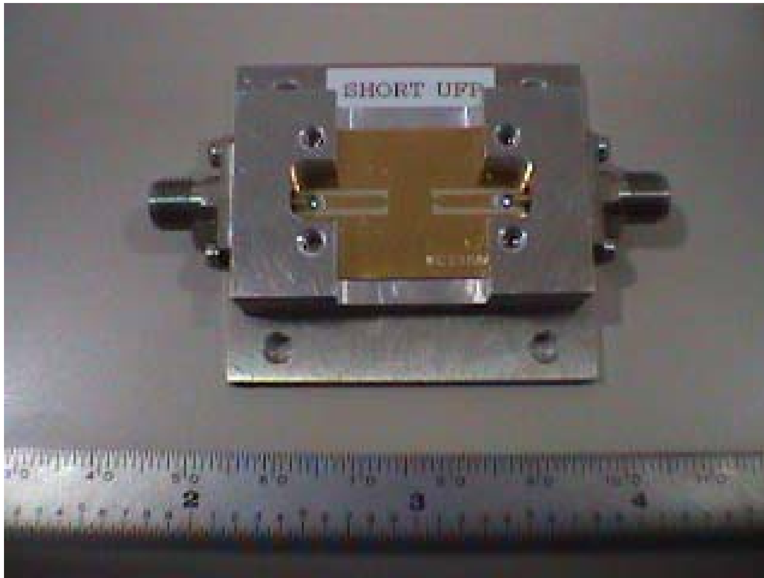
Open


Short

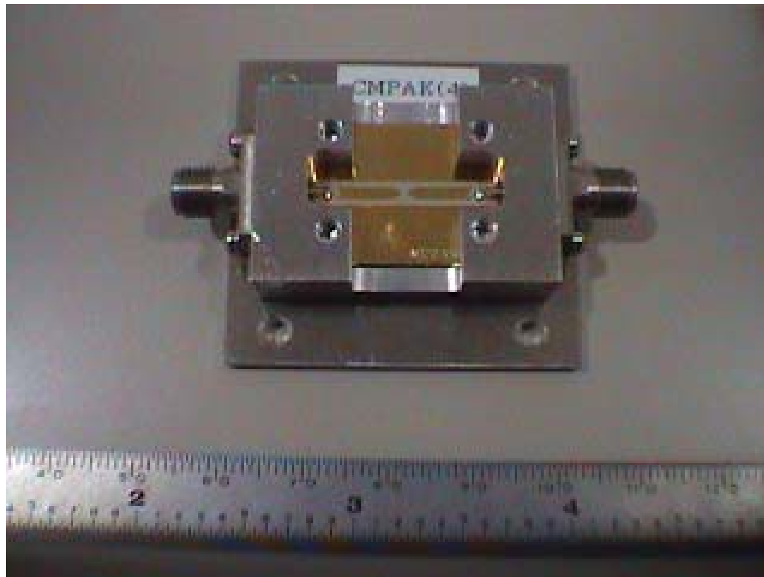
Thru

Fig. 5.17 Open, Short, and Thru correction patterns.

Fig. 5.18 is a photo of the fabricated test fixture and Short correction standard. Open and Thru standards are similarly fabricated. The Thru pattern is used to verify transmission characteristic after the correction procedure is completed.



Short



Test Fixture

Fig. 5.18 Fabricated correction Short standard and the test fixture.

Using the test fixture and correction standards a Super-mini-mold packaged BJT has been measured and de-embedded. Since the BJT is for high frequencies (f_t ~ 10 GHz), the Cold-chip measurement is also used for extracting on-chip parasitic.

Measurement and extractions

Measurement and extraction procedure for Super-mini-mold packaged BJT using the correction standards and the test fixture is as follows:

1. Calibrate network analyzer measurement system including coaxial cables, S-parameter test set, and connectors using 12 term error correction (SOLT) functions.

2. Measure *S*-parameters of the Open standards that are fabricated previously, then transform them to *Y*-parameters.

3. Measure *S*-parameters of the Short standards that are fabricated previously, then transform them to *Y*-parameters.

4. Measure *S*-parameters of the packaged BJT on the test fixture which was fabricated previously, then transform them to *Y*-parameters.

5. Define all equivalent circuits including package and internal chip BJT parasitics with BJT Gummel-Poon model.

6. Using the method described in 5.1.3 perform de-embedding procedure with step 1, step 2, and step 3.

7. Using the Cold-chip measurement described in 5.3 extract all parasitic inductance, capacitance, and resistance elements in the Super-mini-mold BJT.

8. Extract and optimize dc model parameters of BJT Gummel-Poon model.

5.4.2.1 Open standard measurement and simulation

The Open standard that we fabricated has been measured and converted from *S*-parameters to capacitance as shown in Fig. 5.19.

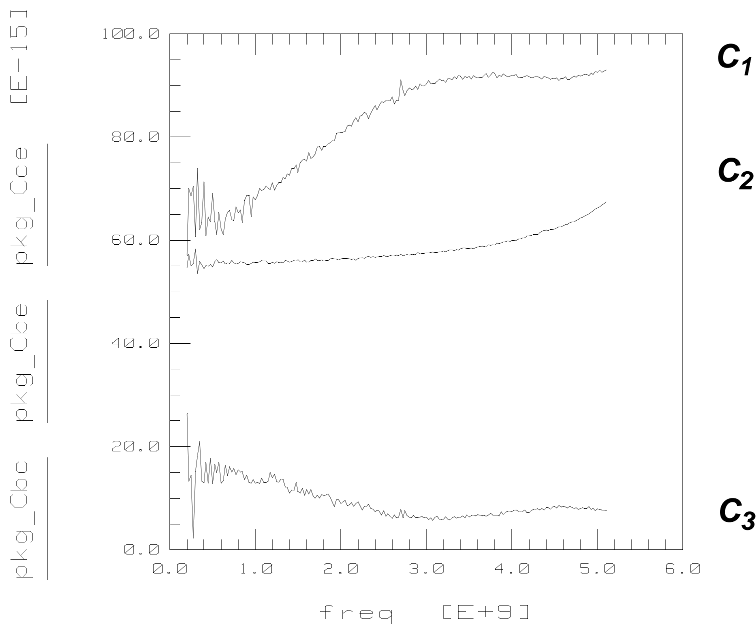
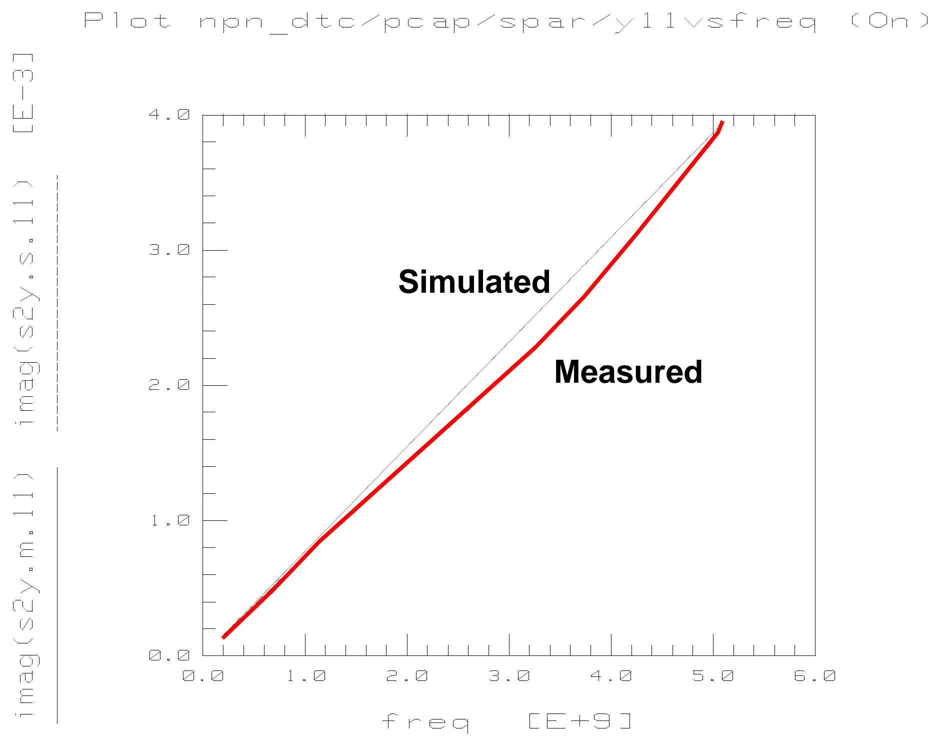


Fig. 5.19 Frequency characteristic of measured package parasitic capacitance.

If there is no other parasitic on the package, the capacitance value should be the same in all frequencies. However, surface leakage currents flow on the package. Therefore, very small amounts of inductance elements are existing. The result capacitance was not constant at each frequency. To simulate the Open standard we adopted the averaged capacitance from 3 GHz to 4 GHz because the frequency characteristic of capacitance was stable. Using the same method S_{11} and S_{22} comparisons are shown in Fig. 5.20 and Fig. 5.21.



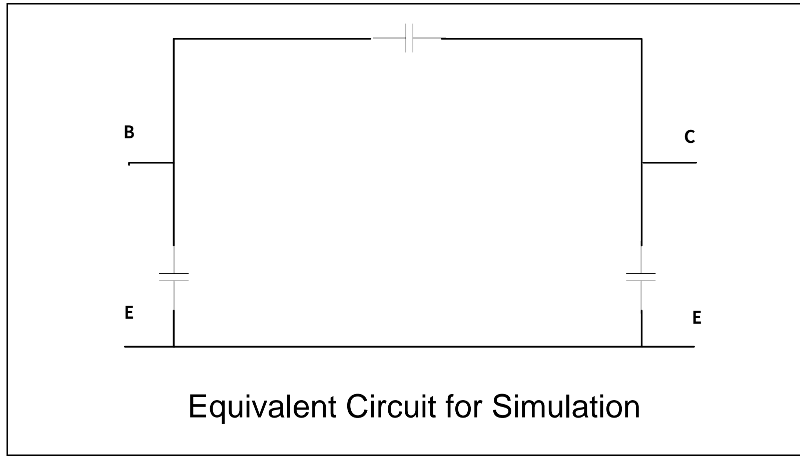


Fig. 5.20 Y11 measurement (Red line) and simulation (Black line). Measured data was obtained from Open package TEG in Fig. 5.15. The parasitic capacitance of the open package equivalent circuit was calculated by using measured Y-parameters with equation in section 5.2. The frequency ranges for the measurement and the simulation are from 200 MHz to 5.1 GHz.

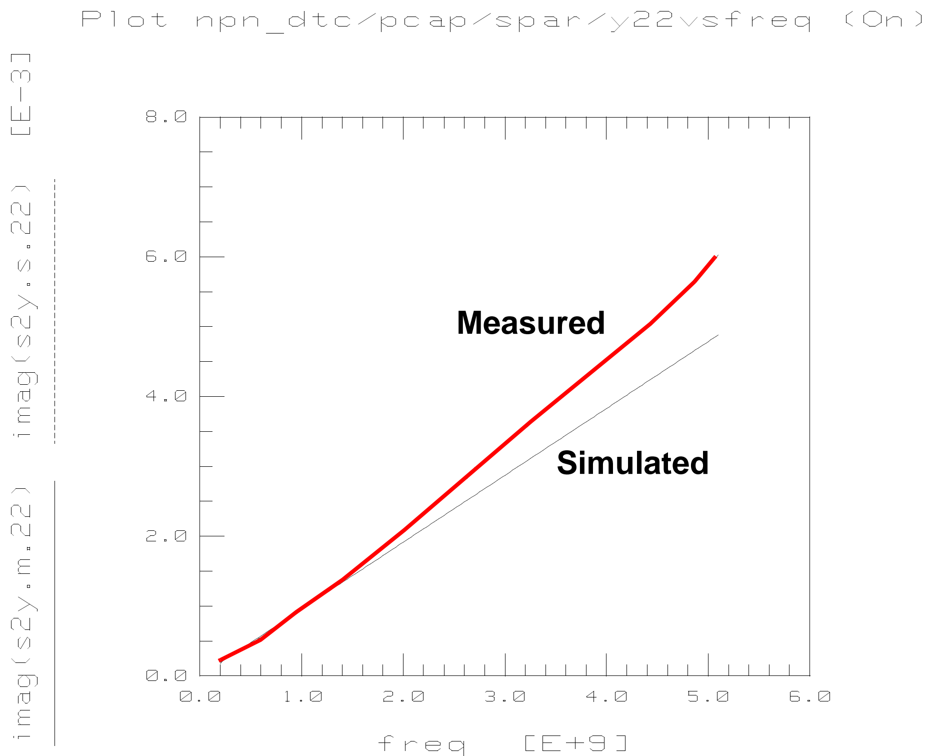
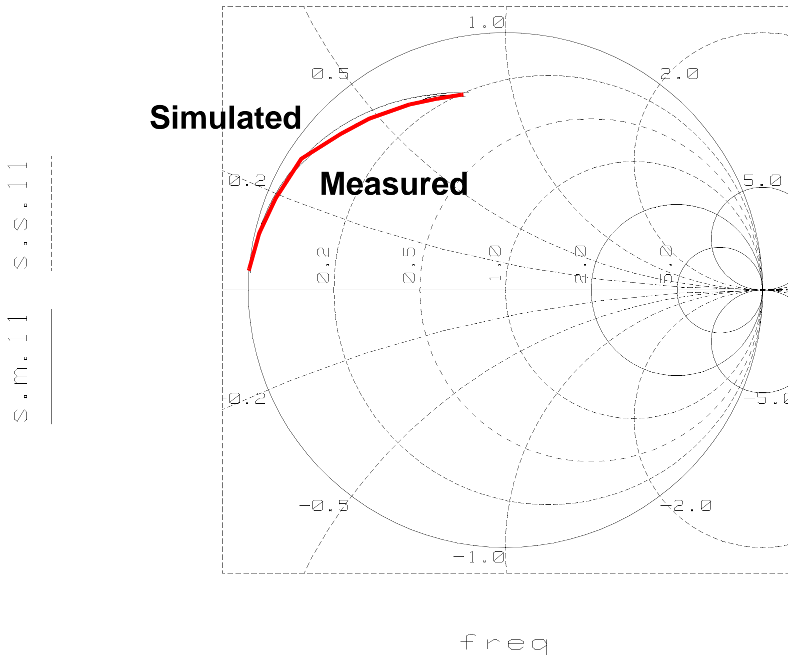


Fig. 5.21 Y_{22} measurement (Red line) and simulation (Black line). Conditions are the same as previous figure.

5.4.2.2 Short standard measurement and simulation

The *S*-parameters of the short standard, whose equivalent circuit is represented by the combination of type *T* and π, was measured and simulated by calculating parasitic components. The verifications of the short standard model are shown in Fig. 5.22, Fig. 5.23, and Fig. 5.24.



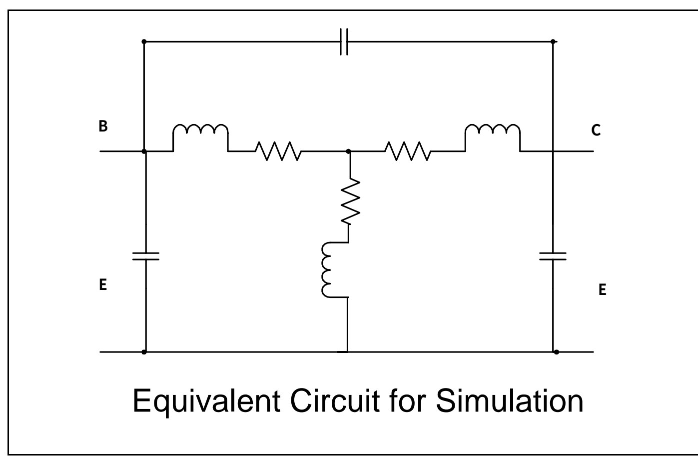


Fig. 5.22 S_{11} measurement (Red line) and simulation (Black line). Measured data was obtained from Short package TEG in Fig. 5.18. The parasitic inductance and resistance of the short package equivalent circuit was calculated by using measured *Z*-parameters with equation (5.38) in section 5.2. The frequency ranges for the measurement and the simulation are from 200 MHz to 5.1. GHz.

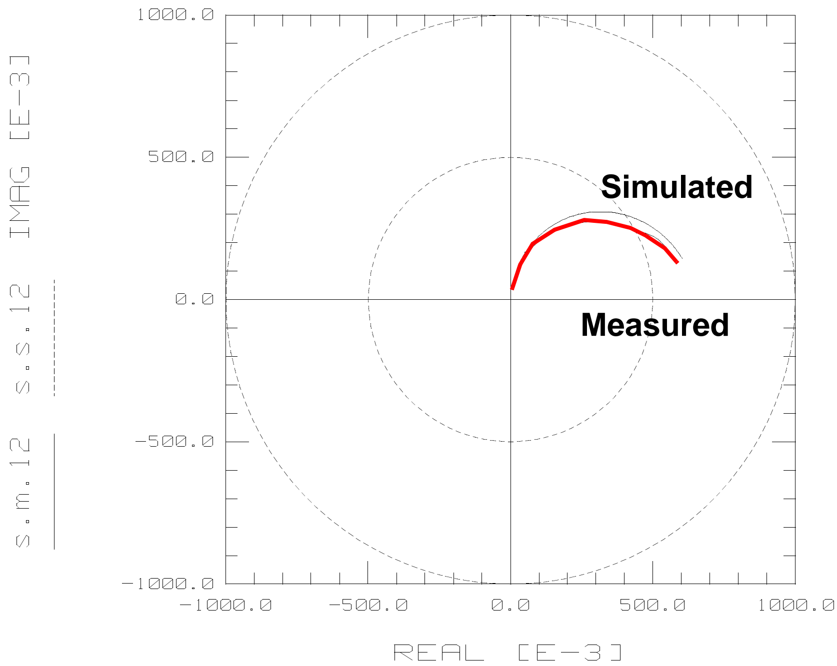


Fig. 5.23 S_{12} measurement (Red line) and simulation (Black line). Conditions are the same as Fig. 5.22.

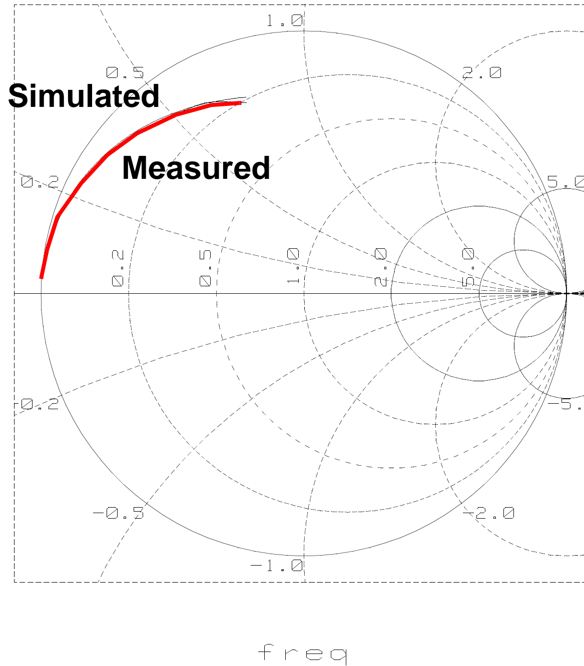
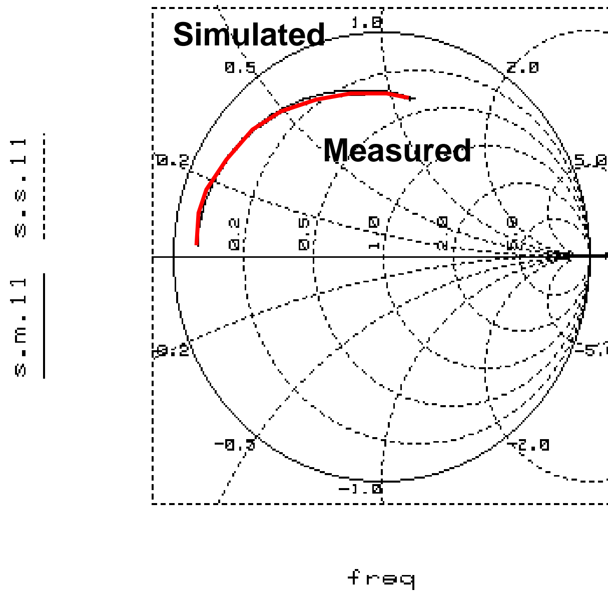


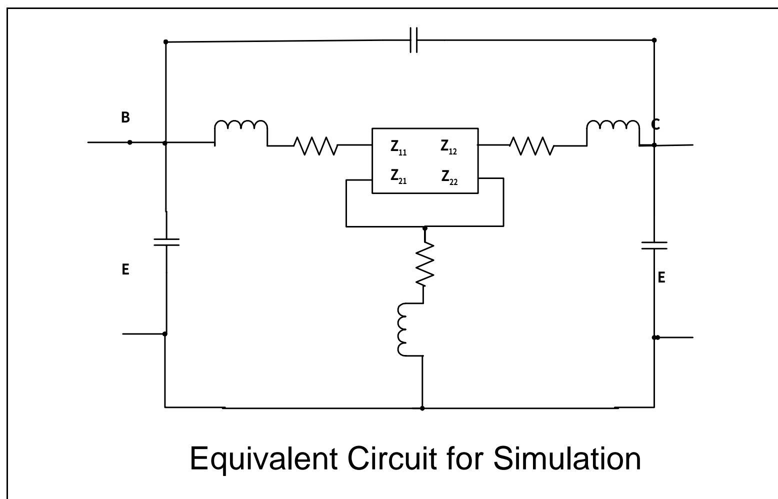
Fig. 5.24 S_{22} measurement (Red line) and simulation (Black line). Conditions are the same as Fig. 5.22.

5.4.2.3 Cold-chip measurement and simulation

Here, any small signal model parameters and internal parasitic elements of the Super-mini-mold chip BJT are extracted by using Cold-chip measurement and it related extraction methods described in section 5.3. All package parasitic elements before the Super-mini-mold chip BJT were de-embedded in advance. The Cold-chip measurement results and simulations whose equivalent circuit can be found in Fig. 5.9 are shown in Fig. 5.25 and Fig. 5.26.

Plot npn_dtc/coldchip/spar/s11 (On)





Equivalent Circuit for Simulation

Fig. 5.25 S_{11} measurement (Red line) and simulation (Black line). Measured data was obtained from chip BJT mounted on the test fixture in Fig. 5.18. The inductance and resistance of the BJT equivalent circuit in Fig. 5.9 was calculated by using measured *S*-parameters with the method described in section 5.3. The frequency ranges for the measurement and the simulation are from 200 MHz to 5.1 GHz.

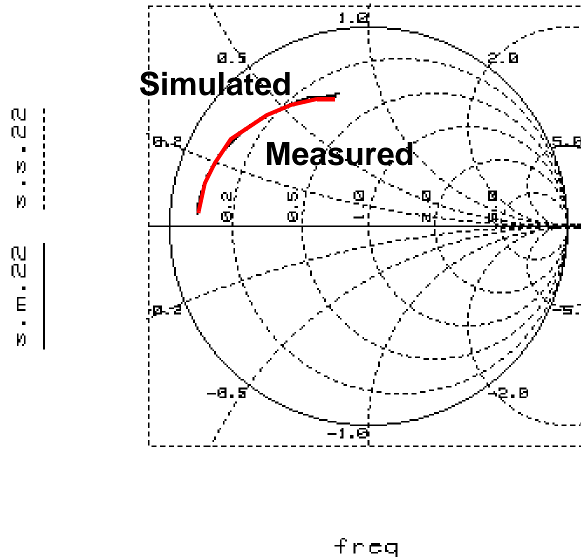
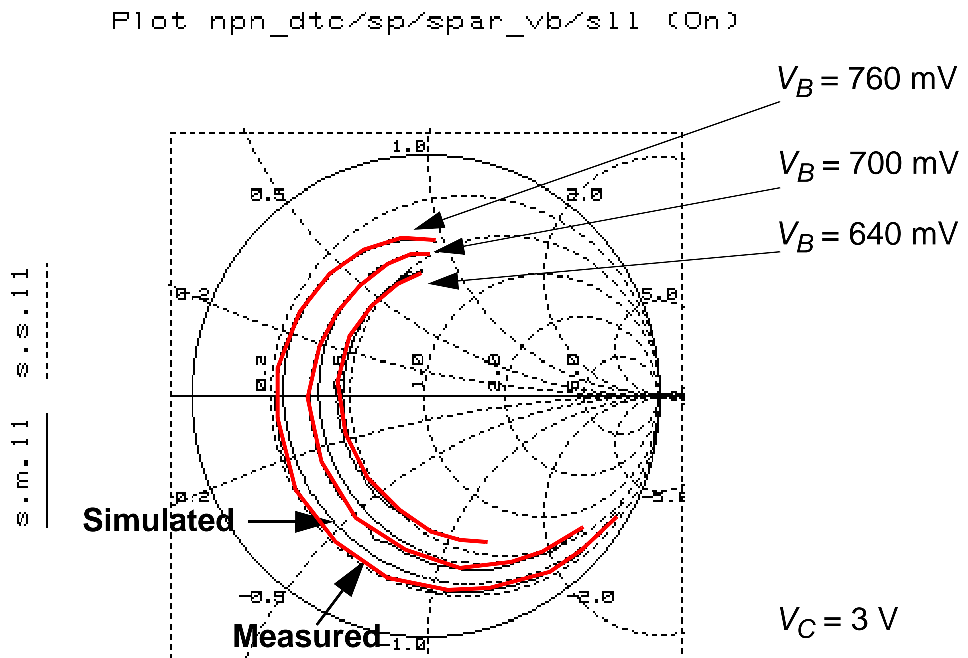


Fig. 5.26 S_{22} measurement (Red line) and simulation (Black line). Conditions are the same as Fig. 5.25.

5.4.2.4 Results measurement and simulation with all extracted model parameters and parasitics

Entire modeling procedure has been completed here. Measured *S*-parameters, that include all package and internal Super-mini-mold chip parasitic elements, and simulated *S*-parameters, whose equivalent circuit is the combination of Fig. 5.4 and Fig. 5.9, are compared in Fig. 5.27 through Fig. 5.30.



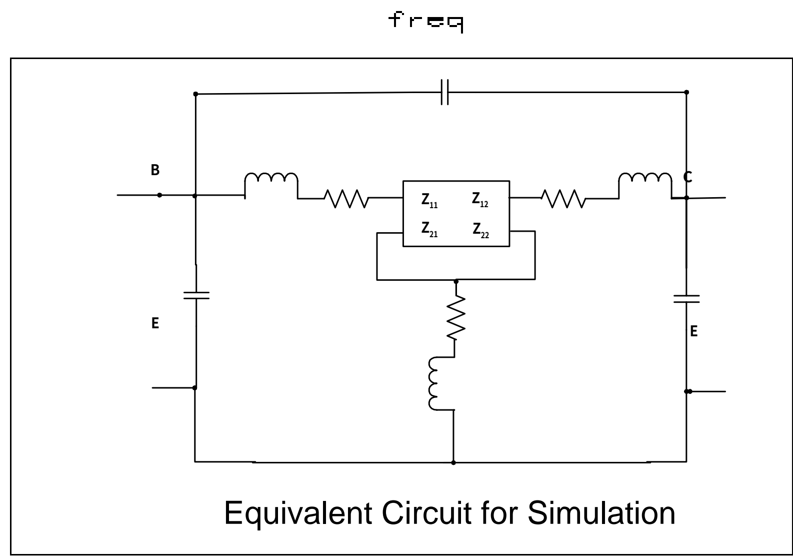


Fig. 5.27 Final S_{11} measurement (Red lines) and simulation (Black lines). Measured data was obtained from chip BJT mounted on the test fixture in Fig. 5.18. All small signal model parameters and parasitic elements were extracted. The frequency ranges for the measurement and the simulation are from 200 MHz to 5.1 GHz.

As shown in Fig. 5.27, good agreement between measured and simulated *S*-parameters are obtained. Since we did not extract bias dependent (large signal) base resistance model parameters, current where base resistance falls halfway to its minimum value, *IRB* and minimum base resistance at high current, *RBM*, of BJT Gummel-Poon model, the simulations at low base bias (V_B = 700 mV and 640 mV) ranges show relatively poor agreements.

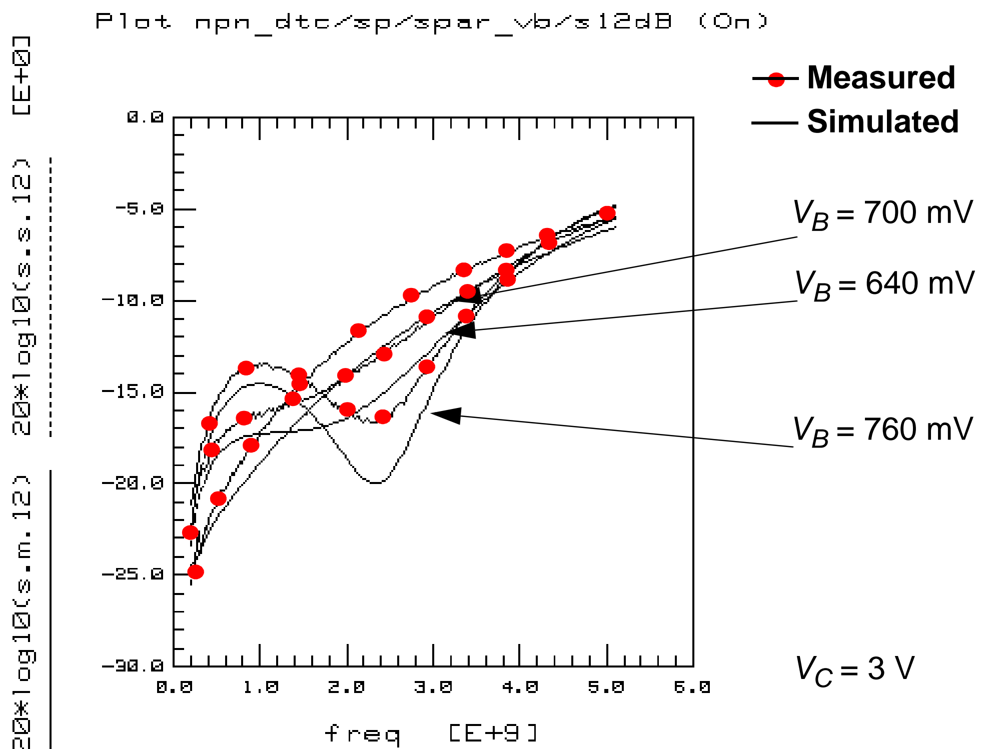


Fig. 5.28 Final S_{12} Measurement and simulation. Conditions are the same as Fig. 5.27.

Since S_{12} means reverse transmission characteristic of the BJT, it is usually very small, therefore, difficult to obtain reasonable agreements between measurement and simulation. However, Fig. 5.28 shows good result whose model parameters can be used for any circuit design projects.

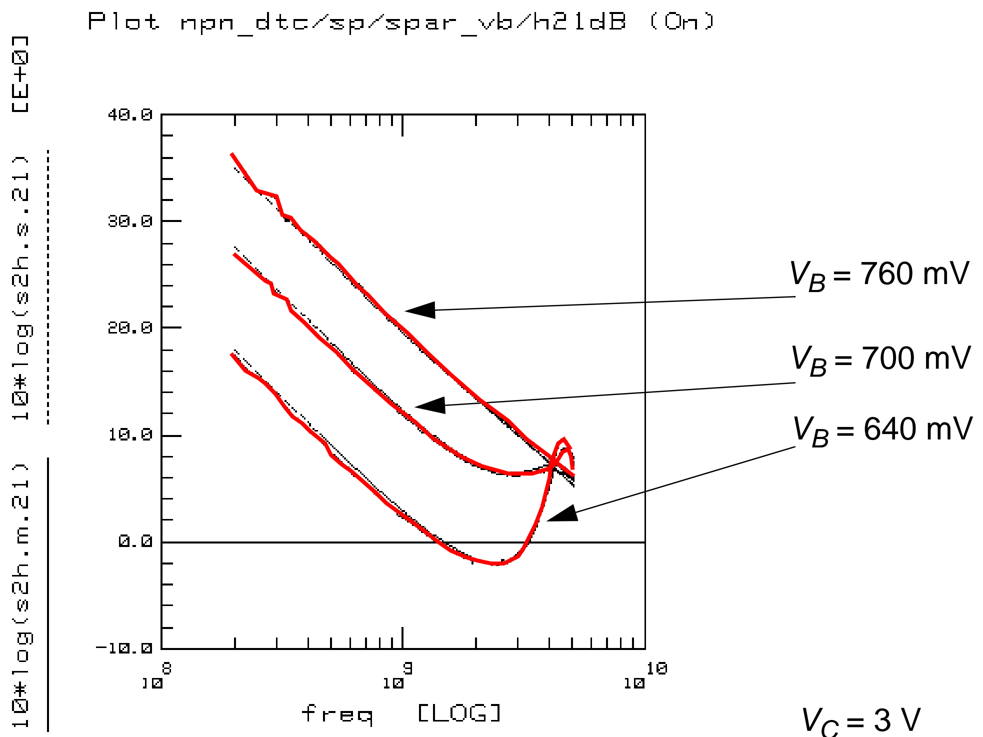


Fig. 5.29 Final H_{21} measurement (Red lines) and simulation (Black lines). Conditions are the same as Fig. 5.27.

Ac current gain characteristic, H_{21}, shows excellent agreement between measured and simulated curves. Because S_{21} and S_{12} strongly affect H_{21}, Fig. 5.29 can be a good reference plot to measure the modeling accuracies.

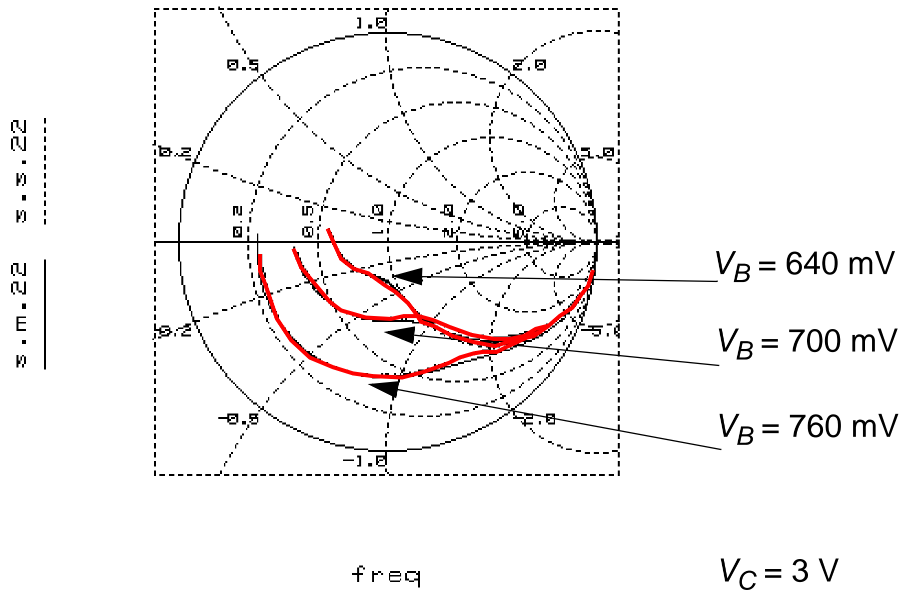


Fig. 5.30 Final S_{22} measurement (Red lines) and simulation (Black lines). Conditions are the same as Fig. 5.27.

Output refraction, S_{22}, also shows excellent agreements between measurement and simulation.

Based on the above verification procedures, the package parasitic elements collection that we mentioned have been certified.

5.5 Conclusions

A small signal modeling of packaged BJT was carried out up to 5 GHz. A new package parasitic de-embedding method had been presenting. Two types of BJT devices, which include TO-CAN package type (ft of about 1GHz) and super-mini-mold type (ft of about 10GHz), were adopted to verify the de-embedding method. The de-embedded S parameters of these two types of BJT's were confirmed by comparison with the simulation by SPICE. Also, the Cold-chip measurement technique was applied to the Super-mini-mold type BJT parameter and parasitic elements extractions. Since the number of applications of transistors in this frequency range is significant, the method is considered effective. If the user of this method prepares two empty packages, it is easy to form Open and Short samples.

There exist other transistors used into the microwave band greater than 5 GHz using a stripline-type package. In such cases, the parasitic capacitance elements of the bonding wire and the resistance element of the pad which were neglected in this paper must be considered. Even in such cases, it is not difficult to apply this method to more complicated equivalent circuits if they can be separated into type T and π circuits. Also, in the case of the strip-line, a distributed circuit modeling is needed as the lumped element model

would be insufficient. In the future, models and calibration methods that can cope with such a situation must be developed.

Chapter 6 Conclusions

Summary

So far, we have researched and developed new compact modeling with SPICE, especially for its model development and parameter extractions. There are many issues to be solved in order to use circuit simulators, effectively. Among them we focused four issues to improve recent circuit simulation environment. First was to develop and implement a new amorphous silicon thin-film-transistor device model. Second was to develop and enhance 1/f noise model for amorphous silicon thin-film-transistors (a-Si TFT) and MOSFET's. Third was to develop a de-embedding technique and extraction methods for a small signal equivalent circuit model of RF bipolar transistors. Finally, fourth was to develop macro models of TFT based active matrix liquid crystal displays.

In chapter 1 we have summarized significance of SPICE simulation and the key technologies and role and importance of device models in order to perform the circuit simulations, fast and accurately. Also, the selection of semiconductor device models and their interaction to device physics were confirmed.

In chapter 2 we newly developed and implemented an a-Si TFT model. The model equations are formulated based on device physics of a-Si TFT's and MOSFET models. Also, the equivalent circuit was assembled from the device structure. Both of drain current and capacitance models were optimized for better conversion. In addition, a liquid crystal capacitance model, which has frequency dependency, was developed by using empirical method for transient analysis of liquid crystal displays. The results a-Si TFT and capacitance models can be applied to optical characteristics of a-Si TFT based active matrix displays.

The model was adopted by Avant!'s H SPICE circuit simulator as MOSFET level 40 model and Agilent's IC-CAP software as HP ATFT model. They has been used by many TFT manufacturers mostly in Japan and in Europe.

In chapter 3, a macro modeling method for large circuit simulations were presented using TFT based liquid crystal displays. The macro model used the a-Si TFT and liquid crystal models that we mentioned in chapter 2. We researched pixel geometry scaling technology to simulate entire display pixels on time domain. Also, busline parasitic modeling was carefully analyzed. The simulation results showed excellent agreement with measurement.

In chapter 4, analysis of 1/f noises and development of flicker noise models for a-Si TFT and MOSFET's had been described. Flicker noise performance is important for low frequency circuit design. Therefore, its SPICE model should be accurate enough in all biases and all device geometries (for MOSFET's). The drain current flicker noise model for a-Si TFT's was based on experiments and UCB JFET model. The drain current flicker noise model for MOSFET's was an physics based analytical model, which has better bias dependency of frequency characteristic than conventional models. Also, the model is channel length and width dependent. We first discovered the channel width dependency which is completely different from existing theory at the time the model was developed.

The 1/f measurement system, which was developed in this research, has been adopted by Agilent and is used by many semiconductor and circuit manufacturers and universities in Japan.

Finally in chapter 5, a new package parasitic correction method was described using bipolar junction transistors as an instance. The method is a kind of de-embedding, therefore, consists with a small signal package parasitic model and extraction procedures. Because of the procedure, bipolar junction transistor's intrinsic part of the measured S-parameters can be

obtained. Two experiments were introduced to verify the procedures and the model.

These methods that are developed in this thesis have been widely used by various RF engineers with some modifications in the world.

In chapter 2, chapter 3, and chapter 4 we solved a-Si TFT modeling and their active matrix display simulation issues. The model included drain current, capacitance, flicker noise, frequency response, and transient simulation capabilities. The model was tuned and implemented into UCB SPICE3e2 for simulating TFT-LCD's. Since TFT-LCD's included huge number of a-Si TFT's, we also had researched and developed an effective simulation method based on macro models. In chapter 4, we solved flicker noise simulation issues in order to simulate jitter of a-Si TFT's on time domain and to simulate RF oscillators using n-MOSFET's. In chapter 5, we solved packaged parasitic issues for measuring and simulating BJT's. Using the parasitic correction procedures, the model parameters of BJT's were accurately extracted.

Throughout the entire discussion, we have reached the two common sense but important conclusions for developing compact models and their extraction methods as follows:

1. Compact models should have good convergence to simulate large circuits and in verious domain. To do so, complicated model physical equations that include many exponents and logarithmics should be replaced by simple mathematical functions such as Taylor expansion and polynominal equations.

2. Each model parameter should be independent in each operation region. To do so, the extracted parameters using the measured data in one particular region must be used in any other operation regions and simulation domains.

Perspective

There are several compact modeling issues to be researched and developed for improving circuit simulation environment. Generally speaking, it is

effective to decrease the number of model parameters in a compact model. In fact, models that device simulators have are physical enough not to use fitting parameters. As described in chapter 1, device simulators' models cannot be used in SPICE simulators since the simulation engine is different from SPICE simulators'. Though device simulators' simulation speed is very slow, the engine is not suitable for circuit simulation purposes. The models that we developed in this research have many empirical equations, the model parameters needed to be extracted by developing specific extraction functions and optimization procedures. As discussed in chapter 1, physical models are better for statistical analysis and process control monitor applications than empirical models. Also, the total number of fitting model parameters will be dramatically decreased.

For new compact semiconductor devices models that are lacked in any SPICE simulators, new structured device models, such as SOI (silicon on insulator) MOSFET, p-Si (poly silicon) TFT, HBT (Hetero bipolar transistor), and LD (lateral double diffusion) MOSFET, are needed for practical circuit design applications. Especially, physical analysis of these devices are also needed to develop physical models.

Because device size becomes smaller and circuit scale becomes larger, continuous research and development of compact modeling are necessary for future circuit simulations.

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